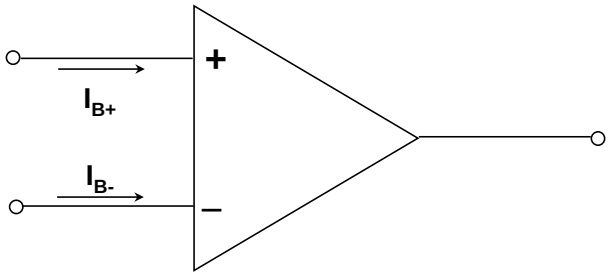
# Op Amp Input Bias Current

## DEFINITION OF INPUT BIAS CURRENT

Ideally, no current flows into the input terminals of an op amp. In practice, there are always two *input bias currents*, $I_{B+}$ and $I_{B-}$ (see Figure 1).




- **A very variable parameter!**
- **$I_B$ can vary from 60 fA (1 electron every 3 μs) to many μA, depending on the device.**
- **Some structures have well-matched $I_B$, others do not.**
- **Some structures' $I_B$ varies little with temperature, but a FET op amp's $I_B$ doubles with every 10°C rise in temperature.**
- **Some structures have $I_B$ which may flow in either direction.**

***Figure 1: Op Amp Input Bias Current***

Values of $I_B$ range from 60 fA (about one electron every three microseconds) in the AD549 electrometer, to tens of microamperes in some high speed op amps. Op amps with simple input structures using bipolar junction transistors (BJT) or FET long-tailed pair have bias currents that flow in one direction. More complex input structures (bias-compensated and current feedback op amps) may have bias currents that are the difference between two or more internal current sources, and may flow in either direction.

Bias current is a problem to the op amp user because it flows in external impedances and produces voltages, which add to system errors. Consider a non-inverting unity gain buffer driven from a source impedance of 1 MΩ. If $I_B$ is 10 nA, it will introduce an additional 10 mV of error. This degree of error is not trivial in any system.

Or, if the designer simply forgets about $I_B$ and uses capacitive coupling, the circuit won't work—at all! Or, if $I_B$ is low enough, it may work momentarily while the capacitor charges, giving even

more misleading results. The moral here is not to neglect the effects of $I_B$, in any op amp circuit. The same admonition goes for in-amp circuits.

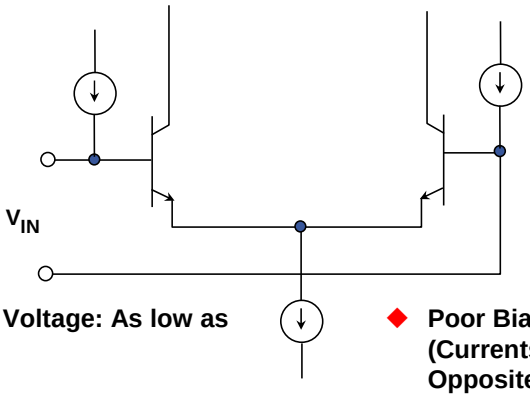
## INPUT OFFSET CURRENT

The *input offset current*, $I_{OS}$, is the difference between $I_{B-}$ and $I_{B+}$, or $I_{OS} = I_{B+} - I_{B-}$. Note also that $I_{OS}$ is only meaningful where the two individual bias currents are fundamentally reasonably well-matched, to begin with. This is true for most voltage feedback (VFB) op amps. However, it wouldn't for example be meaningful to speak of $I_{OS}$ for a current feedback (CFB) op amp, as the currents are radically un-matched.

It should be noted that rail-to-rail input stages comprised of two parallel stages have bias currents that change direction as the common-mode voltage passes through the transition region. Bias and offset currents for these devices are especially difficult to specify, other than simply giving a maximum positive/negative value.

## INTERNAL BIAS CURRENT CANCELLATION CIRCUITS

By providing this necessary bias currents via an internal current source, as in Figure 2 below, the only *external* current then flowing in the input terminals is the difference current between the base current and the current source, which can be quite small.




- **Low Offset Voltage: As low as 10µV**
- **Low Offset Drift: As low as 0.1µV/°C**
- **Temperature Stable $I_{bias}$**
- **Low Bias Currents: <0.5 - 10nA**
- **Low Voltage Noise: As low as 1nV/√Hz**
- **Poor Bias Current Match (Currents May Even Flow in Opposite Directions)**
- **Higher Current Noise**
- **Not Very Useful at HF**
- **Matching source impedances makes offset error due to bias current worse because of additional impedance**

***Figure 2: A Bias Current Compensated Bipolar Input Stage***

Most modern precision bipolar input stage op amps use some means of internal bias current compensation, examples would be the familiar OP07 and OP27 series.

Bias current compensated input stages have many of the good features of the simple bipolar input stage, namely: low voltage noise, low offset, and low drift. Additionally, they have low bias current which is fairly stable with temperature. However, their current noise is not very good, and their bias current matching is poor.

These latter two undesired side effects result from the external bias current being the *difference* between the compensating current source and the input transistor base current. Both of these currents inevitably have noise. Since they are uncorrelated, the two noises add in a root-sum-of-squares fashion (even though the dc currents subtract).
Since the resulting external bias current is the difference between two nearly equal currents, there is no reason why the net current should have a defined polarity. As a result, the bias currents of a bias-compensated op amp may not only be mismatched, they can actually flow in opposite directions! In most applications this isn't important, but in some it can have unexpected effects (for example the droop of a sample-and-hold (SHA) built with a bias-compensated op amp may have either polarity).

In many cases, the bias current compensation feature is not mentioned on an op amp data sheet, and a simplified schematic isn't supplied. It is easy to determine if bias current compensation is used by examining the bias current specification. If the bias current is specified as a "±" value, the op amp is most likely compensated for bias current. Note that this can easily be verified, by examining the *offset current* specification (the difference in the bias currents). If internal bias current compensation exists, the offset current will be of the same magnitude as the bias current. Without bias current compensation, the offset current will generally be at least a factor of 10 smaller than the bias current. Note that these relationships generally hold, regardless of the exact magnitude of the bias currents.

As previously mentioned, rail-to-rail input stages have bias currents that change direction as the common-mode voltage passes through the transition region. Bias and offset currents for these devices are especially difficult to specify, other than simply giving a maximum positive/negative value.

## CANCELING THE EFFECTS OF BIAS CURRENT (EXTERNAL TO THE OP AMP)

When the bias currents of an op amp are well matched (the case with simple bipolar input stage op amps, but *not* internally bias compensated ones, as noted previously), a bias compensation resistor, R3, (R3=R1||R2) introduces a voltage drop in the non-inverting input to match and thus compensate the drop in the parallel combination of R1 and R2 in the inverting input. This minimizes additional offset voltage error, as in Figure 3. Note that if R3 is more than 1 kΩ or so, it should be bypassed with a capacitor to prevent noise pickup. Also note that this form of bias cancellation is useless where bias currents are not well-matched, and will, in fact, make matters worse.

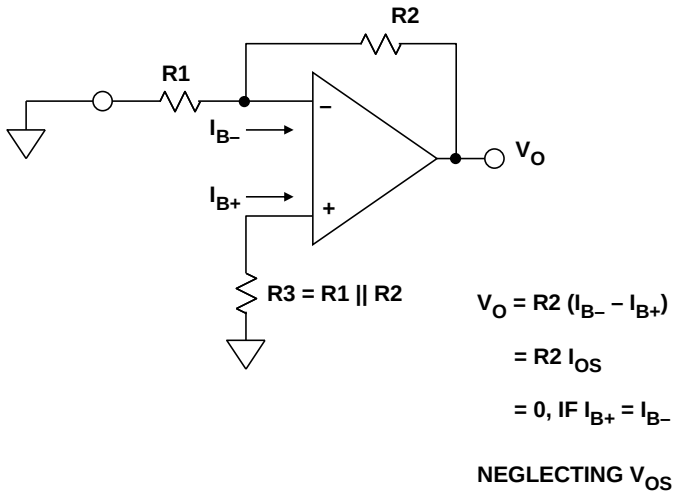
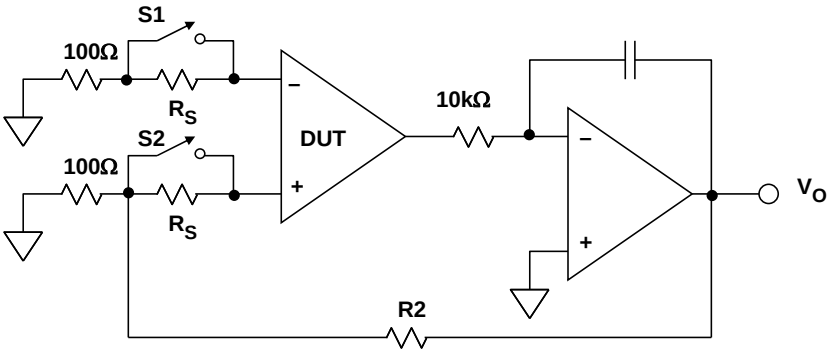



***Figure 3: Canceling the Effects of Input Bias Current within an Application***

## MEASURING INPUT OFFSET AND INPUT BIAS CURRENT

Input bias current (or input offset voltage) may be measured using the test circuit of Figure 4. To measure $I_B$, a large resistance, $R_S$, is inserted in series with the input under test, creating an apparent additional offset voltage equal to $I_B \times R_S$. If the actual $V_{OS}$ has previously been measured and recorded, the change in apparent $V_{OS}$ due to the change in $R_S$ can be determined, and $I_B$ is then easily computed. This yields values for $I_{B+}$ and $I_{B-}$. The rated value of $I_B$ is the average of the two currents, or $I_B = (I_{B+} + I_{B-})/2$.

Typical useful $R_S$ values vary from 100 kΩ for bipolar op amps to 1000 MΩ for some FET input devices.




$R_S >> 100\Omega$ (100kΩ TO 1GΩ)

S1 CLOSED TO TEST $I_{B+}$

S2 CLOSED TO TEST $I_{B-}$

BOTH CLOSED TO TEST $V_{OS}$

BOTH OPEN TO TEST $I_{OS}$

$$V_O = \left[1 + \frac{R2}{100}\right] V_{OS} + \left[1 + \frac{R2}{100}\right] I_{B+} R_S - \left[1 + \frac{R2}{100}\right] I_{B-} R_S$$

***Figure 4: Measuring Input Bias Current***

Extremely low input bias currents must be measured by integration techniques. The bias current in question is used to charge a capacitor, and the rate of voltage change is measured. If the capacitor and general circuit leakage is negligible (this is very difficult for currents under 10 fA), the current may be calculated directly from the rate of change of the output of the test circuit. Figure 5 below illustrates the general concept. With one switch open and the opposite closed, either $I_{B+}$ or $I_{B-}$ is measured.

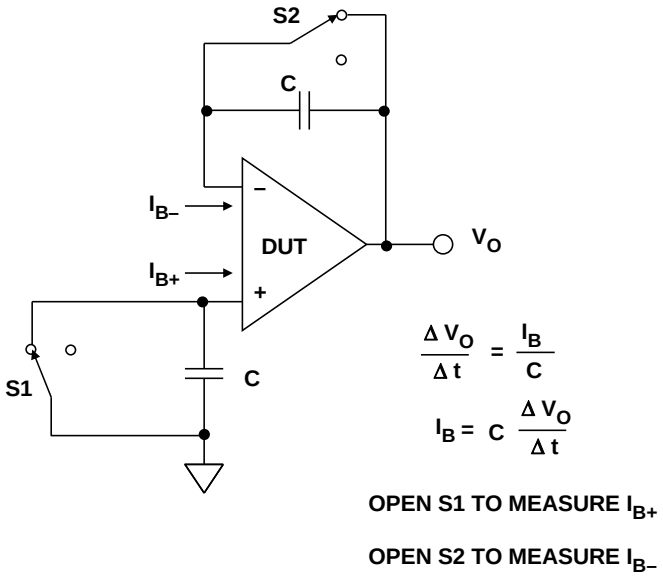



***Figure 5: Measuring Very Low Bias Currents***

It should be obvious that only a premium capacitor dielectric can be used for C, for example Teflon or polypropylene types.

## REFERENCES:


1. Hank Zumbahlen, *Basic Linear Design*, Analog Devices, 2006, ISBN: 0-915550-28-1. Also available as *Linear Circuit Design Handbook*, Elsevier-Newnes, 2008, ISBN-10: 0750687037, ISBN-13: 978-0750687034. Chapter 1.

2. Walter G. Jung, *Op Amp Applications*, Analog Devices, 2002, ISBN 0-916550-26-5, Also available as *Op Amp Applications Handbook*, Elsevier/Newnes, 2005, ISBN 0-7506-7844-5. Chapter 1.
3.