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Low-Jitter, 800Mbps, 10-Port LVDS Repeaters with 100Ω Drive

MAX9153/MAX9154

General Description

The MAX9153/MAX9154 low-jitter, low-voltage differential signaling (LVDS) repeaters are ideal for applications that require high-speed data or clock distribution while minimizing power, space, and noise. The devices accept a single LVDS input (MAX9153) or single LVPECL input (MAX9154) and repeat the signal at 10 LVDS outputs. Each differential output drives 100Ω, allowing point-to-point distribution of signals on transmission lines with 100Ω termination at the receiver input.

Ultra-low 90ps_{p-p} (max) added deterministic jitter and 1ps_{RMS} (max) added random jitter ensure reliable communication in high-speed links that are highly sensitive to timing error, especially those incorporating clock-and-data recovery or serializers and deserializers. The high-speed switching performance guarantees 800Mbps data rate and less than 60ps (max) skew between channels while operating from a single +3.3V supply.

Supply current at 800Mbps is 118mA and reduces to 2μA in power-down mode. LVDS inputs and outputs conform to the ANSI/EIA/TIA -644 standard. A fail-safe feature on the MAX9153 sets the output high when the input is undriven and open, terminated, or shorted. The MAX9153/MAX9154 are available in a 28-pin TSSOP package and are specified for the -40°C to +85°C extended temperature range.

Refer to the MAX9150 data sheet for a pin-compatible 10-port LVDS repeater capable of driving a double-terminated (50Ω) LVDS link.

Refer to the MAX9110/MAX9112 and MAX9111/MAX9113 data sheets for LVDS line drivers and receivers.

Applications

- Cellular Phone Base-Station
- Add/Drop Muxes
- Digital Cross-Connects
- Network Switches/Routers
- Backplane Interconnect
- Clock Distribution

Features

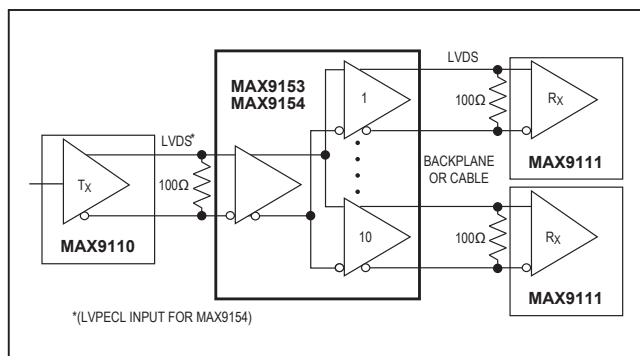
- Ultra-Low 90ps_{p-p} (max) Added Deterministic Jitter at 800Mbps (2²³-1) PRBS Pattern
- 1ps_{RMS} (max) Added Random Jitter
- 60ps (max) Skew Between Channels
- Guaranteed 800Mbps Data Rate
- LVDS (MAX9153) or LVPECL (MAX9154) Input Versions
- Fail-Safe Circuit Sets Output High for Undriven Inputs (MAX9153)
- High-Impedance Differential Input when V_{CC} = 0
- 2μA Power-Down Supply Current
- Conforms to ANSI/EIA/TIA-644 LVDS Standard
- Pin-Compatible Upgrade to DS90LV110

Ordering Information

PART	TEMP. RANGE	PIN-PACKAGE	INPUT
MAX9153EUI+	-40°C to +85°C	28 TSSOP	LVDS
MAX9154EUI+	-40°C to +85°C	28 TSSOP	LVPECL

Note: +Denotes a lead(Pb)-free/RoHS-compliant package.

Typical Application Circuit



Pin Configuration appears at end of data sheet.

19-2167; Rev 1; 5/25

Absolute Maximum Ratings

V_{CC} to GND -0.3V to +4.0V
 $RIN+$, $RIN-$ to GND -0.3V to +4.0V
 \overline{PWRDN} to GND -0.3V to ($V_{CC} + 0.3V$)
 $DO+$, $DO-$ to GND -0.3V to +4.0V
 Short-Circuit Duration ($DO+$, $DO-$) Continuous
 Continuous Power Dissipation ($T_A = +70^\circ\text{C}$)
 28-Pin TSSOP (derate 12.8mW/ $^\circ\text{C}$ above $+70^\circ\text{C}$) 1026mW

Storage Temperature -65°C to $+150^\circ\text{C}$
 Maximum Junction Temperature $+150^\circ\text{C}$
 Operating Temperature Range -40°C to $+85^\circ\text{C}$
 ESD Protection
 Human Body Model ($RIN+$, $RIN-$, $DO+$, $DO-$) $\pm 8\text{kV}$
 Lead Temperature (soldering, 10s) $+300^\circ\text{C}$

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC Electrical Characteristics

($V_{CC} = +3.0V$ to $+3.6V$, $R_L = 100\Omega \pm 1\%$, differential input voltage $|V_{ID}| = 0.05V$ to $1.2V$, MAX9153 LVDS input common-mode voltage $V_{CM} = |V_{ID}|/2$ to $2.4V - |V_{ID}|/2$, MAX9154 LVPECL input voltage range = 0 to V_{CC} , $\overline{PWRDN} = \text{high}$, $T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$, unless otherwise noted. Typical values are at $V_{CC} = +3.3V$, $|V_{ID}| = 0.2V$, $V_{CM} = 1.2V$, $T_A = +25^\circ\text{C}$.) (Notes 1 and 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
CONTROL INPUT (\overline{PWRDN})						
Input High Voltage	V_{IH}		2.0		V_{CC}	V
Input Low Voltage	V_{IL}		GND		0.8	V
Input Current	I_{IN}	$\overline{PWRDN} = \text{high or low}$	-20		20	μA
DIFFERENTIAL INPUT ($RIN+$, $RIN-$)						
Differential Input High Threshold	V_{TH}			-3	50	mV
Differential Input Low Threshold	V_{TL}		-50	-3		mV
Input Current (MAX9153)	I_{RIN+} , I_{RIN-}	$0.05V \leq V_{ID} \leq 0.6V$, $\overline{PWRDN} = \text{high or low}$ (Figure 1)	-15	-3	15	μA
		$0.6V < V_{ID} \leq 1.2V$, $\overline{PWRDN} = \text{high or low}$ (Figure 1)	-20	-4	20	
Power-Off Input Current (MAX9153)	$I_{RIN+}(\text{OFF})$, $I_{RIN-}(\text{OFF})$	$0.05V \leq V_{ID} \leq 0.6V$, $V_{CC} = 0$ or open, $\overline{PWRDN} = 0$ or open (Figure 1)	-15	3	15	μA
		$0.6V < V_{ID} \leq 1.2V$, $V_{CC} = 0$ or open, $\overline{PWRDN} = 0$ or open (Figure 1)	-20	4	20	
Input Resistor 1 (MAX9153)	R_{IN1}	$\overline{PWRDN} = \text{high or low}$ (Figure 1)	103			kΩ
		$V_{CC} = 0$ or open, $\overline{PWRDN} = 0$ or open (Figure 1)	103			
Input Resistor 2 (MAX9153)	R_{IN2}	$\overline{PWRDN} = \text{high or low}$ (Figure 1)	154			kΩ
		$V_{CC} = 0$ or open, $\overline{PWRDN} = 0$ or open (Figure 1)	154			
Input Current (MAX9154)	I_{RIN+} , I_{RIN-}	$V_{RIN+} = 3.6V$, $V_{RIN-} = 3.6V$ or 0, $\overline{PWRDN} = \text{high or low}$ (Figure 2)	-10	3	10	μA
		$V_{RIN+} = 0$, $V_{RIN-} = 3.6V$ or 0, $\overline{PWRDN} = \text{high or low}$ (Figure 2)	-10	± 3	10	
Power-Off Input Current (MAX9154)	$I_{RIN+}(\text{OFF})$, $I_{RIN-}(\text{OFF})$	$V_{RIN+} = 3.6V$, $V_{RIN-} = 0$, $V_{CC} = 0$ or open, $\overline{PWRDN} = 0$ or open (Figure 2)	-10	3	10	μA
		$V_{RIN+} = 0$, $V_{RIN-} = 3.6V$, $V_{CC} = 0$ or open, $\overline{PWRDN} = 0$ or open (Figure 2)	-10	3	10	

Electrical Characteristics (continued)

($V_{CC} = +3.0V$ to $+3.6V$, $R_L = 100\Omega \pm 1\%$, differential input voltage $|V_{ID}| = 0.05V$ to $1.2V$, MAX9153 LVDS input common-mode voltage $V_{CM} = |V_{ID}|/2$ to $2.4V - |V_{ID}|/2$, MAX9154 LVPECL input voltage range = 0 to V_{CC} , $\overline{PWRDN} = \text{high}$, $T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$, unless otherwise noted. Typical values are at $V_{CC} = +3.3V$, $|V_{ID}| = 0.2V$, $V_{CM} = 1.2V$, $T_A = +25^\circ\text{C}$.) (Notes 1 and 2)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Input Resistor 3 (MAX9154)	R _{IN3}	PWRDN = high or low (Figure 2)		360			kΩ
		V _{CC} = 0 or open, PWRDN = 0 or open (Figure 2)		360			
LVDS OUTPUT (DO ₊ , DO ₋)							
Differential Output Voltage	V _{OD}	Figure 3		250	380	450	mV
Charge in V _{OD} Between Complementary Output States	ΔV _{OD}	Figure 3			1	25	mV
Offset (Common-Mode) Voltage	V _{OS}	Figure 3		1.125	1.26	1.375	V
Change in V _{OS} Between Complementary Output States	ΔV _{OS}	Figure 3			3	25	mV
Output High Voltage	V _{OH}	Figure 3				1.6	V
Output Low Voltage	V _{OL}	Figure 3		0.9			V
Differential Output Resistance	R _{ODIFF}	PWDRN = high or low		150	238	330	Ω
		V _{CC} = 0 PWRDN = 0 or open					
Differential High Output Voltage in Fail-Safe	V _{OD+}	R _{IN+} , R _{IN-} undriven with short, open, or 100Ω termination (MAX9153)		250		450	mV
		R _{IN+} , R _{IN-} open (MAX9154)		250		450	
Single-Ended Output Short-Circuit Current	I _{OZ}	PWDRN = low; V _{DO+} = 3.6V or 0, DO ₋ + open; or V _{DO-} = 3.6V or 0, DO ₊ = open		-1		1	μA
		V _{CC} = 0, PWRDN = 0 or open; V _{DO+} = 3.6V or 0, DO ₋ = 3.6V or V _{DO-} = 3.6V or 0, DO ₊ = open		-1		1	
Single-Ended Output Short-Circuit Current	I _{OS}	V _{ID} = +50mV, V _{DO+} = 0 or V _{CC} , V _{DO-} = 0 or V _{CC}		-15		15	mA
		V _{ID} = -50mV, V _{DO+} = 0 or V _{CC} , V _{DO-} = 0 or V _{CC}					
Differential Output Short-Circuit Current (Note 3)	I _{OSD}	V _{ID} = +50mV, V _{OD} = 0		-15		15	mA
		V _{ID} = -50mV, V _{OD} = 0					
SUPPLY							
Supply Current	I _{CC}	DC, R _L = 100Ω (Figure 4)			70	95	mA
		200MHz (400Mbps), R _L = 100Ω	Figure 4 (Note 3)		90	115	
		400MHz (800Mbps), R _L = 100Ω			118	145	
Power-Down Supply Current	I _{CCZ}	PWDRN = low			2	20	μA

AC Electrical Characteristics

($V_{CC} = +3.0V$ to $+3.6V$, $R_L = 100\Omega \pm 1\%$, $C_L = 5pF$, differential input voltage $|V_{ID}| = 0.15V$ to $1.2V$, MAX9153 LVDS input commonmode voltage $V_{CM} = |V_{ID}|/2$ to $2.4V - |V_{ID}|/2$, MAX9154 LVPECL input voltage range = 0 to V_{CC} , $PWRDN = \text{high}$, $T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$, unless otherwise noted. Typical values are at $V_{CC} = +3.3V$, $|V_{ID}| = 0.2V$, $V_{CM} = 1.2V$, $T_A = +25^\circ\text{C}$.) (Notes 3, 4, 5)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Rise Time	t_{LHT}	Figures 4, 5		150	220	450	ps
Fall Time	t_{HLT}			150	220	450	ps
Added Deterministic Jitter (Note 6)	t_{DJ}	$V_{ID} = 200mV$, 2 ²³ - 1 PRBS data, $V_{CM} = 1.2V$	400Mbps (NRZ)	13	50		ps (p-p)
			800Mbps (NRZ)	24	90		
Added Random Jitter (Note 6)	t_{RJ}	$V_{ID} = 200mV$, 50% duty cycle input, $V_{CM} = 1.2V$	200MHz		1		ps (RMS)
			400MHz		1		
Differential Propagation Delay Low to High	t_{PLHD}	Figures 4, 5		1.6	2.3	3.3	ns
Differential Propagation Delay High to Low	t_{PHLD}			1.6	2.3	3.3	
Pulse Skew $t_{PLHD} - t_{PHLD}$	t_{SKEW}	Figures 4, 5			27	80	ps
Channel-to-Channel Skew (Note 7)	t_{CCS}	Figures 4, 5			35	60	ps
Differential Part-to-Part Skew 1 (Note 8)	t_{PPS1}	Figures 4, 5		1.2			ns
Differential Part-to-Part Skew 2 (Note 9)	t_{PPS2}			1.7			ns
Maximum Input Frequency (Note 10)	f_{MAX}	Figures 4, 5		800			Mbps
Power-Down Time	t_{PD}	Figures 6, 7		10	20		ns
Power-Up Time	t_{PU}			20	40		μs

Note 1: Current into a pin is defined as positive. Current out of a pin is defined as negative. All voltages are referenced to ground except V_{TH} , V_{TL} , V_{ID} , V_{OD} , and ΔV_{OD} .

Note 2: Maximum and minimum limits over temperature are guaranteed by design and characterization. Devices are production tested at $T_A = +25^\circ\text{C}$.

Note 3: Guaranteed by design and characterization.

Note 4: C_L includes scope probe and test jig capacitance.

Note 5: Signal generator conditions unless otherwise noted: frequency = 400MHz, 50% duty cycle, $R_O = 50\Omega$, $t_R = 0.6ns$, and $t_F = 0.6ns$ (0% to 100%).

Note 6: Device jitter added to the input signal.

Note 7: t_{CCS} is the magnitude difference in differential propagation delay between outputs for a same-edge transition.

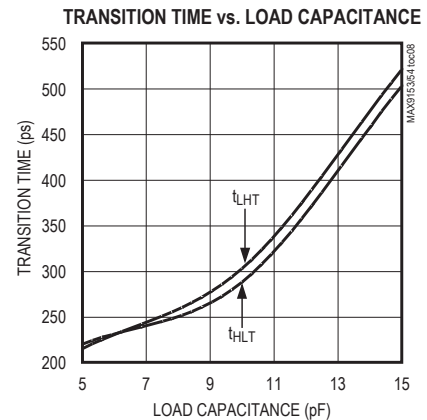
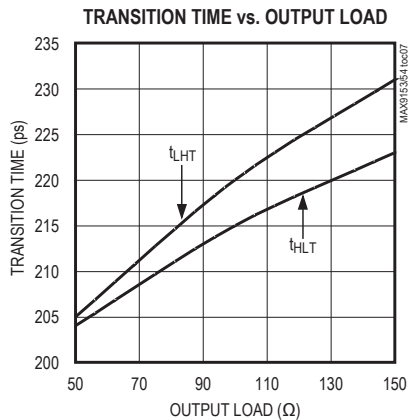
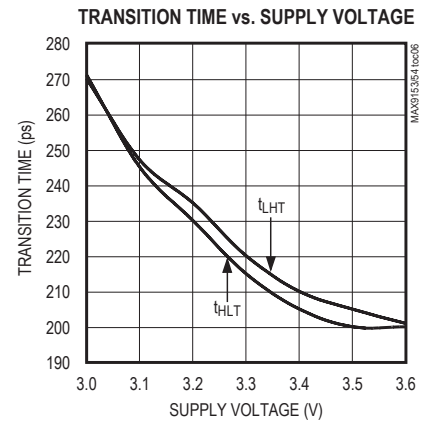
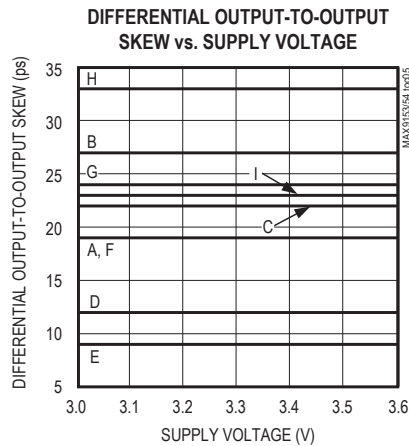
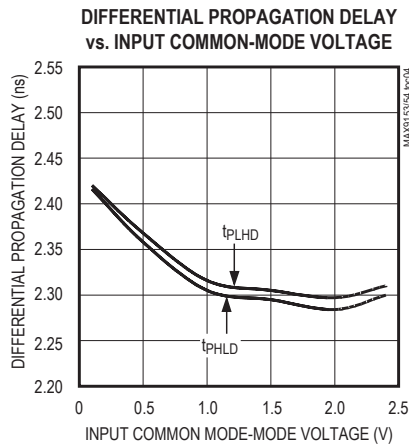
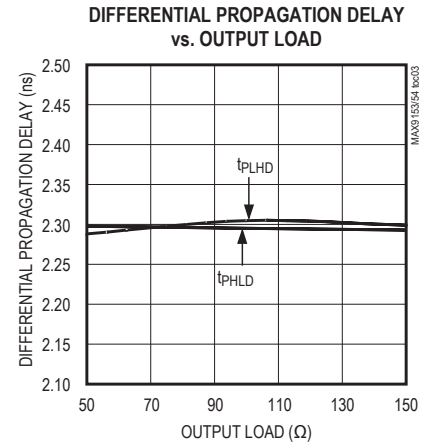
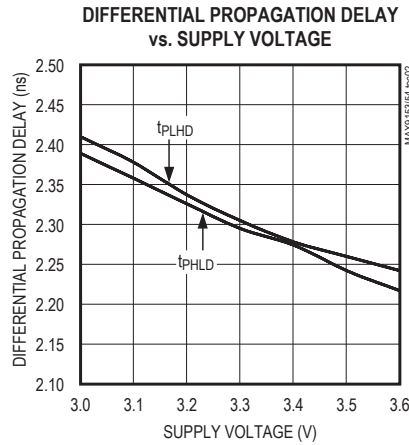
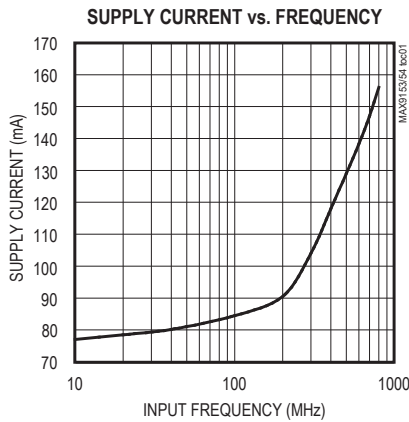
Note 8: t_{PPS1} is the magnitude difference of any differential propagation delays between devices operating over rated conditions at the same supply voltage, input conditions, and ambient temperature.

Note 9: t_{PPS2} is the magnitude difference of any differential propagation delays between devices operating over rated conditions.

Note 10: Device meets V_{OD} DC specification, and AC specifications while operating at f_{MAX} .

Typical Operating Characteristics

($V_{CC} = +3.3V$, $R_L = 100\Omega$, $C_L = 5pF$, $|V_{ID}| = 200mV$, $V_{CM} = 1.2V$, $f_{IN} = 200MHz$, $T_A = +25^\circ C$, unless otherwise noted.)

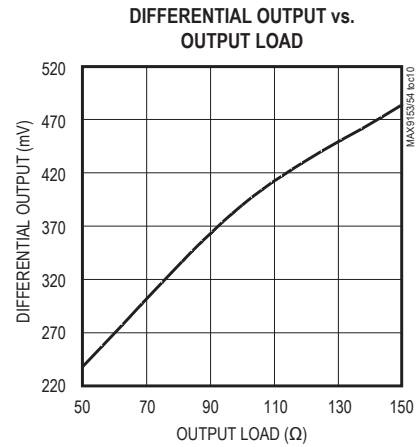
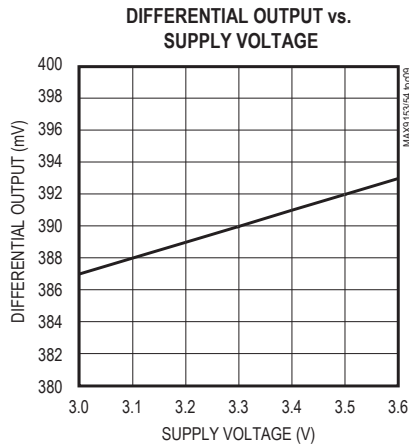


SUPPLY VOLTAGE (V)

A = D05 - D01 B = D05 - D02
C = D05 - D03 D = D05 - D04
E = D05 - D06 F = D05 - D07
G = D05 - D08 H = D05 - D09
I = D05 - D010

Typical Operating Characteristics (continued)

($V_{CC} = +3.3V$, $R_L = 100\Omega$, $C_L = 5pF$, $|V_{ID}| = 200mV$, $V_{CM} = 1.2V$, $f_{IN} = 200MHz$, $T_A = +25^\circ C$, unless otherwise noted.)



Pin Description

PIN	NAME	FUNCTION
1, 3, 11, 13, 16, 18, 20, 24, 26, 28	DO2+, DO1+, DO10+, DO9+, DO8+, DO7+, DO6+, DO5+, DO4+, DO3+	Differential LVDS Outputs
2, 4, 12, 14, 15, 17, 19, 23, 25, 27	DO2-, DO1-, DO10-, DO9-, DO8-, DO7-, DO6-, DO5-, DO4-, DO3-	
5	\overline{PWRDN}	Power Down. Drive \overline{PWRDN} low to disable all outputs and reduce supply current to 2μA. Drive \overline{PWRDN} high for normal operation.
6, 9, 21	GND	Ground
10, 22	V_{CC}	Power. Bypass each V_{CC} pin to GND with 0.1μF and 1nF ceramic capacitors.
7	RIN+	LVDS (MAX9153) or LVPECL (MAX9154) Differential Inputs. RIN+ and RIN- are high-impedance inputs. Connect a resistor from RIN+ to RIN- to terminate the input signal.
8	RIN-	

Detailed Description

LVDS is a signaling method for point-to-point data communication over a controlled-impedance medium as defined by the ANSI/TIA/EIA-644 and IEEE 1596.3 standards. LVDS uses a lower voltage swing than other common communication standards, achieving higher data rates with reduced power consumption, while reducing EMI emissions and system susceptibility to noise.

The MAX9153/MAX9154 are 800Mbps, 10-port repeaters for high-speed, point-to-point, low-power applications. The MAX9153 accepts an LVDS input and has a fail-safe

input circuit. The MAX9154 accepts an LVPECL input. Both devices repeat the input at 10 LVDS outputs. The devices detect differential signals as low as 50mV and as high as 1.2V within the 0 to 2.4V input voltage range as specified in the LVDS standards.

The MAX9153/MAX9154 outputs use a current-steering configuration to generate a 2.5mA to 4.5mA output current. This current-steering approach induces less ground bounce and no shoot-through current, enhancing noise margin and system speed performance. The outputs are short-circuit current limited and are high impedance

MAX9153/MAX9154

(to ground) when $\overline{\text{PWRDN}}$ = low or the device is not powered. The outputs have a typical differential resistance of 238Ω. The internal differential output resistance terminates induced noise and reflections from the primary termination located at the LVDS receiver.

The MAX9153/MAX9154 current-steering output requires a resistive load to terminate the signal and complete the transmission loop. Because the devices switch the direction of current flow and not voltage levels, the output voltage swing is determined by the value of the termination resistor multiplied by the output current. With a typical 3.8mA output current, the MAX9153/MAX9154 produce a 380mV output voltage when driving a transmission line terminated with a 100Ω resistor ($3.8\text{mA} \times 100\Omega = 380\text{mV}$). Logic states are determined by the direction of current flow through the termination resistor.

Table 1. Input/Output Function Table

INPUT, V_{ID}		OUTPUTS, V_{OD}
+50mV	MAX9153 MAX9154	High
-50mV		Low
Open		High
Undriven short	MAX9153	High
Undriven terminated	MAX9153	High

Note: $V_{ID} = R_{IN+} - R_{IN-}$, $V_{OD} = DO_{+} - DO_{-}$
 High = $450\text{mV} > V_{OD} > 250\text{mV}$
 Low = $-250\text{mV} > V_{OD} > -450\text{mV}$

Fail-Safe

The fail-safe feature of the MAX9153 sets the outputs high when the differential input is:

- Open
- Undriven and shorted
- Undriven and terminated

Without a fail-safe circuit, when the input is undriven, noise at the input may switch the outputs and it may appear to the system that data is being sent. Open or undriven terminated input conditions can occur when a cable is disconnected or cut, or when an LVDS driver output is in high impedance. A shorted input can occur because of a cable failure.

When the input is driven with signals meeting the LVDS standard, the input common-mode voltage is less than $V_{CC} - 0.3\text{V}$ and the fail-safe circuit is not activated. If the

Low-Jitter, 800Mbps, 10-Port LVDS Repeaters with 100Ω Drive

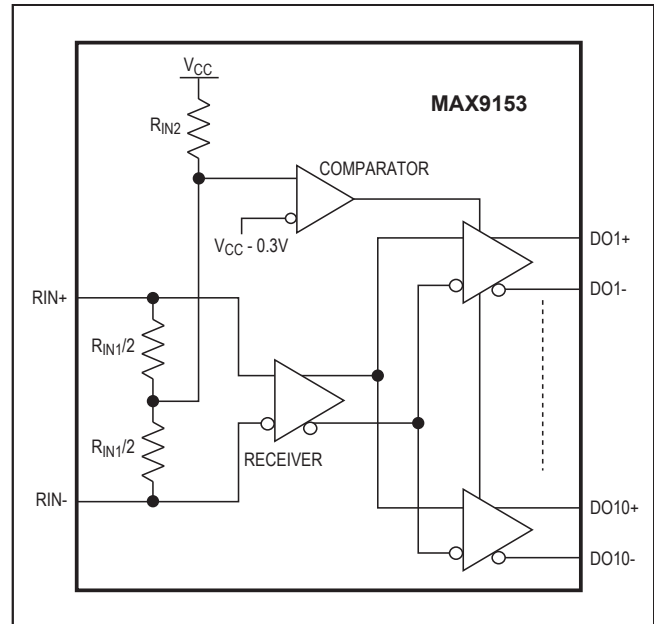


Figure 1. MAX9153 Input Fail-Safe Circuit

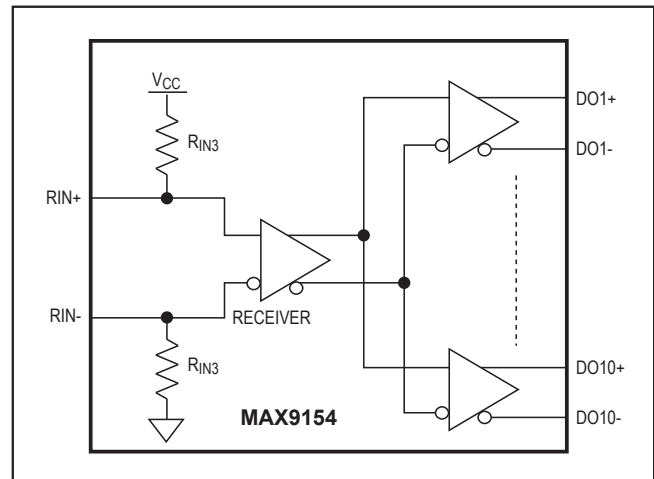


Figure 2. MAX9154 Input Bias Resistors

input is open, undriven and shorted, or undriven and parallel terminated, an internal resistor in the fail-safe circuit pulls both inputs above $V_{CC} - 0.3\text{V}$, activating the fail-safe circuit and forcing the outputs high (Figure 1).

The MAX9154 is essentially the MAX9153 without the fail-safe circuit. The MAX9154 accepts input voltages from 0 to V_{CC} (vs. 0 to 2.4V for the MAX9153), which allows interfacing to LVPECL input signals while retaining a good common-mode tolerance.

Applications Information

Supply Bypassing

Bypass each V_{CC} with high-frequency surface-mount ceramic 0.1μF and 1nF capacitors in parallel as close to the device as possible, with the smaller value capacitor closest to the V_{CC} pin.

Traces, Cables, and Connectors

The characteristics of input and output connections affect the performance of the MAX9153/MAX9154. Use controlled-impedance traces, cables, and connectors with matched characteristic impedance.

Ensure that noise couples as common mode by running the traces of a differential pair close together. Reduce within-pair skew by matching the electrical length of the traces of a differential pair. Excessive skew can result in a degradation of magnetic field cancellation. Maintain the distance between traces of a differential pair to avoid discontinuities in differential impedance. Minimize the number of vias to further prevent impedance discontinuities.

Avoid the use of unbalanced cables, such as ribbon cable. Balanced cables, such as twisted pair, offer superior signal quality and tend to generate less EMI due to canceling effects. Balanced cables tend to pick up noise as common mode, which is rejected by the LVDS receiver.

Termination

The MAX9153/MAX9154 are specified for 100Ω differential characteristic impedance but can operate with 90Ω to 132Ω to accommodate various types of interconnect. The termination resistor should match the differential characteristic impedance of the interconnect and be located close to the LVDS receiver input. Use a ±1% surface-mount termination resistor.

The output voltage swing is determined by the value of the termination resistor multiplied by the output current. With a typical 3.8mA output current, the MAX9153/MAX9154 produce a 380mV output voltage when driving a transmission line terminated with a 100Ω resistor ($3.8\text{mA} \times 100\Omega = 380\text{mV}$).

Chip Information

TRANSISTOR COUNT: 1394

PROCESS: CMOS

Test Circuits and Timing Diagrams

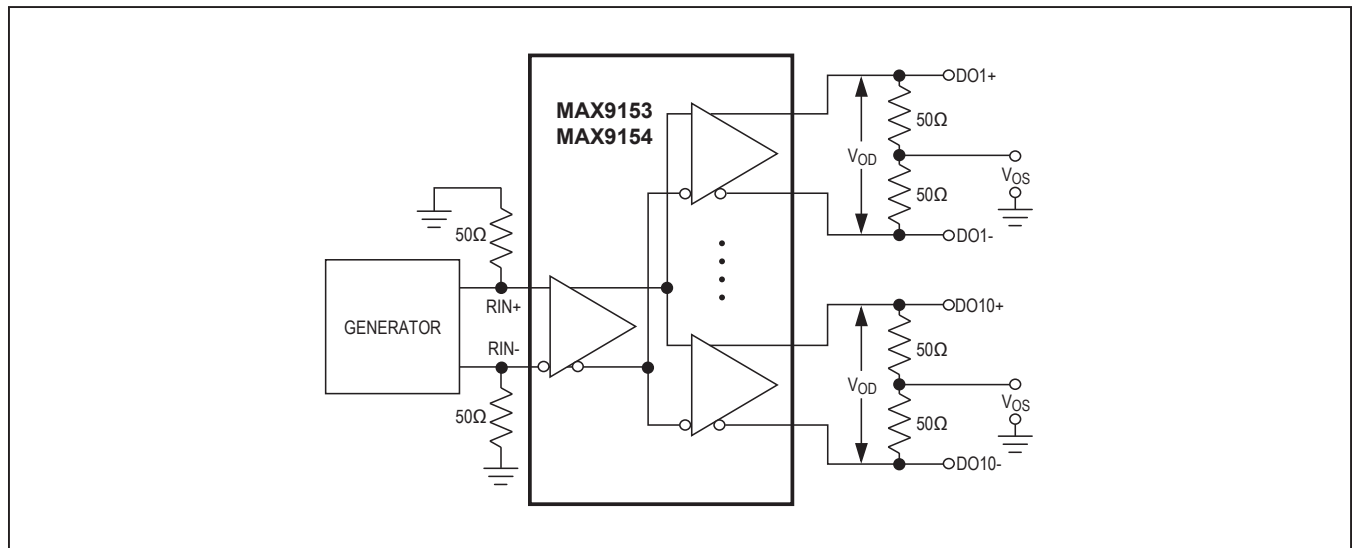


Figure 3. Driver-Load Test Circuit

Test Circuits and Timing Diagrams (continued)

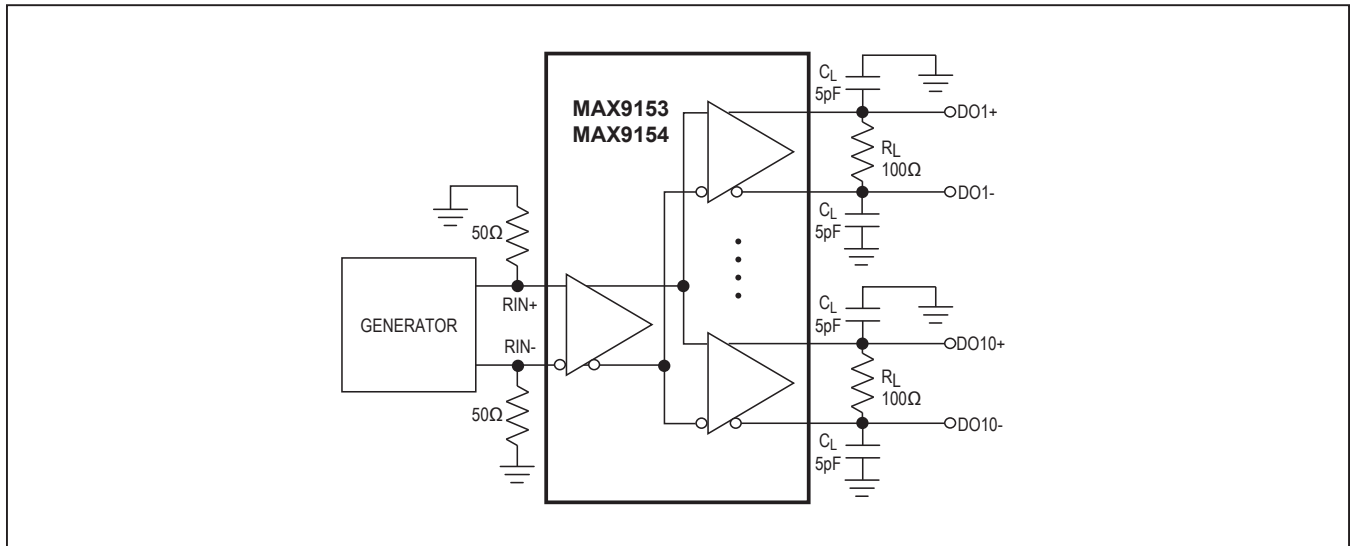


Figure 4. Propagation Delay and Transition Time Test Circuit

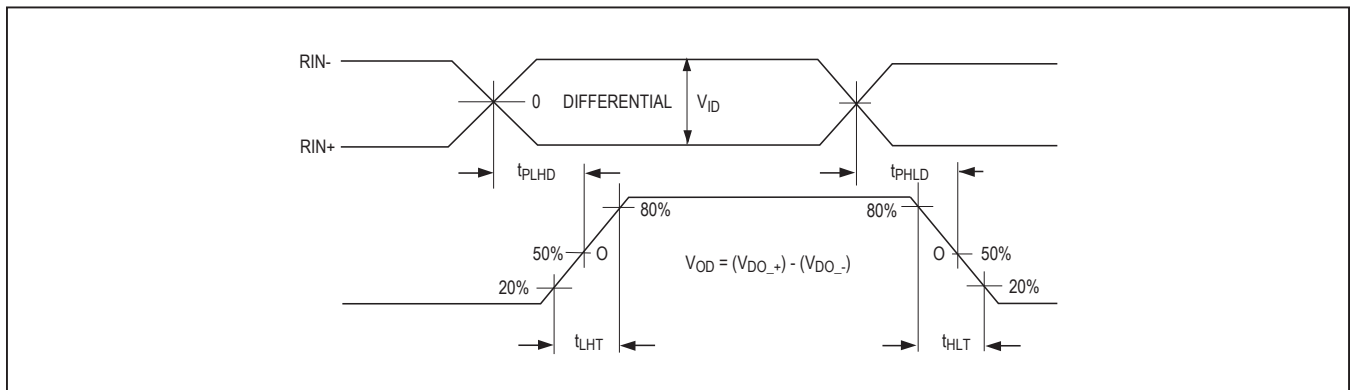


Figure 5. Propagation Delay and Transition Time Waveforms

Test Circuits and Timing Diagrams (continued)

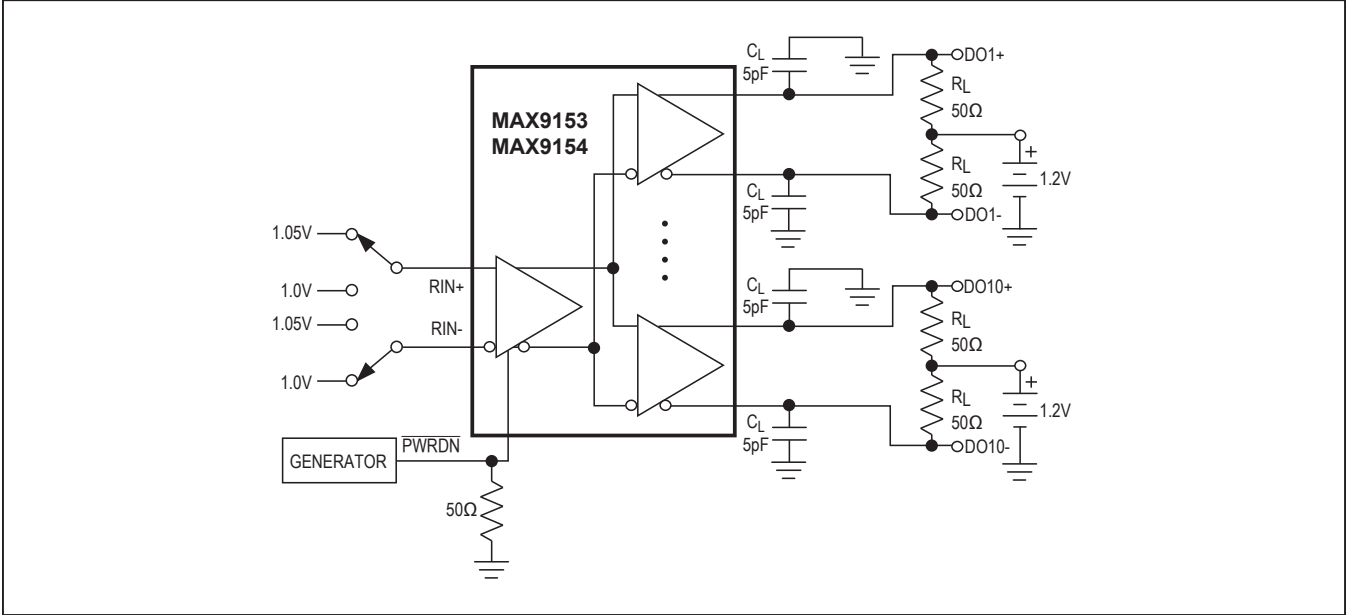


Figure 6. Power-Up/Down Delay Test Circuit

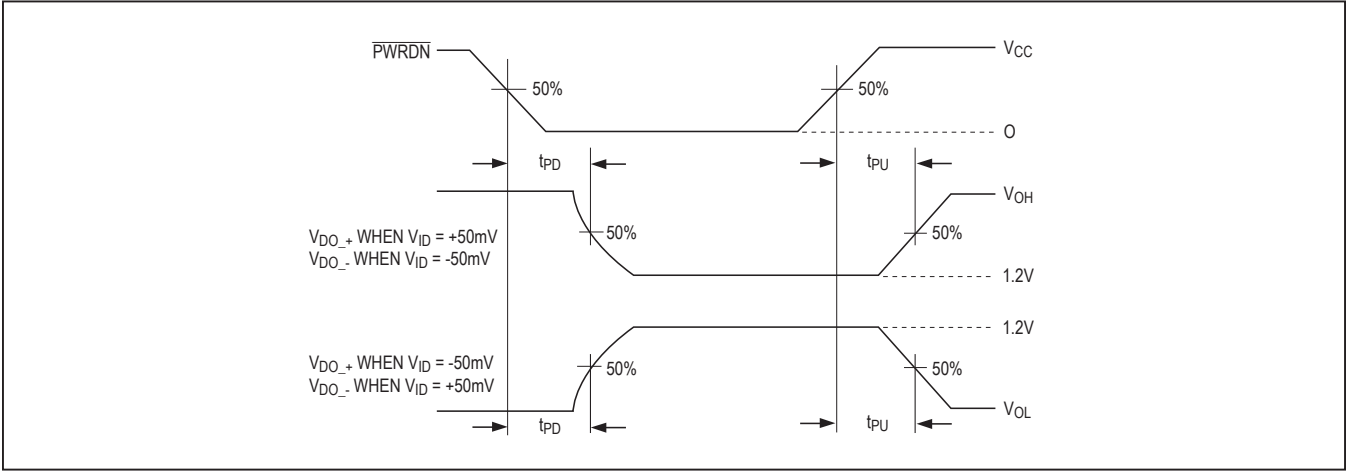
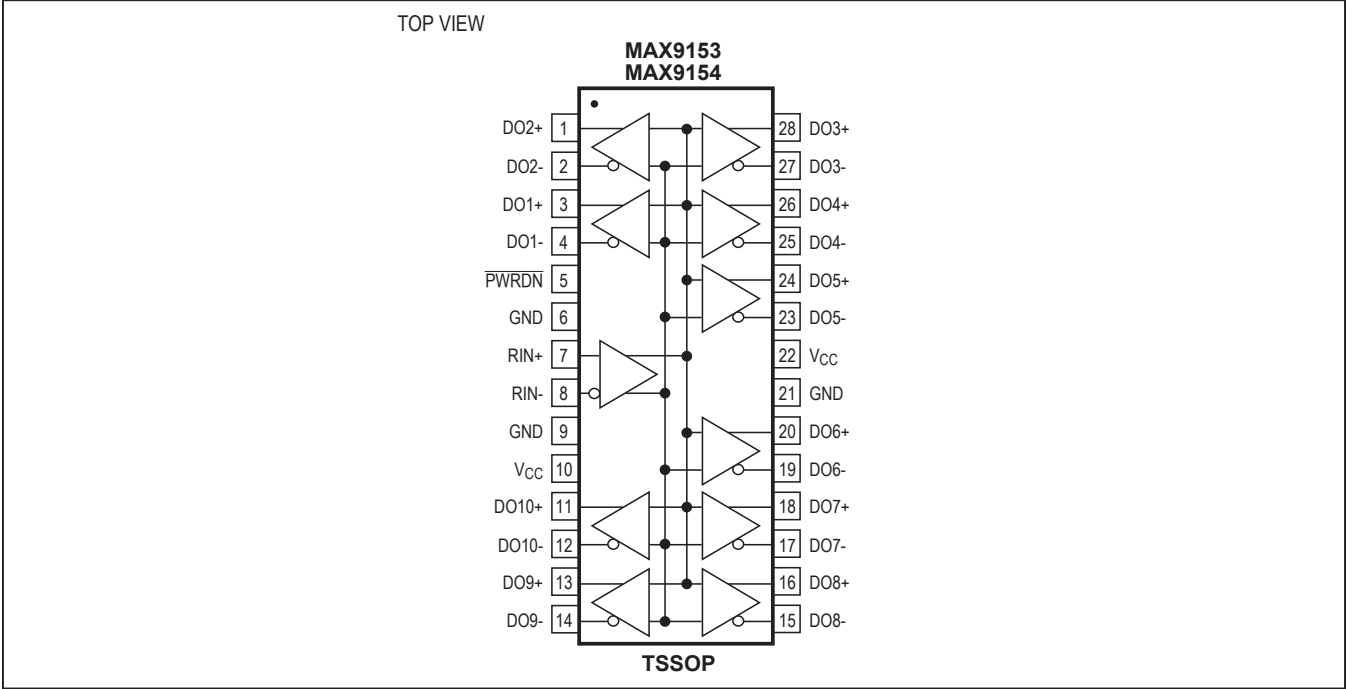
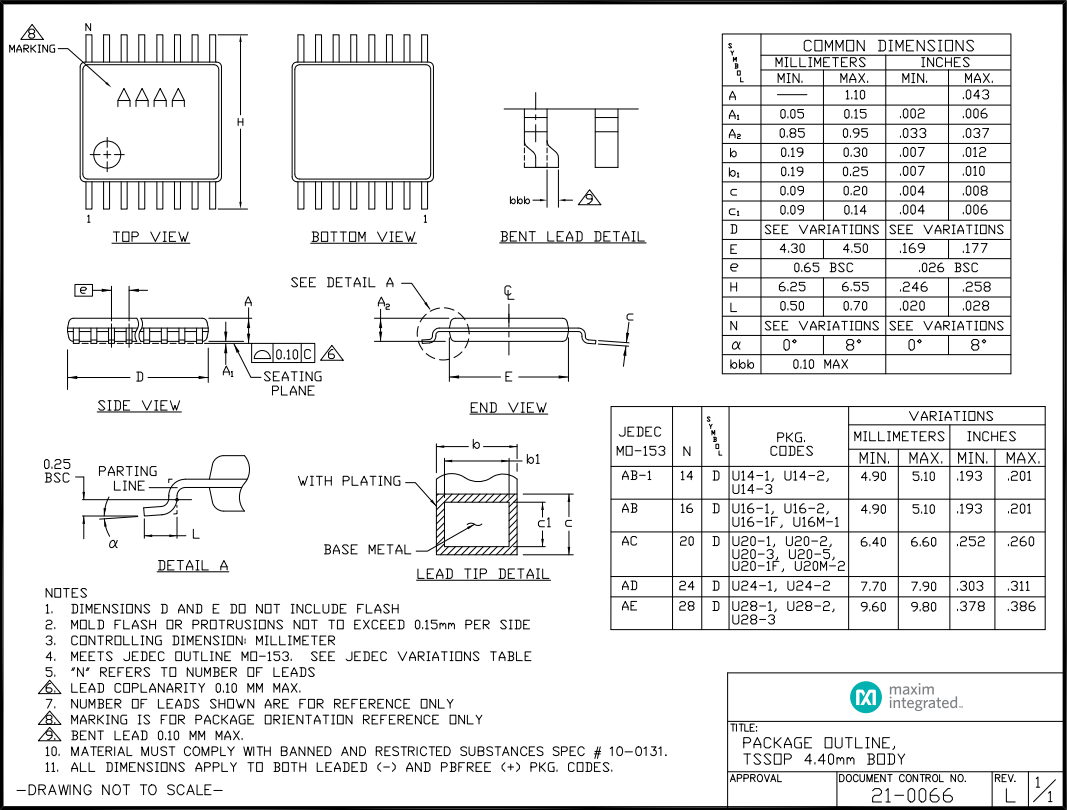


Figure 7. Power-Up/Down Delay Waveforms

Pin Configuration



Package Information



Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	10/01	Initial release	—
1	5/25	Updated <i>Ordering Information</i> table	1



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