MAX77675

Low I_Q SIMO PMIC with 0.5V to 5.5V Outputs Delivering Up to 700mA Total Output Current

General Description

The MAX77675 is a highly efficient, complete power supply for low-power, ultra-compact applications. It provides four programmable buck-boost switching outputs using only one inductor. Operating from a single lithium-ion or Li-ion battery, the MAX77675 delivers a total of 700mA output current ($3.7V_{IN}$, $1.8V_{OUT}$) in less than 40mm2 solution size.

An integrated sequencer controls full startup while an I^2C interface allows the MAX77675 to be dynamically configured and monitored.

This device is part of the single-inductor multiple-output (SIMO) product family.

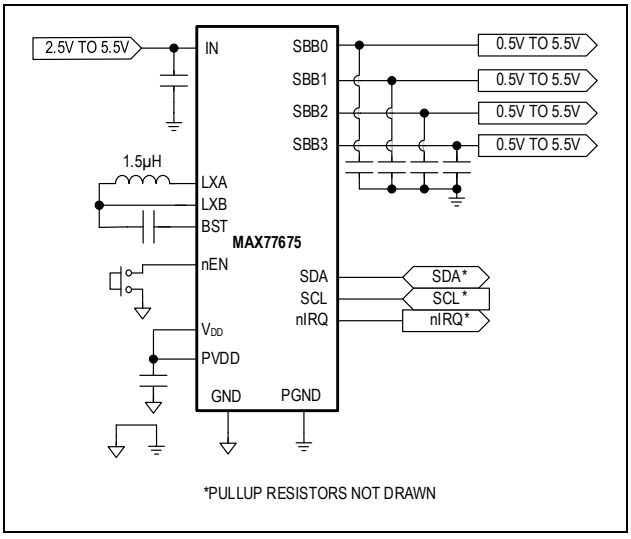
Applications

- TWS Bluetooth™ Headphones/Hearables
- Fitness, Health, Activity Monitors, and Smart Watches
- Portable Devices
- Sensor Nodes and Consumer Internet of Things or IoT

Benefits and Features

- 4x Buck/Buck-Boost/Boost Regulators, 1x Inductor
- 2.5V to 5.5V Input Voltage Range
- 0.5V to 5.5V Output Voltage Range
- 700mA Total Output Current ($3.7V_{IN}$, $1.8V_{OUT}$)
- SIMO
- Up to 90% Efficiency
  - 6.9µA Typical I_Q with Two Outputs Enabled in Low-Power Mode
- I^2C Interface and Dedicated Enable Pin
- Flexible Power Sequencer (FPS)
- 1.99mm x 1.99mm, 16-Bump, 0.5mm Pitch Wafer-Level Package (WLP)
  - < 40mm2 Solution Size

Simplified Block Diagram



***Ordering Information* appears at end of data sheet.**

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Absolute Maximum Ratings

nEN to GND ..... -0.3V to V_{IN} + 0.3V

SCL, SDA to GND ..... -0.3V to +6V

IN, nIRQ to GND ..... -0.3V to +6V

PVDD, V_{DD} to GND ..... -0.3V to +2.2V

SDA Continous Current ..... ±20mA

IN Continuous Current ..... $1.2A_{RMS}$

LXA Continuous Current (Note 1) ..... $1.2A_{RMS}$

LXB Continuous Current (Note 1) ..... $1.2A_{RMS}$

SBB0, SBB1, SBB2, SBB3 to PGND ..... -0.3V to +6V

BST to IN ..... -0.3V to +6V

BST to LXB ..... -0.3V to +6V

SBB0, SBB1, SBB2, SBB3 Short-Circuit Duration ..... Continuous

PGND to GND ..... -0.3V to +0.3V

Operating Temperature Range ..... -40°C to +85°C

Junction Temperature ..... +150°C

Storage Temperature Range ..... -65°C to +150°C

Soldering Temperature (reflow) ..... +260°C

Continuous Power Dissipation (Multilayer Board, T_A = +70°C, derate 20.4mW/°C above +70°C) 1632mW

Note 1: Do not externally bias LXA or LXB. LXA has internal clamping diodes to PGND and IN. LXB has an internal low-side clamping diode to PGND and an internal high-side clamping diode that dynamically connects to a selected SIMO output. It is normal for these diodes to briefly conduct during switching events. When the SIMO regulator is disabled, the LXB to PGND absolute maximum voltage is -0.3V to V_{SBBx} + 0.3V.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Recommended Operating Conditions

PARAMETER	SYMBOL	CONDITION	TYPICAL RANGE	UNIT
IN Voltage	V_{IN}		2.5–5.5	V
SBB0/1/2/3 Output Voltage	V_{SBBx}	CNFG_SBB_TOP.STEP_SZ_SBBx = 0	0.5–5.5	V
		CNFG_SBB_TOP.STEP_SZ_SBBx = 1	0.5000–3.6875	
SBB0/1/2/3 Maximum Combined Output Current	$I_{SBB0} + I_{SBB1} + I_{SBB2} + I_{SBB3}$	*Note 4*	700	mA
V_{DD} Voltage	V_{DD}		1.8	V

Note: These limits are not guaranteed.

Package Information

16 WLP 0.5mm Pitch

Package Code	W161N1+1
Outline Number	*21-100374*
Land Pattern Number	Refer to *Application Note 1891*
Thermal Resistance, Four Layer Board:	
Junction-to-Ambient (θ_{JA})	49°C/W (2s2p board)
Junction-to-Case (θ_{JC})	N/A

For the latest package outline information and land patterns (footprints), go to *www.analog.com/packages*. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to *www.analog.com/thermal-tutorial*.

Electrical Characteristics

(V_{IN} = 3.7V, Limits are 100% tested at T_A = +25°C. Limits over the operating temperature range (T_A = -40°C to +85°C) and relevant supply voltage range are guaranteed by design and characterization, unless otherwise noted. Specifications marked "GBD" are guaranteed by design and not production tested.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
INPUT CURRENT							
Shutdown Current	I_{SHDN}	All SBBx channels are disabled, V_{IN} = 3.7V, V_{LXA} = 0V	T_A = +25°C		0.3		mA
Quiescent Supply Current	I_Q	T_A = +25°C	All channels disabled, bias in LPM		3.8		µA
			All channels disabled, bias in NPM		10		
VOLTAGE MONITORS							
Input Voltage Range	V_{IN}			2.5		5.5	V
POWER-ON RESET (POR)							
POR Threshold	V_{POR}	V_{IN} falling			1.8		V
UNDERVOLTAGE LOCKOUT (UVLO)							
UVLO Threshold	V_{IN_UVLO}	V_{IN} falling, UVLO_F[1:0] = 0x4			2.3		V
UVLO Threshold Hysteresis	V_{INUVLO_HYS}	UVLO_H[1:0] = 0x5 (*Note 2*)			300		mV
OVERVOLTAGE LOCKOUT (OVLO)							
OVLO Threshold	V_{INOVLO}	V_{IN} rising		5.70	5.85	6.00	V
THERMAL MONITORS							
Overtemperature Lockout Threshold	T_{OTLO}	T_J rising			145		°C
Thermal Alarm Temperature 1	T_{JAL1}	T_J rising			90		ºC
Thermal Alarm Temperature 2	T_{JAL2}	T_J rising			120		ºC
ENABLE INPUT (nEN)							
nEN Input Leakage Current	I_{nEN_LKG}	V_{nEN} = V_{IN} = 5.5V CNFG_GLBL_A.PU_DIS = 1	T_A = +25°C	-1	±0.001	+1	µA
		T_A = +85°C			±0.01		
nEN Input Falling Threshold	$V_{TH_nEN_F}$	nEN falling		V_{IN} - 1.6	V_{IN} - 1.2		V
nEN Input Rising Threshold	$V_{TH_nEN_R}$	nEN rising			V_{IN} - 1.1	V_{IN} - 0.6	V
Debounce Time	t_{DBNC_nEN}	CNFG_GLBL_A.DBEN_nEN = 0			100		µs
		CNFG_GLBL_A.DBEN_nEN = 1 (*Note 5*)			30		ms
Manual Reset Time	t_{MRST}	(*Note 3* and *Note 5*)	CNFG_GLBL_A . MRT[1:0] = 0x0	3.75	4.00	5.25	s
			CNFG_GLBL_A . MRT[1:0] = 0x1	7.55	8.00	9.45	
			CNFG_GLBL_A . MRT[1:0] = 0x2	11.35	12.00	13.65	

(V_{IN} = 3.7V, Limits are 100% tested at T_A = +25°C. Limits over the operating temperature range (T_A = -40°C to +85°C) and relevant supply voltage range are guaranteed by design and characterization, unless otherwise noted. Specifications marked "GBD" are guaranteed by design and not production tested.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
			CNFG_GLBL_A . MRT[1:0] = 0x3	15.15	16.00	17.85	
nEN Pullup	R_{nEN_PU}	Pullup to V_{IN}	CNFG_GLBL_A.PU_DIS = 0		200		kΩ
OPEN-DRAIN INTERRUPT OUTPUT (nIRQ)							
Output Low Voltage		Sinking 2mA				0.4	V
Output Falling Edge Time	t_{f_nIRQ}	C_{IRQ} = 25pF (*Note 5*)			1.5		ns
Leakage Current	I_{nIRQ_LKG}	V_{IN} = 5.5V, nIRQ set to high impedance, V_{nIRQ} = 0V or 5.5V	T_A = +25ºC	-1	±0.001	+1	µA
			T_A = +85ºC		±0.01		
FLEXIBLE POWER SEQUENCER							
Power-Up Event Periods	t_{EN}	See *Figure 7*. (*Note 5*)			1.28		ms
Power-Down Event Periods	t_{DIS}	See *Figure 7*. (*Note 5*)			2.56		ms
BIAS							
Enable Delay	t_{BIAS_EN}				1		ms
PVDD Output Voltage	V_{PVDD}				1.8		V
V_{DD} Input Voltage	V_{DD}				1.8		V

Note 2: Programmed at Analog Devices factory.

Note 3: The error in manual reset period is the same percentage-wise for all options.

Electrical Characteristics—SIMO Buck-Boost

(V_{IN} = 3.7V, C_{SBBx} = 22µF, L = 1.5µH, Limits are 100% tested at T_A = +25°C. Limits over the operating temperature range (T_A = -40°C to +85°C) and relevant supply voltage range are guaranteed by design and characterization, unless otherwise noted. Specifications marked "GBD" are guaranteed by design and not production tested.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
GENERAL CHARACTERISTICS							
SIMO Quiescent Supply Current	I_{Q_SIMO}	T_A = +25ºC, bias in LPM (*Note 5*)	Total current for the first channel at 1.8V output		4.0		µA
			Current for each additional channel at 1.8V output		0.2		
		T_A = +25ºC, bias in NPM (*Note 5*)	Current for the first channel at 1.8V output		230		
			Current for each additional channel at 1.8V output		61		
OUTPUT VOLTAGE RANGE (SBB0/1/2/3)							
Programmable Output Voltage Range		CNFG_SBB_TOP_A.STEP_SZ_SBBx = 0		0.5		5.5	V
		CNFG_SBB_TOP_A.STEP_SZ_SBBx = 1		0.5		3.6875	

(V_{IN} = 3.7V, C_{SBBx} = 22µF, L = 1.5µH, Limits are 100% tested at T_A = +25°C. Limits over the operating temperature range (T_A = -40°C to +85°C) and relevant supply voltage range are guaranteed by design and characterization, unless otherwise noted. Specifications marked "GBD" are guaranteed by design and not production tested.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Output DAC Bits					8		bits
Output DAC LSB Size		CNFG_SBB_TOP_A.STEP_SZ_SBBx = 0			25		mV
		CNFG_SBB_TOP_A.STEP_SZ_SBBx = 1			12.5		
OUTPUT VOLTAGE ACCURACY							
Output Voltage Accuracy		I_{SBBx} = 1mA, typical is based on an average over 100ms, V_{DD} = 1.8V, V_{SBBx} = 1.8V	T_A = +25°C	-3.0		+3.0	%
			T_A = -40°C to +85°C	-4.0		+4.0	
		I_{SBBx} = 300mA, typical is based on an average over 100ms, V_{DD} = 1.8V, V_{SBBx} = 1.8V	T_A = +25°C	-2.0		+2.0	
			T_A = -40°C to +85°C	-4.0		+4.0	
TIMING CHARACTERISTICS							
Enable Delay	t_{SIMO_EN}	Delay time from the SIMO receiving its first enable signal to when it begins to switch in order to service that output			450		µs
		After the first SIMO channel has been enabled,subsequent enable signals cause their outputs to begin switching after this delay time.			150		
Soft-Start Slew Rate	dV/dt_{SS}	CNFG_SBB_TOP_ B.SR_SBBx = 0		1.0	2.0	3.0	mV/µs
		CNFG_SBB_TOP_ B.SR_SBBx = 1 (*Note 5*)	CNFG_SBB_TOP_ B.DVS_SLEW = 0		5.0		
			CNFG_SBB_TOP_ B.DVS_SLEW = 1		10		
POWER STAGE CHARACTERISTICS							
LXA Leakage Current		All SBB channels are disabled, V_{IN} = 5.5V, V_{LXA} = 0V, or 5.5V	T_A = +25°C	-1	±0.01	+1	µA
			T_A = +85°C		±0.1		
LXB Leakage Current		All SBB channels are disabled, V_{IN} = 5.5V, V_{LXA} = 0V or 5.5V, all V_{SBBx} = 4.0V	T_A = +25°C	-1	±0.01	+1	µA
			T_A = +85°C		±0.1		
Disabled Output Leakage Current		All SBB channels are disabled, active discharge disabled (ADE_SBBx = 0), V_{SBBx} = 4.0V, V_{LXB} = 0V, V_{IN} = V_{BST} = 5.5V	T_A = +25°C		0.05	1	µA
			T_A = +85°C		0.1		
Active-Discharge Impedance	R_{AD_SBBx}	All SBB channels are disabled, active discharge enabled (ADE_SBBx = 1)		80	140	260	Ω

Note 2: See the *SIMO-Supported Output Current* section for more information.

Electrical Characteristics —I²C Serial Interface

(V_{IN} = 3.7V, Limits are 100% tested at T_A = +25°C. Limits over the operating temperature range (T_A = -40°C to +85°C) and relevant supply voltage range are guaranteed by design and characterization, unless otherwise noted. Specifications marked "GBD" are guaranteed by design and not production tested.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
SDA AND SCL I/O STAGE						
SCL, SDA Input High Voltage	V_{IH}	V_{IN} = 3.7V, T_A = +25ºC	0.7 x V_{DD}			V
SCL, SDA Input Low Voltage	V_{IL}	T_A = +25ºC			0.3 x V_{DD}	V
SCL, SDA Input Hysteresis	V_{HYS}	T_A = +25ºC		0.05 x V_{DD}		V
SCL, SDA Input Leakage Current	I_I	V_{SCL} = V_{SDA} = V_{DD}	-1		+1	µA
SDA Output Low Voltage	V_{OL}	Sinking 20mA			0.4	V
SCL, SDA Pin Capacitance	C_I	(*Note 5*)		10		pF
Output Fall Time from V_{IH} to V_{IL}	t_{OF}	(*Note 5*)			120	ns
I²C-COMPATIBLE INTERFACE TIMING (STANDARD, FAST, AND FAST-MODE PLUS) (*Note 5*)						
Clock Frequency	f_{SCL}		0		1000	kHz
Hold Time (REPEATED) START Condition	t_{HD_STA}		0.26			µs
SCL Low Period	t_{LOW}		0.5			µs
SCL High Period	t_{HIGH}		0.26			µs
Setup Time REPEATED START Condition	t_{SU_STA}		0.26			µs
Data Hold Time	t_{HD_DAT}		0			µs
Data Setup Time	t_{SU_DAT}		50			µs
Setup Time for STOP Condition	t_{SU_STO}		0.26			µs
Bus Free Time between STOP and START Condition	t_{BUF}		0.5			µs
Pulse Width of Suppressed Spikes	t_{SP}	Maximum pulse width of spikes that must be suppressed by the input filter			50	ns
I²C-COMPATIBLE INTERFACE TIMING (HIGH-SPEED MODE, CB = 100pF) (*Note 5*)						
Clock Frequency	f_{SCL}				3.4	MHz
Setup Time REPEATED START Condition	t_{SU_STA}		160			ns
Hold Time (REPEATED) START Condition	t_{HD_STA}		160			ns
SCL Low Period	t_{LOW}		160			ns
SCL High Period	t_{HIGH}		60			ns
Data Setup Time	t_{SU_DAT}		10			ns
Data Hold Time	t_{HD_DAT}		0		70	ns
SCL Rise Time	t_{rCL}	T_A = +25°C	10		40	ns
Rise Time of SCL Signal After REPEATED	t_{rCL1}	T_A = +25°C	10		80	ns

(V_{IN} = 3.7V, Limits are 100% tested at T_A = +25°C. Limits over the operating temperature range (T_A = -40°C to +85°C) and relevant supply voltage range are guaranteed by design and characterization, unless otherwise noted. Specifications marked "GBD" are guaranteed by design and not production tested.)

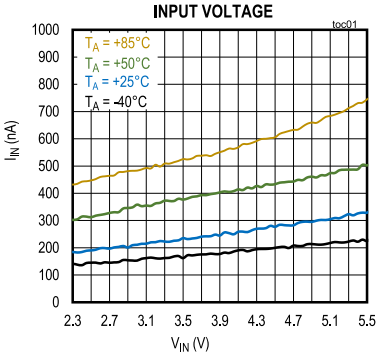
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
START Condition and After Acknowledge Bit						
SCL Fall Time	t_{fCL}	T_A = +25°C	10		40	ns
SDA Rise Time	t_{rDA}	T_A = +25°C	10		80	ns
SDA Fall Time	t_{fDA}	T_A = +25°C	10		80	ns
Setup Time for STOP Condition	t_{SU_STO}		160			ns
Bus Capacitance	C_B				100	pF
Pulse Width of Suppressed Spikes	t_{SP}	Maximum pulse width of spikes that must be suppressed by the input filter			10	ns
I²C-COMPATIBLE INTERFACE TIMING (HIGH-SPEED MODE, CB = 400pF) (*Note 5*)						
Clock Frequency	f_{SCL}				1.7	MHz
Setup Time REPEATED START Condition	t_{SU_STA}		160			ns
Hold Time (REPEATED) START Condition	t_{HD_STA}		160			ns
SCL Low Period	t_{LOW}		320			ns
SCL High Period	t_{HIGH}		120			ns
Data Setup Time	t_{SU_DAT}		10			ns
Data Hold Time	t_{HD_DAT}		0		150	ns
SCL Rise Time	t_{RCL}	T_A = +25°C	20		80	ns
Rise Time of SCL Signal After REPEATED START Condition and After Acknowledge Bit	t_{RCL1}	T_A = +25°C	20		160	ns
SCL Fall Time	t_{FCL}	T_A = +25°C	20		80	ns
SDA Rise Time	t_{RDA}	T_A = +25°C	20		160	ns
SDA Fall Time	t_{FDA}	T_A = +25°C	20		160	ns
Setup Time for STOP Condition	t_{SU_STO}		160			ns
Bus Capacitance	C_B				400	pF
Pulse Width of Suppressed Spikes	t_{SP}	Maximum pulse width of spikes that must be suppressed by the input filter		10		ns

Note 2: Design guidance only. Not production tested.

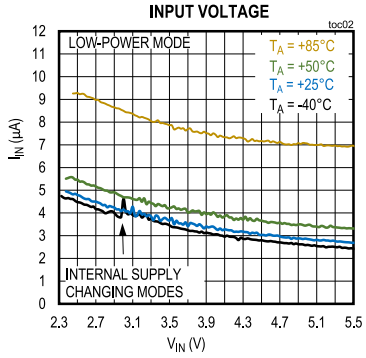
Typical Operating Characteristics

(Typical Applications Circuit. V_{IN} = 3.7V, C_{SBBx} = 22µF, L = 1.5µH, T_A = +25°C, V_{SBB0} = 1.8V, V_{SBB1} = 1.1V, V_{SBB2} = 0.7V, V_{SBB3} = 3.3V, unless otherwise noted.)

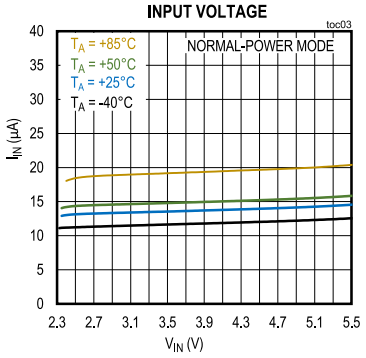
SHUTDOWN CURRENT vs. INPUT VOLTAGE



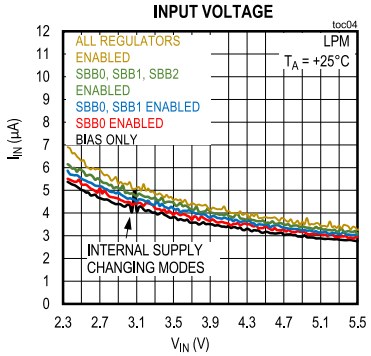
BIAS QUIESCENT CURRENT vs. INPUT VOLTAGE



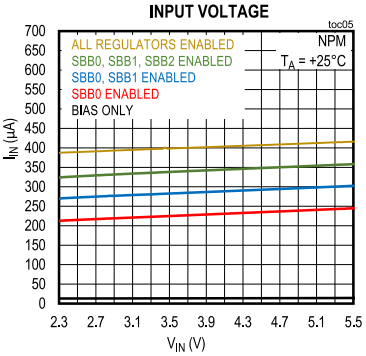
BIAS QUIESCENT CURRENT vs. INPUT VOLTAGE



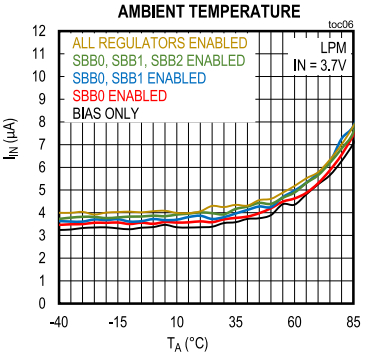
QUIESCENT CURRENT vs. INPUT VOLTAGE



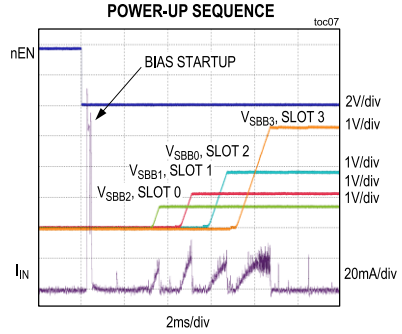
QUIESCENT CURRENT vs. INPUT VOLTAGE



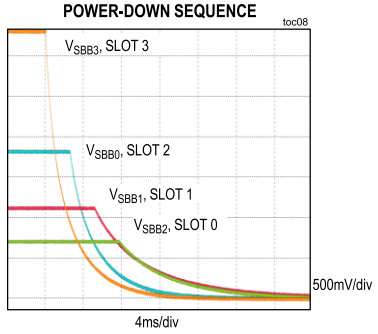
QUIESCENT CURRENT vs. AMBIENT TEMPERATURE



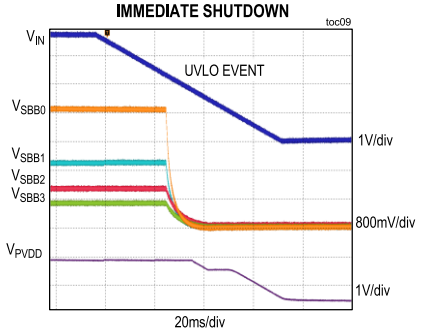
POWER-UP SEQUENCE



POWER-DOWN SEQUENCE

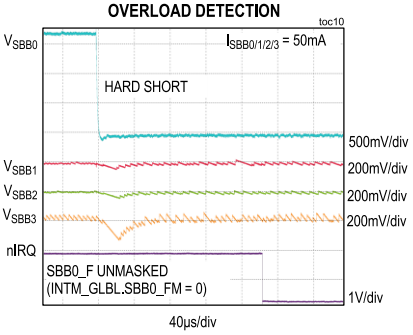


IMMEDIATE SHUTDOWN

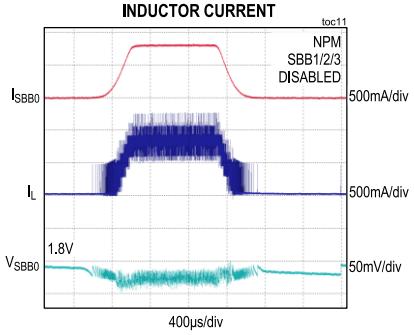


(Typical Applications Circuit. V_{IN} = 3.7V, C_{SBBx} = 22µF, L = 1.5µH, T_A = +25°C, V_{SBB0} = 1.8V, V_{SBB1} = 1.1V, V_{SBB2} = 0.7V, V_{SBB3} = 3.3V, unless otherwise noted.)

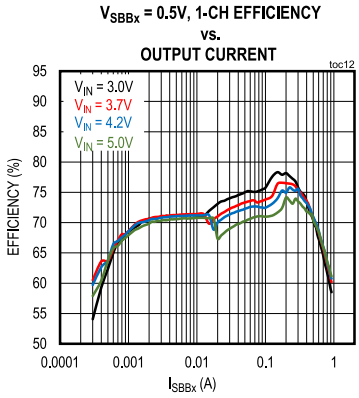
OVERLOAD DETECTION



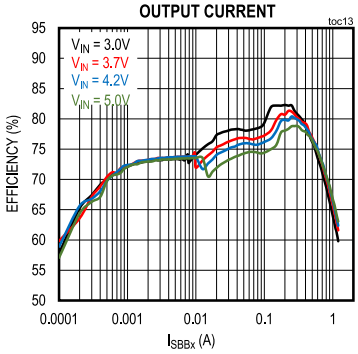
INDUCTOR CURRENT



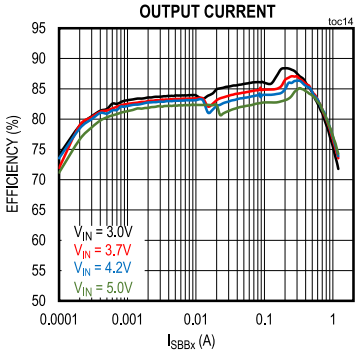
V_{SBBx} = 0.5V, 1-CH EFFICIENCY vs. OUTPUT CURRENT



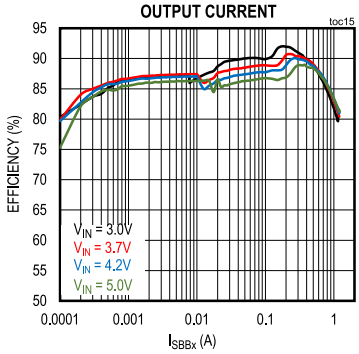
V_{SBBx} = 0.7V, 1-CH EFFICIENCY vs. OUTPUT CURRENT



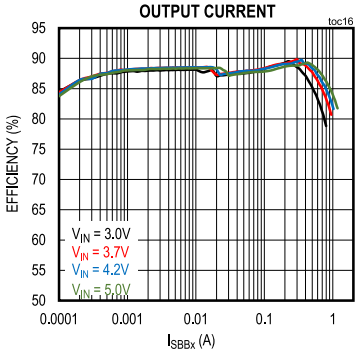
V_{SBBx} = 1.2V, 1-CH EFFICIENCY vs. OUTPUT CURRENT



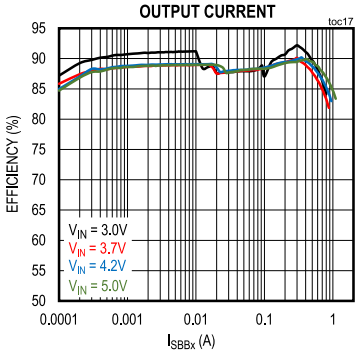
V_{SBBx} = 1.8V, 1-CH EFFICIENCY vs. OUTPUT CURRENT



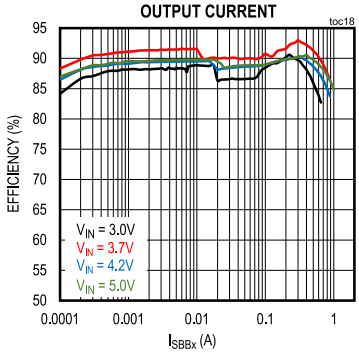
V_{SBBx} = 3.3V, 1-CH EFFICIENCY vs. OUTPUT CURRENT



V_{SBBx} = 4.0V, 1-CH EFFICIENCY vs. OUTPUT CURRENT

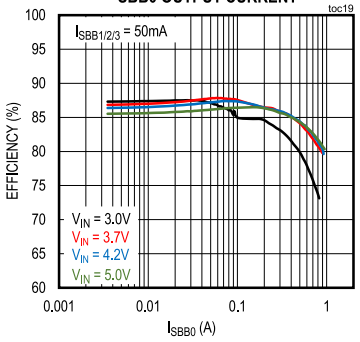


V_{SBBx} = 5.0V, 1-CH EFFICIENCY vs. OUTPUT CURRENT

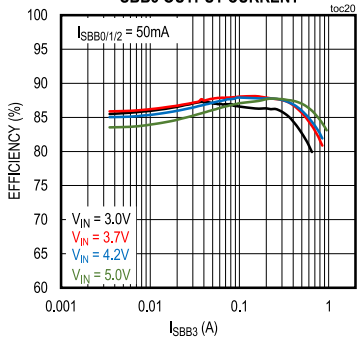


(Typical Applications Circuit. V_{IN} = 3.7V, C_{SBBx} = 22µF, L = 1.5µH, T_A = +25°C, V_{SBB0} = 1.8V, V_{SBB1} = 1.1V, V_{SBB2} = 0.7V, V_{SBB3} = 3.3V, unless otherwise noted.)

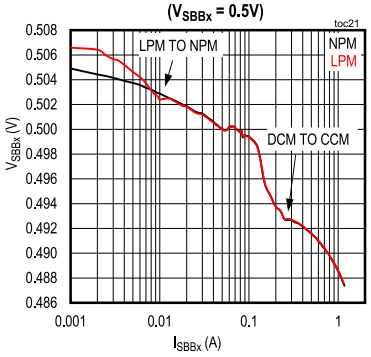
SYSTEM EFFICIENCY vs. SBB0 OUTPUT CURRENT



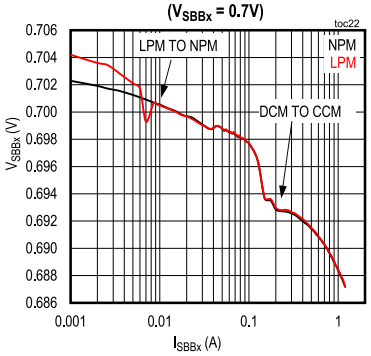
SYSTEM EFFICIENCY vs. SBB3 OUTPUT CURRENT



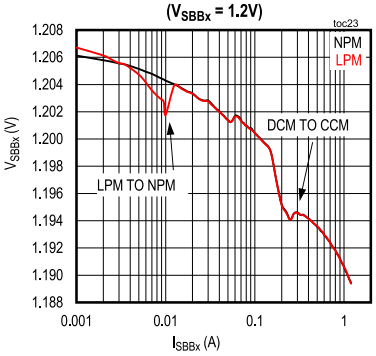
1-CH LOAD REGULATION (V_{SBBx} = 0.5V)



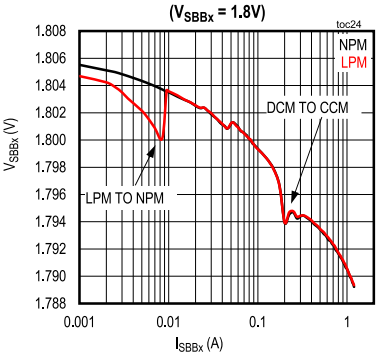
1-CH LOAD REGULATION (V_{SBBx} = 0.7V)



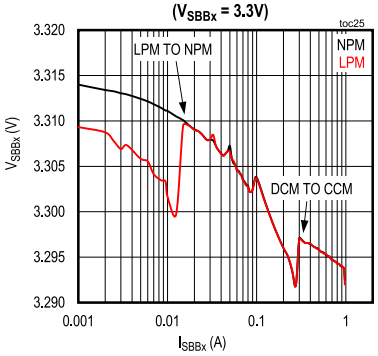
1-CH LOAD REGULATION (V_{SBBx} = 1.2V)



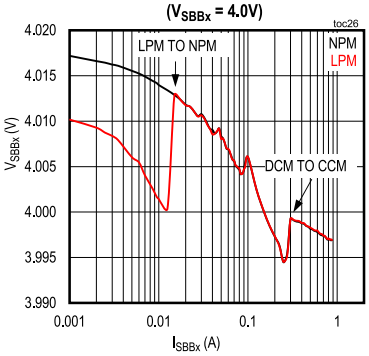
1-CH LOAD REGULATION (V_{SBBx} = 1.8V)



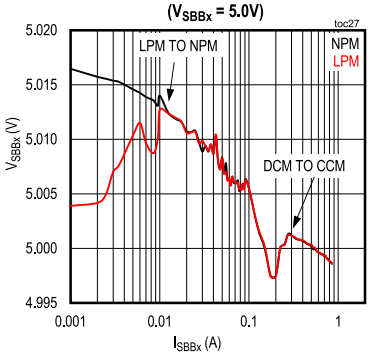
1-CH LOAD REGULATION (V_{SBBx} = 3.3V)



1-CH LOAD REGULATION (V_{SBBx} = 4.0V)

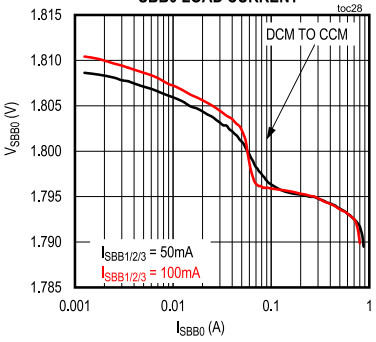


1-CH LOAD REGULATION (V_{SBBx} = 5.0V)

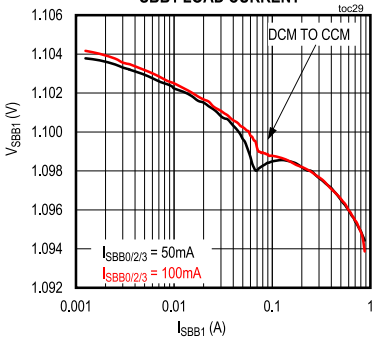


(Typical Applications Circuit. V_{IN} = 3.7V, C_{SBBx} = 22µF, L = 1.5µH, T_A = +25°C, V_{SBB0} = 1.8V, V_{SBB1} = 1.1V, V_{SBB2} = 0.7V, V_{SBB3} = 3.3V, unless otherwise noted.)

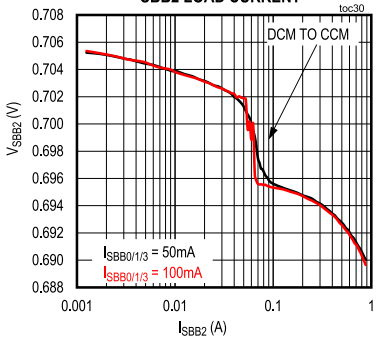
SYSTEM LOAD REGULATION vs. SBB0 LOAD CURRENT



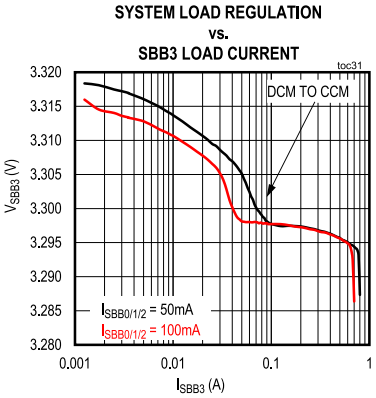
SYSTEM LOAD REGULATION vs. SBB1 LOAD CURRENT



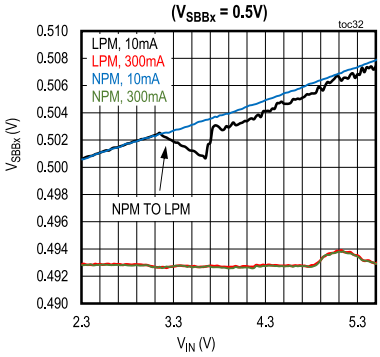
SYSTEM LOAD REGULATION vs. SBB2 LOAD CURRENT



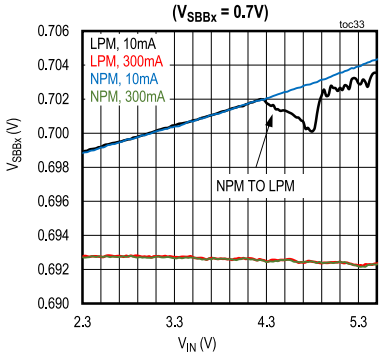
SYSTEM LOAD REGULATION vs. SBB3 LOAD CURRENT



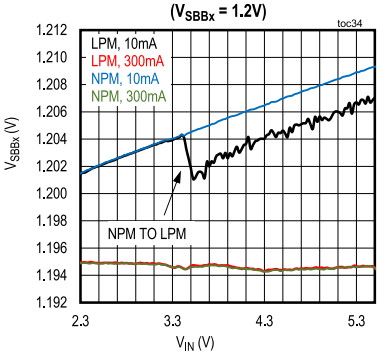
1-CH LINE REGULATION (V_{SBBx} = 0.5V)



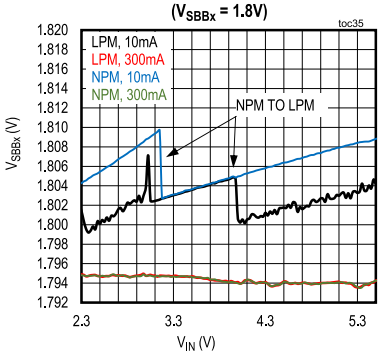
1-CH LINE REGULATION (V_{SBBx} = 0.7V)



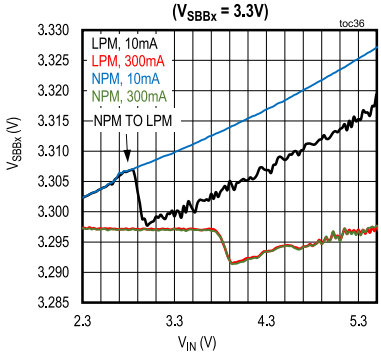
1-CH LINE REGULATION (V_{SBBx} = 1.2V)



1-CH LINE REGULATION (V_{SBBx} = 1.8V)



1-CH LINE REGULATION (V_{SBBx} = 3.3V)



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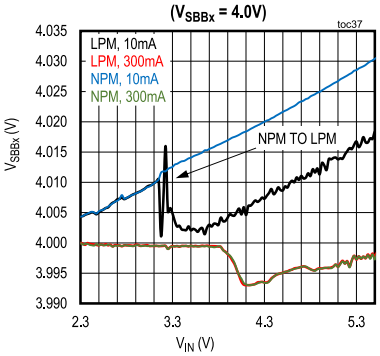
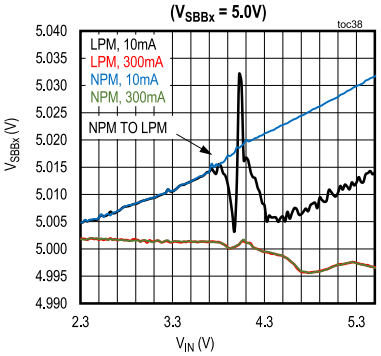
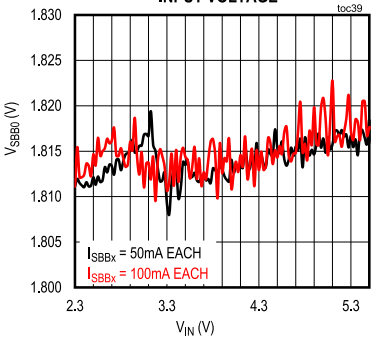
1-CH LINE REGULATION (V_{SBBx} = 4.0V)



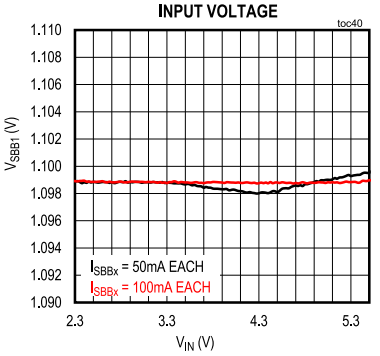
1-CH LINE REGULATION (V_{SBBx} = 5.0V)



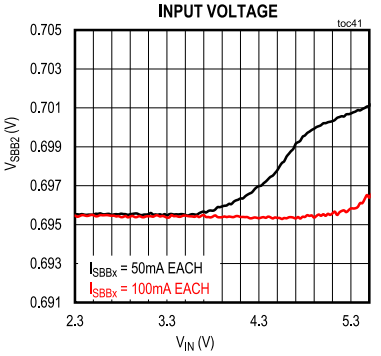
SYSTEM LINE REGULATION vs. INPUT VOLTAGE



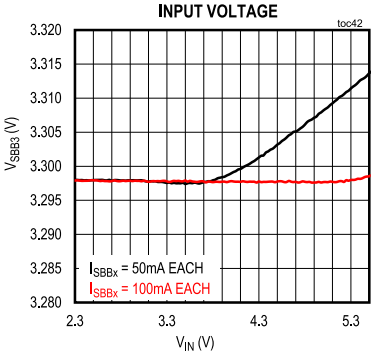
SYSTEM LINE REGULATION vs. INPUT VOLTAGE



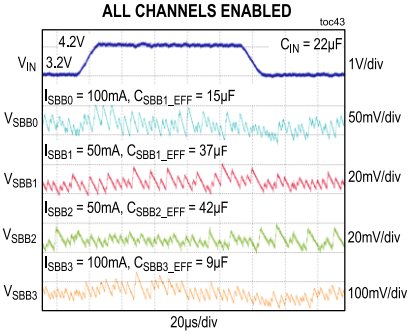
SYSTEM LINE REGULATION vs. INPUT VOLTAGE



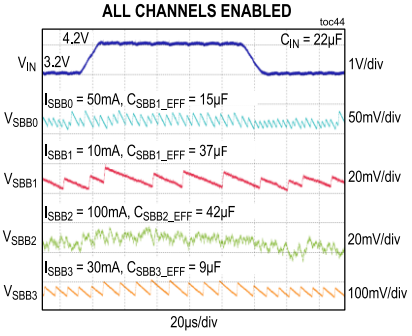
SYSTEM LINE REGULATION vs. INPUT VOLTAGE



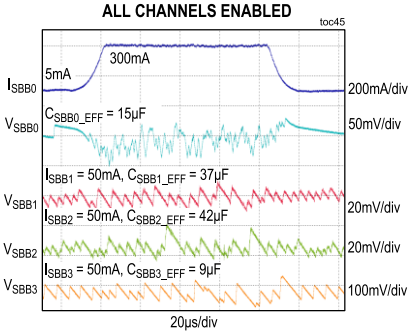
LINE TRANSIENT ALL CHANNELS ENABLED



LINE TRANSIENT ALL CHANNELS ENABLED



SBB0 LOAD TRANSIENT ALL CHANNELS ENABLED



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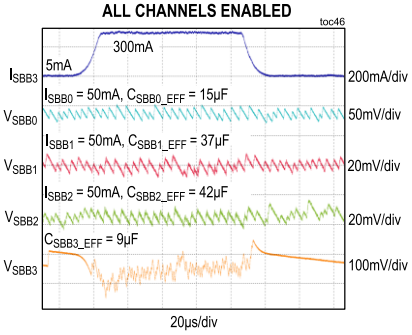
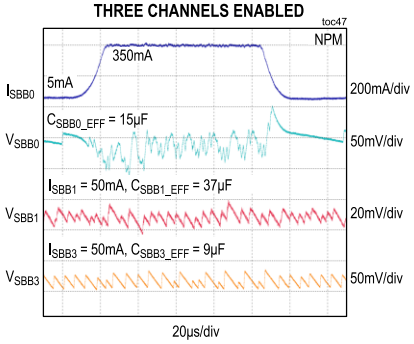
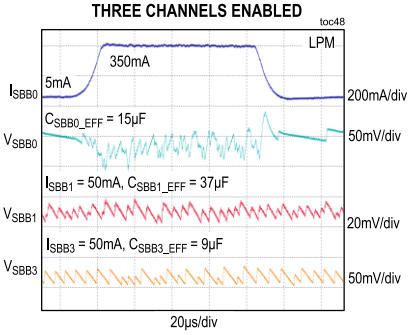
SBB3 LOAD TRANSIENT ALL CHANNELS ENABLED



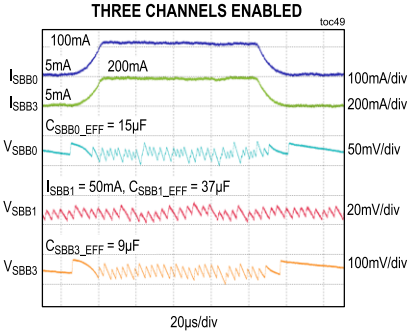
SBB0 LOAD TRANSIENT THREE CHANNELS ENABLED



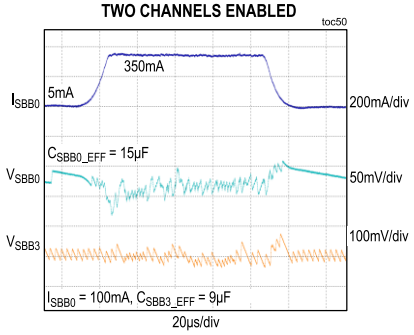
SBB0 LOAD TRANSIENT THREE CHANNELS ENABLED



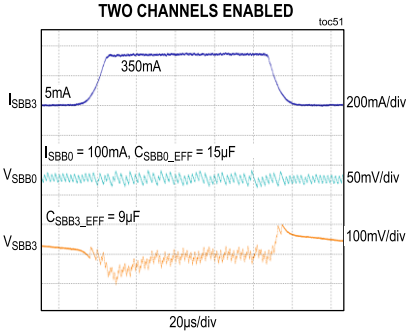
SBB0 AND SBB3 LOAD TRANSIENTS THREE CHANNELS ENABLED



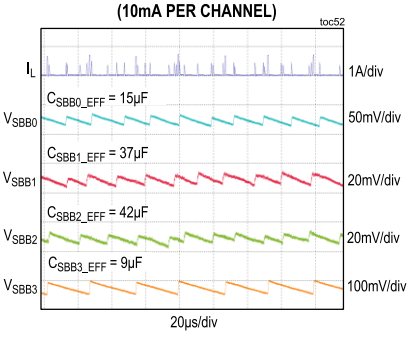
SBB0 LOAD TRANSIENT TWO CHANNELS ENABLED



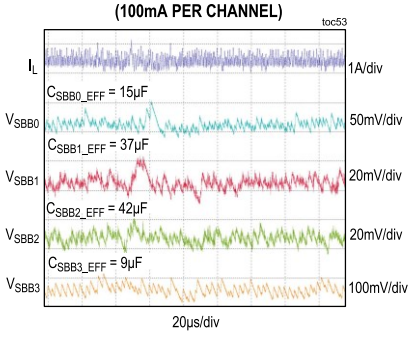
SBB3 LOAD TRANSIENT TWO CHANNELS ENABLED



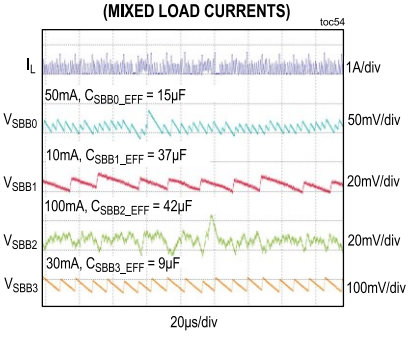
RIPPLE (10mA PER CHANNEL)



RIPPLE (100mA PER CHANNEL)

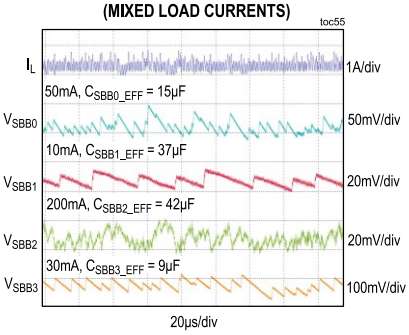


RIPPLE (MIXED LOAD CURRENTS)

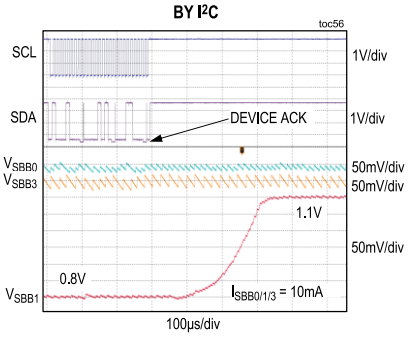


(Typical Applications Circuit. V_{IN} = 3.7V, C_{SBBx} = 22µF, L = 1.5µH, T_A = +25°C, V_{SBB0} = 1.8V, V_{SBB1} = 1.1V, V_{SBB2} = 0.7V, V_{SBB3} = 3.3V, unless otherwise noted.)

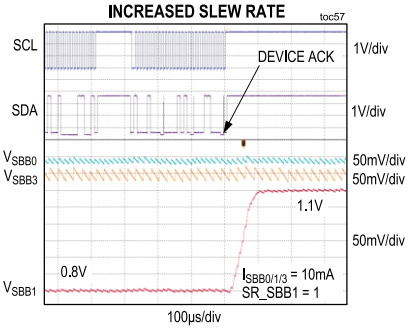
RIPPLE
(MIXED LOAD CURRENTS)



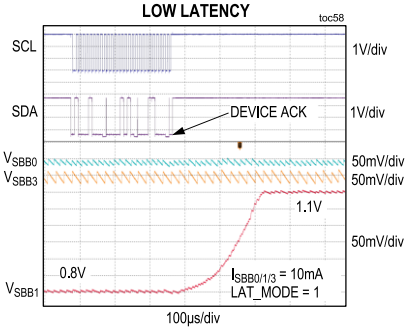
DYNAMIC VOLTAGE CHANGE
BY I²C



DYNAMIC VOLTAGE CHANGE
BY I²C
INCREASED SLEW RATE

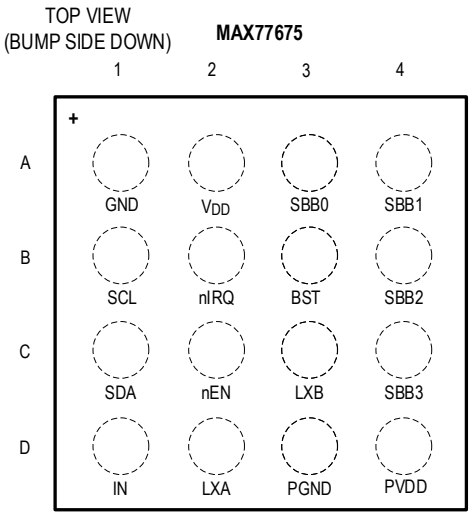


DYNAMIC VOLTAGE CHANGE
BY I²C
LOW LATENCY



Pin Configuration

MAX77675



WLP
(1.99mm x 1.99mm x 0.64mm, 0.5mm PITCH)

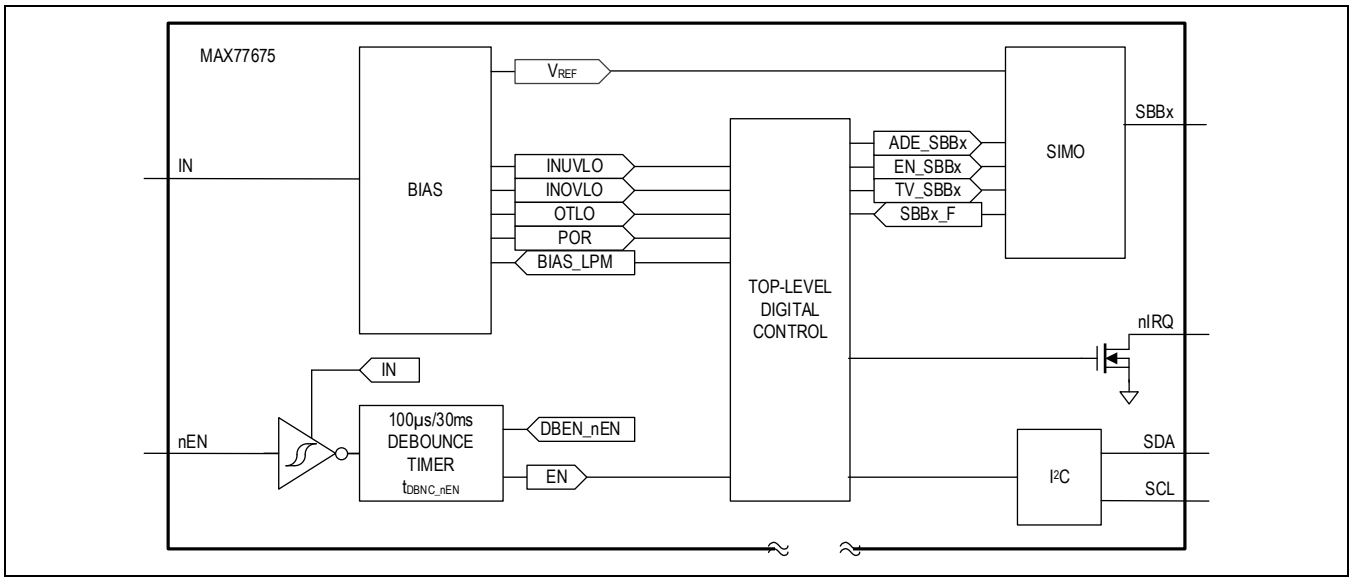
Pin Descriptions

PIN	NAME	FUNCTION	Type
TOP LEVEL			
C2	nEN	Active-Low Enable Input. EN supports push-button, slide-switch, or logic configurations. If unused, connect nEN to GND to enable the IC whenever IN is powered.	Digital Input
B2	nIRQ	Active-Low, Open-Drain Interrupt Pin. Connect a 100kΩ pull-up resistor to nIRQ .	Digital Output
B1	SCL	I^2C Clock	Digital Input
C1	SDA	I^2C Data	Digital I/O
D1	IN	Input Voltage Connection	Power Input
A1	GND	Quiet Ground. Connect GND to PGND and the low-impedance ground plane of the PCB.	Ground
A2	V_{DD}	Device Power Input. Connect to PVDD. Bypass to GND with a 10µF capacitor.	Power Input
D4	PVDD	1.8V Internal Supply. Bypass this pin with a 10µF capacitor and connect to V_{DD}. Do not connect anything else to this pin. If pullup resistors must be connected to PVDD, ensure on the layout the connection points are as close as possible to the capacitor and not the pin. See the *PCB Layout Guide* section for more details.	Power Output
SIMO BUCK BOOST			
A3	SBB0	SIMO Buck-Boost Output 0. SBB0 is the power output for Channel 0 of the SIMO buck-boost. If not used, see the *Unused Outputs* section.	Power Output
A4	SBB1	SIMO Buck-Boost Output 1. SBB1 is the power output for Channel 1 of the SIMO buck-boost. If not used, see the *Unused Outputs* section.	Power Output
B4	SBB2	SIMO Buck-Boost Output 2. SBB2 is the power output for Channel 2 of the SIMO buck-boost. If not used, see the *Unused Outputs* section.	Power Output
C4	SBB3	SIMO Buck-Boost Output 3. SBB3 is the power output for Channel 3 of the SIMO buck-boost. If not used, see the *Unused Outputs* section.	Power Output

B3	BST	SIMO Power Input for the High-Side Output NMOS Drivers. Connect a 10nF ceramic capacitor between BST and LXB.	Power Input
C3	LXB	Switching Node B. LXB is driven between PGND and SBBx when SBBx is enabled. LXB is driven to PGND when all SIMO channels are disabled.	Power I/O
D2	LXA	Switching Node A. LXA is driven between PGND and IN when any SIMO channel is enabled. LXA is driven to PGND when all SIMO channels are disabled.	Power I/O
D3	PGND	Power Ground for the SIMO Low-Side FETs. Connect PGND to GND and the low-impedance ground plane of the PCB.	Ground

Functional Diagrams

Top Level Interconnect



Detailed Description

The MAX77675 provides a power management solution for low-power applications. A SIMO buck-boost regulator efficiently provides four independently programmable power rails.

A bidirectional I²C serial interface allows for configuring and checking the status of the device. An internal on/off controller provides power sequencing and supervisory functionality for the device.

Part Number Decoding

The MAX77675 has different one-time programmable (OTP) options and variants to support a variety of applications. The OTP options set default settings such as output voltage. See *Figure 1* for how to identify these. *Table 1* lists all available OTP options. Refer to *Product Naming Convention* for more details.

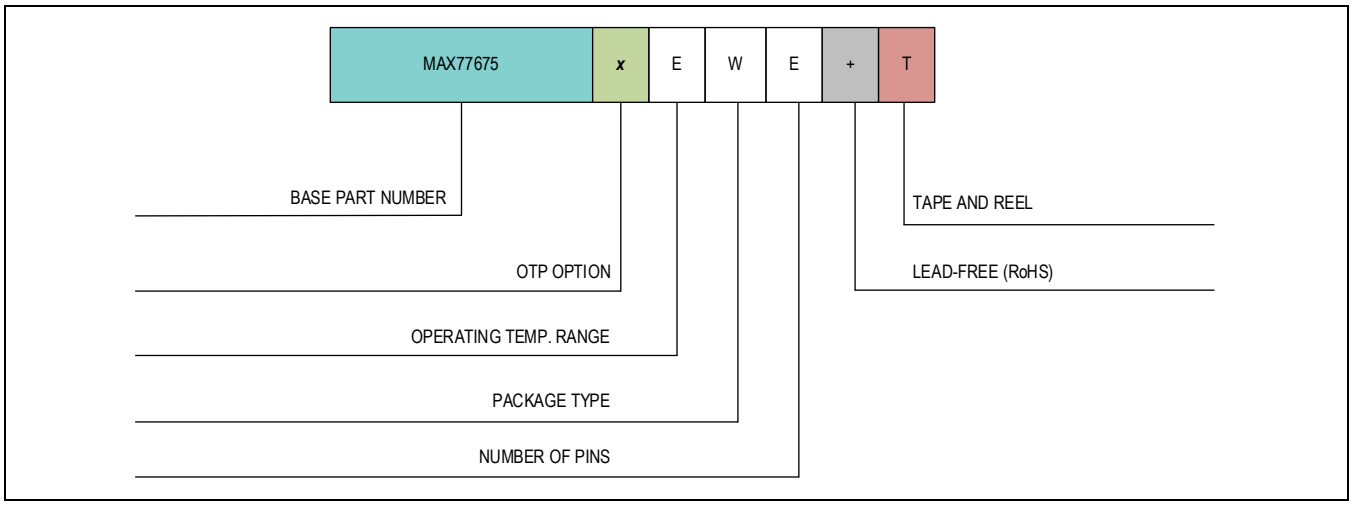


Figure 1. Part Number Decode

Table 1. OTP Options Table

			OTP LETTER AND SETTINGS					
BLOCK	**BIT FIELD NAME**	**SETTING NAME**	**A**	**C**	**O**	**G**	**H**	**L**
Global	CID[7:0]	OTP Identifier	0x3	0xC	0x6	0x7	0x8	0xA
	PU_DIS	Pullup Disable	Disabled	Enabled (200kΩ)	Enabled (200kΩ)	Disabled	Disabled	Disabled
	BIAS_LPM	Bias Power Mode	LPM	LPM	LPM	LPM	LPM	LPM
	MRT	Manual Reset Time	8s	8s	8s	8s	8s	8s
	nEN_MODE	nEN Mode	Logic	Logic	Push-Button	Logic	Logic	Logic
	DBEN_nEN	nEN Debounce Time	100µs	100µs	100µs	100µs	100µs	100µs
	ADDR	I²C Address (7-bit)	0x44	0x40	0x40	0x44	0x52	0x44
	OVLO_R	OVLO Rising Threshold	5.85V	5.65V	5.65V	5.65V	5.65V	5.85V
	UVLO_F	UVLO Falling Threshold	2.30V	2.30V	2.30V	2.30V	2.30V	2.30V
	UVLO_H	UVLO Threshold Hysteresis	0.30V	0.30V	0.30V	0.30V	0.30V	0.30V
SIMO	TV_SBB0[7:0]	SBB0 V_{OUT}	1.800V	3.300V	3.300V	0.850V	0.850V	3.000V
	ADE_SBB0	Active-Discharge Resistor Enable	Enabled	Enabled	Enabled	Enabled	Enabled	Enabled
	EN_SBB0[2:0]	SBB0 Enable Control	FPS Slot 2	FPS Slot 1	Off	FPS Slot 0	FPS Slot 0	FPS Slot 2

			OTP LETTER AND SETTINGS					
	TV_SBB1[7:0]	SBB1 Vout	1.100V	4.000V	5.000V	2.000V	2.000V	1.950V
	ADE_SBB1	Active-Discharge Resistor Enable	Enabled	Enabled	Enabled	Enabled	Enabled	Enabled
	EN_SBB1[2:0]	SBB1 Enable Control	FPS Slot 1	FPS Slot 0	Off	FPS Slot 2	FPS Slot 2	FPS Slot 0
	TV_SBB2[7:0]	SBB2 Vout	0.700V	1.500V	1.800V	2.500V	2.500V	1.250V
	ADE_SBB2	Active-Discharge Resistor Enable	Enabled	Enabled	Enabled	Enabled	Enabled	Enabled
	EN_SBB2[2:0]	SBB2 Enable Control	FPS Slot 0	FPS Slot 3	Off	FPS Slot 1	FPS Slot 1	FPS Slot 1
	TV_SBB3[7:0]	SBB3 V_{OUT}	3.300V	1.800V	1.800V	2.050V	2.050V	1.800V
	ADE_SBB3	Active-Discharge Resistor Enable	Enabled	Enabled	Enabled	Enabled	Enabled	Enabled
	EN_SBB3[2:0]	SBB3 Enable Control	FPS Slot 3	FPS Slot 2	FPS Slot 0	Off	Off	Off

Support Materials

The following support materials are available for this device:

- MAX77675 *Register Map*: Full table of registers that can be read from or written to by I^2C.
- MAX77675 *Programmer's Guide*: Basic software implementation guide. (**Note**: The guide applies to both the MAX77655 and MAX77675.)
- MAX77675 *SIMO Calculator*: Tool to determine if a given set of voltages and currents are supported. The tool can be found under **Design Resources** in the product web page.

Voltage Monitors

The device monitors the input voltage (V_{IN}) to ensure proper operation using three comparators (POR, UVLO, and OVLO). These comparators include hysteresis to prevent their outputs from toggling between states during noisy system transitions.

IN POR Comparator

The IN POR comparator monitors V_{IN} and generates a power-on reset signal (POR). When V_{IN} is below V^{POR}, the device is held in reset (RST = 1, POR = 1). When V_{IN} rises above V_{POR}, the device enters shutdown state (RST = 1, POR = 0). See *Figure 5* and *Table 2* for more details.

IN Undervoltage Lockout Comparator

The IN UVLO comparator monitors VIN and generates an INUVLO signal when the V_{IN} falls below the UVLO threshold. The INUVLO signal is provided to the top-level digital controller. See *Figure 5* and *Table 2* for additional information regarding the UVLO comparator:

- When the device is in the Shutdown state, the UVLO comparator is disabled.
- When transitioning out of the Shutdown state, the UVLO comparator is enabled allowing the device to check for sufficient input voltage. If V_{IN} is above the UVLO rising threshold and a wake-up signal is received, the device can transition to the Resource On state; otherwise, the device transitions back to the Shutdown state.

IN Overvoltage Lockout Comparator

The device is rated for 5.5V maximum operating voltage (V_{IN}) with an absolute maximum input voltage of 6.0V. An OVLO monitor increases the robustness of the device by inhibiting operation when the supply voltage is greater than V_{INOVLO}. See *Figure 5* and *Table 2* for additional information regarding the OVLO comparator:

- When the device is in the Shutdown state, the OVLO comparator is disabled.

Thermal Monitors

The MAX77675 has three global on-chip thermal sensors:

- Junction Temperature Alarm 1 → 90°C
- Junction Temperature Alarm 2 → 120°C
- Junction Temperature Shutdown → 145°C

The junction temperature alarms have maskable rising interrupts as well as status bits (see the *Register Map* section for more information). Unmasking these thermal alarms is recommended for all systems. If the first alarm is triggered, the system software should attempt to lower system power dissipation. If the second alarm is triggered, then attempts to lower the power dissipation were unsuccessful and the system software should turn the device off. Finally, if the junction temperature rises to junction temperature shutdown, then the MAX77675 sets the ERCFLAG.TOVLD bit and automatically turns itself off.

After a junction temperature shutdown event, the system can be enabled again. The system software can read the ERCFLAG register during initialization to see ERCFLAG.TOVLD = 1 and log that an extreme thermal event has occurred.

Thermal Shutdown

The MAX77675 has on-chip thermal sensors to monitor thermal overloads. The thermal overload alarm generates a TOVLD signal when the junction temperature exceeds +145°C (T_{JOVLD}). The on/off controller provides TOVLD. When TOVLD is asserted, the on/off controller forces system reset which disables all functions of the MAX77675. Once all functions are disabled, a wake-up event is required to turn the MAX77675 on again. In the case that a wake-up event turns the MAX77675 on when the junction temperature is still above +145°C, the MAX77675's on/off controller promptly forces system reset which disables all functions again. The thermal monitoring function is sampled in low-power mode to save quiescent current. The host can check if a temperature overload occurred by reading the ERCFLAG.TOLVD flag.

Chip Identification

Different OTP variants of the MAX77675 offer different settings such as settings for default output voltages or power sequencing. These OTP variants are identified by the Chip Identification number, which can be read in the CID register.

nEN Enable Input

The nEN is an active-low, internally debounced digital input that typically comes from the system's on-key. The debounce time is programmable with CNFG_GLBL_A.DBEN_nEN. The primary purpose of this input is to generate a wake-up signal for the PMIC, turning on the regulators. Maskable rising/falling interrupts are available for nEN (INTM_GLBL.nEN_R and INTM_GLBL.nEN_F) for alternate functionality.

The nEN input can be configured to work with a push-button (CNFG_GLBL_A.nEN_MODE[1:0] = 0x0), a slide-switch (CNFG_GLBL_A.nEN_MODE[1:0] = 0x1), or a logic output of an external device (CNFG_GLBL_A.nEN_MODE[1:0] = 0x2). See *Figure 2* for more information. In both push-button and slide-switch modes, the on/off controller looks for a falling edge on the nEN input to initiate a power-up sequence. In logic mode, the on/off controller initiates a power-up or power-down sequence depending on the nEN value. There is no debouncing for logic mode.

nEN Manual Reset

The nEN pin works as a manual reset input when the on/off controller is in the Resource On state. The manual reset function is useful for forcing a power-down in case communication with the processor fails. When nEN is configured for push-button mode and the input is asserted (nEN = LOW) for an extended period (t_{MRST}), the on/off controller initiates a power-down sequence and goes to shutdown mode. When nEN is configured for slide-switch mode and the input is deasserted (nEN = HIGH) for an extended period (t_{MRST}), the on/off controller initiates a power-down sequence and goes to shutdown mode. Logic mode does not depend on a manual reset time (t_{MRST}), so when nEN is pulled high, the on/off controller initiates a power-down sequence and goes to shutdown mode. In all modes, the ERCFLAG.MRST flag sets to indicate a reset occurred.

nEN Triple Functionality: Push-Button vs. Slide-Switch vs. Logic

The nEN digital input can be configured to work with a push-button switch, a slide-switch, or a logic output *Figure 2* shows nEN's triple functionality for power-on sequencing and manual reset.

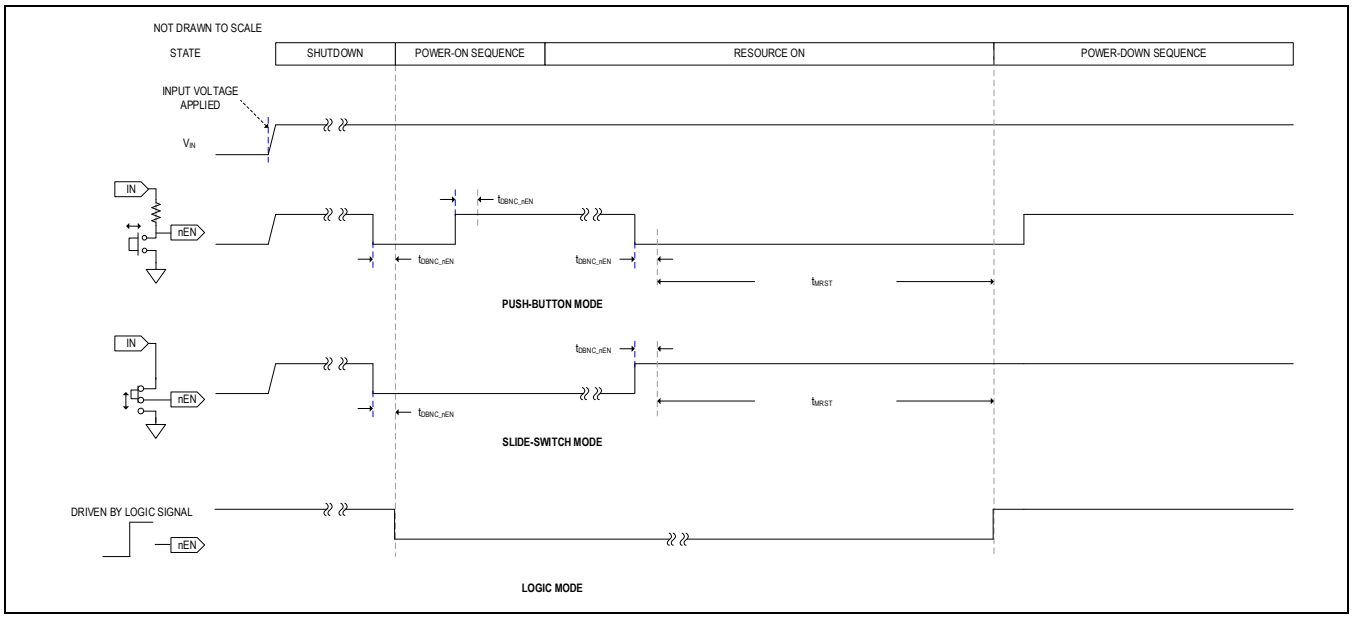


Figure 2. nEN Usage Timing Diagram

Debounced Input

The nEN is debounced on both rising and falling edges to reject undesired transitions. The input must be at a stable logic level for the entire debounce period for the output to change its logic state. *Figure 3* shows an example timing diagram for the nEN debounce.

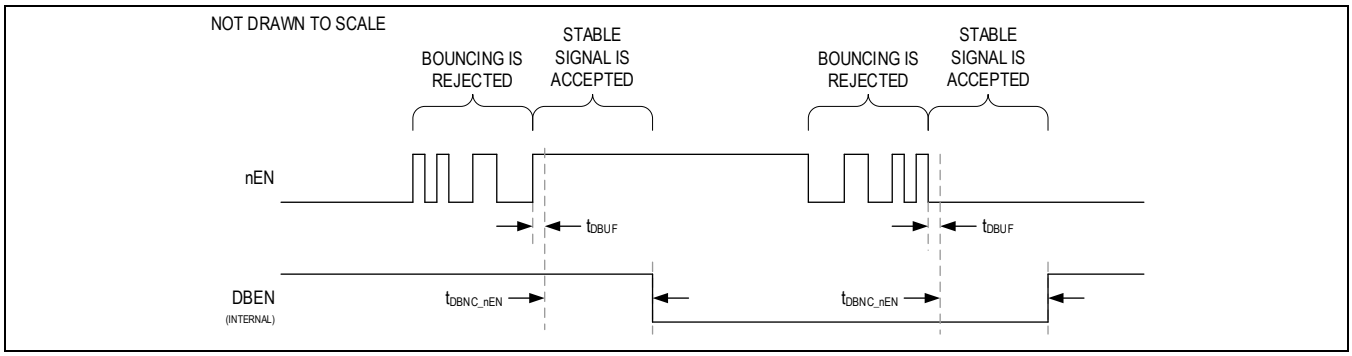


Figure 3. Debounced Input

nEN Internal Pullup Resistors to V_{IN}

The nEN logic thresholds are referenced to V_{IN}. There is an internal pullup resistor between nEN and V_{IN} (R_{nENPU}), which can be enabled by setting CNFG_GLBL_A.PU_DIS = 0. See *Figure 4*. While enabled, the pullup value is approximately 200kΩ. While PU_DIS = 1, the nEN node has high impedance.

Applications using a slide-switch on-key or push-pull digital output connected to nEN can reduce quiescent current consumption by disabling the pullup resistor. Applications using normally-open, momentary, and push-button on-keys (as shown in *Figure 4*) can use the internal resistor to avoid external components.

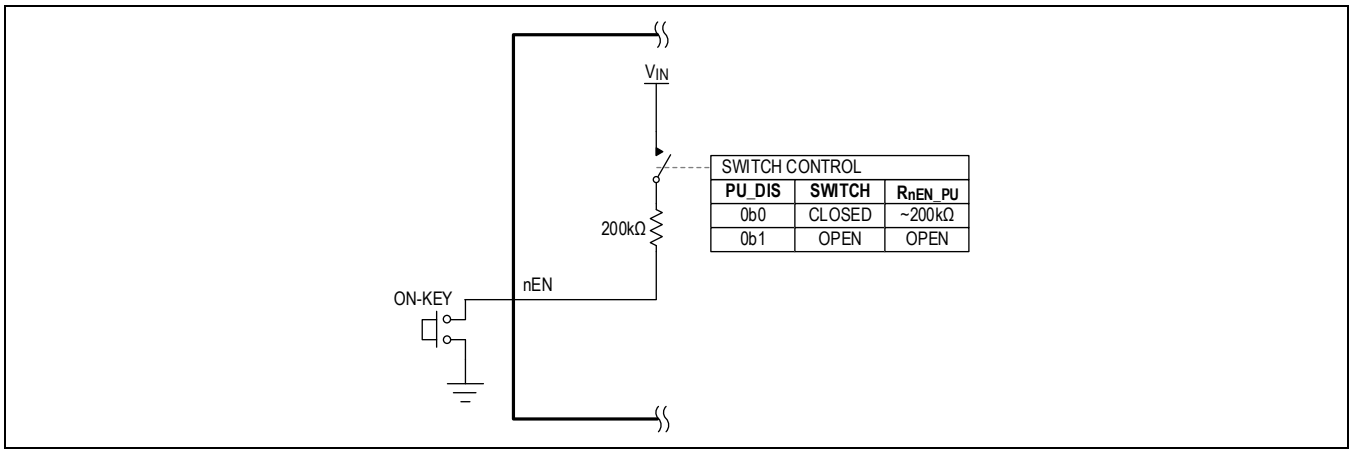


Figure 4. nEN Pullup Resistor Configuration

Interrupts (nIRQ)

Several status, interrupt, and interrupt mask registers monitor key information and update when an interrupt event has occurred. See the *Register Map* section for a comprehensive list of all interrupt bits and status registers.

Depending on OTP, some or all interrupts are masked by default. Initialization software should unmask interrupts of interest.

The nIRQ is an active-low, open-drain output typically routed to a processor's interrupt input for triggering off interrupt events. When any unmasked interrupt occurs, this pin is asserted (LOW). A pullup resistor is required for this signal, and is typically found inside the host processor. If one is unavailable, a board-mounted pullup resistor is required.

On/Off Controller

The on/off controller monitors multiple power-up (wake-up) and power-down (shutdown) conditions to enable or disable resources that are necessary for the system and its processor to move between its operating modes.

Many systems have one power management controller and one processor and rely on the on/off controller to be the master controller. In this case, the on/off controller receives the wake-up events and enables some or all of the regulators in order to power up a processor. This processor then manages the system. To conceptualize this operation, see *Figure 5* and *Table 2*. A typical path through the on/off controller during power-up is as follows:

- Apply power to IN and start in the Shutdown state.
- Press the system's on-key (nEN = LOW) and follow transitions 2, 3A, and 4 to the Resource On state.
- The device performs its desired functions in the Resource On state. When a manual reset occurs, the device follows transitions 5A, 6, and 10 to the Shutdown state.

Some systems have several power management blocks, a main processor, and subprocessors. These systems can use this device as a subpower management block for a peripheral portion of circuitry as long as there is an I^2C port available from a higher level processor. To conceptualize this slave operation, see *Figure 5* and *Table 2*. Optionally, to avoid delay from debouncing the nEN pin, systems should use the MAX77675 with nEN configured to be in logic mode (CNFG_GLBL_A.nEN_MODE[1:0] = 0b10) by OTP. A typical path through the on/off controller used in this way is as follows:

- Apply power to IN and start in the Shutdown state.
- When the higher level processor wants to turn on this device's resources, it pulls nEN LOW to follow transitions 2, 3A, and 4 to the Resource On state.
- The higher level processor can control this device's resources with I^2C commands (e.g., turn on/off regulators).
- When the higher level processor is ready to turn this device off, it turns off everything through the I^2C either with a software command (CNFG_GLBL_B.SFT_CTRL[1:0]) or pulling nEN high to transition along paths 5A, 6, and 10 to the Shutdown state.
- If the higher level processor wants to power down outputs on the FPS but keep the bias enabled (for I^2C communication), it sends a SFT_STBY command (CNFG_GLBL_B.SFT_CTRL[1:0] = 0x3) to transition along paths 5B and 6 to the Standby state.

- Afterward, to exit standby state, the processor sends a SFT_EXIT_STBY command (CNFG_GLBL_B.SFT_CTRL[1:0] = 0x4) to transition along path 7 back to the wake-up action, eventually going back to the Resource On state.

Top Level On/Off Controller

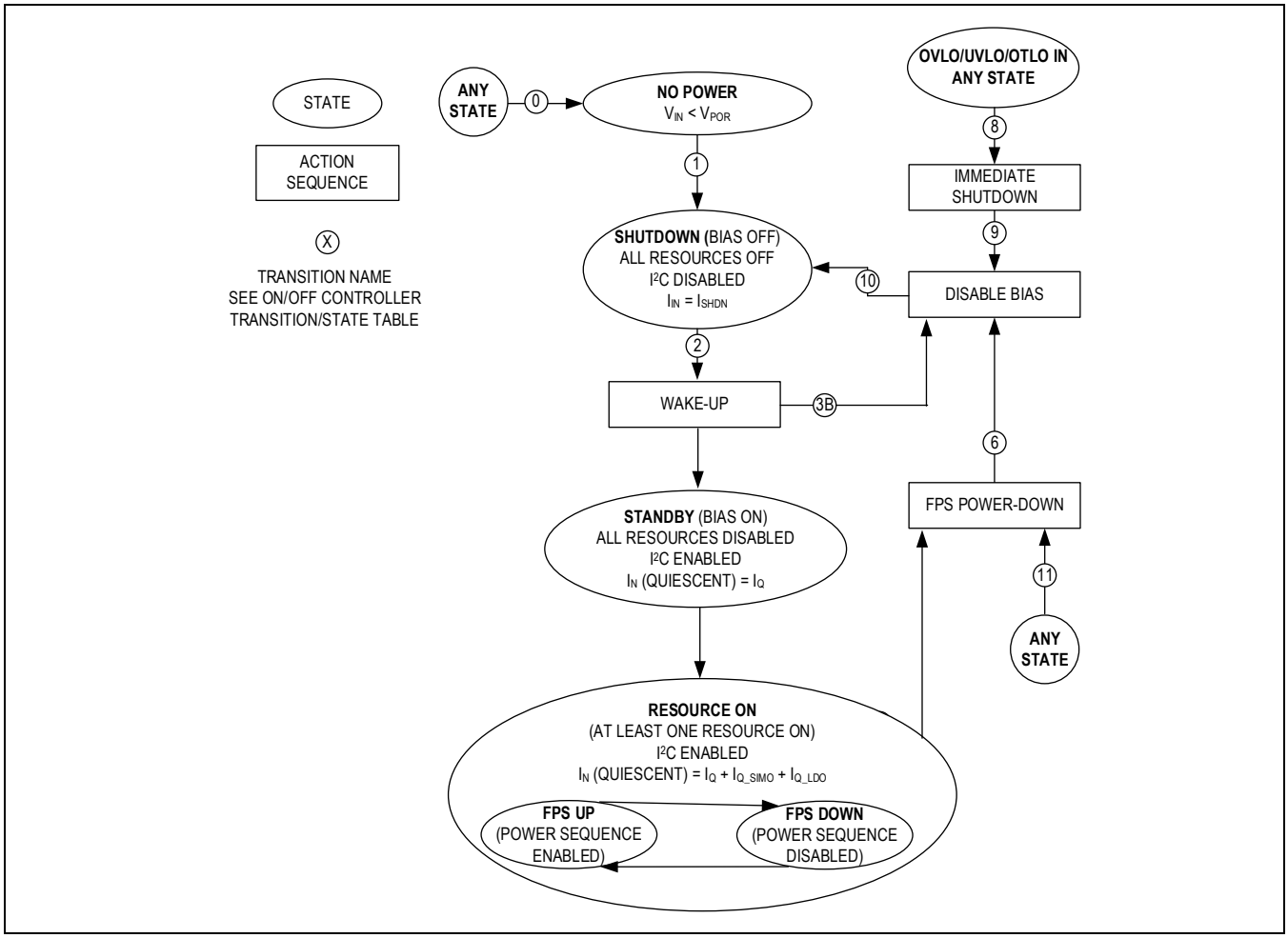


Figure 5. On/Off Controller State Diagram

Table 2. On/Off Controller Transition/State

TRANSITION/STATE	CONDITION
0	IN voltage is below the POR threshold (V_{IN} < V_{POR}).
1	IN voltage is above the POR threshold (V_{IN} < V_{POR}).
SHUTDOWN	The device is waiting for a wake-up signal to enable the main bias circuits. • This is the lowest current state of the device (I_Q ~ 0.3pA) • Main bias circuits and I²C are off. POR comparator is on • The ERCFLAG register value is preserved
2	A wake-up signal is received. • A debounced on-key (nEN) falling edge is detected (push-button or slide-switch mode) **OR** • nEN is LOW (logic mode) **OR** • Internal wake-up flag is set due to cold reset command
3	No faults detected. In the ERCFLAG register: UVLO = 0, OVLO = 0, TOVLD = 0.
4	Power-up sequence is complete.

TRANSITION/STATE	CONDITION
RESOURCE ON	Flexible power sequencer went through power-up and I2C is on. The main bias circuits are enabled.
5A	Request to power-down is received. • Software cold reset (CNFG_GLBL_B.SFT_CTRL[1:0] = 0b01) occurred **OR** • Software power off (CNFG_GLBL_B.SFT_CTRL[1:0] = 0b10) occurred **OR** • Manual reset occurred
5B	I2C command SFT_STBY received to enter standby mode
STANDBY	The device is waiting for a wake-up signal to restart. • SIMO channels on the FPS are off. • SIMO channels that were forced on (CNFG_SBBx_B.EN_SBBx[2:0] = 0x6 or 0x7) stay on • The main bias circuits are enabled, and I^2C is on. • Main bias circuits are in low-power mode if CNFG_GLBL_A.BIAS_LPM = 1.
6	Power-down sequence is finished.
7	Wake-up signal received. • A debounced on-key (nEN) falling edge is detected (push-button mode) **OR** • I^2C wake-up command SFT_EXIT_STBY received **OR** • Manual reset occurred
8	• System overtemperature lockout ($T_J > T_{OTLO}$) **OR** • System undervoltage lockout ($V_{IN} < V_{INUVLO}$) **OR** • System overvoltage lockout ($V_{IN} > V_{INOVLO}$)
9	Immediate shutdown is finished.
10	Bias is disabled.
11	nEN is HIGH (logic mode).

Internal Wake-Up Flags

After transitioning to the Shutdown state because of a reset, to allow the device to power-up again, internal wake-up flags are set to remember the wake-up request. In *Figure 5* and *Table 2*, these internal wake-up flags trigger transition 2. The internal wake-up flags are set when any of the following happens:

- While in push-button or slide-switch mode, nEN is debounced (see the *nEN Enable Input* section)
  - For example, after a push button is pressed or a slide-switch is switched to HIGH
- While in logic mode, nEN is LOW (see the *nEN Enable Input* section)
- Software Cold Reset command sent (CNFG_GLBL.SFT_CTRL[1:0] = 0b01)

On/Off Controller Actions

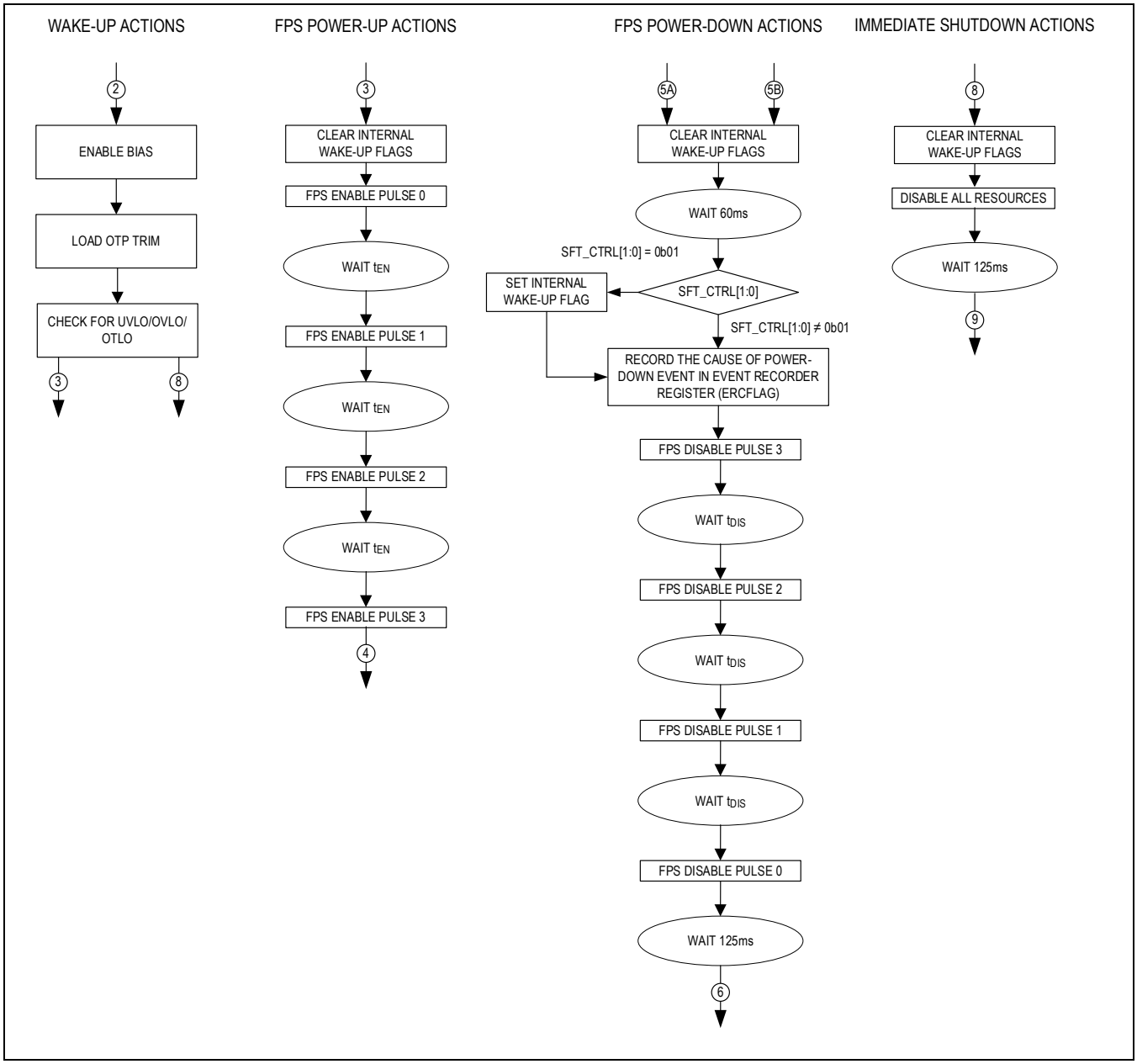


Figure 6. On/Off Controller Actions

Flexible Power Sequencer

The FPS allows resources to power up under hardware or software control. Additionally, each resource can power up independently or among a group of other regulators with adjustable power-up and power-down slots (sequencing). *Figure 7* shows four resources powering up under the control of the FPS.

The flexible sequencing structure consists of one master sequencing timer and four slave resources (SBB0, SBB1, SBB2, and SBB3). When the FPS is enabled, a master timer generates four sequencing events for device power-up and powerdown.

Therefore, the power-down sequence has a total delay up to 195.24ms (60ms + 4 x 2.56ms power-down slot delays + 125ms output discharge delay). If issuing the Software Cold Reset (CNFG_GLBL_A.SFT_CTRL[1:0]), then wait more than 200ms before issuing additional commands through the I^2C.

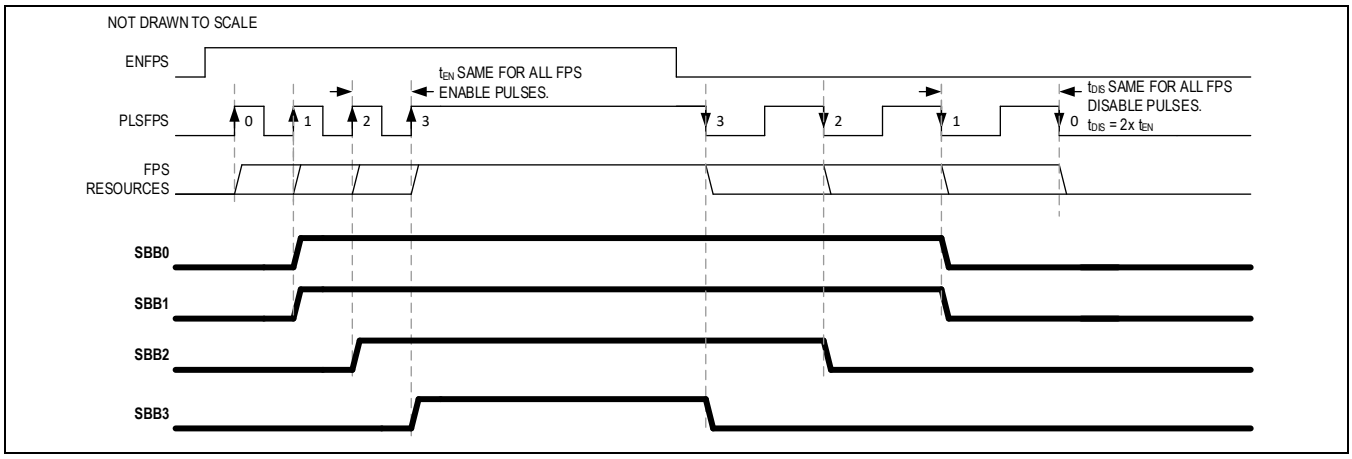


Figure 7. Flexible Power Sequencer Basic Timing Diagram

Startup Timing Diagram Due to nEN

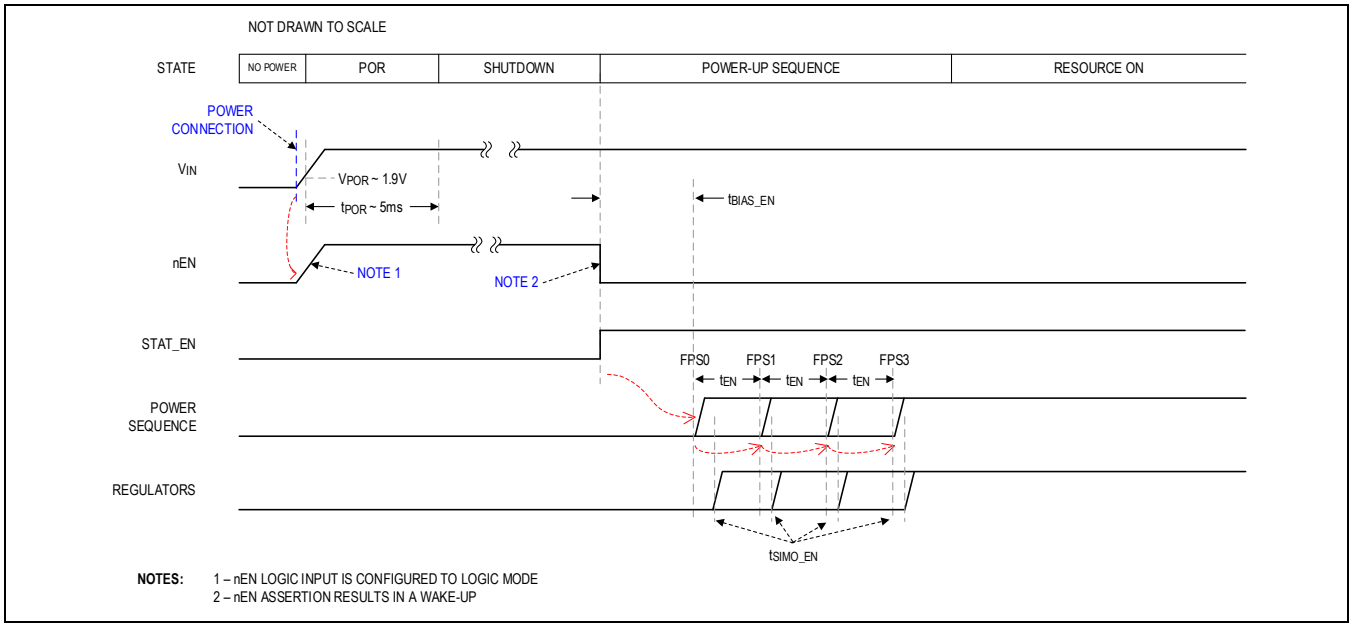


Figure 8. Startup Timing Diagram Due to nEN (Logic Mode)

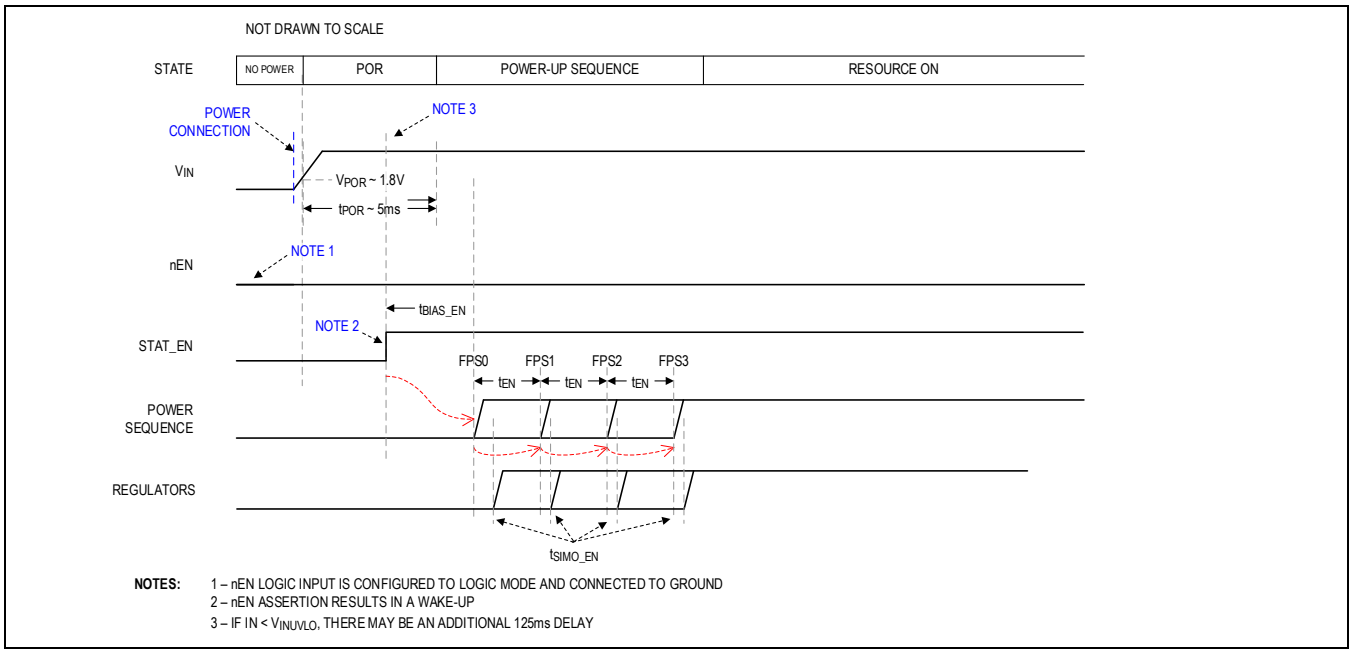


Figure 9. Startup Timing Diagram Due to nEN (Logic Mode; nEN Connected to Ground)

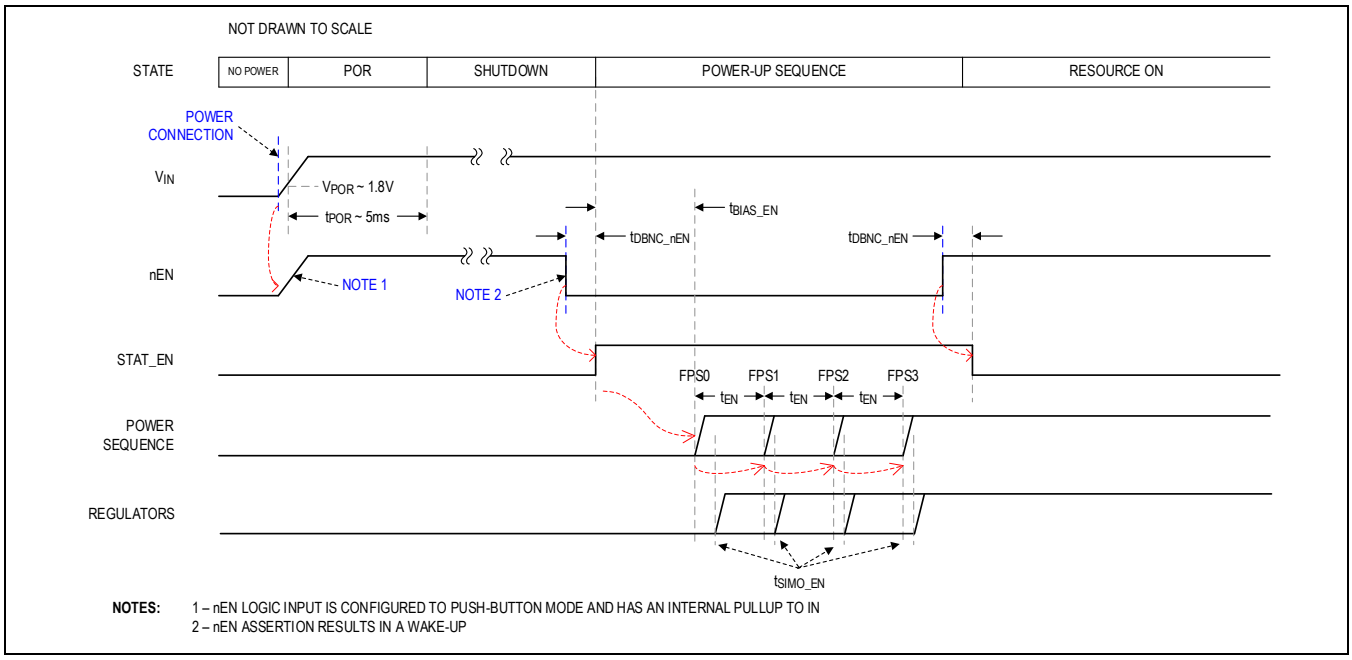


Figure 10. Startup Timing Diagram Due to nEN (Push-Button Mode)

Low-Power Mode

To request the device to enter low-power mode, set CNFG_GLBL_A.BIAS_LPM = 1. This sets both the bias and the SIMO regulator to a lower-power state, reducing quiescent current through signal sampling techniques. The sampling technique reduces quiescent current but increases output voltage ripple and slows down transient response.

Detailed Description—SIMO Buck-Boost

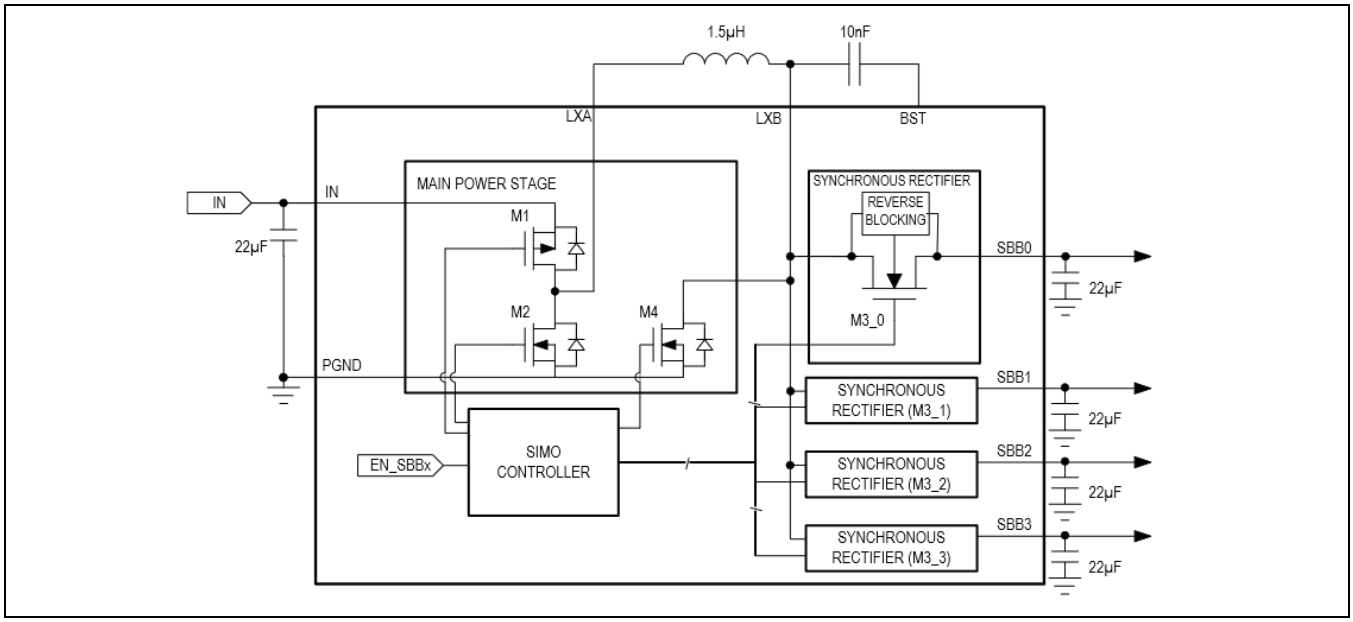


Figure 11. SIMO Simple Block Diagram

The SIMO buck-boost DC-to-DC converter is designed for applications emphasizing low quiescent current and small solution size. A single inductor is used to regulate four separate outputs, saving board space while delivering total system efficiency better than equivalent power solutions using one buck and linear regulators.

For battery applications, the SIMO configuration utilizes the entire battery voltage range due to its ability to create output voltages that are above, below, or equal to the input voltage.

Benefits and Features

- Four Output Channels
- Ideal for Low-Power Designs
  - Delivers > 700mA at 1.8V Output from a 3.7V Input
  - ±2% Accurate Output Voltage
- Small Solution Size
  - Multiple Outputs from a Single Inductor
- Flexible and Easy to Use
  - Automatic Transitions Between Buck, Buck-Boost, and Boost Operating Modes
  - Programmable, On-Chip Active Discharge
- Long Battery Life
  - High Efficiency, 90% Efficiency at 1.8V Output
  - Better Total System Efficiency than a Discrete Buck + LDOs Solution
  - Low Quiescent Current: 0.2 µA Typical for Each Additional Output in Low-Power Mode
  - Low Input Operating Voltage: 2.5V Minimum

Inductor Valley Current

The MAX77675 regulates inductor valley current or the lowest point in an inductor current cycle. Under light loads, in which inductor valley current is 0A, the SIMO regulator operates in discontinuous conduction mode (DCM). If DCM delivers insufficient energy to maintain any output voltage, the regulator switches to continuous conduction mode, raising valley current above 0A. As load current increases, the valley current also increases in discrete steps. *Figure 12* demonstrates how it increases or decreases with changing load current.

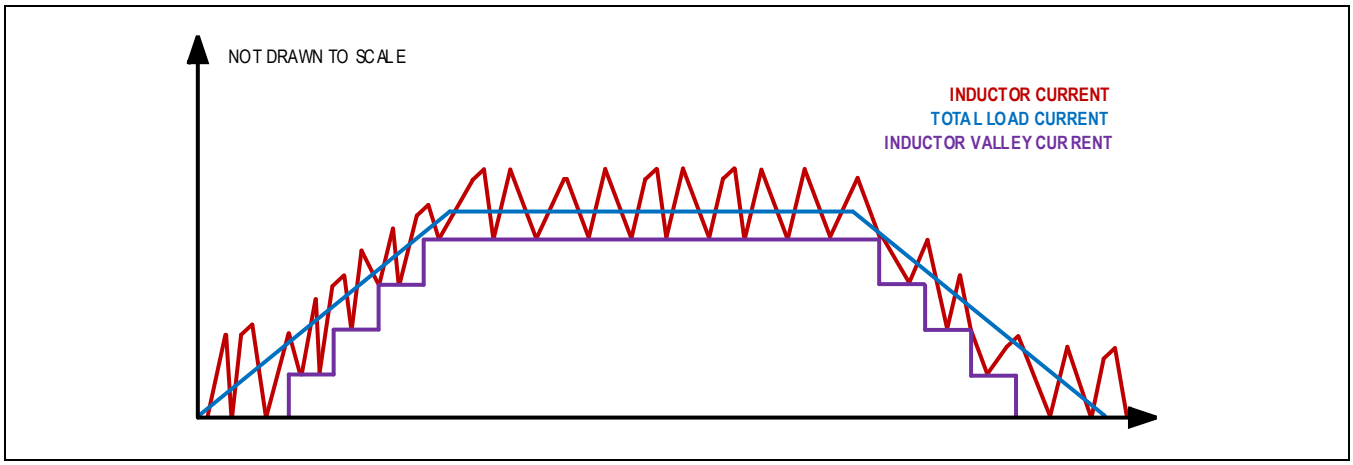


Figure 12. Valley Current Control with Changing Load Current

See the *Typical Operating Characteristics* section for examples.

SIMO Control Scheme

The SIMO buck-boost is designed to service multiple outputs simultaneously. A proprietary controller ensures that all outputs are serviced in a timely manner, even while multiple outputs are contending for the energy stored in the inductor. When no regulator needs service and low-power mode is enabled, the state machine rests in a low-power rest state.

Drive Strength

The SIMO regulator's drive strength for its internal power MOSFETs is adjustable using the CNFG_SBB_TOP.DRV_SBB[1:0] bit field. Faster drive strength results in higher efficiency but requires stricter layout rules or shielding to avoid additional EMI. Slower settings limit EMI in non-ideal settings (e.g., contained layout, antennae adjacent to the device) but lower efficiency. Change the drive strength only once during system initialization.

SIMO Channel Operating Mode

Each SIMO channel can individually operate in one of the three modes (buck, buck-boost, or boost) depending on the output voltage to input voltage ratio. The operating mode is automatically chosen based on the V_{SBBx}/V_{IN} ratio as shown in *Table 3*.

Table 3. SIMO Operating Mode Thresholds

OPERATING MODE	OUTPUT VOLTAGE TO INPUT VOLTAGE RATIO RANGE
Buck Mode	$V_{SBBx}/V_{IN} < 0.6$
Buck-Boost Mode	$0.6 < V_{SBBx}/V_{IN} < 1.25$
Boost Mode	$1.25 < V_{SBBx}/V_{IN}$

Examples

Given IN = 3.1V, SBB0 = 1.8V, SBB1 = 5.0V, SBB2 = 0.7V, and SBB3 = 3.3V, the operating mode for each channel is shown in *Table 4*.

Table 4. Operating Mode Examples

	VOLTAGE (V)	SBBx/IN RATIO	OPERATING MODE
SBB0	1.8	0.581	Buck
SBB1	5.0	1.351	Boost
SBB2	0.7	0.226	Buck
SBB3	3.3	1.064	Buck-Boost

Buck Mode

When an output needs service, switch M3_x remains closed and M4 remains open (see *Figure 11*). M1 and M2 are toggled as in a traditional buck converter. That is, M1 is closed and M2 is open to both deliver energy to the output and charge the inductor. Then, M1 is open and M2 is closed to deliver energy stored in the inductor to the output.

Buck-Boost Mode

Unlike traditional buck-boost regulators, the SIMO regulator uses a three-state buck-boost control scheme. First, M1 and M4 are closed to charge the inductor. Then, M4 is open and M3_x is closed. This is similar to a buck regulator state, delivering energy to the output while continuing to charge the inductor. Finally, M1 is open and M2 is closed delivering energy stored in the inductor to the output.

The second state improves efficiency in buck-boost mode compared to traditional control schemes.

Boost Mode

When an output needs service, switch M1 remains closed and M2 remains open. M3_x and M4 are toggled as in a traditional boost converter. That is, M3_x is open and M4 is closed to charge the inductor. Then, M3_x is closed and M4 is open to deliver energy to the output from both the input and the charged inductor.

Channel-to-Channel Switching

To lower output voltage ripple, the regulator might switch directly from one channel to another using a proprietary algorithm. During the transition from one channel to another, the LXB node is temporarily connected to ground.

SIMO Soft-Start

The soft-start feature of the SIMO limits inrush current during startup, achieved by limiting the slew rate of the output voltage during startup (dV/dt_{SS}).

More output capacitance results in higher input current surges during startup. The following example and set of equations describe this phenomenon during startup.

The current into the output capacitor (I_{CSBB}) during soft-start is as follows:

$$I_{CSBB} = C_{SBB}\frac{dV}{dt_{SS}} \quad (Equation 1)$$

where:

- C_{SBB} is the capacitance on the output of the regulator
- dV/dt_{SS} is the voltage change rate of the output

The input current (I_{IN}) during soft-start is as follows:

$$I_{IN} = \frac{(I_{CSBB} + I_{LOAD})\frac{V_{SBBx}}{V_{IN}}}{\xi} \quad (Equation 2)$$

where:

- I_{CSBB} is from Equation 1
- I_{LOAD} is the current consumed from the external load
- V_{SBBx} is the output voltage
- V_{IN} is the input voltage
- ξ is the efficiency of the regulator
- For example, given the following conditions, the peak input current (I_{IN}) during soft-start is ~71mA.

Given:

- V_{IN} = 3.5V
- V_{SBB2} = 3.3V
- C_{SBB2} = 22µF
- dV/dt_{SS} = 2mV/µs
- R_{LOAD2} = 330Ω (I_{LOAD2} = 3.3V/330Ω = 10mA)
- ξ = 86%

Calculation:

- I_{CSBB} = 22µF x 2mV/µs (from Equation 1)
- I_{CSBB} = 44mA
- $I_{IN} = \frac{(44mA+10mA)\frac{3.3V}{3.5V}}{0.86}$ (from Equation 1)
- I_{IN} ~ 59.2mA

Rising Slew Rate

The rising slew rate while output voltage is increasing to a higher target output voltage is controlled by the CNFG_SBB_TOP_B.SR_SBBx and CNFG_SBB_TOP_B.DVS_SLEW bits. *Table 5* shows which slew rate options are available.

- This only applies to rising slew rates. Falling slew rates are mainly determined by load current.
- Actual rising slew rate may be lower depending on output capacitance and load current.

Table 5. Output Voltage Rising Slew Rates

SR_SBBx	DVS_SLEW	SLEW RATE
0	Don't Care	2mV/ps
1	0	5mV/ps
1	1	10mV/ps

Delay in Changing Output Voltage

When an i^2C command is sent to increase output voltage, there is a delay between the command and the output voltage changing. This delay is around 100ps but can be reduced by setting CNFG_SBB_TOP_B.LAT_MODE = 1, which reduces the delay to around 10ps. While LAT_MODE = 1, the bias is in normal power mode.

When LAT_MODE = 1, also set CNFG_sBB_TOP_B.sR_sBBx = 1. if sR_sBBx = 0, LAT_MODE is ignored.

SIMO Registers

The CNFG_sBB_TOP registers control all siMO channels, modifying parameters such as drive strength and output voltage step size. Each siMO buck-boost channel has a dedicated register to program its target output voltage (CNFG_sBBx_A.TV_sBBx[7:0]). Additional controls are available in the CNFG_sBBx_B register for enabling/disabling the active discharge resistors (ADE_sBBx) and enabling/disabling the siMO buck-boost channels (EN_sBBx[2:0]). To monitor each channel in real time for overload, read the sTAT_GLBL.sBBx_s bits. To check if a channel was overloaded in the past, read the iNT_GLBL.sBBx_F flags. Note that the interrupt flags are cleared upon reading.

For a full description of bits, registers, default values, and reset conditions, see the Register Map section.

SIMO Active Discharge Resistance

Each siMO buck-boost channel has an active-discharge resistor (R_{ADsBBx}) that is automatically enabled/disabled based on a CNFG_sBBx_B.ADE_sBBx and the status of the siMO regulator. The active discharge feature may be enabled (CNFG_sBBx_B.ADE_sBBx = 1) or disabled (CNFG_sBBx_B.ADE_sBBx = 0) independently for each siMO channel. Enabling the active discharge feature helps ensure a complete and timely power down of all system peripherals

If the active-discharge resistor is enabled, then it is enabled whenever the respective channel is disabled.

Bootstrap Refresh

The bootstrap capacitor (connected between the BST and LXB pins) is refreshed when one of the following conditions is true:

- The capacitor has not been refreshed for a predetermined amount of time.
- While switching among three channels to service each one, none of those switching states connected LXB to ground.

Detailed Description—I²C Serial Interface

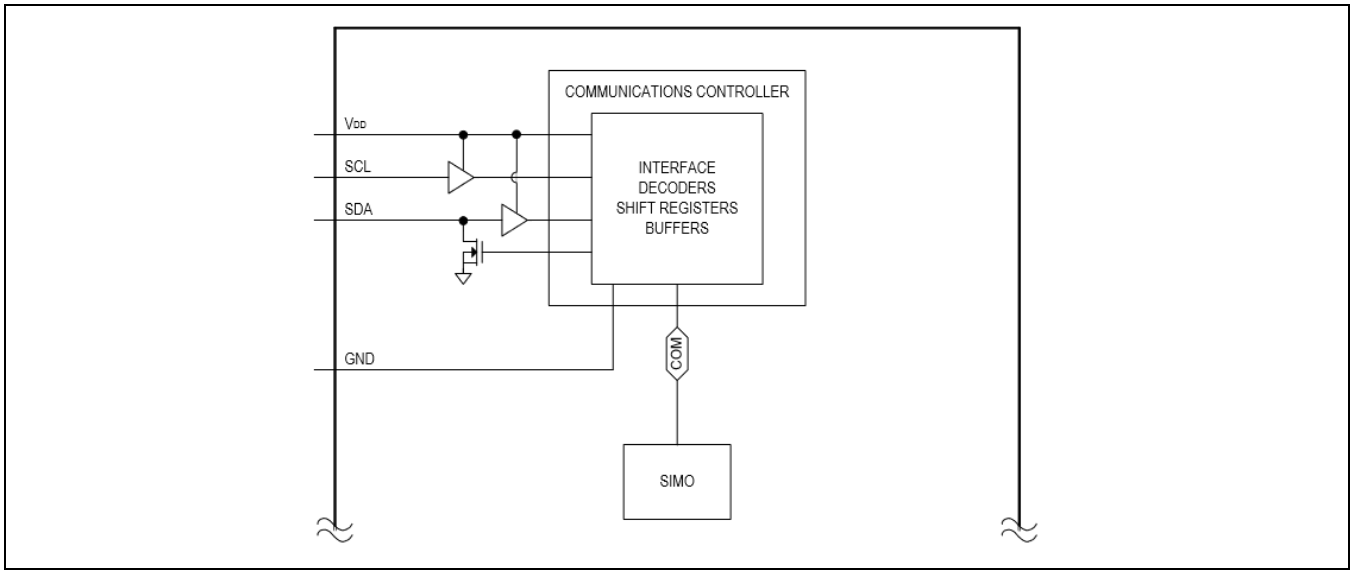


Figure 13. I²C Simplified Block Diagram

This device features a revision 3.0 I²C-compatible, two-wire serial interface consisting of a bidirectional serial data line (SDA) and a serial clock line (SCL). This device acts as a slave-only device and depends on the master to generate the clock signal. The SCL clock rates from 0Hz to 3.4MHz are supported. The I²C serial communication is an open-drain bus and therefore, SDA and SCL require pullups. Optional resistors (24Ω) in series with SDA and SCL protect the device inputs from high-voltage spikes on the bus lines. Series resistors also minimize crosstalk and undershoot on bus signals. *Figure 13* shows the functional diagram for the I²C-based communications controller. For additional information on I²C, refer to the I²C bus specification and user manual, which is available for free through the internet.

Benefits and Features

- I²C Revision 3.0 Compatible Serial Communications Channel
- 0Hz to 100kHz (Standard Mode)
- 0Hz to 400kHz (Fast Mode)
- 0Hz to 1MHz (Fast-Mode Plus)
- 0Hz to 3.4MHz (High-Speed Mode)

I²C System Configuration

The I²C bus is a multimaster bus. The maximum number of devices that can attach to the bus is only limited by bus capacitance.

A device on the I²C bus that sends data to the bus is called a transmitter. A device that receives data from the bus is called a receiver. The device that initiates a data transfer and generates the SCL clock signals to control the data transfer is a master. Any device that is being addressed by the master is considered a slave. The I²C-compatible interface operates as a slave on the I²C bus with transmit and receive capabilities.

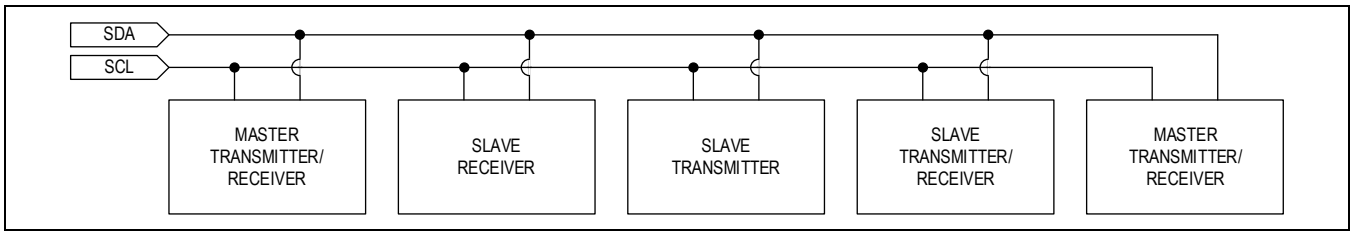


Figure 14. I²C System Configuration

I²C Interface Power

The I²C interface derives its power from V_{DD}. Bypass the V_{DD} pin with a local 1µF ceramic capacitor to ground.

I²C Data Transfer

One data bit is transferred during each SCL clock cycle. The data on SDA must remain stable during the high period of the SCL clock pulse. Changes in SDA while SCL is high are control signals. See the *I2C Start and Stop Conditions* section. Each transmit sequence is framed by a START (S) condition and a STOP (P) condition. Each data packet is nine bits long: eight bits of data followed by the acknowledge bit. Data is transferred with the MSB first.

I²C Start and Stop Conditions

When the serial interface is inactive, SDA and SCL idle high. A master device initiates communication by issuing a START condition. A START condition is a high-to-low transition on SDA with SCL high. A STOP condition is a low-to-high transition on SDA, while SCL is high. See *Figure 15*.

A START condition from the master signals the beginning of a transmission to a slave. The master terminates transmission by issuing a not acknowledge followed by a STOP condition (see the *I2C Acknowledge Bit* section for information on not acknowledge). The STOP condition frees the bus. To issue a series of commands to the slave, the master can issue repeated start (Sr) commands instead of a STOP command to maintain control of the bus. In general, a repeated start command is functionally equivalent to a regular start command.

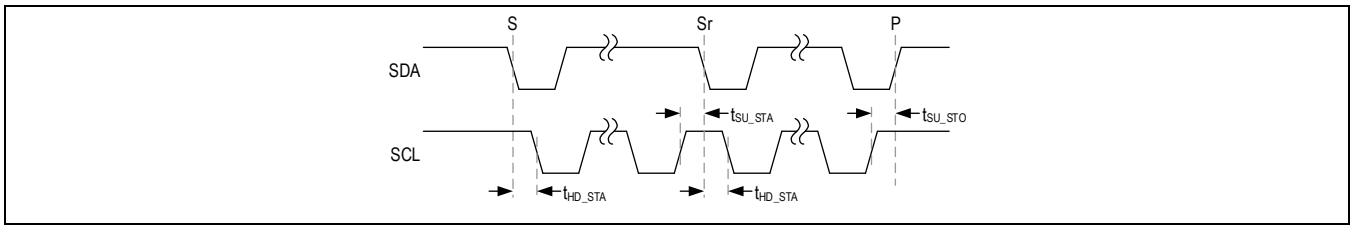


Figure 15. I²C Start and Stop Conditions

I²C Acknowledge Bit

Both the I²C bus master and this device generate acknowledge bits when receiving data. The acknowledge bit is the last bit of each nine-bit data packet. To generate an acknowledge (A), the receiving device must pull SDA low before the rising edge of the acknowledge-related clock pulse (ninth pulse) and keep it low during the high period of the clock pulse. See Figure 16. To generate a not acknowledge (nA), the receiving device allows SDA to be pulled high before the rising edge of the acknowledge-related clock pulse and leaves it high during the high period of the clock pulse.

Monitoring the acknowledge bits allows for detection of unsuccessful data transfers. An unsuccessful data transfer occurs if a receiving device is busy or if a system fault has occurred. In the event of an unsuccessful data transfer, the bus master should reattempt communication at a later time.

This device issues an ACK for all register addresses in the possible address space even if the particular register does not exist.

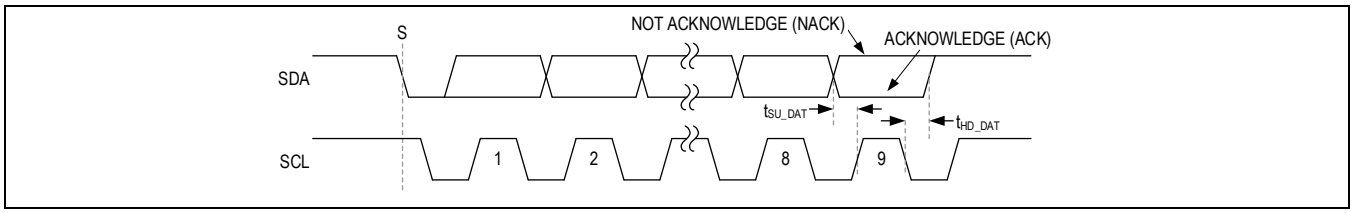


Figure 16. Acknowledge Bit

I²C Slave Address

The I²C controller implements seven-bit slave addressing. An I²C bus master initiates communication with the slave by issuing a START condition followed by the slave address. See *Figure 17*. The address is factory-programmable. See *Table 6*. All slave addresses not mentioned in *Table 6* are not acknowledged.

Table 6. I²C Slave Address Options

ADDRESS	7-BIT SLAVE ADDRESS	8-BIT WRITE ADDRESS	8-BIT READ ADDRESS
Main Address (ADDR[1:0] = 0x0)*	0x40, 0b 100 0000	0x80, 0b 1000 0000	0x81, 0b 1000 0001
Main Address (ADDR[1:0] = 0x1)*	0x44, 0b 100 0100	0x88, 0b 1000 1000	0x89, 0b 1000 1001
Main Address (ADDR[1:0] = 0x2)*	0x48, 0b 100 1000	0x90, 0b 1001 0000	0x91, 0b 1001 0001
Main Address (ADDR[1:0] = 0x3)*	0x52, 0b 101 0010	0xA4, 0b 1010 0100	0xA5, 0b 1010 0101
Test Mode**	0x49, 0b 100 1001	0x92, 0b 1001 0010	0x93, 0b 1001 0011

Perform all reads and writes on the Main Address. The ADDR is a factory OTP option, allowing for address changes in the event of a bus conflict. *Contact support* for more information.

**When test mode is unlocked, the additional address is acknowledged. Test mode details are confidential. If possible, leave the test mode address unallocated to allow for the rare event that debugging needs to be performed in cooperation with Analog Devices.

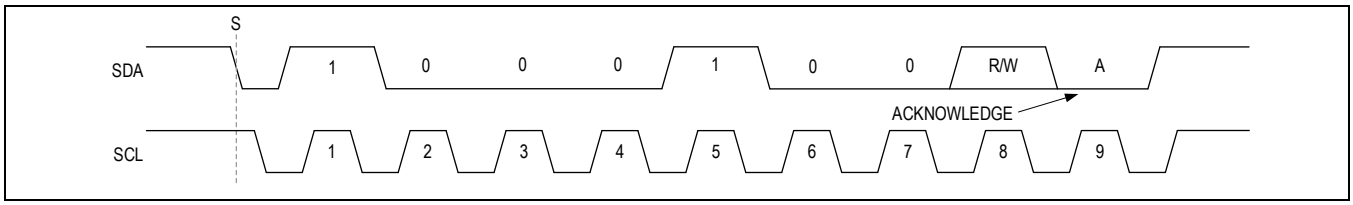


Figure 17. Slave Address Example

I²C Clock Stretching

In general, the clock signal generation for the I²C bus is the responsibility of the master device. The I²C specification allows slow slave devices to alter the clock signal by holding down the clock line. The process in which a slave device holds down the clock line is typically called clock stretching. This device does not use any form of clock stretching to hold down the clock line.

I²C General Call Address

This device does not implement the I²C specifications general call address and does not issue an acknowledge for a general call address (0b0000 0000).

I²C Device ID

This device does not support the I²C Device ID feature.

I²C Communication Speed

This device is compatible with all four communication speed ranges as defined by the I²C Revision 3.0 specification:

- 0Hz to 100kHz (Standard Mode)
- 0Hz to 400kHz (Fast Mode)
- 0Hz to 1MHz (Fast-Mode Plus)
- 0Hz to 3.4MHz (High-Speed Mode)

Operating in standard mode, fast mode, and fast-mode plus does not require any special protocols. The main consideration when changing the bus speed through this range is the combination of bus capacitance and pullup resistors. Larger values of bus capacitance and pullup resistance increase the time constant (C x R), slowing bus operation. Therefore, when increasing bus speeds, the pullup resistance must be decreased to maintain a reasonable time constant. Refer to the Pullup Resistor Sizing section of the I²C bus specification and user manual for detailed guidance on the pullup resistor selection. In general for bus capacitances of 200pF, a 100kHz bus needs 5.6kΩ pullup resistors, a 400kHz bus needs about 1.5kΩ pullup resistors, and a 1MHz bus needs 680Ω pullup resistors. Note that when the open-drain bus is low, the pullup resistor is dissipating power, lower value pullup resistors dissipate more power (V^2/R).

Operating in high-speed mode requires some special considerations. For a full list of considerations, refer to the publicly available I2C bus specification and user manual. Major considerations with respect to this device are as follows:

- The I2C bus master uses current source pullups to shorten the signal rise.
- The I2C slave must use a different set of input filters on its SDA and SCL lines to accommodate for the higher bus.
- The communication protocols need to utilize the high-speed master code.

At power-up and after each stop condition, the I2C input filters are set for standard mode, fast mode, and fast-mode plus (i.e., 0Hz to 1MHz). To switch the input filters for high-speed mode, use the high-speed master code protocols that are described in the *I2C Communication Protocols* section.

I2C Communication Protocols

This device supports both writing and reading from its registers.

Writing to a Single Register

Figure 18 shows the protocol for the I2C master device to write one byte of data. This protocol is the same as the SMBus specification's write byte protocol.

The write byte protocol is as follows:

- The master sends a start command (S). _
- The master sends the 7-bit slave address followed by a write bit (R/$\overline{W}$ = 0).
- The addressed slave asserts an acknowledge (A) by pulling SDA low.
- The master sends an 8-bit register pointer.
- The slave acknowledges the register pointer.
- The master sends a data byte.
- The slave updates with the new data.
- The slave asserts an acknowledge or a not acknowledge for the data byte. The next rising edge on SDA loads the data byte into its target register and the data becomes active.
- The master sends a stop condition (P) or a repeated start condition (Sr). Issuing a P ensures that the bus input filters are set for 1MHz or slower operation. Issuing an Sr leaves the bus input filters in their current state.

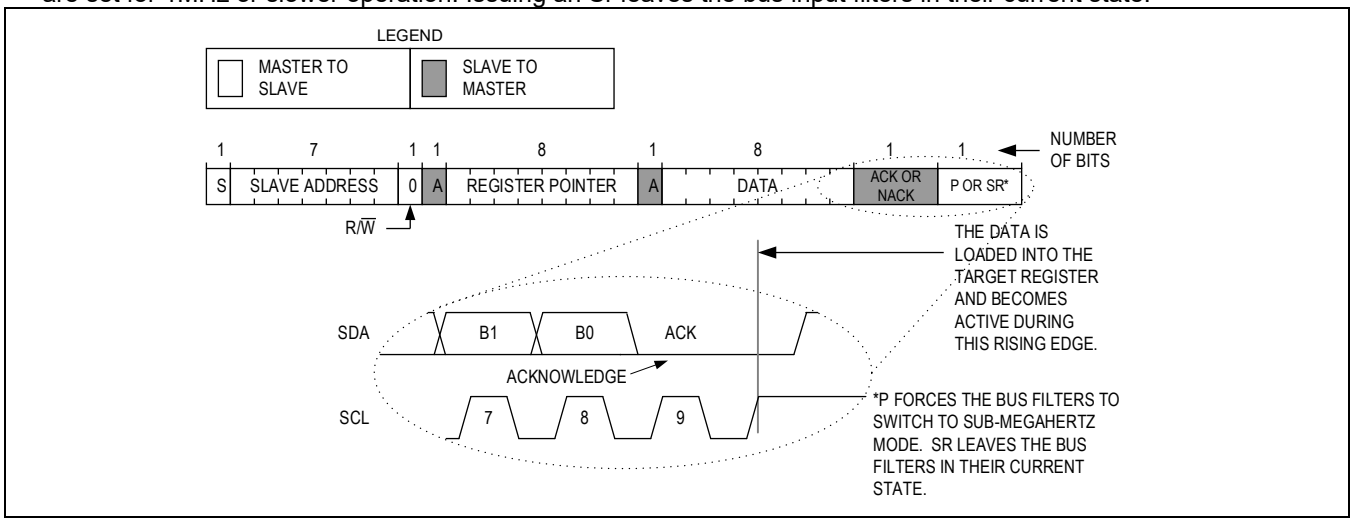


Figure 18. Writing to a Single Register with the Write Byte Protocol

Writing Multiple Bytes to Sequential Registers

Figure 19 shows the protocol for writing to sequential registers. This protocol is similar to the write byte protocol described in the *Writing to a Single Register* section except that the master continues to write after it receives the first byte of data. When the master is done writing, it issues a stop or repeated start.

The protocol for writing to sequential registers is as follows:

- The master sends a start command (S). _
- The master sends the 7-bit slave address followed by a write bit (R/$\overline{W}$ = 0).

- The addressed slave asserts an acknowledge (A) by pulling SDA low.
- The master sends an 8-bit register pointer.
- The slave issues an acknowledge for the register pointer.
- The master sends a data byte.
- The slave issues an acknowledge for the data byte. The next rising edge on SDA loads the data byte into its target register and the data becomes active.
- Steps 6 to 7 are repeated as many times as the master requires.
- During the last issued acknowledge-related clock pulse, the master can issue an acknowledge or a not acknowledge.
- The master sends a stop condition (P) or a repeated start condition (Sr). Issuing a P ensures that the bus input filters are set for 1MHz or slower operation. Issuing an Sr leaves the bus input filters in their current state.

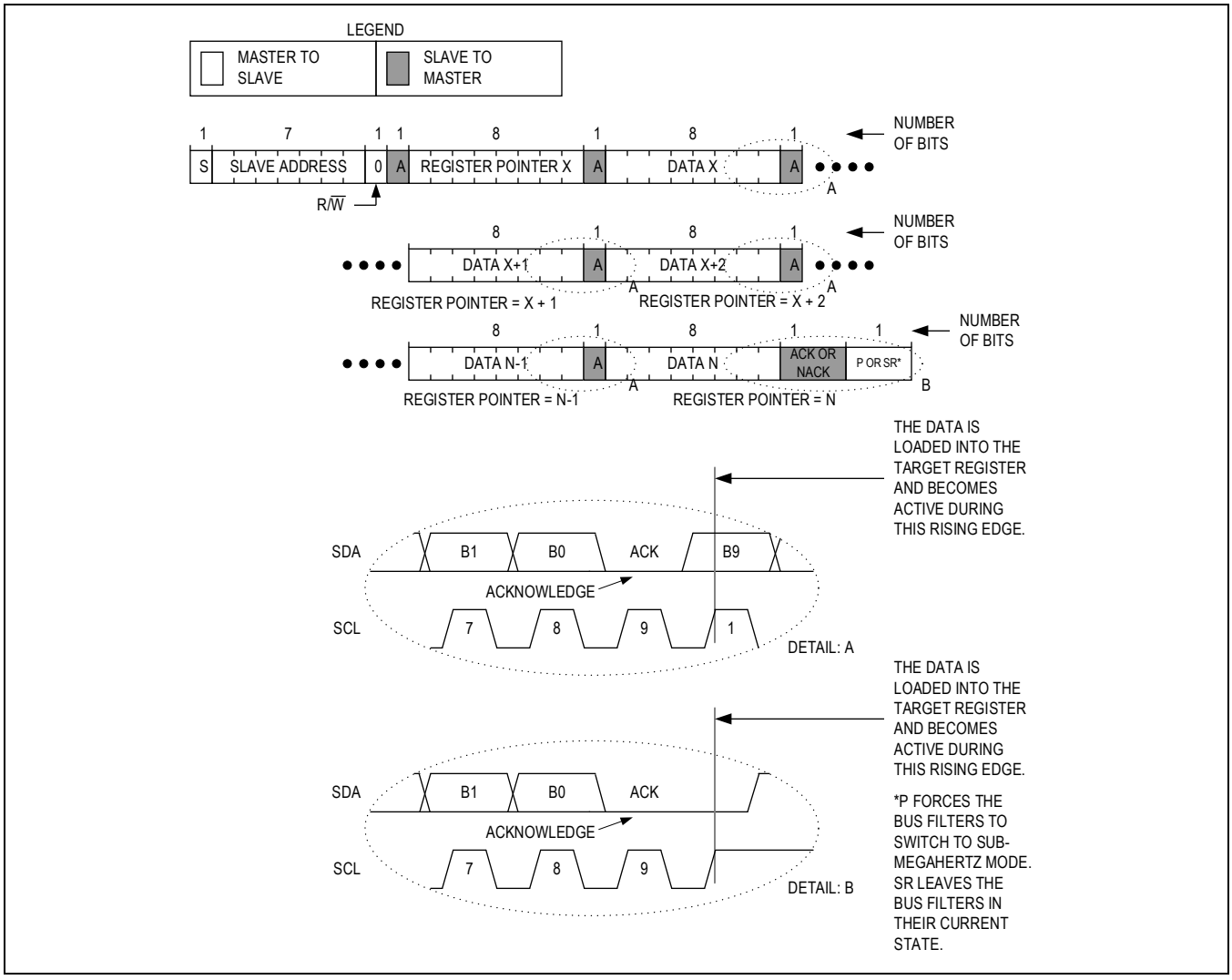


Figure 19. Writing to Sequential Registers X to N

Reading from a Single Register

Figure 20 shows the protocol for the I2C master device to read one byte of data. This protocol is the same as the SMBus specification's read byte protocol.

The read byte protocol is as follows:

- The master sends a start command (S). _
- The master sends the 7-bit slave address followed by a write bit (R/$\overline{W}$ = 0).

- The addressed slave asserts an acknowledge (A) by pulling SDA low.
- The master sends an 8-bit register pointer.
- The slave issues an acknowledge for the register pointer.
- The master sends a repeated start command (Sr). _
- The master sends the 7-bit slave address followed by a read bit (R/$\overline{W}$ = 1).
- The addressed slave asserts an acknowledge by pulling SDA low.
- The addressed slave places 8 bits of data on the bus from the location specified by the register pointer.
- The master issues a not acknowledge (nA).
- The master sends a stop condition (P) or a repeated start condition (Sr). Issuing a P ensures that the bus input filters are set for 1MHz or slower operation. Issuing an Sr leaves the bus input filters in their current state.

Note that when this device receives a stop, the register pointer is not modified. Therefore, if the master wants to reread the same register, it can start at Step 7 in the read byte protocol.

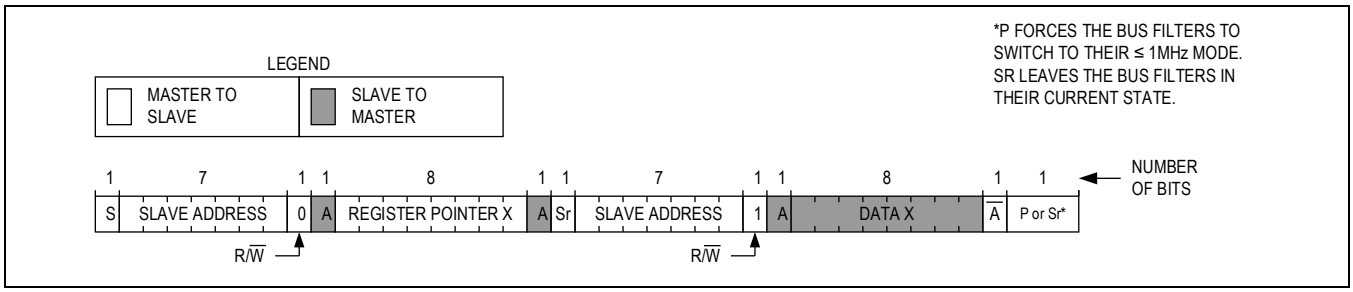


Figure 20. Reading from a Single Register with the Read Byte Protocol

Reading from Sequential Registers

Figure 21 shows the protocol for reading from sequential registers. This protocol is similar to the read byte protocol except that the master issues an acknowledge to signal the slave that it wants more data: when the master has all the data it requires it issues a not acknowledge (nA) and a stop (P) to end the transmission.

The protocol for continuous read from sequential registers is as follows:

- The master sends a start command (S). _
- The master sends the 7-bit slave address followed by a write bit (R/$\overline{W}$ = 0).
- The addressed slave asserts an acknowledge (A) by pulling SDA low.
- The master sends an 8-bit register pointer.
- The slave issues an acknowledge for the register pointer.
- The master sends a repeated start command (Sr). _
- The master sends the 7-bit slave address followed by a read bit (R/$\overline{W}$ = 1).
- The addressed slave asserts an acknowledge by pulling SDA low.
- The addressed slave places 8 bits of data on the bus from the location specified by the register pointer.
- The master issues an acknowledge (A) signaling the slave that it wishes to receive more data.
- Steps 9 and 10 are repeated as many times as the master requires. Following the last byte of data, the master must issue a not acknowledge (nA) to signal that it wishes to stop receiving data.
- The master sends a stop condition (P) or a repeated start condition (Sr). Issuing a stop (P) ensures that the bus input filters are set for 1MHz or slower operation. Issuing an Sr leaves the bus input filters in their current state.

Note that when this device receives a stop, the register pointer is not modified. Therefore, if the master wants to re-read the same register, it can start at Step 7 in the read byte protocol.

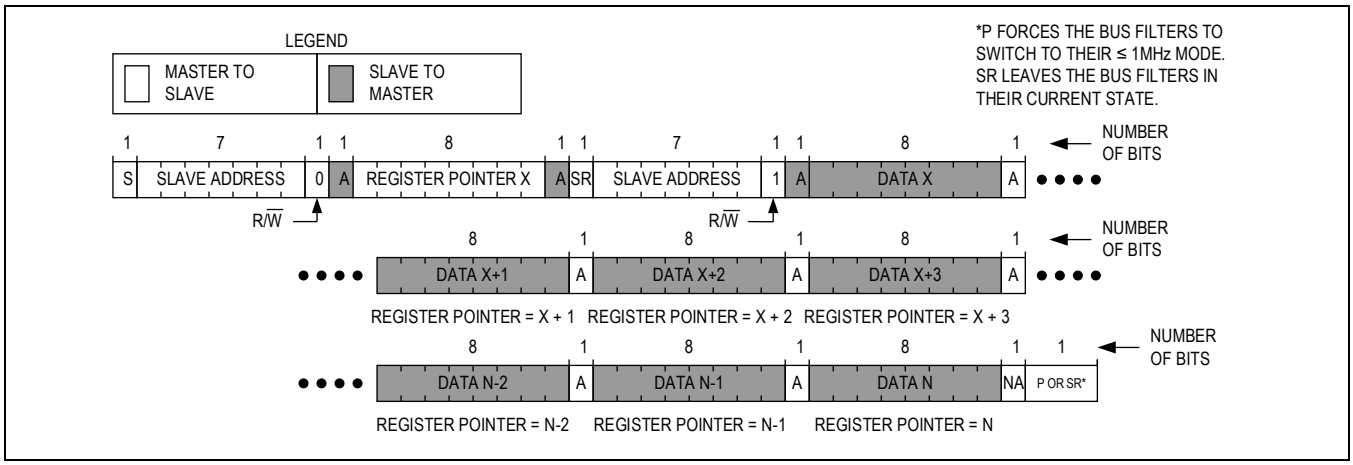


Figure 21. Reading Continuously from Sequential Registers X to N

Engaging HS Mode for Operation Up to 3.4MHz

Figure 22 shows the protocol for engaging HS mode operation. The HS mode operation allows for a bus operating speed up to 3.4MHz.

The engaging HS mode protocol is as follows:

- Begin the protocol while operating at a bus speed of 1MHz or lower.
- The master sends a start command (S).
- The master sends the 8-bit master code of 0b0000 1XXX where 0bXXX are don't care bits.
- The addressed slave issues a not acknowledge (nA).
- The master may increase its bus speed up to 3.4MHz and issue any read/write operation.

The master may continue to issue high-speed read/write operations until a stop (P) is issued. To continue operations in high-speed mode, use repeated start (Sr).

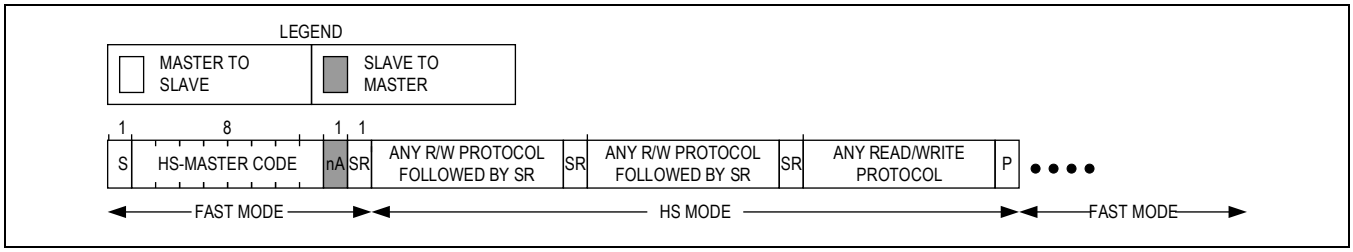


Figure 22. Engaging HS Mode

Register Map

MAX77675

ADDRESS	NAME	MSB							LSB
Configuration									
0x00	CNFG_GLBL_A[7:0]	MRT[1:0]		PU_DIS	BIAS_LPM	SIMO_INT_CH_DIS	nEN_MODE[1:0]		DBEN_nEN
0x01	CNFG_GLBL_B[7:0]	–	–	–	–	–	SFT_CTRL[2:0]		
0x02	INT_GLBL[7:0]	SBB3_F	SBB2_F	SBB1_F	SBB0_F	TJAL2_R	TJAL1_R	nEN_R	nEN_F
0x03	INTM_GLBL[7:0]	SBB3_FM	SBB2_FM	SBB1_FM	SBB0_FM	TJAL2_RM	TJAL1_RM	nEN_RM	nEN_FM
0x04	STAT_GLBL[7:0]	SBB3_S	SBB2_S	SBB1_S	SBB0_S	–	TJAL2_S	TJAL1_S	STAT_EN
0x05	ERCFLAG[7:0]	–	–	SFT_CRST_F	SFT_OFF_F	MRST	UVLO	OVLO	TOVLD
0x06	CID[7:0]	–	–	–	CID[4:0]				
0x07	CNFG_SBB_TOP_A[7:0]	–	–	STEP_SZ_SBB3	STEP_SZ_SBB2	STEP_SZ_SBB1	STEP_SZ_SBB0	DRV_SBB[1:0]	
0x08	CNFG_SBB0_A[7:0]	TV_SBB0[7:0]							
0x09	CNFG_SBB0_B[7:0]	–	–	–	–	ADE_SBB0	EN_SBB0[2:0]		
0x0A	CNFG_SBB1_A[7:0]	TV_SBB1[7:0]							
0x0B	CNFG_SBB1_B[7:0]	–	–	–	–	ADE_SBB1	EN_SBB1[2:0]		
0x0C	CNFG_SBB2_A[7:0]	TV_SBB2[7:0]							
0x0D	CNFG_SBB2_B[7:0]	–	–	–	–	ADE_SBB2	EN_SBB2[2:0]		
0x0E	CNFG_SBB3_A[7:0]	TV_SBB3[7:0]							
0x0F	CNFG_SBB3_B[7:0]	–	–	–	–	ADE_SBB3	EN_SBB3[2:0]		
0x10	CNFG_SBB_TOP_B[7:0]	–	–	DVS_SLEW	LAT_MODE	SR_SBB3	SR_SBB2	SR_SBB1	SR_SBB0

Register Details

CNFG_GLBL_A (0x0)

BIT	7	6	5	4	3	2	1	0
Field	MRT[1:0]		PU_DIS	BIAS_LPM	SIMO_INT_CH_DIS	nEN_MODE[1:0]		DBEN_nEN
Reset	0b00		0b0	0b0	0b0	0b00		0b0
Access Type	Write, Read		Write, Read	Write, Read	Write, Read	Write, Read		Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
MRT	7:6	Manual Reset Time Configuration. See the *nEN Manual Reset* section for more details.	0x0: 4s 0x1: 8s 0x2: 12s 0x3: 16s
PU_DIS	5	Enable or disable an internal pullup resistor at the nEN pin.	0x0: Enable internal nEN pullup (200kΩ) 0x1: Internal pullup disabled
BIAS_LPM	4	Main Bias Low-Power Mode Software Request	0x0: Main Bias forced to be in Normal-Power Mode by software. 0x1: Main Bias request to be in Low-Power Mode by software. If at least one channel is serviced more than twice in 15µs, the regulator automatically enters normal-power mode.
SIMO_INT_CH_DIS	3		0x0: Normal operation (SIMO internal channel supplies 1.8V in LPM mode) 0x1: Internal LDO always supplies 1.8V
nEN_MODE	2:1	nEN Mode	0x0: Push-Button Mode 0x1: Slide-Switch Mode 0x2: Logic Mode 0x3: Reserved
DBEN_nEN	0	Debounce Timer Enable for the nEN Pin	0x0: 100µs Debounce 0x1: 30ms Debounce

CNFG_GLBL_B (0x1)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	–	SFT_CTRL[2:0]		
Reset	–	–	–	–	–	0b000		
Access Type	–	–	–	–	–	Write, Read, Ext		

BITFIELD	BITS	DESCRIPTION	DECODE
SFT_CTRL	2:0	Software Control Functions. See the *On/Off Controller* section for more information about what each command does.	0x0: No Action 0x1: Software Cold Reset (SFT_CRST). The device powers down, resets, and then powers up again. 0x2: Software Off (SFT_OFF). The device powers down, resets, and then remains off until a wake-up event. 0x3: Software Standby (SFT_STBY). The device powers

BITFIELD	BITS	DESCRIPTION	DECODE
			down and goes to standby mode. 0x4: Software Exit Standby (SFT_EXIT_STBY). The device exits standby mode and powers up again. 0x5 - 0x7: Reserved

INT_GLBL (0x2)

BIT	7	6	5	4	3	2	1	0
Field	SBB3_F	SBB2_F	SBB1_F	SBB0_F	TJAL2_R	TJAL1_R	nEN_R	nEN_F
Reset	0b0	0b0	0b0	0b0	0b0	0b0	0b0	0b0
Access Type	Read Clears All	Read Clears All	Read Clears All	Read Clears All	Read Clears All	Read Clears All	Read Clears All	Read Clears All

BITFIELD	BITS	DESCRIPTION	DECODE
SBB3_F	7	SBB3 Channel Fault Interrupt	0x0: SBB3 was not overloaded since the last time this bit was read. 0x1: SBB3 was overloaded since the last time this bit was read.
SBB2_F	6	SBB2 Channel Fault Interrupt	0x0: SBB2 was not overloaded since the last time this bit was read. 0x1: SBB2 was overloaded since the last time this bit was read.
SBB1_F	5	SBB1 Channel Fault Interrupt	0x0: SBB1 was not overloaded since the last time this bit was read. 0x1: SBB1 was overloaded since the last time this bit was read.
SBB0_F	4	SBB0 Channel Fault Interrupt	0x0: SBB0 was not overloaded since the last time this bit was read. 0x1: SBB0 was overloaded since the last time this bit was read.
TJAL2_R	3	Thermal Alarm 2 Rising Interrupt	0x0: The junction temperature has not risen above TJAL2 since the last time this bit was read. 0x1: The junction temperature has risen above TAJL2 since the last time this bit was read.
TJAL1_R	2	Thermal Alarm 1 Rising Interrupt	0x0: The junction temperature has not risen above TJAL1 since the last time this bit was read. 0x1: The junction temperature has risen above TAJL1 since the last time this bit was read.
nEN_R	1	nEN Rising Interrupt	0x0: No nEN rising edges have occurred since the last time this bit was read. 0x1: An nEN rising edge has occurred since the last time this bit was read.
nEN_F	0	nEN Falling Interrupt	0x0: No nEN falling edges have occurred since the last time this bit was read. 0x1: An nEN falling edge has occurred since the last time this bit was read.

INTM_GLBL (0x3)

BIT	7	6	5	4	3	2	1	0
Field	SBB3_FM	SBB2_FM	SBB1_FM	SBB0_FM	TJAL2_RM	TJAL1_RM	nEN_RM	nEN_FM

Reset	0b1	0b1	0b1	0b1	0b1	0b1	0b1	0b1
Access Type	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION
SBB3_FM	7	SBB3 Channel Fault Interrupt Mask
SBB2_FM	6	SBB2 Channel Fault Interrupt Mask
SBB1_FM	5	SBB1 Channel Fault Interrupt Mask
SBB0_FM	4	SBB0 Channel Fault Interrupt Mask
TJAL2_RM	3	Thermal Alarm 2 Rising Interrupt Mask
TJAL1_RM	2	Thermal Alarm 1 Rising Interrupt Mask
nEN_RM	1	nEN Rising Interrupt Mask
nEN_FM	0	nEN Falling Interrupt Mask

STAT_GLBL (0x4)

BIT	7	6	5	4	3	2	1	0
Field	SBB3_S	SBB2_S	SBB1_S	SBB0_S	–	TJAL2_S	TJAL1_S	STAT_EN
Reset	0b0	0b0	0b0	0b0	–	0b0	0b0	0b0
Access Type	Read Only	Read Only	Read Only	Read Only	–	Read Only	Read Only	Read Only

BITFIELD	BITS	DESCRIPTION	DECODE
SBB3_S	7	SBB3 Channel Regulation Status	0x0: SBB3 is overloaded or disabled 0x1: SBB3 is not overloaded
SBB2_S	6	SBB2 Channel Regulation Status	0x0: SBB2 is overloaded or disabled 0x1: SBB2 is not overloaded
SBB1_S	5	SBB1 Channel Regulation Status	0x0: SBB1 is overloaded or disabled 0x1: SBB1 is not overloaded
SBB0_S	4	SBB0 Channel Regulation Status	0x0: SBB0 is overloaded or disabled 0x1: SBB0 is not overloaded
TJAL2_S	2	Thermal Alarm 2 Status	0x0: The junction temperature is less than TJAL2 0x1: The junction temperature is greater than TJAL2
TJAL1_S	1	Thermal Alarm 1 Status	0x0: The junction temperature is less than TJAL1 0x1: The junction temperature is greater than TJAL1
STAT_EN	0	Debounced Status for the nEN input.	0x0: nEN is not asserted (logic HIGH) 0x1: nEN is asserted (logic LOW)

ERCFLAG (0x5)

BIT	7	6	5	4	3	2	1	0
Field	–	–	SFT_CRST_F	SFT_OFF_F	MRST	UVLO	OVLO	TOVLD
Reset	–	–	0b0	0b0	0b0	0b0	0b0	0b0
Access Type	–	–	Read Clears All	Read Clears All	Read Clears All	Read Clears All	Read Clears All	Read Clears All

BITFIELD	BITS	DESCRIPTION	DECODE
SFT_CRST_F	5	Software Cold Reset Flag	0x0: The software cold reset has not occurred since the last read of this register. 0x1: The software cold reset has occurred since the last read of this register. This indicates that software has set SFT_CTRL[1:0] = 0b01.
SFT_OFF_F	4	Software Off Flag	0x0: The SFT_OFF function has not occurred since the last read of this register. 0x1: The SFT_OFF function has occurred since the last read of this register. This indicates that software has set SFT_CTRL[1:0] = 0b10.
MRST	3	Manual Reset Timer	0x0: A manual reset has not occurred since this last read of this register. 0x1: A manual reset has occurred since this last read of this register.
UVLO	2	Undervoltage Lockout	0x0: The undervoltage lockout has not occurred since this last read of this register. 0x1: The undervoltage lockout has occurred since the last read of this register. This indicates that the V_{IN} voltage fell below UVLO (~2.4V)
OVLO	1	Overvoltage Lockout	0x0: The overvoltage lockout has not occurred since this last read of this register. 0x1: The overvoltage lockout has occurred since the last read of this register. This indicates that the V_{IN} voltage rose above OVLO (~5.85V)
TOVLD	0	Thermal Overload	0x0: The thermal overload has not occurred since the last read of this register. 0x1: The thermal overload has occurred since the last read of this register. This indicates that the junction temperature exceeded +145ºC.

CID (0x6)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	CID[4:0]				
Reset	–	–	–	0b00000				
Access Type	–	–	–	Read Only				

BITFIELD	BITS	DESCRIPTION
CID	4:0	Chip Identification Code. These bits track the OTP configuration.

CNFG_SBB_TOP_A (0x7)

BIT	7	6	5	4	3	2	1	0
Field	–	–	STEP_SZ_SBB3	STEP_SZ_SBB2	STEP_SZ_SBB1	STEP_SZ_SBB0	DRV_SBB[1:0]	
Reset	–	–	0b0	0b0	0b0	0b0	0b00	
Access Type	–	–	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	

BITFIELD	BITS	DESCRIPTION	DECODE
STEP_SZ_SBB3	5	Selects the output voltage step size for SBB3. Changing step size also affects the maximum programmable output voltage. New step size setting takes effect only after TV_SBBx update. If set to 0b0, the programmable range becomes 0.500V - 5.500V. If set to 0b1, the programmable range becomes 0.5000V - 3.6875V.	SBB3 Output Voltage Step Size 0b0 = 25.0mV, 0b1 = 12.5mV
STEP_SZ_SBB2	4	Selects the output voltage step size for SBB2. Changing step size also affects the maximum programmable output voltage. New step size setting takes effect only after TV_SBBx update. If set to 0b0, the programmable range becomes 0.500V - 5.500V. If set to 0b1, the programmable range becomes 0.5000V - 3.6875V.	SBB2 Output Voltage Step Size 0b0 = 25.0mV, 0b1 = 12.5mV
STEP_SZ_SBB1	3	Selects the output voltage step size for SBB1. Changing step size also affects the maximum programmable output voltage. New step size setting takes effect only after TV_SBBx update. If set to 0b0, the programmable range becomes 0.500V - 5.500V. If set to 0b1, the programmable range becomes 0.5000V - 3.6875V.	SBB1 Output Voltage Step Size 0b0 = 25.0mV, 0b1 = 12.5mV
STEP_SZ_SBB0	2	Selects the output voltage step size for SBB0. Changing step size also affects the maximum programmable output voltage. New step size setting takes effect only after TV_SBBx update. If set to 0b0, the programmable range becomes 0.500V - 5.500V.	SBB0 Output Voltage Step Size 0b0 = 25.0mV, 0b1 = 12.5mV

BITFIELD	BITS	DESCRIPTION	DECODE
		If set to 0b1, the programmable range becomes 0.5000V - 3.6875V.	
DRV_SBB	1:0	SIMO Buck-Boost (All Channels) Drive Strength Trim. See the *Drive Strength* section for more details.	0x0: Fastest transition time (~0.6ns) 0x1: A little slower than 0b00 (~1.2ns) 0x2: A little slower than 0b01 (~1.8ns) 0x3: A little slower than 0b10 (~8ns)

CNFG_SBB0_A (0x8)

BIT	7	6	5	4	3	2	1	0
Field	TV_SBB0[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
TV_SBB0	7:0	SIMO Buck-Boost Channel 0 Target Output Voltage. When STEP_SZ_SBB0 = 0b0, the programmable range is 0.5V to 5.5V in 25.0mV increments. V_{SBB0} = 0.5V + 0.0250V x TV_SBB0[7:0] When STEP_SZ_SBB0 = 0b1, the programmable range is 0.5000V to 3.6875V in 12.5mV increments. V_{SBB0} = 0.5V + 0.0125V x TV_SBB0[7:0]	SBB0 Target Output Voltage When CNFG_SBB0_C.STEP_SZ_SBB0 = 0b0, 0x0 = 0.500V, 0x1 = 0.525V, 0x2 = 0.550V, 0x3 - 0xC6 = 0.5 + (TV_SBB0 x 0.025)V, 0xC7 = 5.475V, 0xC8 = 5.500V, 0xC9 - 0xFF = Reserved When CNFG_SBB0_C.STEP_SZ_SBB0 = 0b1, 0x0 = 0.5000V, 0x1 = 0.5125V, 0x2 = 0.5250V, 0x3 - 0xFD = 0.5 + (TV_SBB0 x 0.0125)V, 0xFE = 3.6750V, 0xFF = 3.6875V

CNFG_SBB0_B (0x9)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	ADE_SBB0	EN_SBB0[2:0]		
Reset	–	–	–	–	0b0	0b000		
Access Type	–	–	–	–	Write, Read	Write, Read		

BITFIELD	BITS	DESCRIPTION	DECODE
ADE_SBB0	3	SIMO Buck-Boost Channel 0 Active-Discharge Enable	0x0: The active discharge function is disabled. When SBB0 is disabled, its discharge rate is a function of the output capacitance and the external load. 0x1: The active discharge function is enabled. When SBB0 is disabled, an internal resistor (R_{AD_SBB0}) is activated from SBB0 to PGND to help the output voltage discharge. The output voltage discharge rate is a function of the output capacitance, the external loading, and the internal R_{AD_SBB0} load.
EN_SBB0	2:0	Enable Control for SIMO Buck-Boost Channel 0. Select an FPS slot that the channel powers up and powers down in or whether the channel is forced on or off. After the SIMO is enabled, the bias circuits may be programmed back to low-power mode (CNFG_GLBL_A.BIAS_LPM = 1) to decrease quiescent current.	0x0: FPS slot 0 0x1: FPS slot 1 0x2: FPS slot 2 0x3: FPS slot 3 0x4: Off 0x5: Same as 0x4 0x6: On 0x7: Same as 0x6

CNFG_SBB1_A (0xA)

BIT	7	6	5	4	3	2	1	0
Field	TV_SBB1[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
TV_SBB1	7:0	SIMO Buck-Boost Channel 1 Target Output Voltage. When STEP_SZ_SBB1 = 0b0, the programmable range is 0.5V to 5.5V in 25.0mV increments. V_{SBB1} = 0.5V + 0.0250V x TV_SBB1[7:0] When STEP_SZ_SBB1 = 0b1, the programmable range is 0.5000V to 3.6875V in 12.5mV increments. V_{SBB1} = 0.5V + 0.0125V x TV_SBB1[7:0]	SBB1 Target Output Voltage When CNFG_SBB1_C.STEP_SZ_SBB1 = 0b0, 0x0 = 0.500V, 0x1 = 0.525V, 0x2 = 0.550V, 0x3 - 0xC6 = 0.5 + (TV_SBB1 x 0.025)V, 0xC7 = 5.475V, 0xC8 = 5.500V, 0xC9 - 0xFF = Reserved When CNFG_SBB1_C.STEP_SZ_SBB1 = 0b1, 0x0 = 0.5000V, 0x1 = 0.5125V, 0x2 = 0.5250V, 0x3 - 0xFD = 0.5 + (TV_SBB1 x 0.0125)V, 0xFE = 3.6750V, 0xFF = 3.6875V

CNFG_SBB1_B (0xB)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	ADE_SBB1	EN_SBB1[2:0]		
Reset	–	–	–	–	0b0	0b000		
Access Type	–	–	–	–	Write, Read	Write, Read		

BITFIELD	BITS	DESCRIPTION	DECODE
ADE_SBB1	3	SIMO Buck-Boost Channel 1 Active-Discharge Enable	0x0: The active discharge function is disabled. When SBB1 is disabled, its discharge rate is a function of the output capacitance and the external load. 0x1: The active discharge function is enabled. When SBB1 is disabled, an internal resistor (R_{AD_SBB1}) is activated from SBB1 to PGND to help the output voltage discharge. The output voltage discharge rate is a function of the output capacitance, the external loading, and the internal R_{AD_SBB1} load.
EN_SBB1	2:0	Enable Control for SIMO Buck-Boost Channel 1. Select an FPS slot that the channel powers up and powers down in or whether the channel is forced on or off. After the SIMO is enabled, the bias circuits may be programmed back to low-power mode (CNFG_GLBL_A.BIAS_LPM = 1) to decrease quiescent current.	0x0: FPS slot 0 0x1: FPS slot 1 0x2: FPS slot 2 0x3: FPS slot 3 0x4: Off 0x5: Same as 0x4 0x6: On 0x7: Same as 0x6

CNFG_SBB2_A (0xC)

BIT	7	6	5	4	3	2	1	0
Field	TV_SBB2[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
TV_SBB2	7:0	SIMO Buck-Boost Channel 2 Target Output Voltage. When STEP_SZ_SBB2 = 0b0, the programmable range is 0.5V to 5.5V in 25.0mV increments. V_{SBB2} = 0.5V + 0.0250V x TV_SBB2[7:0] When STEP_SZ_SBB2 = 0b1, the programmable range is 0.5000V to 3.6875V in 12.5mV increments. V_{SBB2} = 0.5V + 0.0125V x TV_SBB2[7:0]	SBB2 Target Output Voltage When CNFG_SBB2_C.STEP_SZ_SBB2 = 0b0, 0x0 = 0.500V, 0x1 = 0.525V, 0x2 = 0.550V, 0x3 - 0xC6 = 0.5 + (TV_SBB2 x 0.025)V, 0xC7 = 5.475V, 0xC8 = 5.500V, 0xC9 - 0xFF = Reserved

BITFIELD	BITS	DESCRIPTION	DECODE
			When CNFG_SBB2_C.STEP_SZ_SBB2 = 0b1, 0x0 = 0.5000V, 0x1 = 0.5125V, 0x2 = 0.5250V, 0x3 - 0xFD = 0.5 + (TV_SBB2 x 0.0125)V, 0xFE = 3.6750V, 0xFF = 3.6875V

CNFG_SBB2_B (0xD)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	ADE_SBB2	EN_SBB2[2:0]		
Reset	–	–	–	–	0b0	0b000		
Access Type	–	–	–	–	Write, Read	Write, Read		

BITFIELD	BITS	DESCRIPTION	DECODE
ADE_SBB2	3	SIMO Buck-Boost Channel 2 Active-Discharge Enable	0x0: The active discharge function is disabled. When SBB2 is disabled, its discharge rate is a function of the output capacitance and the external load. 0x1: The active discharge function is enabled. When SBB2 is disabled, an internal resistor (R_{AD_SBB2}) is activated from SBB2 to PGND to help the output voltage discharge. The output voltage discharge rate is a function of the output capacitance, the external loading, and the internal R_{AD_SBB2} load.
EN_SBB2	2:0	Enable Control for SIMO Buck-Boost Channel 2. Select an FPS slot that the channel powers up and powers down in or whether the channel is forced on or off. After the SIMO is enabled, the bias circuits may be programmed back to low-power mode (CNFG_GLBL_A.BIAS_LPM = 1) to decrease quiescent current.	0x0: FPS slot 0 0x1: FPS slot 1 0x2: FPS slot 2 0x3: FPS slot 3 0x4: Off 0x5: Same as 0x4 0x6: On 0x7: Same as 0x6

CNFG_SBB3_A (0xE)

BIT	7	6	5	4	3	2	1	0
Field	TV_SBB3[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
TV_SBB3	7:0	SIMO Buck-Boost Channel 3 Target Output Voltage. When STEP_SZ_SBB3 = 0b0, the programmable range is 0.5V to 5.5V in 25.0mV increments. V_{SBB3} = 0.5V + 0.0250V x TV_SBB3[7:0] When STEP_SZ_SBB3 = 0b1, the programmable range is 0.5000V to 3.6875V in 12.5mV increments. V_{SBB3} = 0.5V + 0.0125V x TV_SBB3[7:0]	SBB3 Target Output Voltage When CNFG_SBB3_C.STEP_SZ_SBB3 = 0b0, 0x0 = 0.500V, 0x1 = 0.525V, 0x2 = 0.550V, 0x3 - 0xC6 = 0.5 + (TV_SBB3 x 0.025)V, 0xC7 = 5.475V, 0xC8 = 5.500V, 0xC9 - 0xFF = Reserved When CNFG_SBB3_C.STEP_SZ_SBB3 = 0b1, 0x0 = 0.5000V, 0x1 = 0.5125V, 0x2 = 0.5250V, 0x3 - 0xFD = 0.5 + (TV_SBB3 x 0.0125)V, 0xFE = 3.6750V, 0xFF = 3.6875V

CNFG_SBB3_B (0xF)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	ADE_SBB3	EN_SBB3[2:0]		
Reset	–	–	–	–	0b0	0b000		
Access Type	–	–	–	–	Write, Read	Write, Read		

BITFIELD	BITS	DESCRIPTION	DECODE
ADE_SBB3	3	SIMO Buck-Boost Channel 3 Active-Discharge Enable	0x0: The active discharge function is disabled. When SBB3 is disabled, its discharge rate is a function of the output capacitance and the external load. 0x1: The active discharge function is enabled. When SBB3 is disabled, an internal resistor (R_{AD_SBB3}) is activated from SBB3 to PGND to help the output voltage discharge. The output voltage discharge rate is a function of the output capacitance, the external loading, and the internal R_{AD_SBB3} load.
EN_SBB3	2:0	Enable Control for SIMO Buck-Boost Channel 3. Select an FPS slot that the channel powers up and powers down in or whether the channel is forced on or off. After the SIMO is enabled, the bias circuits may be programmed back to low-power mode (CNFG_GLBL_A.BIAS_LPM = 1) to decrease quiescent current.	0x0: FPS slot 0 0x1: FPS slot 1 0x2: FPS slot 2 0x3: FPS slot 3 0x4: Off 0x5: Same as 0x4 0x6: On 0x7: Same as 0x6

CNFG_SBB_TOP_B (0x10)

BIT	7	6	5	4	3	2	1	0
Field	–	–	DVS_SLEW	LAT_MODE	SR_SBB3	SR_SBB2	SR_SBB1	SR_SBB0
Reset	–	–	0b0	0b0	0b0	0b0	0b0	0b0
Access Type	–	–	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
DVS_SLEW	5	Select DVS slew rate	0x0: 5mV/µs 0x1: 10mV/µs
LAT_MODE	4	If set, reduces the latency between changing output voltage (CNFG_SBBx_A.TV_SBBx[7:0]) and the start of SBBx voltage ramp. Low-power mode not supported while this bit is set to 1. This bit is ignored if SR_SBBx = 0.	0x0: Low quiescent current, high latency (~100µs) 0x1: High quiescent current, low latency (~10µs)
SR_SBB3	3	Controls the rising slew rate when SBB3 ramps from one voltage setting to a higher setting.	0x0: 2mV/µs 0x1: See DVS_SLEW
SR_SBB2	2	Controls the rising slew rate when SBB2 ramps from one voltage setting to a higher setting.	0x0: 2mV/µs 0x1: See DVS_SLEW
SR_SBB1	1	Controls the rising slew rate when SBB1 ramps from one voltage setting to a higher setting.	0x0: 2mV/µs 0x1: See DVS_SLEW
SR_SBB0	0	Controls the rising slew rate when SBB0 ramps from one voltage setting to a higher setting.	0x0: 2mV/µs 0x1: See DVS_SLEW

Applications Information

Configuring Power Modes

The MAX77675's power mode is configurable through CNFG_GLBL_A.BIAS_LPM and CNFG_GLBL_A.SIMO_INT_CH_DIS to meet requirements depending on whether quiescent current or performance is more important.

After configuring these bits, avoid changing them in real time while the system is operating and drawing load current.

If the system enters a state with low current draw (e.g., <5mA per channel) and low quiescent current is needed, configure the MAX77675 to be in low-power mode as described in *Table 7*. If there is >5mA per channel, use normal-power mode and set SIMO_INT_CH_DIS = 1 if low-quiescent current is still required.

Table 7. Power Mode Configuration

BIAS_LPM	SIMO_INT_CH_DIS	DESCRIPTION	BENEFITS	TRADE-OFFS
0	Don't Care	Normal-Power Mode	• Lower ripple • Faster transient response	• Highest quiescent current state
1	0	Low-Power Mode	• Lowest quiescent current state	• Higher ripple • Slower transient response
1	1	Everything except for the bias is in low-power mode	• Lower ripple compared to low-power mode	• Slower transient response • Quiescent current increased by about 10pA (typical) compared to low-power mode • Higher ripple compared to normalpower mode

Applications Information—SIMO Buck-Boost

SIMO-Supported Output Current

The maximum supported output current is limited by inductor valley current (see the *Inductor Valley Current* section). When the valley current is at its maximum value, channels enter overload condition, triggering their respective fault interrupt flags. While the absolute maximum valley current is 1.2A (eight valley steps), stay below 900mA (six valley steps) to avoid valley current occasionally reaching the absolute maximum.

In addition, if the average inductor current is above 700mA, ripple on the output channels can increase out of specifications.

To predict if a given set of conditions is supported, estimate the average inductor current and maximum valley current the regulator experiences. A calculator tool is provided (see the *Support Materials* section) for convenience. *Table 8* shows some example results using the calculator.

Table 8. SIMO-Supported Output Current for Common Applications

PARAMETERS	EXAMPLE 1	EXAMPLE 2	EXAMPLE 3	EXAMPLE 4	EXAMPLE 5
V_{IN}	2.7V	4.0V	3.7V	3.7V	5.0V
SBB0	1.8V at 100mA	1.8V at 30mA	1.8V at 100mA	1.8V at 300mA	1.8 V at 150mA
SBB1	3.3V at 200mA	3.3V at 200mA	1.1V at 120mA	1.2V at 100mA	1.2V at 70mA
SBB2	0.5V at 250mA	5.0V at 100mA	0.7V at 200mA	3.2V at 20mA	0.85 V at 100mA
SBB3	5.0V at 50mA	5.0V at 100mA	3.3V at 80mA	2.85 V at 100mA	2.0V at 80mA
Maximum I_L, average	864mA	696mA	550mA	597mA	400mA
Maximum I_L, valley	750mA	600mA	450mA	450mA	300mA
Overloaded	No	No	No	No	No
Higher ripple	Yes	No	No	No	No

To manually estimate average inductor current, first estimate the average inductor current for each channel using the following equations:

$$I_{L_avg} = \begin{cases} I_{out} & , \ \frac{V_{SBBx}}{V_{IN}} < 0.6 \ \text{(Buck Mode)} \\ \frac{3}{2} x I_{out} & , \ 0.6 \leq \frac{V_{SBBx}}{V_{IN}} \leq 1.25 \ \text{(Buck-Boost Mode)} \\ I_{out} x \frac{V_{SBBx}}{V_{IN} x \eta} & , \ \frac{V_{SBBx}}{V_{IN}} > 1.25 \ \text{(Boost Mode)} \end{cases} \quad \text{(Equation 3)}$$

where η is efficiency (see the *Typical Operating Characteristics* section for efficiency values). The sum of the average currents is the expected maximum, average inductor current. Then, using the total average inductor current, estimate the number of valley current steps with the following equation:

$$I_{L_valley_steps} = \frac{I_{L_{avg}}}{I_{valley_{step}}} \quad \text{(Equation 4)}$$

where I_{valley_step} is 150mA. If the number of steps is above the previously mentioned maximum value (8), the regulator is overloaded. If the average inductor current is above 700mA, expect higher output voltage ripple.

Overload

While in overload condition, the output voltage can drop for any channel. A host controller can detect which channels are "overloaded" by reading either the status bits (STAT_GLBL.SBBx_S) or the interrupt bits (INT_GLBL.SBBx_F), where x is the channel number. Status bits convey the current state of the channel while interrupt bits indicate if a channel had entered overload in the past. If the status bit indicates that a channel is overloaded, its output voltage is most likely out of regulation.

Inductor Selection

Choose an inductance from 1.0µH to 2.2µH; 1.5µH inductors work best for most designs. Larger inductances transfer more energy to the output for each cycle and typically result in larger output voltage ripple and better efficiency. See the *Output Capacitor Selection* section for more information on how to size the output capacitor to control ripple.

Choose an inductor whose saturation current is above the worst case peak inductor current. For example, if the worst case occurs while drawing 700mA, the worst case peak inductor current is around 1.2A. For systems where the expected load currents are notwell known, use an inductorwith saturation currents 2A.

Consider the DC resistance (DCR), AC resistance (ACR), and package size of the inductor. Typically, smaller-sized inductors have larger DC and AC resistance, reducing efficiency. Note that many inductor manufacturers have inductor families containing different versions of core material to balance trade-offs between DCR, ACR (i.e., core losses), and component cost.

Input Capacitor Selection

Choose the input bypass capacitance (C_{IN}) to be at least 10µF. A value of 22µF nominal is recommended to account for voltage derating. Larger values of C_{IN} improve the decoupling for the SIMO regulator.

The C_{IN} reduces the current peaks drawn from the battery or input power source during SiMO regulator operation and reduces switching noise in the system. Ceramic capacitors with X5R or X7R dielectric are highly recommended due to their small size, low ESR, and small temperature coefficients.

To fully utilize the available input voltage range of the device (5.5V max), use a capacitor with a voltage rating of 6.3V at minimum.

Bootstrap Capacitor Selection

Choose the bootstrap capacitance (C_{BST}) to be 10nF. Smaller values of C_{BST} result in insufficient gate drive for the output high-side power FETs. Larger values of C_{BST} (>100nF) have the potential to degrade the startup performance.

Ceramic capacitors with 0201 or 0402 case size are recommended.

Output Capacitor Selection

Choose each output bypass capacitance (CsBBx) based on the target output voltage ripple (AVsBBx): typical value is 22µF. In addition, consider using at least 44µF for an individual channel if either the channel's output voltage is less than 1.5V or the channel is lightly loaded while another channel is heavily loaded.

Larger values of C_{SBBx} improve the output voltage ripple but increase the input surge currents during soft-start and output voltage changes. The output voltage ripple is a function of the inductance (L), the output voltage ($VSBB_X$), and the inductor current ripple (AII). which is typically 300mA to 500mA. See Equation 5 to estimate the minimum effective capacitance for a given ripple. However, always have the minimum capacitance at 10µF.

$$C_{SBBx} = \frac{\Delta I_L{}^2 x L}{2 x V_{SBBx} x \Delta V_{SBBx}} \quad \text{(Equation 5)}$$

Ceramic capacitors with X5R or X7R dielectric are highly recommended due to their small size, low ESR, and small temperature coefficients.

A capacitor's effective capacitance decreases with DC bias voltage. This effect is more pronounced with physically smaller capacitors. Due to this, it is possible for 0603 capacitors to perform well while 0402 capacitors of the same nominal capacitance perform poorly. Consider the effective output capacitance value after initial tolerance, bias voltage, aging, and temperature derating.

PVDD and VDD Capacitors

Always have a minimum of 10µF capacitance near the PVDD pin. If possible, place an additional 1µF to 10µF near the V_{DD} pin. If there is not enough room on the PCB, V_{DD} can share PVDD's capacitor. The tradeoff is an occasional 5mV (approximate) droop on the output channels while in low-power mode.

If V_{DD} and PVDD are not connected, place at minimum a 1µF capacitor near the V_{DD} pin.

Unused Outputs

Do not leave unused outputs unconnected. If an output left unconnected is accidentally enabled, the charged inductor experiences an open circuit, and the output voltage soars above the absolute maximum rating, damaging the device. If an output is not used, do one of the following:

1. Disable the output (CNFG_SBBx_B.EN_SBBx[2:0] = 0x4 or 0x5) and connect the output to ground. If an unused output is enabled by default or can be accidentally enabled, do one of the other recommendations instead.
2. Bypass the unused output with a 1µF capacitor to ground.
3. Connect the unused output to IN or a different output channel if the unused output is programmed to a lower voltage. Since the output voltage is higher than the unused output, the regulator does not service the unused output even if it is unintentionally enabled.

• Note that some OTP options have the active-discharge resistors enabled by default. Connecting an unused output to IN is **not recommended** if the active discharge is enabled by default. If connecting the unused output to a different channel, disable the active discharge resistor (CNFG_SBBx_B.ADE_SBBx = 0) of the unused channel.

Output Voltage Ripple

Ripple is highest when there is heavy load on at least one channel while other channels have less load.

While the regulator is operating in CCM (inductor valley current is greater than 0A), the output voltage ripple for one channel is affected by other channels. For example, channels may droop lower in voltage while waiting for another channel to be serviced. In addition, while one or more channels are loaded with more than 300mA, other channels may occasionally have larger spikes in voltage ripple. Ripple also increases with output voltage.

Assuming at least 300mA total load current and 22µF of output capacitance, for channels whose output voltage is 2.5V or less, the occasional spike in voltage ripple can be up to 200mV while the average ripple is < 100mV. For channels whose output voltage is greater than 2.5V, the occasional spike in voltage ripple can be up to 300mV while the average ripple is < 120mV.

See the *Output Capacitor Selection* section for recommendations on how much output capacitance to use.

PCB Layout Guide

Capacitors

Place decoupling capacitors as close as possible to the IC such that connections from capacitor pads to pin and from capacitor pads to ground pins are short. Keeping the connections short lowers parasitic inductance and resistance, improving performance and shrinking the physical size of hot loops.

If connections to the capacitors are through vias, use multiple vias to minimize parasitics. Also, connect loads to the capacitor pads rather than the device pins.

Input Capacitor at IN

Minimize the parasitic inductance from PGND to input capacitor to IN to reduce ringing on the LXA voltage.

Output Capacitors at SBBx

The output capacitors experience large changes in current as the regulator charges and discharges the inductor. Minimize parasitic inductance from SBBx to output capacitor to PGND

Inductor

Keep the inductor close to the IC to reduce trace resistance. However, prioritize any regulator input/output capacitors over the inductor. Use the appropriate trace width from LXA to inductor to LXB to support the worst case, peak inductor current (see the *Inductor Selection* section). Likewise, if there are vias in the path, use an appropriate number of vias to support the current.

Ground Connections

As the switching regulator charges and discharges the inductor, current flows from PGND to the input capacitor ground, from output capacitor ground to PGND, or from output capacitor ground to input capacitor ground. Therefore, use a wide, continuous copper plane to connect PGND to the capacitor grounds.

When connecting the GND and PGND pins together, ensure noise from the power ground does not enter the analog ground (where GND is connected). For example, assuming the ground pins are connected through a solid ground plane on an internal layer, one via connecting GND to the internal ground plane may be sufficient to protect GND from most of the noise in the power-ground plane. Likewise, if there are other higher current or noisy circuitry near this device, avoid connecting the GND pin directly to their grounds.

For more guidelines on grounding, refer to the Technical Articles section at *https://www.analog.com/en/design-centef/packaging-quality-symbols-footprints/package-resources.html*.

Example PCB Layout

Figure 23 shows an example layout.

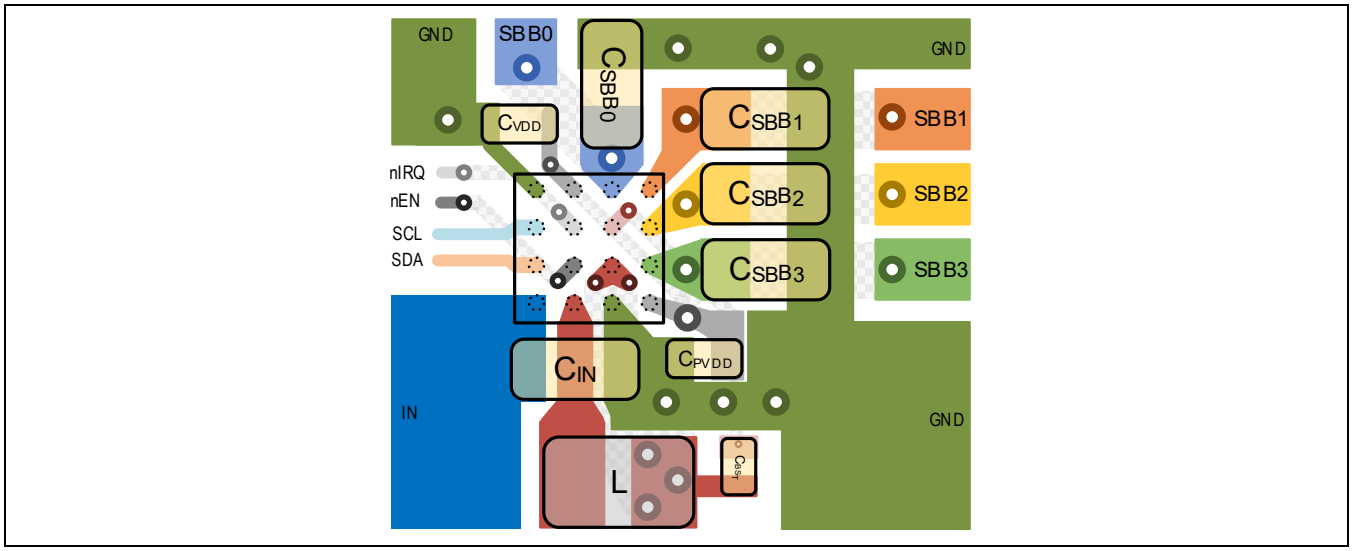
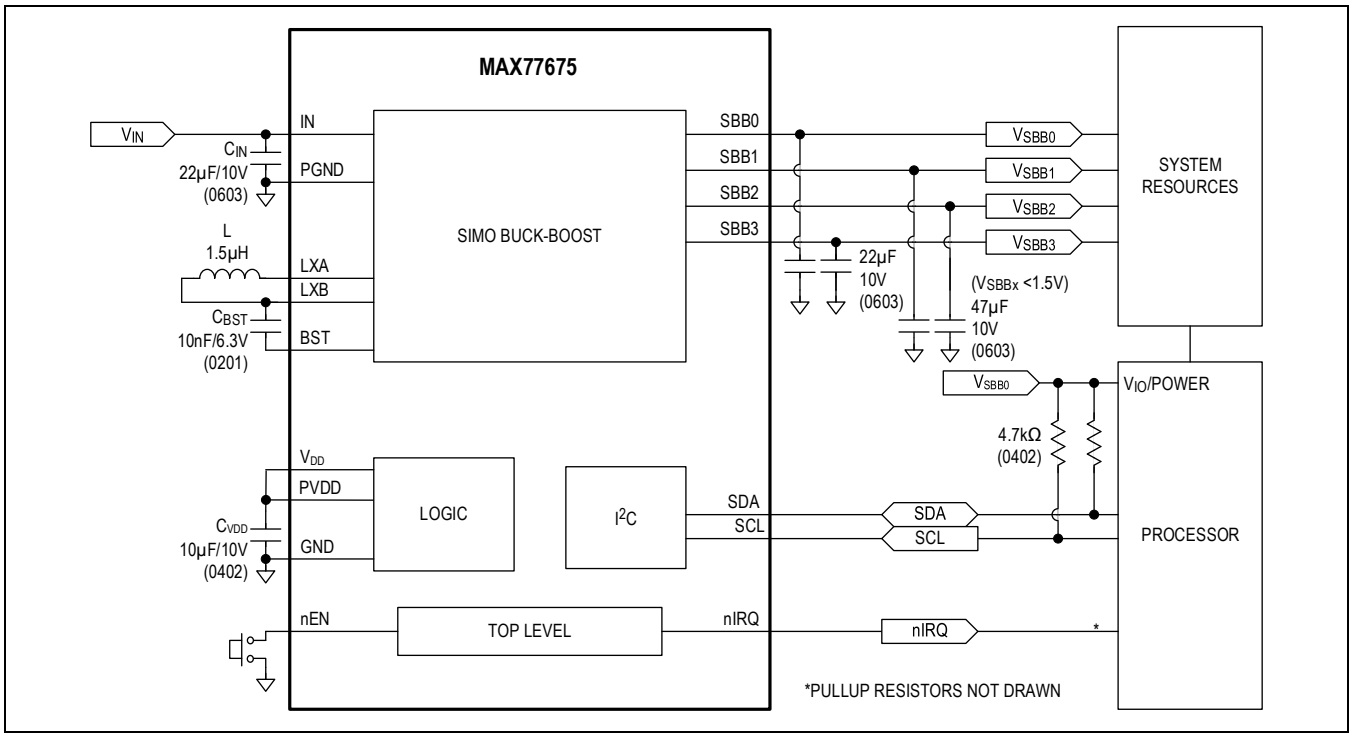


Figure 23. PCB Top Layer and Component Placement Example

Typical Application Circuits

Typical Applications Circuit



Ordering Information

PART	TEMP RANGE	PIN-PACKAGE	OPTIONS
MAX77675EWE+T*	-40°C to +85°C	16 WLP	—
MAX77675AEWE+T	-40°C to +85°C	16 WLP	See Table 1
MAX77675CEWE+T	-40°C to +85°C	16 WLP	See Table 1
MAX77675OEWE+T	-40°C to +85°C	16 WLP	See Table 1
MAX77675GEWE+T	-40°C to +85°C	16 WLP	See Table 1
MAX77675HEWE+T	-40°C to +85°C	16 WLP	See Table 1
MAX77675LEWE+T	-40°C to +85°C	16 WLP	See Table 1

+Denotes a lead(Pb)-free/RoHS-compliant package.

T = Tape and reel.

**Custom samples only. Not for production or stock. Contact factory for more information.*

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	3/23	Release for Market Intro	—
1	10/23	Updated Table 1 and *Ordering Information* table	24, 63
2	6/26	Updated *Pin Descriptions*, Table 1, *Applications Information* (Inductor Selection, Input Capacitor Selection, Output Capacitor Selection, PVDD and VDD Capacitors), and *Ordering Information*; added Figure 11 and Figure 13	20, 22, 23, 32, 36, 37, 56, 57, 59
3	7/26	Removed future product asterisks from MAX77675OEWE+T in the *Ordering Information* table	59
4	7/26	Removed future product asterisks from MAX77675GEWE+T, MAX77675HEWE+T, and MAX77675LEWE+T in the *Ordering Information* table	59
5	8/26	Added future product asterisks MAX77675GEWE+T**, MAX77675HEWE+T** in the *Ordering Information* table	59
6	9/26	Removed future product asterisks from MAX77675GEWE+T and MAX77675HEWE+T in the *Ordering Information* table	59

NOTES

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