5A Boost Converter with I²C Interface, Dynamic Voltage Scaling, and Short Circuit Protection

MAX77371

General Description

The MAX77371 is an ultrasonic, high-performance boost converter with an input voltage range from 2.5V to 5.5V and a configurable switching current limit of up to 5.0A. The IC operates in Ultrasonic mode (f_{SW} > 25kHz) at low loads and transitions into Skip and CCM modes of operation at higher load currents. When selected, the device can operate in forced PWM mode.

The output voltage can be widely varied between 4.5V and 10.0V.

The MAX77371 features a true shutdown mode that disconnects V_{IN} and V_{OUT} when the EN pin is pulled low. It also implements short circuit, overcurrent, voltage, and temperature protection features. The MAX77371 is available in a 20-bump, 0.35mm pitch wafer-level package (WLP).

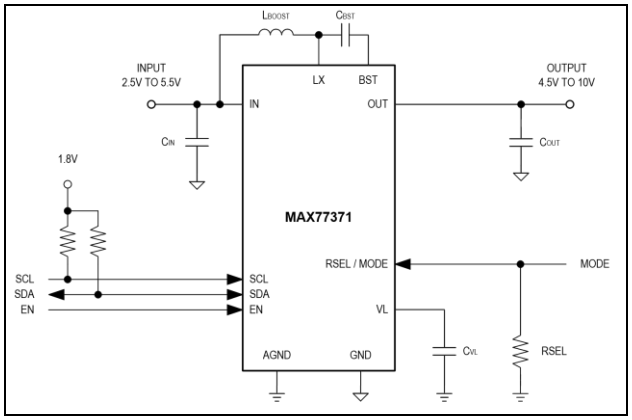
Applications

- AR/VR Laser Driver Bias
- Wireless Charging Circuit Bias

Features and Benefits

- 2.5V to 5.5V Input Voltage Range
- 4.5V to 10.0V Output Voltage Range
- Up to 5.0A Cycle-by-Cycle Inductor Current Limit
- 95% Peak Efficiency
- I²C Serial Interface Enabling:
  - Dynamic Voltage Scaling (DVS)
  - Mode Configuration
  - Current Limit Adjustment
- Ultrasonic Mode (USM with f_{SW} > 25kHz) to Alleviate Acoustic Audible Interference for Light Load Operation
- 2MHz Switching Frequency
- Forced PWM (FPWM) Operation
- True Shutdown Mode
  - Output Disconnects from Input with no Forward or Reverse Current
- Output Short Circuit Protection
- Overcurrent Protection
- Overvoltage Protection
- Thermal Shutdown Protection
- Package:
  - 1.89mm x 1.46mm, 0.35mm Pitch 20-Bump WLP
- -40°C to +125°C Operating Temperature Range

Simplified Application Diagram



Ordering Information appears at end of data sheet.

19-101967; Rev 3; 5/26

Absolute Maximum Ratings

IN to AGND .....-0.3V to +6.0V
SDA, SCL to AGND.....-0.3V to +2.0V
EN, RSEL to AGND..... -0.3V to IN + 0.3V
VL to AGND.....-0.3V to +2.2V
GND to AGND .....-0.3V to +0.3V
OUT to GND.....-0.3V to +17.8V
LX RMS current.....-4.0A to +4.0A
LX to GND..... -0.3V to OUT + 0.3[0]V
BST to GND ..... -0.3V to LX + 2.0V

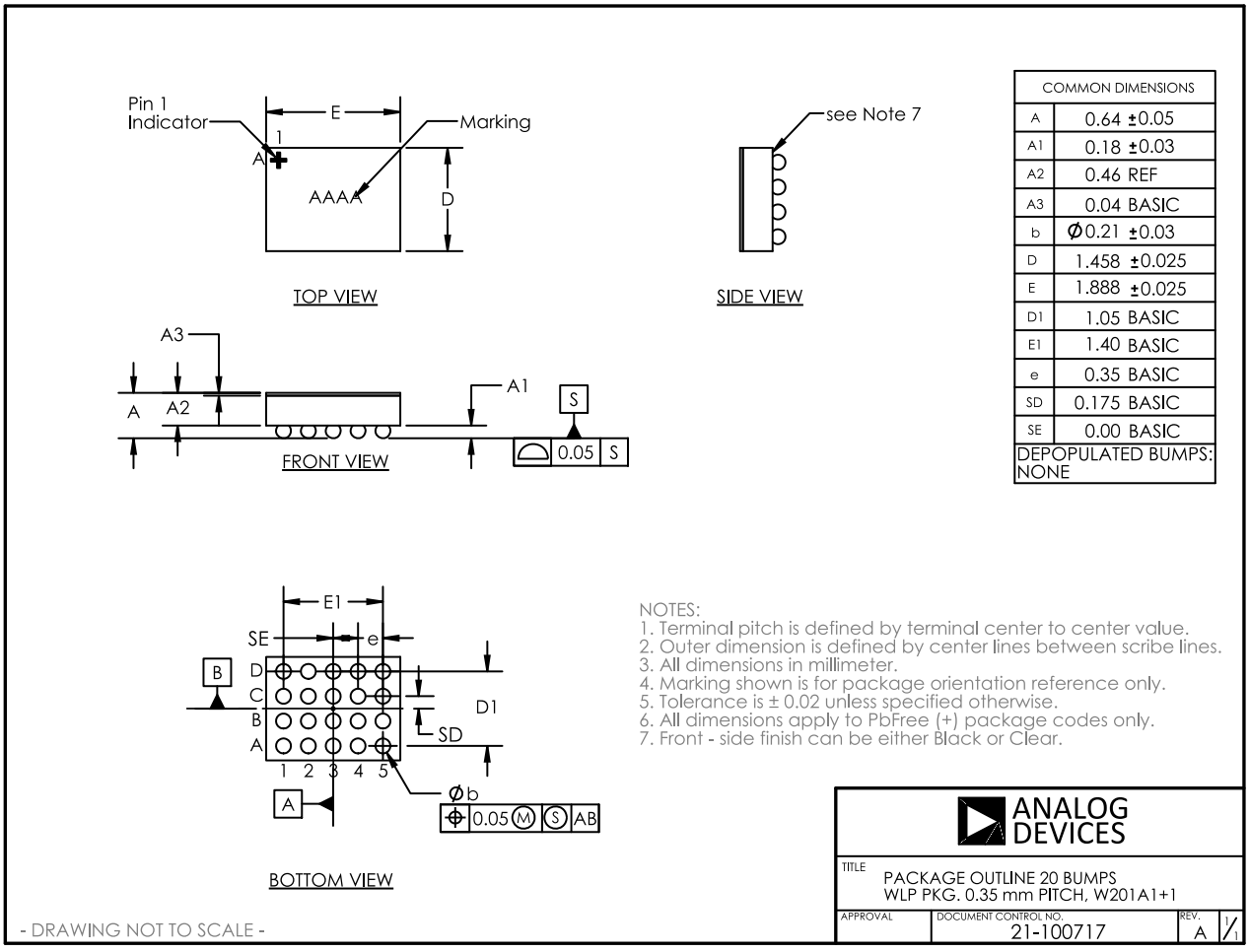
Output Short Circuit Duration ..... Continuous
Continuous Power Dissipation (T_A = +70°C) .....
(derate 15.73mW/°C above +70°C) 1258.46mW
Operating JunctionTemperature Range ..... -40°C to +125°C
Maximum Junction Temperature..... +150°C
Storage Temperature Range ..... -65°C to +150°C
Lead Temperature (soldering, 10 seconds)..... +300°C
Soldering Temperature (reflow)..... +260°C

Note 1: LX pin has internal clamps to GND and OUT. These diodes may be forward-biased during switching transitions. During these transitions, the max LX current should be within the Max RMS Current rating for safe operation.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Package Information

Package Code	W201A1+1
Outline Number	*21-100717*
Land Pattern Number	Refer to *Application Note 1891*
Thermal Resistance, Four Layer Board:	
Junction-to-Ambient (θ_{JA})	63.57°C/W
Junction-to-Case Thermal Resistance (θ_{JC})	N/A



COMMON DIMENSIONS	
A	0.64 ±0.05
A1	0.18 ±0.03
A2	0.46 REF
A3	0.04 BASIC
b	Ø0.21 ±0.03
D	1.458 ±0.025
E	1.888 ±0.025
D1	1.05 BASIC
E1	1.40 BASIC
e	0.35 BASIC
SD	0.175 BASIC
SE	0.00 BASIC
DEPOPULATED BUMPS: NONE	

NOTES:
1. Terminal pitch is defined by terminal center to center value.
2. Outer dimension is defined by center lines between scribe lines.
3. All dimensions in millimeter.
4. Marking shown is for package orientation reference only.
5. Tolerance is ± 0.02 unless specified otherwise.
6. All dimensions apply to PbFree (+) package codes only.
7. Front - side finish can be either Black or Clear.

ANALOG DEVICES

TITLE: PACKAGE OUTLINE 20 BUMPS
WLP PKG. 0.35 mm PITCH, W201A1+1

APPROVAL | DOCUMENT CONTROL NO. 21-100717 | REV. A | 1/1

Electrical Characteristics

(V_{IN} = 3.3V, V_{OUT} = 7.0V, EN = HIGH, T_J = -40ºC to +125ºC, unless otherwise specified; see *Table 2*.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Input Voltage Range	V_{IN}	Guaranteed by output accuracy test	2.5		5.5	V
Input Voltage UVLO	V_{IN_UVLO}	V_{IN} rising	2.0	2.1	2.2	V
		V_{IN} falling	1.8	1.9	2.0	
Supply Current into IN	I_{Q_IN}	V_{EN} = V_{IN}, not switching when in skip mode, V_{OUT} = 4.5V to 10.0V, T_J = -40°C to +85°C, (*Note 3*)		15	30	µA
		V_{EN} = V_{IN}, not switching when in ultrasonic mode, V_{OUT} = 4.5V to 9.0V, T_J = -40°C to +85°C, (*Note 3*)		240		
Input Shutdown Current	I_{SD_IN}	V_{EN} = 0V, V_{OUT} = 0V, T_J = +25°C		100	200	nA
LX Maximum Duty Cycle	DC_MAX	T_J = +25°C (*Note 4*)		90		%
POWER SWITCHES						
High-Side R_{DSON}	R_{DS_H}			30	57	mΩ
Low-Side R_{DSON}	R_{DS_L}			30	57	mΩ
Load Switch	R_{DS_LSW}			30	57	mΩ
OUTPUT VOLTAGE						
Output Voltage Range	V_{OUT}	Guaranteed by output accuracy test. V_{OUT} > V_{IN} + 200mV	4.5		10.0	V
Output Accuracy	V_{OUT_ACC}	Measured when the part in FPWM (*Note 5*)	-1.0		+1.0	%
Output Accuracy in USM	$V_{OUT\_ACC\_USM}$	Measured when the part is in ultrasonic or skip mode at no load, V_{OUT} = 4.5V to 9.0V, T_J = -40°C to +85°C (*Note 5*)			+4	%
DC Load Regulation	ACC_{LOAD}	Load from 50mA to I_{OUT} at 80% of peak inductor current limit (5.0A setting)		-1.0		%
DC Line Regulation	ACC_{LINE}	Duty cycle varied from 25% to maximum		-1.0		%
Overvoltage Protection Threshold	V_{OVP}			17.2		V
Overvoltage Protection Release Threshold	V_{OVP_REL}			16.5		V
SWITCHING PERFORMANCE						
Switching Frequency	f_{SW}	V_{IN} = 2.5V to 5.5V, DC_MAX > DC > 22%, T_J = +25°C		2.0		MHz
LX t_{ON}	t_{ON}	V_{IN} = 3.3V, V_{OUT} = 5.0V (*Note 6*)	136	170	204	ns
		V_{IN} = 3.3V, V_{OUT} = 7.0V (*Note 6*)	211	264	317	
LX Minimum t_{ON}	t_{ON_MIN}	(*Note 6*)	40	50	60	ns
LX Minimum t_{OFF}	t_{OFFMIN}			120		ns
LIGHT LOAD PERFORMANCE						
Ultrasonic Mode Minimum Switching Frequency	f_{USM}	V_{IN} = 2.5V to 5.5V, V_{OUT} - V_{IN} > 250mV	25	31	36	kHz
Zero Crossing Threshold	I_{ZX_LX}	Out of ultrasonic mode, operating in skip mode (*Note 7*)	75	150	225	mA
STARTUP						

(V_{IN} = 3.3V, V_{OUT} = 7.0V, EN = HIGH, T_J = -40ºC to +125ºC, unless otherwise specified; see *Table 2*.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Soft-Start Rate	dV/dt	V_{IN} = 3.3V, V_{OUT} from 5.0V to 10.0V, in boost mode, C_{OUT_EFF} = 10µF, T_J = +25°C			1.0		V/ms
ENABLE, RSEL, ACTIVE DISCHARGE							
Required Select Resistor Accuracy	ACC_{RSEL}	Use the resistor from the RSEL Selection table		-1		+1	%
Select Resistor Detection Time	t_{RSEL}	C_{RSEL} < 2pF, (*Note 8*)			600	1320	µs
Active Discharge Resistance	R_{DIS}	Between OUT and GND			100	200	Ω
Enable Input Leakage	I_{LEAK_EN}	T_J = +25°C, V_{EN} = 5.5V			1	150	nA
Enable Voltage High Threshold	V_{IH}	V_{EN} rising, LX begins switching			0.8	1.2	V
Enable Voltage Low Threshold	V_{IL}	V_{EN} falling, LX stops switching		0.4			V
RSEL/MODE High Threshold	V_{IH}	V_{MODE} rising			0.8	1.2	V
RSEL/MODE Low Threshold	V_{IL}	V_{MODE} falling		0.4			V
PROTECTION							
Inductor Peak Current Limit	I_{PEAK_LX}	V_{OUT} = 7.0V (*Note 7*)	Default OTP recipe	4.5	5.0	5.5	A
			Default OTP recipe	3.6	4.0	4.4	
Short Circuit Current Limit	I_{SC}	V_{IN} > V_{OUT}		560	700	890	mA
Thermal Shutdown Threshold	T_{SHUT_R}	T_J rising			165		°C
	T_{SHUT_F}	T_J falling			150		
SDA AND SCL I/O STAGE							
SCL, SDA Input High Voltage	V_{IH}	SCL, SDA pulled to 1.2V or 1.8V		0.8			V
SCL, SDA Input Low Voltage	V_{IL}	SCL, SDA pulled to 1.2V or 1.8V				0.4	V
SCL, SDA Input Leakage Current	$I_{SCL\_SDA\_LKG}$	SCL, SDA pulled to 1.2V or 1.8V, V_{SCL} = V_{SDA} = 0V and 2.0V		-10		+10	µA
SDA Output Low Voltage	V_{OL}	Sinking 20mA				0.4	V
SCL, SDA Pin Capacitance	C_{IN}	SCL, SDA pulled to 1.2V or 1.8V			10		pF
Fall Time from V_{IH} to V_{IL}	t_{FALL} (*Note 9*)					120	ns
I²C Enable Time	t_{I2C_EN}	EN = high to first I²C command			900		µs
I²C-COMPATIBLE INTERFACE TIMING (STANDARD, FAST, AND FAST-MODE PLUS) (*Note 9*)							
Clock Frequency	f_{SCL}			0		1000	kHz
Hold Time (REPEATED) START Condition	t_{HD_STA}			0.26			µs
SCL Low Period	t_{LOW}			0.5			µs
SCL High Period	t_{HIGH}			0.26			µs
Setup Time (REPEATED) START Condition	t_{SU_STA}			0.26			µs

(V_{IN} = 3.3V, V_{OUT} = 7.0V, EN = HIGH, T_J = -40ºC to +125ºC, unless otherwise specified; see *Table 2*.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Data Hold Time	t_{HD_DAT}		0			ns
Data Setup Time	t_{SU_DAT}		50			ns
Setup Time for STOP Condition	t_{SU_STO}		0.26			µs
Bus Free Time Between STOP and START Conditions	t_{BUF}		0.5			µs
Pulse Width of Suppressed Spikes	t_{SP}	Maximum pulse width of spikes that must be suppressed by the input filter		50		ns

Note 2: Limits over the specified operating temperature and supply voltage range are guaranteed by design, characterization, and production tested at room temperature only.

Note 3: This measurement was taken in test mode.

Note 4: Guaranteed by measuring LX frequency. Maximum duty cycle is a function of input voltage since LX on time varies with V_{IN}.

Note 5: This does not include load, line regulation, and effects of output voltage ripple.

Note 6: Does not include delays.

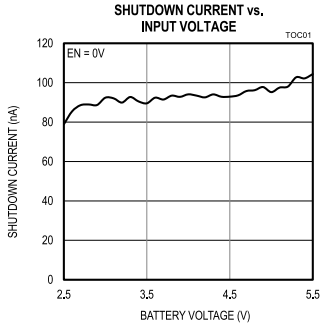
Note 7: This is a static measurement. Due to propagation delays, the actual peak current limit depends on V_{IN} and L.

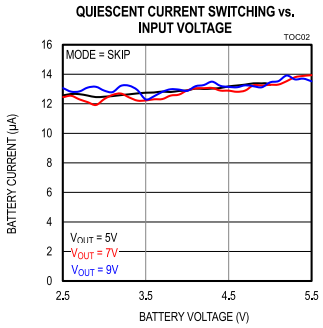
Note 8: This is the time required to determine the RSEL value. This time adds to the startup time.

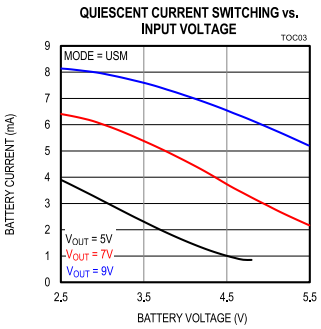
Note 9: Design guidance only. Not Production tested.

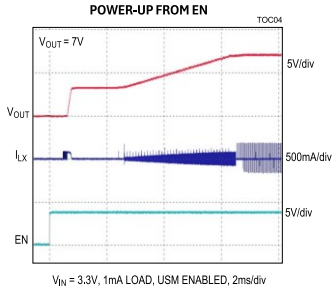
Typical Operating Characteristics

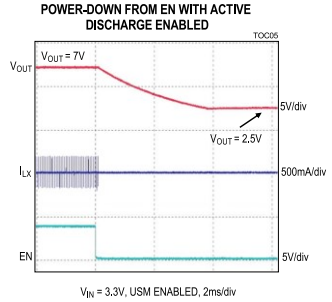
(V_{IN} = 3.3V, V_{OUT} = 7V, I_{PEAK} = 5A, L = CIGW252012TMR47ML(0.47µH), Mode = Skip, unless otherwise noted.)

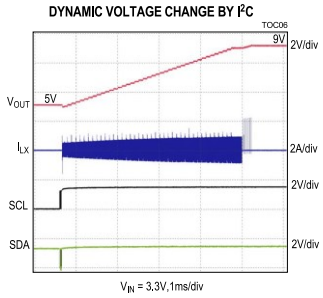


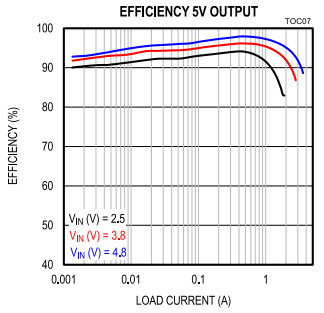


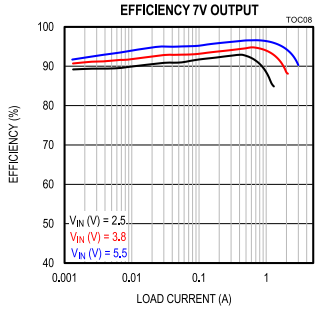


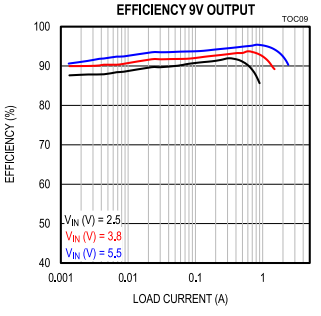






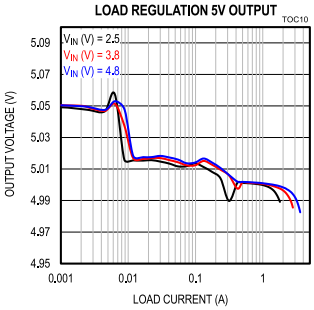




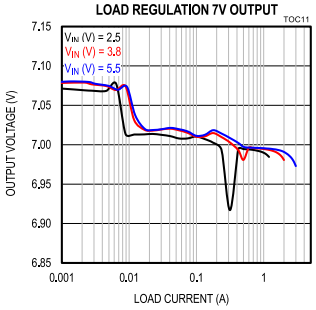


(V_{IN} = 3.3V, V_{OUT} = 7V, I_{PEAK} = 5A, L = CIGW252012TMR47ML(0.47µH), Mode = Skip, unless otherwise noted.)

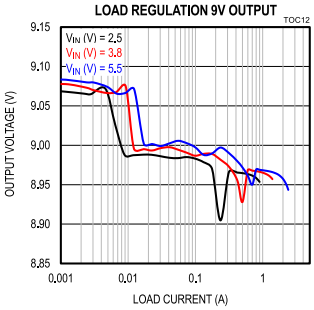
LOAD REGULATION 5V OUTPUT



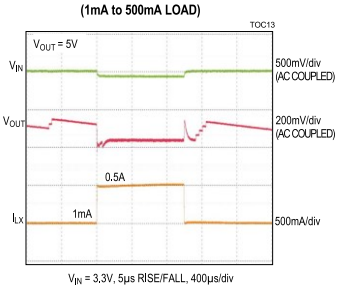
LOAD REGULATION 7V OUTPUT



LOAD REGULATION 9V OUTPUT

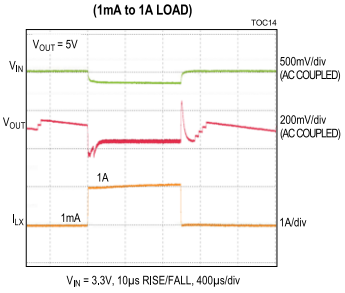


LOAD TRANSIENT (1mA to 500mA LOAD)



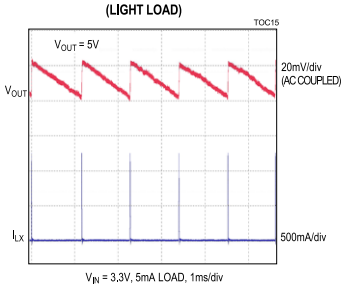
VIN = 3.3V, 5µs RISE/FALL, 400µs/div

LOAD TRANSIENT (1mA to 1A LOAD)



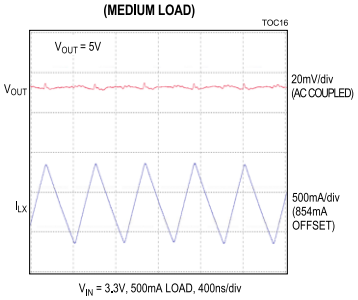
VIN = 3.3V, 10µs RISE/FALL, 400µs/div

SWITCHING WAVEFORM (LIGHT LOAD)



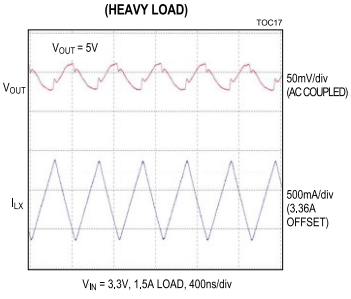
VIN = 3.3V, 5mA LOAD, 1ms/div

SWITCHING WAVEFORM (MEDIUM LOAD)



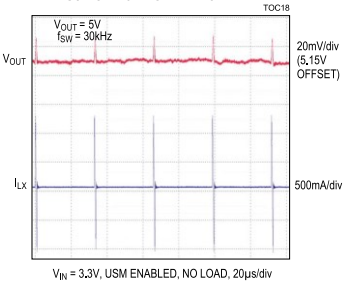
VIN = 3.3V, 500mA LOAD, 400ns/div

SWITCHING WAVEFORM (HEAVY LOAD)



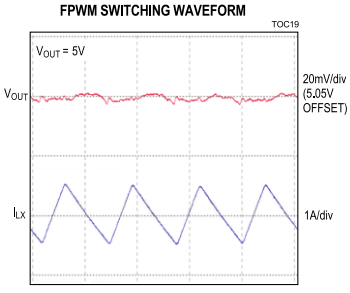
VIN = 3.3V, 1.5A LOAD, 400ns/div

USM SWITCHING WAVEFORM



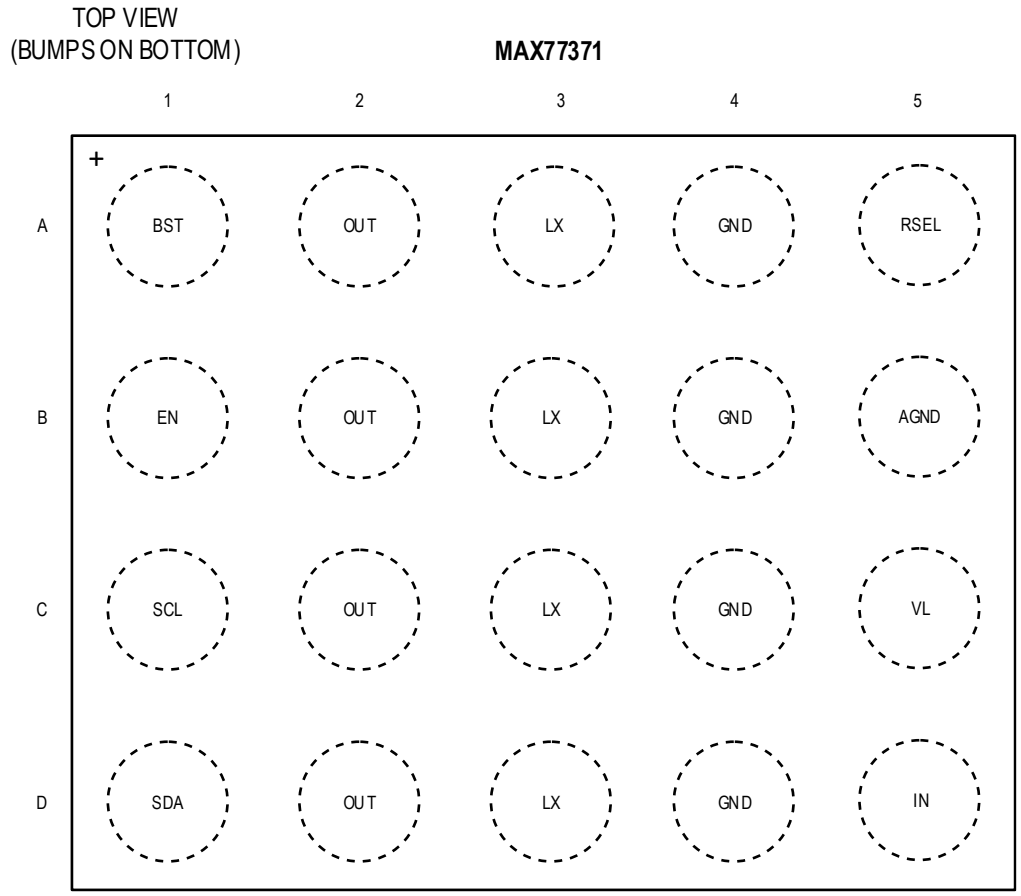
VIN = 3.3V, USM ENABLED, NO LOAD, 20µs/div

FPWM SWITCHING WAVEFORM



VIN = 3.3V, FPWM ENABLED, NO LOAD, 1µs/div

Pin Configurations



WLP
(20-BUMP, 0.35mm PITCH)

Pin Descriptions

PIN	NAME	FUNCTION	Type
A1	BST	Bootstrap pin for driving high-side MOSFET. Connect a 100nF capacitor between the LX and BST pin with minimum loop inductance.	Power
A2, B2, C2, D2	OUT	Output pins. Connect ceramic capacitors between OUT to GND.	Power
A3, B3, C3, D3	LX	Switching node pins. Connect an inductor from LX to the input supply node.	Power
A4, B4, C4, D4	GND	Power ground pins. Connect to system GND.	Ground
A5	RSEL/ MODE	Configuration and mode select pin. Connect a resistor from RSEL to GND to select the desired configuration. After the device starts, the RSEL circuit is disabled, and the pin is configured as a digital input. Drive this pin high to enable forced PWM mode after power-up. Forcing the pin low or leaving it pulled low will revert back to the light load efficient mode of operation acquired at the startup, see *Table 2*. Care must be taken that the total capacitance on this pin should be less than 2pF. Note the driving signal cannot be higher than V_{IN}. Furthermore, external signal drivers may not be strong enough to drive very low impedance RSEL resistance, in which case forcing PWM operation through the I²C interface is desired.	Analog/Digital
B1	EN	Enable the input pin. Force this pin to higher than 1.2V to enable the boost converter. Force this pin below 0.4V to disable the part and enter True Shutdown Mode. Connect to IN if the feature is not used. Note the driving signal cannot be higher than V_{IN}.	Digital
B5	AGND	Analog ground pin. Connect to system GND.	Ground
C1	SCL	Open drain I²C clock input pin. Pull it up to a 1.2V or 1.8V V_{IO} system voltage rail.	Digital
C5	VL	1.8V internal regulator output pin. Connect a 1.0µF capacitor between this pin and GND.	Power
D1	SDA	Open drain I²C data pin. Pull it up to 1.2V or 1.8V V_{IO} system voltage rail.	Digital
D5	IN	Input pin. Connect a 22µF ceramic capacitor from IN to ground. Depending on the specific application requirements, more capacitance may be needed.	Power

OTP Options

The MAX77371A device will have default features selected through the RSEL function and external RSEL resistor. The MAX77371P has the RSEL function disabled; default features are preprogrammed in nonvolatile memory, as seen in *Table 1*. Both devices use the same I²C address, 0x20, in seven-bit representation.

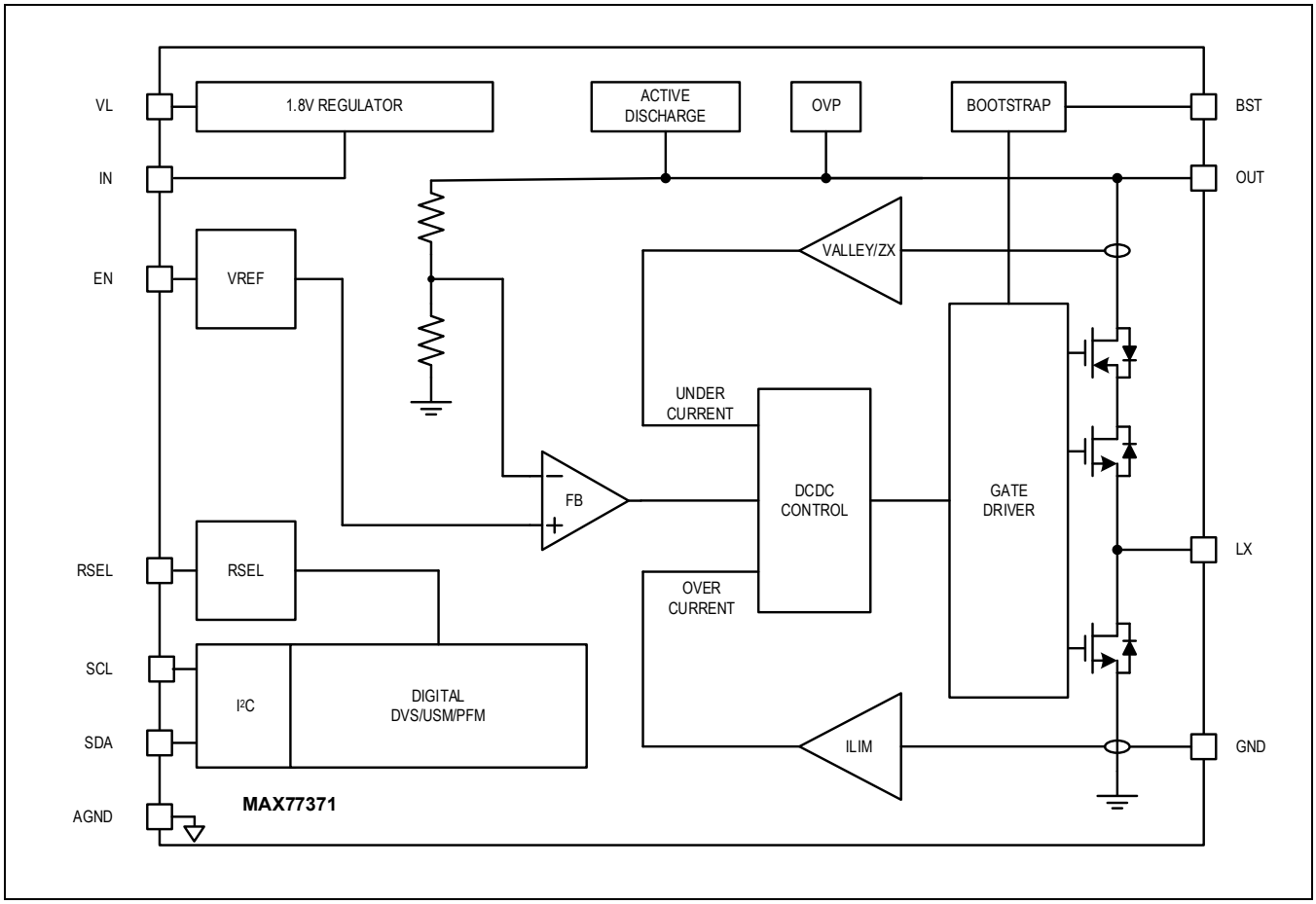
Table 1. OTP Options Table

FEATURES	PART NUMBER	PART NUMBER
	MAX77371AAWP+	MAX77371PAWP+
I²C Address	0 x 20*	0 x 20*
ILIM	RSEL**	5A
USM	RSEL**	No
V_{OUT}	RSEL**	5.1V

** 7-bit representation.*

***Default selected by RSEL.*

Functional Diagrams



Detailed Description

The MAX77371 is an ultrasonic boost converter with an input voltage range of 2.5V to 5.5V. The output voltage is adjustable between 4.5V and 10.0V using a single external resistor connected between RSEL and GND or through an I²C-accessible register. The IC operates in Ultrasonic Mode (USM), Skip Mode, Discontinuous Conduction Mode, and Continuous Conduction Mode (CCM) depending on a user selection or load conditions. In Ultrasonic Mode, the switching frequency of the IC is kept above 25kHz even at light loads to stay away from the audible frequency range. The IC can operate in the CCM mode regardless of the load levels by enabling the FPWM mode. The part is equipped with a cycle-to-cycle switch current limit, thermal shutdown, overvoltage, and short circuit protection to protect the system and the device itself.

Operation

Using the RSEL configuration feature, the IC can be configured in an auto skip or auto ultrasonic mode. In auto skip mode, the switching frequency is lowered at light load to improve efficiency. In auto ultrasonic mode, a minimum switching frequency of 25kHz is enforced. The ultrasonic mode can also be controlled through an I²C-accessible register.

The IC features an FPWM mode of operation. In this mode, quasi-constant switching frequency of about 2.0MHz is enabled regardless of load level. This mode can be controlled through the RSEL/MODE pin or an I²C-accessible register.

Skip Mode

In skip mode, the MAX77371 skips the switching cycles and regulates the output voltage at a higher threshold (2% nominal). This reduces the switching losses and improves efficiency at light load conditions.

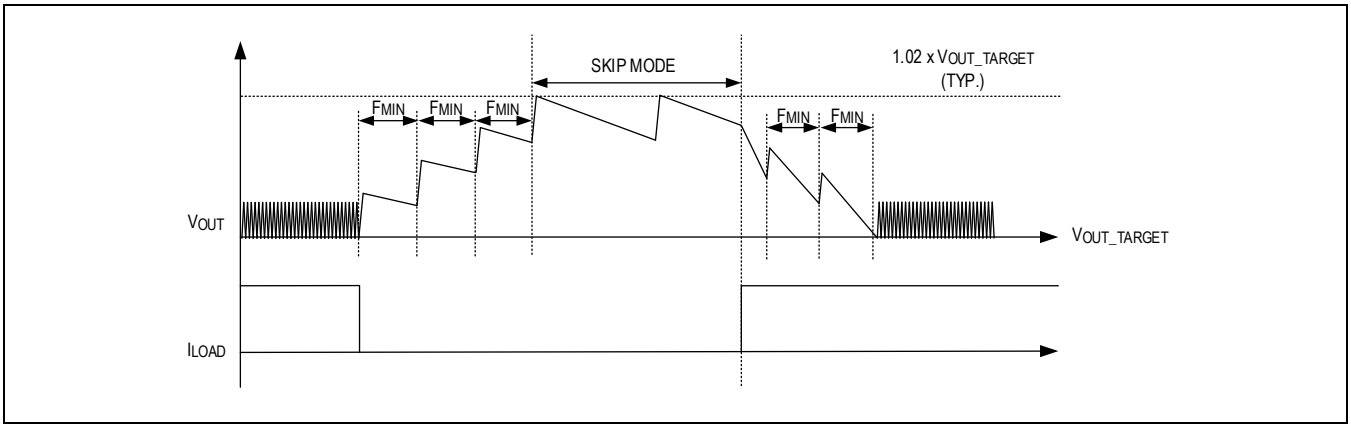


Figure 1. Skip mode operation

Ultrasonic Mode

The IC features ultrasonic mode (USM) in which the converter seamlessly operates at a switching frequency of 30kHz (typical) to avoid acoustic audible noise interference while operating at light loads. The USM circuit operates by clamping the minimum switching frequency. When the load current reduces, the switching frequency decreases until it reaches 30kHz (typical). USM is turned on at this stage. In USM, the IC switches at 30kHz (typical) until the output voltage reaches 2% above the output voltage target. The device then continues switching at about 30kHz (typical) while keeping the boost discharge cycle on even after the inductor current crosses 0A, resulting in the output capacitor discharging to the input. This extra cycle is necessary to prevent the output voltage from ramping up.

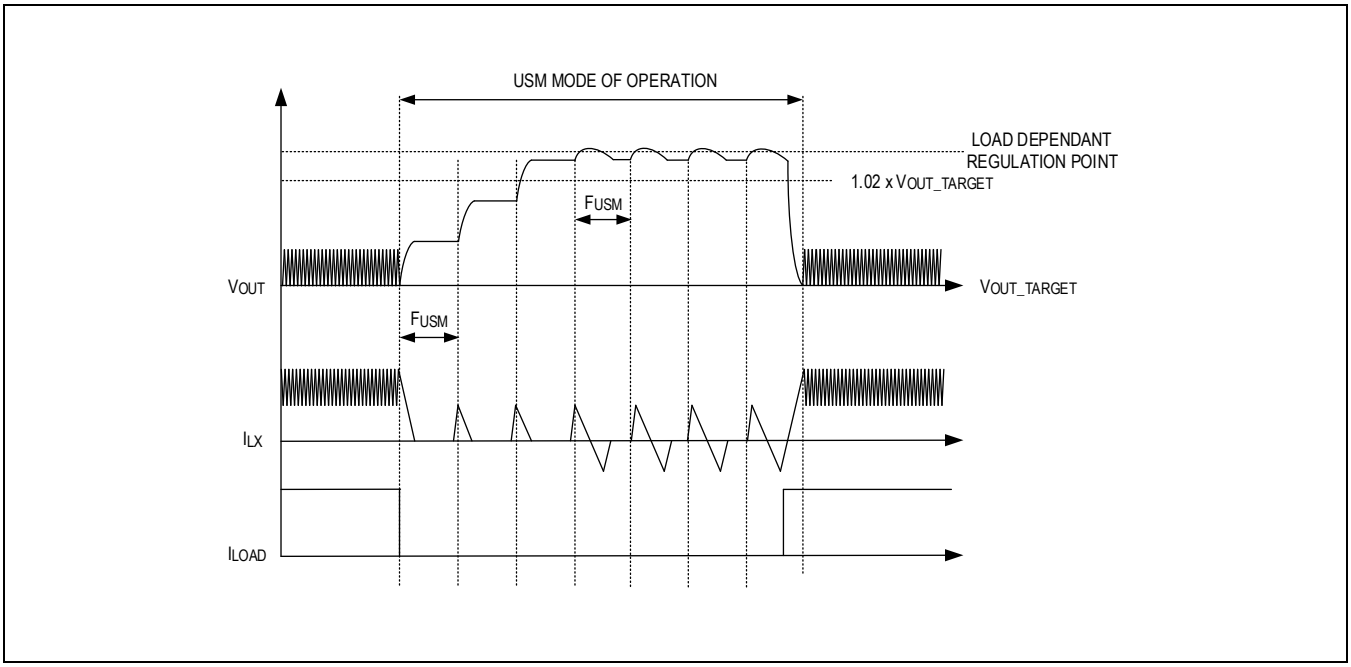


Figure 2. Ultrasonic mode operation

Forced PWM and Continuous Conduction Mode

Forced PWM mode is enabled through a pin (RSEL/Mode) or an I²C-accessible register. In forced PWM mode, the IC keeps the switching frequency quasi-constant at about 2MHz across the whole load range. When the load current decreases, the output of the internal error amplifier decreases to lower the inductor peak current and deliver less power. The high-side FET is not turned off even if the current through the FET goes negative to maintain the switching frequency at the heavy load.

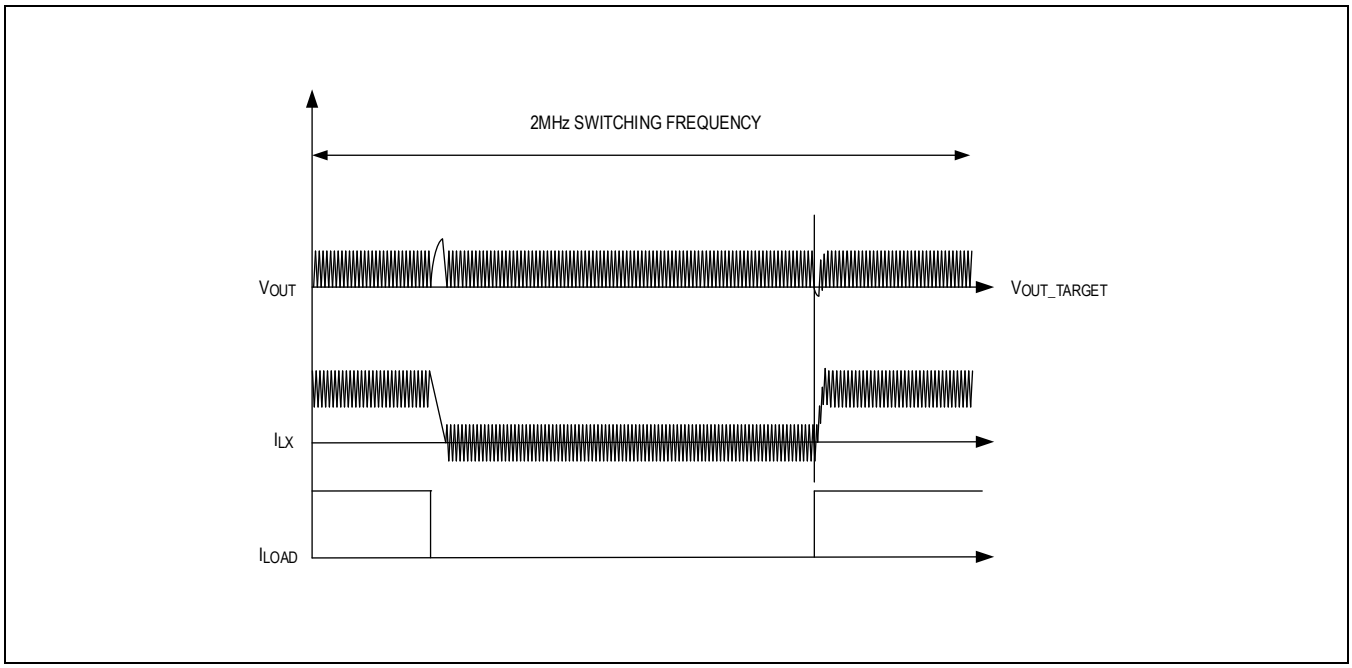


Figure 3. Forced PWM operation

Configuration Selection

The IC has a unique single resistor output selection method where the resistor connected between RSEL and GND is used to select different device configurations. The advantages of using a single RSEL are as follows:

- Lower cost and smaller size since only one resistor is needed versus the two resistor strings needed in typical feedback connections.
- No power loss through feedback resistors during operation, leading to higher efficiency.
- It allows customers to stock just one part in their inventory system and use it in multiple projects with different output voltages by changing a single standard 1% resistor.

Table 2. RSEL Table

OUTPUT VOLTAGE (V)	ILIM (A)	DCM MODE	RSEL (Ω)*
4.5	5.0	USM	OPEN
5.0	5.0	USM	100000
5.5	5.0	USM	86600
6.0	5.0	USM	75000
6.5	5.0	USM	64900
7.0	5.0	USM	56200
7.5	5.0	USM	48700
8.0	5.0	USM	42200
8.5	5.0	USM	36500
9.0	5.0	USM	30900
10.0	5.0	Skip	26100

OUTPUT VOLTAGE (V)	ILIM (A)	DCM MODE	RSEL (Ω)*
4.5	4.0	USM	2870
5.0	4.0	USM	2490
5.5	4.0	USM	2150
6.0	4.0	USM	1870
6.5	4.0	USM	1620
7.0	4.0	USM	1400
7.5	4.0	USM	1210
8.0	4.0	USM	1050
8.5	4.0	USM	909
9.0	4.0	USM	768
10.0	4.0	Skip	649
Special Trim**	—	—	Short to Ground

** Use a standard 1% resistor at the RSEL pin.*

***For special trim, contact an Analog Devices representative.*

The RSEL functionality is disabled in the MAX77371PAWP+ version. The default output voltage, peak current, and mode of operation are set through OTP to 5.0V, 5.0A, and skip mode. The RSEL/MODE pin is used only for MODE functionality. The pin is tristated at startup and cannot be used to enable FPWM. After the startup ends, the MODE pin can be pulled high/low to change the mode of operation to/from FPWM. The I²C interface can be used to read the default settings and to modify configuration.

Active Discharge

The IC offers configurable active discharge functionality. The active discharge feature is enabled (OUT_DIS = 0) by default and it can be disabled (OUT_DIS =1) through I²C. The active discharge feature allows V_{OUT} to be discharged to PGND through an internal 100Ω resistor for a small amount of time when the boost regulator is turned off. The boost regulator can be turned off by pulling EN low.

With active discharge enabled, the output voltage discharge rate is a function of output capacitance, external load, and internal active discharge resistance. With active discharge disabled, the output voltage discharge rate is a function of output capacitance and external load.

Enable and Disable

The IC is enabled when the input voltage is above the UVLO threshold and the EN pin is pulled above 1.2V. When the EN pin is pulled below 0.4V, the IC goes into true shutdown mode. If the feature is not used, EN can be tied to IN. Note that the EN driving signal cannot be higher than V_{IN}.

Once EN is pulled low, switching stops and output is allowed to be discharged for 4.0ms and below 4.0V (nominal) before the active discharge circuit gets disengaged.

Startup

The IC startup sequence is initiated at an EN transition to a logic high or input voltage crossing the rising UVLO threshold if EN is tied to IN. In the first step, the RSEL is acquired which typically takes 600µs. Then, the LX pin gets pulled low for several cycles to ensure the BST capacitor gets properly charged. After this, the output is linearly charged with a constant 700mA until it reaches the input voltage level. Subsequently, as soon as the internal reference catches up to the output level, the boost regulator turns on and the boost soft start routine begins. The IC implements a 1V/ms soft start rate to control inrush current into output capacitors. If output is overloaded during the linear charging phase, the device goes into a hiccup mode where it will pause the startup for about 7.0ms before it initiates another startup attempt.

Undervoltage Lockout

When the input voltage falls below the UVLO falling threshold during the operation, the IC disables the output immediately. If the EN pin is kept HIGH, the IC automatically reinitiates the startup procedure when the input voltage rises above the UVLO rising threshold.

Load Disconnect

The IC features a load disconnect function that completely disconnects the output from the input during shutdown or fault conditions.

Applications Information

Inductor Selection

Select an inductor with a saturation current rating (ISAT) greater than or equal to the maximum switching current limit threshold (ILIM) setting. In general, inductors with lower saturation current and higher DCR ratings are physically small. Higher values of DCR reduce converter efficiency. Choose the inductor's RMS current rating (IRMS) (the current at which the temperature rises appreciably) based on the maximum expected load condition. The chosen inductor value should ensure that the peak-inductor ripple current (I_{PEAK}) is below the ILIM setting so that the converter can maintain regulation. The inductors recommended for different ranges of output voltages are shown in *Table 3*.

Table 3. Inductor and Output Capacitor Selection

OUTPUT VOLTAGE RANGE (V)	RECOMMENDED INDUCTANCE VALUE (nH)	EFFECTIVE OUTPUT CAPACITANCE REQUIRED (µF)
4.5 to 5.5	330	15
5.0 to 9.0	470	15 at 5.0V 10 at 7.0V 8 at 9.0V
9.0 to 10.0	680	7 at 10.0V

**For instance, the effective capacitance requirement can be achieved using 4 x 22µF, X5R, 0603 capacitors.*

Input Capacitor Selection

For most applications, use a 10V 22µF nominal ceramic input capacitor (CIN) that maintains 7µF or higher effective capacitance at its working voltage. Effective CIN is the actual capacitance value seen from the converter input during operation. Larger values improve decoupling for the converter but increase inrush current from the voltage supply when connected. CIN reduces the current peaks drawn from the input power source and reduces switching noise in the system. The ESR/ESL of CIN and its series PCB trace should be very low (i.e., < 15mΩ + < 2nH) for frequencies up to the converter's switching frequency. Pay special attention to the capacitor's voltage rating, initial tolerance, variation with temperature and AC ripple, and DC bias characteristics when selecting CIN. Ceramic capacitors with X7R dielectrics are highly recommended due to their small size, low ESR, and small temperature coefficients. In applications with a maximum ambient temperature below 85°C, X5R dielectric ceramic capacitors are also recommended. All ceramic capacitors derate with DC bias voltage (effective capacitance goes down as DC bias goes up). Generally, smaller case-size capacitors derate more heavily compared to larger case sizes (0603 case size performs better than 0402). Consider the effective capacitance value carefully by consulting the manufacturer's data sheet. Refer to *Tutorial 5527* for more information.

Output Capacitor Selection

Sufficient output capacitance (C_{OUT}) is required for stable operation of the converter. For minimum effective output capacitance for different output voltage targets are shown in *Table 3*. Effective C_{OUT} is the actual capacitance value seen by the converter output during operation. Larger values (above the required effective minimum) improve load transient performance but increase input surge currents during soft start and output voltage changes. The output filter capacitor must have low enough ESR for frequencies up to the converter's switching frequency to meet output ripple and load transient requirements. The output capacitance must be high enough to absorb the inductor energy while transitioning from full load to no-load conditions. For most applications, 4 x 22µF capacitors ($25V_{DC}$) is recommended for C_{OUT}. Pay special attention to capacitor's voltage rating, initial tolerance, variation with temperature and AC ripple, and DC bias characteristics when selecting C_{OUT}. Ceramic capacitors with X7R dielectrics are highly recommended due to their small size, low ESR, and small temperature coefficients. In applications with maximum ambient temperature below 85°C, X5R dielectric ceramic capacitors are also recommended. All ceramic capacitors derate with DC bias voltage (effective capacitance goes down as DC bias goes up). Generally, smaller case-size capacitors derate more heavily compared to larger case sizes (0603 case size performs better than 0402). Consider the effective capacitance value carefully by consulting the manufacturer's data sheet. Refer to *Tutorial 5527* for more information.

Bootstrap Capacitor Selection

The MAX77371 integrates bootstrap circuit that requires a small external ceramic capacitor between the BST and SW pins to provide the gate drive voltage for the high-side FET. The recommended value for this ceramic capacitor is 100nF.

RSEL Resistor Selection

The resistor between RSEL pins and GND should have a tolerance of ±1% for the internal ADC to read the value accurately.

PCB Layout Guidelines

A careful circuit board layout is critical for low switching power losses and clean, stable operation.

When designing the PCB, use the following guidelines:

- Place the input capacitors (C_{IN}) and output capacitors (C_{OUT}) immediately next to the IN and OUT pins of the IC, respectively. Since the IC operates at a high switching frequency with a fast LX edge, this placement is critical for minimizing parasitic inductance within the input and output current loops, which can cause high voltage spikes and can damage the internal switching MOSFETs.
- When routing LX traces on a separate layer, make sure to include enough vias to minimize trace impedance. Routing LX traces on multiple layers is recommended to reduce trace impedance further. Furthermore, do not let LX traces take up an excessive area. The voltage on this node switches very quickly, and additional area creates more radiated emissions.
- Connect the GND bumps to the low-impedance ground plane on the PCB with vias placed next to the bumps. Do not create GND islands, as GND islands risk interrupting the hot loops.
- Keep the power traces and load connections short and wide. This is essential for high converter efficiency. Do not neglect ceramic capacitor DC voltage derating. Choose capacitor values. See the *Output Capacitor Selection* section and refer to *Tutorial 5527* for more information.

Register Map

User Registers

Registers reset when shut down.

ADDRESS	NAME	MSB							LSB
User Registers									
0x00	GLOBAL 1[7:0]	FPWM_EN	USM_EN	–	–	–	OUT_DIS	ILIM_SELECT	SLEW_RATE
0x02	VOUT_SELECT[7:0]	VOUT[7:0]							

Register Details

GLOBAL 1 (0x0)

BIT	7	6	5	4	3	2	1	0
Field	FPWM_EN	USM_EN	–	–	–	OUT_DIS	ILIM_SELECT	SLEW_RATE
Reset	0x0	0b0	–	–	–	0b0	0b0	0b0
Access Type	Write, Read	Write, Read	–	–	–	Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
FPWM_EN	7	Forced PWM Mode Enable	0x0: FPWM mode is set by the RSEL/MODE pin 0x1: FPWM mode is enabled regardless of the state of the RSEL/MODE pin
USM_EN	6	Ultra-sonic Mode Enable*	0x0: Ultra-sonic mode is disabled. 0x1: Ultra-sonic mode is enabled.
OUT_DIS	2	Output Discharge	0x0: Enable 0x1: Disable
ILIM_SELECT	1	ILIM Setting*	0x0: 4A 0x1: 5A
SLEW_RATE	0	Slew rate options during DVS	0x0: 1.0V/ms 0x1: 5.0V/ms

VOUT_SELECT (0x2)

BIT	7	6	5	4	3	2	1	0
Field	VOUT[7:0]							
Reset	0x0							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
VOUT	7:0	Output Voltage Selection 100 mV Resolution, Default selected by RSEL	0x0: Reserved 0x1: Reserved ... 0x1D: 4.5V 0x1E: 4.6V 0x54: 10V 0x55: Reserved ... 0xFF: Reserved

*Defaulted selected by RSEL

I²C Address

The I²C addresses are shown in *Table 4*.

Table 4. I²C Address

7-BIT ADDRESS	8-BIT WRITE ADDRESS	8-BIT READ ADDRESS
0 x 20, 0b 010 0000	0 x 40, 0b 0100 0000	0 x 41, 0b 0100 0001
0 x 28, 0b 010 1000	0 x 50, 0b 0101 0000	0 x 51, 0b 0101 0001

The default device has a 0 x 20 I²C address (7-bit representation) programmed in OTP.
The variant device has a 0 x 28 I²C address (7-bit representation) programmed in OTP.

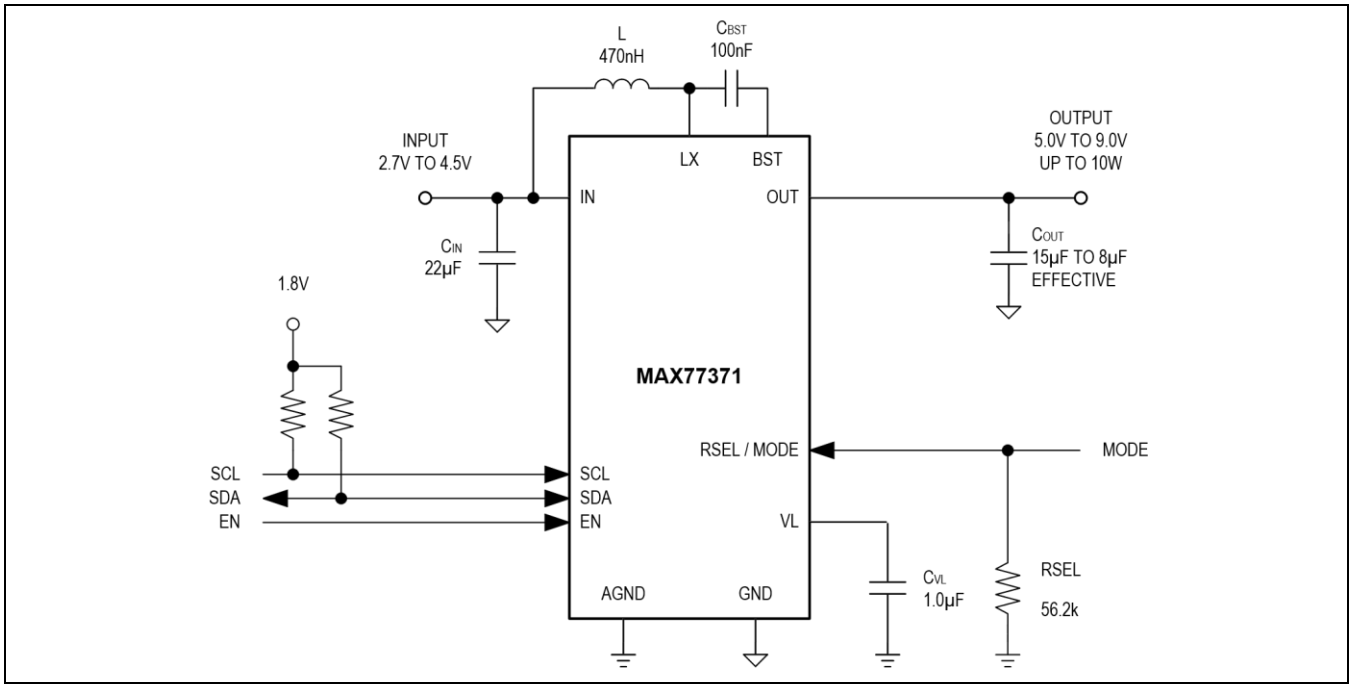
I²C Interface User Guidelines

The I²C interface is activated 900µs after the device is enabled. Output voltage scaling will take effect after the device reaches regulation into the default target level. Changing the mode of operation, current limit level, or slew rate through I²C is not recommended before the default regulating point has been reached. Upon reset, either by disabling MAX77371 or due to UVLO protection, I²C accessible run-time registers will be reset to default values. The default values follow the settings in *Table 5*.

Table 5. MAX77371PAWP+ Default I²C Register Values

REGISTER BITFIELD	DEFAULT SETTING
SLEW_RATE	1.0V/ms
ILIM_SELECT	5A
OUT_DIS	Enabled
USM_EN	Disabled
FPWM_EN	Disabled
V_{OUT}	5.1V

Typical Application Circuit



Ordering Information

PART NUMBER	TEMP RANGE	PACKAGE	OPTIONS
MAX77371AAWP+T	-40°C to +125°C	WLP	Table 1
MAX77371PAWP+T	-40°C to +125°C	WLP	Table 1

+Denotes a lead(Pb)-free/RoHS-compliant package.
T = Tape and reel.

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	1/25	Initial release	—
1	3/25	Updated *Electrical Characteristics* table, *Operation* section, and *Ordering Information* table	3–5, 10, 18
2	4/25	Updated *Register Details* section	15, 16
3	5/26	Added POD to *Package Information* section, updated *Configuration Selection* section	3, 14