Click here to ask an associate for production status of specific part numbers.

Ultra-Low I_Q, Low-Noise 3.5W Buck-Boost Converter

MAX77348A, MAX77348B

General Description

The MAX77348 is an ultra-low quiescent current, non-inverting buck-boost converter capable of supporting up to 3.5W output power. The device employs a unique control algorithm that seamlessly transitions between the buck, buck-boost, and boost modes, minimizing discontinuities and subharmonics in the output voltage ripple.

The MAX77348 is ideal for a system handling less than 3.5W output power from a single cell Li-Ion battery and requiring high system efficiency with precise voltage control. The MAX77348's low-noise operation makes it optimum to supply power for RF system power, ear bud applications, and other portable audio systems.

Built-in undervoltage lockout (UVLO), output active discharge, and thermal shutdown protection ensures safe operation under abnormal operating conditions.

The MAX77348 is available with a highly configurable I^2C serial interface. The device is available in 16-bump, 1.77mm x 2.01mm, 0.4mm pitch WLP package.

Applications

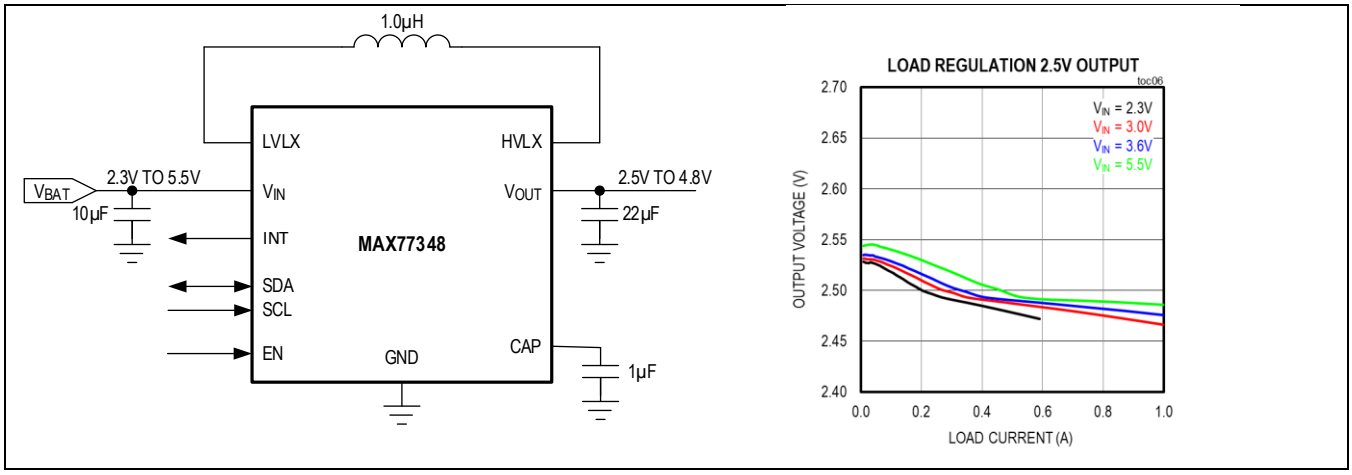
- True Wireless Stereo (TWS) Systems
- Narrow Band Internet of Things (NB IoT)
- Portable Audio/Wireless Systems

Benefits and Features

- Input Voltage Range: 2.3V to 5.5V
- Output Voltage Range: 2.5V to 4.8V
- Ultra-Low, 3.5µA (typ) Quiescent Current
- Dynamic Voltage Scaling (DVS)
- Optimized Load Regulation Performance
- Power Good Interrupt
- Output Active Discharge
- Low, Continuous Noise Profile
  - Eliminates Discontinuities Over Operating Range
  - Eliminates Need for Post-Filtering Low Dropout (LDO) in Noise Sensitive Applications
- Protection Features
  - Undervoltage Lockout (UVLO)
  - Thermal Shutdown
  - 6.4ms Soft-Start
- I^2C Interface with Status Interrupts
  - Programmable V_{OUT}
  - Peak Current Limit Level (IPSET1/IPSET2)

***Ordering Information* appears at end of data sheet.**

Simplified Block Diagram



19-101597; Rev 0; 10/22

Absolute Maximum Ratings

IN, OUT, SDA, SCL, EN, INTb, CAP to GND ..... -0.3V to +6V

LVLX to GND ..... -0.3V to V_{IN} + 0.3V

HVLX to GND ..... -0.3V to Min. (V_{OUT} + 0.3, +6.0)V

Continuous Power Dissipation for WLP package at T_A = 70°C (Derate 17.26mW/°C above +70°C) (Note 1) 1381mW

Maximum Junction Temperature ..... +150°C

Storage Temperature Range ..... -40°C to +150°C

Soldering Temperature (Reflow) ..... +260°C

Note 1: Package thermal measurement is based on JESD-51 series.

Note 2: Thermal Parameters are based on FR-4, 4-layer board.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Recommended Operating Conditions

Operating Junction Temperature ..... -40°C to +125°C

Input Voltage Range ..... 2.3V to 5.5V

Output Voltage Range ..... 2.5V to 4.8V

Electrical Characteristics

(Typicals are at $T_J \approx T_A$ = +25°C, V_{SYS} = +3.6V unless otherwise specified. Limits are 100% tested at T_J = +25°C. Limits over the operating temperature range (T_J = -40°C to +125°C) and relevant supply voltage range are guaranteed by design and characterization). (Note 1))

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
GLOBAL INPUT SUPPLY							
Operating Voltage Range	V_{IN}			2.3		5.5	V
Input UVLO Rising Threshold	V_{UVLO_RISING}				2.19		V
Input UVLO Falling Threshold	$V_{UVLO\_FALLING}$				2.10		V
Shutdown Supply Current	I_{SHDN}	I^2C Controlled			0.3		µA
Input Quiescent Current	I_Q	No load, V_{OUT} = 5V, V_{IN} = 3.7V	V_{CAP} forced to V_{IN}, T_J up to 85°C		3.5	5.0	µA
	I_{Q_FAST}	No load, V_{OUT} = 5V, V_{IN} = 3.7V	EN = High		35		
Maximum Output Operative Power (Note 3)	P_{MAX}	Integrator enabled, V_{IN} > 2.7V, V_{OUT} ≥ 3.2V	FETSCALE = 0, L = 1µH, C_{OUT_EFF} = 8µF	3.5			W
Maximum Output Operative Power (Note 5)	P_{MAX}	Integrator enabled, V_{IN} > 2.7V, V_{OUT} ≥ 3.2V	FETSCALE = 1, L = 2.2µH, C_{OUT_EFF} = 4µF	1.75			W
		Integrator disabled, V_{IN} > 3.2V (Note 4), V_{OUT} ≥ 3.2V	FETSCALE = 0, L = 1µH, C_{OUT_EFF} = 8µF	3.2			
			FETSCALE = 1, L = 2.2µH, C_{OUT_EFF} = 4µF	1.75			
Output Voltage Program Range	V_{OUT}	50mV step resolution		2.5		4.8	V
Average Output Voltage Accuracy	ACC_OUT	I_{OUT} = 1mA, C_{OUT_EFF} = 8µF		-2.4		+2.4	%
Output UVLO Falling threshold	$V_{OUT\_UVLO\_FALLING}$				1.87		V
Output UVLO Rising threshold	$V_{OUT\_UVLO\_RISING}$				1.96		V
Line Regulation Error	V_{LINE_REG}			-1.0		+1.0	%/V
Load Regulation Error	V_{LOAD_REG}	Integrator enabled, V_{IN} = 2.7V, V_{OUT} = 3.3V, FETSCALE = 0, P_{OUT} = 3.5W			-1.0		%

(Typicals are at $T_J \approx T_A$ = +25°C, V_{SYS} = +3.6V unless otherwise specified. Limits are 100% tested at T_J = +25°C. Limits over the operating temperature range (T_J = -40°C to +125°C) and relevant supply voltage range are guaranteed by design and characterization). (Note 1))

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
		Integrator disabled, V_{IN} = 3.7V, V_{OUT} = 5V, P_{OUT} = 1.5W, FETSCALE = 1, C_{OUT} = 4µF, L = 2.2µH		-3.2		
Line Transient Response	V_{LINE_TRAN}	V_{OUT} = 3.4V, V_{IN} from 3.4V to 2.9V, 1µs fall time, I_{LOAD} = 750mA, INTEGEN = 1, SWOFRCIN = 0		0		mV
Load Transient Response	V_{LOAD_TRAN}	V_{OUT} = 5V, V_{IN} = 3.7V, I_{LOAD} = 10µA to 700mA, INTEGEN = 1		-150		mV
Input Supply Current During Start-up	I_{IN_STUP}	V_{IN} = 3.6V, V_{OUT} = 5V, I_{LOAD} = 0		1		mA/C_{OUT} (µF)
Maximum Output Power During Start-up (Note 3)	P_{MAX_STUP}	FETSCALE = 0	400	600		mW
		FETSCALE = 1	200	300		
Soft-start Time	t_{SS}	Time from V_{OUT} = 0V to final value		6.4		ms
Start-up Time	$t_{STARTUP}$	Time from EN = 1 to V_{OUT} in regulation, EN = HIGH			13	ms
Active Discharge Current	I_{ACTD}			20		mA
Passive Discharge Resistance	R_{PSVD}			1.2		kΩ
DIGITAL						
SDA, SCL, INTb, EN Input Leakage Current	I_{LK}	T_J = +25˚C	-1.0		+1.0	µA
SDA, SCL, EN Input Logic High	V_{IH}		1.4			V
SDA, SCL, EN Input Logic Low	V_{IL}				0.4	V
INTb Output Logic Low	V_{OL}	I_{OL} = 4mA			0.4	V
SCL Clock Frequency	f_{SCL}				680	kHz
Bus Free Time Between STOP and START condition	t_{BUF}		0.75			µs
START Condition (Repeated) Hold Time	t_{HD_STA}	(Note 7)	0.35			µs
Low Period of SCL Clock	t_{LOW}		0.75		1.25	µs

(Typicals are at $T_J \approx T_A$ = +25°C, V_{SYS} = +3.6V unless otherwise specified. Limits are 100% tested at T_J = +25°C. Limits over the operating temperature range (T_J = -40°C to +125°C) and relevant supply voltage range are guaranteed by design and characterization). (Note 1))

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
High Period of SCL Clock	T_{HIGH}		0.35			µs
Setup Time for a Repeated START Condition	t_{SU_STA}		0.35			µs
Data Hold Time	t_{HD_DAT}	(Note 8)			0.53	µs
Data Setup Time	t_{SU_DAT}		100			ns
Setup Time for STOP Condition	t_{SU_STO}		0.35			µs
Spike Pulse Width Suppressed by Input Filter	t_{SP}		50			ns

Note 3: All devices are 100% production tested at T_A = +25°C. Limits over the operating temperature range are guaranteed by design.

Note 4: Output power across the input operating voltage range is limited by input current. See TOC03 for details on how the power limit changes with V_{IN}.

Note 5: The parameter is not production tested and values are generated through characterization only.

Note 6: Operation down to 2.7V is supported with the integrator disabled, but stability is only guaranteed up to 1.75W output power. Beyond 1.75W, oscillation can occur unless output capacitance is increased.

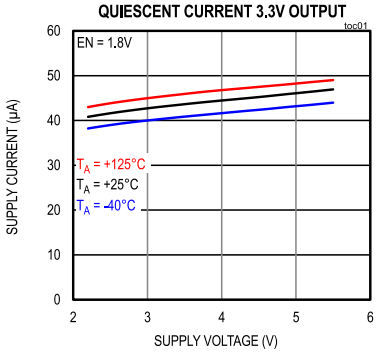
Note 7: f_{SCL} must meet the minimum clock low time plus the rise/fall times.

Note 8: The maximum t_{HD_DAT} must be met only if the device does not stretch the low period (t_{LOW}) of the SCL signal.

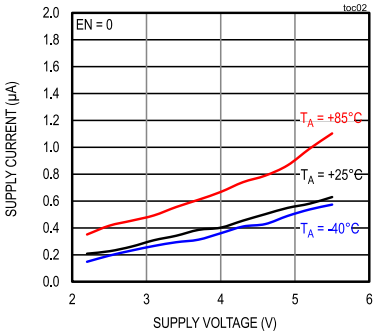
Typical Operating Characteristics

V_{IN} = +3.7V, C_{IN} = 22µF (0402 case size), C_{OUT} = 2 x 22µF (2 x 0402 case size), L = 2.2µH (2520 case size), TA = +25ºC, unless otherwise noted.

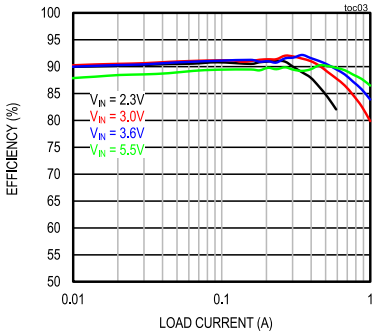
QUIESCENT CURRENT 3.3V OUTPUT



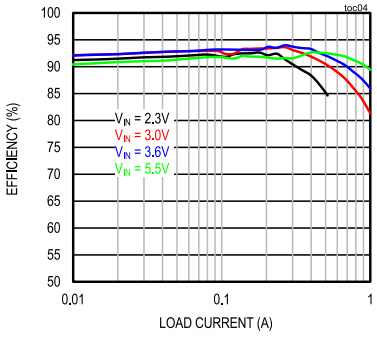
SHUTDOWN CURRENT 3.3V OUTPUT



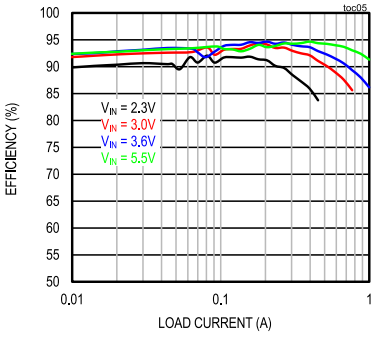
EFFICIENCY vs. LOAD 2.5V OUTPUT



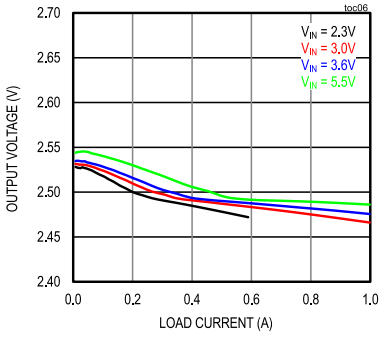
EFFICIENCY vs. LOAD 3.3V OUTPUT



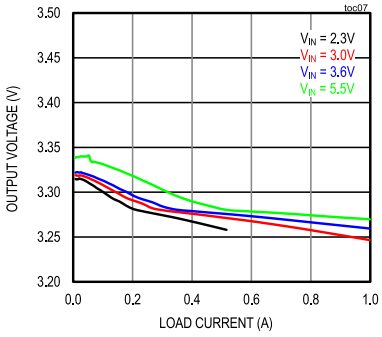
EFFICIENCY vs. LOAD 4.8V OUTPUT



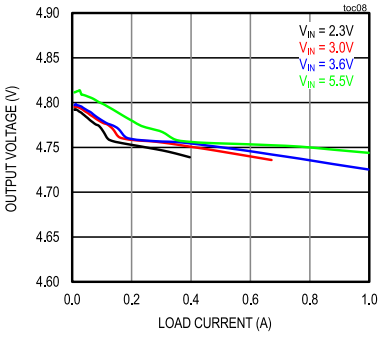
LOAD REGULATION 2.5V OUTPUT



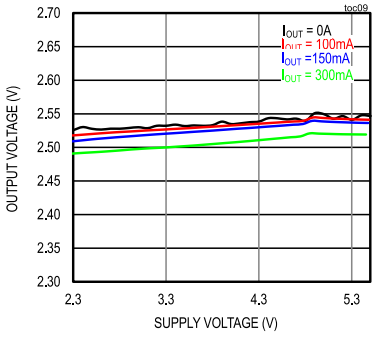
LOAD REGULATION 3.3V OUTPUT



LOAD REGULATION 4.8V OUTPUT

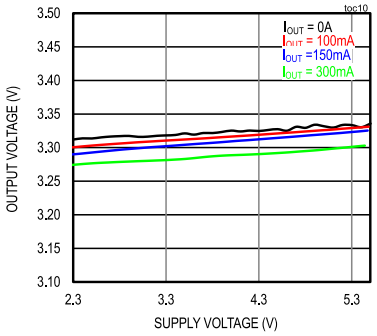


LINE REGULATION 2.5VOUT

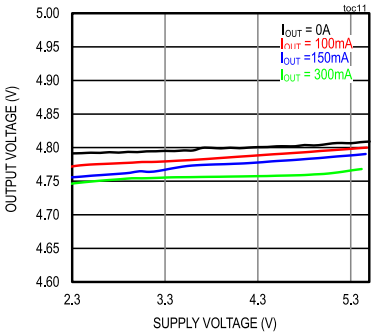


V_{IN} = +3.7V, C_{IN} = 22µF (0402 case size), C_{OUT} = 2 x 22µF (2 x 0402 case size), L = 2.2µH (2520 case size), TA = +25ºC, unless otherwise noted.

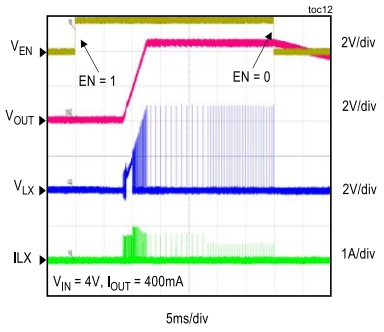
LINE REGULATION 3.3VOUT



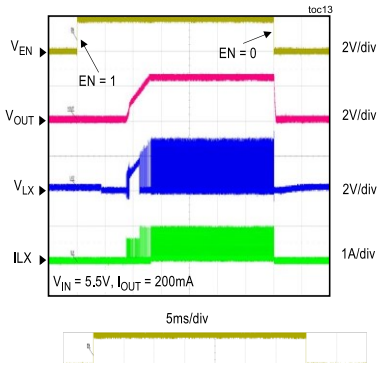
LINE REGULATION 4.8VOUT



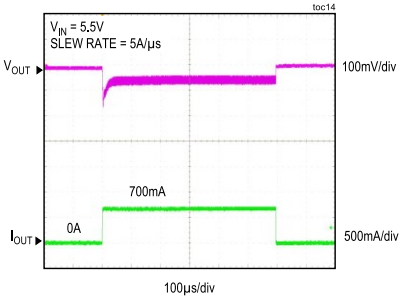
BOOST STARTUP & SHUTDOWN WAVEFORM 4.5V OUTPUT



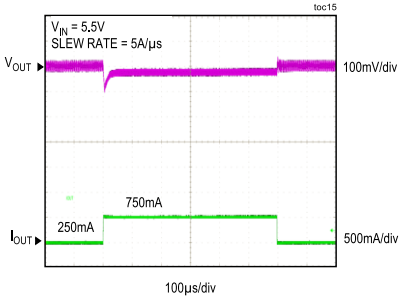
BUCK STARTUP & SHUTDOWN WAVEFORM 2.5V OUTPUT



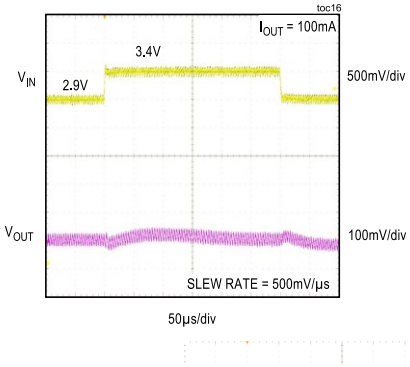
LOAD TRANSIENT RESPONSE 3.3V OUTPUT



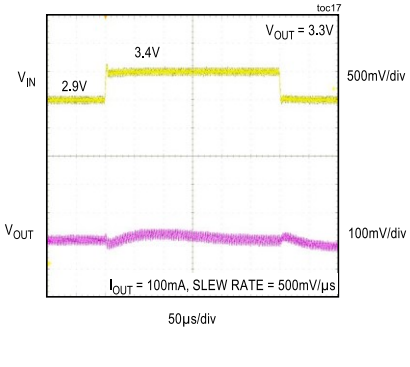
LOAD TRANSIENT RESPONSE 3.3V OUTPUT



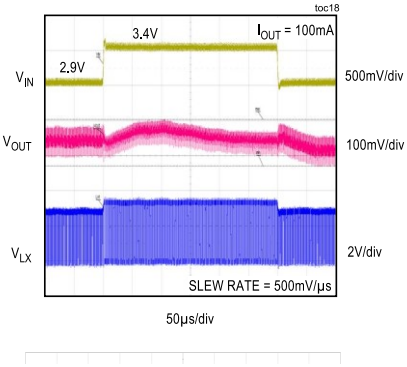
LINE TRANSIENT RESPONSE 2.5V OUTPUT



BUCK TO BOOST LINE TRANSIENT RESPONSE

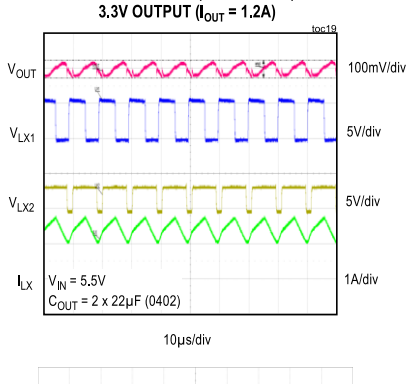


LINE TRANSIENT RESPONSE 4.8V OUTPUT

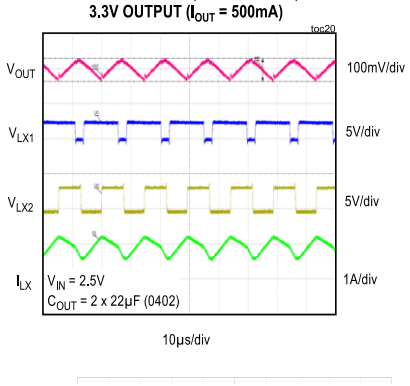


V_{IN} = +3.7V, C_{IN} = 22µF (0402 case size), C_{OUT} = 2 x 22µF (2 x 0402 case size), L = 2.2µH (2520 case size), TA = +25ºC, unless otherwise noted.

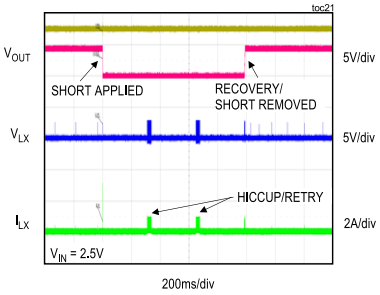
OUTPUT RIPPLE (BUCK MODE)
3.3V OUTPUT (I_{OUT} = 1.2A)



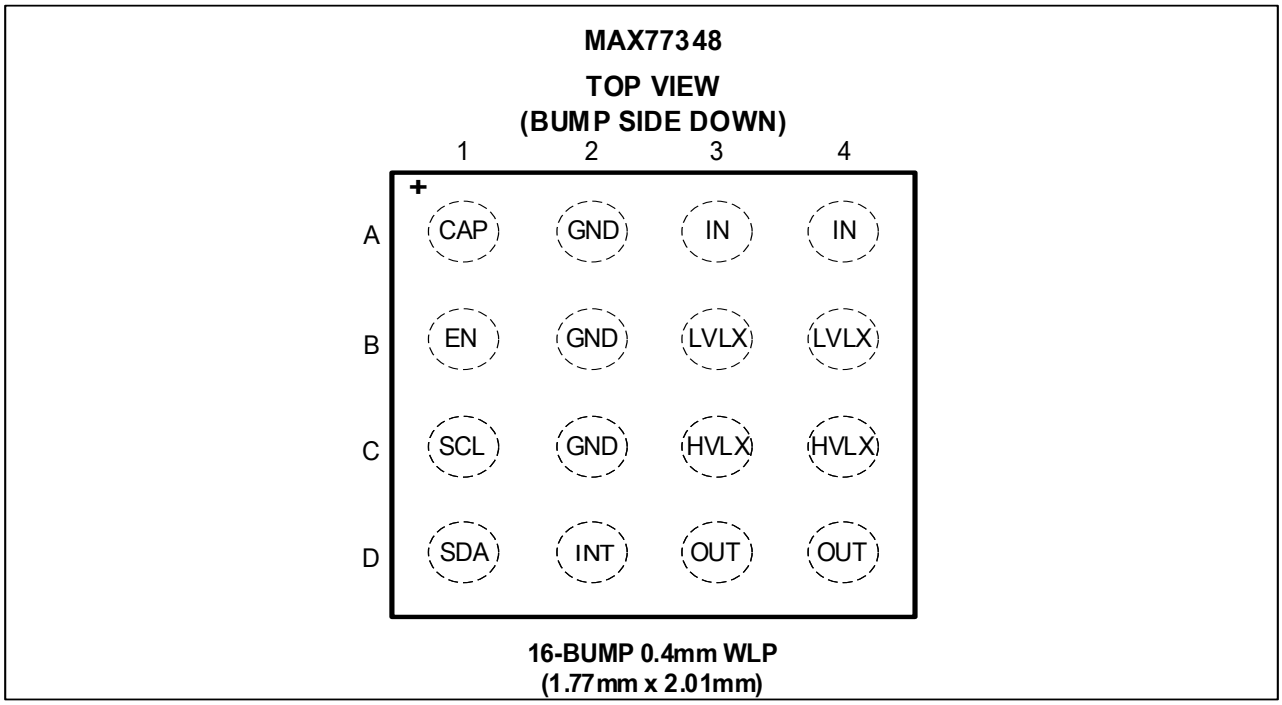
OUTPUT RIPPLE (BOOST MODE)
3.3V OUTPUT (I_{OUT} = 500mA)



SHORT-CIRCUIT HICCUP AND RECOVERY
4.5V OUTPUT



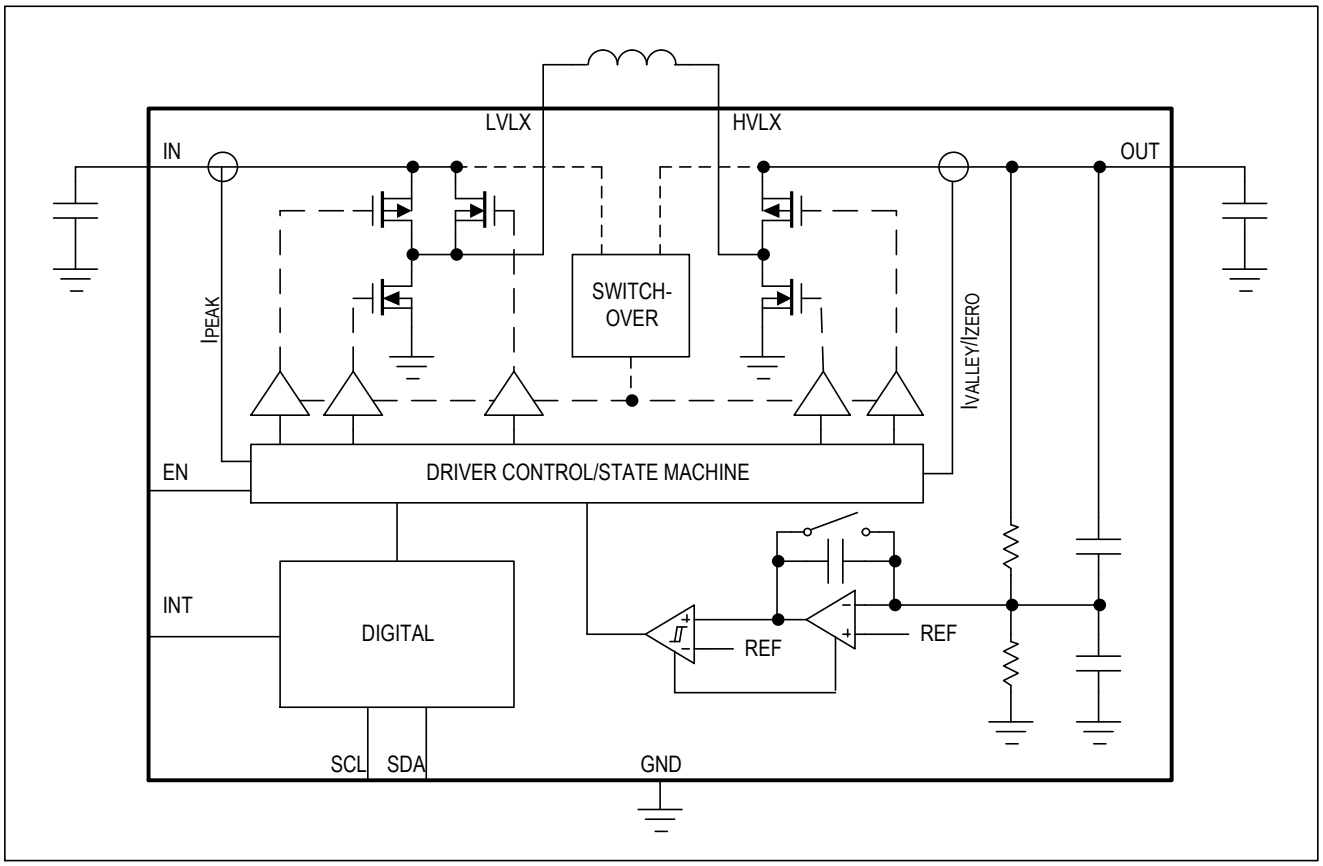
Pin Configurations



Pin Descriptions

PIN	NAME	FUNCTION	Type
A1	CAP	Bypass Capacitor Connection for Internal Supply. Connect through 470nF of capacitance to GND.	P
A2, B2, C2	GND	Ground	G
A3, A4	IN	Input Supply. Bypass to GND with effective capacitance equal to the minimum of 5µF and the value of the derating curve for a bias voltage V_{IN} placed as close to the device as possible.	P
B1	EN	Chip Enable pin	DI
B3, B4	LVLX	Switching Node. Connect to HVLX through a 1µH inductor if FETScale = 0 or a 2.2µH inductor if FETScale = 1	P
C1	SCL	I^2C Serial Clock Input. Note the EN setting. If a version is disabled by default, use an external supplied source for the I^2C interface to enable the output by I^2C command.	DI
C3, C4	HVLX	Switching Node. Connect to LVLX through a 1µH inductor if FETScale = 0 or a 2.2µH inductor if FETScale = 1	P
D1	SDA	I^2C Serial Data Input/Open-Drain Output. Note the EN setting. If a version is disabled by default, use an externally supplied source for the I^2C interface to enable the output by I^2C command.	DI/DO
D2	INTb	Interrupt Output. Open-drain, connect through pullup resistor to system logic supply.	DI
D3, D4	OUT	Buck-Boost Output. If FETScale = 0, bypass to GND with effective capacitance equal to twice the value of the derating curve for a bias voltage V_{OUT}, placed as close to the device as possible. If FETScale = 1, bypass to GND with effective capacitance equal to the value of the derating curve for a bias voltage V_{OUT}, placed as close to the device as possible.	P

Functional Diagram



Detailed Description

The MAX77348 is an ultra-low quiescent current, non-inverting buck-boost converter with 1A current capability at 3.5V intended for applications that require long run times while also demanding bursts of high current. A peak/valley current-controlled hysteretic architecture yields a fast-transient response time with minimal settling time that allows the device to handle large load transients in high peak-power applications. The device has a unique control algorithm that seamlessly transitions between buck, buck-boost, and boost operations to minimize discontinuities and subharmonic noise in the output ripple. The low, 2.3V start-up voltage is compatible with a variety of power sources, and the near-zero minimum operating voltage extracts as much energy as possible from the source. Low inductance and capacitance requirements allow for a small total-solution size and make the MAX77348 well-suited for space-constrained applications. The device has high efficiency and low noise that also makes it suitable for wireless and noise-sensitive applications such as low-power wide-area network (LPWAN) and optical sensor systems. It has an ultra-low, 3.5µA (typ) quiescent current and discontinuous conduction mode (DCM) to operate at low loads and extend run time in low average-power, battery-powered applications

Start-Up

The MAX77348 is guaranteed to start up with a minimum input voltage of 2.3V. After device start-up, an internal bootstrapping function allows the device to operate to very low input voltages limited only by the amount of current that can be drawn effectively from the input.

Switching Phases

Depending on the register settings and input-to-output voltage relationship, the buck-boost sequences through the following switching phases in a particular order to deliver charge to the output. Only two switches are on in each phase.

- Φ1: MP1 on, MP2 on. Inductor charges.
- Φ2: MP1 on, MN2 on. Inductor charges.
- Φ3: MN1 on, MP2 on. Inductor discharges.
- Φ4: MN1 on, MN2 on. Freewheeling.

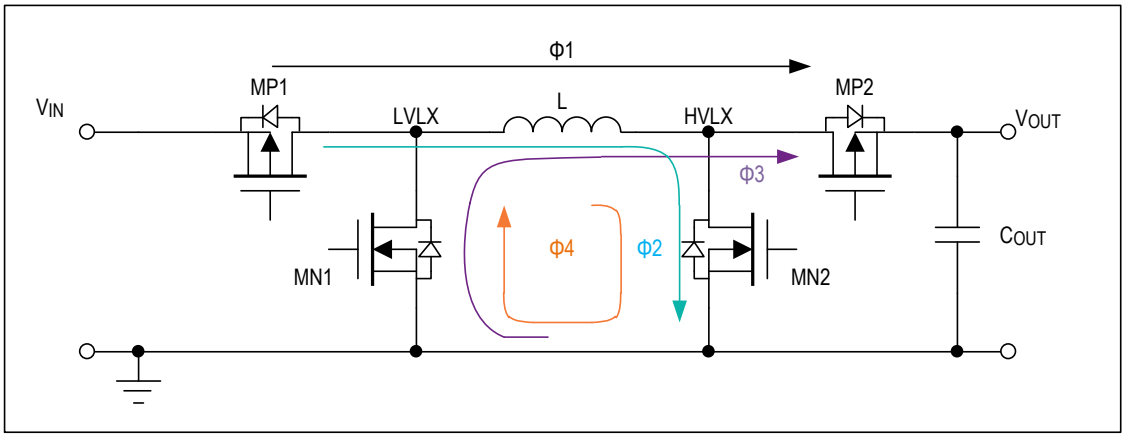


Figure 1. Buck-Boost Regulator and Switching Phases

Buck-Boost Mode

When Mode = 0 (register 0x01[2]), the regulator operates in the buck-boost mode. The inductor charges in Φ2 up to IPSet1 (register 0x03[3:0]). The buck-boost then transitions to Φ1. If $V_{IN} > V_{OUT}$, the inductor continues charging until either the current reaches IPSet1 + IPSet2 (register 0x03[7:4]) or after a 500ns delay. If $V_{IN} \leq V_{OUT}$, the buck-boost waits for the 500ns timeout to elapse or until the current drops to the valley limit. Next, the regulator enters Φ3 to discharge the inductor current to the valley limit. When the inductor current reaches the valley-current crossing threshold or falls below 0, the regulator freewheels in Φ4 until the next charge phase. When operating in continuous conduction mode (CCM), the buck-boost enters Φ4 for approximately 30ns if ZCCMPDIS = 1 (register 0x01[4]). The buck-boost skips Φ4 when operating in CCM and ZCCMPDIS = 0. The valley behavior is determined by ZCCMPDIS. *Figure 2* shows the inductor current in buck-boost mode.

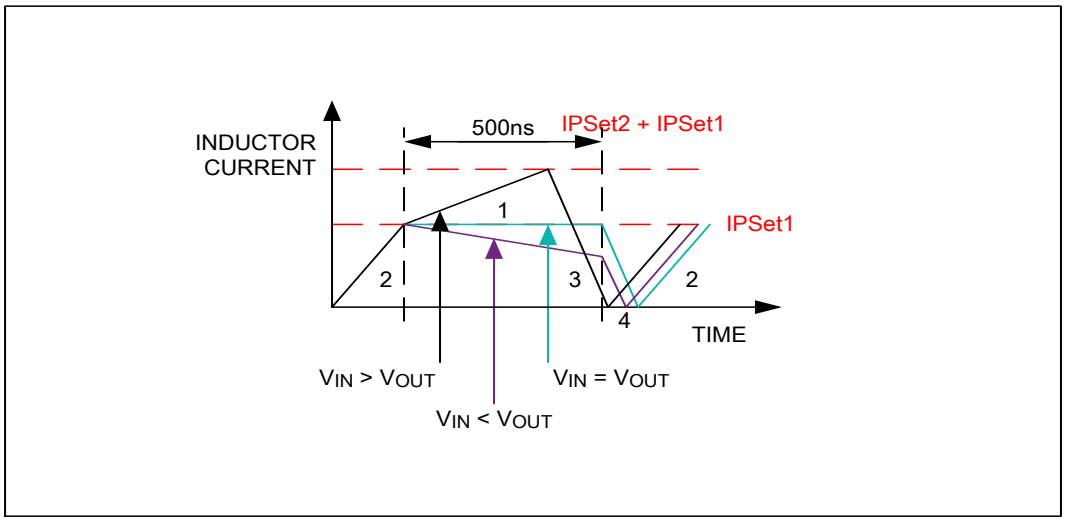


Figure 2. Inductor Current in Buck-Boost Mode

Buck-Only Mode

To maximize efficiency when V_{IN} > V_{OUT}, the buck-boost regulator has a buck-only mode. When Mode = 1, the regulator behaves as a synchronously rectified buck regulator. If the device is set to buck-only mode, the regulator never enters Φ2. Instead, the inductor is always charged in Φ1. The inductor charges until its current reaches IPSet1 or the 500ns timeout elapses. The regulator then transitions to Φ3 to provide a path to deliver the inductor current to the output. *Figure 3* shows the inductor current in buck-only mode.

Buck-only mode reduces switching losses present in the buck-boost mode. Use the buck-only mode when V_{OUT} is always less than V_{IN}.

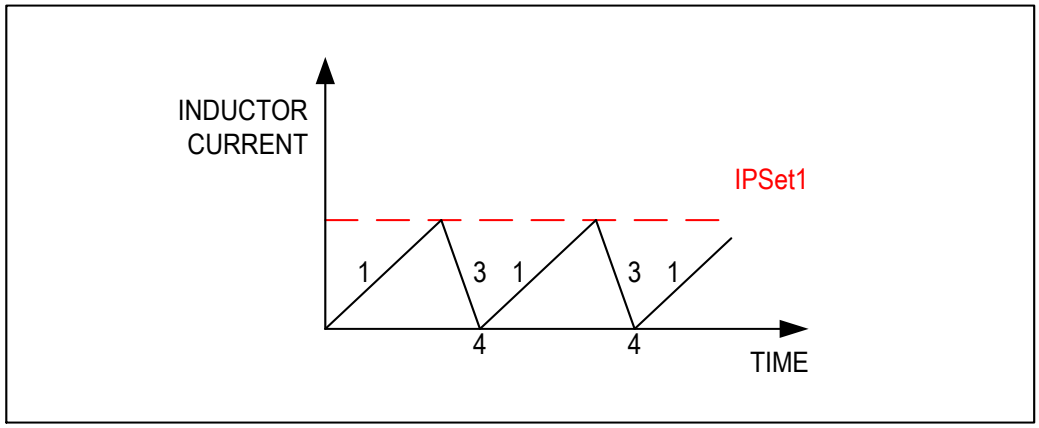


Figure 3. Inductor Current in Buck-Only Mode

Inductor Peak and Valley Current Limit

The buck-boost regulator monitors the maximum and minimum values of the inductor current. If IPAdptDis = 1 (register 0x04[1]), the peak currents are fixed to the values in IPAdptDis (register 0x03) and the valley current is fixed to 0mA. If AdptDis = 0, the peak and valley currents are allowed to change based on load requirements.

Peak currents are set in the CFG2 register. IPSet1 controls the peak current when V_{IN} < V_{OUT} and begins the timeout period for Φ1. IPSet2 sets a secondary current limit in buck-boost mode when V_{IN} > V_{OUT}. The total inductor current limit when V_{IN} > V_{OUT} is IPSet1 + IPSet2. The buck-boost regulator transitions from Φ1 to Φ3 if the inductor current reaches IPSet1 + IPSet2 or if the 500ns timeout has elapsed. Minimizing the difference between IPSet1 and IPSet2 reduces the output ripple but decreases efficiency. Care must be taken to optimize the peak current settings to keep a low output ripple while maximizing efficiency. *Figure 4* present the safe operating area of IPSet2 with respect to IPSet1. Selecting values outside of the limits shown in *Figure 4* can cause unwanted behavior. *Figure 5* is the graphical guide to select combinations of IPSet1 and IPSet2 to balance efficiency and voltage ripple for specific VSet values.

To control inrush current during start-up, the MAX77348 forces discontinuous conduction mode during start-up (valley current is always 0) and overrides the peak current settings with IP1SS and IP2SS. Once the output reaches its final voltage, continuous conduction mode is allowed, and the IPSet1 and IPSet2 settings are restored.

The MAX77348 behavior when IPAdptDis = 0 can be further defined with a zero current comparator. The device transitions to Φ4 when its control loop detects a zero current crossing.

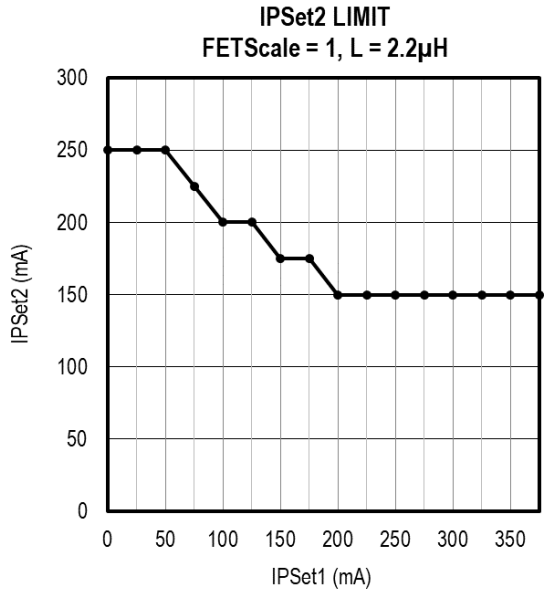


Figure 4. Minimum IPSet2 Limit for a Given IPSet1 Setting for FETScale = 1 (FETScale Setting)

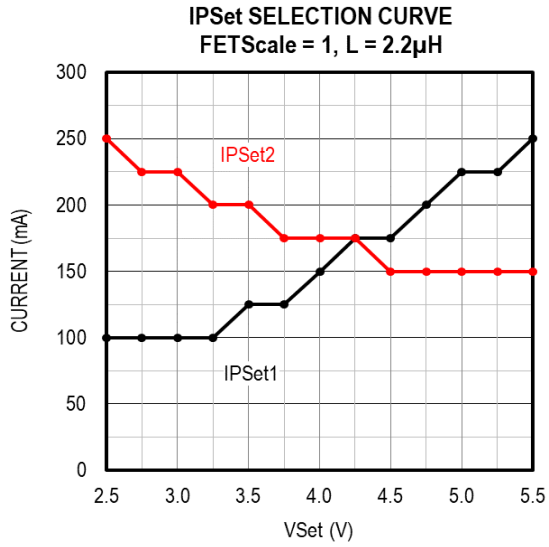


Figure 5. Recommended IPSet1 and IPSet2 Settings for FETScale = 1 (FETScale Setting)

When ZCCmpDis = 1 (register 0x01[4]), the zero-crossing comparator is disabled, and the buck-boost operates with only peak and valley current limits. In this configuration, the valley current limit acts as the zero-crossing limit. In DCM, the valley limit is 0mA and is a true zero current crossing. In CCM, the peak and valley limits are automatically adjusted by the adaptive current control, so the effective zero current point might be larger than 0mA. This causes the MAX77348 to briefly enter $\Phi 4$ each time the inductor current reaches the valley current threshold before transitioning to an inductor-charging phase. Setting ZCCmpDis = 0 enables the zero current comparator and the buck-boost operates with peak, valley, and zero crossing current limits. While the adaptive current loop adjusts the peak and valley currents, the zero crossing limit is fixed at 0mA. In DCM, the regulator functions similarly to when ZCCmpDis = 1. However, in CCM, the valley current is greater than the zero crossing current, so the regulator bypasses $\Phi 4$ and directly enters an inductor-charging phase when the inductor current reaches the valley current threshold.

Disabling the zero current crossing comparator reduces the buck-boost output ripple. Enabling the comparator improves efficiency in CCM by removing the Φ4 stage in CCM that is otherwise present when ZCCmpDis = 1.

Integrator Control Loop Disable

The MAX77348 contains an integrator in its control loop for normal operation. This integrator improves the load regulation for larger loads, but increases the transient response time. For applications where the output must quickly settle to a final regulation value to prevent noise injection during sensitive measurements (such as in photoplethysmography (PPG) measurements), the integrator can be disabled so the regulator operates with a proportional-only control loop. The IntegEn bit (register 0x04[2]) enables and disables the integrator to speed response time on load transients (integrator off) or to increase the load capacity (integrator on). Note that when the integrator is disabled, output stability is only guaranteed up to the maximum output power for input voltages down to 2.5V. To operate at lower input voltages, increase the output capacitance.

Input Operating Voltage

Operating at low input voltages enables a system to extract as much energy as possible from its energy source before shutting down. After start-up and with SwoFrcIn = 0, and V_{OUT} ≥ 2.5V, the MAX77348 can operate to very low input voltages limited only by the amount of current that can be drawn effectively from the input. This allows a system to run the MAX77348 well below the minimum start-up voltage, albeit at a reduced power capability.

When the input voltage is low, the R_{ON} of the input p-channel MOSFET increases. To offset the inherent increase in resistance, an n-channel MOSFET is present in parallel with the input MOSFET. The n-channel MOSFET is only enabled when the input voltage falls below V_{UVLO_F} to reduce switching losses at higher input voltages. To provide sufficient overdrive for the n-channel device, it is necessary to keep V_{OUT} ≥ 2.5V.

Output Operating Power and Other Optimizations

The MAX77348 is a highly flexible device with many operating modes to optimize application performance. For applications settling time to a steady-state voltage during a load transient that is critical, the user benefits from a proportional-only output response (IntegEn = 0, disabled), which trades an increased steady-state load regulation error for speed of settling. On the other hand, some applications are not as sensitive to response time, but benefit from the lower steady-state load regulation error provided when the integrator is enabled (IntegEn = 1, enabled).

The efficiency can also be optimized by selecting the FETScale setting according to which the load region should be the focus for efficiency. If the application should primarily be optimized for light-load efficiency, the FETScale = 1 (enabled) setting is preferable and vice-versa. Note that the improvement in efficiency at light loads with FETScale = 1 comes with the tradeoff of lower maximum output power, which should be a consideration when configuring the setting. A comparison of performances for each setting can be found in the *Typical Operating Characteristics* section.

Finally, the MAX77348 features an internal switchover circuit (configured by SwoFrcIN), which manages the supply from which the internal circuitry of the buck-boost is driven. For applications where quiescent current is important and the primary operating mode is to boost the output, the switchover should be forced to the input (SwoFrcIN = 1). This is because the quiescent current when SwoFrcIN = 0 is drawn from the output, meaning that the input current is increased by the boost ratio and the efficiency of the conversion. However, in cases where a low input operating voltage must be supported, the SwoFrcIN = 0 setting allows the input voltage to drop much lower since the output voltage can be used to enhance the switching FETs of the buck-boost, keeping the on-resistance low. Note that when SwoFrcIN = 1, the buck-boost output automatically shuts down when V_{IN} falls below V_{UVLO_F} (2.10V typ). Instead, when SwoFrcIN = 0, the output continues to run even when V_{IN} falls very low and is only disabled when the output voltage falls below $V_{OUT\_UVLO\_F}$ or when the user disables the device. In this operating mode, the output power capabilities begin to decrease as the input voltage falls. To indicate that the input voltage has fallen to a critical level, the device generates an 'In UVLO' status and interrupt for the system, which means that V_{IN} has dropped below V_{UVLO_F} and the source might be in a critical state. A comparison of performances for each setting can be found in the *Typical Operating Characteristics* section.

For each combination of the above settings, there are tradeoffs to consider.

Device Control

The MAX77348 enables system flexibility by providing an interface between the device and a host microcontroller. Different parameters of the regulator, such as output voltage, inductor peak current levels, FET scaling, etc., can be optimized in real time for any application. While default values are programmed by the factory, new values can be set in

the I^2C registers. The device with I^2C control takes special care to observe the default setting of EN. Versions with EN disabled by default need to have another power supply that allows the system to wake the buck-boost by I^2C command.

The full configuration settings and status information provided through this interface are detailed in the register descriptions. The slave address information of MAX77348 can be found in the *Applications Information* section.

Thermal Shutdown

The IC contains an internal thermal protection circuit that monitors die temperature. The IC enters thermal shutdown when the junction temperature (T_J) exceeds the thermal shutdown rising threshold (135ºC typical). The IC exits thermal shutdown and starts up automatically when the thermal temperature falls below the thermal shutdown falling threshold (120ºC typical). Note that toggling EN is not required for the IC to start-up once the device exits thermal shutdown.

Dynamic Voltage Scaling (DVS)

The output voltage of MAX77348 can be changed at any point while the device is enabled without restarting the device. This feature is known as dynamic voltage scaling (DVS). DVS enables systems to operate at different voltage rails when the voltage or power requirements of the system change in different operating modes. By decreasing the voltage to the minimum value required by an operating mode, the overall system efficiency increases. The output voltage is set in VSet[5:0] (register 0x02[5:0]).

Table 1. Characteristics and Device Settings

CHARACTERISTICS					DEVICE SETTINGS		
MAX. OUTPUT POWER (V_{IN}, V_{OUT} ≥ 3.2V) (W)	QUIESCENT CURRENT	OPTIMIZED FOR: STEADY-STATE LOAD REGULATION ERROR OR LOAD TRANSIENT SETTLING TIME	EFFICIENCY OPTIMIZED CURRENT RANGE	INPUT OPERATING VOLTAGE < $V_{UVLO\_FALLING}$	FETSCALE	INTEGEN	SWOFRCIN
3.2	INCREASED IN BOOST MODE	SETTLING TIME	HIGH	YES	0	0	0
3.2	LOWEST	SETTLING TIME	HIGH	NO	0	0	1
3.5	INCREASED IN BOOST MODE	LOAD REGULATION	HIGH	YES	0	1	0
3.5	LOWEST	LOAD REGULATION	HIGH	NO	0	1	1
1.75	INCREASED IN BOOST MODE	SETTLING TIME	LOW/MEDIUM	YES	1	0	0
1.75	LOWEST	SETTLING TIME	LOW/MEDIUM	NO	1	0	1
1.75	INCREASED IN BOOST MODE	LOAD REGULATION	LOW/MEDIUM	YES	1	1	0
1.75	LOWEST	LOAD REGULATION	LOW/MEDIUM	NO	1	1	1

Applications Information

Input and Output Capacitors

The MAX77348 is designed to be compatible with small case-size ceramic capacitors. As such, the device has low-input and low-output capacitance requirements to accommodate the steep voltage derating of 0603 and 0402 (imperial) capacitors. The sample derating curve in *Figure 6* presents the minimum capacitance required at IN and OUT. To ensure stability and low noise, the capacitance on IN should be the minimum of 5µF and the value of *Figure 6* at the lowest expected V_{IN}. The capacitance on OUT should be equal to the value of *Figure 6* at the highest expected V_{OUT} for FETScale = 1 and twice that value for FETScale = 0.

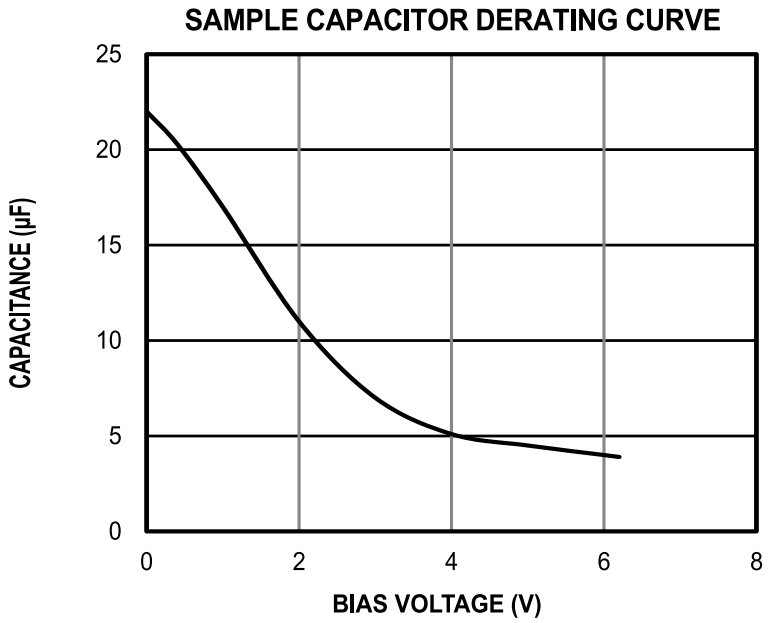


Figure 6. Capacitor Derating for Input Output Capacitance

Selecting the Inductor

Inductor selection for the MAX77348 should be optimized for the intended application. A 2.2µH inductor value is required when FET scaling is enabled (FETScale = 1), while 1µH is required when FET scaling is disabled (FETScale = 0). Aside from the inductor value physical size, DC resistance (DCR), maximum average current, and saturation current are the primary factors to consider. The maximum average inductor current is obtained using the following equation:

$$I_{L\_MAX} = \frac{V_{OUT\_MAX} \times I_{OUT\_MAX}}{\eta \times V_{IN\_MIN}}$$

where,

V_{OUT_MAX} = Maximum expected operating voltage,

I_{OUT_MAX} = Maximum expected output current,

V_{IN_MIN} = Minimum expected operating input voltage,

η = Expected worst-case efficiency in the minimum input voltage and maximum output power case (see the *Typical Operating* Characteristics to estimate efficiency).

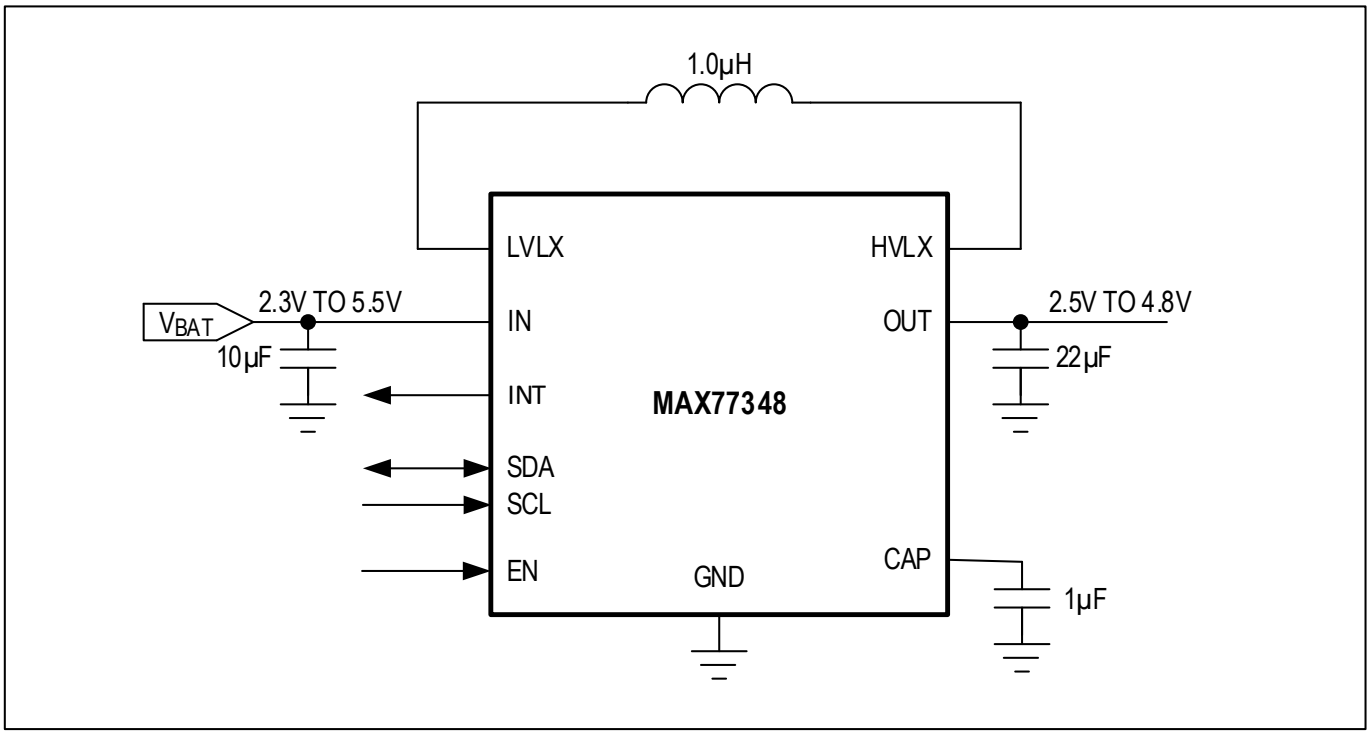
The average inductor current calculated above dictates the required maximum average current for temperature rise on the inductor. To determine the required inductor saturation current, calculate the peak current.

The peak current for this converter can be calculated as:

$I_{L\_PEAK} = I_{L\_MAX}$ + (1.1 x IPSet1)

where, IPSet1 is the peak current setting described in register 0x03. When selecting an inductor, one primary factor in achieving high efficiency is the DCR of the inductor. For maximum efficiency, select an inductor with the lowest DCR possible in the required package size. Another factor to consider is magnetic losses. Generally, magnetic losses are lower in inductors with larger physical size and/or higher saturation current ratings. In most cases, avoid ferrite inductors as they tend to exhibit poor AC characteristics, especially in the discontinuous conduction mode (DCM).

Typical Application Circuit



I²C Interface

The MAX77348 contains an I²C-compatible interface for data communication with a host controller (SCL and SDA). The MAX77348 can support I²C frequencies from 0kHz to 680kHz. SCL and SDA require pullup resistors connected to a positive supply.

Slave Address

The MAX77348 supports three different 7-bit slave addresses through factory setting: 0b1101000 (0x68) plus the Read/Write bit, 0b1101100 (0x6C) plus the Read/Write bit, or 0b1101110 (0x6E) plus the Read/Write bit. The address is the first byte of information sent to the MAX77348 after the START condition.

START, STOP, and REPEATED START Conditions

When writing to the MAX77348 using I²C, the master sends a START condition (S) followed by the MAX77348 I²C write address. After the address, the master sends the register address of the register to be programmed. The master then ends communication by issuing a STOP condition (P) to relinquish control of the bus, or a REPEATED START condition (Sr) to communicate to another I²C slave. See *Figure 7*.

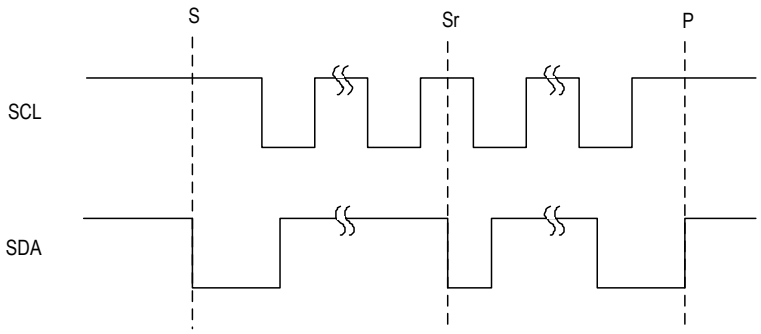


Figure 7. I²C START, STOP, and REPEATED START Conditions

Bit Transfer

One data bit is transferred on the rising edge of each SCL clock cycle. The data on SDA must remain stable during the high period of the SCL clock pulse. Changes in SDA while SCL is high and stable are considered control signals (see the Start, Stop, and Repeated Start Condition section). Both SDA and SCL remain high when the bus is not active.

Single-Byte Write

In this operation, the master sends an address and two data bytes to the slave device (*Figure 8*). The following procedure describes the single byte write operation:

- The master sends a START condition.
- The master sends the 7-bit slave address plus a write bit (low).
- The addressed slave asserts an ACK on the data line.
- The master sends the 8-bit register address.
- The slave asserts an ACK on the data line only if the address is valid (NACK if not).
- The master sends 8 data bits.
- The slave asserts an ACK on the data line.
- The master generates a STOP condition.

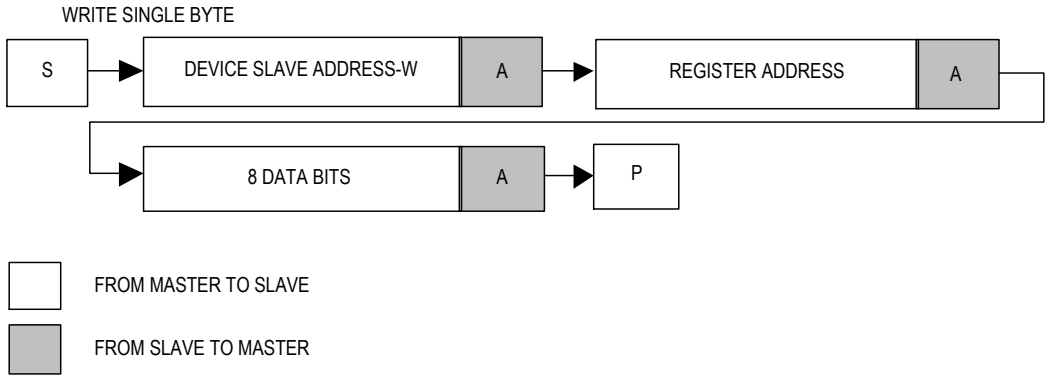


Figure 8. Write Byte Sequence

Burst Write

In this operation, the master sends an address and multiple data bytes to the slave device (*Figure 9*). The slave device automatically increments the register address after each data byte is sent, unless the register being accessed is 0x00, in which case the register address remains the same. The following procedure describes the burst write operation:

- The master sends a START condition.
- The master sends the 7-bit slave address plus a write bit (low).
- The addressed slave asserts an ACK on the data line.
- The master sends the 8-bit register address.
- The slave asserts an ACK on the data line only if the address is valid (NACK if not).
- The master sends 8 data bits.
- The slave asserts an ACK on the data line.
- Repeat 6 and 7 N-1 times.
- The master generates a STOP condition.

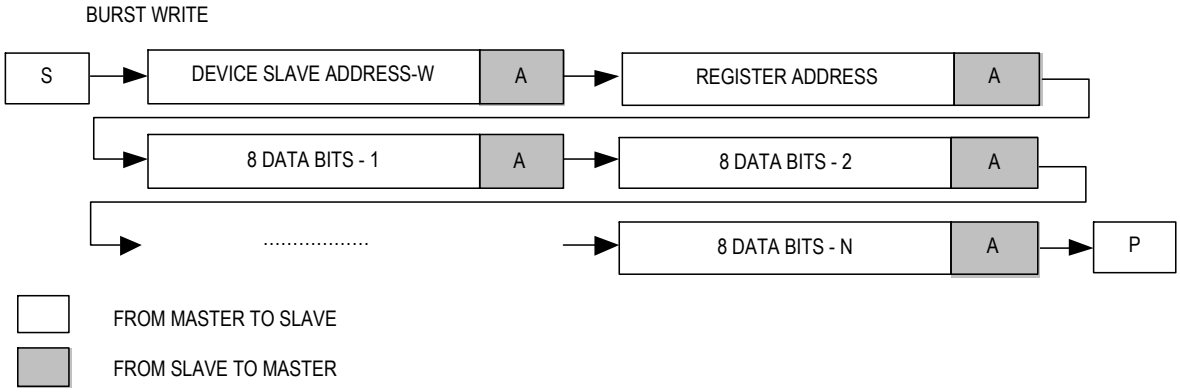


Figure 9. Burst Write Sequence

Single Byte Read

In this operation, the master sends an address plus two data bytes and receives one data byte from the slave device (*Figure 10*). The following procedure describes the single byte read operation:

- The master sends a START condition.
- The master sends the 7-bit slave address plus a write bit (low).
- The addressed slave asserts an ACK on the data line.
- The master sends the 8-bit register address.
- The slave asserts an ACK on the data line only if the address is valid (NACK if not).
- The master sends a REPEATED START condition.
- The master sends the 7-bit slave address plus a read bit (high).
- The addressed slave asserts an ACK on the data line.
- The slave sends 8 data bits.
- The master asserts a NACK on the data line.
- The master generates a STOP condition.

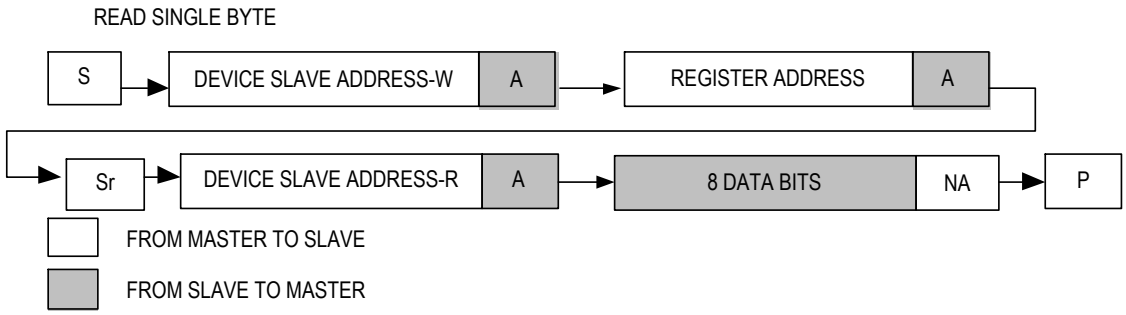


Figure 10. Read Byte Sequence

Burst Read

In this operation, the master sends an address plus two data bytes and receives multiple data bytes from the slave device (*Figure 11*). The following procedure describes the burst byte read operation:

- The master sends a START condition.

- The master sends the 7-bit slave address plus a write bit (low).
- The addressed slave asserts an ACK on the data line.
- The master sends the 8-bit register address.
- The slave asserts an ACK on the data line only if the address is valid (NACK if not).
- The master sends a REPEATED START condition.
- The master sends the 7-bit slave address plus a read bit (high).
- The slave asserts an ACK on the data line.
- The slave sends 8 data bits.
- The master asserts an ACK on the data line.
- Repeat 9 and 10 N-2 times.
- The slave sends the last 8 data bits.
- The master asserts a NACK on the data line.
- The master generates a STOP condition.

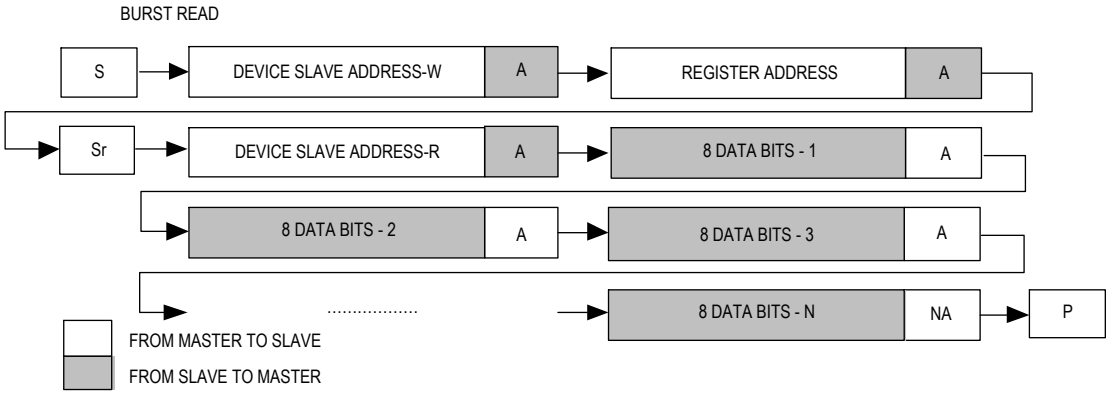


Figure 11. Burst Read Sequence

Acknowledge Bits

Data transfers are acknowledged with an acknowledge bit (ACK) or a not-acknowledge bit (NACK). Both the master and the MAX77348 generate ACK bits. To generate an ACK, pull SDA low before the rising edge of the ninth clock pulse and hold it low during the high period of the ninth clock pulse (*Figure 12*). To generate a NACK, leave SDA high before the rising edge of the ninth clock pulse and leave it high for the duration of the ninth clock pulse. Monitoring for NACK bits detects unsuccessful data transfers.

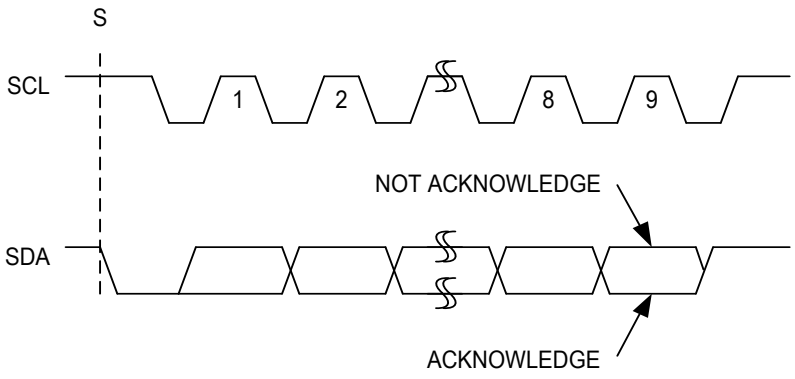


Figure 12. Acknowledge Bits

Clock Stretching

In general, the clock signal generation for I^2C bus is the responsibility of the master device. I^2C specification allows slow slave devices to alter the clock signal by holding down the clock line. The process in which a slave device holds down the clock line is called clock stretching. MAX77348 does not use any form of clock stretching to hold down the clock line.

General Call Address

MAX77348 does not implement I^2C specification 'General Call Address'. If MAX77348 sees 'General Call Address (00000000b)', it does not issue an ACKNOWLEDGE (A).

Register Map

MAX77348

ADDRESS	NAME	MSB							LSB
Global Configuration									
0x00	CHIPID[7:0]	BUCK_I[7:0]							
0x01	CFG0[7:0]	EN	RAMPEN	FAST	ZCCMPDIS	LOWEMI	MODE	ACTDSC	PSVDSC
0x02	CFG1[7:0]	FHIGHSH[1:0]		VSET[5:0]					
0x03	CFG2[7:0]	IPSET2[3:0]				IPSET1[3:0]			
0x04	CFG3[7:0]	RESERVED	PASTHRMODE	SWOFRCIN	RESERVED	RESERVED	INTEGEN	IPADPTDIS	FETSCALE
0x05	STATUS[7:0]	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	OUTGOOD	INUVLO
0x06	INT[7:0]	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	OUTGOODINT	INUVLOINT
0x07	INTMSK[7:0]	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	OUTGOODINTM	INUVLOINTM
0x50	LOCKMSK[7:0]	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	BBLCK
0x51	LOCKUNLOCK[7:0]	PASSWD[7:0]							

Register Details

CHIPID (0x0)

BIT	7	6	5	4	3	2	1	0
Field	BUCK_I[7:0]							
Reset	0xCustom							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION	DECODE
BUCK_I	7:0	ChipID[7:0] indicates the version of the device in use	Option A = 0x10 Option B = 0x11 Option C = 0x12

CFG0 (0x1)

BIT	7	6	5	4	3	2	1	0
Field	EN	RAMPEN	FAST	ZCCMPDIS	LOWEMI	MODE	ACTDSC	PSVDSC
Reset	0bCustom	0b1	0bCustom	0b1	0b0	0b0	0b0	0bCustom
Access Type	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
EN	7	Output Enable	0x0 = Disable output 0x1 = Enable output Reset value: Option A, B = 0b1 Option C = 0b0
RAMPEN	6	Ramp Enable	0x0 = Output voltage setting transition is performed without intermediate steps 0x1 = Output voltage setting increases are performed with a digital ramp of 50mV every 50µs
FAST	5	Buck-boost Pre-trigger Mode Setting. Increases the quiescent current of the buck-boost to improve output regulation during load transients.	0x0 = Normal-Low Quiescent Current Operation 0x1 = Fast response mode enabled-Quiescent Current increased to 35µA (typ) Reset Value: Option A = 1 Option B = 0 Option C = 0

BITFIELD	BITS	DESCRIPTION	DECODE
ZCCMPDIS	4	Zero-Crossing Comparator Disable-Latched internally, it can only be changed when EN = 0.	0x0 = Enabled 0x1 = Disabled
LOWEMI	3	Low EMI Mode. Increases the rise/fall time of HVLX/LVLX to reduce EMI at the cost of efficiency.	0x0 = Normal Operation 0x1 = Increase rise/fall time on HVLX/LVLX by three times
MODE	2	Buck-Boost Operating Mode. Configures the regulator to operate in buck-boost or buck-only mode, latched internally, can only be changed while EN = 0.	0x0 = Buck-Boost Mode 0x1 = Buck-Only Mode
ACTDSC	1	Active Discharge Control	0x0 = Buck-Boost not actively discharged 0x1 = Buck-Boost actively discharged on shutdown
PSVDSC	0	Passive Discharge Control	0x0 = Buck-Boost not passively discharged 0x1 = Buck-Boost passively discharged on shutdown Reset Value: Option A = 0 Option B = 1 Option C = 1

CFG1 (0x2)

BIT	7	6	5	4	3	2	1	0
Field	FHIGHSH[1:0]		VSET[5:0]					
Reset	0b11		0xCustom					
Access Type	Write, Read		Write, Read					

BITFIELD	BITS	DESCRIPTION	DECODE
FHIGHSH	7:6	f_{HIGH} Thresholds. Selects the switching frequency threshold f_{HIGH}; If the buck-boost switching frequency exceeds the f_{HIGH} rising threshold, all the blocks are kept ON (I_Q is higher) until the frequency reaches the f_{HIGH} falling threshold. A small glitch on V_{OUT} can be present at the f_{HIGH} crossover.	0x0 = 25kHz Rising/6.125kHz falling 0x1 = 35kHz Rising/8.25kHz falling 0x2 = 50kHz Rising/12.5kHz falling 0x3 = 100kHz Rising/25kHz falling
VSET	5:0	Output Voltage Setting. 2.5V to 5.5V Linear scale 50mV increments.	0x00 = 2.50V 0x01 - 0x2E = 2.50V + (VSET x 0.05)V 0x2F - 0x3F = 4.8V Reset Value: Option A = 0x28

BITFIELD	BITS	DESCRIPTION	DECODE
			Option B = 0x2A Option C = 0x2A

CFG2 (0x3)

BIT	7	6	5	4	3	2	1	0
Field	IPSET2[3:0]				IPSET1[3:0]			
Reset	0xCustom				0x8			
Access Type	Write, Read				Write, Read			

BITFIELD	BITS	DESCRIPTION	DECODE
IPSET2	7:4	Norminal Maximum Peak Current Setting. See the Buck-Boost Operation section for a description of the peak current settings - 0mA (minimum t_{ON}) to 750mA, linear scale, 50mA increments for FETSCALE = 0. 0mA (minimum t_{ON}) to 375mA, linear scale, 25mA increments for FETSCALE = 1.	For FETSCALE = 0, 0x0 = 0mA (minimum t_{ON}) 0x1 - 0xF = (IPSET2 x 50)mA For FETSCALE = 1, 0x0 = 0mA (minimum t_{ON}) 0x1 - 0xF = (IPSET2 x 25)mA Reset Value: Option A, C = A Option B = 6
IPSET1	3:0	Norminal Maximum Peak Current Setting. See the Buck-Boost Operation section for a description of the peak current settings - 0mA (minimum t_{ON}) to 750mA, linear scale, 50mA increments for FETSCALE = 0. 0mA (minimum t_{ON}) to 375mA, linear scale, 25mA increments for FETSCALE = 1.	For FETSCALE = 0, 0x0 = 0mA (minimum t_{ON}) 0x1 - 0xE = (IPSET2 x 50)mA 0xF = 750mA For FETSCALE = 1, 0x0 = 0mA (minimum t_{ON}) 0x1 - 0xE = (IPSET2 x 25)mA 0xF = 375mA

CFG3 (0x4)

BIT	7	6	5	4	3	2	1	0
Field	RESERVED	PASTHRMODE	SWOFRCIN	RESERVED	RESERVED	INTEGEN	IPADPTDIS	FETSCALE
Reset	0b1	0b0	0b1	0b0	0b0	0b1	0b0	0bCustom
Access Type	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
RESERVED	7	Reserved	
PASTHRMODE	6	Pass Through Mode. Bypasses the regulator to connect V_{OUT} to V_{IN}. This can only be enabled when EN = 0.	0x0 = Pass Through Mode disabled 0x1 = Pass Through Mode enabled; Enable only when EN = 0
SWOFRCIN	5	Force Switch-Over. Controls how the device powers the internal circuitry.	0x0 = Switch-over supply forced to V_{OUT} when V_{OUT} > $V_{OUT\_UVLO\_R}$ 0x1 = Switch-over supply forced to V_{IN}.
RESERVED	4	Reserved. Returns "0."	
RESERVED	3	Reserved. Returns "0."	
INTEGEN	2	Integrator Enable. The integrator can be disabled to improve settling time on load transients at the cost of load regulation error. Latched internally, it can only be changed when EN = 0.	0x0 = Integrator disabled 0x1 = Integrator enabled
IPADPTDIS	1	Adaptive Peak/Valley Current Adjustment Disable	0x0 = Enabled 0x1 = Disabled Peak current fixed to the values set by IPSET1 and IPSET2. Valley current is fixed to 0mA; This setting is equivalent to forcing discontinuous conduction mode and greatly diminishes the output power capability of the part. Generally this is not a recommended setting.
FETSCALE	0	FET Scale. Reduces FET sizes by a factor of two. This setting can be used to optimize efficiency for lighter loads if it is acceptable to support lower maximum output power. If FETSCALE = 0, the part requires a 1µH inductor and at least twice the derated capacitance. If FETSCALE = 1the part requires a 2.2µH inductor. Latched internally, it can only be changed when EN = 0.	0x0 = FET scaling disabled 0x1 = FET scaling enabled Reset Value: Option A, C = 0 Option B = 1

STATUS (0x5)

BIT	7	6	5	4	3	2	1	0
Field	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	OUTGOOD	INUVLO
Reset	0b0	0b0	0b0	0b0	0b0	0b0	0b0	0b0
Access Type	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
RESERVED	7	Reserved. Returns "0."	
RESERVED	6	Reserved. Returns "0."	
RESERVED	5	Reserved. Returns "0."	
RESERVED	4	Reserved. Returns "0."	
RESERVED	3	Reserved. Returns "0."	
RESERVED	2	Reserved. Returns "0."	
OUTGOOD	1	Status of Output Voltage	0x0 = Output has not reached full power capability 0x1 = Output voltage is high enough to support full power capability
INUVLO	0	Status register showing whether input voltage is low enough to enable parallel input NMOS.	0x0 = V_{IN} high enough for full power operation 0x1 = Power might be limited due to low V_{IN}

INT (0x6)

BIT	7	6	5	4	3	2	1	0
Field	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	OUTGOODINT	INUVLOINT
Reset	0b0	0b0	0b0	0b0	0b0	0b0	0b0	0b0
Access Type	Read Only	Read Only	Read Only	Read Only	Read Only	Read Only	Read Only	Read Only

BITFIELD	BITS	DESCRIPTION	DECODE
RESERVED	7	Reserved. Returns "0."	
RESERVED	6	Reserved. Returns "0."	
RESERVED	5	Reserved. Returns "0."	
RESERVED	4	Reserved. Returns "0."	
RESERVED	3	Reserved. Returns "0."	
RESERVED	2	Reserved. Returns "0."	
OUTGOODINT	1	Output Voltage Good Interrrupt	0x0 = Output voltage is not reached in regulation 0x1 = Output voltage is in regulation
INUVLOINT	0	INUVLO Interrupt	0x0 = V_{IN} high enough for full power operation 0x1 = Power might be limited due to low V_{IN}

INTMSK (0x7)

BIT	7	6	5	4	3	2	1	0
Field	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	OUTGOODINTM	INUVLOINTM
Reset	0b0	0b0	0b0	0b0	0b0	0b0	0b0	0b0
Access Type	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
RESERVED	7	Reserved. Returns "0."	
RESERVED	6	Reserved. Returns "0."	
RESERVED	5	Reserved. Returns "0."	
RESERVED	4	Reserved. Returns "0."	
RESERVED	3	Reserved. Returns "0."	
RESERVED	2	Reserved. Returns "0."	
OUTGOODINTM	1	Output Voltage Good Interrrupt Mask	0x0 = Not masked 0x1 = Masked
INUVLOINTM	0	INUVLO Interrupt Mask	0x0 = Not masked 0x1 = Masked

LOCKMSK (0x50)

BIT	7	6	5	4	3	2	1	0
Field	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	BBLCK
Reset	0b0	0b0	0b0	0b0	0b0	0b0	0b0	0b1
Access Type	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
RESERVED	7	Reserved. Returns "0."	
RESERVED	6	Reserved. Returns "0."	
RESERVED	5	Reserved. Returns "0."	
RESERVED	4	Reserved. Returns "0."	
RESERVED	3	Reserved. Returns "0."	

BITFIELD	BITS	DESCRIPTION	DECODE
RESERVED	2	Reserved. Returns "0."	
RESERVED	1	Reserved. Returns "0."	
BBLCK	0	Lock Mask for Buck-Boost Registers	0x0 = Buck-Boost Registers not masked from locking/unlocking 0x1 = Buck-Boost Registers masked from locking/unlocking

LOCKUNLOCK (0x51)

BIT	7	6	5	4	3	2	1	0
Field	PASSWD[7:0]							
Reset	0xFF							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
PASSWD	7:0	Lock/Unlock Password	0xAA = BBLCK unmasked to lock the BBSTVSSET 0x55 = BBLCK unmasked to unlock the BBSTVSET

Ordering Information

Part Number	Default EN	VSet [V]	Default FETScale	I^2C Slave Address
MAX77348AEWE+T	Enable	4.50	Disabled	0x68
MAX77348BEWE+T	Enable	4.60	Enabled	0x6C

Package Information

Package Code	N161A2+1S
Outline Number	21-100516
Land Pattern Number	
Thermal Resistance, Single Layer Board:	
Junction-to-Ambient (θ_{JA})	
Junction-to-Case Thermal Resistance (θ_{JC})	
Thermal Resistance, Four Layer Board:	
Junction-to-Ambient (θ_{JA})	
Junction-to-Case Thermal Resistance (θ_{JC})	

Revision History

REVISION NUMBER	REVISION DATE	DECRIPTION	PAGES CHANGED
0	10/22	Release for market intro	—