IEEE 802.3bt-Compliant, Powered Device with Power Telemetry and Power/Current Limit

MAX5996C

General Description

The MAX5996C provides a complete interface for a powered device (PD) to comply with the IEEE® 802.3af/at/bt standard in a power-over-ethernet (PoE) system with a detection signature, classification signature, and an integrated N-channel power MOSFET switch with startup inrush current control. During the startup period, the device limits the current to 135mA and switches to a higher current limit when the power MOSFET is fully enhanced. The device features multi-event classification, intelligent MPS, and an input UVLO with wide hysteresis and deglitch time to assure glitch-free transition during power-on/off. The device can withstand a maximum voltage of 100V at the input.

The device can detect the presence of a wall adapter and allow a smooth switchover from the PoE power source to the wall adapter. The device also provides a power-good (PG) signal, two-step current limit, foldback control, and overtemperature protection.

The intelligent maintain power signature (IMPS) feature allows the device to automatically enable MPS current by detecting the port current.

The MAX5996C features a constant power/current limit for driving an external DC-DC controller. The MEC (multi-event classification) pin provides patterned signals to indicate the power level allocated from PSE to PD in seven different scenarios, and accurate real-time power telemetry reporting. The MAX5996C LLDP pin enables control of power- or current-limit configuration with an external microcontroller.

The MAX5996C is available in a 16-pin, 5mm x 5mm, TQFN power package. This device is rated over the -40°C to +125°C temperature range.

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Benefits and Features

- Accurate Power Telemetry
- Constant Power/Current Limit
- LLDP Power/Current Level Setting
- IEEE 802.3bt Compliant
- Built-in 90W Power MOSFET Switch
- Multi-Event Classification
- Multi-Event Power Level Indication
- Simplified Wall Adapter Interface
- Inrush Current Limit during Startup
- Current Limit during Normal Operation
- Overtemperature Protection
- Intelligent MPS
- 5mm x 5mm, 16-Pin TQFN

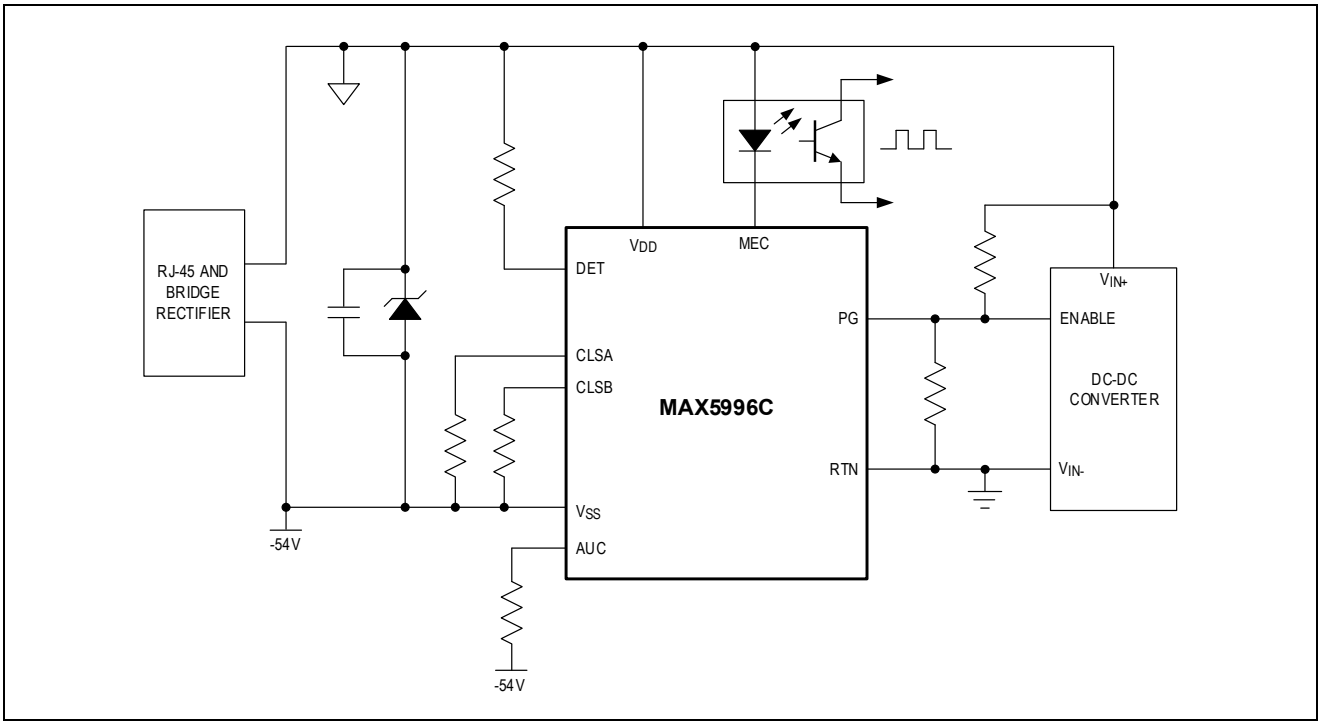
Applications

- IEEE 802.3bt Powered Devices
- VOIP Phones, IP Security Cameras
- Wireless Access Point
- Small Cell, Pico Cell
- Lighting
- Building Automation

***Ordering Information* appears at end of data sheet.**

19-101124; Rev 3; 4/25

Simplified Block Diagram



Absolute Maximum Ratings

V_{DD} to V_{SS} ..... -0.3V to +100V

RTN, WAD, MEC, PG, DET to V_{SS} ..... -0.3V to +100V

PCN to V_{SS} ..... -0.3V to +100V

TRSP, AUC, LLDP, CLSA, CLSB to V_{SS} ..... -0.3V to +6V

Maximum Current on CLSA, CLSB (100ms, max) 100mA

Continuous Power Dissipation ((T_A = +70°C) (*Note 1*) (TQFN (derate 28.6mW/°C above +70°C)) (multilayer board) 2285.7mW

Operating Temperature Range ..... -40°C to +125°C

Maximum Junction Temperature ..... +150°C

Storage Temperature Range ..... -65°C to +150°C

Lead Temperature (soldering, 10s) ..... +300°C

Soldering Temperature (reflow) ..... +260°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Package Information

16 TQFN-EP

Package Code	T1655+5
Outline Number	*21-100484*
Land Pattern Number	*90-100171*
Thermal Resistance, Four-Layer Board:	
Junction to Ambient (θ_{JA})	35°C/W
Junction to Case (θ_{JC})	2.7°C/W

For the latest package outline information and land patterns (footprints), go to www.analog.com/en/resources/packaging-quality-symbols-footprints/package-index.html. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to www.analog.com/en/resources/technical-articles/thermal-characterization-of-ic-packages.html.

Electrical Characteristics

(V_{IN} = (V_{DD} - V_{SS}) = 48V, R_{CLSA} = 619Ω, R_{CLSB} = 619Ω; RTN, WAD, PG, MEC, PCN, and LLDP are unconnected, all voltages are referenced to V_{SS}, unless otherwise noted. T_A = T_J = -40°C to +125°C, unless otherwise noted. Typical values are at T_A = +25°C. (Note 1))

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
DETECTION MODE						
Input Offset Current	I_{OFFSET}	V_{IN} = 1.4V to 10.1V (Note 2)			10	µA
Effective Differential Input Resistance	D_R	V_{IN} = 1.4V to 10.1V with 1V step, V_{DD} = RTN = WAD = PG = MEC (Note 3)	23.95	25	25.5	kΩ
CLASSIFICATION MODE						
Classification Disable Threshold	$V_{TH,CLS}$	V_{IN} rising (Note 6)	22	22.8	23.6	V
Classification Stability Time				0.2		ms
Classification Current (Note 4)	I_{CLASS}	V_{IN} = 12.5V to 20.5V, V_{DD} = RTN = WAD = PG, $R_{CLS\_}$ = 619Ω	0		3.96	mA
		V_{IN} = 12.5V to 20.5V, V_{DD} = RTN = WAD = PG, $R_{CLS\_}$ = 118Ω	9.12		11.88	
		V_{IN} = 12.5V to 20.5V, V_{DD} = RTN = WAD = PG, $R_{CLS\_}$ = 66.5Ω	17.2		19.8	
		V_{IN} = 12.5V to 20.5V, V_{DD} = RTN = WAD = PG, $R_{CLS\_}$ = 43.2Ω	26.3		29.7	
		V_{IN} = 12.5V to 20.5V, V_{DD} = RTN = WAD = PG, $R_{CLS\_}$ = 30.9Ω	36.4		43.6	
Mark Event Threshold	V_{THM}	V_{IN} falling	10.1	10.7	11.6	V
Hysteresis on Mark Event Threshold				0.82		V
Mark Event Current	I_{MARK}	V_{IN} falling to enter mark event, 5.2V < V_{IN} < 10.1V	1.0		3.5	mA
Reset Event Threshold	V_{THR}	V_{IN} falling	2.8	3.8	5.2	V
POWER MODE						
V_{IN} Supply Voltage Range					60	V
V_{IN} Supply Current	I_Q	Power MOSFET is ON and no load		1.3	1.8	mA
V_{IN} Turn-On Voltage	V_{ON}	V_{IN} rising	34.3	35.4	36.6	V
V_{IN} Turn-Off Voltage	V_{OFF}	V_{IN} falling	30			V
V_{IN} Turn-On/-Off Hysteresis	V_{HYST_UVLO}	(Note 5)		4.2		V
V_{IN} Deglitch Time	t_{OFF_DLY}	V_{IN} falling from 40V to 20V (Note 6)	30	120		µs
Mode Delay	t_{DELAY}	From PG pulled low to high when entering into power mode, V_{IN} = 48V, C_{OUT} = 47µF	90	96	102	ms
Power MOSFET On-Resistance	R_{ON_ISO}	I_{RTN} = 950mA, T_J = +25°C		0.1	0.2	Ω
		I_{RTN} = 950mA, T_J = +85°C		0.15	0.25	Ω
		I_{RTN} = 950mA, T_J = +125°C		0.2		
RTN Leakage Current	I_{RTN_LKG}	V_{RTN} = 12.5V to 30V			10	µA
OVERCURRENT LIMIT						

(V_{IN} = (V_{DD} - V_{SS}) = 48V, R_{CLSA} = 619Ω, R_{CLSB} = 619Ω; RTN, WAD, PG, MEC, PCN, and LLDP are unconnected, all voltages are referenced to V_{SS}, unless otherwise noted. T_A = T_J = -40°C to +125°C, unless otherwise noted. Typical values are at T_A = +25°C. (*Note 1*))

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Inrush Current Limit	I_{INRUSH}	During initial turn-on period, V_{RTN} - V_{VSS} = 1.5V		90	135	182	mA
Overcurrent Limit during Normal Operation (*Note 7*)	I_{MAX}	1 to 5 Event detected	After inrush completed, V_{RTN} = 1V (*Note 9*)	1800	2400	3000	mA
Overcurrent Limit in Foldback Condition	I_{MAX_FLDBK}	Both during inrush and after inrush completed V_{RTN} - V_{VSS} = 7.5V			45		mA
Foldback Threshold		V_{RTN} (*Note 8*)		6.5	7	7.5	V
WAD							
WAD Detection Threshold	$V_{WAD-REF}$	V_{WAD} rising, V_{IN} = 14V to 48V (referenced to RTN)		8	9	10	V
WAD Detection Threshold Hysteresis		V_{WAD} rising, V_{RTN} = 0V, V_{SS} unconnected			0.35		V
WAD Input Current	I_{WAD_LKG}	V_{WAD} = 10V (referenced to RTN)				3.5	µA
PG							
PG Sink Current	I_{PG}	V_{RTN} = 1.5V, V_{PG} = 0.8V, during inrush period		125	230	375	µA
PG Off-Leakage Current	I_{PG_LEAK}	V_{PG} = 60V				1	µA
MEC							
Pulse Width of START Bit for Class Indication					250		µs
Pulse Width of START Bit for Power Monitoring					900		µs
50% Pulse Width					500		µs
75% Pulse Width					750		µs
Repetitive Period					1000		µs
MEC Sink Current		V_{MEC} = 3.5V (referenced to RTN), V_{SS} disconnected		0.9	1.5	2.35	mA
MEC Off-Leakage Current		V_{MEC} = 48V				1	µA
MEC Power-Limiting Alert Threshold					P_{MAX} – 1.8		W
MEC Power-Limiting Alert Hysteresis					1.8		W
MEC Current-Limiting Alert Threshold					I_{LIM} – 60		mA
MEC Current-Limiting Alert Hysteresis					60		mA
MEC Power-/Current-Limiting Alert Time	t_{ALERT}	MEC pulled to V_{SS}			2		ms
MEC Power-/Current-Limiting Alert Period	t_{ALERT_P}				64		ms
AUC							
AUC Pull-up Current	I_{AUC_PUP}			8.5	9	9.5	µA
AUC Voltage Threshold	V_{AUC1}			0.47	0.5	0.53	V
	V_{AUC2}			1.73	1.8	1.87	

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PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
	V_{AUC3}		4.31	4.4	4.49	
MAINTAIN POWER SIGNATURE						
PoE MPS Current Rising Threshold	I_{MPS_RISE}			28.7		mA
PoE MPS Current Falling Threshold	I_{MPS_FALL}			24		mA
PoE MPS Current Threshold Hysteresis	I_{MPS_HYS}			4.3		mA
PoE MPS Time High	t_{MPS_HIGH}	AUC floating	80	84	90	ms
PoE MPS Time Low	t_{MPS_LOW}	AUC floating	217	228	240	ms
PoE MPS Time High	t_{MPS_HIGH}	AUC 332K 1% tolerance to V_{SS}	75	80	85	ms
PoE MPS Time Low	t_{MPS_LOW}	AUC 332K 1% tolerance to V_{SS}	218	232	246	ms
THERMAL SHUTDOWN						
Thermal-Shutdown Threshold	T_{SD}	T_J rising		150		°C
Thermal-Shutdown Hysteresis	V_{CDLY_HYS}	T_J falling		30		°C
POWER LEVEL IDENTIFICATION						
Maximum Power Level	P_{MAX}	CLASS 0/3		12.65		W
		CLASS 4		24.96		
		CLASS 5		37.27		
		CLASS 6		49.57		
		CLASS 7		59.41		
		CLASS 8		69.26		
Current Threshold	I_{TH1}	EVENT 4	4.5	6.5	8.5	mA
	I_{TH2}	EVENT 5	21	23	25	
CURRENT-LIMIT THRESHOLD						
Maximum Current Limit	I_{LIM}	CLASS 0/3		302		mA
		CLASS 4		591		
		CLASS 5		886		
		CLASS 6		1181		
		CLASS 7		1413		
		CLASS 8		1645		
POWER MONITORING (THROUGH MEC PIN)						
Power Report Offset				±0.5		W
Power Report Accuracy		12.65W ≤ P_{MAX} < 24.96W, V_{IN} = 48V	-5.5		+5.5	%
		24.96W ≤ P_{MAX} < 69.26W, V_{IN} = 48V	-3		+3	
ADC						
Resolution				7		bits
Power Reading Range	P_{MEC}	All classes		90		W
Power LSB Step Size	P_{LSB}			703.2		mW

(V_{IN} = (V_{DD} - V_{SS}) = 48V, R_{CLSA} = 619Ω, R_{CLSB} = 619Ω; RTN, WAD, PG, MEC, PCN, and LLDP are unconnected, all voltages are referenced to V_{SS}, unless otherwise noted. T_A = T_J = -40°C to +125°C, unless otherwise noted. Typical values are at T_A = +25°C. (*Note 1*))

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
POWER LIMIT LOOP						
Power Loop Response Time				20		ms
Power-Limit Accuracy		12.65W ≤ P_{MAX} < 69.26W, V_{IN} = 48V	-5.5		+5.5	%
Current-Limit Accuracy		302mA ≤ I_{LIM} < 1645mA, V_{IN} = 48V	-3.5		+3.5	%
TRSP Pin Pull-up Current during Detecting Time	I_{TRSP}	V_{TRSP} = V_{VSS}		333		µA
TRSP Pin Detecting Time	t_{DETECT}	t_{TRSP} CAP = 50nF		60		µs
TRSP Pin Source Current		I_{RTN} = 0A, CLASS 0~3, V_{TRSP} = 2V		10		µA
TRSP Pin Sink Current		I_{RTN} = 0.6A, CLASS 0~3, V_{TRSP} = 2V		10		µA
PCN Pin Sink Current		PCN = 1.8V to 4V, I_{RTN} = 0.6A, CLASS 0~3	500			µA
PCN Pin Leakage Current		PCN = 2V, I_{RTN} = 0A, CLASS 0~3			10	µA
		T_A = -40°C to +125°C (*Note 9*) TRSP float			10	
LLDP						
LLDP Logic Threshold	V_{TH_LLDP}	Falling and rising	1.5		3	V
LLDP Pull-up Current	I_{PUP_LLDP}	V_{LLDP} = 0V		500		µA
LLDP Input Pulse Period	T_{LLDP}			1		ms
LLDP Input Reference 50% Pulse Duration	T_{LLDP_1}	(*Note 10*)		500		µs
LLDP Input Reference 75% Pulse Duration	T_{LLDP_2}	(*Note 11*)		750		µs
LLDP Input Pulse Tolerance		(*Note 12*)	-20		+20	µs
Detection Watchdog Timeout	t_{DEC}			2		ms
LLDP DAC Resolution				8		bits
LLDP DAC Power Reading Range	P_{LLDP}	Power mode		90		W
LLDP DAC Power LSB Step Size	P_{LSB}	Power mode		351.6		mW
LLDP DAC Current Reading Range	I_{LLDP}	Current mode		1.8		A
LLDP DAC Current LSB Step Size	I_{LSB}	Current mode		7.03		mA
LLDP Minimum Power-Limit Threshold Setting	P_{LIM_MIN}	Power mode		10		W
LLDP Minimum Current-Limit Threshold Setting	I_{LIM_MIN}	Current mode		140		mA

Note 1: All devices are 100% production tested at T_A = +25°C. Limits over temperature are guaranteed by design.

Note 2: The input offset current is illustrated in the *Detailed Description*.

Note 3: Effective differential input resistance is defined as the differential resistance between V_{DD} and V_{SS}.

Note 4: The classification current is turned off whenever the device is in power mode.

Note 5: UVLO hysteresis is guaranteed by design, not production tested.

Note 6: 20V glitch on input voltage, which takes V_{DD} below V_{ON} shorter than or equal to t_{OFF_DLY}, does not cause the MAX5996C to exit power-on mode.

Note 7: The maximum current limit during normal operation is guaranteed by design; not production tested.

Note 8: In power mode, current-limit foldback is used to reduce the power dissipation in the power MOSFET during an overload condition across V_{DD} and RTN.

Note 9: The specification is guaranteed by GBD data. In the production test it will be only tested at +25°C.

Note 10: 500µs LLDP pulse as bit “0” reference pulse for following data pulses.

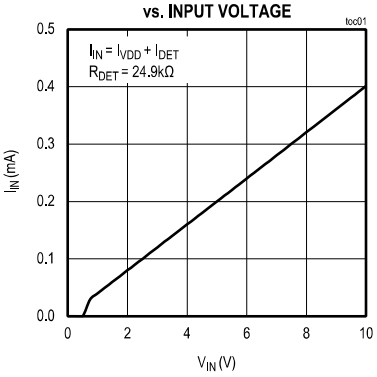
Note 11: 750µs LLDP pulse as bit “1” reference pulse for following data pulses.

Note 12: LLDP data pulse duration tolerances with respect to two 50% and 75% reference pulse durations.

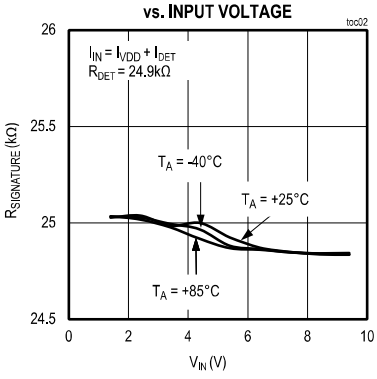
Typical Operating Characteristics

V_{IN} = V_{DD} - V_{SS} = +54V, R_{CLSA} = 30.9Ω, R_{CLSB} = 619Ω, R_{DET} = 24.9kΩ. AUC, WAD, MEC, and LLDP are unconnected unless otherwise noted. All voltages are referenced to V_{SS}.

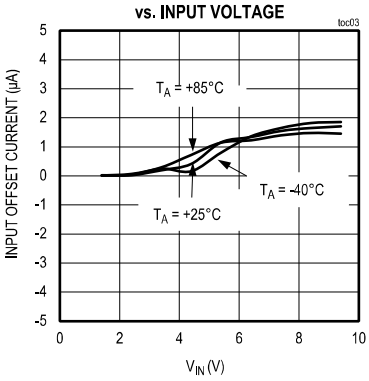
DETECTION CURRENT vs. INPUT VOLTAGE



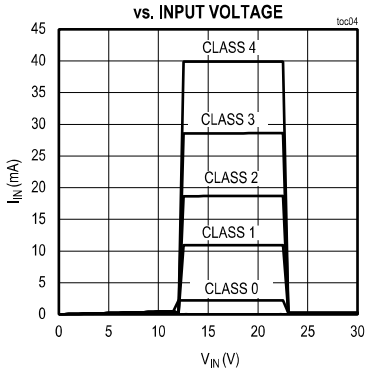
SIGNATURE RESISTANCE vs. INPUT VOLTAGE



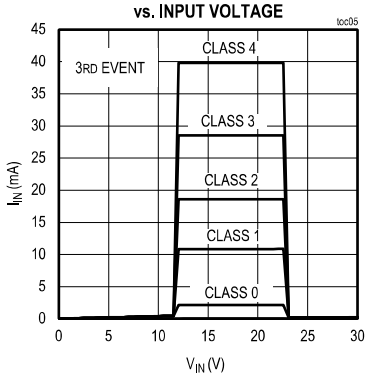
INPUT OFFSET CURRENT vs. INPUT VOLTAGE



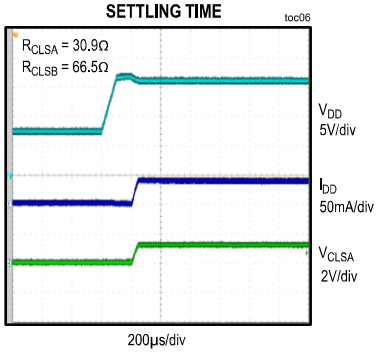
CLASSIFICATION CURRENT vs. INPUT VOLTAGE



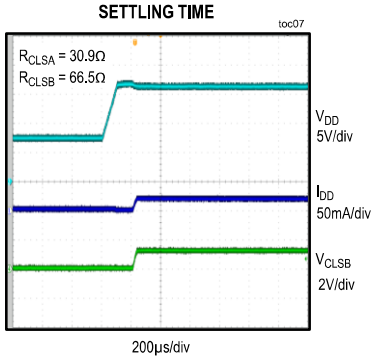
CLASSIFICATION CURRENT vs. INPUT VOLTAGE



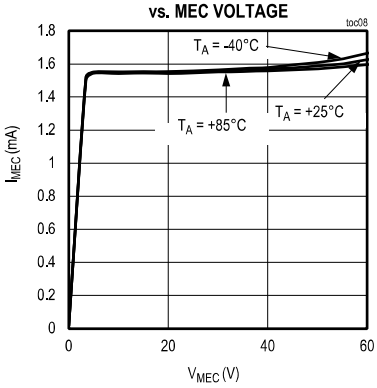
CLASSIFICATION SETTLING TIME



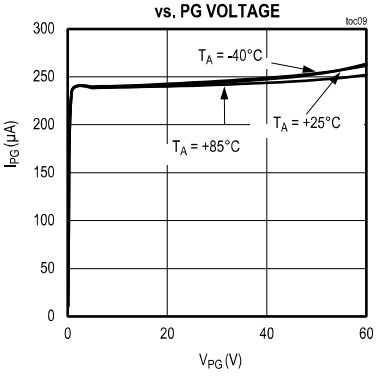
CLASSIFICATION SETTLING TIME



MEC SINK CURRENT vs. MEC VOLTAGE



PG SINK CURRENT vs. PG VOLTAGE



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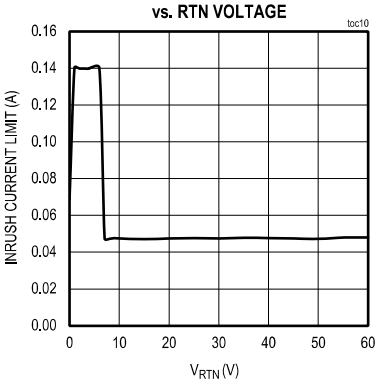
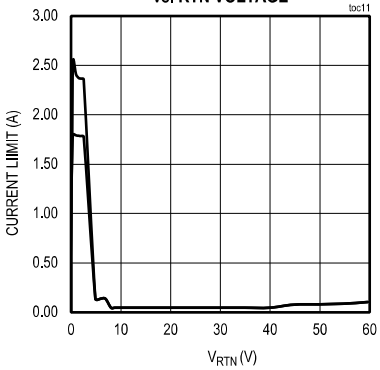
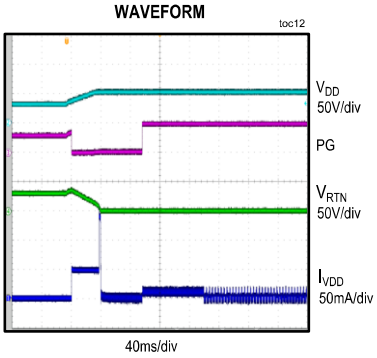
INRUSH CURRENT LIMIT vs. RTN VOLTAGE



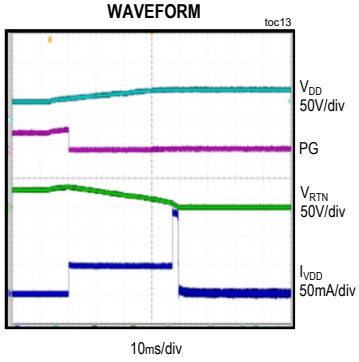
NORMAL OPERATION LIMIT vs. RTN VOLTAGE



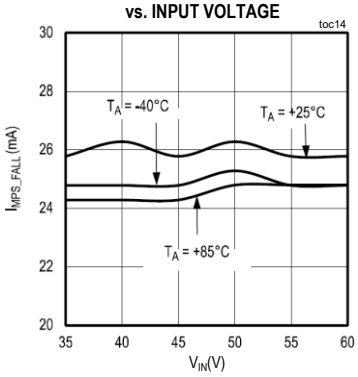
STARTUP INRUSH CONTROL WAVEFORM



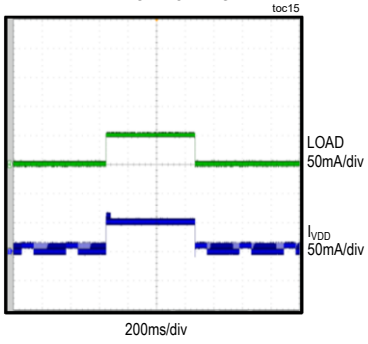
STARTUP INRUSH CONTROL WAVEFORM



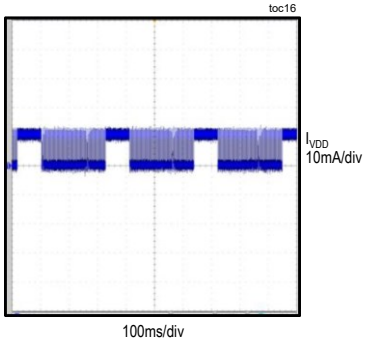
MPS CURRENT FALLING THRESHOLD vs. INPUT VOLTAGE



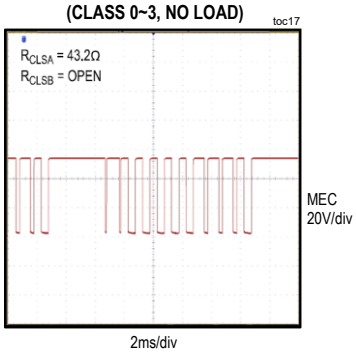
MPS CURRENT WAVEFORM WITH LOAD CHANGE



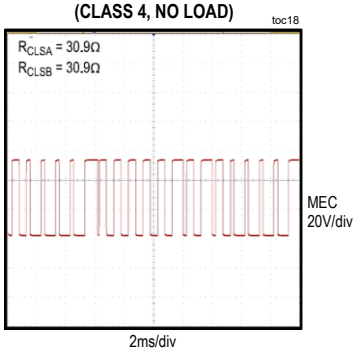
MPS CURRENT WAVEFORM



MEC WAVEFORM (CLASS 0~3, NO LOAD)

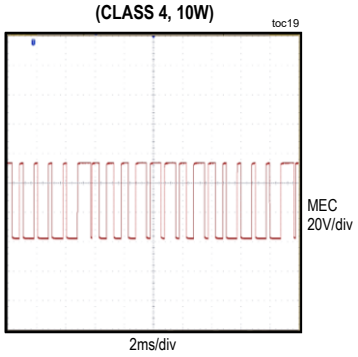


MEC WAVEFORM (CLASS 4, NO LOAD)

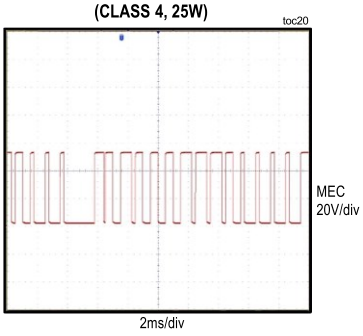


V_{IN} = V_{DD} - V_{SS} = +54V, R_{CLSA} = 30.9Ω, R_{CLSB} = 619Ω, R_{DET} = 24.9kΩ. AUC, WAD, MEC, and LLDP are unconnected unless otherwise noted. All voltages are referenced to V_{SS}.

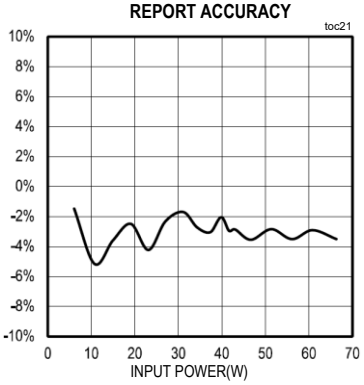
MEC WAVEFORM (CLASS 4, 10W)



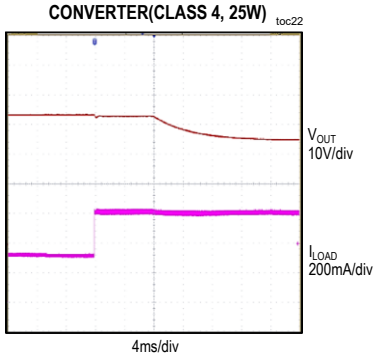
MEC WAVEFORM (CLASS 4, 25W)



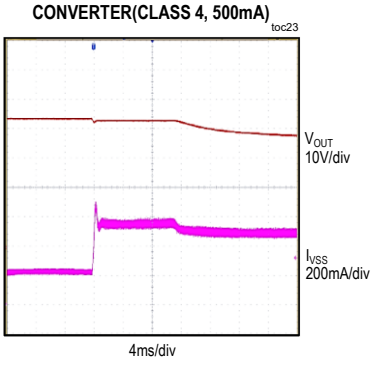
MEC POWER TELEMETRY REPORT ACCURACY



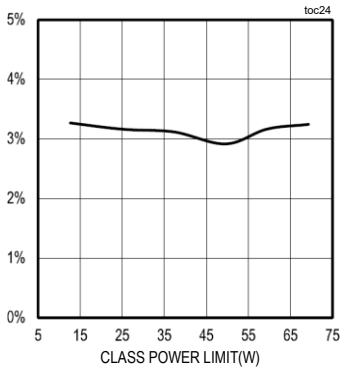
POWER LIMIT RESPONSE with DC-DC CONVERTER(CLASS 4, 25W)



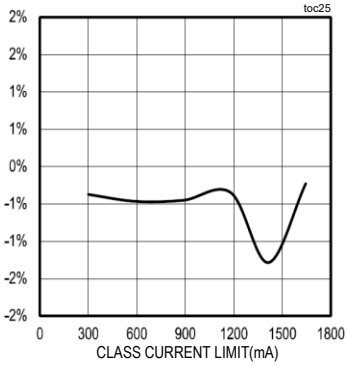
POWER LIMIT RESPONSE with DC-DC CONVERTER(CLASS 4, 500mA)



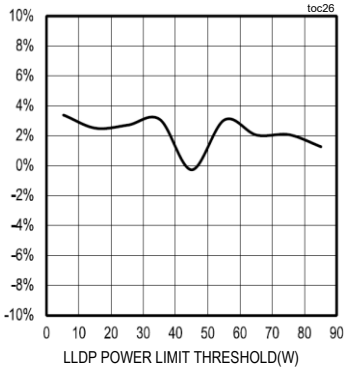
POWER LIMIT ACCURACY



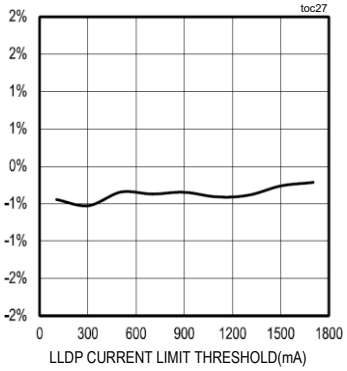
CURRENT LIMIT ACCURACY



LLDP POWER LIMIT ACCURACY

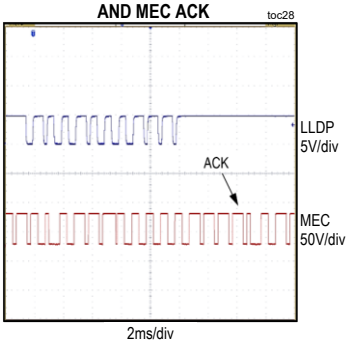


LLDP CURRENT LIMIT ACCURACY

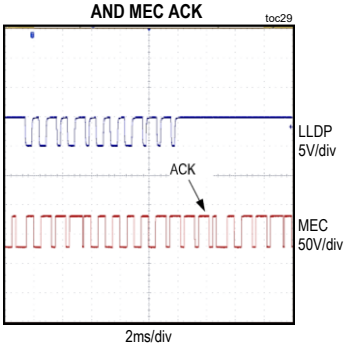


V_{IN} = V_{DD} - V_{SS} = +54V, R_{CLSA} = 30.9Ω, R_{CLSB} = 619Ω, R_{DET} = 24.9kΩ. AUC, WAD, MEC, and LLDP are unconnected unless otherwise noted. All voltages are referenced to V_{SS}.

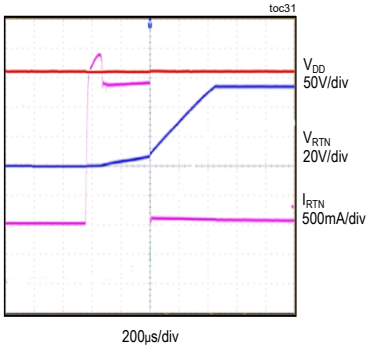
LLDP POWER MODE INPUT (25W) AND MEC ACK



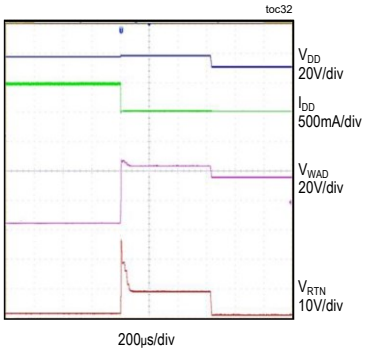
LLDP LIMIT MODE INPUT (500mA) AND MEC ACK



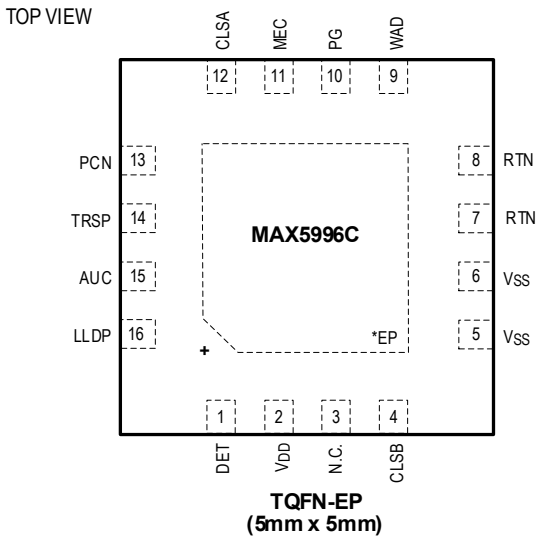
OVERLOAD CURRENT LIMIT



48V WALL ADAPTER PLUG IN



Pin Configurations



*EP = EXPOSED PAD. CONNECT EP TO V_{SS}.

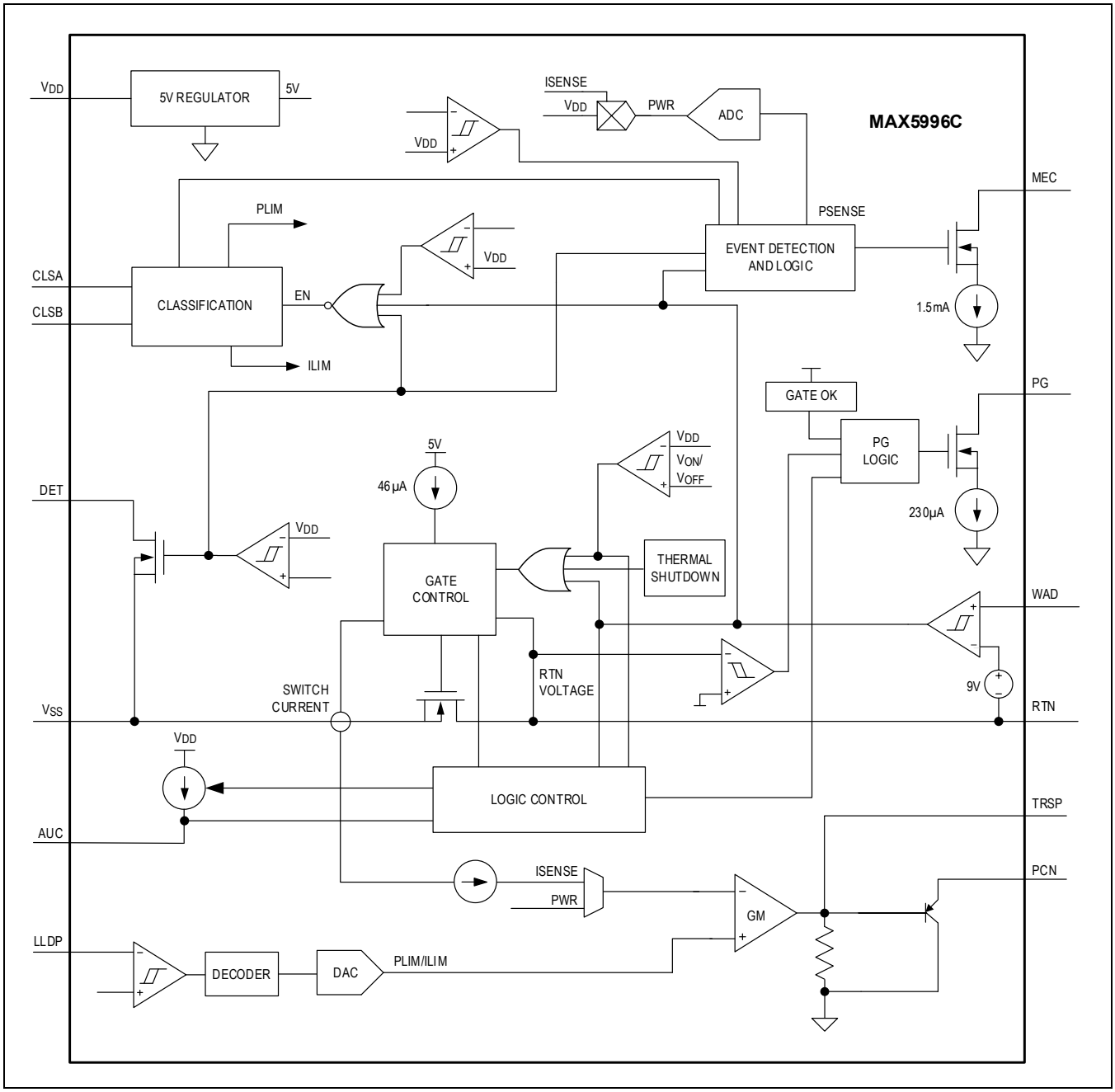
Pin Descriptions

PIN	NAME	FUNCTION
1	DET	Detection Resistor Input. Connect a signature resistor (R_{DET} = 24.9kΩ) from DET to V_{DD}.
2	V_{DD}	Positive Supply Input. Connect a 68nF bypass capacitor between V_{DD} and V_{SS}.
3	N.C.	No Connection. Not internally connected.
4	CLSB	Classification Resistor Input. Connect a resistor (R_{CLS}) from CLSB to V_{SS} to set the classification current. See *Table 1*.
5,6	V_{SS}	Negative Supply Input. V_{SS} connects to the source of the power MOSFET.
7,8	RTN	Drain of Power MOSFET. RTN connects to the drain of power MOSFET. Connect RTN to the downstream DC-DC converter ground, as shown in the *Typical Application Circuit*.
9	WAD	Wall Power Adapter Detector Input. Wall adapter detection is enabled the moment V_{DD} - V_{SS} crosses the mark event threshold. Detection occurs when the voltage from WAD to RTN is greater than 9V. When a wall power adapter is present, the power MOSFET turns off. Connect WAD directly to RTN when the wall power adapter or other auxiliary power source is not used.
10	PG	Open-Drain, Power-Good Indicator Output. PG sinks 230µA to disable the downstream DC-DC converter while turning on the power MOSFET. The PG current sink is disabled during detection, classification, and in the steady-state power mode.
11	MEC	Multi-Event Classification, Power Telemetry Report, or Wall Adapter Indication Output. This pin is an open-drain output, and it generates duty cycle patterns to indicate the power level allocated by PSE, and also to report real-time power consumption and wall adapter presence. The MEC only generates pattern pulses after the power MOSFET is fully turned on and PG asserts. The MEC also sends out an ACK pulse when the device detects a valid LLDP data frame. When entering power- or current-limiting mode, MEC is pulled low for 2ms and repeats every 64ms to “alert” the system.
12	CLSA	Classification Resistor Input. Connect a resistor (R_{CLS}) from CLSA to V_{SS} to set the classification current for the 3at/af standard. See *Table 1*.

13	PCN	Power/Current Control Output Pin. Connect the PCN pin to the DC-DC controller IC COMP pin to sink current to limit converter output power/current when port power/current reaches the limit.
14	TRSP	Power/Current Control Loop Transconductance Amplifier Output. Connect a capacitor to V_{SS}, or a capacitor with a series resistor to RTN to set the power/current loop response time. Floating the TRSP pin disables the power-limiting function.
15	AUC	MPS Configuration Input. Connect a resistor (1% accuracy) between AUC and V_{SS} to program the amplitude and duty cycle of the MPS current in MPS mode. There are two settings: floating and 332kΩ to V_{SS} for the MPS current duty cycle and amplitude. See *Table 3*.
16	LLDP	Input Pin for Recognizing Power Limit Level Requests from System Management Microcontroller through a Series of Pulses. This power-limit request overwrites the power-/current-limit identification from physical classification. Leave the LLDP pin floating if not used. When LLDP is left floating, the device is in power mode, and when LLDP is shorted to V_{SS} or receiving current-limit pulses, the device is in current mode.
—	EP	Exposed Pad. Do not use EP as an electrical connection to V_{SS}. EP is internally connected to V_{SS} through a resistive path and must be connected to V_{SS} externally. To optimize power dissipation, solder the exposed pad to a large copper power plane.

Functional Diagrams

Block Diagram



Detailed Description

Operation Mode

Depending on the input voltage (V_{IN} = V_{DD} - V_{SS}), the MAX5996C operates in four different modes: PD detection, PD classification, mark event, and PD power. The device enters PD detection mode when the input voltage is between 1.4V and 10.1V. The device enters PD classification mode when the input voltage is between 12.5V and 20.5V. The device enters PD power mode once the input voltage exceeds V_{ON}.

Detection Mode

In detection mode, the power source equipment (PSE) applies two voltages on V_{IN} in the 1.4V to 10.1V range (1V step minimum) and then records the current measurements at the two points. The PSE then computes ΔV/ΔI to ensure the presence of the 24.9kΩ signature resistor.

In detection mode, most of the device internal circuitry is off and the offset current is less than 10µA. Polarity protection diodes at the input terminal prevent internal damage to the device (see the *Typical Application Circuit*). Since the PSE uses a slope technique (ΔV/ΔI) to calculate the signature resistance, the DC offset due to the protection diodes is subtracted and does not affect the detection process.

Classification Mode

In classification mode, the PSE classifies the PD based on the power requested by the PD. This allows the PSE to efficiently manage power distribution. Two external resistors connected from CLSA/CLSB to V_{SS} set the classification signature to the PSE and define the power requested from the PD. R_{CLSA} sets classification current for the 1st and 2nd class events for class 0~4 PDs compliant with the IEEE 802.3af/at standards, and R_{CLSB} sets classification current for the 3rd to 5th class events for class 1~8 PDs compliant with the IEEE 802.3bt standard.

The PSE classifies the PD by applying a voltage at the PD input and measuring the current sourced out of the PSE. When the PSE applies a voltage between 12.5V and 20.5V, the device exhibits a series of events with current characteristics. *Table 1* shows the R_{CLSA} and R_{CLSB} resistor values needed to set for the PD class and the PD power requested defined by IEEE 802.3af/at/bt standards. The PSE uses the number of class events and classification current information to classify the power requirement of the PD. The classification current includes the current drawn by R_{CLSA} and R_{CLSB} and the supply current of the device, so the total current drawn by the PD is within the IEEE 802.3af/at/bt standards. The classification current is turned off whenever the device is in power mode.

Table 1. PD Class with Classification Resistor R_{CLSA} and R_{CLSB}

PD CLASS	POWER REQUESTED BY PD (W)	RCLSA (Ω)	RCLSB (Ω)
0	13	619	619
1	3.84	118	118
2	6.49	66.5	66.5
3	13	43.2	43.2
4	25.5	30.9	30.9
5	40	30.9	619
6	51	30.9	118
7	62	30.9	66.5
8	71.3	30.9	43.2

Multi-Event Classification and Detection

IEEE 802.3bt defines physical classification to allow a PD to communicate its power classification to the connected PSE and to allow the PSE to inform the PD of the PSE's allocated power. The PD classes (0~8) and PD power requests during multi-event classification are configured by setting the R_{CLSA} and R_{CLSB} resistor values in *Table 1*. This configuration is compatible with the IEEE 802.3af/at standard.

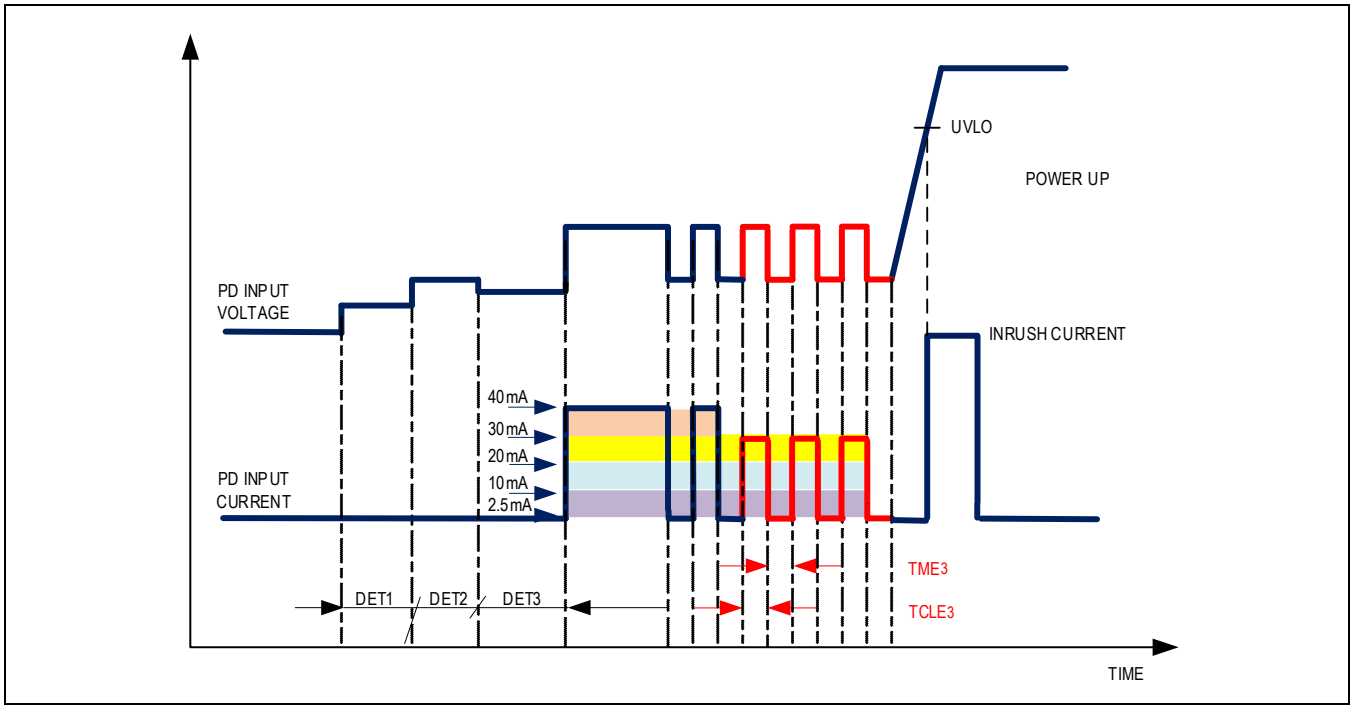


Figure 1. Multi-Event Classification

Power Mode

The MAX5996C enters power mode when V_{IN} rises above the undervoltage-lockout threshold (V_{ON}). When V_{IN} rises above V_{ON}, the device turns on the power MOSFET to connect V_{SS} to RTN with inrush current limit internally set to 53mA (typ) when V_{RTN} - V_{SS} > 7V and 135mA (typ) when V_{RTN} - V_{SS} < 7V. The power MOSFET is fully turned on when the voltage at RTN is near V_{SS} and the inrush current is reduced below the inrush limit. Once the power MOSFET is fully turned on, the device changes to the normal operation current limit. The open-drain, power-good output (PG) remains low for a t_{DELAY} time (see the *Electrical Characteristics*) until the power MOSFET fully turns on to keep the downstream DC-DC converter disabled during inrush. Note that using larger output capacitors will result in longer start-up t_{DELAY} time.

Power Demotion

The power demotion feature is provided for the situation where the power level the PD requested is not available at the PSE. When power demotion occurs, the PD must operate in a reduced power mode while connected to a lower power PSE. In power demotion mode, the PSE provides the power that its classification indicates. For example, an IEEE 802.3af PSE issues up to a single event regardless of PD Class.

Multi-Event Indication (MEC)

The MAX5996C communicates its available power level to the system user through the MEC pin. The MEC pin state is a result of the number of classification/mark events and whether the PD is in PoE or auxiliary power operation. The MEC pin can indicate power allocated from the PSE to the PD in five different cases. The MAX5996C uses a unique encoding method on the MEC pin to indicate the power levels that are higher than 12.95W. The first pulse sent from MEC is START bit (256µs, 25% duty) for the system to detect. Then the pattern of 2nd, 3rd, and 4th pulses that are double or triple the pulse width of the START bit (50% and 75% duty) are issued to indicate the type of PSE and power allocated from the PSE. This pulse train is repeated at a certain frequency.

The number of events and the maximum power granted from the PSE at the PD input are listed in *Table 2*. 1-Event and 2-Event are compatible with the IEEE 802.3af/at standards. 3-Event, 4-Event, and 5-Event indicate the IEEE 802.3bt standard.

The MEC is enabled after the power MOSFET is fully on until V_{IN} drops below the UVLO threshold.

Table 2. MEC Pattern with Number of Events and PD Class

CLASS	NUMBER OF EVENTS	MAXIMUM POWER GRANTED AT PD INPUT
0-3	1	13W
	Wall Adapter	
4	2 or 3	25.5W
5	4	40W
6	4	51W
7	5	62W
8	5	71.3W

The MEC pin also reports real-time power consumption as shown in *Figure 2*. The 90% pulse (900µs) is the start bit of power telemetry. After, the 50% pulse (500µs) represents bit “0”, and the 75% pulse (750µs) represents bit “1”. There are a total of 7-bit digitized pulses representing the power consumption at the PD. The eighth bit in the sequence is a DON’T CARE.

The last pulse in the MEC pulse series is the ACK pulse for the LLDP pin. The 75% duration pulse is ACK pulse, and the 50% duration pulse is a NACK pulse. Once the LLDP pin detects valid LLDP data, an ACK pulse is sent out from MEC to acknowledge the system MCU. If there are no LLDP input pulses or the LLDP input pulses are not valid, a NACK pulse will be sent out in MEC pulses.

When the device enters power- or current-limiting mode, MEC will be pulled low immediately for 2ms and repeat this 2ms “low” pulse every 64ms to “alert” system for power/current-limiting mode until the device exits power- or current-limiting mode. The MEC pattern will be interrupted by this 2ms “low” pulse intermittently. The power-limit alert “low” pulse may occur at any point during the MEC pattern.

When there is an overload condition, and the device enters current-limiting/foldback mode, the MEC pin stops giving out data pulses and switches to high impedance. When the device exits the overload current-limiting mode, the MEC pin resumes pulse generating.

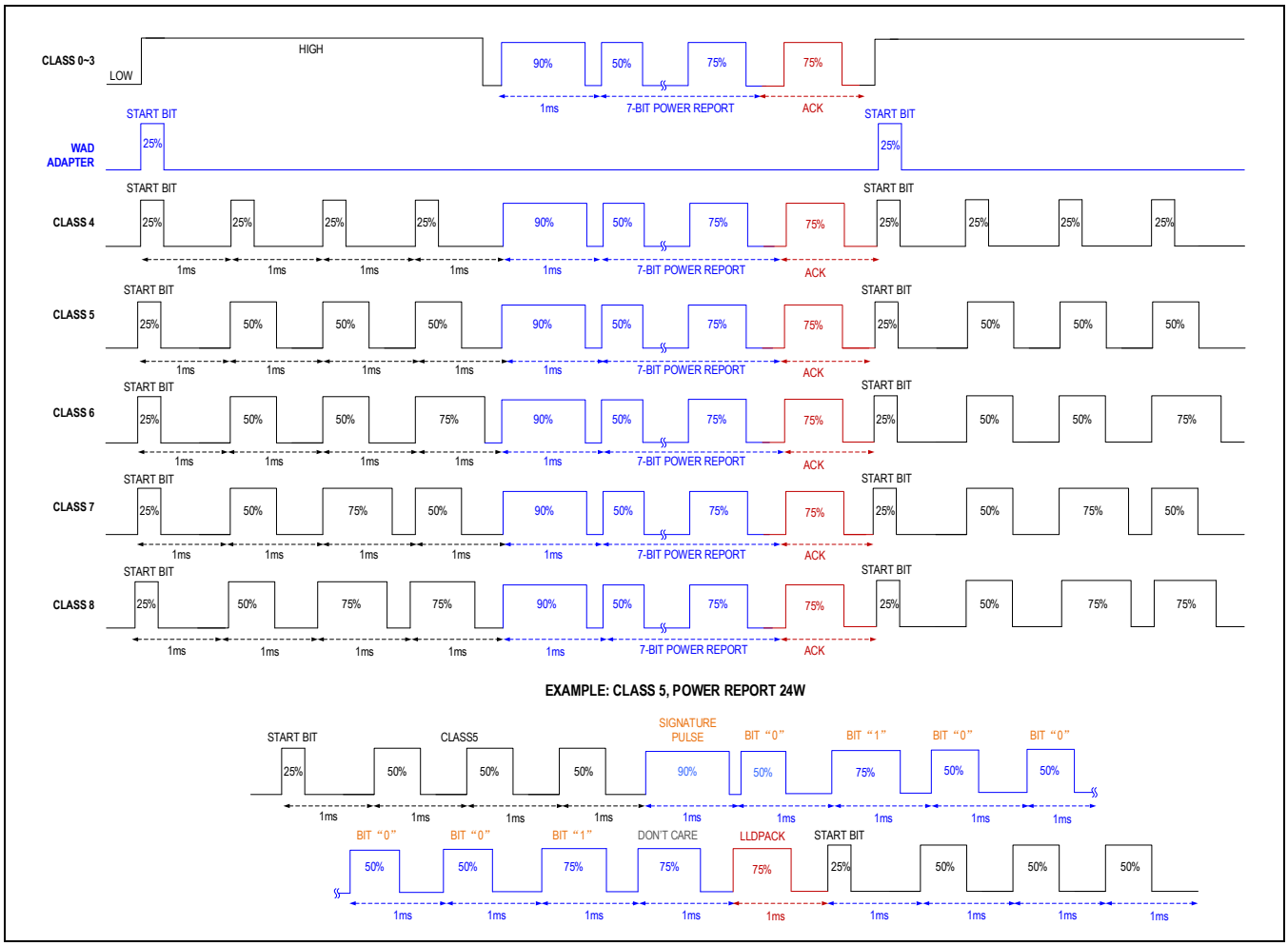


Figure 2. MEC Waveforms in Different Scenarios

Undervoltage Lockout

The MAX5996C operates with a turn-on UVLO threshold (V_{ON}) at 35.4V and a turn-off UVLO threshold (V_{OFF}) at 30V. When the input voltage is above V_{ON}, the device enters power mode and the power MOSFET is turned on. When the input voltage goes below V_{OFF} for longer than t_{OFF_DLY}, the power MOSFET turns off.

Intelligent MPS

The MAX5996C intelligent MPS feature enables applications that require low-power standby modes. The MPS current is generated to comply with the IEEE 802.3bt standard for a PSE to maintain power on in standby modes. A minimum current (10mA or 20mA) of the port is able to be maintained with MPS mode to avoid the power disconnection from the PSE. The device automatically enters MPS mode when the port current is lower than 24mA (typ) and exits MPS mode when the port current is greater than 28.7mA (typ).

Figure 3 shows intelligent MPS behavior. The MPS comparator is an autozero comparator and it will sample the port current every 32µs. The MPS comparator is always switched on when the power MOSFET is fully turned on. If the MPS comparator falling threshold is triggered continuously within 320µs, the part enters MPS mode and the MPS current is generated. Once the part enters MPS mode, it waits for the t_{MPS} timer to elapse before checking the MPS comparator again.

In MPS mode, the intelligent MPS modulation scheme is shown in *Figure 3* (the MPS duty cycle is 25%). PG remains high to enable the downstream DC-DC converter in MPS mode.

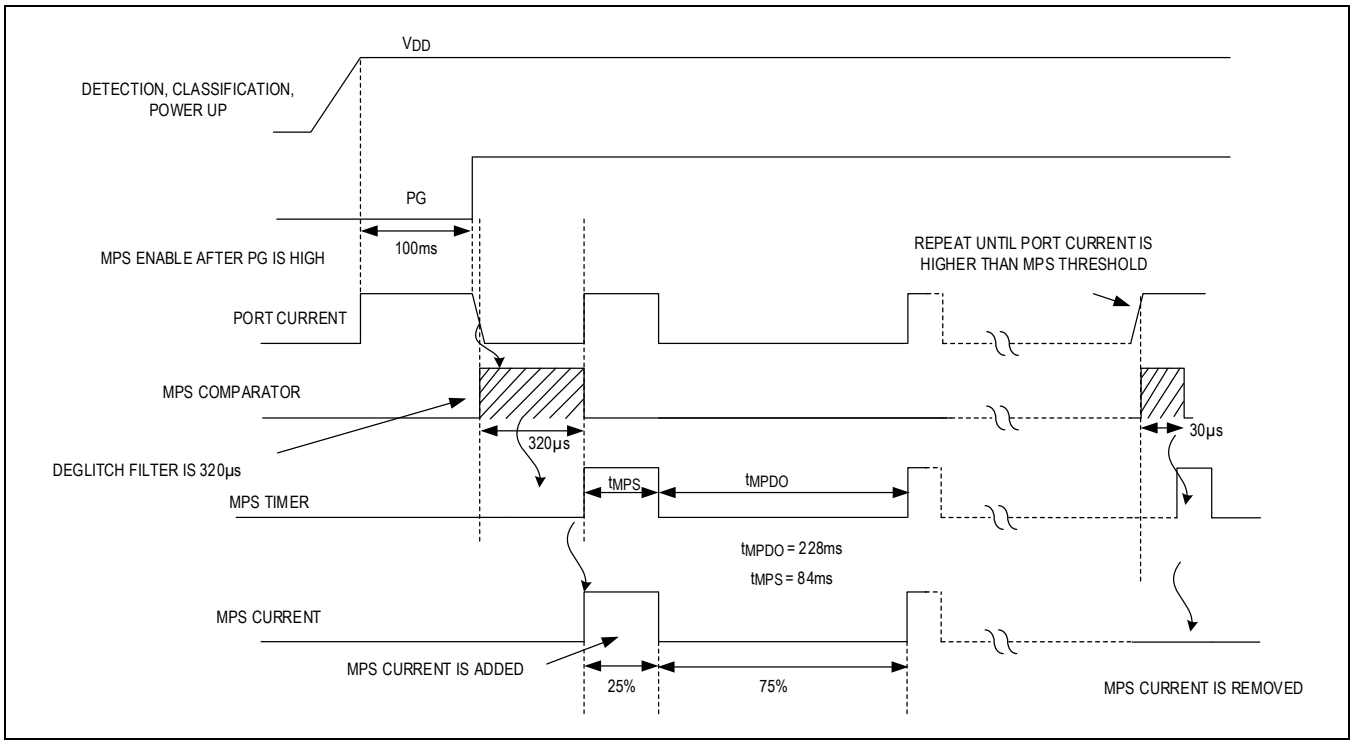


Figure 3. Intelligent MPS Behavior

Power-Good Output

An open-drain output (PG) is used to allow disabling downstream DC-DC converter until the power MOSFET is fully turned on. PG is pulled low to V_{SS} for a period of t_{DELAY} and until the power MOSFET is fully turned on. Using larger output capacitors will result in longer t_{DELAY} time. PG is also pulled low in an overtemperature event and pulled high once the device comes out of thermal shutdown and resumes normal operation.

Configurable MPS

Connecting a resistor (1% accuracy) between AUC and V_{SS} programs the amplitude and duty cycle of MPS current in MPS mode; there are two settings: floating (> 25%) and 332kΩ (25%).

Table 3. AUC Configuration for MPS Current

AUC PIN CONFIGURATION	MPS DUTY CYCLE	MPS CURRENT AMPLITUDE	SUPPORT AUTOCLASS
AUC floating	> 25%	10mA	NO
Connect 332kΩ between AUC and V_{SS}	25%	20mA	NO

The MAX5996C modulates the I_{MPS} duty-cycle current according to resistor values on the AUC pin. The I_{MPS} modulation scheme is shown in *Figure 4*.

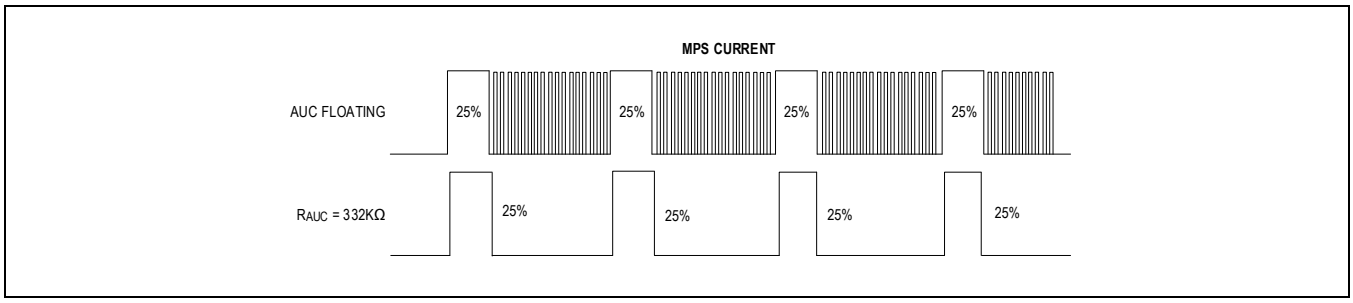


Figure 4. MPS Current with Different AUC Configuration

Thermal-Shutdown Protection

The MAX5996C includes thermal protection from excessive heating. If the junction temperature exceeds the thermal-shutdown threshold of +150°C, the device turns off the internal power MOSFET and MEC current sink. When the junction temperature falls below +120°C, the device enters startup mode and then power mode. Startup mode ensures the downstream DC-DC converter is turned off by pulling PG low until the power MOSFET is fully turned on.

Wall Power Adapter Detection and Operation

The device features wall power adapter detection for applications where an auxiliary power source such as a wall power adapter is used to power the PD by connecting it to the WAD pin to RTN. Once the input voltage exceeds the mark event threshold, wall adapter detection is enabled. The device gives the priority to the wall adapter and smoothly switches the power supply to the wall adapter when the wall adapter is detected. The device detects a wall power adapter when the voltage from WAD to RTN is greater than 9V. When a wall power adapter is detected, the internal power MOSFET turns off, the MEC current sink turns on to indicate a certain pattern (see the *Multi-Event Indication (MEC)* section), the classification current is disabled if V_{IN} is in the classification range, and the intelligent MPS comparator is turned off.

Power Level Identification

The MAX5996C can identify power class levels by measuring the R_{CLSB} value and recognizing the number of the classification events. The power class level is used to set the reference for the power/current control loop to implement power/current limiting when the power/current is reaching the limit. See *Table 2*.

Power Limiting

When the LLDP pin is floating or receiving power limit pulses, the device works in power limit mode. The power limiting function is disabled during power MOSFET power-up, enabled 1.2ms (typ) after the power MOSFET is fully enhanced, and stays enabled at normal operation. When the PD power reaches the limit, the constant power loop starts to sink current from the PCN pin and the overdrive COMP pin of the DC-DC controller IC (for example, the MAX5974 or MAX15158) to limit the output power of the converter. Once power limit control takes over, the loop will be dominated by a constant power loop.

Power limiting can be disabled by floating the TRSP pin.

When the PD current reaches the overload current limit (2.4A, typ), the PD current-limiting function takes control immediately to limit the current and protect the power MOSFET from overheating.

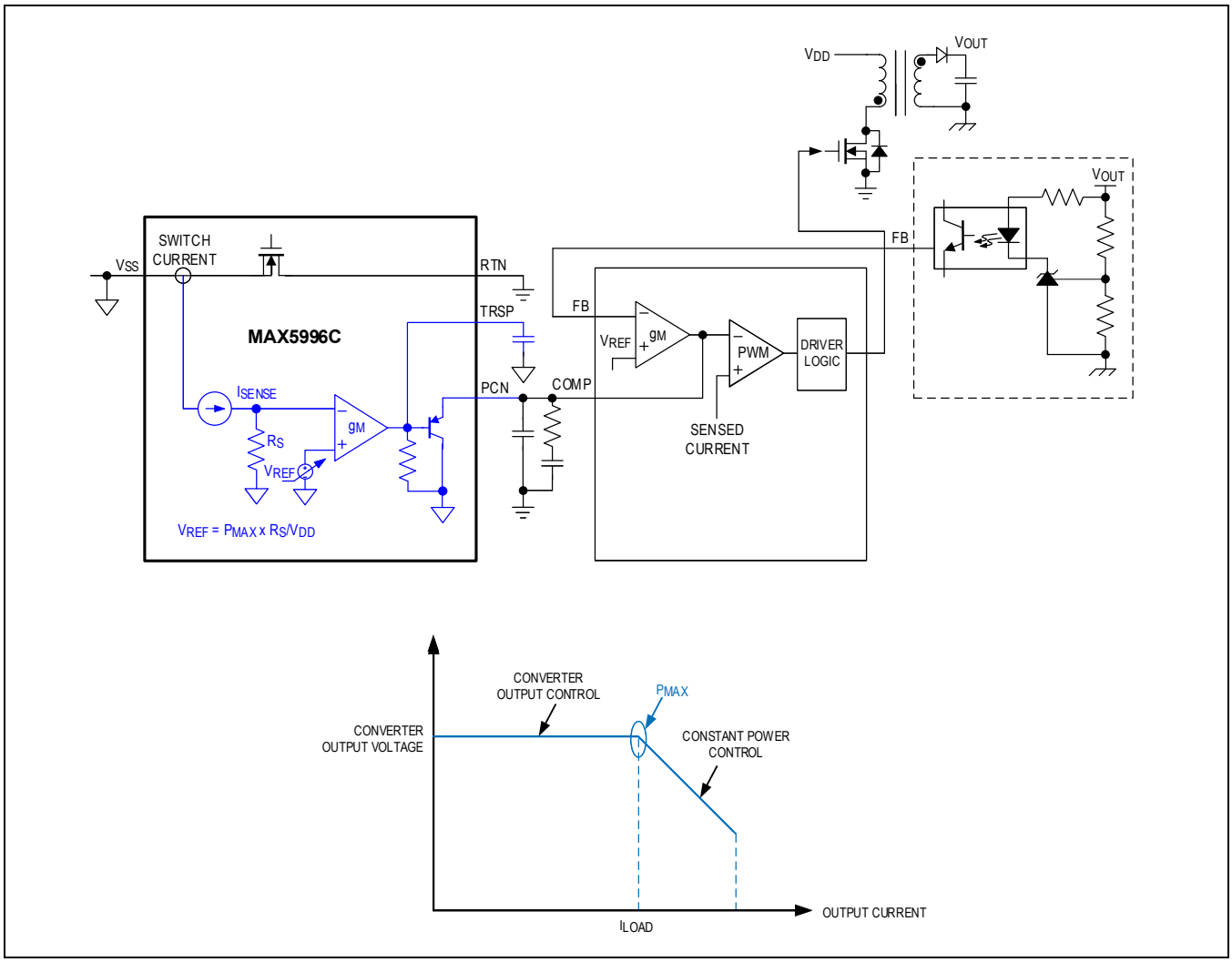


Figure 5. Constant Power Limiting

Current Limit

When the LLDP pin is shorted to V_{SS} or receiving current-limit pulses, the device works in current-limit mode. The current-limiting function is also disabled during power MOSFET power-up and enabled 1.2ms (typ) after the power MOSFET is fully enhanced and stays enabled at normal operation. Instead of limiting power in power mode, in current-limiting mode, the device watches the power MOSFET current. When the power MOSFET current reaches the limit, the loop starts to sink current from PCN pin and overdrive the COMP pin of the MAX5974 (or other DC-DC controller IC) to limit output power, therefore limiting the PD current. The current-limit thresholds are determined from the classification process, and each PD class corresponds to specific current-limit thresholds. (See the *Electrical Characteristics* table.) The current-limiting function can be disabled by floating the TRSP pin.

When the PD current reaches overload current limit (2.4A, typ), the PD current-limiting function takes control immediately to limit the current to protect the power MOSFET from overheating.

Overload Current Limit

The power MOSFET is protected from output overload conditions with an overcurrent limit. An overload at the output results in the current being limited at the threshold (2.4A, typ) and output voltage droop. When $V_{RTN} - V_{VSS}$ exceeds approximately 7.5V the overcurrent limit reverts to inrush current limit (45mA, typ) to further reduce the power dissipation on the power MOSFET.

LLDP Power Level Identification

The Link Layer Discovery Protocol (LLDP) is a link layer protocol used by network devices to negotiate the power level. The main idea is that, after valid detection, the PSE powers up the PD at Type 1 power for the PD system to build up the communication, and then the PD will negotiate the power through software.

The MAX5996C LLDP pin enables the LLDP support by recognizing patterned input pulses from the system management microcontroller to configure the power or current level (P_{MAX} or I_{MAX}) to the PD controller to limit the power or current consumption.

The MAX5996C supports power-limiting and current-limiting modes. The LLDP pin is used to configure which mode the device works with. *Figure 6* is a PD with a non-LLDP configuration, meaning there is no connection or communication from LLDP to the system MCU. In this case:

- When the LLDP pin is left floating, the device works with the power-limiting mode.
- When the LLDP pin is shorted to V_{SS}, the device works with the current-limiting mode.

Figure 7 shows a PD with an LLDP configuration. The LLDP pin behaves as an input pin to recognize power-/current-limit level requests from the system MCU through a series of patterned pulses. The power-/current-limit level information overwrites the limits from the classification process.

Note that when there are no pulses coming from the MCU, the LLDP pin is also “floating” and so it will be in power-limiting mode unless certain patterned current-limiting mode pulses come into the LLDP pin to switch the mode.

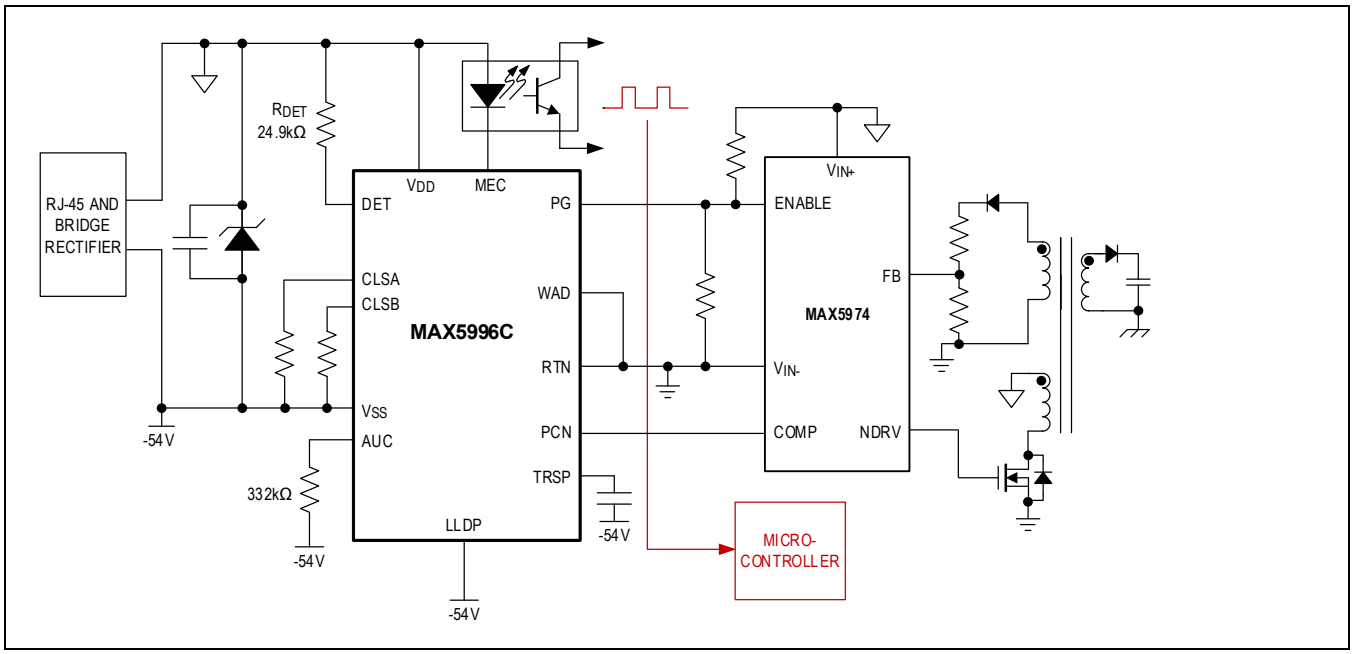


Figure 6. MAX5996C with Non-LLDP Configuration and Set to Current-Limiting Mode

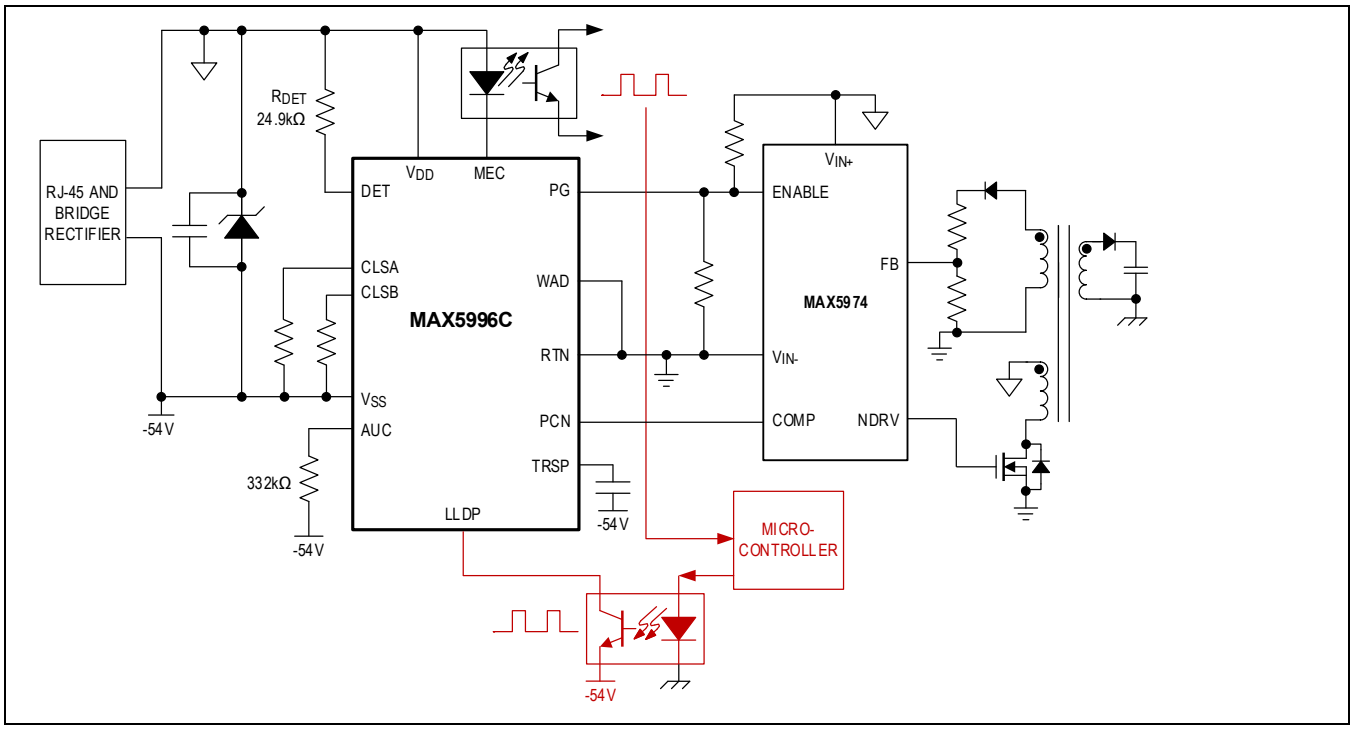


Figure 7. MAX5996C with LLDP Configuration

The LLDP input pulses are a series of 50% (500µs) or 75% (750µs) pulses with a 1000µs period. The first two pulses are the LLDP signature and references, and the following eight pulses represent 8-bit power or current level. The 50% pulse represents bit "0," and the 75% pulse represents bit "1." There needs to be at least a 22ms gap between two LLDP data frames. See *Figure 8*.

- When the two signature pulses are 50% first and 75% second, the device is in power-limit mode. The following data pulses represent power-limit information.
- When the two signature pulses are 75% first and 50% second, the device is in current-limit mode. The following data pulses represent current-limit information.

The device only allows mode changing when the power- or current-limit loop is not active.

Once the power/current-limit level is recognized and identified from the LLDP pin, the LLDP power/current-limit level overwrites the power/current level from the classification process. The PD controller uses the LLDP limit level as the power/current-limiting control reference. The new LLDP power/current level reading overwrites the previous one.

When the MAX5996C powers down and up again, the default power/current level is the level from the classification process until the LLDP reads back to the power/current level and overwrites it.

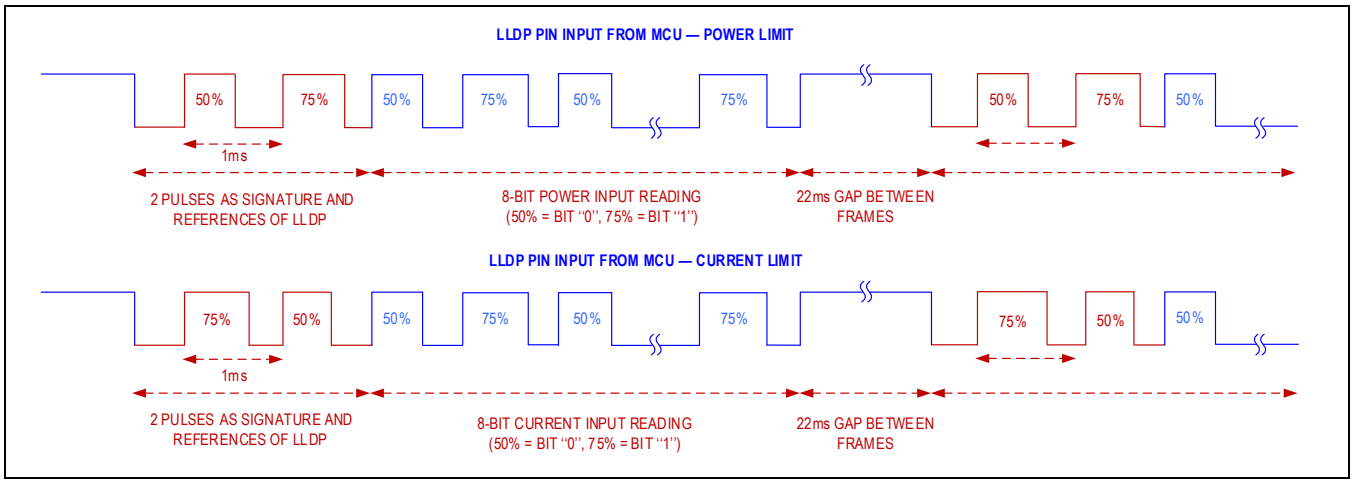
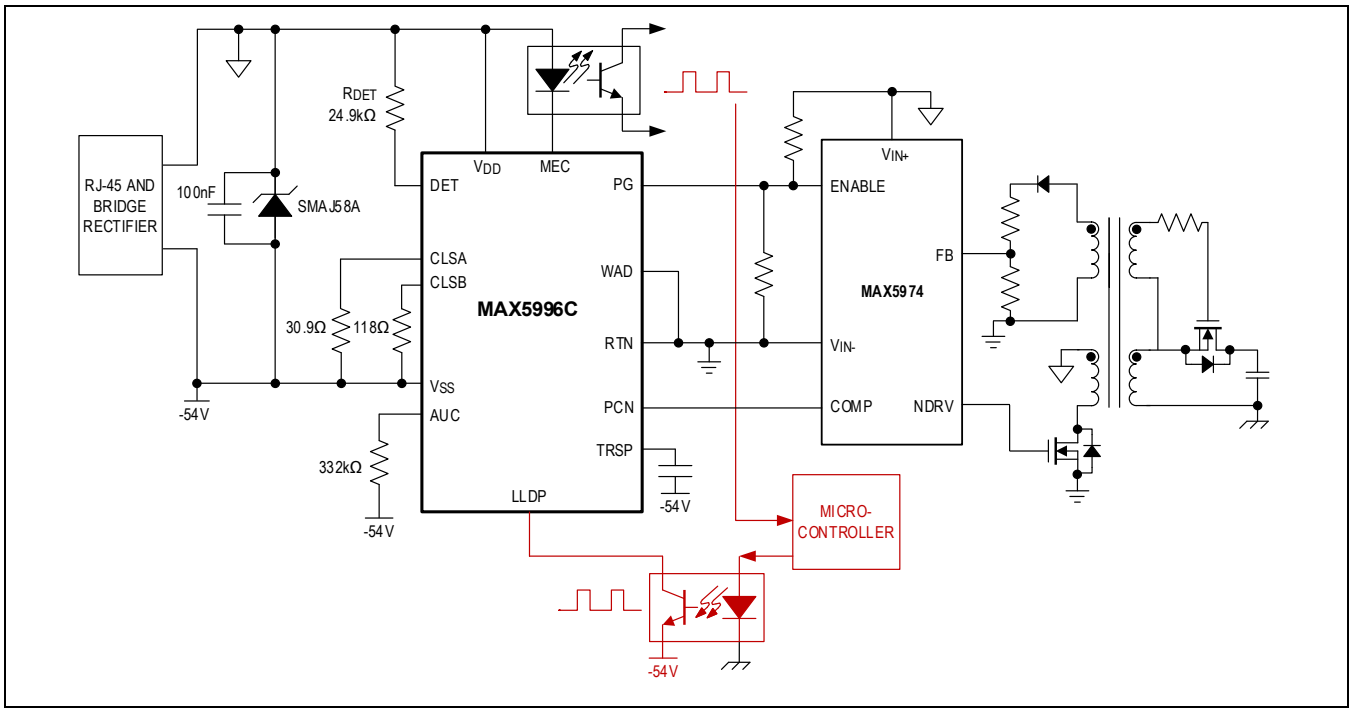


Figure 8. LLDP Input Pulses

Typical Application Circuit



Ordering Information

PART NUMBER	TEMP RANGE	PIN-PACKAGE	INTELLIGENT MPS	CONSTANT POWER/ CURRENT LIMIT	LLDP	POWER TELEMETRY
MAX5996CATE+/ MAX5996CATE+T	-40°C to +125°C	16 TQFN-EP	Yes	Yes	Yes	Yes

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	9/21	Release for Market Intro	—
1	3/22	Updated Electrical Characteristics table; removed MAX5996A and MAX5996B from this data sheet	All
2	3/25	Updated Electrical Characteristics table, Pin Descriptions, ADC Resolution, LSB size, and Figures	All
3	4/25	Removed TOC30	12