MAX30131/MAX30132/ MAX30134

1-, 2-, 4-Channel, Ultra-Low Power Electrochemical Sensor AFEs

General Description

The MAX30131/MAX30132/MAX30134 are 1-, 2-, and 4-channel (respectively) ultra-low power programmable analog front ends (AFE) for use with electrochemical sensors. The devices provide the biasing and complete measurement path, including the analog to digital converters (ADCs). The flexibility of the MAX30131/MAX30132/MAX30134 enables them to work with both two and three terminal electrochemical sensors, providing both DC current measurement and electrochemical impedance spectroscopy (EIS) measurement capability. The devices include an internal temperature sensor and programmable voltage reference to support external temperature monitoring, and an external reference source to integrate voltage monitoring of bias and supply voltages for safety and compliance.

The MAX30131/MAX30132/MAX30134 support single-, dual-, and quad- two-terminal or three-terminal electrochemical sensors, respectively. Ultra-low power allows for the continuous biasing of the sensor to maintain accuracy and fast response when a measurement is required. The MAX30131/MAX30132/MAX30134 operate over a 1.73V to 5.0V voltage range. Total current consumption can be less than 5μA depending on the configuration, measurement frequency, and number of sensors. Communication is through a 4-pin SPI serial interface plus a configurable interrupt pin and four configurable general purpose input/outputs (GPIOs) for direct control of internal functions.

The MAX30131/MAX30132/MAX30134 are available in a 25-bump WLP package and operate over a 0°C to +70°C temperature range.

Applications

- Electrochemical Sensors
- Continuous Glucose Monitors
- Sweat Sensors
- Wearable Devices

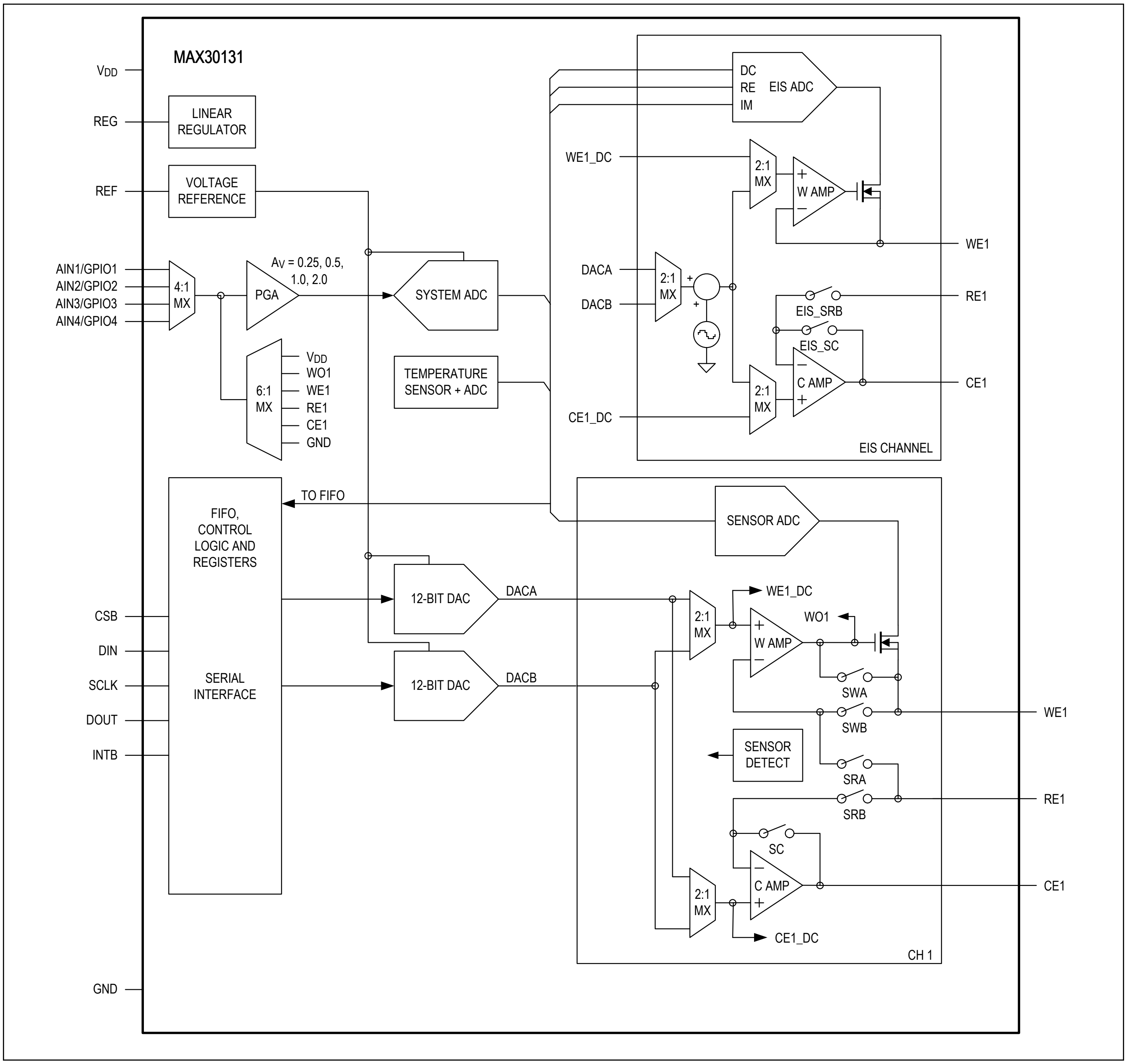
Benefits and Features

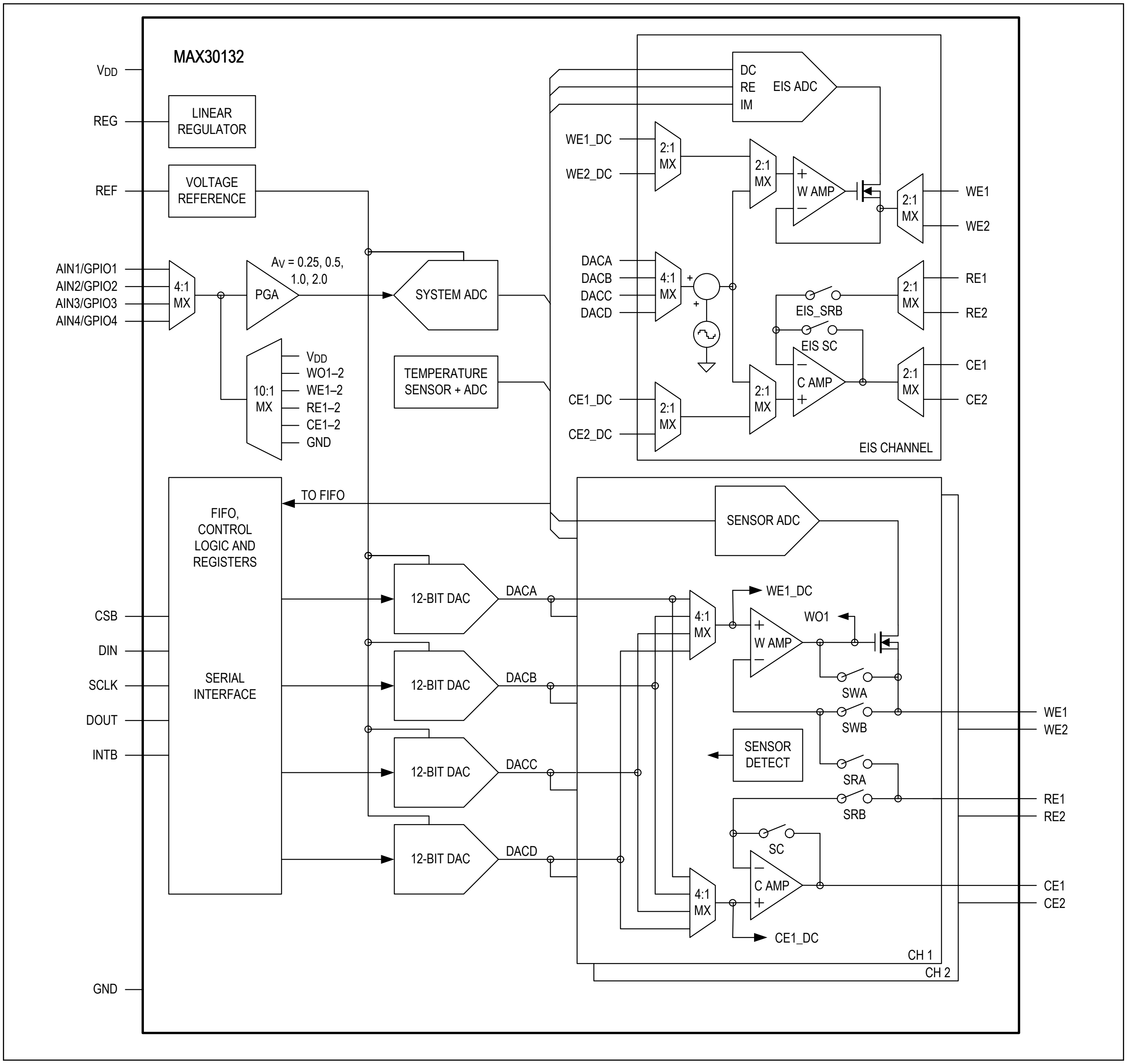
- Multichannel Operation
  - Up to Four Independent DC Channels
  - 1 Switchable EIS Channel
- High Accuracy and Precision
  - Up to Four 12-Bit Voltage DACs
  - Up to Four 16-Bit Current ADCs
    - Programmable 0.8pA to 30pA Resolution
  - One 16-Bit EIS ADC
    - Programmable 0.014Hz to 27kHz Sine Wave Drive
  - 12-Bit Voltage System ADC
  - 16-Bit Temperature Sensor
  - Programmable, 30ppm/°C Voltage Reference
- Autonomous Modes with 256 Word Configurable FIFO and Programmable Alarm
- Long Battery Life for 2- and 3-Terminal Sensors
  - 3.5μA Continuous Bias Supply Current for Single 2- or 3-Terminal Sensor
  - Add 0.25μA for Each Additional Sensor
- Small Size
  - 25-Bump WLP 2.93mm x 2.93mm
- Safety and Compliance
  - Monitor Sensor Bias Voltages for Compliance
  - Monitor Supply/Battery Voltage and Temperature
- Simple and Robust Digital Interface
  - 8MHz 4-Wire SPI Interface
  - Programmable Interrupt
  - Four Programmable GPIOs
- IEC61000-4-2 ESD: ±15kV Air, ±8kV Contact On Sensor Pins

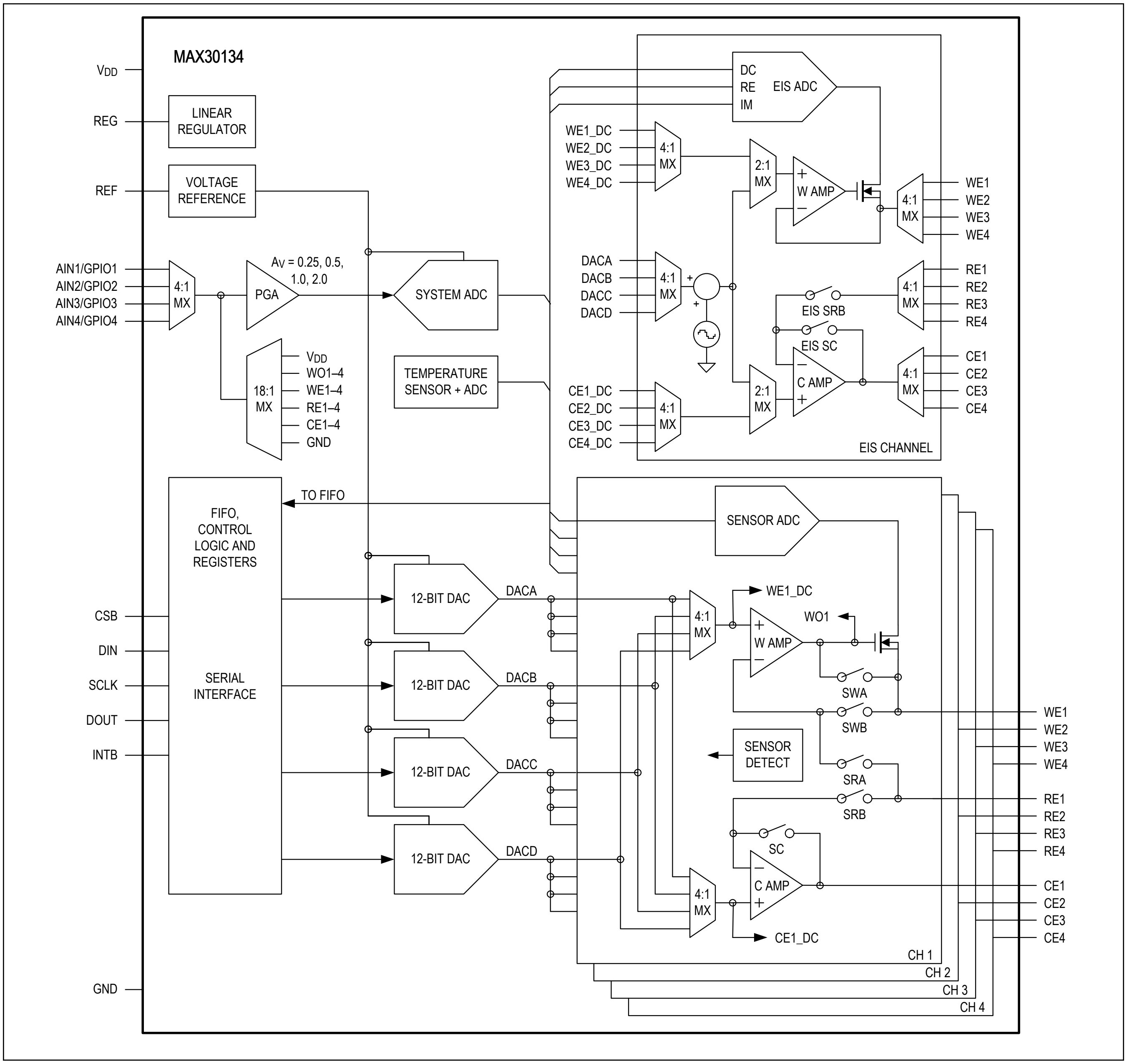
Ordering Information appears at end of data sheet.

19-100638; Rev 5; 2/25

Simplified Block Diagram




MAX30132
VDD
REG
REF
LINEAR REGULATOR
VOLTAGE REFERENCE
AIN1/GPIO1
AIN2/GPIO2
AIN3/GPIO3
AIN4/GPIO4
4:1 MX
PGA
AV = 0.25, 0.5, 1.0, 2.0
SYSTEM ADC
10:1 MX
VDD
WO1–2
WE1–2
RE1–2
CE1–2
GND
TEMPERATURE SENSOR + ADC
FIFO, CONTROL LOGIC AND REGISTERS
TO FIFO
SERIAL INTERFACE
CSB
DIN
SCLK
DOUT
INTB
GND
12-BIT DAC
DACA
DACB
DACC
DACD
DC
RE
IM
EIS ADC
WE1_DC
WE2_DC
2:1 MX
W AMP
WE1
WE2
RE1
RE2
CE1
CE2
EIS_SRB
EIS SC
C AMP
CE1_DC
CE2_DC
EIS CHANNEL
SENSOR ADC
4:1 MX
WO1
SWA
SWB
SRA
SRB
SC
SENSOR DETECT
CH 1
CH 2


MAX30134
V_{DD}
REG
LINEAR REGULATOR
REF
VOLTAGE REFERENCE
AIN1/GPIO1
AIN2/GPIO2
AIN3/GPIO3
AIN4/GPIO4
4:1 MX
PGA
A_V = 0.25, 0.5, 1.0, 2.0
SYSTEM ADC
18:1 MX
V_{DD}
WO1–4
WE1–4
RE1–4
CE1–4
GND
TEMPERATURE SENSOR + ADC
DC
RE
IM
EIS ADC
WE1_DC
WE2_DC
WE3_DC
WE4_DC
4:1 MX
2:1 MX
W AMP
+
–
4:1 MX
WE1
WE2
WE3
WE4
DACA
DACB
DACC
DACD
4:1 MX
+
+
EIS SRB
EIS SC
RE1
RE2
RE3
RE4
C AMP
CE1
CE2
CE3
CE4
CE1_DC
CE2_DC
CE3_DC
CE4_DC
EIS CHANNEL
FIFO, CONTROL LOGIC AND REGISTERS
TO FIFO
SERIAL INTERFACE
CSB
DIN
SCLK
DOUT
INTB
GND
12-BIT DAC
DACA
12-BIT DAC
DACB
12-BIT DAC
DACC
12-BIT DAC
DACD
SENSOR ADC
WE1_DC
WO1
4:1 MX
W AMP
SWA
SWB
SENSOR DETECT
SRA
SRB
SC
C AMP
4:1 MX
CE1_DC
CH 1
CH 2
CH 3
CH 4
WE1
WE2
WE3
WE4
RE1
RE2
RE3
RE4
CE1
CE2
CE3
CE4

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Absolute Maximum Ratings

V_{DD} to GND	-0.3V to +5.5V
Analog Pins to GND	-0.3V to (V_{DD} + 0.3V)
Digital Pins to GND	-0.3V to (V_{DD} + 0.3V)
Maximum Current at Any Pin	±20mA
Junction Temperature	+150°C
Operating Temperature Range	0°C to +70°C
Storage Temperature Range	-40°C to +150°C
Soldering Temperature WLP (reflow)	+260°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Package Information

25-Bump WLP 0.5mm Pitch

Package Code	W25202+1
Outline Number	21-100305
Land Pattern Number	Refer to ***Application Note 1891***
Thermal Resistance, Four-Layer Board:	
Junction to Ambient (θ_{JA})	47°C/W

For the latest package outline information and land patterns (footprints), go to ***www.maximintegrated.com/packages***. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to ***www.maximintegrated.com/thermal-tutorial***.

Electrical Characteristics

(V_{DD} = 3.3V, V_{REF} = 1.536V, C_{REG} = 1µF, C_{REF} = 500pF, WE = 1.2V, CE = 0.6V, CE shorted to RE, T_A = 0°C to +70°C, unless otherwise noted.), (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
WE CHARACTERISTICS						
Resolution				12		bits
Integral Nonlinearity	INL	I_{LOAD} = 20µA,18 < DAC Code < 4095		±0.5	±2	LSB
Differential Nonlinearity	DNL	I_{LOAD} = 20µA,18 < DAC Code < 4095			±1	LSB
Gain Error		DAC code = 4095			0.5	%
Offset Error		DAC code = 266		±0.5	±3.5	mV
Offset Drift		DAC code = 266		15		µV/°C
Voltage Accuracy		DAC code = 0xFFF, REF_MODE = 0	-1		+1	%
Maximum Output Voltage		CP_EN = 0, Guaranteed by DC PSR			V_{DD} - 1.1	V
		CP_EN = 1, Guaranteed by DC PSR			V_{DD} - 0.7	
Minimum Output Voltage		Sn_OFFSET_SEL[2:0] = 0, I_{LOAD} = 20µA	0.01			V
		Sn_OFFSET_SEL[2:0] ≠ 0	0.250			
DC Power Supply Rejection		1.73V < V_{DD} < 5.0V, WE = 0.63V, Sn_CP_EN = 0			200	µV/V
		1.73V < V_{DD} < 5.0V, WE = 1.03V, Sn_CP_EN = 1			200	
Load Regulation		0µA < I_{LOAD} < 50µA			10	µV/µA

Electrical Characteristics (continued)

(V_{DD} = 3.3V, V_{REF} = 1.536V, C_{REG} = 1μF, C_{REF} = 500pF, WE = 1.2V, CE = 0.6V, CE shorted to RE, T_A = 0°C to +70°C, unless otherwise noted.), (Note 1)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Output Voltage Rise Time		WE rises from 10% to 90% of V_{REF}			500		μs
Output Voltage Noise		0.1Hz to 10Hz			72		μV_{P-P}
Output Drive Current		WE shorted to WO, $\Delta V_{WE} < \pm 5mV$	Sourcing	50			μA
			Sinking	50			
		Sn_ILIM_EN = 1	Sourcing, R_L = 0Ω	25		60	
Output Off Leakage Current		WE voltage = V_{REF} - 1LSB, T_A = 25°C			±10	±100	pA
		WE voltage = 0.2V, T_A = 25°C			±10	±100	
WE DC-Series Resistance	RS_{DC}			40	60	80	kΩ
WO Switch Resistance				600	1350	2100	Ω
Charge Injection on Switches					±40		pC
Turn-On Time		Settle within 0.5 LSB			10		ms
RE CHARACTERISTICS							
Input Voltage Range		CP_EN = 0, guaranteed by CE DC PSR and INL		0.1		V_{DD} - 1.1	V
		CP_EN = 1, guaranteed by CE DC PSR and INL		0.1		V_{DD} - 0.7	
Input Bias Current		RE voltage = V_{REF} - 1 LSB, T_A = 25°C			±10	±100	pA
		RE voltage = 0.2V, T_A = 25°C			±10	±100	
Charge Injection on Switches					±10		pC
CE CHARACTERISTICS							
Resolution					12		bits
Integral Nonlinearity	INL	I_{LOAD} = 20μA, 0.1 < V_{OUT} < V_{REF} - 1LSB			±0.5	±2	LSB
Differential Nonlinearity	DNL	I_{LOAD} = 20μA, 0.1 < V_{OUT} < V_{REF} - 1LSB				±1	LSB
Gain Error		DAC code = 4095				0.5	%
Offset Error		DAC code = 266			±0.5	±3.5	mV
Offset Drift		DAC code = 266			< 5		μV/°C
Voltage Accuracy		DAC code = 0xFFF, REF_MODE = 0		-1		+1	%
Output Voltage Range		I_{LOAD} = 20μA	CP_EN = 0	0.1		V_{DD} - 1.1	V
			CP_EN = 1	0.1		V_{DD} - 0.7	
DC Power Supply Rejection		1.73V < V_{DD} < 5V, CE = 0.63V, CP_EN = 0				200	μV/V
		1.73V < V_{DD} < 5V, CE = 1.03V, CP_EN = 1				200	
Load Regulation		-50μA < I_{LOAD} < +50μA				10	μV/μA

Electrical Characteristics (continued)

(V_{DD} = 3.3V, V_{REF} = 1.536V, C_{REG} = 1µF, C_{REF} = 500pF, WE = 1.2V, CE = 0.6V, CE shorted to RE, T_A = 0°C to +70°C, unless otherwise noted.), (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Output Voltage Rise Time		CE rises from 10% to 90% of V_{REF}		500		µs
Output Voltage Noise		0.1Hz to 10Hz		72		$µV_{P-P}$
Output Drive Current		Sourcing	50			µA
		Sinking	50			
Charge Injection on Switches				±10		pC
Turn-On Time		Settle within 0.5 LSB		10		ms
SENSOR ADC						
Resolution				16		bits
Integral Nonlinearity	INL	Sn_FSR[2:0] = 500nA		± 4		LSB
Offset Error		Sn_FSR[2:0] = 2000nA, I_{IN} = 0nA, (Note 4, TOC15)			±10	LSB
		Sn_FSR[2:0] = 1000nA, I_{IN} = 0nA, (Note 4, TOC15)			±10	
		Sn_FSR[2:0] = 500nA, I_{IN} = 0nA, (TOC15, TOC32)			±10	
		Sn_FSR[2:0] = 250nA, I_{IN} = 0nA, (TOC15, TOC32)			±20	
		Sn_FSR[2:0] = 100nA, I_{IN} = 0nA, (TOC15, TOC32)			±40	
		Sn_FSR[2:0] = 50nA, I_{IN} = 0nA, (TOC15, TOC32)			±80	
Gain Error (Current Accuracy)		Sn_FSR[2:0] = 2000nA, I_{IN} = 0.9FS at T_A = 25ºC, (Note 4, TOC16, TOC33)		±0.2	±2	%
		Sn_FSR[2:0] = 1000nA, I_{IN} = 0.9FS at T_A = 25ºC, (Note 4, TOC16, TOC33)		±0.2	±2	
		Sn_FSR[2:0] = 500nA, I_{IN} = 0.9FS at T_A = 25ºC, (TOC16, TOC33)		±0.2	±1	
		Sn_FSR[2:0] = 250nA, I_{IN} = 0.9FS at T_A = 25ºC, (TOC16, TOC33)		±0.2	±1	
		Sn_FSR[2:0] = 100nA, I_{IN} = 0.9FS at T_A = 25ºC, (TOC16, TOC33)		±0.2	±2	
		Sn_FSR[2:0] = 50nA, I_{IN} = 0.9FS at T_A = 25ºC, (TOC16, TOC33)		±0.2	±2	
Offset Drift		Sn_FSR[2:0] = 500nA, I_{IN} = 0nA		0.08		LSB/°C
		Sn_FSR[2:0] = 50nA, I_{IN} = 0nA		0.4		
Gain Drift		Sn_FSR[2:0] = 500nA, I_{IN} = 0.9FS		10		LSB/°C
		Sn_FSR[2:0] = 50nA, I_{IN} = 0.9FS		20		
Channel-to-Channel Offset Matching		Sn_FSR[2:0] = 500nA, I_{IN} = 0nA		±0	10	LSB
		Sn_FSR[2:0] = 50nA, I_{IN} = 0nA		±0.7		

Electrical Characteristics (continued)

(V_{DD} = 3.3V, V_{REF} = 1.536V, C_{REG} = 1µF, C_{REF} = 500pF, WE = 1.2V, CE = 0.6V, CE shorted to RE, T_A = 0°C to +70°C, unless otherwise noted.), (Note 1)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Channel-to-Channel Gain Matching		Sn_FSR[2:0] = 500nA, I_{IN} = 0.9FS at T_A = 25ºC				±2	%
		Sn_FSR[2:0] = 50nA, I_{IN} = 0.9FS at T_A = 25ºC				±4	
DC Power Supply Rejection	PSR	Sn_FSR[2:0] = 500nA, I_{IN} = 0.9FS, 1.73V < V_{DD} < 5V		-1000	±40	+1000	pA/V
		Sn_FSR[2:0] = 50nA, I_{IN} = 0.9FS, 1.73V < V_{DD} < 5V		-250	±10	+250	
Signal-to-Noise	SNR	Sn_FSR[2:0] = 500nA, I_{IN} = 0.9FS, Integration time = 1.6s			+95		dB
		Sn_FSR[2:0] = 50nA, I_{IN} = 0.9FS, Integration time = 1.6s			+90		
Channel-to-Channel Crosstalk					-80		dB
					-80		
ADC Conversion Time Range	INT	CLKSEL = 34.95233kHz		0.1		240	s
		CLKSEL = 40.96kHz		0.1		205	
ADC Full Range	I_{WE}	Sn_FSR[2:0] = 000			50		nA
		Sn_FSR[2:0] = 001			100		
		Sn_FSR[2:0] = 010			250		
		Sn_FSR[2:0] = 011		490	500	510	
		Sn_FSR[2:0] = 100			1000		
		Sn_FSR[2:0] = 101			2000		
Offset Current		Sn_FSR [2:0] = 500nA	Sn_OFFSET_SEL [2:0] = 1	9	10	11	%FS
			Sn_OFFSET_SEL [2:0] = 2	18	20	22	
			Sn_OFFSET_SEL [2:0] = 3	45	50	55	
			Sn_OFFSET_SEL [2:0] = 4	7	9	11	nA
			Sn_OFFSET_SEL [2:0] = 5	16	19	22	
			Sn_OFFSET_SEL [2:0] = 6	34	40	46	
			Sn_OFFSET_SEL [2:0] = 7	67	80	93	
EIS CHARACTERISTICS							
Stimulus Frequency Range	f_{STIM}	EIS_FINE_FREQ[3:0] = 0, Accuracy < ±2%		0.0195		20,000	Hz
		EIS_FINE_FREQ[3:0] ≠ 0, Accuracy < ±4%, T_A = 25°C		0.0138		27,085	
Number of Stimulus Cycles	N_S	Set by EIS_NUM_SINEWAVES[2:0]		1		128	

Electrical Characteristics (continued)

(V_{DD} = 3.3V, V_{REF} = 1.536V, C_{REG} = 1µF, C_{REF} = 500pF, WE = 1.2V, CE = 0.6V, CE shorted to RE, T_A = 0°C to +70°C, unless otherwise noted.), (Note 1)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Number of Wait Cycles	N_W	Set by EIS_SETTLE[3:0]		0		15	
Stimulus Voltage Amplitude		Minimum		4	5	6	mV_{P-P}
		Maximum		78	80	82	
		Step Size			5		
WEn Total Harmonic Distortion		V_{P-P} = ±40mV, f_{STIM} = 1.25kHz, T_A = 25°C, N_W = 8		-40	-50		dB
WE/RE Voltage Range		Guaranteed by PSR				V_{DD} - 1.1	V
		Guaranteed by phase and magnitude accuracy, WE = CE = 0.29V, (Note 3)		0.25			
CE Voltage Range		Guaranteed by PSR (Note 2)				V_{DD} - 0.25	V
		Guaranteed by phase and magnitude accuracy, WE = CE = 0.29V, (Note 3)		0.25			
WE EIS Series Resistance	RS_{EIS}			100	150	235	Ω
WE Output Drive Current		Sn_ILIM_EN = 1, sourcing	EIS_ADC_FS_RANGE[1:0] = 00	5	7	10	µA
		Sn_ILIM_EN=1, sourcing	EIS_ADC_FS_RANGE[1:0] = 01	10	13	16	
		Sn_ILIM_EN = 1, sourcing	EIS_ADC_FS_RANGE[1:0] = 10	21	27	32	
			EIS_ADC_FS_RANGE[1:0] = 11	35	44	54	
		Sn_ILIM_EN = 0, sourcing		250			
		Sinking	EIS_ADC_FS_RANGE[1:0] = 00	2.5	3	3.5	
			EIS_ADC_FS_RANGE[1:0] = 01	5	6	7	
			EIS_ADC_FS_RANGE[1:0] = 10	12.5	15	17.5	
			EIS_ADC_FS_RANGE[1:0] = 11	25	30	35	
CE Output Drive Current		ΔV_{CE} < ±5mV		-50		+50	µA
EIS ADC							
Resolution					16		bits
EIS ADC FS		EIS_ADC_FS_RANGE[1:0] = 00			4		$µA_{P-P}$
		EIS_ADC_FS_RANGE[1:0] = 01			8		
		EIS_ADC_FS_RANGE[1:0] = 10			20		
		EIS_ADC_FS_RANGE[1:0] = 11, T_A = 25°C		39.2	40	40.8	

Electrical Characteristics (continued)

(V_{DD} = 3.3V, V_{REF} = 1.536V, C_{REG} = 1µF, C_{REF} = 500pF, WE = 1.2V, CE = 0.6V, CE shorted to RE, T_A = 0°C to +70°C, unless otherwise noted.), (Note 1)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Impedance Conversion Time		Measured at WE, N_W = 0			$2^N/f_{STIM}$ + $3584/f_{FAST}$		s
Phase Measurement Accuracy		WE = 0.63V, T_A = 25°C (Note 3)			±0.5	±1.5	Degrees
Magnitude Measurement Accuracy		WE = 0.63V, T_A = 25°C (Note 3)			±0.5	±1.5	%
DC Power Supply Rejection	PSR	1.73V < V_{DD} < 5V, WE = 0.63V, T_A = 25°C (Note 3)		-0.6		+0.6	%/V
		1.73V < V_{DD} < 5V, WE = 0.63V, T_A = 25°C (Note 3)		-0.1		+0.1	Degrees/V
Signal-to-Noise	SNR	(Note 3)			+80		dB
CV AND SWV CHARACTERISTICS							
V_{STEP} Range		Set by (EIS_DAC_INC[3:0] + 1) x V_{REF} / 2^{12}		0.4		1.6	mV
T_{STEP} Range		Set by EIS_CLK_DIV[4:0]	EIS_INTG = 50µs	0.8		6.4	ms
			EIS_INTG = 200µs	1.6		6.4	
SWV Amplitude Range	V_{AMP}	Set by EIS_AMPLITUDE[3:0]		±2.5		±40	mV
SWV Frequency Range	f_{SWV}	Set by EIS_CLK_DIV[4:0]	EIS_INTG = 50µs	156		1250	Hz
			EIS_INTG = 200µs	156		625	
SYSTEM ADC							
Resolution					12		bits
Integral Nonlinearity	INL	(*TOC36*)				±1.5	LSB
Differential Nonlinearity	DNL	(*TOC37*)				±1.5	LSB
Gain Error		V_{IN} = 0.9FS, GA = 1			±0.05	±1	%
Gain Drift		V_{IN} = 0.9FS, GA = 1			±0.01		%/°C
Power Supply Rejection	PSR	1.73V < V_{DD} < 5V, V_{IN} = 0.9FS, GA = 1		-6		+6	mV/V
Signal-to-Noise	SNR	Input voltage = 0.9FS, GA = 1			80		dB
Conversion Time					8.5		ms
Full Scale Reference				0		V_{REF}	V
Input Voltage Range				0		V_{REF}/GA	V
Programmable Gain	GA				2		V/V
					1		
					0.5		
					0.25		
SAMPLE RATE CLOCK							
Sample Rate Clock	f_{SLOW}	SCLK = 0, Sn_FSR[2:0] ≤ 500nA		-2% of typ	34.952	+2% of typ	kHz
		SCLK = 1, Sn_FSR[2:0] ≤ 500nA		-2% of typ	40.96	+2% of typ	

Electrical Characteristics (continued)

(V_{DD} = 3.3V, V_{REF} = 1.536V, C_{REG} = 1μF, C_{REF} = 500pF, WE = 1.2V, CE = 0.6V, CE shorted to RE, T_A = 0°C to +70°C, unless otherwise noted.), (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Minimum Free Running Sample Rate		SENS_PERIOD[3:0] = 0xA		0.004		SPS
Maximum Free Running Sample Rate		SENS_PERIOD[3:0] = 0x0		10		SPS
System ADC Clock	f_{MED}		-2% of typ	128	+2% of typ	kHz
EIS ADC Clock	f_{FAST}		-2% of typ	10.24	+2% of typ	MHz
EXTERNAL CLOCK						
External Sample Rate Clock Frequency				32.768		kHz
VOLTAGE REFERENCE (V_{REF})						
Reference Output Voltage		RVAL[1:0] = 00, (*TOC18*)	1.521	1.536	1.551	V
		RVAL[1:0] = 01, (*TOC18*)	2.028	2.048	2.068	
		RVAL[1:0] = 10, (*TOC18*)	3.042	3.072	3.102	
		RVAL[1:0] = 11, (*TOC18*)	4.035	4.096	4.157	
Output Voltage Temperature Drift				10		ppm/°C
Line Regulation		1.73V < V_{DD} < 5V		±5	±100	μV/V
Load Regulation		Source 100μA		15	35	μV/μA
Short-Circuit Current		Source		30		mA
Output Voltage Noise		0.1Hz–10Hz		10		μV_{RMS}
Turn-On Time		Settle to 0.1%		4		ms
V_{REF} Capacitance					500	pF
EXTERNAL REFERENCE						
External Voltage Reference Range			1.536		4.096	V
Input Impedence		DAC and System ADC enabled	4.8	6.4	8.3	MΩ
TEMPERATURE SENSOR						
Temperature Measurement Error		+30°C to +50°C, ±3 sigma	-0.5		+0.5	°C
		+0°C to +70°C, ±3 sigma (*TOC38*)	-1		+1	
Resolution		16-Bit		1/195		°C
Repeatability		16-Bit, (*TOC17*)		0.008		$°C_{RMS}$
Conversion Time	t_{CONV}	16-Bit		15	16	ms
Response Time		Mounted, 63%, (Note 5)		3.5		s
SENSOR DETECT CHARACTERISTICS						
Current Threshold	I_{DETECT}	Sn_DETECTOR_THRESHOLD[1:0] = 0	14.3	22.3	30.4	nA
		Sn_DETECTOR_THRESHOLD[1:0] = 1	28.8	44.7	60.5	
		Sn_DETECTOR_THRESHOLD[1:0] = 2	57.8	89.3	120.8	
		Sn_DETECTOR_THRESHOLD[1:0] = 3	115.7	178.6	241.5	

Electrical Characteristics (continued)

(V_{DD} = 3.3V, V_{REF} = 1.536V, C_{REG} = 1µF, C_{REF} = 500pF, WE = 1.2V, CE = 0.6V, CE shorted to RE, T_A = 0°C to +70°C, unless otherwise noted.), (Note 1)

<table>
<tr><th>PARAMETER</th><th>SYMBOL</th><th colspan="2">CONDITIONS</th><th>MIN</th><th>TYP</th><th>MAX</th><th>UNITS</th></tr>
<tr><td>Trigger Delay</td><td></td><td colspan="2"></td><td></td><td>$4592/f_{SLOW}$</td><td></td><td>ms</td></tr>
<tr><td rowspan="4">Sensor Detect Bias Voltage</td><td rowspan="4">V_{DETECT}</td><td colspan="2">DETECTOR_BIAS[1:0] = 00, Sn_DET = 0</td><td>175.6</td><td>221.5</td><td>267.4</td><td rowspan="4">mV</td></tr>
<tr><td colspan="2">DETECTOR_BIAS[1:0] = 01, Sn_DET = 0</td><td>382.2</td><td>443</td><td>503.8</td></tr>
<tr><td colspan="2">DETECTOR_BIAS[1:0] = 10, Sn_DET = 0</td><td>589.3</td><td>664.5</td><td>739.6</td></tr>
<tr><td colspan="2">DETECTOR_BIAS[1:0] = 11, Sn_DET = 0</td><td>795.9</td><td>885.9</td><td>976</td></tr>
<tr><td colspan="8">POWER SUPPLY</td></tr>
<tr><td>Power Supply Voltage</td><td>V_{DD}</td><td colspan="2">Verified during PSRR Test</td><td>1.73</td><td></td><td>5</td><td>V</td></tr>
<tr><td colspan="8">POWER SUPPLY / DC BIAS MODE</td></tr>
<tr><td rowspan="5">V_{DD} Supply Current</td><td rowspan="5">I_{DD}</td><td colspan="2">DACA_EN = 1, S1_WE_AMP_EN = 1, S1_CE_AMP_EN = 1, T_A = 25°C, (<i>TOC23</i>)</td><td></td><td>3.5</td><td>7</td><td rowspan="5">µA</td></tr>
<tr><td colspan="2">DACA_EN = 1, S1_WE_AMP_EN = 1, S1_CE_AMP_EN = 1, (<i>TOC23</i>)</td><td></td><td></td><td>14</td></tr>
<tr><td rowspan="2">MAX30134</td><td>DACx_EN = 1, Sx_WE_AMP_EN = 1, Sx_CE_AMP_EN = 1, T_A = 25°C</td><td></td><td>5.75</td><td>9.5</td></tr>
<tr><td>DACx_EN = 1, Sx_WE_AMP_EN = 1, Sx_CE_AMP_EN = 1</td><td></td><td></td><td>16.5</td></tr>
<tr><td colspan="2">per additional DAC channel, T_A = 25°C</td><td></td><td>0.2</td><td></td></tr>
<tr><td>V_{DD} Supply Current</td><td>I_{DD}</td><td colspan="2">per additional WE amplifier, T_A = 25°C</td><td></td><td>0.2</td><td></td><td>µA</td></tr>
<tr><td>V_{DD} Supply Current</td><td>I_{DD}</td><td colspan="2">per additional CE amplifier, T_A = 25°C</td><td></td><td>0.3</td><td></td><td>µA</td></tr>
</table>

Electrical Characteristics (continued)

(V_{DD} = 3.3V, V_{REF} = 1.536V, C_{REG} = 1µF, C_{REF} = 500pF, WE = 1.2V, CE = 0.6V, CE shorted to RE, T_A = 0°C to +70°C, unless otherwise noted.), (Note 1)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
POWER SUPPLY / DC MEASUREMENT MODE (CURRENT DURING CONVERSION)							
V_{DD} Supply Current	I_{DD}	DACA_EN = 1, S1_WE_AMP_EN = 1, S1_CE_AMP_EN = 1, T_A = 25°C			7.3	11	µA
		DACA_EN = 1, S1_WE_AMP_EN = 1, S1_CE_AMP_EN = 1				18.5	
		DACx_EN = 1, S1_WE_AMP_EN = 1, S1_CE_AMP_EN = 1, S2_WE_AMP_EN = 1, S2_CE_AMP_EN = 1, T_A = 25°C			10.5	15	
		DACx_EN = 1, S1_WE_AMP_EN = 1, S1_CE_AMP_EN = 1, S2_WE_AMP_EN = 1, S2_CE_AMP_EN = 1				21.5	
		DACx_EN = 1, Sn_WE_AMP_EN = 1, Sn_CE_AMP_EN = 1, T_A = 25°C			15.3	21	
		DACx_EN = 1, Sn_WE_AMP_EN = 1, Sn_CE_AMP_EN = 1				27.5	
POWER SUPPLY / EIS MEASUREMENT MODE							
V_{DD} Supply Current	I_{DD}	DACA_EN = 1, S1_WE_AMP_EN = 1, S1_CE_AMP_EN = 1, EIS_ADC_FS = 20µA, EIS_CLK_DIV = 0x0B (80Hz), EIS_AMPLITUDE = 40mV_{P-P}, I_{LOAD} = 1µA, (*TOC27*)			950	1300	µA
		DACA_EN = 1, S1_WE_AMP_EN = 1, S1_CE_AMP_EN = 1, EIS_ADC_FS = 20µA, EIS_CLK_DIV = 0x07 (1.25kHz), EIS_AMPLITUDE = 40mV_{P-P}, I_{LOAD} = 1µA, (*TOC27*)			1300	1750	
POWER SUPPLY / SYSTEM (CURRENT DURING CONVERSION)							
V_{DD} Supply Current	I_{DD}	System ADC mode, during conversion, (*TOC28*)			18.4	28	µA
	I_{DD}	Die temperature mode, operation current, (*TOC29*)			96	135	µA
	I_{DD}	Single sensor detect active, T_A = 25°C, (*TOC30*)			1.2	4	µA
		Single sensor detect active, (*TOC30*)				12.5	
		Shutdown (*TOC31*)	T_A = 25°C		1	3.8	
						12.5	
Out Of Range V_{DD} Threshold–Low Side	OOR				1.6		V
Out Of Range V_{DD} Threshold–High Side	OOR				5.2		V
DIGITAL I/O CHARACTERISTICS							
Input Leakage Current	I_{IN}	V_{IN} = 0V, T_A = +25°C (SDI, SCLK, CSB, GPIOx)			10	100	nA
		V_{IN} = V_{DD}, T_A = +25°C (SDI, SCLK, CSB, GPIOx)			10	100	

Electrical Characteristics (continued)

(V_{DD} = 3.3V, V_{REF} = 1.536V, C_{REG} = 1µF, C_{REF} = 500pF, WE = 1.2V, CE = 0.6V, CE shorted to RE, T_A = 0°C to +70°C, unless otherwise noted.), (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
SDO Output Low Voltage	V_{OL_SDO}	I_{SINK} = 2mA			0.4	V
SDO Output High Voltage	V_{OH_SDO}	I_{SOURCE} = 2mA	V_{DD} - 0.4			V
Open Drain Output Low Voltage	V_{OL_OD}	I_{SINK} = 6mA, INTB, GPIOx			0.4	V
Input Voltage Low	V_{IL}	SDI, SCLK, CSB, GPIO			0.4	V
Input Voltage High	V_{IH}	SDI, SCLK, CSB, GPIO	V_{DD} - 0.4			V
Input Hysteresis	V_{HYS}	SDI, SCLK, CSB, GPIO		340		mV
Input Capacitance	C_{IN}	SDI, SCLK, CSB, GPIO		10		pF
SPI TIMING CHARACTERISTICS (Note 6)						
SCLK Frequency	f_{SCLK}				8	MHz
SCLK Period	t_{CP}		125			ns
SCLK Pulse Width High	t_{CH}		40			ns
SCLK Pulse Width Low	t_{CL}		40			ns
CSB Fall to SCLK Rise Setup Time	t_{CSS0}	to 1st SCLK rising edge	20			ns
CSB Fall to SCLK Rise Hold Time	t_{CSH0}	Applies to inactive rising edge preceding 1st rising edge	5			ns
CSB Rise to SCLK Rise Hold Time	t_{CSH1}	Applies to 24th rising edge	500			ns
SCLK Rise to CSB Fall	t_{CSF}	Applies to 24th rising edge	500			ns
CSB Pulse Width High	t_{CSPW}		250			ns
SDI to SCLK Rise Setup Time	t_{DS}		15			ns
SDI to SCLK Rise Hold Time	t_{DH}		10			ns
SCLK Fall to SDO Transition	t_{DOT}	C_{LOAD} = 50pF			67.5	ns
CSB Fall to SDO Enabled	t_{DOE}	C_{LOAD} = 0pF	25			ns
CSB Rise to SDO Hi-Z	t_{DOZ}	Disable Time			25	ns
GPIO Active Pulse Width	t_{PLGPIO}		1			µs
ESD						
HBM		Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001		±2000		V
CDM		Charged-device model (CDM), per JEDEC specification JESD22- VC101		±750		V
IEC		Per IEC/EN 61000-4-2 (WEn, CEn, REn Only) Contact		±8		kV
		Air		±15		

Note 1: All devices are 100% production tested at T_A = +25°C. Specifications over temperature limits are guaranteed by Maxim Integrated bench or proprietary automated test equipment (ATE) characterization.

Note 2: CE amplifier configured in a non-inverting gain of 2.5 by connecting 100K from RE to CE and 150K from RE to GND.

Note 3: Load is series RC between WE and CE with R_{LOAD} = 3.2kΩ and C_{LOAD} = 100nF, F_{STIM} = 1.25kHz, EIS_AMPLITUDE[3:0] = 7 (±40mV), EIS_NUM_SINEWAVES[2:0] = 3 (average 8 cycles), EIS_ADC_FS_RANGE[1:0] = 3 (40μA). Trimmed using a ±1% tolerance R_{LOAD} and C_{LOAD}.

Note 4: If any Sn_FSR[2:0] > 500nA, all sensor ADC integration times are decreased by 4x.

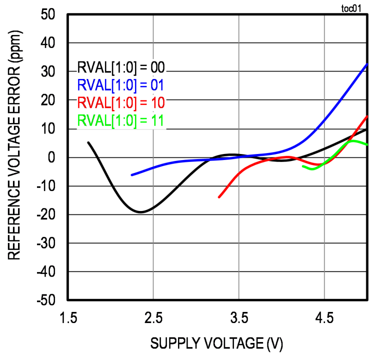
Note 5: Mounted: Part is on 4-layer PCB.

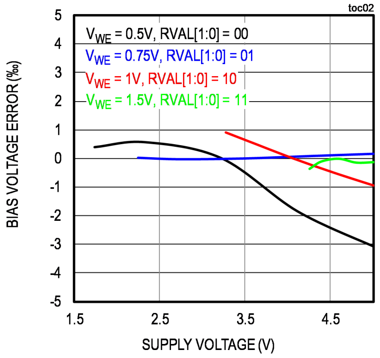
Note 6: Limits guaranteed for 1.73V < V_{DD} < 5.0V.
See timing thresholds:

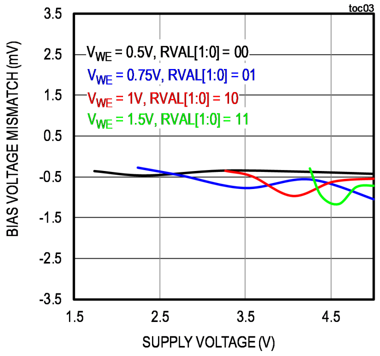
SUPPLY	**V_{OL} (V)**	**V_{OH} (V)**
1.73V < V_{DD} < 1.8V	0.4	V_{DD} - 0.275
1.8V < V_{DD} < 3.3V	0.4	V_{DD} - 0.4
3.3V < V_{DD} < 5.0V	0.5	V_{DD} - 0.4

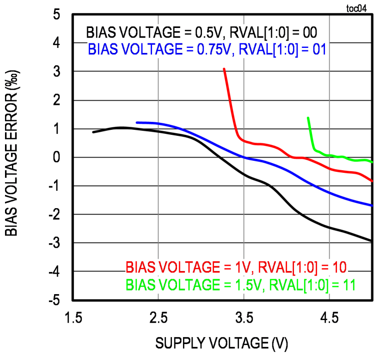
Typical Operating Characteristics

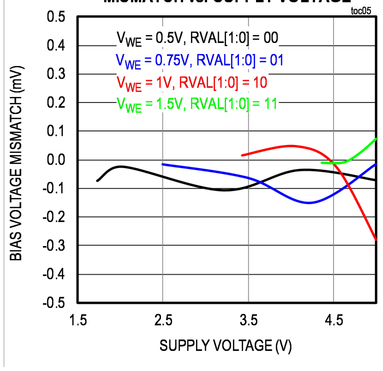
(V_{DD} = 3.3V, V_{REF} = 1.536V, C_{REG} = 1µF, C_{REF} = 500pF, T_A = 25°C, unless otherwise noted.)

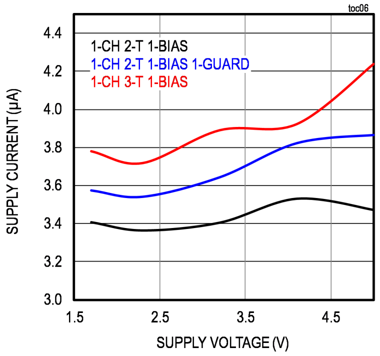

REFERENCE VOLTAGE ERROR vs. SUPPLY VOLTAGE

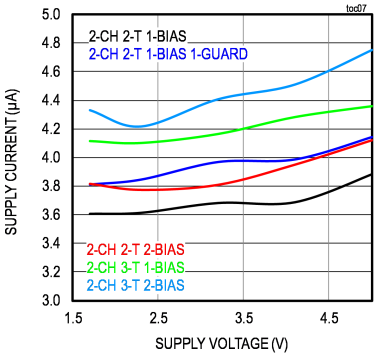

2-TERMINAL BIAS VOLTAGE ERROR vs. SUPPLY VOLTAGE

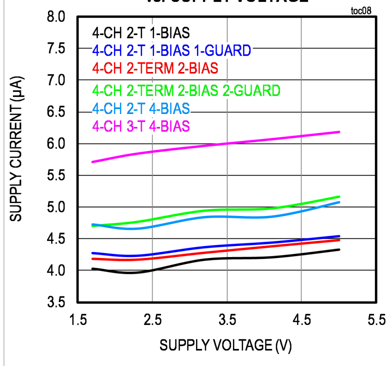

2-TERMINAL BIAS VOLTAGE MISMATCH vs. SUPPLY VOLTAGE

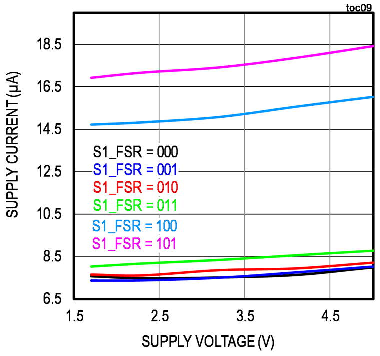

3-TERMINAL BIAS VOLTAGE ERROR vs. SUPPLY VOLTAGE


3-TERMINAL BIAS VOLTAGE MISMATCH vs. SUPPLY VOLTAGE


1-CH BIAS SUPPLY CURRENT vs. SUPPLY VOLTAGE

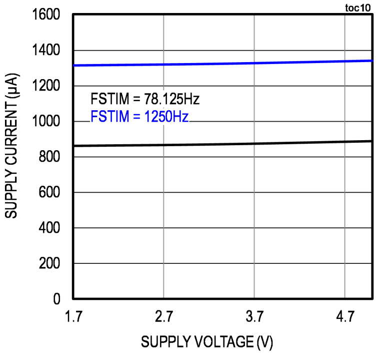

2-CH BIAS SUPPLY CURRENT vs. SUPPLY VOLTAGE

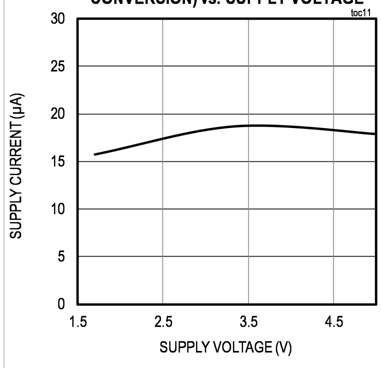

4-CH BIAS SUPPLY CURRENT vs. SUPPLY VOLTAGE

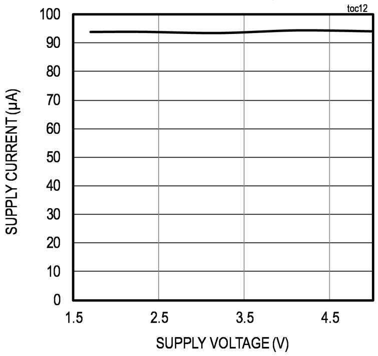

SENSOR DC ADC SUPPLY CURRENT vs. SUPPLY VOLTAGE (S1_OFFSET_SEL = d'6)

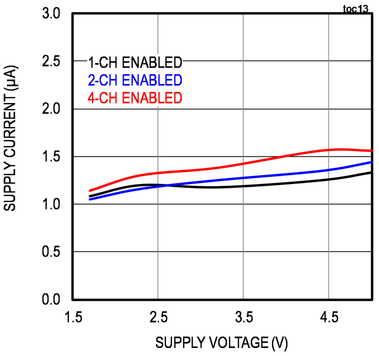
Typical Operating Characteristics (continued)

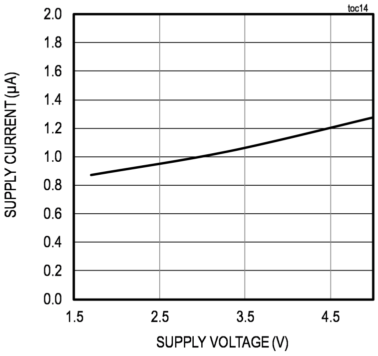
(V_{DD} = 3.3V, V_{REF} = 1.536V, C_{REG} = 1µF, C_{REF} = 500pF, T_A = 25°C, unless otherwise noted.)

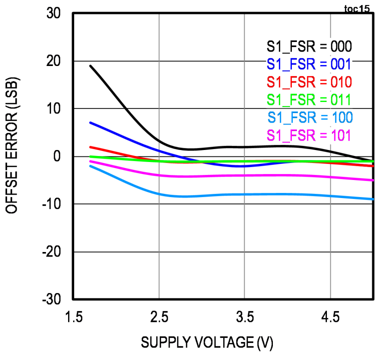

EIS ADC SUPPLY CURRENT (DURING CONVERSION) vs. SUPPLY VOLTAGE

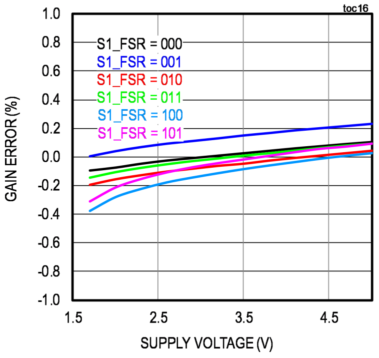

SYS ADC SUPPLY CURRENT (DURING CONVERSION) vs. SUPPLY VOLTAGE

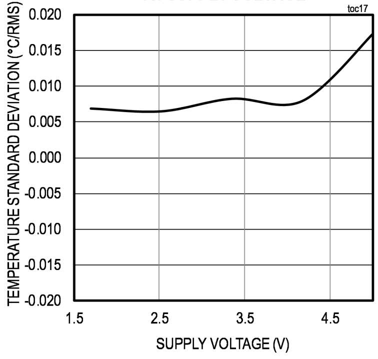

TEMP ADC SUPPLY CURRENT (DURING CONVERSION) vs. SUPPLY VOLTAGE

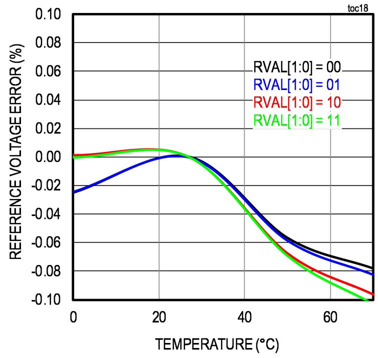

SENSOR DETECT SUPPLY CURRENT vs. SUPPLY VOLTAGE


SHUTDOWN SUPPLY CURRENT vs. SUPPLY VOLTAGE


SENSOR DC ADC OFFSET ERROR vs. SUPPLY VOLTAGE

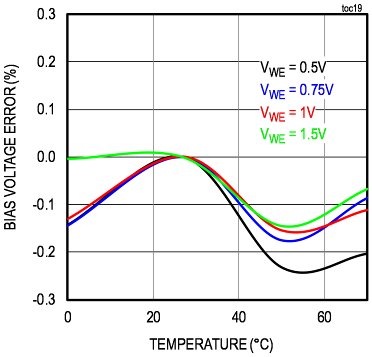

SENSOR DC ADC GAIN ERROR vs. SUPPLY VOLTAGE

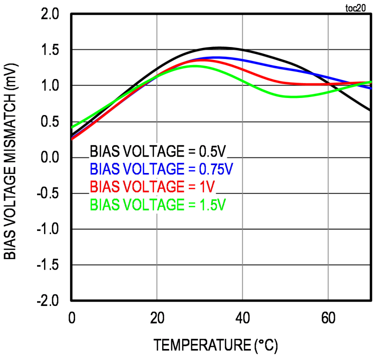

TEMP ADC REPEATABILITY vs. SUPPLY VOLTAGE

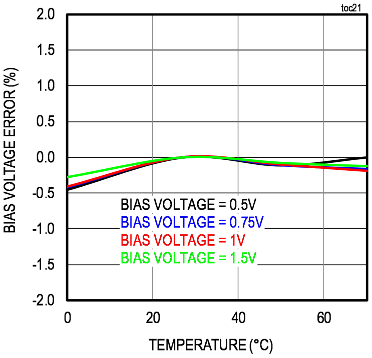

REFERENCE VOLTAGE ERROR vs. TEMPERATURE

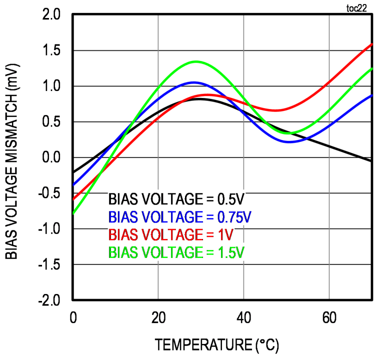
Typical Operating Characteristics (continued)

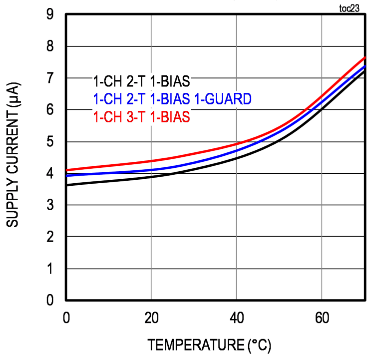
(V_{DD} = 3.3V, V_{REF} = 1.536V, C_{REG} = 1µF, C_{REF} = 500pF, T_A = 25°C, unless otherwise noted.)

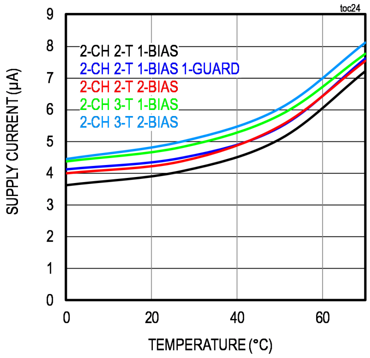

2-TERMINAL BIAS VOLTAGE ERROR vs. TEMPERATURE

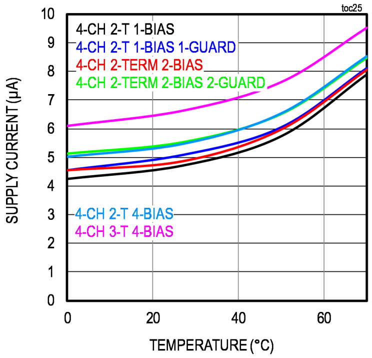

2-TERMINAL BIAS VOLTAGE MISMATCH vs. TEMPERATURE

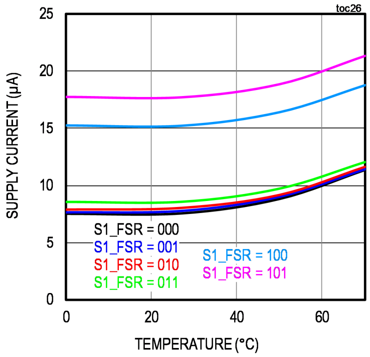

3-TERMINAL BIAS VOLTAGE ERROR vs. TEMPERATURE

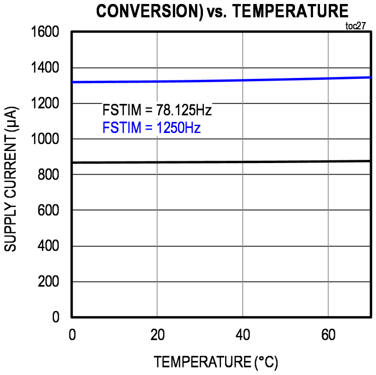

3-TERMINAL BIAS VOLTAGE MISMATCH vs. TEMPERATURE


1-CH BIAS SUPPLY CURRENT vs. TEMPERATURE


2-CH BIAS SUPPLY CURRENT vs. TEMPERATURE


4-CH BIAS SUPPLY CURRENT vs. TEMPERATURE

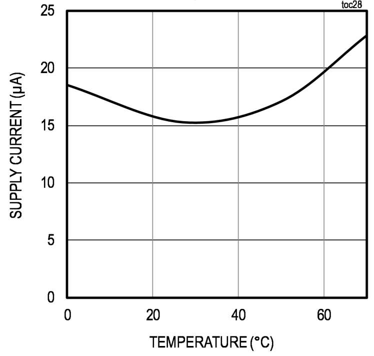

SENSOR DC ADC SUPPLY CURRENT vs. TEMPERATURE. S1_OFFSET_SEL = d'6


EIS ADC SUPPLY CURRENT (DURING CONVERSION) vs. TEMPERATURE

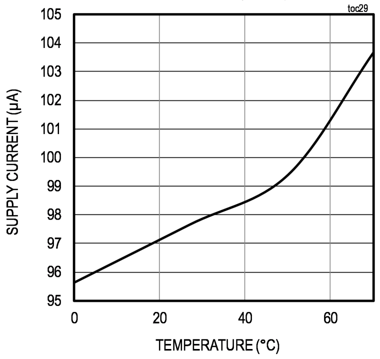
Typical Operating Characteristics (continued)

(V_{DD} = 3.3V, V_{REF} = 1.536V, C_{REG} = 1µF, C_{REF} = 500pF, T_A = 25°C, unless otherwise noted.)

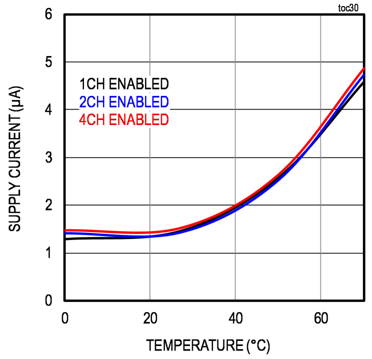
SYS ADC SUPPLY CURRENT (DURING CONVERSION) vs. TEMPERATURE



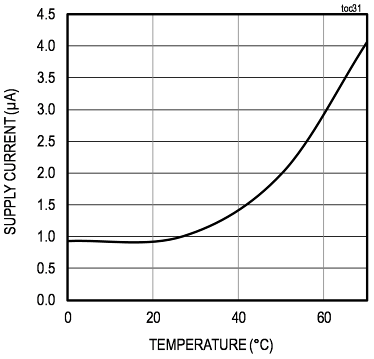
TEMP ADC SUPPLY CURRENT (DURING CONVERSION) vs. TEMPERATURE



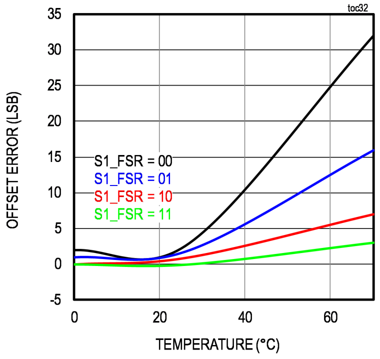
SENSOR DETECT SUPPLY CURRENT vs. TEMPERATURE



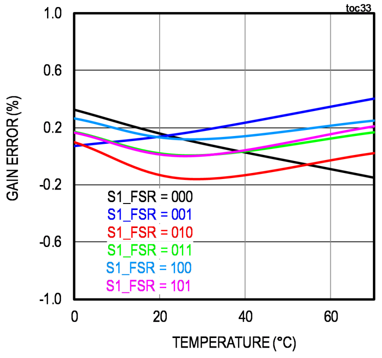
SHUTDOWN SUPPLY CURRENT vs. TEMPERATURE



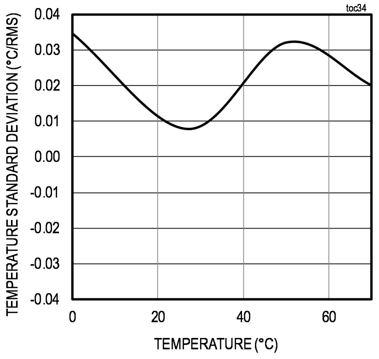
SENSOR DC ADC OFFSET ERROR vs. TEMPERATURE



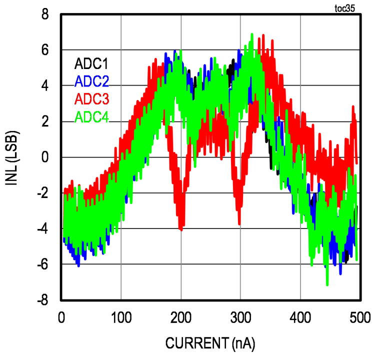
SENSOR DC ADC GAIN ERROR vs. TEMPERATURE



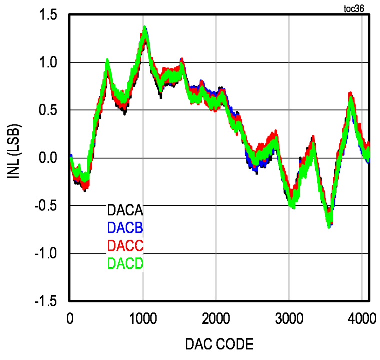
TEMP ADC REPEATABILITY vs. TEMPERATURE



SENSOR DC ADC INL

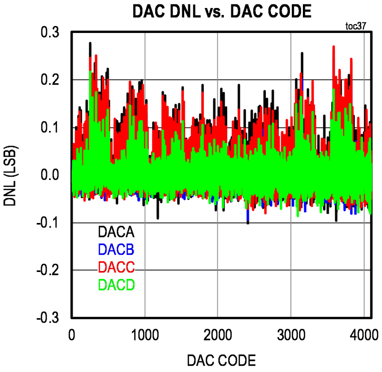


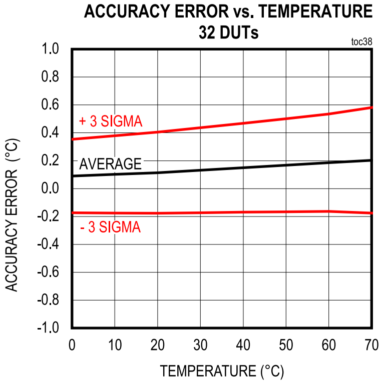
DAC INL vs. DAC CODE



Typical Operating Characteristics (continued)

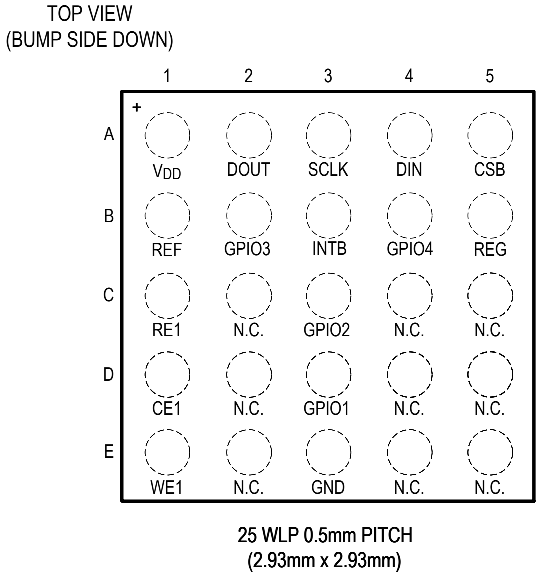
(V_{DD} = 3.3V, V_{REF} = 1.536V, C_{REG} = 1μF, C_{REF} = 500pF, T_A = 25°C, unless otherwise noted.)



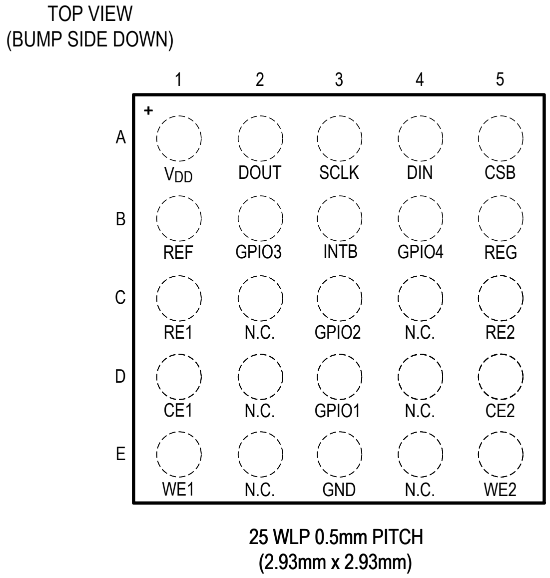


Pin Configurations

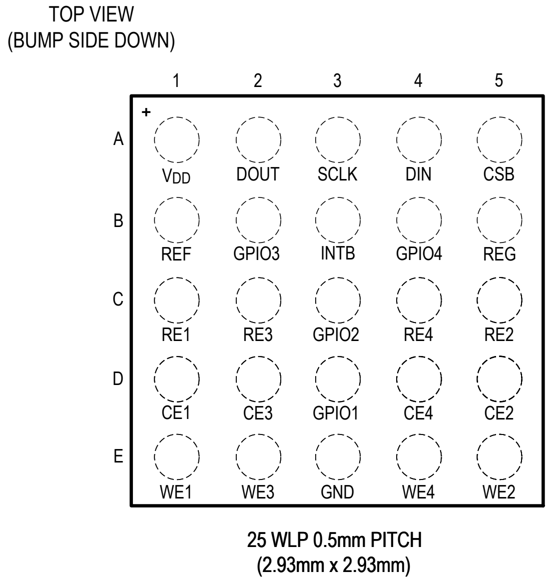
MAX30131



MAX30132



MAX30134



Pin Description

PIN			NAME	FUNCTION
MAX30131	MAX30132	MAX30134		
POWER				
A1	A1	A1	V_{DD}	Analog and Digital Supply Voltage. Connect V_{DD} to an externally regulated supply or battery. Connect a 1µF capacitor in parallel with 0.1µF capacitor between V_{DD} and GND.
E3	E3	E3	GND	Analog and Digital Ground
B5	B5	B5	REG	Linear Regulator Output. For internal use only. Connect a 1µF capacitor between REG and GND.
C5, D5, E5, C2, D2, E2, C4, D4, E4	C2, D2, E2, C4, D4, E4	—	N.C.	Not Connected. Do not connect.
ELECTROCHEMICAL				
E1	E1	E1	WE1	Working Electrode 1. Analog output connected to working electrode of 2- or 3-terminal electrochemical sensor and input to measure current. This bump connection can be alternatively used as a unity gain amplifier output or guard ring output.
C1	C1	C1	RE1	Reference Electrode 1. Analog input connected to reference electrode of 3-terminal electrochemical sensor.
D1	D1	D1	CE1	Counter Electrode 1. Analog output connected to counter electrode of 2- or 3-terminal electrochemical sensor. This connection can be alternatively used as a unity gain amplifier output or guard ring output.
—	E5	E5	WE2	Working Electrode 2. Analog output connected to working electrode of 2- or 3-terminal electrochemical sensor and input to measure current. This bump connection can be alternatively used as a unity gain amplifier output or guard ring output.

Pin Description (continued)

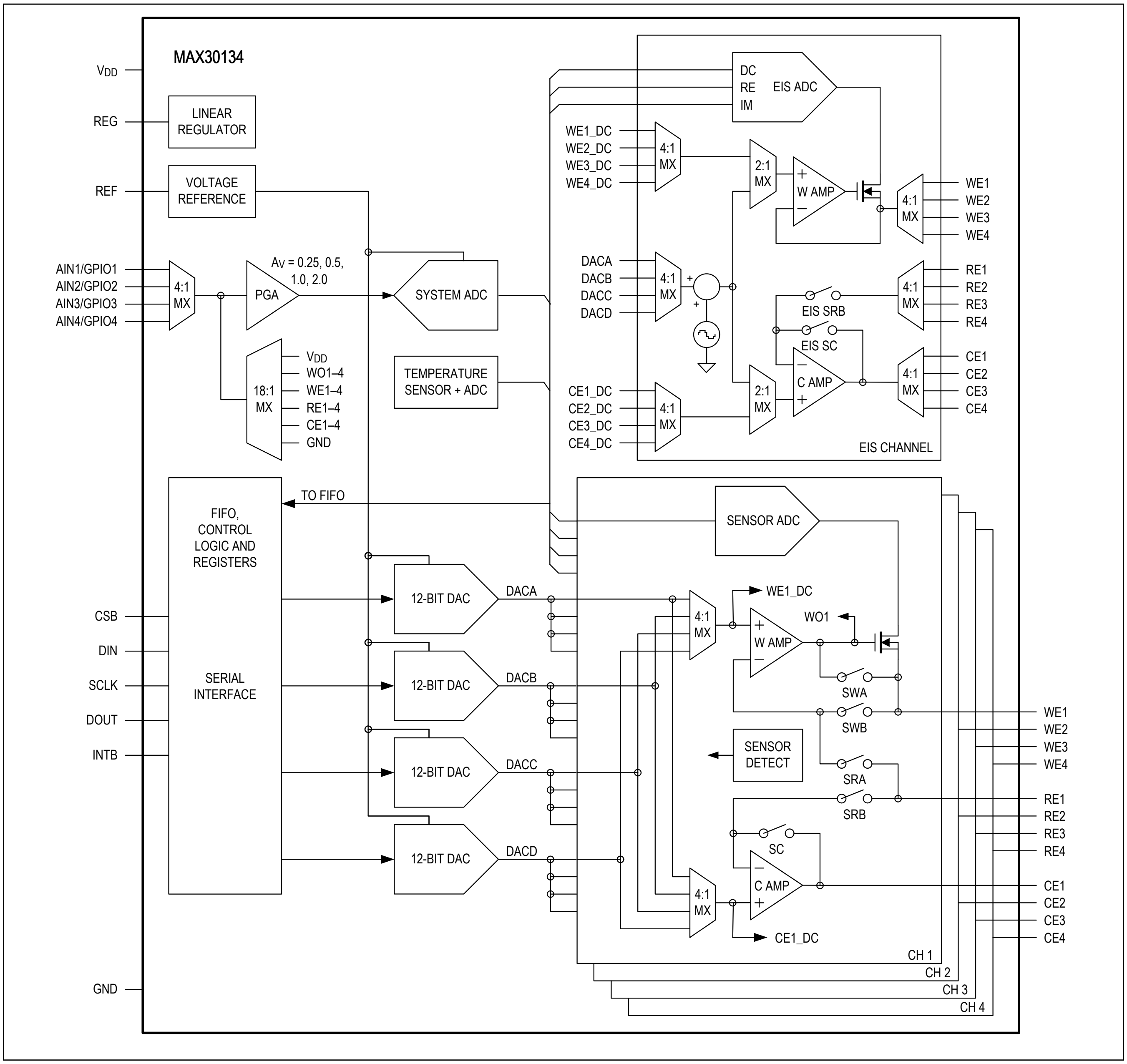
PIN			NAME	FUNCTION
MAX30131	**MAX30132**	**MAX30134**		
—	C5	C5	RE2	Reference Electrode 2. Analog input connected to reference electrode of 3-terminal electrochemical sensor.
—	D5	D5	CE2	Counter Electrode 2. Analog output connected to counter electrode of 2- or 3-terminal electrochemical sensor. This connection can be alternatively used as a unity gain amplifier output or guard ring output.
—	—	E2	WE3	Working Electrode 3. Analog output connected to working electrode of 2- or 3-terminal electrochemical sensor and input to measure current. This bump connection can be alternatively used as a unity gain amplifier output or guard ring output.
—	—	C2	RE3	Reference Electrode 3. Analog input connected to reference electrode of 3-terminal electrochemical sensor.
—	—	D2	CE3	Counter Electrode 3. Analog output connected to counter electrode of 2- or 3-terminal electrochemical sensor. This connection can be alternatively used as a unity gain amplifier output or guard ring output.
—	—	E4	WE4	Working Electrode 4. Analog output connected to working electrode of 2- or 3-terminal electrochemical sensor and input to measure current. This bump connection can be alternatively used as a unity gain amplifier output or guard ring output.
—	—	C4	RE4	Reference Electrode 4. Analog input connected to reference electrode of 3-terminal electrochemical sensor.
—	—	D4	CE4	Counter Electrode 4. Analog output connected to counter electrode of 2- or 3-terminal electrochemical sensor. This connection can be alternatively used as a unity gain amplifier output or guard ring output.
DIGITAL INTERFACE				
B3	B3	B3	INTB	Interrupt Output. INTB is a programmable status output. It can be used to interrupt an external device.
A2	A2	A2	DOUT	Serial Data Output. DOUT changes state on the falling edge of SCLK when CSB is low. DOUT is three-stated when CSB is high.
A3	A3	A3	SCLK	Serial Clock Input. Clocks data in and out of the serial interface when CSB is low.
A4	A4	A4	DIN	Serial Data Input. DIN is clocked into the device on the rising edge of SCLK when CSB is low.
A5	A5	A5	CSB	Active-Low Chip-Select Input. Enables the serial interface.
REFERENCE				
B1	B1	B1	REF	Internal Reference Voltage Output/External Reference Voltage Input. External decoupling capacitor not required. Capacitance from REF to GND must be less than 500pF to be stable.
ANALOG INPUT/GPIO				
D3	D3	D3	AIN1/GPIO1	Analog Input 1 or General Purpose Input/Output 1. Programmable to be an analog input voltage to the system ADC, digital input to directly control internal blocks, or general purpose digital input/output.

Pin Description (continued)

PIN			NAME	FUNCTION
MAX30131	**MAX30132**	**MAX30134**		
C3	C3	C3	AIN2/GPIO2	Analog Input 2 or General Purpose Input/Output 2. Programmable to be an analog input voltage to the system ADC, digital input to directly control internal blocks, or general purpose digital input/output.
B2	B2	B2	AIN3/GPIO3	Analog Input 3 or General Purpose Input/Output 3. Programmable to be an analog input voltage to the system ADC, digital input to directly control internal blocks, or general purpose digital input/output.
B4	B4	B4	AIN4/GPIO4	Analog Input 4 or General Purpose Input/Output 4. Programmable to be an analog input voltage to the system ADC, digital input to directly control internal blocks, or general purpose digital input/output.

Functional Diagrams

Block Diagram



Detailed Description

The MAX30131/MAX30132/MAX30134 electrochemical analog front ends continuously bias up to one, two, or four sensors, respectively at ultra-low power. They measure sensor DC current from the working electrode with a precision,16-bit, current mode, analog to digital converter (ADC) and can perform electrochemical impedance spectroscopy (EIS) measurements up to 27kHz. They have built-in autonomous modes, digital alarms, and can monitor the compliance voltages of the sensor terminals as well as other internal and external voltages with a 12-bit system ADC. An internal temperature sensor measures the die temperature. Data from the sensor ADCs, EIS ADC, system ADC, and temperature sensor are tagged with a unique identifier and stored in a 256-word FIFO. The functional block diagram for the quad-channel version (MAX30134) is shown in the *Block Diagram*.

Serial Interface

The 4-wire serial peripheral interface (SPI) allows access to the internal registers to configure the device as well as read the sensor data, system voltages, and temperature from FIFO memory. A programmable interrupt (INTB) is available to notify the MCU to service the AFE. This can be used to maximize the time that the MCU is in sleep mode, which reduces system power and extends battery life.

Voltage Reference

The internal voltage reference (Figure 1) is programmable from 1.536V to 4.096V using REF_VAL[1:0] (0x68) and is used by the internal DACs and system ADC. V_{DD} must be at least 150mV greater than the selected voltage reference. The internal voltage reference is buffered and brought out to the REF pin so that it can be used by external circuitry, but has limited drive capability. For example, it can be be used to drive an external thermistor provided the current draw is less than 100µA. By setting REF_MODE = 1 (0x68), the buffer is shut down, switch SW is opened, and the internal data converters use the external voltage applied to the REF pin. The voltage applied to the reference pin must be greater than 1.536V and less than 4.096V. With power-on-reset (POR) or soft-reset (RESET = 1 0x14), REF_VAL[1:0] (0x68) defaults to 1.536V. BUF is enabled and SW is closed. After POR or soft-reset, wait at least 12ms for REF to fully settle before making any measurements.

REF_EN (0x68) is provided so that the internal voltage reference and buffer can be turned off independent of shutdown mode. This can be used to reduce power when the sensor detect function is being used. When REF_EN is set to 0, all analog functions are disabled apart from the sensor detect function, which has its own independent bias.

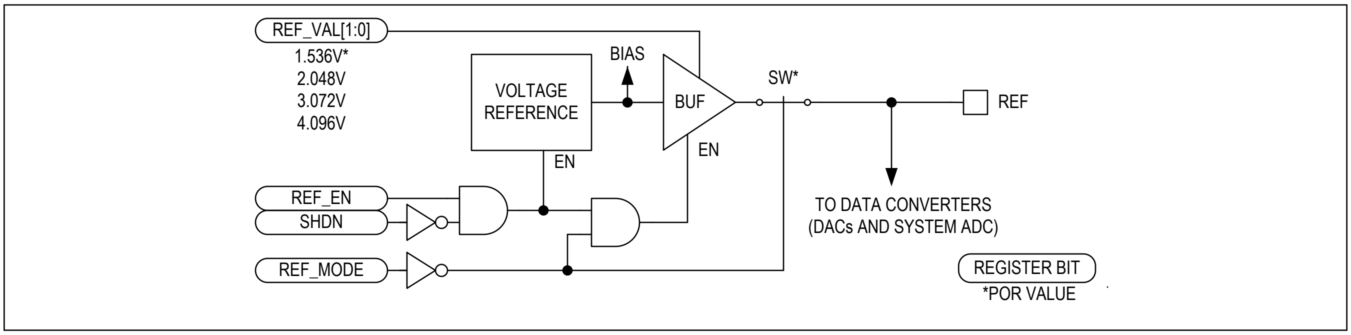


Figure 1. Internal Voltage Reference

Sensor DACs

The 12-bit digital-to-analog converters (DACs) provide DC bias to the sensors and the EIS DAC. They are shared by the working and counter amplifiers for each sensor channel and between sensor channels for the 2- and 4-channel versions. There are two DACs for the 1-channel version and four DACs for the 2- and 4-channel versions. A simplified diagram of the DACs is shown in Figure 2.

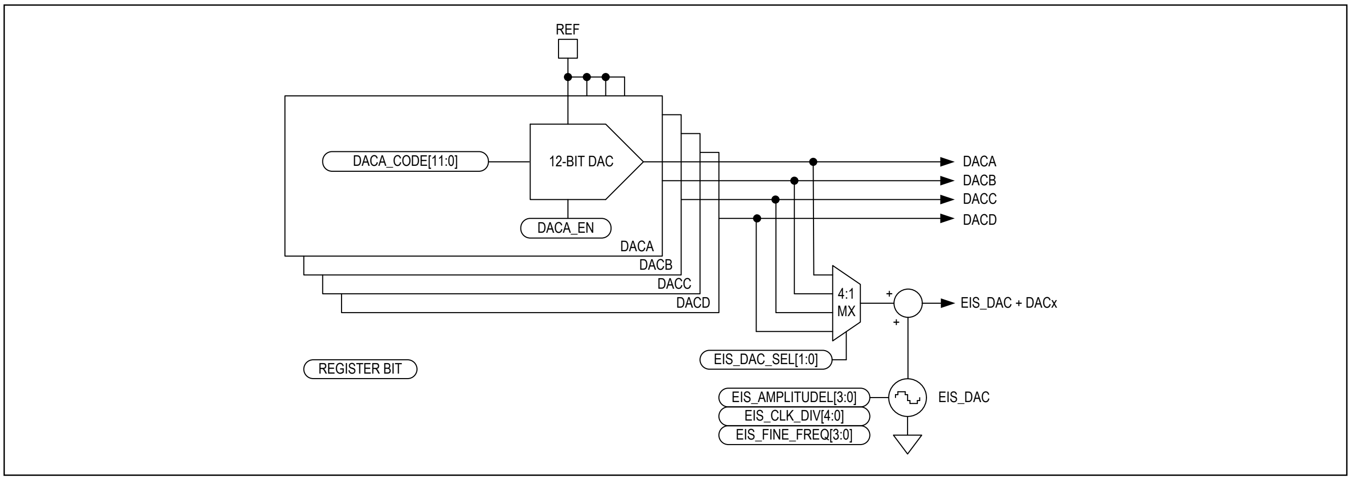


Figure 2. Internal DACs

Each DAC is independent and is enabled using DACx_EN bits where x = A, B, C, or D. The DAC output voltage (V_{DACx}) for codes greater than 18 LSBs is given by:

$$V_{DACx} = V_{REF}\left(\frac{CODE}{2^{12}}\right)$$

Where CODE is DACx_CODE[11:0] and V_{REF} is the voltage at the REF pin.

The EIS DAC adds a programmable sine wave onto the DC sensor bias for use in EIS mode. The DC value used by the EIS DAC is selected by EIS_DAC_SEL[1:0] (0x68). The amplitude of the sine wave is independent of the REF pin voltage and is programmable through EIS_AMPLITUDE[3:0] (0x79) in 5mV$_{P-P}$ increments from 5mV$_{P-P}$ to 80mV$_{P-P}$. The frequency of the sine wave is set by EIS_CLK_DIV[4:0] (0x7A) and EIS_FINE_FREQ[3:0] (0x7F). For more information on the EIS operating mode, refer to the *EIS Sine Wave* section.

Sensor AFE

Each sensor channel can bias and measure current in 2- and 3-terminal electrochemical sensors. Both AC and DC current can be measured at the working electrode. The DACs and EIS ADC are shared between sensor channels for the multi-channel versions.

Figure 3 shows the detailed channel block diagram for a sensor AFE. Each sensor channel includes a working amplifier, a counter amplifier, analog switches, sensor detect, and a current mode ADC (sensor ADC). Each amplifier can be individually powered up or down depending on the sensor configuration. Unused amplifiers can be configured to be used as a guard ring driver to protect sensitive traces on the printed circuit board (PCB). The analog switches are individually opened or closed to provide the flexibility for the front end to be used with a wide variety of sensors. The sensor detect circuit is used when the device is in low-power mode with the front end powered down and detects when a sensor attached to the electrode pins becomes active or wet. When a wet sensor is detected, a status bit is asserted and an interrupt is generated if enabled, see the *Sensor Detect* section.

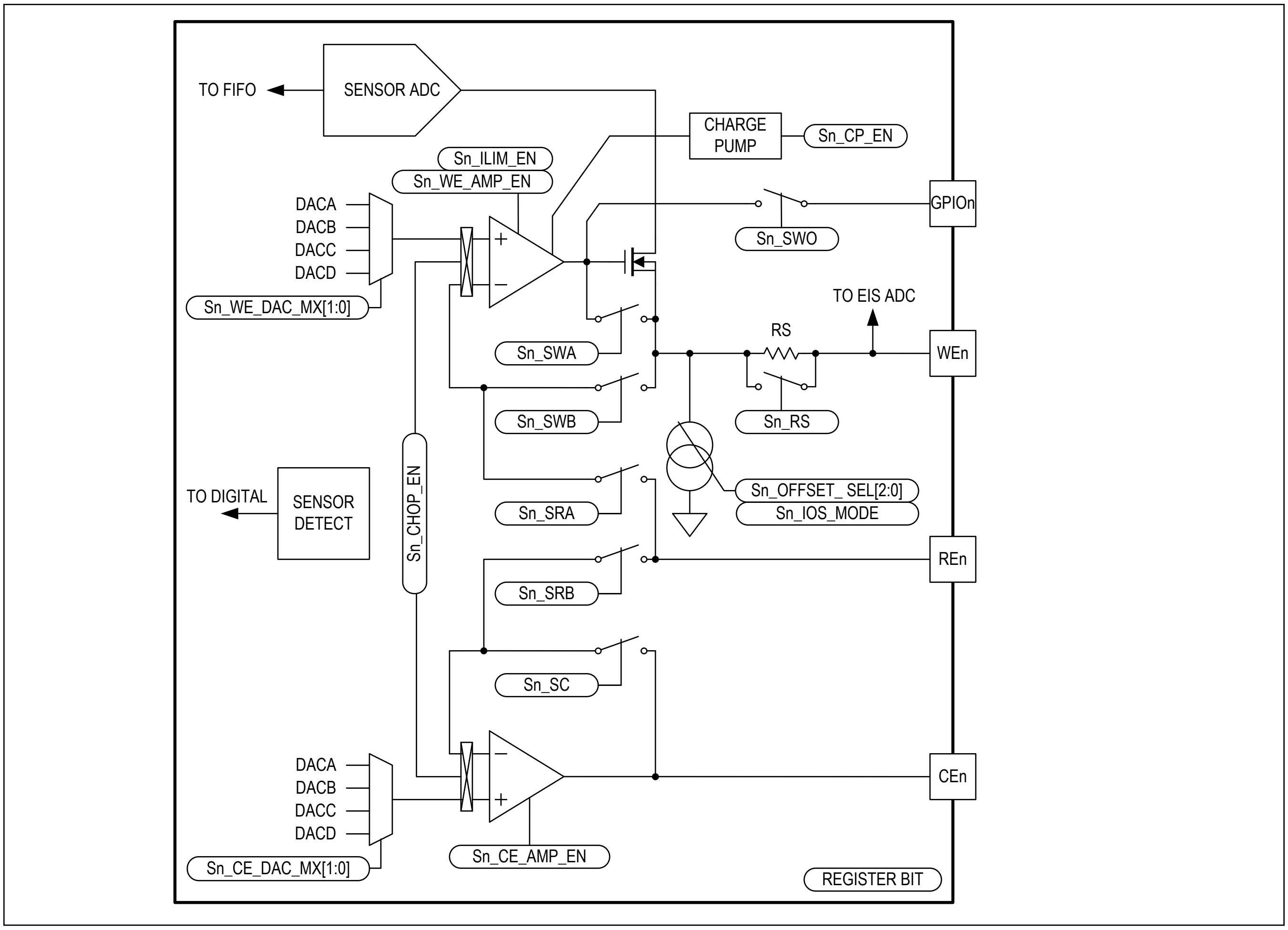


Figure 3. Detailed Sensor Block Diagram

Figure 3 shows the main register control bits that are used to configure Sensor n AFE, where n = 1, 2, 3, 4.

Sn_WE_DAC_MX[1:0] and Sn_CE_DAC_MX[1:0] select which DAC is used to bias the WEn and CEn ampllifiers, which in turn are enabled by Sn_WE_AMP_EN and Sn_CE_AMP_EN (0x20, 0x2D, 0x3A, 0x47). The five switches Sn_SWA, Sn_SWB, Sn_SRA, Sn_SRB and Sn_SC (0x21, 0x2E, 0x3B, 0x48) are used to configure the Sensor AFE to the target application. Examples are given in the Sensor Configurations section. SWO is used to connect the WEn amplifier outputs to the respective GPIOn pins. In use cases where 50Hz/60Hz rejection is critical, a large bypass capacitor can be connected between WEn and GPIOn to filter out the noise.

The WEn pin can be biased up to V_{DD} - 1.1V. If a higher WEn voltage is needed, then set Sn_CP_EN (0x20, 0x2D, 0x3A, 0x47) to 1. This turns on the charge pump in the WEn amplifier output stage allowing the WEn pin to go up to V_{DD} - 0.7V. The frequency of the charge pump is typically 500kHz when the system ADC is disabled. When the system ADC in enabled by setting SYS_SELECT (0x55) to 1, the charge pump frequency is locked to 4x the system ADC clock (512kHz ±2%).

The sensor ADC is unipolar, and incorporates an offset current to allow measurements of negative current. Use Sn_OFFSET_SEL[2:0] (0x23, 0x30, 0x3D, 0x4A) to add a positive offset current to the sensor current. Adding a positive offset current raises the base signal level above zero and allows the ADC to track negative signals. If needed, the offset current can be automatically subtracted from the measurement using IOFFSET_CONV (0x80). See the Sensor ADC section for more details. By default, the offset current programmed by Sn_OFFSET_SEL[2:0] is present at the WE pin all the time. This is best for minimizing the disturbance on the WE pin when an ADC conversion gets initiated. If desired, the offset current can be configured to be present only during an ADC conversion by setting Sn_IOS_MODE (0x22, 0x2F, 0x3C, 0x49) to 1.

The input referred offset voltage of the WEn and CEn amplifiers is trimmed to less than ±2mV. Setting Sn_CHOP_EN (0x20, 0x2D, 0x3A, 0x47) to 1 turns on the chopper within these amplifiers to reduce this offset voltage, offset voltage temperature drift and flicker noise. However, setting Sn_CHOP_En to 1 creates some ripple in the bias voltage, which can be undesirable in some applications.

When the SWA switch is closed, the WE amplifier drives the WEn pin directly. To limit the drive current in this mode and comply with IEC 60601 set Sn_ILIM_EN (0x21, 0x2E, 0x3B, 0x48) to 1.

When the capacitance at the WE pin is high, the stability of the WE amplifier can be compromised and oscillation can occur. If this happens set Sn_RS (0x21, 0x2E, 0x3B, 0x48) to 1. This adds a 60kΩ resistor (RS) in series with WEn output to isolate the amplifier output from the load capacitance. This method results in a voltage drop and bias voltage shift when the sensor current is large.

Sensor Configurations

This section gives sample configurations of the Sensor AFEs for specific use cases. The switch settings for each case are summarized in Table 1.

Table 1. Sensor Switch Configurations

SWITCH	3 TERMINAL, WE DRIVE	3 TERMINAL, CE DRIVE	2 TERMINAL, WE DRIVE	6 TERMINAL, WE x 4 DRIVE
Sn_SWA	Open	Open	Open	Open x 4
Sn_SWB	**Closed**	Open	**Closed**	**Closed x 4**
Sn_SRA	Open	**Closed**	Open	Open x 4
Sn_SRB	**Closed**	Open	Open	**Closed x 4**
Sn_SC	Open	**Closed**	**Closed**	Open x 4

Figure 4 shows how to configure the AFE to measure WE current with a 3-terminal electrochemical sensor. The working and counter amplifiers are both powered up and biased using two of the DACs. In this configuration, switch Sn_SWA is open, Sn_SWB is closed, Sn_SRA is open, Sn_SRB is closed, and Sn_SC is open.

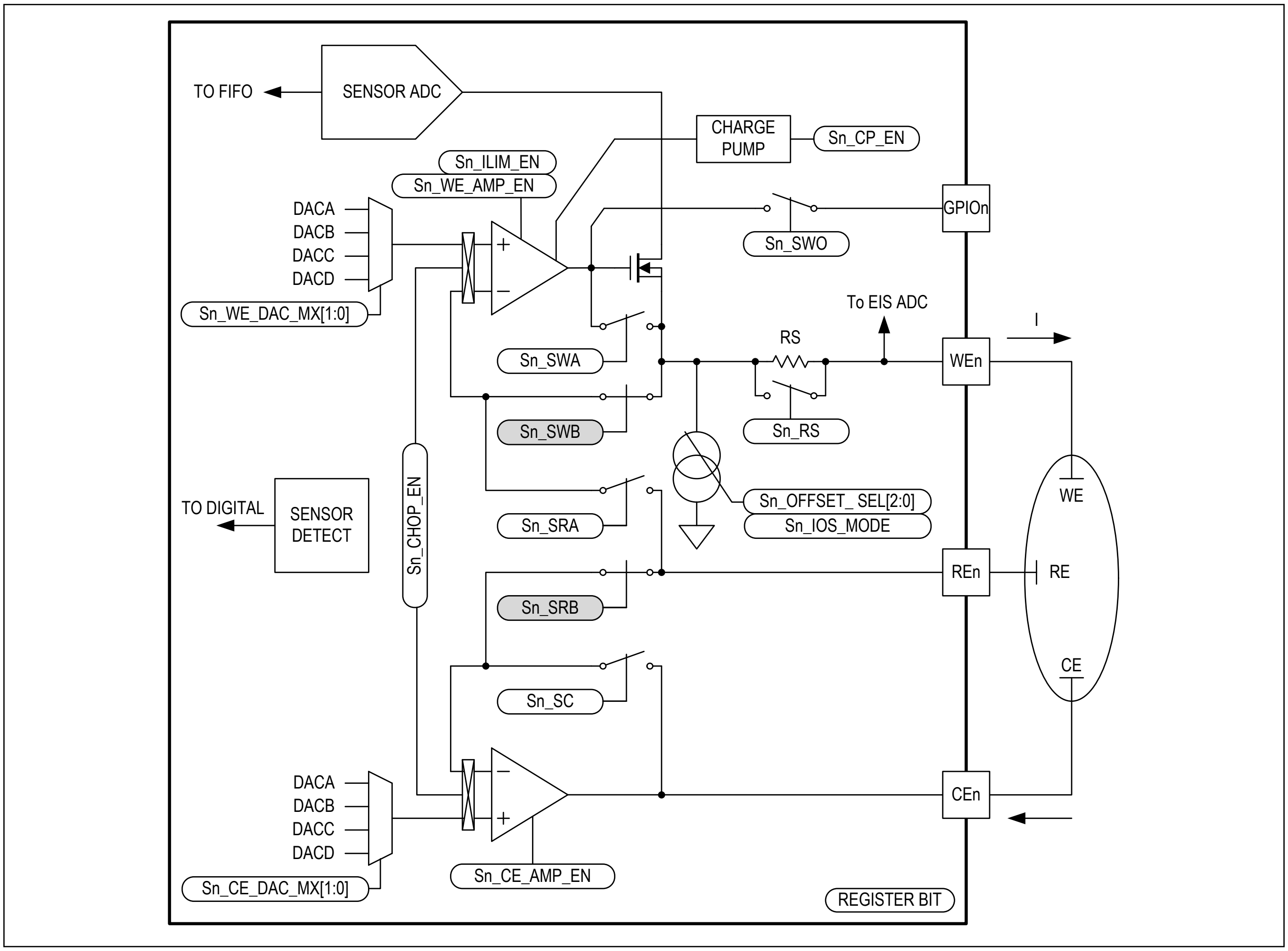


Figure 4. Sensor 1 Block Diagram—3 Terminal Sensor Measuring WE Current

Figure 5 shows how to configure the AFE to measure CE current with a 3-terminal electrochemical sensor. The working and counter amplifiers are both powered up and biased using two of the DACs. In this configuration, switch Sn_SWA is open, Sn_SWB is open, Sn_SRA is closed, Sn_SRB is open, and Sn_SC is closed. The switches are effectively opposite the previous configuration and the sensor is connected upside down compared to the configuration in Figure 4. This allows the sensor current to be measured by the sensor ADC and for current to flow out of the working electrode.

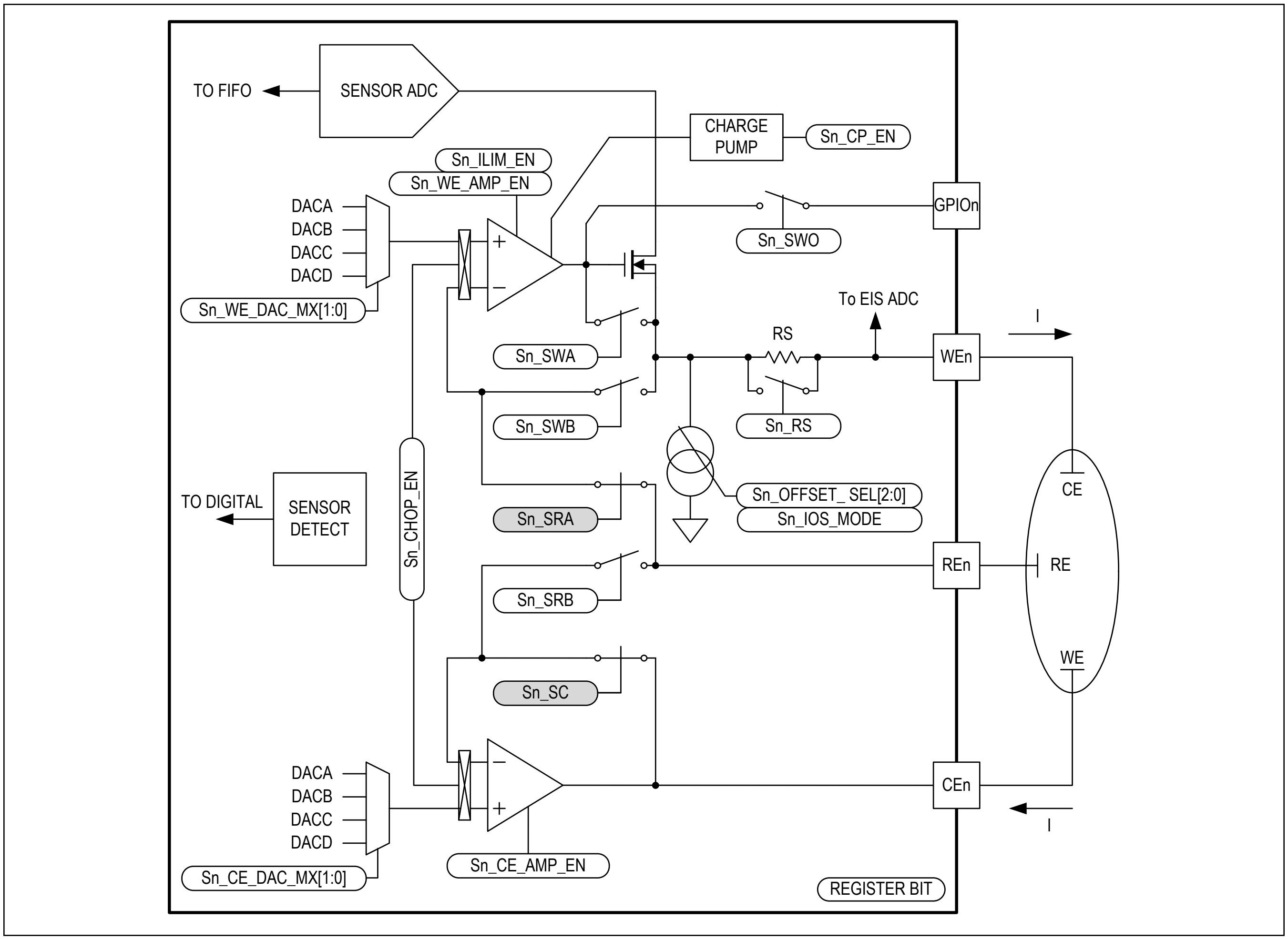


Figure 5. Sensor 1 Block Diagram—3 Terminal Sensor Measuring CE Current

Figure 6 shows how to configure the AFE to measure WE current with a 2-terminal electrochemical sensor. The working amplifier is powered up and biased with one of the DACs and the counter amplifier is powered up if optionally used as a guard ring driver. When used as a guard ring driver for the working electrode traces on the PCB then the same DAC used for the working amplifier is used with the counter amplifier. In this configuration, switch Sn_SWA is open, Sn_SWB is closed, Sn_SRA is open, Sn_SRB is open, and Sn_SC is closed.

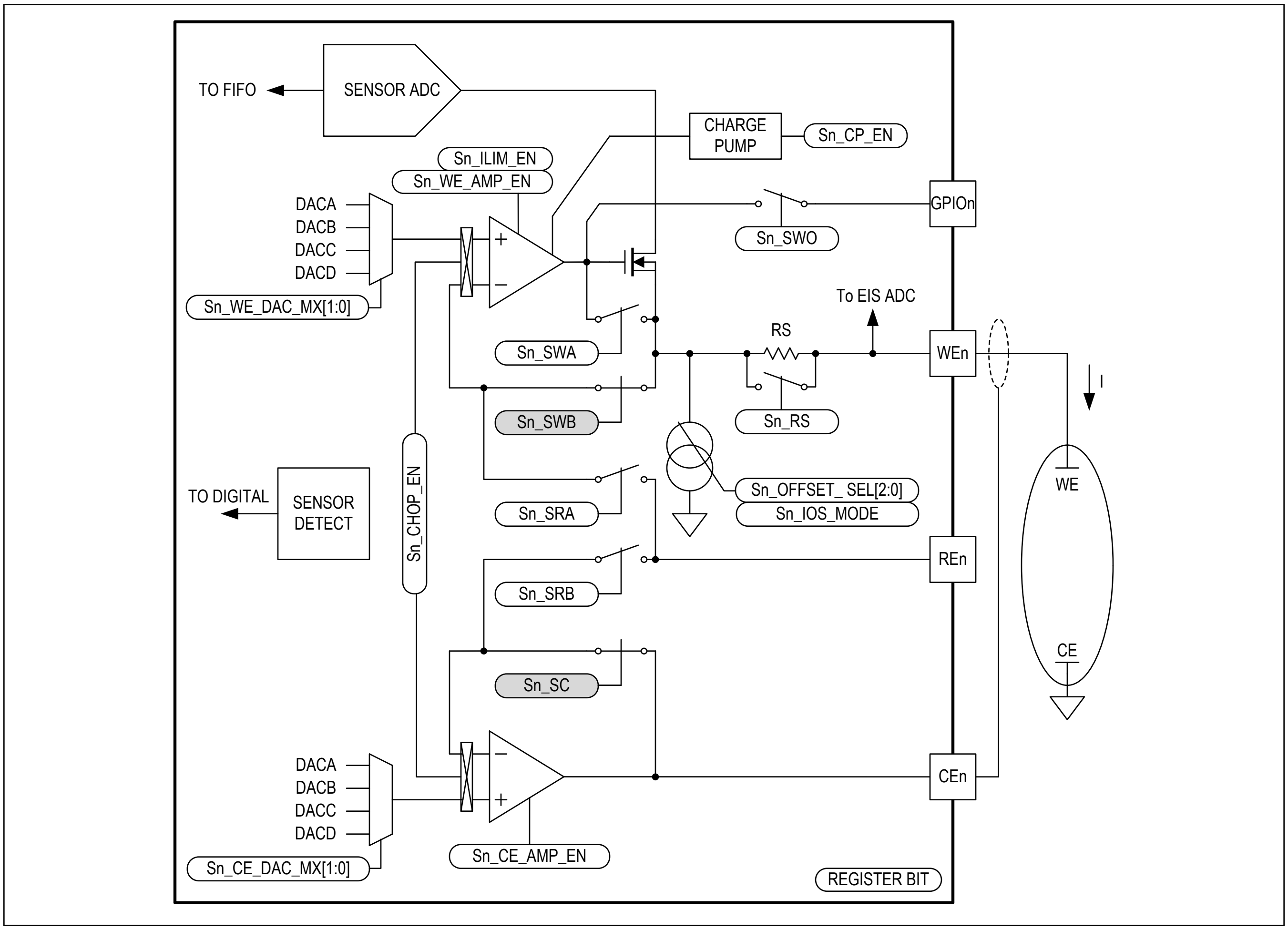


Figure 6. Sensor 1 Block Diagram—2 Terminal Sensor Measuring WE Current

Figure 7 shows how to configure the AFE to measure WE current with a 6-terminal electrochemical sensor with 4 WE, 1 RE, and 1 CE. The working and counter amplifiers are both powered up and biased using two or more of the DACs. The SHARED_CA option is enabled, Sn_SWA switches are open, the Sn_SWB switches are closed, the Sn_SRA switch is open, the Sn_SRB switch is closed, and the Sn_SC switch is open.

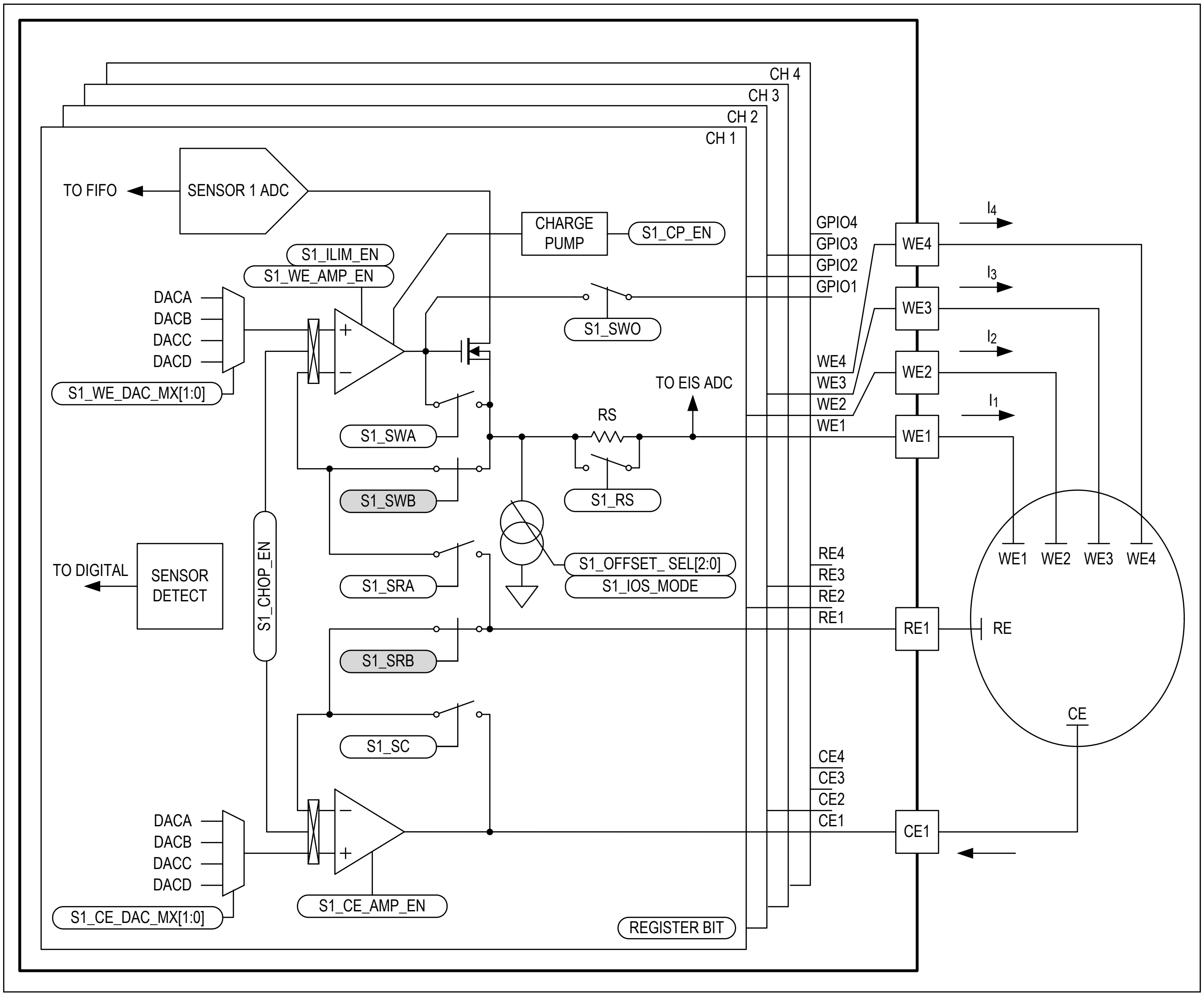


Figure 7. Sensor 1 Block Diagram—6 Terminal Sensor Measuring WE Current

Sensor ADC

The simplified diagram of the sensor ADC is shown in Figure 8.

Current from the sensor (I_{SENSOR}) plus the offset current (I_{OFF}) programmed by Sn_OFFSET_SEL[2:0] (0x23, 0x30, 0x3D, 0x4A) flows directly to the current mode sigma-delta ADC. The sigma-delta ADC integrates the input current and compares it to the programmable reference current set by Sn_FSR[2:0] (0x23, 0x30, 0x3D, 0x4A) to generate a bit stream whose density is proportional to the input current. The bit stream is then filtered to give a digital representation of the sensor current. Compared to the traditional transimpedance amplifier (TIA) approach, the benefit of this architecture is that it can achieve very low noise and high precision while using minimal power.

Figure 8 shows the main register control bits used to configure the sensor ADC.

The ADC full-scale reference current is set by Sn_FSR[2:0] and can be programmed to either 50nA, 100nA, 200nA, 500nA, 1000nA, or 2000nA. To maximize the signal-to-quantization-noise ratio, choose the smallest full-scale current that does not saturate the ADC. The ADC conversion time is set by Sn_CONV_TIME[3:0] (0x24, 0x31, 0x3E, 0x4B) and CLK_SEL (0x14) and is programmable from 0.1s to 240s. At conversion times below 1s, the ADC resolution drops slightly below 16 bits. Details can be found in the register map description for Sn_CONV_TIME[3:0]. Note that a longer conversion time leads to higher power consumption.

SENS_CONV_TYPE (0x80) selects the type of measurement to be made on sensor n. This can be either a DC or an EIS measurement. Set SENS_CONV_TYPE to 0 to perform a DC measurement and set SENS_CONV_TYPE to 1 to perform an EIS measurement. EIS measurement can be performed on only one sensor at a time, while DC measurement can be performed on multiple channels simultaneously. Sn_SELECT (0x24, 0x31, 0x3E, 0x4B) selects sensor n for either manual or automatic current conversion. Setting Sn_SELECT to 0 excludes sensor n from either conversion.

IOFFSET_CONV[1:0] (0x80) selects how the offset current selected by Sn_OFFSET_SEL[2:0] is handled. The user can choose whether the offset current is measured separately, combined with the sensor current, or subtracted from the sensor current. Set IOFFSET_CONV to 0 to measure the sensor current plus the offset current. Set IOFFSET_CONV to 1 to measure only the offset current. Set IOFFSET_CONV to 2 to perform both a sensor current plus offset current measurement and a separate offset current-only measurement. Because two separate measurements are made when IOFFSET_CONV is set to 2, the time for the measurement to complete is twice as long as for a single measurement. For ADC conversions done with IOFFSET_CONV set to 2, the offset current is subtracted from the sensor current, and the result is stored in the FIFO. The offset current is stored separately in the Sn_IOFFSET[15:0] (0x2B, 0x38, 0x45, 0x52) bits. Note that in this mode, if the sensor current is less than the offset current, a value of 0nA is reported.

To convert the tagged FIFO result to the channel n sensor current (I_{Sn}), use this equation:

$$I_{Sn} = \frac{\text{counts} \times \text{SnFSR}}{2^{16}} - \text{SnOFFSET}$$

where,

Counts = Unsigned count from bits 15:0 of the tagged FIFO word

SnFSR = Full-scale range current set by Sn_FSR[2:0]

SnOFFSET = Offset value set by Sn_OFFSET_SEL[2:0]. See register 0x23 for valid offset currents.

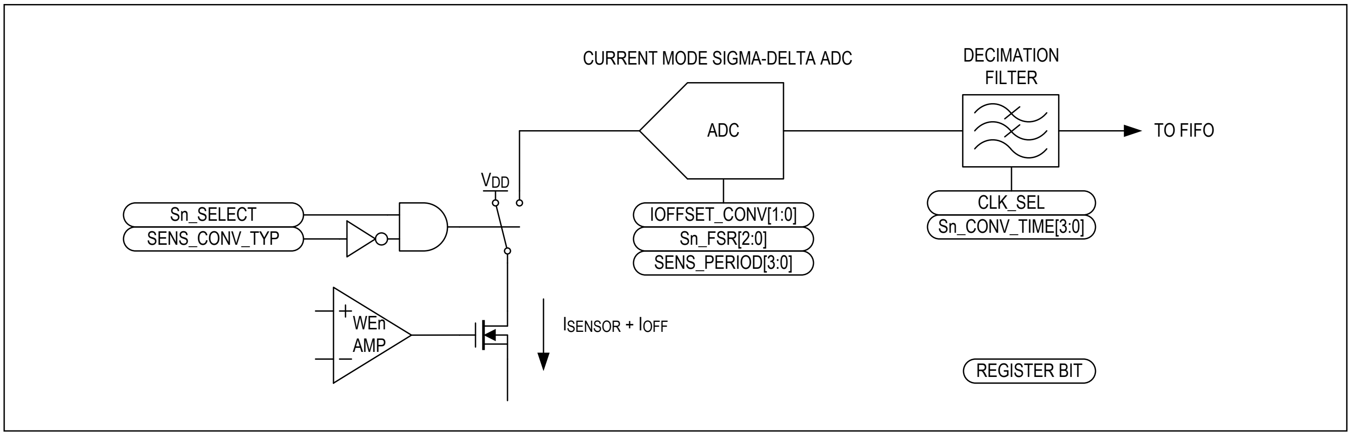


Figure 8. DC Sensor ADC

Sensor Operating Modes

The sensor ADC can be set to run in autonomous mode, AUTO (0x83) set to 1, or single conversion mode, AUTO set to 0. In autonomous mode the period between each ADC conversion is set by SENS_PERIOD[1:0] (0x80) and CLK_SEL (0x14). Note the period between ADC conversions (t_{PERIOD}) must be the same or longer than the ADC integration time (t_{INT}) and ADC precharge time (t_{PRE}) as shown in Figure 9. The integration time of the sensor ADC (t_{INT}) is primarily set by Sn_CONV_TIM[3:0] (0x24, 0x31, 0x3E, 0x4B), but it is also a function of CLK_SEL and Sn_FSR[2:0] (0x23, 0x30, 0x3D, 0x4A). See the Register Map for more details.

After completing all the required settings, set CONVERT to 1 to initiate ADC conversions. If AUTO is set to 0, the ADC converts one sample for each selected sensor then stops and clears the CONVERT bit.

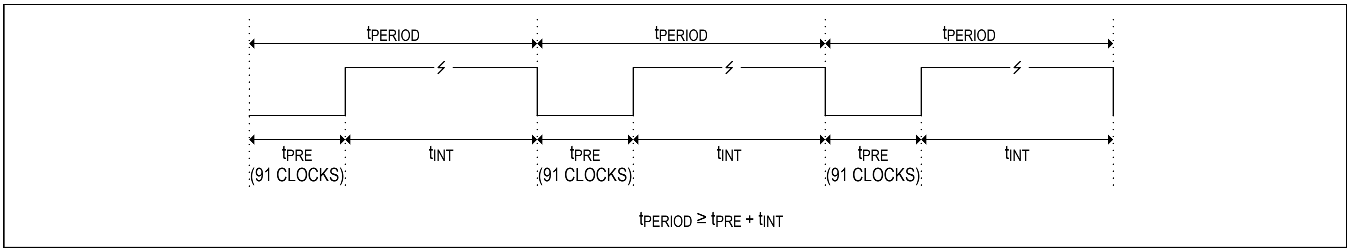


Figure 9. Sensor ADC Timing

Offset and Gain Calibration

The simplified sensor ADC signal path for offset currents is shown in Figure 10. Offset current is necessary in this architecture to provide current bias for the WE pin and raise the ADC output above zero so that near zero and bipolar ADC measurements can be performed. There are two different offset currents in each channel: a programmable current that is controlled by Sn_OFFSET_SEL[2:0] (0x23, 0x30, 0x3D, 0x4A) and a fixed 50nA current. The 50nA current is used to bias the WE pin when not making measurements and the programmable current is used to set the ADC offset count during sensor ADC measurements. When the ADC is not converting, S1.n is switched to V_{DD}, S2.n is closed, and the fixed 50nA bias current is used to bias the WEn pin. When the ADC is converting, the 50nA current is switch off (S2.n opened), and the offset current selected by Sn_OFFSET_SEL[2:0] is combined (S3.n closed) with the sensor current and fed to the ADC (S1.n switched to ADC). How the ADC handles the offset current is determined by IOFFSET_CONV[1:0] (0x80).

When an ADC conversion is done with IOFFSET_CONV[1:0] set to 0, the ADC measures the sensor current plus the offset current.

When an ADC conversion is done with IOFFSET_CONV[1:0] set to 1, the ADC measures the offset current programmed by Sn_OFFSET_SEL[2:0] only. This mode is useful for calibrating the gain error between different full-scale ranges.

Since offset current is not part of the real signal, removing it from the ADC output can be desirable. To do this, set IOFFSET_CONV[1:0] to 2. This performs two ADC conversions. The first converts with S2.n and S4.n closed and S1.n in the V_{DD} position to measure the offset current, and the second converts with only S3.n closed and S1.n in the ADC position to measure the offset current plus the sensor current. The sensor current is then calculated by subtracting the first result from the second result and stored in the FIFO. The result from the first conversion is also stored in the Sn_IOFFSET[15:0] bits. Subtracting hardware offset uses double the power because it needs to run two ADC conversions. Since the offset current doesn't drift much with time, it might be better to perform offset measurement every so often and subtract it in the software using the Sn_IOFFSET[15:0] bits.

The ADC has six different full-scale ranges set by Sn_FSR[2:0] (0x23, 0x30, 0x3D, 0x4A), but only the 500nA range is calibrated to ±1%. To determine the gain error in the other three ranges, set IOFFSET_CONV[1:0] to 1 to measure only the offset current with S2.n and S4.n closed and S1.n in the V_{DD} position. For example, to measure the gain error at 250nA, set Sn_OFFSET_SEL[2:0] to 7 and run two ADC conversions in the 500nA range and the 250nA range. Use the measurement result from the 500nA range to calculate the offset current to 1% accuracy and then back-calculate the gain error in the 250nA range. The same procedure can be applied to the other full-scale ranges.

$$\text{IOFFSET} = \frac{500\text{nA} \times \text{ADC\_OUT}_{(500\text{nA})}}{65536}$$

$$\text{FSR}_{(250\text{nA})} = \frac{\text{IOFFSET} \times 65536}{\text{ADCOUT}_{(250\text{nA})}}$$

To measure the gain mismatch between different channels, perform an ADC conversion with SENSOR_CAL set to 1. The offset current from channel 1 is cycled through the four channels using S5.n, and the results are stored in the Sn_IOFFSET[15:0] (0x2B, 0x38, 0x45, 0x52) bits. S2.n is closed to keep the bias on the sensor, and S1.n is in the V_{DD} position. Since the same offset current is injected into each channel, the difference in the ADC output is purely caused by a mismatch in the ADC gain.

To measure a current flowing into the WEn pin, set the offset current larger than the maximum signal current. The maximum amount of current that WEn can sink is limited by the offset current. If the current flowing into the WEn pin is greater than the offset current, the WEn pin rises above the voltage that is set by the DAC. The signal can be calculated by subtracting the signal + offset conversion from the offset-only conversion.

Note: The digital control logic controls switches S1.n to S5.n; the user cannot control them directly.

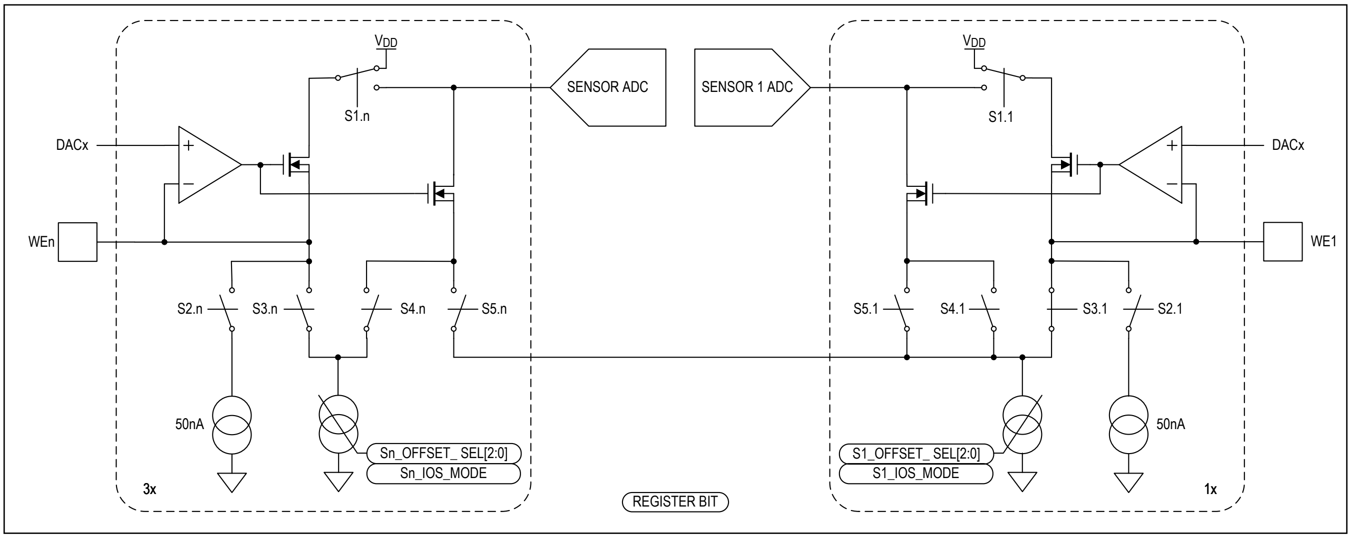


Figure 10. DC Offset Current Calibration

Sensor Detect

Each sensor channel has an independent, low power detect circuit that can be used to detect when the state of the sensor changes. Figure 11 shows the simplified diagram of the detect circuit.

It operates by applying a small voltage bias to the WEn pin and comparing the WEn current against a threshold current (I_{DETECT}). The applied voltage bias is set globally for all sensor channels by DETECTOR_BIAS[1:0] (0x1F) and is programmable from 200mV to 800mV in 200mV increments. I_{DETECT} is individually set per sensor channel by Sn_DETECTOR_THRESHOLD[1:0] (0x22, 0x2F, 0x3C, 0x49) and is programmable to either 20nA, 40nA, 80nA, or 160nA. The circuit is enabled by setting Sn_DETECTOR_EN (0x22, 0x2F, 0x3C, 0x49) to 1. If the WEn current is higher than the threshold current I_{DETECT}, the WE pin is pulled low and trips the comparator. A deglitching filter is used to reject pulses narrower than 10ms. If the pulse lasts for more than 10ms, the counter gets incremented by 1, and the WE pin is discharged back to ground. If the cycle repeats four times, the sensor detect circuit asserts the Sn_DET (0x02, 0x03) status bit, and generates an interrupt on INTB if enabled. In the case of a single false trigger, the sensor detect times out and resets itself after 400ms. Once the status bit is asserted, the sensor detect must be disabled to reset the counter.

The sensor detect block and the sensor AFE cannot both drive the WEn pin, so only one should be enabled at a time. While in sensor detect mode, the CE pin is pulled to ground. The RE pin is not driven, but it can be shorted to CE by closing Sn_SRB and Sn_SC (0x21, 0x2E, 0x3B, 0x48) AFE switches.

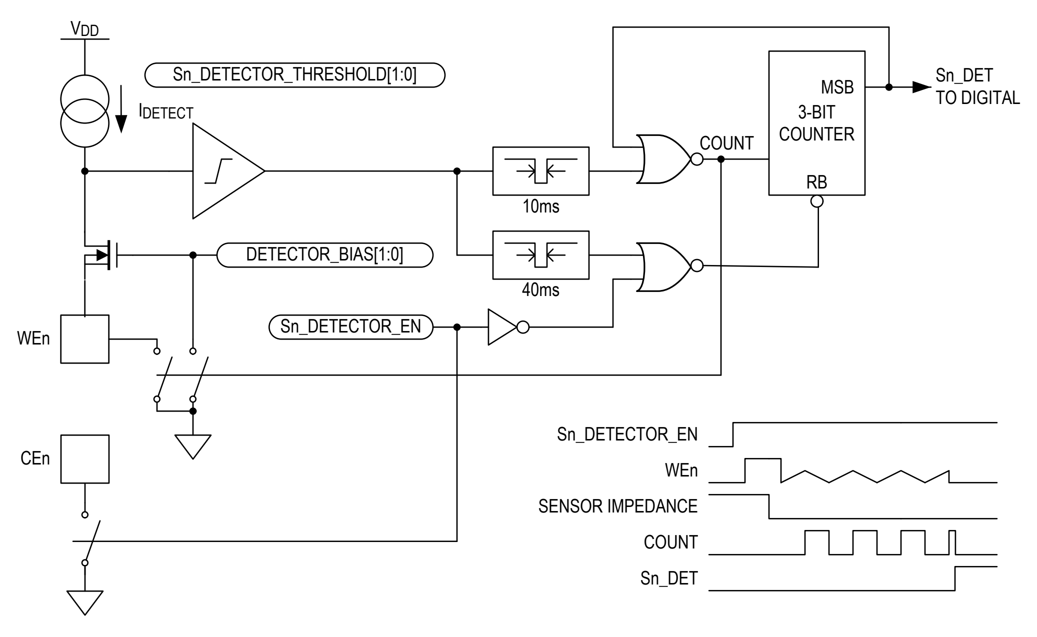


Figure 11. Sensor Detect

EIS Sensor ADC

The electrochemical impedance spectroscopy (EIS) ADC is used in EIS mode to measure the complex impedance of a sensor. In EIS mode, a small-signal sine wave is driven onto one of the sensor channels and the EIS ADC measures the real and imaginary admittance and the DC bias current at the transmitted frequency. This EIS ADC is shared between sensors for the multichannel devices.

Figure 12 show the main register control bits that are used to configure the EIS sensor. In EIS mode, the user can superimpose a small sine wave on top of one of the 4 DC DAC's to generate a stimulus for EIS measurement using EIS_DAC_SEL[1:0] (0x78). Only the channel that is making an EIS measurement receives the sine wave, the rest of the channels retain their DC biases.

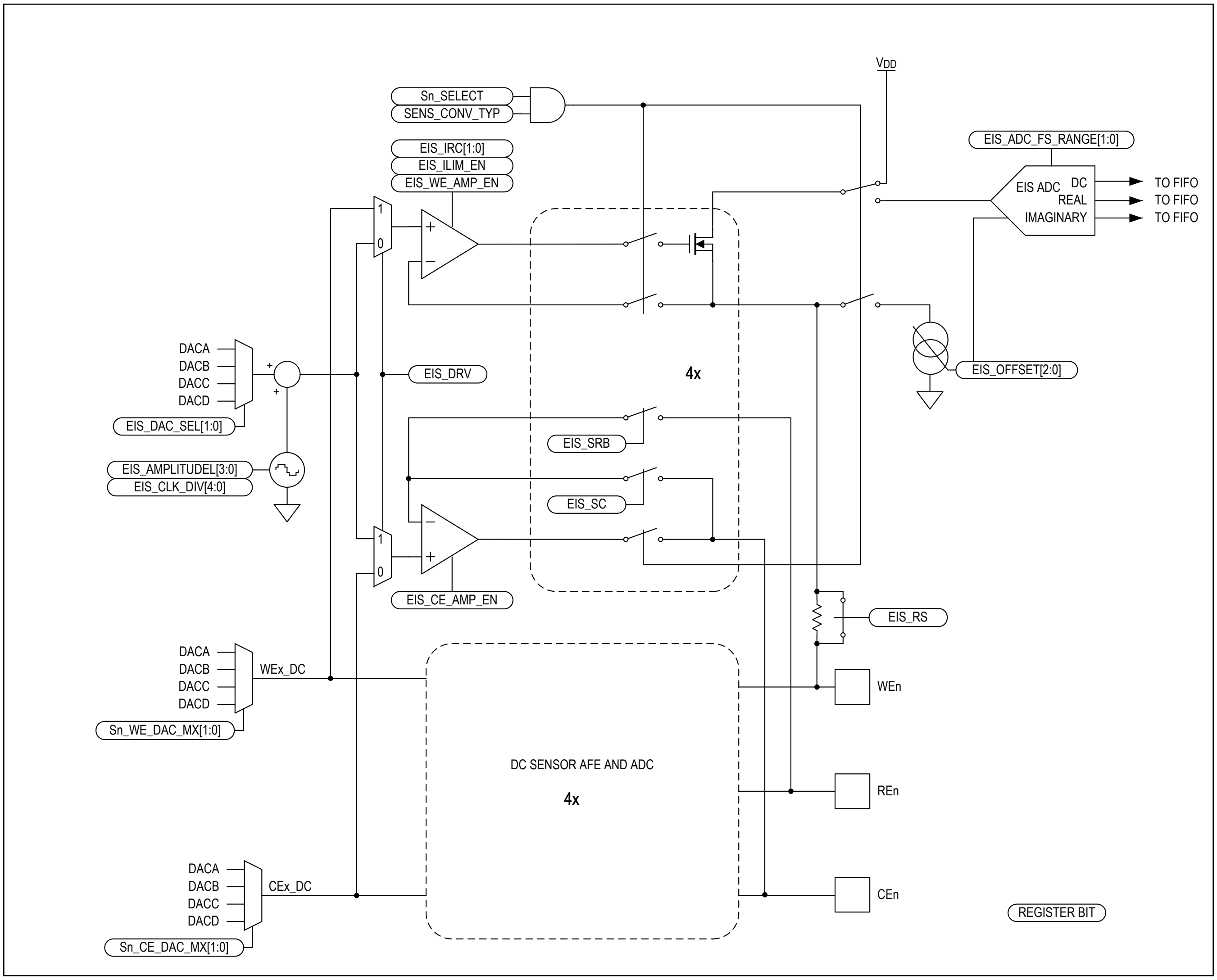


Figure 12. EIS Block Diagram

EIS Operating Theory

I and Q Codes from Sigma Delta ADC

In EIS mode, a sinusoid is superimposed on the DC voltage of either the working electrode (WE) or counter electrode (CE) while the working electrode current is measured. Figure 13 demonstrates a simplified EIS measurement setup. DC + AC voltage is applied to WE while CE is at virtual ground. Since the current is measured at the drain of the nMOS transistor, the voltage of WE can be driven. The output current feeds a sigma-delta modulator that is filtered in the digital domain, creating a sequence of ADC codes. A digital correlator extracts the In-phase (I) and Quadrature-phase (Q) components at the same time. When driving the counter electrode (CE) the measurement current is inverted compared to driving from the working electrode (WE) resulting in a 180-degree phase change, which must be accounted for. Since voltage is driven and current is measured, admittance rather than impedance is measured, but they are simply complex-number inverses of each other. The I code is proportional to conductance and the Q code to susceptance. Phase and Admittance is calculated directly from these I and Q codes.

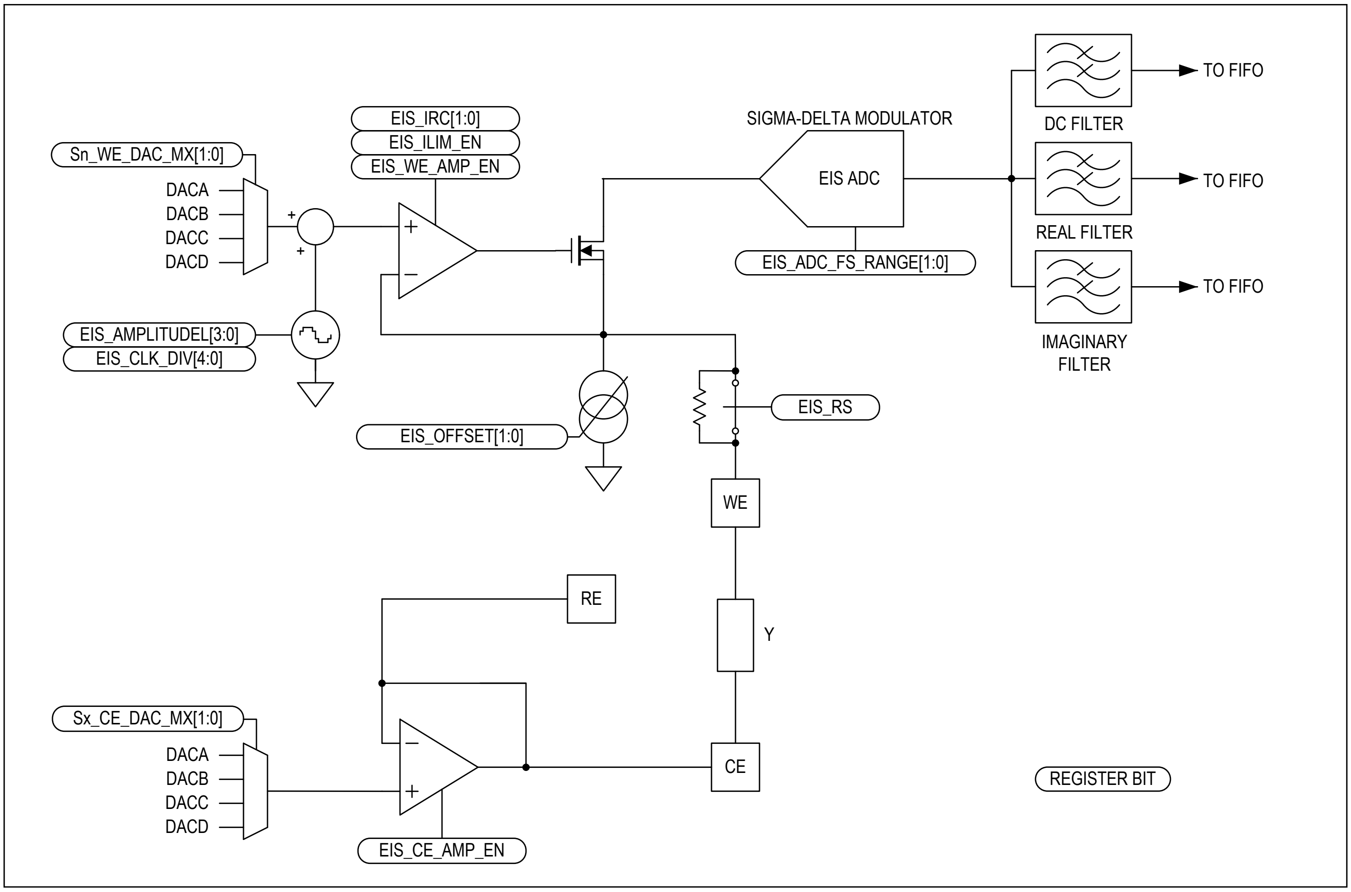


Figure 13. Simplified EIS Measurement Setup

Filter Gain K_{CIC}

Multiple cascade integrator comb (CIC) filters are used to decimate the output of the EIS sigma-delta modulator. The gain factor of these filters is dependent on the clock divider, EIS_CLK_DIV[5:0] (0x7A), used to generate frequency of the synthesized sine wave and is shown in Table 2. The measured admittances are adjusted by these factors as outlined in the *Calculating Admittance, Impedance, and Phase* section.

Table 2. CIC FILTER FACTORS APPLIED TO THE ADMITTANCE MEASUREMENTS

EIS_CLK_DIV[5:0]	f_S (Hz)	k_{CIC}
3	14,142 to 27,058	0.7298
4	7,701 to 13,543	0.8332
5	3,536 to 6,771	0.8831
6	1,768 to 3,386	0.8960
7	883.9 to 1,693	0.8992
8	441.9 to 846.4	0.9000
9	221.0 to 423.2	0.9002
10	110.5 to 211.6	0.9003
≥ 11	≤ 108.3	1.0000

EIS Configuration Registers

EIS Mode Setup

To enable EIS mode on the device, the sensor conversion type bit SENS_CONV_TYPE (0x80) must be set to 1, enabling the AC mode, and AC_MODE[1:0] (0xA0) must be set to 0, EIS Mode. When the device is in EIS mode and a conversion is started an EIS measurement is made on the enabled DC sensors WE, RE, and CE pins. If sensor 2 is enabled, then the EIS circuitry is connected to the WE2, RE2, and CE2 pins during the EIS measurement. If two sensor channels are enabled, only the sensor channel with the lowest index is used. For example, if channel 2 and 3 are both enabled, only channel 2 performs an EIS measurement. An EIS measurement can be performed on only one sensor at a time, while DC measurement can be performed on multiple channels simultaneously. By design, the DC and the EIS measurements are mutually exclusive and only one can be active at a time. However, the DC biases are independent of the ADC operation and are maintained by the DAC and AFE at all times.

EIS Sine Wave

EIS Frequency

The frequency of the EIS sine wave is controlled by 4 registers: EIS_CLOCK_DIV[5:0] (0x7A), EIS_FINE_FREQ[3:0] (0x7F), FAST_TRIM_ADJ[7:0] (0x75), and SLOW_TRIM_ADJ[7:0] (0x76). EIS_CLOCK_DIV[5:0] is used to select the octave and EIS_FINE_FREQ is used to select one of 16 steps within the selected octave. The FAST_TRIM_ADJ[7:0] and SLOW_TRIM_ADJ[7:0] are determined by the *Fine Frequency Adjust Calibration* procedure explained in the EIS calibration section. These fine frequency adjust registers must be set correctly to obtain the selected frequency.

The available EIS sine wave frequencies are given in Table 3 and Table 4. The left most column of each table is the coarse code, which is the value set in the EIS_CLOCK_DIV[5:0] register. The fine frequency codes across the top of the table are the 2's complement value set in the EIS_FINE_FREQ[3:0] register. The coarse code has allowed values of 3 to 23 and the fine frequency code can vary from -8 to 7 (4 bit, 2's complement), giving a total of 21 x 16 = 336 available frequencies ranging from 0.0138Hz to 27.085kHz.

EIS frequencies below 110Hz use a different base clock then frequencies above 110Hz. This results in a break in the octave boundary for the coarse code step between 10 and 11 and a need for two separate equations to determine the EIS sine-wave frequency (f_S).

For coarse codes 3 to 10 use:

$$f_S = 160000x2^{\left(\frac{\mathrm{FINE}}{16} - \mathrm{COARSE}\right)}$$

For coarse codes 11 to 23 use:

$$f_S = 80x2^{\left(\frac{\mathrm{FINE}}{16} - (\mathrm{COARSE} - 11)\right)}$$

where COARSE is the coarse code set in EIS_CLK_DIV[5:0] and FINE is the 2's complement value of the 4-bit code set in EIS_FINE_FREQ[3:0].

Table 3. EIS MODE SYNTHESIS FREQUENCIES 1

COARSE CODE*	**FINE FREQUENCY CODE**								
	-8	**-7**	**-6**	**-5**	**-4**	**-3**	**-2**	**-1**	**0**
3	14142	14768	15422	16105	16818	17563	18340	19152	20000
4	7071	7384	7711	8052	8409	8781	9170	9576	10000
5	3536	3692	3856	4026	4204	4391	4585	4788	5000
6	1768	1846	1928	2013	2102	2195	2293	2394	2500
7	884	923	964	1007	1051	1098	1146	1197	1250
8	442	462	482	503	526	549	573	599	625
9	221	231	241	252	263	275	287	300	313
10	110	115	120	126	131	137	143	149	156
11	56.6	59.1	61.7	64.4	67.3	70.3	73.4	76.6	80.0
12	28.3	29.5	30.8	32.2	33.6	35.1	36.7	38.3	40.0
13	14.1	14.8	15.4	16.1	16.8	17.6	18.3	19.2	20.0
14	7.07	7.38	7.71	8.05	8.41	8.78	9.17	9.58	10.00
15	3.54	3.69	3.86	4.03	4.20	4.39	4.59	4.79	5.00
16	1.77	1.85	1.93	2.01	2.10	2.20	2.29	2.39	2.50
17	0.884	0.923	0.964	1.007	1.051	1.098	1.146	1.197	1.250
18	0.442	0.462	0.482	0.503	0.526	0.549	0.573	0.599	0.625
19	0.221	0.231	0.241	0.252	0.263	0.274	0.287	0.299	0.313
20	0.110	0.115	0.120	0.126	0.131	0.137	0.143	0.150	0.156
21	0.0552	0.0577	0.0602	0.0629	0.0657	0.0686	0.0716	0.0748	0.0781
22	0.0276	0.0288	0.0301	0.0315	0.0328	0.0343	0.0358	0.0374	0.0391
23	0.0138	0.0144	0.0151	0.0157	0.0164	0.0172	0.0179	0.0187	0.0195

**Coarse Code is called EIS_CLK_DIV in the register map.*

Table 4. EIS MODE SYNTHESIS FREQUENCIES 2

COARSE CODE*	**FINE FREQUENCY CODE**							
	0	**1**	**2**	**3**	**4**	**5**	**6**	**7**
3	20000	20885	21810	22776	23784	24837	25937	27085
4	10000	10443	10905	11388	11892	12419	12968	13543
5	5000	5221	5453	5694	5946	6209	6484	6771
6	2500	2611	2726	2847	2973	3105	3242	3386
7	1250	1305	1363	1423	1487	1552	1621	1693
8	625	653	682	712	743	776	811	846
9	313	327	341	356	372	389	406	424
10	156	163	170	178	186	194	202	211
11	80.0	83.5	87.2	91.1	95.1	99.3	103.7	108.3
12	40.0	41.8	43.6	45.6	47.6	49.7	51.9	54.2
13	20.0	20.9	21.8	22.8	23.8	24.8	25.9	27.1
14	10.00	10.44	10.91	11.39	11.89	12.42	12.97	13.54
15	5.00	5.22	5.45	5.69	5.95	6.21	6.48	6.77
16	2.50	2.61	2.73	2.85	2.97	3.10	3.24	3.39
17	1.250	1.305	1.363	1.423	1.487	1.552	1.621	1.693
18	0.625	0.653	0.682	0.712	0.743	0.776	0.811	0.846
19	0.313	0.326	0.341	0.356	0.372	0.388	0.405	0.423
20	0.156	0.163	0.170	0.178	0.186	0.194	0.203	0.212
21	0.0781	0.0816	0.0852	0.0890	0.0929	0.0970	0.1013	0.1058
22	0.0391	0.0408	0.0426	0.0445	0.0465	0.0485	0.0507	0.0529
23	0.0195	0.0204	0.0213	0.0222	0.0232	0.0243	0.0253	0.0265

**Coarse Code is called EIS_CLK_DIV in the register map.*

EIS DC Offset DAC

EIS_DAC_SEL[1:0] (0x78) selects one of the four voltage DACs (DACx, were x = A, B, C, or D) to be used for the DC-voltage offset of the EIS sine wave. The selected DAC can still be used as a DC voltage input to other WE or CE amplifiers when it is being used as the EIS sine-wave voltage offset.

EIS WE vs. CE Drive

EIS_DRV (0x7B) selects if the sine wave is added on the WE pin or the CE pin. Figure 14 shows both configurations when driving a load Y and external electrode parasitic capacitance to ground, $C_{WE\text{-}PAR}$ and $C_{CE\text{-}PAR}$. When driving the WE pin, the current measured by the EIS ADC includes the Load current (I_Y), Offset current (I_{OFF}), and the parasitic capacitance current ($I_{WE\text{-}PAR}$) of the WE connection to the load. At a higher frequency this can become a significant factor of the measured current. Driving the sine wave on the CE pin avoids measuring parasitic capacitance and leakage on the WE pin since, in this configuration, the WE pin is actively driven to maintain a constant voltage and $I_{WE\text{-}PAR}$ is zero. Also note when driving the CE pin, the AC current is inverted resulting in an admittance rotated by 180 degrees. The current at the EIS ADC when driving the CE pin is $I_{OFF} – I_Y$. This 180-degree phase change can be accounted for by inverting the MSB of the 2's complement EIS_PHASE_ADVANCE[7:0] (0x7E), which has the effect of inverting the drive EIS drive signal.

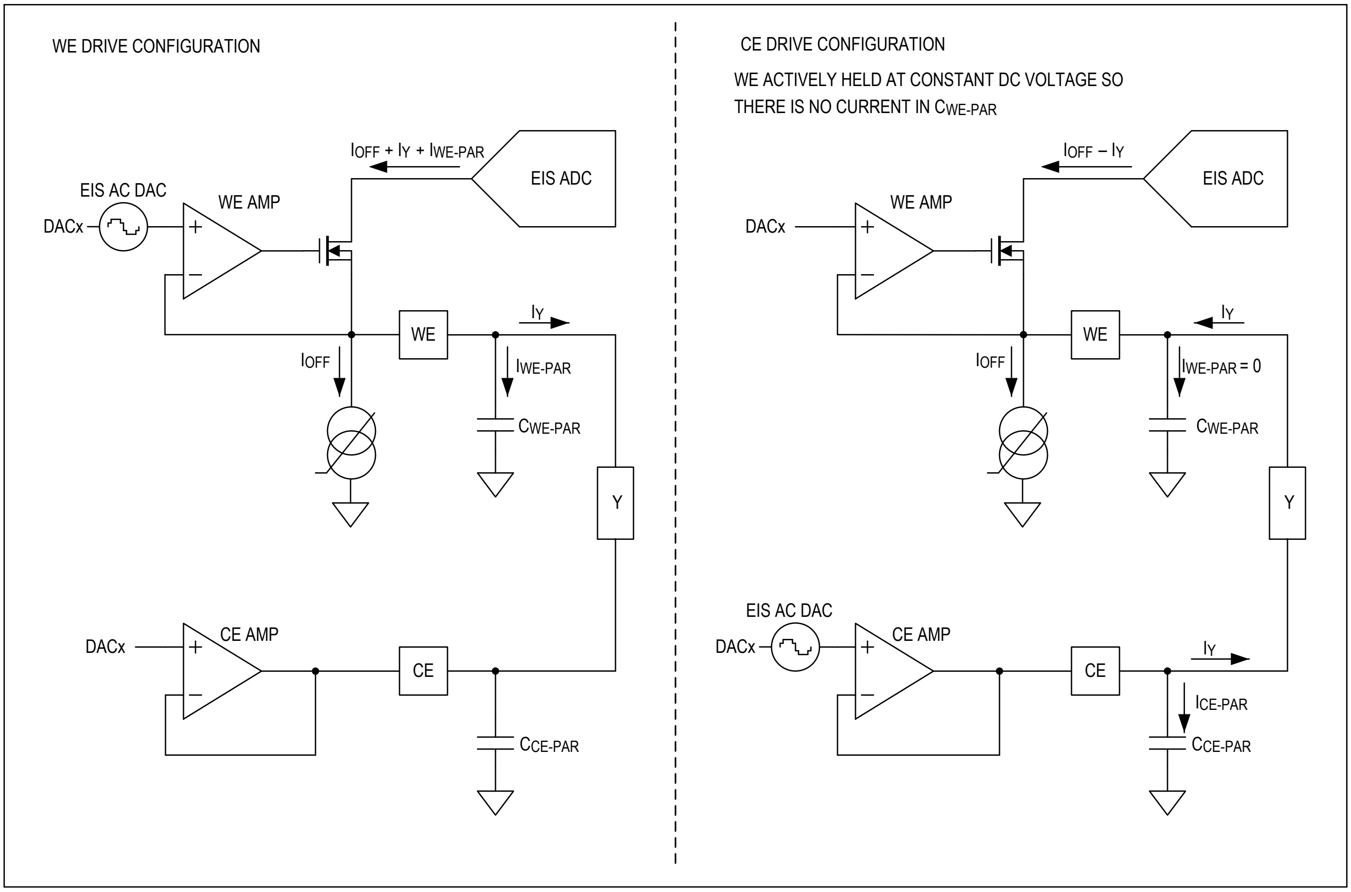


Figure 14. EIS WE and CE Drive Configuration

EIS Amplitude

EIS_AMPLITUDE[3:0] (0x79) sets the amplitude of the EIS sine wave. The available range is $5mV_{P-P}$ to $80mV_{P-P}$.

EIS amplitude = $5mV_{P-P}$ x (EIS_AMPLITUDE[3:0] + 1)

The EIS sine wave is synthesized by a dedicated DAC using 256 samples per cycle for all EIS sine-wave frequencies. There are a few factors to consider when choosing the EIS amplitude. First and foremost, the amplitude should comply with the sensor manufacturer's recommendation. Exceeding the limit can result in damage or unwanted effects in the measured data. Secondly, using a larger amplitude increases the signal and hence the SNR in the case where the noise is dominated by the AFE or the sensor. However, setting the amplitude too large could causes the ADC to saturate.

EIS Settle and Cycle Averages

EIS_SETTLE[3:0] (0x7F) and EIS_NUM_SINEWAVES[2:0] (0x78) control the total number of sine waves to be generated during a measurement. EIS_SETTLE[3:0] can be set to values of 0 through 15 and is the number of sine-wave cycles to be generated before the EIS ADC starts making measurements. EIS settling cycles allows time for any transients to dissipate before a measurement begins.

To reduce noise and improve interference rejection, multiple sine-wave cycles can be averaged during an EIS measurement. EIS_NUM_SINEWAVES[2:0] bits set the number of sine waves over which the EIS ADC averages the measurement.

Number cycles averaged = $2^{\text{EIS\_NUM\_SINEWAVES[2:0]}}$

EIS_NUM_SINEWAVES[2:0] = 0 makes a measurement of 1 sine-wave cycle and EIS_NUM_SINEWAVES[2:0] = 7 makes a measurement averaged over 128 sine-wave cycles.

Phase Advance

When making an EIS admittance, measurement phase errors are caused by the following: (1) EIS DAC zero-order hold that results in a half-period clock delay, (2) Analog buffers multiplexers, mirrors, etc. all have some delay, (3) delta-sigma modulator delays, (4) ADC-decimation filters and correlator delays. The phase of the generated sine wave must be correctly aligned with the phase of the data sampling to obtain the correct I and Q codes. This alignment is accomplished by setting the EIS_PHASE_ADVANCE[7:0] (0x7E) register with a phase advance correction value determined in a calibration procedure for each measurement frequency. Before each measurement at a new EIS frequency, the EIS_PHASE_ADVANCE[7:0] must contain the correct phase advance value before the measurement is started. EIS_PHASE_ADVANCE[7:0] is an 8 bit 2's complement value with each bit representing 360/256 = 1.40625 degrees. For example, a value of 0x05 represents 5 x 1.4 degrees = 7.0 degrees and a value of 0xFC represents -4 x 1.4 degrees = -5.6 degrees. The correct phase advance value for each EIS frequency is determined using the procedure outlined in the *EIS Calibration* section.

EIS ADC Sensor Full-Scale Range and Offset

The EIS ADC full-scale range, EIS_ADC_FS_RANGE[1:0] (0x7D), should be set to maximize the signal-to-quantization noise ratio by using the smallest full-scale range that does not result in saturation in the EIS ADC or its downstream digital filters during a measurement. The available EIS_ADC_FS_RANGE[1:0] settings are 4μA, 8μA, 20μA, and 40μA for codes 0 to 3, respectively. The choice of EIS_ADC_FS_RANGE[1:0] and EIS_AMPLITUDE[7:0] are interrelated. It can be difficult to recognize if an EIS measurement is saturated from the output data and care must be taken to pre-calculate the expected maximum current and ensure that the selected settings do not saturate the EIS ADC. For example, to measure the 13.19kΩ internal calibration resistance with an EIS amplitude of $80mV_{P-P}$ a peak-to-peak current of about 6.1μA is generated. The best choice for the EIS full-scale range is 8μA since this is the smallest selection that is greater than 6.1μA.

It is important that the measured DC-offset current is at the middle of the EIS ADC measurement range to center the EIS AC current in the middle of EIS range and thus, avoid clipping the peaks. This is accomplished by setting the EIS ADC DC offset, EIS_OFFSET[2:0] (0x7C), to an appropriate value.

Available values are 0.125 full-scale range to 0.5 full-scale range in 0.0625 steps.

EIS ADC DC offset = ((8 - EIS_OFFSET[2:0])/16) x EIS full-scale range

EIS_OFFSET[2:0] = 7 (0.0625 x ADC FSR) is not allowed.

If EIS_OFFSET[3:0] is set to 0 (0.5 full-scale range), then zero DC current is in the middle of the EIS ADC range. This is the correct EIS offset to use when the WE and CE Drive voltages are equal. For more details on how to properly set EIS ADC full-scale range, offset, and amplitude, see the *Avoiding Saturation* section.

EIS AFE Switch Settings

EIS circuity can be configured in either a 2-terminal or 3-terminal configuration. For 2-terminal configuration, set EIS_SC (0x7B) = 1 and EIS_SWB (0x7B) = 0 to connect the CE amplifier feedback to the CE pin only. For 3-terminal configuration set EIS_SC = 0 and EIS_SWB = 1, so the CE amplifier feedback is from the RE pin only.

EIS RC Zero Location

EIS_RC[1:0] (0x7B) sets the location of zero in the EIS amplifier. The zero can be used to cancel out the output pole to keep the amplifier stable. The pole location can be calculated as 1.33 x I/C, where C is the effective load capacitance that is not zeroed out by a series resistor at high frequency and I is the AFE bias current set by EIS_ADC_FS_RANGE[1:0]. Match the zero frequency with the pole frequency. If the amplifier oscillates, reduce the zero frequency.

EIS Series Resistor

EIS_RS (0x7C) is used to bypass the 150Ω WE output series resistor. The resistor can help improve WE amplifier stability and is useful when driving high-capacitance loads.

EIS Current Limit

EIS_ILIM_EN (0x7C) enables the current limit on the WE amplifier. The current limit changes with EIS_ADC_FS_RANGE[1:0] with the maximum being 50μA.

Making an EIS Measurement

This section describes how to set up an EIS measurement on sensor 1 in 2-terminal mode. It is assumed that the load impedance at the measurement frequency is greater than 10kΩ such that saturation does not occur with the selected EIS amplitude, and EIS ADC range and offset.

Sensor ADC Setup

First select a sensor channel on which to make the calibration measurement and match the sensor ADC switch setup to the EIS switch setup. This is required because the electrode pins not driven by the EIS sine wave during the measurement retain the voltages set up in the sensor ADC configuration. Also, with the sensor channel selected for the EIS measurement configured to match the EIS setup the voltages on the WE, RE, and CE pins are stable before starting an EIS measurement.

Enable WE and CE amplifiers (S1_WE_AMP_EN = 1 and S1_CE_AMP_EN = 1) and select DACA for WE and CE (S1_WE_DAC_MX[1:0] = 0 and S1_CE_DAC_MX[1:0] = 0) by setting register 0x20 to 0xC0.

Set up switches for 2-terminal measurement (S1_SC = 1 and S1_SRB = 0) and enable sensor 1 (S1_EN = 1), by setting register 0x21 to 0xA0 and register 0x24 to 0x01.

Voltage DAC Setup

Set V_{REF} to 1.536V (REF_VAL[1:0] = 0) and enable it by setting (REF_EN = 1). REF_EN is set to 1 by setting register 0x68 to 0x05.

Set DACA to 0.600V (DACA_CODE[11:0] = 0x640) and enable it (DACA_EN = 1). The voltage setup on the sensor channel CE amplifier is the same voltage used by the EIS CE amplifier. Setting WE and CE voltages to be equal sets the I_{DC} current to zero during EIS measurement. With the EIS offset set to 50% full-scale range, the sine-wave current is centered in the middle of the selected range allowing for the largest amplitude to be used without saturation.

EIS Sensor Setup

Set the EIS DC voltage offset to DACA (EIS_DAC_SELECT[1:0] = 0) and the number of sine wave cycles to an average of 32 (EIS_NUM_SINEWAVE = 5), by setting register 0x78 to 0x28.

Set the EIS sine-wave amplitude to $80mV_{P-P}$ (EIS_AMPLITUDE[3:0] = 15), by setting register 0x79 to 0xF0.

Enable the EIS WE and CE amplifiers and set up the EIS switches for a 2-terminal measurement, (EIS_WE_AMP = 1, EIS_CE_AMP = 1, EIS_SC = 1, EIS_SRB = 0) by setting register 0x7B to 0xE0.

Set the EIS ADC offset to 50% full-scale range (EIS_OFFSET[2:0] = 0), by setting register 0x7C to 0x00.

Set the EIS ADC full-scale range to 8μA (EIS_ADC_FS_RANGE[1:0] = 1) by setting 0x7D to 0x01.

EIS_SETTLE[3:0](0x7F) is typically set to 1 cycle for frequencies below 1Hz and set to 15 cycles for frequencies above 10Hz. Between 1Hz and 10Hz the value should be selected to allow at least 1 second of settling time.

Determining Measurement Time

The time for an EIS measurement to complete depends on the sine-wave frequency, number of sine-wave periods averaged, plus extra cycles added at the beginning according to EIS_SETTLE[3:0]. There is on average an extra half cycle because the EIS always starts and ends at the AC zero crossing. The formula to calculate EIS measurement time is

EIS measurement time = ADC_Setup + (EIS_SETTLE[3:0] + # Cycles Averaged + 0.5) / f_S

where,

ADC_Setup = Setup time (350μs),

f_S = Sine-wave frequency,

For example, the measurement time for a 5kHz and 8 sine waves with EIS_SETTLE[3:0] set to 2 is estimated to be

EIS measurement time = 350μs + (2 + 8 + 0.5) / 5kHz = 2.45ms

EIS Measurement Conversion

With the EIS measurement setup complete, an EIS measurement is made at each desired measurement frequency by setting the frequency select and phase advance registers.

Set the EIS_CLK_DIV[5:0] (0x7A), EIS_FINE_FREQ[3:0] (0x7F), and either FAST_TRIM_ADJUST[0:7] (0x75) or SLOW_TRIM_ADJUST[0:7] (0x76) to generate the desired EIS drive frequency.

Set EIS_PHASE_ADVANCE[7:0](0x7E) to the value determined as outlined in the *EIS Calibration* section.

Read the Status 1 (0x00) register to clear the status flags.

Set the CONVERT (0x83) bit to 1 to start an EIS conversion.

When the EIS conversion is complete the CONVERT bit is cleared and the AC_DATA_RDY(0x00) and FIFO_DATA_RDY(0x00) status bits are set.

Read the code_I (EIS Real) and code_Q (EIS Imaginary) data from the FIFO.

Calculating Admittance, Impedance, and Phase

After each EIS measurement completes, the FIFO is loaded with three different count values, code_I, code_Q, and code_DC. Code_I and code_Q are 16-bit 2’s complement counts representing the in-phase and quadrature-phase admittance measurements, respectfully. Code_DC is a 12-bit count representing the DC current of the measurement. See Table 9 for how to interpret leading data tags and extract the code count from each 3-byte FIFO data word.

The real Y_R and imaginary Y_I admittance are calculated using the following equations.

$$Y_R = \frac{\text{code}_I \times I_{\text{FSR}}}{2^{15} \times K_{\text{CIC}} \times V_{P-P}}, \quad Y_I = \frac{\text{code}_Q \times I_{\text{FSR}}}{2^{15} \times K_{\text{CIC}} \times V_{P-P}}$$

Where,

code_I = 16-bit in-phase code, 2's complement representation,

code_Q = 16-bit quadrature-phase code, 2's complement representation.

I_{FSR} = Full-scale current of EIS ADC set by EIS_ADC_FS_RANGE[1:0] (0x7D),

K_{CIC} = Frequency dependent gain factor of the CIC filter (see Table 2)

$V_{P\text{-}P}$ = Peak-to-peak voltage of the sine wave set by EIS_AMPLITUDE[3:0] (0x79),

The 2^{15} constant instead of the expected 2^{16} constant accounts for the admittances being signed at 16 bits (-32,768 to +32,767). Thus, the code feeding the correlator is adjusted by a factor of 2; otherwise, the admittances would go out of range. The EIS DC measurement is also adjusted by a factor of 2.

Note: if I_{FSR} is in µA and $V_{P\text{-}P}$ is in volts, then the admittance is in units of µS.

To calculate the impedance, first calculate the magnitude of the admittance and then use the relationship |Z| = 1/|Y|, where,

$$|Y| = \sqrt{Y_R^2 + Y_I^2}$$

and

$$|Z| = \frac{1}{|Y|} = \frac{1}{\sqrt{Y_R^2 + Y_I^2}}$$

Since code_I and code_Q are proportional to their respective admittances the phase of the complex admittance vector can be calculated directly from code_I and code_Q. The arctan2(y,x) function is typically used since it preserves the correct sign of the phase for vectors in different quadrants. It is also important to remember that the sign of the phase calculated for admittance has the opposite sign as the phase calculated for impedance. This sign flip arises because Z = 1/Y and when inverting a complex number 1/j = -j. The phase angle for the final calculated impedance will therefore be:

$$\theta_Z = -\arctan2\left(\text{code}_Q, \text{code}_I\right) \times \frac{180}{\pi}$$

If the real Z_R and imaginary Z_I impedance vectors are needed, they can then be calculated from:

$$Z_R = |Z|\cos(\theta_Z) \quad \text{and} \quad Z_I = |Z|sin(\theta_Z)$$

The DC current of the EIS measurement is calculated from the code_DC by:

$$I_{DC} = \frac{code_{DC} \times I_{FSR}}{2^{11}} - \frac{3}{2} \times \frac{I_{FSR} \times (8 - EIS\_OFFSET[2:0])}{16}$$

where,

$code_{DC}$ = Unsigned count from bits 11:0 of an EIS DC current tagged FIFO word,

I_{FSR} = Full-scale-range current set by EIS_ADC_FS_RANGE[1:0] (0x7D),

EIS_OFFSET[2:0] = Unsigned count set in EIS_OFFSET[2:0] (0x7C).

Example Calculation

In this example it is assumed that the following EIS value were set.

EIS_FS_RANGE[1:0] = 1, 8μA

EIS_OFFSET[2:0] = 0, 0.5 full-scale range

EIS_AMPLITUDE[3:0] = 15, 80mV$_{P-P}$

The EIS sine-wave frequency is < 110Hz and the K_{CIC} value is 1.

After the EIS measurement is complete the following three hex code words are read from the FIFO

0x0411EB → Tag = 4, 16-bit code = 0x11EB, 2's complement $code_I$ count = 4587

0x08F47A → Tag = 8, 16-bit code = 0xF47A, 2's complement $code_Q$ count = –2950

0x0F562B → Tag = F5, 12-bit code = 0x62B, $code_{DC}$ count = 1579

$code_I$ and $code_Q$ with a count greater than 32767 are negative since the MSB of the 16-bit code is set to 1 and the negative 2's complement count is calculated by subtracting 65536 from the raw count.

From $code_I$ and $code_Q$, Y_R and Y_I are calculated

$$Y_R = \frac{code_I \times I_{FSR}}{2^{15} \times K_{CIC} \times V_{P-P}} = \frac{4578 \times 8\mu A}{2^{15} \times 1 \times 0.08V} = 13.998\mu S$$

$$Y_I = \frac{code_Q \times I_{FSR}}{2^{15} \times K_{CIC} \times V_{P-P}} = \frac{-2950 \times 8\mu A}{2^{15} \times 1 \times 0.08V} = -9.003\mu S$$

Next |Y| and |Z| are calculated as

$$|Y| = \sqrt{(13.998\mu S)^2 + (9.003\mu S)^2} = 16.643\mu S$$

$$|Z| = \frac{1}{16.643\mu S} \times 1000000\frac{\mu S}{S} = 60,083\Omega$$

Theta, θ_Z, is calculated using an arctan2(y,x) function applied to $code_I$ and $code_Q$.

$$\theta_Z = -\arctan2(-2950, 4587) \times \frac{180}{\pi} = 32.75\,°$$

Next, Z_R and Z_I are calculated to be

$$Z_R = 60,083\Omega \times \cos\left(32.75\,° \times \frac{\pi}{180}\right) = 50,535\Omega$$

$$Z_I = 60,083\Omega \times \sin\left(32.75\,° \times \frac{\pi}{180}\right) = 32,500\Omega$$

A graphical representation of the calculation result is shown in Figure 15.

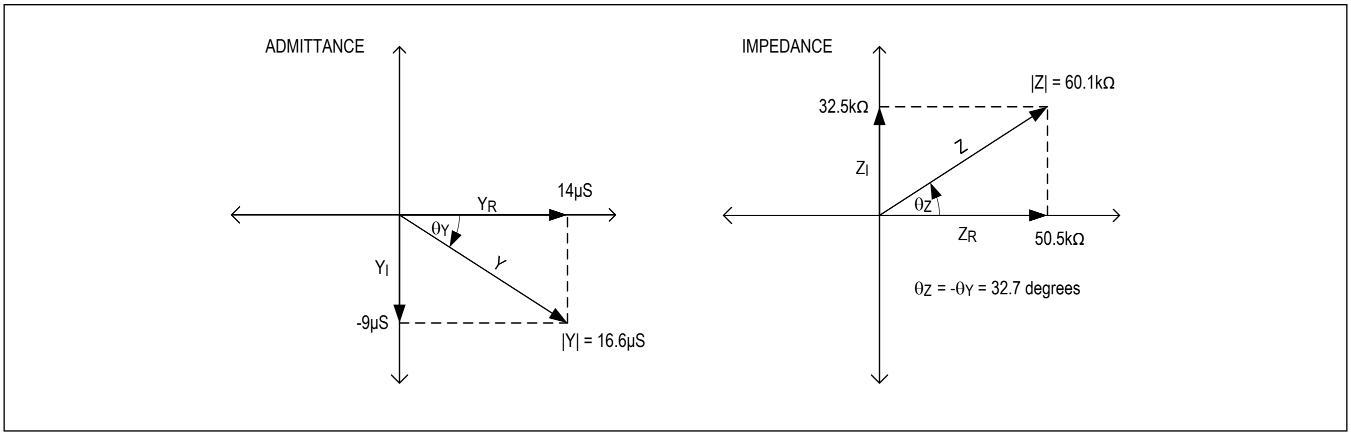


Figure 15. EIS Calculation Example

Finally, the EIS DC current is calculated as

$$I_{DC} = \frac{code_{DC} \times I_{FSR}}{2^{11}} - \frac{3}{2} \times \frac{I_{FSR} \times (8 - \text{EIS\_OFFSET[2:0]})}{16}$$

$$I_{DC} = \frac{1579 \times 8\mu A}{2^{11}} - \frac{3}{2} \times \frac{8\mu A \times (8 - 0)}{16} = 0.168\mu A$$

EIS Calibration

To make accurate EIS phase and magnitude measurements both a phase-advance correction and magnitude-correction factor need to be determined at each measurement frequency. Phase errors are caused by the following: (1) EIS DAC zero-order hold that results in a half-period clock delay, (2) Analog buffers multiplexers, mirrors, etc., all have some delay (3) delta-sigma modulator delays, (4) ADC decimation filters and correlator delays. The phase of the generated sine wave must be correctly aligned with the phase of the data sampling to obtain the correct I and Q codes. This alignment is accomplished by setting the EIS_PHASE_ADVANCE[7:0] (0x7E) register with the phase advance correction. Phase advance correction can be determined by using either the auto-phase advance calibration procedure or by making an EIS measurement of an internal calibration resistor, a purely real impedance, and calculating the phase error. The magnitude correction factor is calculated by making an EIS measurement of an internal calibration resistor and comparing the measurement result with the resistance of the calibration resistor.

Fine Frequency Adjust Calibration

In order to use the fine frequencies with an EIS_FINE_FREQ[3:0] (0x7F) value different from zero, the correct FAST_TRIM_ADJ[7:0] (0x75) or SLOW_TRIM_ADJ[7:0] (0x76) values must be determined. FAST_TRIM_ADJ[7:0] is use for frequencies paired with EIS_CLK_DIV[5:0] codes less than 11 and SLOW_TRIM_ADJ[7:0] is used for frequencies paired with EIS_CLK_DIV[5:0] codes greater than or equal to 11. To determine the correct frequency adjust values, it is required to run a fine-frequency calibration for each frequency setting.

First select the EIS_CLK_DIV[5:0] and EIS_FINE_FREQ[3:0] that corresponds to the desired frequency. Start the frequency adjust calibration by setting EIS_FREQ_TRIM_CAL (0x78) to 1. The EIS_FREQ_TRIM_CAL bit is cleared and the EIS_CAL_DONE (0x00) status bit is set when the calibration completes. The calibration takes about 1ms to complete. For frequencies above 110Hz (EIS_CLK_DIV[5:0] < 11) the calibrated frequency adjust code is placed in the FAST_TRIM_ADJ[7:0] register. For frequencies below 110Hz (EIS_CLK_DIV[5:0] ≥ 11), the calibrated frequency adjust code is placed in the SLOW_TRIM_ADJ[7:0] register. These values can be saved so the next time an EIS_CLK_DIV[5:0] and EIS_FINE_FREQ[3:0] pair is used to select a frequency; calibration is not required and it is only necessary to load the saved value into the FAST/SLOW_TRIM_ADJ register before starting an EIS measurement. Alternatively, users can repeat the calibration every time they change EIS_FINE_FREQ[3:0] (expect code 0), but this takes about 1ms and some energy.

Important Note: Because the fine frequency calibration makes use of the FIFO, it is necessary to always clear the FIFO after the calibration completes.

Direct EIS Calibration Measurement

Phase advance calibration values can be determined directly by making an EIS measurement of a purely real impedance. The results of the EIS measurement is also used to determine the magnitude correction factor, and in practice both the phase advance calibration values and magnitude correction factors are obtained from the same EIS measurement. The basic procedure is to set the phase advance to 0 and make an EIS measurement of the internal calibration resistor. Using the $code_I$ and $code_Q$ values obtained from the measurement, calculate the phase advance error and the impedance magnitude |Z|, then compare this impedance with the actual value of the internal calibration resistor to determine the magnitude correction factor.

Since the 13.19kΩ internal calibration resistor is measured during final factory testing of the device and its variance stored in EIS_CAL_RES_VARIATION[7:0] (0x77), its actual resistance is known to 0.25% and is the best choice for calibration.

EIS Calibration Setup

The following setup is an example and it should be noted that the user is free to use different DAC voltages and DAC channels, different EIS sine-wave setups, etc. All register values not called out should be in their default power-on reset state.

DC Sensor Setup for EIS Calibration

Set up and enable a sensor channel for a 2-terminal measurement, with WE and CE amplifiers driven by DACA.

Set and enable V_{REF} to 1.536V.

Set and enable DACA to 0.600V.

EIS Sensor Setup for Calibration

Set up the sine wave for DACA DC offset, 32-cycle average, and $80mV_{P-P}$

EIS_DAC_SELECT[1:0] (0x78) = 0 (DACA)

EIS_NUM_SINEWAVE[2:0] (0x78) = 5 (32 cycle average)

EIS_AMPLITUDE[3:0] (0x79) = 15 ($80mV_{P-P}$)

Enable the EIS, WE, and CE amplifiers and set up the EIS switches for a 2-terminal measurement, EIS_WE_AMP_EN (0x7B) = 1

EIS_CE_AMP_EN (0x7B) = 1

EIS_SC (0x7B) = 1

EIS_SRB (0x7B) = 0

Set the EIS ADC offset to 50% full-scale range, select the 13.19kΩ internal calibration resistor, and connect the EIS circuity to the selected resistor.

EIS_OFFSET[2:0] (0x7C) = 0 (offset = 50%)

EIS_CAL_RES[1:0] (0x7C) = 2 (13.19kΩ)

EIS_I_CAL_EN (0x7C) = 1 (connect the EIS circuity to the internal calibration resistor only)

With the EIS amplitude set to $80mV_{P-P}$ the peak-to-peak current across the 13.19kΩ resistor is 0.08/13.19kΩ = 6.07µA. This makes 8µA the best choice for the EIS ADC full-scale range.

EIS_ADC_FS_RANGE[1:0] (0x7D) = 1 (8µA).

Set the number of settle cycles from 1 to 15 depending on the selected frequency.

EIS_SETTLE[3:0] (0x7F) is typically set to 0 (1 cycle) for frequencies below 1Hz, and set to 15 (16 cycles) for frequencies above 10Hz. Between 1Hz and 10Hz the value is selected primarily based on how long the measurement takes to complete.

EIS Frequency Setup for Calibration

With the above setup complete, an EIS measurement is made at each desired measurement frequency by setting EIS_CLK_DIV[5:0] (0x7A), EIS_FINE_FREQ[3:0] (0x7F), and either FAST_TRIM_ADJUST[0:7] (0x75) or SLOW_TRIM_ADJUST[0:7] (0x76) to generate the desired EIS drive frequency.

EIS Calibration Measurement

Finally, set EIS phase advance to 0 and start the EIS measurement.

Set EIS_PHASE_ADVANCE[7:0] (0x7E) = 0.

Read the Status 1 (0x00) register to clear the status flags.

Set the CONVERT (0x83) bit to 1 to start an EIS conversion.

When the EIS conversion is complete, the CONVERT bit is cleared and the AC_DATA_RDY(0x00) and FIFO_DATA_RDY(0x00) status bits are set.

Read $code_I$ (EIS Real) and $code_Q$ (EIS Imaginary) data from the FIFO.

Calculating Phase Advance Error

Because we know the measurement was made on a purely real impedance, the phase-advance error, θ_E, is the same as the angle the complex impedance vector makes with respect to the real impedance axis, θ_Z. Since the real and imaginary vectors are proportional to the I and Q codes, the phase-advance error, $\theta_E = \theta_Z = -\theta_Y$, can be calculated directly from $code_I$ and $code_Q$ using the arctan2 function.

$$\theta_E = -\arctan2(code_Q, code_I) \times \frac{180}{\pi}$$

From the phase-advance error θ_E, calculate the 2’s complement code used to set EIS_PHASE_ADVANCE[7:0] for future measurement at this EIS drive frequency.

$$\text{EIS\_PHASE\_ADVANCE}[7:0] = \text{round}\left(\theta_E \times \frac{256}{360}\right)$$

Where EIS_PHASE_ADVANCE[7:0] is an 8-bit 2’s complement formatted number, i.e., 0xFF = –1. Each bit represents 1.4 degrees and the phase advance correction is ±0.7 degrees of the calculated value.

Calculating Magnitude Correction Factor

To calculate the magnitude correction factor, we need to calculate both the actual value of the calibration resistor, R_{CAL}, and the impedance magnitude of the EIS measurement |Z|.

The actual calibration resistor value is calculated using the equation:

$$R_{CAL} = 13,190\Omega \times (1 + 0.0025 \times \text{EIS\_CAL\_RES\_VARIATION}[7:0])$$

where,

EIS_CAL_RES_VARIATION[7:0] is an 8-bit 2's complement formatted number.

For example, if EIS_CAL_RES_VARIATION[7:0] = 0xF9, the 2's complement count is -7 and the measured value of the calibration resistor at factory final test to within 0.25% is:

$$R_{CAL} = 13,190\Omega \times (1 + 0.0025 \times (-7)) = 12,959\Omega$$

Calculate |Z| as outlined in the *Calculating Admittance, Impedance, and Phase* section. The magnitude correction factor, m_{CF}, is the ratio of the actual resistance to the measured resistance and is calculated as:

$$m_{CF}(\text{coarse, fine}) = \frac{R_{CAL}}{|Z|}$$

where m_{CF}(coarse,fine) is a function of the selected frequency, where course is the value set in EIS_CLK_DIV[5:0] and fine is the value set in EIS_FINE_FREQ[3:0].

Repeat this measurement and calculations for each desired measurement frequency and save the phase advance and magnitude correction factors to be used on future measurements.

Auto EIS Phase-Advance Calibration

Auto phase-advance calibration is accomplished by first selecting a measurement frequency by setting EIS_CLK_DIV[5:0] (0x7A), EIS_FINE_FREQ[3:0] (0x7F), and either FAST_TRIM_ADJUST[0:7] (0x75) or SLOW_TRIM_ADJUST[0:7] (0x76) to generate the desired frequency. Before starting the auto-phase advance calibration set EIS_RCAL_RES[1:0] (0x7C) to select one of the internal calibration resistors, and set EIS_I_CAL_EN (0x7C) to

1 to connect the EIS circuity to the calibration resistor. Next, set EIS_PH_ADV_CAL (0x78) to 1—this starts the auto phase-advance calibration. Eight consecutive EIS measurements are made using the current EIS settings and the phase advance error result is placed in EIS_PHASE_ADVANCE[7:0] (0x7E). EIS_PH_ADV_CAL is cleared to indicate completion of the auto EIS phase advance calibration for the selected frequency. Before each future EIS measurement at this EIS drive frequency the EIS_PHASE _ADVANCE[7:0] register must be set to this phase-advance error. The time to complete an auto phase-advance calibration is:

Phase calibration time = 8 x (EIS_SETTLE[3:0] + # Cycles Averaged + 0.5) / f_S

Important Note: After an auto phase-advance calibration completes, the FIFO must be reset as the auto calibration procedure makes use of the FIFO and does not clear it when finished.

Applying Calibrations to an EIS Measurement

Before the start of each EIS measurement, set the measurement frequency by setting the corresponding course-fine code pair and the fine-frequency trim adjust code. For course codes below 11, set FAST_TRIM ADJ[7:0] and for course codes ≥ 11 set SLOW_TRIM_ADJ[7:0] to the code previously determined as described in the *Fine Frequency Adjust Calibration* section.

Set PHASE_ADVANCE[7:0] to the phase advance code calculated from the calibration procedure for the course-fine code pair.

Set EIS_NUM_SINEWAVE[2:0] and EIS_SETTLE[3:0] as needed.

Set EIS_ADC_FS_RANGE[1:0] to maximize signal but avoid saturation.

Take an EIS measurement and read the FIFO to obtain code_I and code_Q values.

Calculate the phase angle, θ_Z, corrected admittances Ycorr_R, Ycorr_I, and |Ycorr|:

$$\theta_Z = -\arctan2\left(\text{code}_Q,\ \text{code}_I\right) \times \frac{180}{\pi}$$

$$\text{Ycorr}_R = \frac{Y_R}{m_{CF}(\text{coarse, fine})} = \frac{\text{code}_I \times I_{FSR}}{2^{15} \times K_{CIC}(\text{coarse}) \times V_{P-P} \times m_{CF}(\text{coarse, fine})}$$

$$\text{Ycorr}_I = \frac{Y_I}{m_{CF}(\text{coarse, fine})} = \frac{\text{code}_Q \times I_{FSR}}{2^{15} \times K_{CIC}(\text{coarse}) \times V_{P-P} \times m_{CF}(\text{coarse, fine})}$$

where,

I_{FSR} = EIS full-scale range,

$V_{P\text{-}P}$ = EIS peak-to-peak amplitude,

m_{CF}(coarse,fine) = Magnitude correction factor for the coarse-fine code frequency pair,

K_{CIC}(coarse) = Frequency dependent gain factor of the CIC filter.

$$|\text{Ycorr}| = \sqrt{\text{Ycorr}_R^{\,2} + \text{Ycorr}_I^{\,2}}$$

Calculate corrected impedances |Zcorr|, Zcorr_R, and Zcorr_I from |Ycorr| and θ_Z.

$$|\text{Zcorr}| = \frac{1}{|\text{Ycorr}|}$$

$$\text{Zcorr}_R = |\text{Zcorr}| \times \cos\left(\theta_Z\right)$$

$$\text{Zcorr}_I = |\text{Zcorr}| \times \sin\left(\theta_Z\right)$$

Figure 16 is a graphical representation of the applied correction factor.

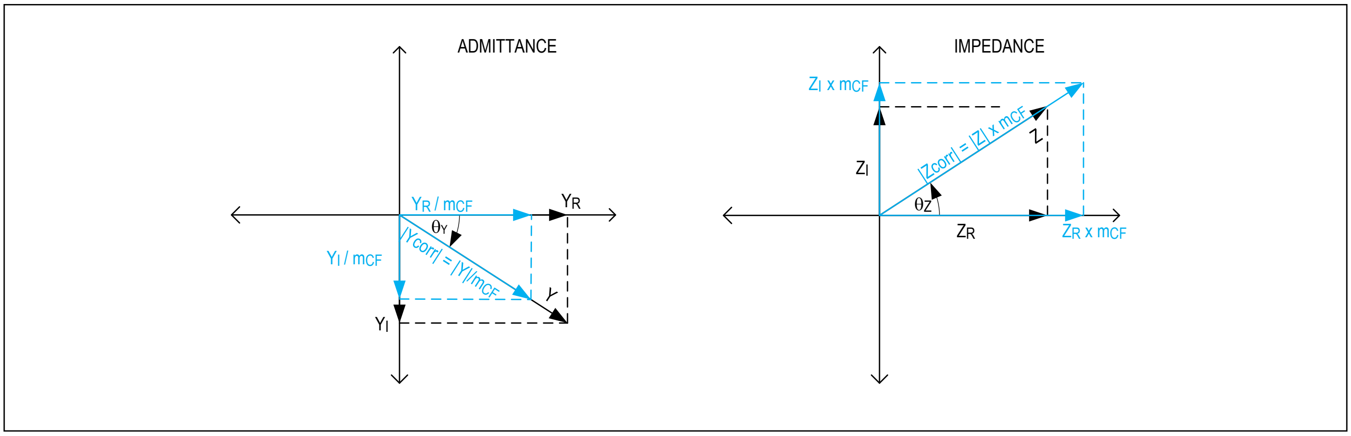


Figure 16. EIS Magnitude Correction Factor

Optimization

Avoiding Saturation

When making an EIS measurement, care must be taken to avoid saturation by ensuring that the EIS current signal seen by the EIS ADC remains within its full-scale range limits. Saturation is defined as signal clipping and or ADC count underflow/overflow in the digital filters. It is possible to calculate if clipping of the current at the lower limit has occurred from the EIS FIFO data. Clipping of the EIS current signal at the high limit can not be determined from the FIFO data.

Clipping at the lower current limit is defined by the inequality.

$$16 \times \text{code}_{DC} - \frac{\sqrt{\text{code}_I^2 + \text{code}_Q^2}}{2} \le 0$$

There is no substitute for carefully calculating the expected current when setting up an EIS measurement to ensure saturation does not occur. One clue that saturation might have occurred from clipping at the high limit is a calculated phase angle θ_Z >> |90| degrees. Phase angles to the left of the imaginary axis typically happen because the EIS phase advance angle for the measurement frequency was incorrectly set or overflow has occurred on the high limit, causing a large positive 2's complement count to wrap around to a large negative count. Not all high-limit clipping results in large phase angles.

If the expected range of the EIS impedance measurement is known, one can calculate the expected signal and DC-offset current (I_{DC}), then select the EIS amplitude, EIS full-scale range (FSR), and EIS offset to ensure saturation does not occur. If the EIS sine-wave, DC-voltage offset, and the applied return electrode voltage are equal the EIS_OFFSET[2:0] (0x7C) should be set to 0 (0.5 x FSR). This centers the measured EIS current signal in the selected EIS full-scale range when there is no DC-current component. The EIS ADC input range is always from 0 to the full-scale range setting. The selected offset current is subtracted from the measured current before it is presented to the EIS ADC. An offset of 0.5 x FSR sets the effective measurement range from -FSR / 2 to +FSR / 2. An EIS full-scale range of 8μA and an EIS offset 0.5 x FSR results in an effective current range of -4μA to 4μA.

As an example, consider measuring the 13.19kΩ calibration resistor with an EIS amplitude of 80mV$_{P-P}$, EIS FSR of 8μA, and an EIS offset of 0.5 x FSR with the average WE drive voltage equal to the CE/RE return electrode voltage. The measured current signal amplitude is calculated as 80mV / 13.19kΩ = 6.07μA and the DC current is 0μA. Figure 17 show the resulting EIS current with respect to the effective EIS FSR in the left plot. The middle plot shows current clipping that occurs if there is a DC-offset current of 3.03μA brought about by driving the average WE drive voltage 40mV greater than the CE/RE return electrode voltage, I_{DC} = 40mV/13.19kΩ = 3.03μA. The plot on the right show how adjusting the EIS-offset current moves the full-scale range limits so clipping no longer occurs when the 3μA DC-offset current is present. In this case the EIS-offset current is set to 0.125 x FSR or 0.125 x 8μA = 1μA, having the effect of subtracting 1μA from the EIS ADC 0 to 8μA range and resulting in an effective range of -1μA to 7μA.

For impedances less than 2kΩ, the EIS amplitude must be less than 80mV$_{P-P}$ to avoid saturation. 80mV/2kΩ = 40μA the maximum EIS FSR available. Ideally EIS amplitude, FSR and Offset should be adjusted so that the AC-current signal is centered in EIS FSR and the current amplitude is as large as possible without clipping the signal.

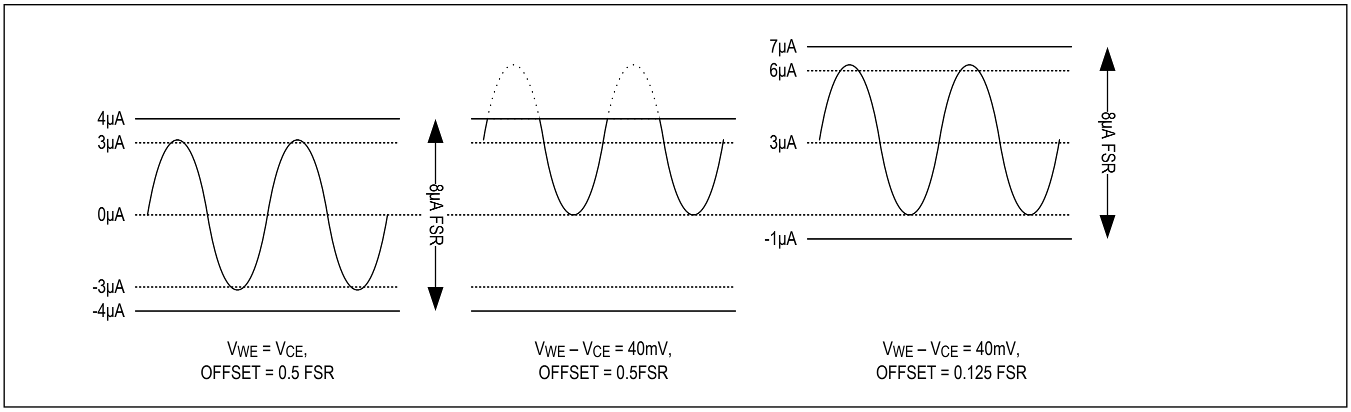


Figure 17. EIS Calibration Resistor Measurement Current

EIS Frequency Response

The frequency response of the EIS signal path H(f) for frequencies above 110Hz is shown below, with no attenuation at the stimulus frequency, f_S.

$$H(f) = \mathrm{sinc}^2\left(\frac{N \times \pi \times (f - f_S)}{f_S}\right), \text{ where } \mathrm{sinc}(x) = \sin(x)/x$$

and the noise equivalent bandwidth (NEB) is

$$\mathrm{NEB} = \frac{f_S}{N}$$

To improve the noise performance, the NEB can be lowered by increasing the number of sine waves (N) that are averaged during an EIS measurement. For example, if the noise is coming in externally, going from N = 1 to N = 2 cycles improves the noise by 3dB or 2dB unless the noise is dominated by the quantization noise of the ADC. Note the signal is normalized regardless of the number of cycles averaged.

The EIS signal path bandwidth is widest for f_S = 20kHz and N = 1. This is plotted below in Figure 18.

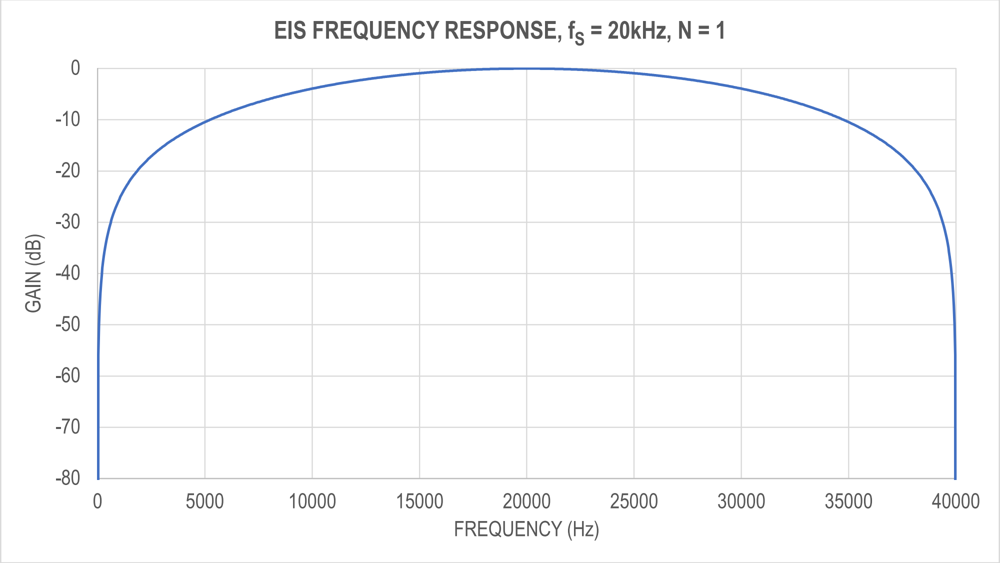


Figure 18. EIS Frequency Response with a Stimulus of 20kHz and Only One Cycle Integrated (N = 1)

Placing a Null Near 60Hz

Figure 19 shows many nulls that occur when the argument of the transfer-function sinc() is a positive integer multiple of PI. In North America, due to the power grid running at 60Hz, it might be desirable to put a null at 60Hz. For a given frequency response of

$$H(f) = \mathrm{sinc}^2\left(\frac{N \times \pi \times \left(f - f_S\right)}{f_S}\right)$$

the null frequencies occur when:

$$N = \frac{k \times f_S}{\left|f - f_S\right|}$$

where k is a positive integer (e.g., 1, 2, 3, …) and N = 1, 2, 4, 8, 16, …, 128 where N is equivalent to the number of sine-wave cycles in the stimulus. For example, to null 60Hz with a stimulus frequency of 156.25Hz, for k = 5, gives N = 8.11, choose N = 8 and a null close to 60Hz is obtained. Figure 19 shows that example.

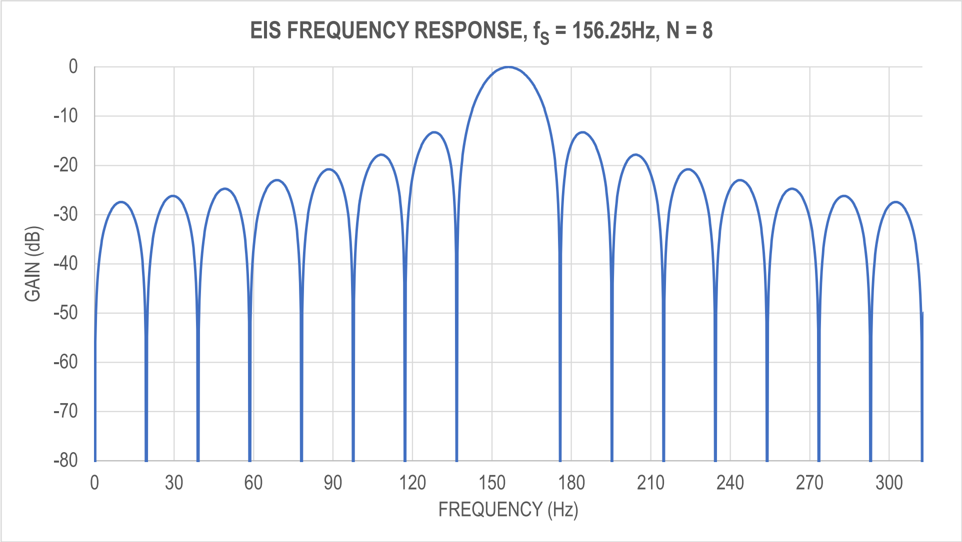


Figure 19. Frequency Response with a Stimulus of 156.25Hz and N = 8, Null Near 60Hz

Measurement Repeatability

A resistance measurement was repeated 40 times with the following settings: V_{P-P} = 40mV, I_{FSR} = 20μA, f = 1250Hz, N = 8.

Mean Resistance = 6586.9Ω

Standard Deviation = 10.37Ω or 0.157% relative to the mean.

If the measurement is not quantization-noise limited then the repeatability is improved as N is increased beyond 8, improving roughly $\sqrt{2}$ for every doubling of N.

Extracting Parasitics

When making complex admittance or impedance measurements, the presence of a parasitic shunt capacitance or series resistance can affect the accuracy of the measurement. These situations are shown in Figure 20

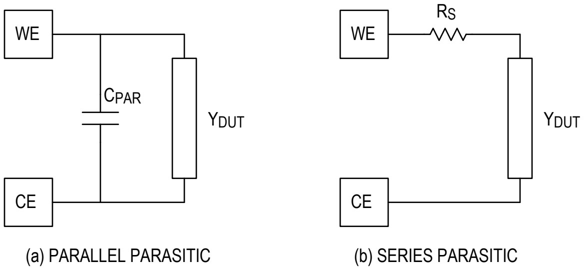


Figure 20. Parasitic C and R

Provided the above shunt capacitance C_{PAR} and series resistance R_S are known, they can be subtracted from the measured admittance or impedance using the equations below:

$Y_{MEAS} = Y_{DUT} + Y_{PAR} = Y_{DUT} + j\omega C_{PAR}$

or

$Y_{DUT} = Y_{MEAS} - j\omega C_{PAR}$.

and

$$Z_{MEAS} = \frac{1}{Y_{MEAS}} = Z_{DUT} + Z_{PAR} = Z_{DUT} + R_S$$

or

$$Z_{DUT} = Z_{MEAS} - R_S.$$

Subtracting R_S from the measured admittance is most useful when the on-chip resistor RS_{EIS} is introduced to stabilize the WE amplifier for large capacitive loads.The value of RS_{EIS} is typically 150Ω and the actual value can be calculated using the formula below:

RSEIS = 150Ω x (1 + 0.0025 x EIS_CAL_RES_VARIATION[7:0])

where, EIS_CAL_RES_VARIATION[7:0] is an 8 bit 2's complement formatted number.

Cyclic Voltammetry Mode

Cyclic voltammetry (CV) is enabled by setting SENS_CONV_TYP (0x80) to 1 and AC_MODE[1:0] (0xA0)to 1. In this mode, the waveform shown in Figure 21 is generated on the selected WE pin when CONVERT (0x83) is set to 1.

The parameters in the CV timing diagram are defined as the following:

V_{START} is set by the DC DAC selected by EIS_DAC SEL[1:0] (0x78)

V_{STEP} is set by (EIS_DAC_INC[3:0] + 1) x $V_{REF}/2^{12}$, EIS_DAC_INC[3:0] (0xA0)

V_{STOP} is set by EIS_DAC_STOP[11:0] (0xA1)

t_{STEP} is set by EIS_CLK_DIV[4:0] (0x7A)

t_{ADC} (EIS ADC Conversion time) is set by EIS_INTEG (0xA0)

t_{ADC_PRE} = 175µs

The staircase waveform is generated by incrementing the code of the DC DAC, selected by EIS_DAC_SEL[1:0] by the number of LSBs specified in EIS_DAC_INC[3:0]. The selected DACx_CODE[11:0] (0x69, 0x6B, 0x6D, 0x6F) (where x = A, B, C, or D) continues incrementing until the code reaches the stop code specified in EIS_DAC_STOP[11:0]. Then, DACx_CODE[11:0] decrements back to its initial value using the code step-size specified in EIS_DAC_INC[3:0]. The ramp reaches the V_{STOP} condition or based on the DAC code settings below.

1. EIS_DAC_STOP[11:0] = DACx_CODE[11:0] + N x (EIS_DAC_INC[3:0] + 1), the ramp completes N steps and reaches EIS_DAC_STOP[11:0], where N is the number of steps in the staircase.
2. EIS_DAC_STOP[11:0] ≠ DACx_CODE[11:0] + N x (EIS_DAC_INC[3:0] + 1), the ramp completes N - 1 steps and reaches DACx_CODE[11:0] + (N - 1) x (EIS_DAC_INC[3:0] + 1).

After reaching the EIS_DAC_STOP[3:0] condition, the DACx_CODE[11:0] is decremented back to its initial value using the same number of steps in the incrementing ramp.

At each step in the staircase waveform, the EIS ADC performs two ADC conversions. One at the midpoint of the step and one at the end of the step. In CV mode, the full-scale current of the EIS ADC is set by EIS_ADC_FS_RANGE[1:0] (0x7D), and the integration time is set by EIS_INTEG (0xA0). EIS_INTEG is programmable to either 50µs or 200µs by setting EIS_INTEG to 0 or 1, respectively. At the end of each ADC conversion, the data is tagged and stored in the FIFO.

The length of each step in the staircase (t_{STEP}) is programmed by EIS_CLK_DIV[4:0] (0x7A). In CV mode, the EIS_CLK_DIV[4:0] codes are restricted depending on the value of EIS_INTEG. For EIS_INTEG set to 0 (t_{ADC}=50µs), the allowable codes are 0x07 through 0x0A, corresponding to step lengths of 0.8ms, 1.6ms, 3.2ms, and 6.4ms. For EIS_INTEG set to 1 (t_{ADC} = 200µs), the allowable codes are 0x08 through 0x0A corresponding to step lengths of 1.6ms, 3.2ms, and 6.4ms.

When making CV measurements, the EIS ADC current data is saved in the FIFO using a 16-bit unsigned number and shares the same tags (0x04 through 0x07) as Sensor n EIS REAL (Table 9). To convert the codes to current when taking data in CV or SWV mode, use the equation:

$$I = \frac{3}{2}\left(\frac{\text{codes}}{2^{16}} \times I_{FSR} - \frac{(8 - \text{EIS\_OFFSET}[2:0])}{16} \times I_{FSR}\right)$$

where,

Codes = Decimal value from bits 15:0 of the CV tagged FIFO data word

I_{FSR} = EIS ADC full-scale range set by EIS_ADC_FS_RANGE[1:0] (0x7D)

EIS_OFFSET[2:0] = Unsigned count set in EIS_OFFSET[2:0] (0x7C)

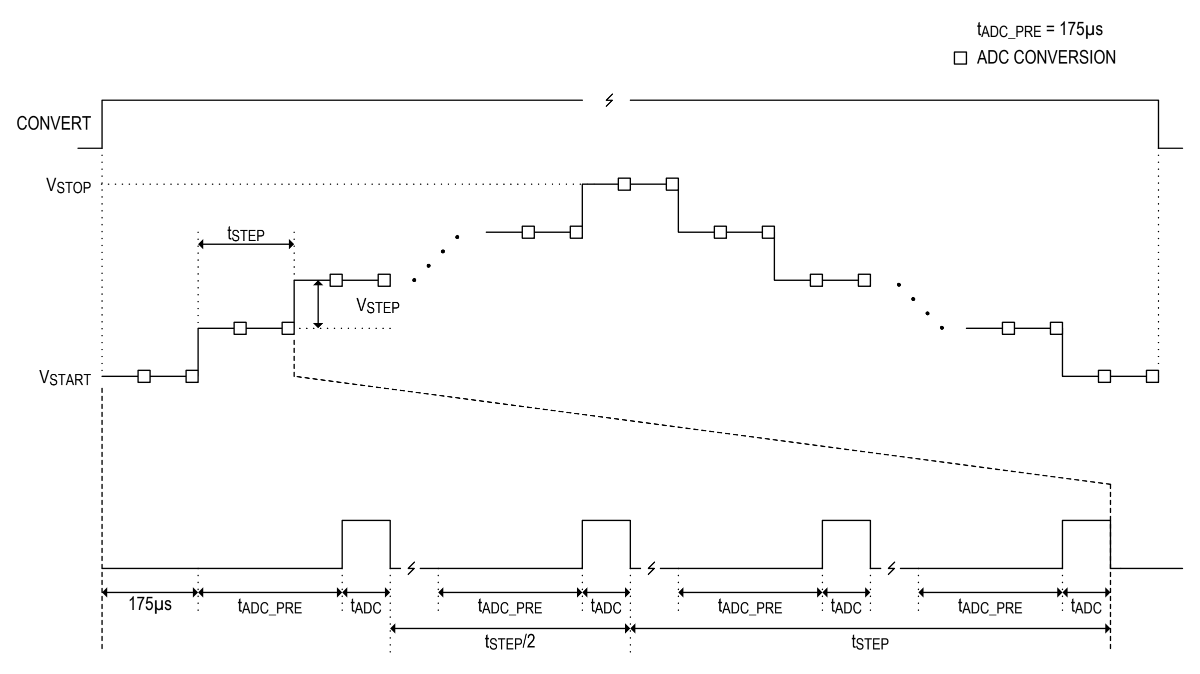


Figure 21. CV Timing Waveform

Square Wave Voltammetry Mode

SWV is entered by setting SENS_CONV_TYPE (0x80) to 1 and AC_MODE[1:0] (0xA0) to 2. In this mode, the waveform shown below in Figure 22 is generated on the selected WE pin when CONVERT is set to 1.

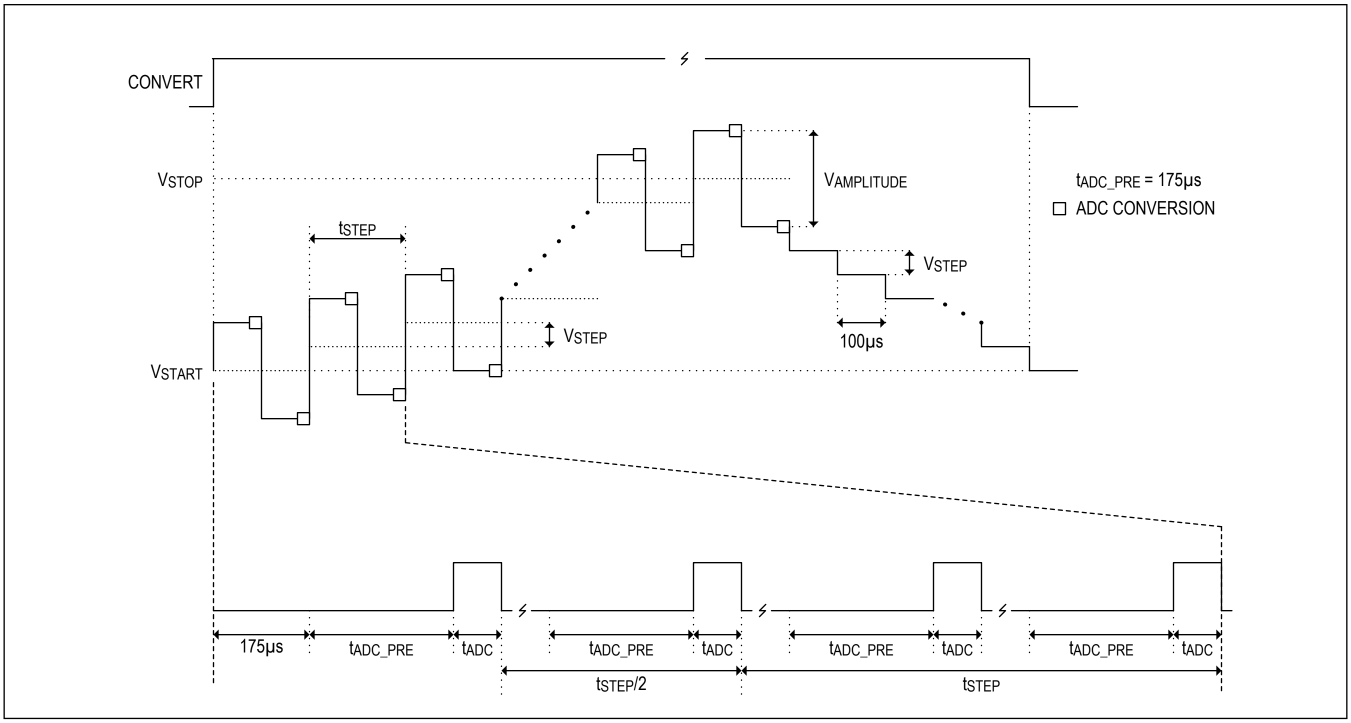


Figure 22. SWV Timing Waveform

The parameters in SWV timing diagram are defined as the following:

V_{START} is set by the DC DAC selected by EIS_DAC SEL[1:0] (0x78)

V_{STEP} is set by (EIS_DAC_INC[3:0] + 1) x V_{REF} / 2^{12}, EIS_DAC_INC[3:0] (0xA0)

V_{STOP} is set by EIS_DAC_STOP[11:0] (0xA1)

t_{STEP} is set by EIS_CLK_DIV[4:0] (0x7A)

$V_{AMPLITUDE}$ is set by EIS_AMPLITUDE[3:0] (0x79)

t_{ADC} (EIS ADC Conversion time) is set by EIS_INTEG (0xA0)

t_{ADC_PRE} = 175µs

The square-wave staircase waveform is created by generating consecutive square-wave pulses each having their DC offset incremented by V_{STEP} until the DC offset reaches V_{STOP}. The waveform generator then decrements the DC offset back to V_{START} with short, 100µs, steps. In SWV mode, DC offset steps are controlled by incrementing the code of the DC DAC, selected by EIS_DAC_SEL[1:0] by the number of LSBs specified in EIS_DAC_INC[3:0]. The selected DACx_CODE[11:0] (0x69, 0x6B, 0x6D, 0x6F) (where x = A, B, C, or D) continues incrementing until the code reaches the stop code specified in EIS_DAC_STOP[11:0]. Then DACx_CODE[11:0] decrements back to its initial value. The ramp reaches the V_{STOP} condition based on the DAC code settings below.

1. EIS_DAC_STOP[11:0] = DACx_CODE[11:0] + N x (EIS_DAC_INC[3:0] + 1), the ramp completes N steps and reaches EIS_DAC_STOP[11:0], where N is the number of steps in the staircase.

2. EIS_DAC_STOP[11:0] ≠ DACx_CODE[11:0] + N x (EIS_DAC_INC[3:0] + 1), the ramp completes N - 1 steps and reaches DACx_CODE[11:0] + (N - 1) x (EIS_DAC_INC[3:0] + 1).

After reaching the EIS_DAC_STOP[3:0] condition, the DACx_CODE[11:0] is decremented back to its initial value using the same number of steps in the incrementing ramp but with short, t_{STEP} = 100µs steps.

At each step in the staircase, a single cycle square wave is superimposed on the step. The amplitude of the square wave is set by EIS_AMPLITUDE[3:0] (0x79) and is programmable from ±2.5mV to ±40mV about the DC step value. Since the amplitude set by EIS_AMPLITUDE[3:0] is independent of V_{REF}, the user must ensure that V_{REF} x EIS_DAC_STOP[11:0] / 2^{12} + EIS_AMPLITUDE[3:0] / 2 < V_{REF}.

The EIS ADC performs two ADC conversions. One at the end on the positive phase of the square wave and one at the end of the negative phase of the square wave. In SWV mode, the full-scale current of the EIS is still set by EIS_ADC_FS_RANGE[1:0] (0x7D), but the integration time is set by EIS_INTEG (0xA0) and is programmable to either 50µs or 200µs. At the end of each ADC conversion the data is tagged and stored in the FIFO.

The period of each step in the staircase (t_{STEP}) and in turn the period of the square wave superimposed on staircase is programmed by EIS_CLK_DIV[4:0] (0x7A). In SWV mode, the EIS_CLK_DIV[4:0] codes are restricted depending on the value of EIS_INTEG. For EIS_INTEG set to 0 (t_{ADC} = 50µs), the allowable codes are 0x07 through 0x0A corresponding to single cycle frequencies of 1250Hz, 625Hz, 312.5Hz, and 156.25Hz. For EIS_INTEG set to 1 (t_{ADC} = 200µs), the allowable codes are 0x08 through 0x0A corresponding to single-cycle frequencies of 625Hz, 312.5Hz, and 156.25Hz.

When the DACx_CODE[11:0] (0x69, 0x6B, 0x6D, 0x6F) reaches its stop value, ADC conversions stop, and the staircase decrements back to its initial value at a fixed period of approximately 100µs and no ADC conversions are done.

When making SWV measurements, the EIS ADC current data is saved in the FIFO using a 16-bit unsigned number and shares the same tags, 0x04 thru 0x07, as Sensor n EIS REAL (Table 9). To convert the codes to current when taking data in CV or SWV mode use the equation:

$$I = \frac{3}{2}\left(\frac{\text{codes}}{2^{16}} \times I_{FSR} - \frac{(8 - \text{EIS\_OFFSET}[2:0])}{16} \times I_{FSR}\right)$$

where,

Codes = Decimal value from bits 15:0 of the SWV tagged FIFO data word

I_{FSR} = EIS ADC full-scale range set by EIS_ADC_FS_RANGE[1:0] (0x7D)

EIS_OFFSET[2:0] = Unsigned count set in EIS_OFFSET[2:0] (0x7C)

System ADC

The analog-to-digital converter input is a single-ended analog voltage and the output is a 12-bit binary digital word. The system ADC can perform voltage readings from 22 different input sources. These sources are separated into three different categories: GPIO inputs, sensor electrodes, and supplies. Each of these categories has an independent gain amplifier setting. The input reference to the ADC is programmable and is present on the REF pin. The programmable gain amplifier (PGA) with high input impedance provides a gain of ¼, ½, 1, or 2. Each input category is programmed to use an independent gain. For the GPIO inputs, the PGA is set by SYS_AIN_GAIN[1:0] (0x54); for the V_{DD} and GND inputs, the PGA is set by SYS_PWR_GAIN[1:0] (0x54); and for the WOn, WEn, REn and CEn sensor voltage inputs, the PGA gain is set by SYS_SENSV_GAIN[1:0] (0x54). Gains less than 1 can be used to measure voltages greater than the reference voltage, but less than the supply voltage. External voltages greater than the supply voltage, but less than the absolute maximum voltage, can be measured when the system input buffer is bypassed; OPA_BYPASS_EN (0x54) set to 1. When the input voltage buffer is bypassed, the signal must be able to drive a 14MΩ load. When OPA_BYPASS_EN = 0, the input voltage buffer is enabled, and the input signal loading is negligible. For all supply and GPIO inputs, the gain must be set such that the input voltage is less than V_{REF}.

The supply voltages can be monitored for remaining battery life calculation as well as ensuring that there is enough supply voltage to operate the device. Remote temperature can be monitored using the external inputs with a thermistor to ensure operation within a specified temperature range or to adjust for any temperature dependence with the sensors. Sensor voltages can be monitored for compliance and to ensure that the sensor is biased and functioning properly.

There is a programmable digital alarm that can detect when a measurement is above or below the programmed alarm threshold. When the alarm is tripped, it asserts a status bit and generates an interrupt if enabled. The number of trips can be programmed and if the trips are required to be consecutive or not. See the *System ADC Alarms* section.

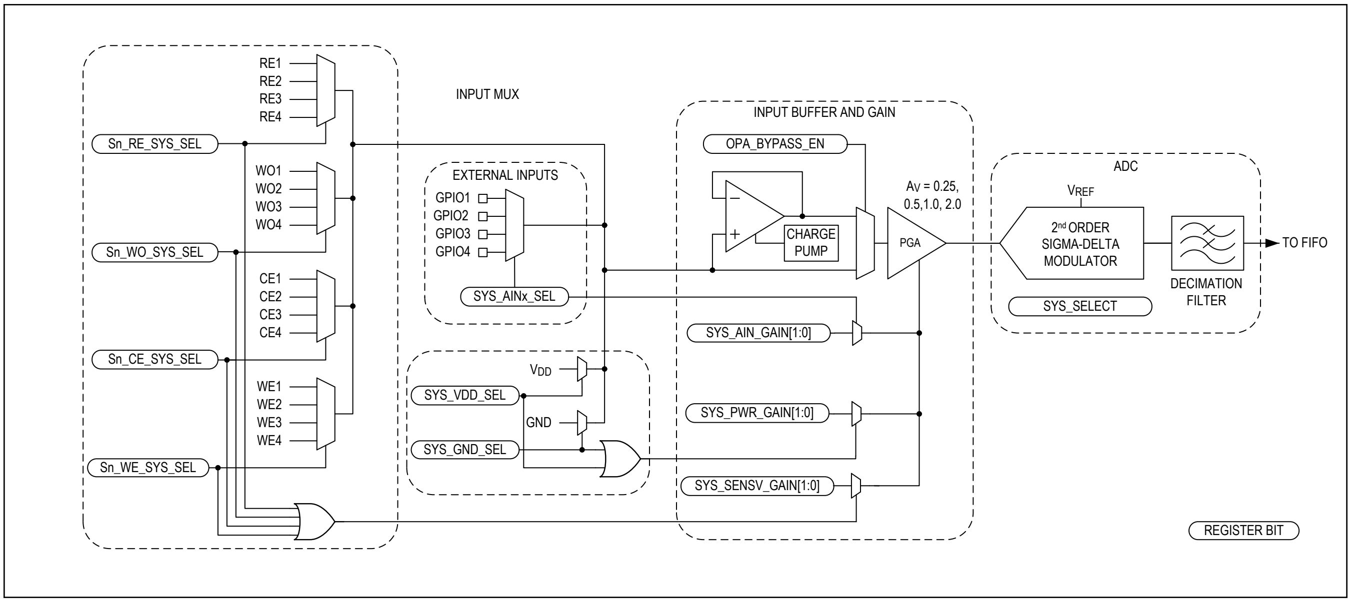


Figure 23. System ADC

To set up system ADC voltage measurements, SYS_SELECT (0x55) must be set to 1, and one or more of the system input select bits must be set to 1. GPIO input signals are controlled by AINn_SYS_SEL (0x55), where n = 0, 1, 2, or 3. Supply input signals are controlled by VDD_SYS_SEL and GND_SYS_SEL (0x55). The sensor input signals are controlled by Sn_WE_SYS_SEL, Sn_RE_SYS_SEL, Sn_CE_SYS_SEL, and Sn_WO_SYS_SEL (0x56, 0x57). The selected inputs are measured sequentially by the system ADC when CONVERT (0x83) is set to 1. When all selected system ADC voltage measurements are complete, status bit SYS_ADC_DATA_RDY (0x01) is set to 1.

The system ADC can be set for single conversion or automatic conversion by the AUTO (0x83) bit. If AUTO = 1 the system ADC continuously converts the selected inputs at the rate determined by SYS_PERIOD[3:0] (0x81). If AUTO = 0, then the system ADC converts each selected input once.

The system ADC input voltage is calculated using this formula:

$$V_{IN} = \text{ADC\_CODE} \times \frac{V_{REF}}{2^{12} \times \text{GAIN}}$$

where:

ADC_CODE = 12-bit system ADC output code

V_{REF} = REF pin voltage

GAIN = Gain of the PGA (¼, ½, 1, or 2.)

System ADC Offset

Offset in the system ADC signal path adds error to the measurement. Offset errors can be handled by the system ADC in one of two ways:

When SYS_CONV_TYPE (0x80) is set to 0, the system ADC completes an offset and an offset + signal measurement for each input selected. The offset measurement count is subtracted from the offset + signal measurement count and the resulting signal count is placed in the FIFO.

When SYS_CONV_TYPE is set to 1, the system ADC completes an offset measurement only once for each category of input signals (supply, sensor, or GPIO), and completes an offset + signal measurement for each selected input. The single offset measurement count for a category will be subtracted from the offset + signal measurement count of each measurement in that category. The resulting signal count for each measurement is placed in the FIFO.

The offset count used in the last system ADC voltage measurement is available to the user in the read-only register

SYS_VOFFSET[11:0] (0x5E, 0x5F).

Temperature Sensor

The temperature sensor provides measurements with ±0.5°C accuracy over the body temperature range of +30°C to +50°C and an accuracy of ±1.0°C over 0°C to +70°C. The resolution of the temperature sensor is 16 bits, corresponding to a resolution of 0.00513°C. The temperature data is stored as a left-justified, 16-bit sign-extended 2's complement number in the FIFO. Table 5 gives examples of digital output data and the corresponding temperature reading for 16-bit resolution conversions.

To calculate the temperature from the measurement result, convert the 2's complement value to the decimal value and divide by 195.

$$T = \frac{2'scomp(codes)}{195}$$

For example, if the result is 0x1C2F, then convert the result to a decimal format to get 7215 decimals, then divide by 195 to convert the codes to temperature T = 7215/195 or +37°C.

Table 5. 16-BIT TEMPERATURE DATA FORMAT

TEMPERATURE (°C)	DIGITAL OUTPUT (BINARY)	DIGITAL OUTPUT (HEXADECIMAL)	DIGITAL OUTPUT (DECIMAL)
+70	0011 0101 0101 0010	3552	13,650
+37	0001 1100 0010 1111	1C2F	7,215
+15	0000 1011 0110 1101	0B6D	2,925
+2	0000 0001 1000 0110	0186	390
+1	0000 0000 1100 0011	00C3	195
+0.3333	0000 0000 0100 0001	0041	65
+0.1026	0000 0000 0001 0100	0014	20
+0.0103	0000 0000 0000 0010	0002	2
+0.0051	0000 0000 0000 0001	0001	1
0	0000 0000 0000 0000	0000	0
-0.0051	1111 1111 1111 1111	FFFF	-1
-1	1111 1111 0011 1101	FF3D	-195

The output temperature data is calibrated in degrees Celsius; for Fahrenheit applications, a lookup table or conversion routine must be used. To initiate a temperature measurement and analog-to-digital conversion, set TEMP_SELECT to 1 and CONVERT to 1. If AUTO is set to 0, then a single temperature measurement is performed. If AUTO is set to 1, then continuous temperature conversion is performed at the period set by TEMP_PERIOD[3:0]. To stop continuous temperature measurements, set CONVERT to 0.

Alarms

Sensor ADC Alarms

In this section, the functions of registers Sn_LO_MODE, Sn_LO_TRIP, Sn_LO_TRIP_CNT[1:0], Sn_LO_DET_CNTR[2:0] and Sn_RST_LO_CNTR at address (0x25, 0x32, 0x3F, 0x4C) and Sn_HI_MODE, Sn_HI_TRIP, Sn_HI_TRIP_CNT[1:0], Sn_HI_DET_CNTR[2:0] and Sn_RST_HI_CNTR at address (0x26, 0x33, 0x40, 0x4D), where n = 1, 2, 3, or 4 are described.

Each sensor channel has independent alarm functions and configurations. Each channel has independent upper and lower alarms, where x = HI (upper alarm) or LO (lower alarm). The alarms can be configured to work with either the absolute ADC count, Sn_x_MODE set to 0, or the difference between the current ADC count and previous ADC count, Sn_x_MODE set to 1. In difference mode, only positive differences are compared with the upper threshold and only negative differences are compared with the lower threshold. This allows the user to set an alarm for the maximum rate of positive and/or negative current change from the sensor. In addition, each alarm can be configured to trip on 1 to 4 consecutive threshold crossings, Sn_x_TRIP_CNT[1:0] and Sn_x_TRIP set to 0, or 1 to 4 accumulated threshold crossings, Sn_x_TRIP_CNT[1:0] and Sn_x_TRIP = 1. The current number of threshold crossings is stored in a read-only register, Sn_x_DET_CNTR[2:0], that can be reset by the user at any time by setting Sn_RST_x_CNTR to 1. When a given alarm condition is met, the status bit for that alarm, Sn_ADC_DATA_x (0x02, 0x03), is set in the status register block. If desired, this can trigger an interrupt on INTB by setting the corresponding interrupt enable bit Sn_ADC_DATA_x_EN to 1 (0x07, 0x08). The upper and lower alarm thresholds are user programmable and are stored in registers Sn_HI_THRESH[15:0] (0x29, 0x36, 0x43, 0x50) and Sn_LO_THRESH[15:0] (0x27, 0x34, 0x41, 0x4D). At power-on reset, the default values are 0xFFFF and 0x000, respectively. More details can be found in the register map descriptions.

System ADC Alarms

The alarm functions for the system ADC only work on the current ADC count. There is no differential mode for the system ADC alarms. Like the sensor ADC, the system ADC has independent upper and lower alarms, where x = HI (upper alarm) or LO (lower alarm) that can be configured to trip on 1 to 4 consecutive alarm crossings, SYS_x_TRIP_CNT[1:0] and SYS_x_TRIP set to 0, or 1 to 4 accumulated alarm crossings, SYS_x_TRIP_CNT[1:0] and SYS_x_TRIP set to 1. The current trip count is stored in a read only register' SYS_x_DET_CNTR[2:0] (0x58, 0x59), which can be reset by the user at any time by setting SYS_RST_x_CNTR (0x58, 0x59) to 1. When a given alarm condition is met, the status bit for the system ADC alarm, SYS_ADC_DATA_x (0x01), is set in the status register block and, if desired, this can trigger an interrupt on INTB by setting SYS_ADC_DATA_x_EN (0x06) to 1. The upper and lower alarm thresholds for the system ADC are user programmable and are stored in registers SYS_HI_THRESH[15:0] (0x05C, 0x5D) and SYS_LO_THRESH[15:0] (0x5A, 0x5B). At power-on reset, the default values are 0xFFFF and 0x000, respectively. The system ADC can be configured to measure multiple inputs in succession. If the system ADC alarms are enabled in this condition, then extreme care must be taken to avoid false alarms. When using an alarm with the system ADC, it is recommended that only one input be selected and the alarm is set specifically for that input. More details can be found in the register map descriptions.

Temperature ADC Alarms

The alarm functions for the temperature ADC are the same as for the system ADC. The only difference is that the threshold comparison is done using signed data. This is because the temperature reading can go below 0°C.

The temperature ADC has independent upper and lower alarms, where x = HI (upper alarm) or LO (lower alarm) that can be configured to trip on 1 to 4 consecutive alarm crossings,TEMP_x_TRIP_CNT[1:0] (0x61, 0x62) and TEMP_x_TRIP (0x61, 0x62) set to 0, or 1 to 4 accumulated alarm crossings, TEMP_x_TRIP_CNT[1:0] and TEMP_x_TRIP set to 1. The current trip count is stored in a read-only register, TEMP_x_DET_CNTR[2:0] (0x61, 0x62), which can be reset by the user at any time by setting TEMP_RST_x_CNTR (0x61,0x62) to 1. When a given alarm condition is met, the status bit for the temperature ADC alarm, TEMP_DATA_x (0x01), is set in the status register block and, if desired, this can trigger an interrupt on INTB by setting TEMP_DATA_x_EN (0x06) to 1. The upper and lower alarm thresholds for the temperature ADC are user programmable and are stored in registers TEMP_HI_THRESH[15:0] (0x65, 0x66) and TEMP_LO_THRESH[15:0] (0x63, 0x64). For the alarm functions to work correctly, the thresholds must be entered in a 2's complement signed data format. At power-on reset, the default values are 0x7FFF and 0x8000, respectively. More details can be found in the register map descriptions.

GPIO

The device has four general-purpose input/output (GPIO) pins. Each GPIO pin can be independently configured using GPIOx_MODE[3:0] (0x90, 0x91, 0x92, 0x93) to be either an analog input, digital input, or digital output. When configured as an analog input, GPIOx_MODE[3:0] set to 0, the voltage on the GPIOx pin can be measured using the system ADC (see Figure 23 for more details). When configured as a digital input by setting GPIOx_MODE[3:0] to 1, the falling and rising edge transition on the GPIOx pin are reported by the GPIOx_FDET and GPIOx_RDET (0x04) status bits. If needed, an interrupt for any of these edge-detect bits can be programmed by setting the corresponding GPIOx_FDET_EN or GPIOx_FDET_EN (0x09) bit to 1. In digital input mode, a floating GPIOx pin can be avoided by setting GPIOx_IPU (0x90, 0x91, 0x92, 0x93) to 1. This connects a 1MΩ pullup resistor between V_{DD} and the GPIOx. When configured as a digital output, the GPIOx pin can be configured by setting GPIOx_OCFG[1:0] (0x90, 0x91, 0x92, 0x93) to be either open drain, active drive, or weak pullup. In this mode, the output is set low by setting GPIOx_MODE[3:0] to 0xC or set high by setting GPIOx_MODE[3:0] to 0xD. When a GPIOx pin is configured as a digital input or output, its logic level can be read back through GPIOx_LL (0x94).

The GPIO pins also have modes for externally triggering the internal sensor, system, and temperature ADC conversions, powering down the chip and disconnecting the internal circuits on the WE, RE, and CE pins. They can also be used to provide external clocks for synchronization and control. See the descriptions for GPIOx_MODE[3:0] for more details.

Status Bits and Interrupt

The MAX30131/MAX30132/MAX30134 have multiple status bits that report on the status of internal operations and conditions. All status bits are read only and self clear when the register containing the status bit is read. All status bits, except PWR_RDY (0x00), have a corresponding interrupt enable bit. When the paired enable bit is set to 1, the INTB pin transitions to its active state when the status bit gets set. The active state and output drive capability of the interrupt pin is configured by INTB_OCFB[1:0] (0x95). It can be set to either open drain (default), active drive-high, active drive-low, or open drain with a weak pullup. In the default open-drain mode, an external resistor must be connected between the INTB pin and the supply interface. The active state in this mode is low. The PWR_RDY status bit always issues an interrupt when set and cannot be masked. It is always set at power-on reset and the user must clear this status bit and the interrupt by reading status register 0x00.

SPI Timing

Detailed SPI Timing

The detailed SPI timing is illustrated in Figure 24. The timings indicated are all specified in the *Electrical Characteristics* table.

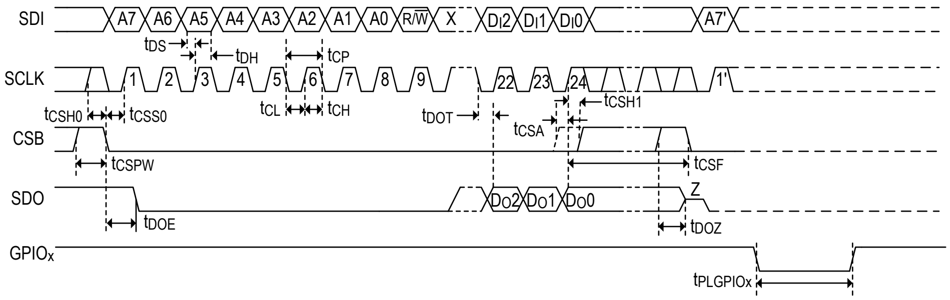


Figure 24. Detailed SPI Timing Diagram

Single Register SPI Read/Write Transaction

The MAX30131/MAX30132/MAX30134 are SPI/QSPI/Microwire/DSP compatible. The operation of the SPI interface is in

Figure 25 and Figure 26.

Data is clocked into the MAX30131/MAX30132/MAX30134 on the SCLK rising edge while clocked out on SCLK falling edge.

For single-byte register access, SPI read and write transactions are done in a 3-byte, 24 clock-cycle SPI instruction framed by a CSB low interval. The content of the SPI transaction consists of the register address byte, A[7:0], followed by one command byte, which defines the transaction as write or read (W = 0, R = 1), followed by a single data byte either written to or read from the register designated by the address byte. Write mode transactions are executed on the 24th SCLK rising edge using the address, command, and data bytes. For single register access, CSB is then deasserted to conclude the transaction. A rising CSB edge preceding the 24th rising edge of SCLK by t_{CSH1} (Figure 24) results in the transaction being aborted.

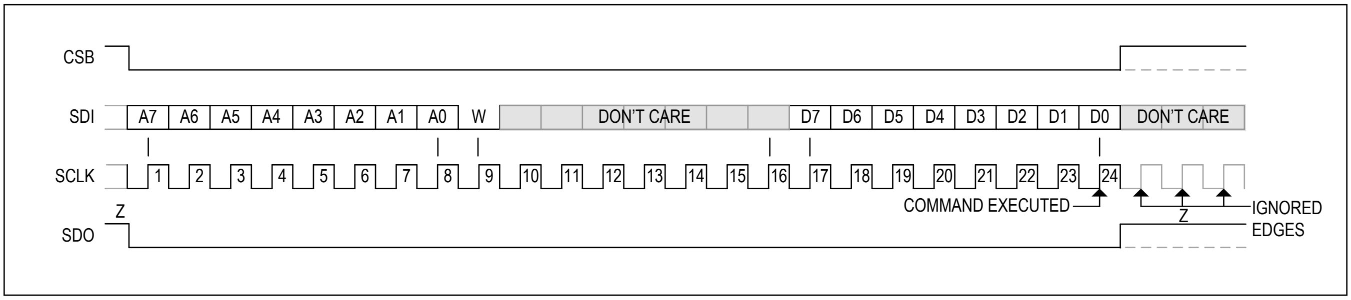


Figure 25. SPI Write Transaction

Single-byte register read transactions fetch the requested data before the 16th SCLK rising edge and present the MSB of the requested data on the following SCLK falling edge, allowing the microcontroller to latch the data MSB on the 17th SCLK rising edge. To conclude the transaction, CSB is deasserted after the 24th SCLK rising edge.

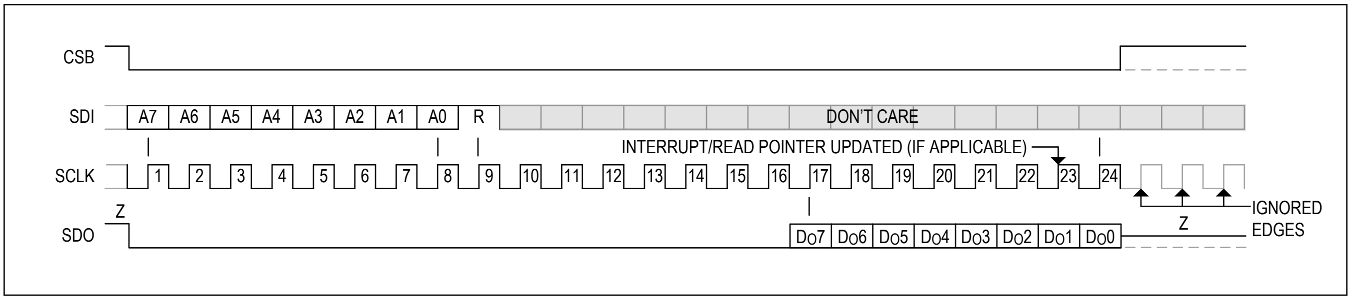


Figure 26. SPI Read Transaction

Burst Mode SPI Read/Write Transaction

For register burst write access, additional groups of 8 SCLK cycles are applied after the initial 24 cycles. The register address is automatically incremented after the 24th SCLK cycle and after each subsequent group of 8 SCLK cycles. The data bytes received after the first 24 SCLK cycles are sequentially written to their automatically calculated address. Therefore, if a transaction is (24 + (8 x N)) SCLK cycles long, N + 1 adjacent registers are written starting at the address specified by the first byte.

For register burst read access, additional groups of 8 SCLK cycles are applied after the initial 24 cycles. The register address is automatically incremented after the 24th SCLK cycle and after each subsequent group of 8 SCLK cycles. The content of those automatically calculated addresses is retrieved each time a new group of 8 SCLK cycles are applied. Therefore, if a transaction is (24 + (8 x N)) SCLK cycles long, N + 1 adjacent registers are read starting at the address specified by the first byte.

FIFO Data SPI Read Transaction

The SPI read transactions for FIFO_DATA register access has a minimum of 5 bytes. The first byte is the address byte for FIFO_DATA; the second byte is the command byte; and the next three bytes are the data bytes, as the FIFO data is 22-bit wide. Burst transactions allow to access adjacent FIFO locations, as the FIFO Read Pointer is automatically incremented after each group of three data bytes. The register address, however, is not incremented with FIFO_DATA burst transactions.

FIFO Description

The MAX30131/MAX30132/MAX30134 have a 256-word FIFO which holds 21-bit wide data. The ADC conversion data from all the Sensor ADCs, EIS ADC, Temperature Sensor, and the System ADC are saved in the FIFO along with a unique tag, which identifies the type of data. There is also a bit in the FIFO data, which indicates if the data corresponds to manual or autonomous mode ADC conversion. The processor does a burst read of three bytes from the FIFO to get the 21-bit data using the serial interface.

There are seven registers controlling how the FIFO is configured and read out. These registers are illustrated in Table 6.

Table 6. FIFO REGISTERS

ADDRESS	REGISTER NAME	B7	B6	B5	B4	B3	B2	B1	B0
0x0A	FIFO Write Pointer	FIFO_WR_PTR[7:0]							
0x0B	FIFO Read Pointer	FIFO_RD_PTR[7:0]							
0x0C	FIFO Counter 1	FIFO_DATA_COUNT[8]	OVF_COUNTER[6:0]						
0x0D	FIFO Counter 2	FIFO_DATA_COUNT[7:0]							
0x0E	FIFO Data	FIFO_DATA[7:0]							
0x0F	FIFO Configuration 1	FIFO_A_FULL[7:0]							
0x10	FIFO Configuration 2	-	-	-	FLUSH_FIFO	FIFO_STAT_CLR	A_FULL_TYPE	FIFO_RO	-

Write Pointer (0x0A)

FIFO_WR_PTR[7:0] points to the FIFO location where the next item is to be written. This pointer advances for each item pushed on to the FIFO by the internal conversion process. The write pointer is an 8-bit counter and wraps around to count 0x00 on the next item after count 0xFF.

Read Pointer (0x0B)

FIFO_RD_PTR[7:0] points to the location where the next item from the FIFO is read using the serial interface. This advances each time an item is read from the FIFO. The read pointer can be both read and written to. This allows an item to be reread from the FIFO if it has not already been overwritten. The read pointer is updated from an 8-bit counter and wraps around to count 0x00 from count 0xFF. Writing to the read pointer can affect the state of status register bits related to the FIFO and lead to unexpected behavior. Writing to the FIFO read pointer should be used for debug purposes only.

FIFO Overflow Counter (0x0C)

OVF_COUNTER[6:0] logs the number of items lost if the FIFO is not read in a timely fashion. This counter holds/ saturates at count value 0x7F. When a complete item is popped from the FIFO (when the read pointer advances), the OVF_COUNTER is reset to zero. This counter is essentially a debug tool. It should be read immediately before reading the FIFO in order to check if an overflow condition has occurred.

FIFO Data Counter (0x0C and 0x0D)

FIFO_DATA_COUNT[8:0] is a read-only register which holds the number of items available in the FIFO for the processor to read. This increments when a new item is pushed to the FIFO, and decrements when the processor reads an item from the FIFO.

FIFO Data (0x0E)

FIFO_DATA[7:0] is a read-only register used to retrieve data from the FIFO. It is important to burst read the item from the FIFO. Each item is three bytes. So burst reading three bytes at FIFO_DATA register using the serial interface advances the FIFO_RD_PTR. The format and data type of the data stored in the FIFO is determined by the tag associated with the data.

Number of Samples in the FIFO

Number of samples available in the FIFO after the last read can be obtained by reading the OVF_COUNTER[6:0] and FIFO_DATA_COUNT[8:0] registers using the following pseudo-code:

```
read the FIFO COUNTER 1 register
read the FIFO COUNTER 2 register
if OVF_COUNTER == 0 //no overflow occurred
    NUM_AVAILABLE_SAMPLES = FIFO_DATA_COUNT
else
    NUM_AVAILABLE_SAMPLES = 256 // overflow occurred and data has been lost
```

FIFO_WR_PTR[7:0] and FIFO_RD_PTR[7:0] are available for debug. They can also be used to calculate the number of available samples using the following pseudo-code:

```
If OVF_COUNTER is zero,
    NUM_AVAILABLE_ITEMS = FIFO_WR_PTR – FIFO_RD_PTR
    (Note: pointer wrap around should be taken into account)
else
    NUM_AVAILABLE_ITEMS = 256
```

FIFO Data Format

Table 7 shows the data format in the FIFO, and Table 8 shows the order in which the three bytes of the FIFO data are read through the serial interface. Table 9 lists the tags for each data type.

When reading a FIFO data word, AUTO, bit 20, indicates whether the measurement was made in AUTO mode with AUTO set to 1, or Manual mode with AUTO set to 0. The data tag can be 4 or 8 bits long, depending on the tag value in bits [19:16]. For values of bits [19:16] less then or equal to 0xC, bits [15:0] will contain counts data. For values of bits [19:16] greater than 0xC, bits [19:12] will make up the tag value and bits [11:0] will contain counts data.

Table 7. FIFO DATA FORMAT

FIFO DATA FORMAT (FIFO_DATA[23:0])																							
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
-	-	-	F20	F19	F18	F17	F16	F15	F14	F13	F12	F11	F10	F9	F8	F7	F6	F5	F4	F3	F2	F1	F0
Byte 1								Byte 2								Byte 3							

Table 8. FIFO DATA BYTE ORDER

SAMPLE NUMBER	BYTE NUMBER	FIFO DATA READ FORMAT							
		BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Sample N	1	-	-	-	F20	F19	F18	F17	F16
	2	F15	F14	F13	F12	F11	F10	F9	F8
	3	F7	F6	F5	F4	F3	F2	F1	F0
Sample N + 1	1	-	-	F21	F20	F19	F18	F17	F16
	2	F15	F14	F13	F12	F11	F10	F9	F8
	3	F7	F6	F5	F4	F3	F2	F1	F0
Sample N + 2	1	-	-	-	F20	F19	F18	F17	F16
	2	F15	F14	F13	F12	F11	F10	F9	F8
	3	F7	F6	F5	F4	F3	F2	F1	F0
…									
Sample N + 255	1	-	-	-	F20	F19	F18	F17	F16
	2	F15	F14	F13	F12	F11	F10	F9	F8
	3	F7	F6	F5	F4	F3	F2	F1	F0

Table 9. FIFO DATA TAGS

TAG	DATA TYPE	FIFO_DATA[20:0]
0x0	Sensor 1 DC Current	AUTO, 4’h0, S1_ADC_DATA[15:0]
0x1	Sensor 2 DC Current	AUTO, 4’h1, S2_ADC_DATA[15:0]
0x2	Sensor 3 DC Current	AUTO, 4’h2, S3_ADC_DATA[15:0]
0x3	Sensor 4 DC Current	AUTO, 4’h3, S4_ADC_DATA[15:0]
0x4	Sensor 1 EIS Real, CV, SWV	AUTO, 4’h4, S1_EISR_ADC_DATA[15:0]
0x5	Sensor 2 EIS Real, CV, SWV	AUTO, 4’h5, S2_EISR_ADC_DATA[15:0]
0x6	Sensor 3 EIS Real, CV, SWV	AUTO, 4’h6, S3_EISR_ADC_DATA[15:0]
0x7	Sensor 4 EIS Real, CV, SWV	AUTO, 4’h7, S4_EISR_ADC_DATA[15:0]
0x8	Sensor 1 EIS Imaginary	AUTO, 4’h8, S1_EISI_ADC_DATA[15:0]
0x9	Sensor 2 EIS Imaginary	AUTO, 4’h9, S2_EISI_ADC_DATA[15:0]
0xA	Sensor 3 EIS Imaginary	AUTO, 4’hA, S3_EISI_ADC_DATA[15:0]
0xB	Sensor 4 EIS Imaginary	AUTO, 4’hB, S4_EISI_ADC_DATA[15:0]
0xC	Temperature Sensor	AUTO, 4’hC, TEMP_ADC_DATA[15:0]
0xD0	Sensor 1 Working Amplifier Output	AUTO, 8’hD0, S1_WO_ADC_DATA[11:0]
0xD1	Sensor 1 Working Electrode pin	AUTO, 8’hD1, S1_WE_ADC_DATA[11:0]
0xD2	Sensor 1 Reference Electrode pin	AUTO, 8’hD2, S1_RE_ADC_DATA[11:0]
0xD3	Sensor 1 Counter Electrode pin	AUTO, 8’hD3, S1_CE_ADC_DATA[11:0]
0xD4	Sensor 2 Working Amplifier Output	AUTO, 8’hD4, S2_WO_ADC_DATA[11:0]

Table 9. FIFO DATA TAGS (continued)

0xD5	Sensor 2 Working Electrode pin	AUTO, 8’hD5, S2_WE_ADC_DATA[11:0]
0xD6	Sensor 2 Reference Electrode pin	AUTO, 8’hD6, S2_RE_ADC_DATA[11:0]
0xD7	Sensor 2 Counter Electrode pin	AUTO, 8’hD7, S2_CE_ADC_DATA[11:0]
0xD8	Sensor 3 Working Amplifier Output	AUTO, 8’hD8, S3_WO_ADC_DATA[11:0]
0xD9	Sensor 3 Working Electrode pin	AUTO, 8’hD9, S3_WE_ADC_DATA[11:0]
0xDA	Sensor 3 Reference Electrode pin	AUTO, 8’hDA, S3_RE_ADC_DATA[11:0]
0xDB	Sensor 3 Counter Electrode pin	AUTO, 8’hDB, S3_CE_ADC_DATA[11:0]
0xDC	Sensor 4 Working Amplifier Output	AUTO, 8’hDC, S4_WO_ADC_DATA[11:0]
0xDD	Sensor 4 Working Electrode pin	AUTO, 8’hDD, S4_WE_ADC_DATA[11:0]
0xDE	Sensor 4 Reference Electrode pin	AUTO, 8’hDE, S4_RE_ADC_DATA[11:0]
0xDF	Sensor 4 Counter Electrode pin	AUTO, 8’hDF, S4_CE_ADC_DATA[11:0]
0xE0	V_{DD} supply voltage	AUTO, 8’hE0, VDD_ADC_DATA[11:0]
0xE1	Ground reference	AUTO, 8’hE1, GND_ADC_DATA[11:0]
0xE2–0xEF	Reserved	
0xF0	External analog input 0	AUTO, 8’hF0, AIN0_ADC_DATA[11:0]
0xF1	External analog input 1	AUTO, 8’hF1, AIN1_ADC_DATA[11:0]
0xF2	External analog input 2	AUTO, 8’hF2, AIN2_ADC_DATA[11:0]
0xF3	External analog input 3	AUTO, 8’hF3, AIN3_ADC_DATA[11:0]
0xF4	Reserved	
0xF5	Sensor 1 EIS DC Current	1'b0, 8’hF5, EIS1_DC_DATA[11:0]
0xF6	Sensor 2 EIS DC Current	1'b0, 8’hF6, EIS1_DC_DATA[11:0]
0xF7	Sensor 3 EIS DC Current	1'b0, 8’hF7, EIS1_DC_DATA[11:0]
0xF8	Sensor 4 EIS DC Current	1'b0, 8’hF8, EIS1_DC_DATA[11:0]
0xF9–0xFD	Reserved	
0xFE	Empty FIFO Read	10’h0FE, Dont_care[11:0]
0xFF	Reserved	

Notes:

- For 16-bit ADC data, the tags are 4 bits. For 12-bit ADC data, the tags are 8 bits.
- For SWV or CV modes, tag used for the EIS Real Data is used for the selected Sensor.
- AUTO = 1 for Auto mode conversions; AUTO = 0 for manual mode conversions.
- ADC data is signed for some data types and unsigned for the others.
- An attempt to read an empty FIFO is identified by the empty FIFO tag 0xFE.

FIFO_A_FULL (0x0F) FIFO_A_FULL[7:0] sets the watermark for the FIFO and determines when A_FULL (0x00) gets asserted. The A_FULL bit is set when the FIFO contains 256 minus FIFO_A_FULL[7:0] items. If the A_FULL_EN (0x05) interupt enable bit is set an interrupt is asserted on the INTB pin. This condition should prompt the applications processor to read samples out of the FIFO before it fills. The A_FULL bit and the interrupt on the INTB pin are cleared when the status register is read.

The microcontroller can read both the FIFO_WR_PTR and FIFO_RD_PTR to calculate the number of items available in the FIFO, or just read the OVF_COUNTER and FIFO_DATA_COUNT registers, and read as many items as needed to empty the FIFO. Alternatively, if the microcontroller always responds much faster than the selected sample rate, it can read 256 minus FIFO_A_FULL[7:0] items when it detects an A_FULL interrupt to empty the FIFO.

FIFO_RO (0x10)

The FIFO_RO bit defines the rollover behavior when the FIFO is full. If FIFO_RO is set low, then a new data sample is not written to the FIFO and is lost when the FIFO is full. If FIFO_RO is set high, then the FIFO rolls over to the first location and a new data sample is written to the FIFO, overwriting the old data sample.

A_FULL_TYPE (0x10)

The A_FULL_TYPE bit defines the behavior of the A_FULL interrupt. If the A_FULL_TYPE bit is set low, the A_FULL interrupt gets asserted when the A_FULL condition is detected and cleared by status register read, but reasserts for every sample if the A_FULL condition persists. If the A_FULL_TYPE bit is set high, the A_FULL interrupt gets asserted only when a new A_FULL condition is detected. The interrupt gets cleared on STATUS 1 (0x00) read, and does not reassert for every sample until a new A_FULL condition is detected.

FIFO_STAT_CLR (0x10)

The FIFO_STAT_CLR bit defines how the A_FULL and FIFO_DATA_RDY status bits are cleared. If FIFO_STAT_CLR is set low, A_FULL and FIFO_DATA_RDY interrupts are not cleared by FIFO_DATA register read, but are cleared by status register read. If FIFO_STAT_CLR is set high, A_FULL and FIFO_DATA_RDY interrupts are cleared by a FIFO_DATA register read or a status register read.

FLUSH_FIFO (0x10)

The FIFO Flush bit is used for flushing the FIFO. If FLUSH_FIFO is set high then the FIFO is emptied and the FIFO_WR_PTR[7:0], FIFO_RD_PTR[7:0], FIFO_DATA_COUNT[8:0] and OVF_COUNTER[6:0] are reset to zero. FLUSH_FIFO is a self-clearing bit.

Register Map

Overview of All Registers

ADDRESS	NAME	MSB							LSB
STATUS									
0x00	STATUS 1[7:0]	A_FULL	FIFO_DATA_RDY	–	AC_DATA_RDY	EIS_CAL_DONE	INVALID_CFG	VDD_OOR	PWR_RDY
0x01	STATUS 2[7:0]	SYS_ADC_DATA_RDY	SYS_ADC_DATA_LO	SYS_ADC_DATA_HI	–	TEMP_DATA_RDY	TEMP_DATA_LO	TEMP_DATA_HI	–
0x02	STATUS 3[7:0]	S2_ADC_DATA_RDY	S2_ADC_DATA_LO	S2_ADC_DATA_HI	S2_DET	S1_ADC_DATA_RDY	S1_ADC_DATA_LO	S1_ADC_DATA_HI	S1_DET
0x03	STATUS 4[7:0]	S4_ADC_DATA_RDY	S4_ADC_DATA_LO	S4_ADC_DATA_HI	S4_DET	S3_ADC_DATA_RDY	S3_ADC_DATA_LO	S3_ADC_DATA_HI	S3_DET
0x04	STATUS 5[7:0]	GPIO4_RDET	GPIO3_RDET	GPIO2_RDET	GPIO1_RDET	GPIO4_FDET	GPIO3_FDET	GPIO2_FDET	GPIO1_FDET
INTERRUPT ENABLES									
0x05	INTERRUPT ENABLE 1[7:0]	A_FULL_EN	FIFO_DATA_RDY_EN	–	AC_DATA_RDY_EN	EIS_CAL_DONE_EN	INVALID_CFG_EN	VDD_OOR_EN	–
0x06	INTERRUPT ENABLE 2[7:0]	SYS_ADC_DATA_RDY_EN	SYS_ADC_DATA_LO_EN	SYS_ADC_DATA_HI_EN	–	TEMP_DATA_RDY_EN	TEMP_DATA_LO_EN	TEMP_DATA_HI_EN	–
0x07	INTERRUPT ENABLE 3[7:0]	S2_ADC_DATA_RDY_EN	S2_ADC_DATA_LO_EN	S2_ADC_DATA_HI_EN	S2_DET_EN	S1_ADC_DATA_RDY_EN	S1_ADC_DATA_LO_EN	S1_ADC_DATA_HI_EN	S1_DET_EN
0x08	INTERRUPT ENABLE 4[7:0]	S4_ADC_DATA_RDY_EN	S4_ADC_DATA_LO_EN	S4_ADC_DATA_HI_EN	S4_DET_EN	S3_ADC_DATA_RDY_EN	S3_ADC_DATA_LO_EN	S3_ADC_DATA_HI_EN	S3_DET_EN
0x09	INTERRUPT ENABLE 5[7:0]	GPIO4_RDET_EN	GPIO3_RDET_EN	GPIO2_RDET_EN	GPIO1_RDET_EN	GPIO4_FDET_EN	GPIO3_FDET_EN	GPIO2_FDET_EN	GPIO1_FDET_EN
FIFO									
0x0A	FIFO WRITE POINTER[7:0]	FIFO_WR_PTR[7:0]							
0x0B	FIFO READ POINTER[7:0]	FIFO_RD_PTR[7:0]							
0x0C	FIFO COUNTER 1[7:0]	FIFO_DATA_COUNT[8]	OVF_COUNTER[6:0]						
0x0D	FIFO COUNTER 2[7:0]	FIFO_DATA_COUNT[7:0]							
0x0E	FIFO DATA[7:0]	FIFO_DATA[7:0]							
0x0F	FIFO CONFIGURATION 1[7:0]	FIFO_A_FULL[7:0]							

ADDRESS	**NAME**	**MSB**							**LSB**
0x10	FIFO CONFIGURATION 2[7:0]	–	–	–	FLUSH_FIFO	FIFO_STAT_CLR	A_FULL_TYPE	FIFO_RO	–
SYSTEM CONTROL									
0x14	SYSTEM CONTROL[7:0]	BYPASS_LDO	CLK_SEL	SENSOR_CAL	–	–	–	SHDN	RESET
0x1F	SENSOR CONFIGURATION[7:0]	–	–	–	–	–	SHARED_CA	DETECTOR_BIAS[1:0]	
SENSOR 1									
0x20	SENSOR 1 CONFIGURATION 1[7:0]	S1_WE_AMP_EN	S1_CE_AMP_EN	S1_WE_DAC_MX[1:0]		S1_CE_DAC_MX[1:0]		S1_CP_EN	S1_CHOP_EN
0x21	SENSOR 1 CONFIGURATION 2[7:0]	S1_SWB	S1_SWA	S1_SC	S1_SRB	S1_SRA	S1_ILIM_EN	S1_RS	S1_SWO
0x22	SENSOR 1 CONFIGURATION 3[7:0]	–	–	–	–	S1_IOS_MODE	S1_DETECTOR_EN	S1_DETECTOR_THRESHOLD[1:0]	
0x23	SENSOR 1 CONFIGURATION 4[7:0]	S1_FSR[2:0]			–	–	S1_OFFSET_SEL[2:0]		
0x24	SENSOR 1 CONFIGURATION 5[7:0]	–	–	–	S1_CONV_TIME[3:0]				S1_SELECT
0x25	SENSOR 1 ALARM LOW SETUP[7:0]	S1_LO_MODE	S1_LO_TRIP	S1_LO_TRIP_CNT[1:0]		S1_LO_DET_CNTR[2:0]			S1_RST_LO_CNTR
0x26	SENSOR 1 ALARM HIGH SETUP[7:0]	S1_HI_MODE	S1_HI_TRIP	S1_HI_TRIP_CNT[1:0]		S1_HI_DET_CNTR[2:0]			S1_RST_HI_CNTR
0x27	SENSOR 1 ALARM LOW MSB[7:0]	S1_LO_THRESH[15:8]							
0x28	SENSOR 1 ALARM LOW LSB[7:0]	S1_LO_THRESH[7:0]							
0x29	SENSOR 1 ALARM HIGH MSB[7:0]	S1_HI_THRESH[15:8]							
0x2A	SENSOR 1 ALARM HIGH LSB[7:0]	S1_HI_THRESH[7:0]							
0x2B	SENSOR 1 OFFSET CURRENT MSB[7:0]	S1_IOFFSET[15:8]							
0x2C	SENSOR 1 OFFSET CURRENT LSB[7:0]	S1_IOFFSET[7:0]							
SENSOR 2									
0x2D	SENSOR 2 CONFIGURATION 1[7:0]	S2_WE_AMP_EN	S2_CE_AMP_EN	S2_WE_DAC_MX[1:0]		S2_CE_DAC_MX[1:0]		S2_CP_EN	S2_CHOP_EN
0x2E	SENSOR 2 CONFIGURATION 2[7:0]	S2_SWB	S2_SWA	S2_SC	S2_SRB	S2_SRA	S2_ILIM_EN	S2_RS	S2_SWO

ADDRESS	NAME	MSB							LSB
0x2F	SENSOR 2 CONFIGURATION 3[7:0]	–	–	–	–	S2_IOS_MODE	S2_DETECTOR_EN	S2_DETECTOR_THRESHOLD[1:0]	
0x30	SENSOR 2 CONFIGURATION 4[7:0]	S2_FSR[2:0]			–	–	S2_OFFSET_SEL[2:0]		
0x31	SENSOR 2 CONFIGURATION 5[7:0]	–	–	–	S2_CONV_TIME[3:0]				S2_SELECT
0x32	SENSOR 2 ALARM LOW SETUP[7:0]	S2_LO_MODE	S2_LO_TRIP	S2_LO_TRIP_CNT[1:0]		S2_LO_DET_CNTR[2:0]			S2_RST_LO_CNTR
0x33	SENSOR 2 ALARM HIGH SETUP[7:0]	S2_HI_MODE	S2_HI_TRIP	S2_HI_TRIP_CNT[1:0]		S2_HI_DET_CNTR[2:0]			S2_RST_HI_CNTR
0x34	SENSOR 2 ALARM LOW MSB[7:0]	S2_LO_THRESH[15:8]							
0x35	SENSOR 2 ALARM LOW LSB[7:0]	S2_LO_THRESH[7:0]							
0x36	SENSOR 2 ALARM HIGH MSB[7:0]	S2_HI_THRESH[15:8]							
0x37	SENSOR 2 ALARM HIGH LSB[7:0]	S2_HI_THRESH[7:0]							
0x38	SENSOR 2 OFFSET CURRENT MSB[7:0]	S2_IOFFSET[15:8]							
0x39	SENSOR 2 OFFSET CURRENT LSB[7:0]	S2_IOFFSET[7:0]							
SENSOR 3									
0x3A	SENSOR 3 CONFIGURATION 1[7:0]	S3_WE_AMP_EN	S3_CE_AMP_EN	S3_WE_DAC_MX[1:0]		S3_CE_DAC_MX[1:0]		S3_CP_EN	S3_CHOP_EN
0x3B	SENSOR 3 CONFIGURATION 2[7:0]	S3_SWB	S3_SWA	S3_SC	S3_SRB	S3_SRA	S3_ILIM_EN	S3_RS	S3_SWO
0x3C	SENSOR 3 CONFIGURATION 3[7:0]	–	–	–	–	S3_IOS_MODE	S3_DETECTOR_EN	S3_DETECTOR_THRESHOLD[1:0]	
0x3D	SENSOR 3 CONFIGURATION 4[7:0]	S3_FSR[2:0]			–	–	S3_OFFSET_SEL[2:0]		
0x3E	SENSOR 3 CONFIGURATION 5[7:0]	–	–	–	S3_CONV_TIME[3:0]				S3_SELECT
0x3F	SENSOR 3 ALARM LOW SETUP[7:0]	S3_LO_MODE	S3_LO_TRIP	S3_LO_TRIP_CNT[1:0]		S3_LO_DET_CNTR[2:0]			S3_RST_LO_CNTR
0x40	SENSOR 3 ALARM HIGH SETUP[7:0]	S3_HI_MODE	S3_HI_TRIP	S3_HI_TRIP_CNT[1:0]		S3_HI_DET_CNTR[2:0]			S3_RST_HI_CNTR
0x41	SENSOR 3 ALARM LOW MSB[7:0]	S3_LO_THRESH[15:8]							

ADDRESS	NAME	MSB							LSB
0x42	SENSOR 3 ALARM LOW LSB[7:0]	S3_LO_THRESH[7:0]							
0x43	SENSOR 3 ALARM HIGH MSB[7:0]	S3_HI_THRESH[15:8]							
0x44	SENSOR 3 ALARM HIGH LSB[7:0]	S3_HI_THRESH[7:0]							
0x45	SENSOR 3 OFFSET CURRENT MSB[7:0]	S3_IOFFSET[15:8]							
0x46	SENSOR 3 OFFSET CURRENT LSB[7:0]	S3_IOFFSET[7:0]							
SENSOR 4									
0x47	SENSOR 4 CONFIGURATION 1[7:0]	S4_WE_AMP_EN	S4_CE_AMP_EN	S4_WE_DAC_MX[1:0]		S4_CE_DAC_MX[1:0]		S4_CP_EN	S4_CHOP_EN
0x48	SENSOR 4 CONFIGURATION 2[7:0]	S4_SWB	S4_SWA	S4_SC	S4_SRB	S4_SRA	S4_ILIM_EN	S4_RS	S4_SWO
0x49	SENSOR 4 CONFIGURATION 3[7:0]	–	–	–	–	S4_IOS_MODE	S4_DETECTOR_EN	S4_DETECTOR_THRESHOLD[1:0]	
0x4A	SENSOR 4 CONFIGURATION 4[7:0]	S4_FSR[2:0]			–	–	S4_OFFSET_SEL[2:0]		
0x4B	SENSOR 4 CONFIGURATION 5[7:0]	–	–	–	S4_CONV_TIME[3:0]				S4_SELECT
0x4C	SENSOR 4 ALARM LOW SETUP[7:0]	S4_LO_MODE	S4_LO_TRIP	S4_LO_TRIP_CNT[1:0]		S4_LO_DET_CNTR[2:0]			S4_RST_LO_CNTR
0x4D	SENSOR 4 ALARM HIGH SETUP[7:0]	S4_HI_MODE	S4_HI_TRIP	S4_HI_TRIP_CNT[1:0]		S4_HI_DET_CNTR[2:0]			S4_RST_HI_CNTR
0x4E	SENSOR 4 ALARM LOW MSB[7:0]	S4_LO_THRESH[15:8]							
0x4F	SENSOR 4 ALARM LOW LSB[7:0]	S4_LO_THRESH[7:0]							
0x50	SENSOR 4 ALARM HIGH MSB[7:0]	S4_HI_THRESH[15:8]							
0x51	SENSOR 4 ALARM HIGH LSB[7:0]	S4_HI_THRESH[7:0]							
0x52	SENSOR 4 OFFSET CURRENT MSB[7:0]	S4_IOFFSET[15:8]							
0x53	SENSOR 4 OFFSET CURRENT LSB[7:0]	S4_IOFFSET[7:0]							
SYSTEM ADC									
0x54	SYSTEM ADC SETUP[7:0]	SYS_AIN_GAIN[1:0]		SYS_PWR_GAIN[1:0]		SYS_SENSV_GAIN[1:0]		OPA_BYPASS_EN	–
0x55	SYSTEM ADC IN SEL1[7:0]	AIN4_SYS_SEL	AIN3_SYS_SEL	AIN2_SYS_SEL	AIN1_SYS_SEL	VDD_SYS_SEL	GND_SYS_SEL	–	SYS_SELECT

ADDRESS	NAME	MSB							LSB
0x56	SYSTEM ADC IN SEL2[7:0]	S2_WO_SYS_SEL	S2_WE_SYS_SEL	S2_RE_SYS_SEL	S2_CE_SYS_SEL	S1_WO_SYS_SEL	S1_WE_SYS_SEL	S1_RE_SYS_SEL	S1_CE_SYS_SEL
0x57	SYSTEM ADC IN SEL3[7:0]	S4_WO_SYS_SEL	S4_WE_SYS_SEL	S4_RE_SYS_SEL	S4_CE_SYS_SEL	S3_WO_SYS_SEL	S3_WE_SYS_SEL	S3_RE_SYS_SEL	S3_CE_SYS_SEL
0x58	SYSTEM ADC ALARM LOW SETUP[7:0]	–	SYS_LO_TRIP	SYS_LO_TRIP_CNT[1:0]		SYS_LO_DET_CNTR[2:0]			SYS_RST_LO_CNTR
0x59	SYSTEM ADC ALARM HIGH SETUP[7:0]	–	SYS_HI_TRIP	SYS_HI_TRIP_CNT[1:0]		SYS_HI_DET_CNTR[2:0]			SYS_RST_HI_CNTR
0x5A	SYSTEM ADC ALARM LOW MSB[7:0]	–	–	–	–	SYS_LO_THRESH[11:8]			
0x5B	SYSTEM ADC ALARM LOW LSB[7:0]	SYS_LO_THRESH[7:0]							
0x5C	SYSTEM ADC ALARM HIGH MSB[7:0]	–	–	–	–	SYS_HI_THRESH[11:8]			
0x5D	SYSTEM ADC ALARM HIGH LSB[7:0]	SYS_HI_THRESH[7:0]							
0x5E	SYSTEM OFFSET VOLTAGE MSB[7:0]	–	–	–	–	SYS_VOFFSET[11:8]			
0x5F	SYSTEM OFFSET VOLTAGE LSB[7:0]	SYS_VOFFSET[7:0]							
TEMPERATURE									
0x60	TEMPERATURE CONFIGURATION[7:0]	RESERVED[1:0]		–	–	–	–	–	TEMP_SELECT
0x61	TEMP ALARM LOW SETUP[7:0]	–	TEMP_LO_TRIP	TEMP_LO_TRIP_CNT[1:0]		TEMP_LO_DET_CNTR[2:0]			TEMP_RST_LO_CNTR
0x62	TEMP ALARM HIGH SETUP[7:0]	–	TEMP_HI_TRIP	TEMP_HI_TRIP_CNT[1:0]		TEMP_HI_DET_CNTR[2:0]			TEMP_RST_HI_CNTR
0x63	TEMP ALARM LOW MSB[7:0]	TEMP_LO_THRESH[15:8]							
0x64	TEMP ALARM LOW LSB[7:0]	TEMP_LO_THRESH[7:0]							
0x65	TEMP ALARM HIGH MSB[7:0]	TEMP_HI_THRESH[15:8]							
0x66	TEMP ALARM HIGH LSB[7:0]	TEMP_HI_THRESH[7:0]							
DAC AND REFERENCE									
0x68	REFERENCE CONTROL[7:0]	–	–	–	–	REF_MODE	REF_VAL[1:0]		REF_EN
0x69	DACA MSB CODE[7:0]	DACA_CODE[11:4]							
0x6A	DACA EN LSB CODE[7:0]	DACA_CODE[3:0]				–	–	–	DACA_EN
0x6B	DACB MSB CODE[7:0]	DACB_CODE[11:4]							
0x6C	DACB EN LSB CODE[7:0]	DACB_CODE[3:0]				–	–	–	DACB_EN

ADDRESS	NAME	MSB							LSB
0x6D	DACC MSB CODE[7:0]	DACC_CODE[11:4]							
0x6E	DACC EN LSB CODE[7:0]	DACC_CODE[3:0]				–	–	–	DACC_EN
0x6F	DACD MSB CODE[7:0]	DACD_CODE[11:4]							
0x70	DACD EN LSB CODE[7:0]	DACD_CODE[3:0]				–	–	–	DACD_EN
EIS									
0x75	FAST_FREQ_TRIM_ADJ[7:0]	FAST_TRIM_ADJ[7:0]							
0x76	SLOW_FREQ_TRIM_ADJ[7:0]	SLOW_TRIM_ADJ[7:0]							
0x77	EIS CAL RES VAR[7:0]	EIS_CAL_RES_VARIATION[7:0]							
0x78	EIS SETUP 1[7:0]	EIS_DAC_SEL[1:0]		EIS_NUM_SINEWAVES[2:0]			–	EIS_FREQ_TRIM_CAL	EIS_PH_ADV_CAL
0x79	EIS SETUP 2[7:0]	EIS_AMPLITUDE[3:0]				–	–	–	–
0x7A	EIS CLOCK SETUP[7:0]	–	–	–	EIS_CLK_DIV[4:0]				
0x7B	EIS AFE 1[7:0]	EIS_WE_AMP_EN	EIS_CE_AMP_EN	EIS_SC	EIS_SRB	EIS_RC[1:0]		EIS_DRV	–
0x7C	EIS AFE 2[7:0]	EIS_RS	EIS_OFFSET[2:0]			EIS_ILIM_EN	EIS_I_CAL_EN	EIS_CAL_RES[1:0]	
0x7D	EIS ADC FS RANGE[7:0]	–	–	–	–	–	–	EIS_ADC_FS_RANGE[1:0]	
0x7E	PHASE_ADVANCE[7:0]	EIS_PHASE_ADVANCE[7:0]							
0x7F	EIS SETUP 3[7:0]	EIS_SETTLE[3:0]				EIS_FINE_FREQ[3:0]			
CONVERT SETUP									
0x80	CONVERT SETUP 1[7:0]	SENS_CONV_TYPE	IOFFSET_CONV[1:0]		SYS_CONV_TYPE	SENS_PERIOD[3:0]			
0x81	CONVERT SETUP 2[7:0]	TEMP_PERIOD[3:0]				SYS_PERIOD[3:0]			
0x83	CONVERT START[7:0]	–	–	–	–	–	–	AUTO	CONVERT
GPIO AND INTB									
0x90	GPIO1 SETUP[7:0]	GPIO1_MODE[3:0]				GPIO1_IPU	GPIO1_ICFG	GPIO1_OCFG[1:0]	
0x91	GPIO2 SETUP[7:0]	GPIO2_MODE[3:0]				GPIO2_IPU	GPIO2_ICFG	GPIO2_OCFG[1:0]	
0x92	GPIO3 SETUP[7:0]	GPIO3_MODE[3:0]				GPIO3_IPU	GPIO3_ICFG	GPIO3_OCFG[1:0]	
0x93	GPIO4 SETUP[7:0]	GPIO4_MODE[3:0]				GPIO4_IPU	GPIO4_ICFG	GPIO4_OCFG[1:0]	
0x94	GPIO INPUT[7:0]	–	–	–	–	GPIO4_LL	GPIO3_LL	GPIO2_LL	GPIO1_LL
0x95	INTB SETUP[7:0]	–	–	–	–	–	EN_VDD_OOR	INTB_OCFG[1:0]	

ADDRESS	NAME	MSB							LSB
SWV AND CV									
0xA0	SWV SETUP 1[7:0]	EIS_DAC_INC[3:0]				–	EIS_INTEG	AC_MODE[1:0]	
0xA1	SWV SETUP 2[7:0]	EIS_DAC_STOP[11:4]							
0xA2	SWV SETUP 3[7:0]	–	–	–	–	EIS_DAC_STOP[3:0]			
IDENTIFIERS									
0xFE	REVISION ID[7:0]	–	–	–	–	–	–	–	–
0xFF	PART IDENTIFIER[7:0]	PART_ID[7:0]							

Register Details

STATUS 1 (0x00)

BIT	7	6	5	4	3	2	1	0
Field	A_FULL	FIFO_DATA_RDY	–	AC_DATA_RDY	EIS_CAL_DONE	INVALID_CFG	VDD_OOR	PWR_RDY
Reset	0b0	0b0	–	0b0	0b0	0b0	0b0	0b1
Access Type	Read Only	Read Only	–	Read Only	Read Only	Read Only	Read Only	Read Only

A_FULL

The FIFO is considered to be almost full when it has 256 minus FIFO_A_FULL[7:0] items. See the FIFO_A_FULL[7:0] description in FIFO Configuration 1 (register 0x0F).

A_FULL is a read-only bit. It is set to 1 when the FIFO is almost full. This bit is cleared when STATUS 1 (register 0x00) is read. It is also cleared when FIFO_DATA (0x0E) is read, if FIFO_STAT_CLR (0x10) = 1.

FIFO_DATA_RDY

FIFO_DATA_RDY is a read-only bit. It is set to 1 when new data is saved in the FIFO. It is cleared by reading STATUS 1 (register 0x00). It is also cleared by reading FIFO_DATA (0x0E) if FIFO_STAT_CLR = 1 (0x10).

AC_DATA_RDY

AC_DATA_RDY is a read-only bit. It is set to 1 when the AC conversion completes. It is automatically cleared when the STATUS 1 register (0x00) is read.

When AC_MODE[1:0] (0xA0) = 00, EIS conversion is completed when conversion ends for the number of sinewaves programmed in EIS_NUM_SINEWAVES (0x78), data is available in the FIFO, and the sinewave returns to its midpoint.

When AC_MODE is programmed to 01 or 10, AC conversion is completed when the DC DAC code has ramped up to the programmed value and returned back to the DC DAC code programmed for the DAC selected by EIS_DAC_SEL[1:0] (0x78) for SWV or CV mode conversions.

EIS_CAL_DONE

EIS_CAL_DONE is a read-only bit. It is set to 1 when the EIS frequency trim calibration or EIS phase-advance calibration completes. It is automatically cleared when STATUS 1 (register 0x00) is read. See EIS_FREQ_TRIM_CAL and EIS_PH_ADV_CAL (0x78) for details.

INVALID_CFG

INVALID_CFG is a read-only bit. It is set to 1 when the attempted configuration cannot be completed within the sample period. It is automatically cleared when STATUS 1 (register 0x00) is read. The configuration is invalid if the period programmed for AUTO (0x83) mode is not wide enough for all the selected conversions to complete.

VDD_OOR

VDD_OOR is a read-only bit. It is set to 1 when V_{DD} is out of range (V_{DD} < 1.6V and V_{DD} > 5V typ). It is automatically cleared when STATUS 1 (register 0x00) is read. The detection circuitry has a 10ms delay time and continues to trigger as long as V_{DD} is out of range. To enable VDD_OOR functionality, both EN_VDD_OOR (0x95) and REF_EN (0x68) must be set to 1 (enabled); otherwise, VDD_OOR is always set to 0.

PWR_RDY

PWR_RDY is a read-only bit, and it indicates that V_{DD} had gone below the UVLO Threshold (1.55V). This bit is not triggered by a soft reset. This bit is cleared when STATUS 1 (register 0x00) is read or by setting SHDN (0x14) to 1.

STATUS 2 (0x01)

BIT	7	6	5	4	3	2	1	0
Field	SYS_ADC_DATA_RDY	SYS_ADC_DATA_LO	SYS_ADC_DATA_HI	–	TEMP_DATA_RDY	TEMP_DATA_LO	TEMP_DATA_HI	–
Reset	0b0	0b0	0b0	–	0b0	0b0	0b0	–
Access Type	Read Only	Read Only	Read Only	–	Read Only	Read Only	Read Only	–

SYS_ADC_DATA_RDY

SYS_ADC_DATA_RDY is set to 1 when all conversions in the system ADC conversion sequence have been completed. This read-only bit is cleared when STATUS 2 (register 0x01) is read.

SYS_ADC_DATA_LO

SYS_ADC_DATA_LO is set to 1 when the system ADC data has gone below the system ADC Alarm Low Threshold. This read-only bit is cleared when STATUS 2 (register 0x01) is read.

SYS_ADC_DATA_HI

SYS_ADC_DATA_HI is set to 1 when the system ADC data has gone above the system ADC Alarm High Threshold. This read-only bit is cleared when STATUS 2 (register 0x01) is read.

TEMP_DATA_RDY

TEMP_DATA_RDY is set to 1 when the temperature sensor ADC conversion has been completed, and the data is available in the FIFO. This read-only bit is cleared when STATUS 2 (register 0x01) is read.

TEMP_DATA_LO

TEMP_DATA_LO is set to 1 when the temperature sensor ADC data has gone below the Temperature Alarm Low Threshold. This read-only bit is cleared when STATUS 2 (register 0x01) is read.

TEMP_DATA_HI

TEMP_DATA_HI is set to 1 when the temperature sensor ADC data has gone above the Temperature Alarm High Threshold. This read-only bit is cleared when STATUS 2 (register 0x01) is read.

STATUS 3 (0x02)

BIT	7	6	5	4	3	2	1	0
Field	S2_ADC_DATA_RDY	S2_ADC_DATA_LO	S2_ADC_DATA_HI	S2_DET	S1_ADC_DATA_RDY	S1_ADC_DATA_LO	S1_ADC_DATA_HI	S1_DET
Reset	0b0	0b0	0b0	0b0	0b0	0b0	0b0	0b0
Access Type	Read Only	Read Only	Read Only	Read Only	Read Only	Read Only	Read Only	Read Only

S2_ADC_DATA_RDY

The Sn_ADC_DATA_RDY (n = 1 to 4) bit is set to 1 when the sensor n ADC has completed, and the data is available in the FIFO. This is a read-only bit. It is cleared when STATUS 3 (n = 1 or 2) (register 0x02) or STATUS 4 (n = 3 or 4) (register 0x03)is read.

S2_ADC_DATA_LO

The Sn_ADC_DATA_LO (n = 1 to 4) bit is set to 1 when the sensor n ADC data has gone below the sensor n Alarm Low Threshold. This is a read-only bit. It is cleared when the STATUS 3 (n = 1 or 2) (register 0x02) or STATUS 4 (n = 3 or 4) (register 0x03) is read.

S2_ADC_DATA_HI

The Sn_ADC_DATA_HI (n = 1 to 4) bit is set to 1 when the sensor n ADC data has gone above the sensor n Alarm High Threshold. This is a read-only bit. It is cleared when the STATUS 3 (n = 1 or 2) (register 0x02) or STATUS 4 (n = 3 or 4) (register 0x03) is read.

S2_DET

The Sn_DET (n = 1 to 4) bit is set to 1 when sensor n is "wet" (sensor is in sensing fluid). It is cleared when the STATUS 3 (n = 1 or 2) (register 0x02) or STATUS 4 (n = 3 or 4) (register 0x03) is read. Sensor detection is enabled by setting Sn_DETECTOR_EN (n = 1 to 4) (0x22, 0x2F, 0x3C, 0x49) to 1.

S1_ADC_DATA_RDY

See S2_ADC_DATA_RDY for details.

S1_ADC_DATA_LO

See S2_ADC_DATA_LO for details.

S1_ADC_DATA_HI

See S2_ADC_DATA_HI for details.

S1_DET

See S2_DET for details.

STATUS 4 (0x03)

BIT	7	6	5	4	3	2	1	0
Field	S4_ADC_DATA_RDY	S4_ADC_DATA_LO	S4_ADC_DATA_HI	S4_DET	S3_ADC_DATA_RDY	S3_ADC_DATA_LO	S3_ADC_DATA_HI	S3_DET
Reset	0b0	0b0	0b0	0b0	0b0	0b0	0b0	0b0
Access Type	Read Only	Read Only	Read Only	Read Only	Read Only	Read Only	Read Only	Read Only

S4_ADC_DATA_RDY

See S2_ADC_DATA_RDY for details.

S4_ADC_DATA_LO

See S2_ADC_DATA_LO for details.

S4_ADC_DATA_HI

See S2_ADC_DATA_HI for details.

S4_DET

See S2_DET for details.

S3_ADC_DATA_RDY

See S2_ADC_DATA_RDY for details.

S3_ADC_DATA_LO

See S2_ADC_DATA_LO for details.

S3_ADC_DATA_HI

See S2_ADC_DATA_HI for details.

S3_DET

See S2_DET for details.

STATUS 5 (0x04)

BIT	7	6	5	4	3	2	1	0
Field	GPIO4_RDET	GPIO3_RDET	GPIO2_RDET	GPIO1_RDET	GPIO4_FDET	GPIO3_FDET	GPIO2_FDET	GPIO1_FDET
Reset	0b0	0b0	0b0	0b0	0b0	0b0	0b0	0b0
Access Type	Read Only	Read Only	Read Only	Read Only	Read Only	Read Only	Read Only	Read Only

GPIO4_RDET

The GPIOx_RDET (x = 1 to 4) bit is set to 1 when at least one rising edge is detected on the GPIOx pin. It is cleared when STATUS 5 (register 0x04) is read. GPIOx_RDET is only active when GPIOx_MODE[3:0] (x = 1 to 4) (0x90, 0x91, 0x92, 0x93) = 0x1.

GPIO3_RDET

See GPIO4_RDET for details.

GPIO2_RDET

See GPIO4_RDET for details.

GPIO1_RDET

See GPIO4_RDET for details.

GPIO4_FDET

The GPIOx_FDET (x = 1 to 4) bit is set to 1 when a falling edge is detected on the GPIOx pin. It is cleared when

STATUS 5 (register 0x04) is read. GPIOx_FDET is only active when GPIOx_MODE[3:0] (x = 1 to 4) (0x90, 0x91, 0x92, 0x93) = 0x1.

GPIO3_FDET

See GPIO4_FDET for details.

GPIO2_FDET

See GPIO4_FDET for details.

GPIO1_FDET

See GPIO4_FDET for details.

INTERRUPT ENABLE 1 (0x05)

BIT	7	6	5	4	3	2	1	0
Field	A_FULL_EN	FIFO_DATA_RDY_EN	–	AC_DATA_RDY_EN	EIS_CAL_DONE_EN	INVALID_CFG_EN	VDD_OOR_EN	–
Reset	0b0	0b0	–	0b0	0b0	0b0	0b0	–
Access Type	Write, Read	Write, Read	–	Write, Read	Write, Read	Write, Read	Write, Read	–

A_FULL_EN

Set A_FULL_EN to 1 to assert an interrupt on theINTB pin when the A_FULL (0x00) status bit is set. INTB is deasserted when STATUS 1 (register 0x00) is read.

FIFO_DATA_RDY_EN

Set FIFO_DATA_RDY_EN to 1 to assert an interrupt on the INTB pin when the FIFO_DATA_RDY (0x00) status bit is set. INTB is deasserted when STATUS 1 (register 0x00) is read.

AC_DATA_RDY_EN

Set AC_DATA_RDY_EN to 1 to assert an interrupt on the INTB pin when the AC_DATA_RDY (0x00) status bit is set. INTB is deasserted when STATUS 1 (register 0x00) is read.

EIS_CAL_DONE_EN

Set EIS_CAL_DONE_EN to 1 to assert an interrupt on the INTB pin when the EIS_CAL_DONE (0x00) status bit is set. INTB is deasserted when STATUS 1 (register 0x00) is read.

INVALID_CFG_EN

Set INVALID_CFG_EN to 1 to assert an interrupt on the INTB pin when the INVALID_CFG (0x00) status bit is set. INTB is deasserted when STATUS 1 (register 0x00) is read.

VDD_OOR_EN

Set VDD_OOR_EN to 1 to assert an interrupt on the INTB pin when the VDD_OOR (0x00) status bit is set. INTB is deasserted when STATUS 1 (register 0x00) is read.

INTERRUPT ENABLE 2 (0x06)

BIT	7	6	5	4	3	2	1	0
Field	SYS_ADC_DATA_RDY_EN	SYS_ADC_DATA_LO_EN	SYS_ADC_DATA_HI_EN	–	TEMP_DATA_RDY_EN	TEMP_DATA_LO_EN	TEMP_DATA_HI_EN	–
Reset	0b0	0b0	0b0	–	0b0	0b0	0b0	–
Access Type	Write, Read	Write, Read	Write, Read	–	Write, Read	Write, Read	Write, Read	–

SYS_ADC_DATA_RDY_EN

Set SYS_ADC_DATA_RDY_EN to 1 to assert an interrupt on the INTB pin when the SYS_ADC_DATA_RDY (0x01) status bit is set. INTB is deasserted when STATUS 2 (register 0x01) is read.

SYS_ADC_DATA_LO_EN

Set SYS_ADC_DATA_LO_EN to 1 to assert interrupt on the INTB pin when the SYS_ADC_DATA_LO (0x01) status bit is set. INTB is deasserted when STATUS 2 (register 0x01) is read.

SYS_ADC_DATA_HI_EN

Set SYS_ADC_DATA_HI_EN to 1 to assert an interrupt on the INTB pin when the SYS_ADC_DATA_HI (0x01) status bit is set. INTB is deasserted when STATUS 2 (register 0x01) is read.

TEMP_DATA_RDY_EN

Set TEMP_DATA_RDY_EN to 1 to assert an interrupt on the INTB pin when the TEMP_ADC_DATA_RDY (0x01) status bit is set. INTB is deasserted when STATUS 2 (register 0x01) is read.

TEMP_DATA_LO_EN

Set TEMP_DATA_LO_EN to 1 to assert an interrupt on the INTB pin when the TEMP_DATA_LO (0x01) status bit is set. INTB is deasserted when STATUS 2 (register 0x01) is read.

TEMP_DATA_HI_EN

Set TEMP_DATA_HI_EN to 1 to assert an interrupt on the INTB pin when the TEMP_ADC_DATA_HI (0x01) status bit is set. INTB is deasserted when STATUS 2 (register 0x01) is read.

INTERRUPT ENABLE 3 (0x07)

BIT	7	6	5	4	3	2	1	0
Field	S2_ADC_DATA_RDY_EN	S2_ADC_DATA_LO_EN	S2_ADC_DATA_HI_EN	S2_DET_EN	S1_ADC_DATA_RDY_EN	S1_ADC_DATA_LO_EN	S1_ADC_DATA_HI_EN	S1_DET_EN
Reset	0b0	0b0	0b0	0b0	0b0	0b0	0b0	0b0
Access Type	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read

S2_ADC_DATA_RDY_EN

Set Sn_ADC_DATA_RDY_EN (n = 1 to 4) to 1 to assert an interrupt on the INTB pin when the Sn_ADC_DATA_RDY (n = 1 or 2; 0x02) (n = 3 or 4; 0x03) status bit is set. INTB is deasserted when the corresponding STATUS register is read.

S2_ADC_DATA_LO_EN

Set Sn_ADC_DATA_LO_EN (n = 1 to 4) to 1 to 1 to assert an interrupt on the INTB pin when the Sn_ADC_DATA_LO (n = 1 or 2; 0x02) (n = 3 or 4; 0x03) status bit is set. INTB is deasserted when the corresponding STATUS register is read.

S2_ADC_DATA_HI_EN

Set Sn_ADC_DATA_HI (n = 1 to 4) to 1 to assert an interrupt on the INTB pin when the Sn_ADC_DATA_HI (n = 1 or 2; 0x02) (n = 3 or 4; 0x03) status bit is set. INTB is deasserted when the corresponding STATUS register is read.

S2_DET_EN

Set Sn_DET_EN (n = 1 to 4) to 1 to assert an interrupt on the INTB pin when the Sn_DET (n = 1 or 2; 0x02) (n = 3 or 4; 0x03) status bit is set. INTB is deasserted when the corresponding STATUS register is read.

S1_ADC_DATA_RDY_EN

See S2_ADC_DATA_RDY_EN for details.

S1_ADC_DATA_LO_EN

See S2_ADC_DATA_LO_EN for details.

S1_ADC_DATA_HI_EN

See S2_ADC_DATA_HI_EN for details.

S1_DET_EN

See S2_DET_EN for details.

INTERRUPT ENABLE 4 (0x08)

BIT	7	6	5	4	3	2	1	0
Field	S4_ADC_DATA_RDY_EN	S4_ADC_DATA_LO_EN	S4_ADC_DATA_HI_EN	S4_DET_EN	S3_ADC_DATA_RDY_EN	S3_ADC_DATA_LO_EN	S3_ADC_DATA_HI_EN	S3_DET_EN
Reset	0b0	0b0	0b0	0b0	0b0	0b0	0b0	0b0
Access Type	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read

S4_ADC_DATA_RDY_EN

See S2_ADC_DATA_RDY_EN for details.

S4_ADC_DATA_LO_EN

See S2_ADC_DATA_LO_EN for details.

S4_ADC_DATA_HI_EN

See S2_ADC_DATA_HI_EN for details.

S4_DET_EN

See S2_DET_EN for details.

S3_ADC_DATA_RDY_EN

See S2_ADC_DATA_RDY_EN for details.

S3_ADC_DATA_LO_EN

See S2_ADC_DATA_LO_EN for details.

S3_ADC_DATA_HI_EN

See S2_ADC_DATA_HI_EN for details.

S3_DET_EN

See S2_DET_EN for details.

INTERRUPT ENABLE 5 (0x09)

BIT	7	6	5	4	3	2	1	0
Field	GPIO4_RDET_EN	GPIO3_RDET_EN	GPIO2_RDET_EN	GPIO1_RDET_EN	GPIO4_FDET_EN	GPIO3_FDET_EN	GPIO2_FDET_EN	GPIO1_FDET_EN
Reset	0b0	0b0	0b0	0b0	0b0	0b0	0b0	0b0
Access Type	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read

GPIO4_RDET_EN

Set GPIOx_RDET_EN (x = 1 to 4) to 1 to assert an interrupt on the INTB pin when the GPIOx_RDET (0x04) status bit is set. INTB is deasserted when STATUS 5 (register 0x04) is read.

GPIO3_RDET_EN

See GPIO4_RDET_EN for details.

GPIO2_RDET_EN

See GPIO4_RDET_EN for details.

GPIO1_RDET_EN

See GPIO4_RDET_EN for details.

GPIO4_FDET_EN

Set GPIOx_FDET_EN (x = 1 to 4) to 1 to assert an interrupt on the INTB pin when the GPIOx_FDET (0x04) status bit is set. INTB is deasserted when STATUS 5 (register 0x04) is read.

GPIO3_FDET_EN

See GPIO4_FDET_EN for details.

GPIO2_FDET_EN

See GPIO4_FDET_EN for details.

GPIO1_FDET_EN

See GPIO4_FDET_EN for details.

FIFO WRITE POINTER (0x0A)

BIT	7	6	5	4	3	2	1	0
Field	FIFO_WR_PTR[7:0]							
Reset	0x00							
Access Type	Read Only							

FIFO_WR_PTR

FIFO_WR_PTR[7:0] points to the location where the next sample will be written. This pointer advances for each sample pushed on to the circular FIFO. See the FIFO Description section for more details.

FIFO READ POINTER (0x0B)

BIT	7	6	5	4	3	2	1	0
Field	FIFO_RD_PTR[7:0]							
Reset	0x00							
Access Type	Write, Read, Dual							

FIFO_RD_PTR

FIFO_RD_PTR[7:0] points to the location from where the processor gets the next sample from the FIFO using the serial interface. This advances each time a sample is popped from the circular FIFO.

The processor can also write to this pointer after reading the samples. This allows rereading (or retrying) samples from the FIFO. However, writing to FIFO_RD_PTR can have adverse effects if it results in the FIFO being almost full. See the FIFO Description section for more details.

FIFO COUNTER 1 (0x0C)

BIT	7	6	5	4	3	2	1	0
Field	FIFO_DATA_COUNT[8]	OVF_COUNTER[6:0]						
Reset	0b0	0b0000000						
Access Type	Read Only	Read Only						

FIFO_DATA_COUNT

FIFO_DATA_COUNT[8] is a read-only bit that holds the most significant bit of the number of items available in the FIFO for the processor to read. The lower 8 bits are in the FIFO COUNTER 2 register.

The 9-bit FIFO_DATA_COUNT[8:0] register increments when a new item is pushed to the FIFO and decrements when the processor reads an item from the FIFO. See the FIFO Description section for more details.

OVF_COUNTER

When the FIFO is full, any new samples result in new or old samples getting lost depending on the FIFO_RO (0x10). OVF_COUNTER[6:0] counts the number of samples lost. It saturates at 0x7F counts and is cleared when a sample is read from the FIFO. See the FIFO Description section for more details.

FIFO COUNTER 2 (0x0D)

BIT	7	6	5	4	3	2	1	0
Field	FIFO_DATA_COUNT[7:0]							
Reset	0x00							
Access Type	Read Only							

FIFO_DATA_COUNT

FIFO_DATA_COUNT[7:0] is a read-only register that holds the lower 8 bits of the number of items available in the FIFO for the processor to read. See the FIFO_DATA_COUNT (0x0C) description for details.

FIFO DATA (0x0E)

BIT	7	6	5	4	3	2	1	0
Field	FIFO_DATA[7:0]							
Reset								
Access Type	Read Only							

FIFO_DATA

FIFO_DATA[7:0] is a read-only register used to read data from the FIFO. The FIFO_RD_PTR[7:0] (0x0B) increments when the processor burst reads one complete sample word, which is three bytes. The external register address does not increment when the processor reads FIFO DATA[7:0]. Hence, burst reading register 0x0E does not advance to register 0x0F but instead advances the FIFO_RD_PTR[7:0] to the next unread sample in the FIFO. See the FIFO Description section for more details.

FIFO CONFIGURATION 1 (0x0F)

BIT	7	6	5	4	3	2	1	0
Field	FIFO_A_FULL[7:0]							
Reset	0x7F							
Access Type	Write, Read							

FIFO_A_FULL

FIFO_A_FULL[7:0] indicates how many new samples can be written to the FIFO before the A_FULL interrupt is asserted. For example, if set to 0x0F, the interrupt triggers when there are 15 empty spaces left (241 entries), and so on. See the FIFO Description section for more details.

FIFO_A_FULL[7:0]	FREE SPACE BEFORE INTERRUPT	# OF SAMPLES IN FIFO
0x00	0	256
0x01	1	255
0x02	2	254
0x03	3	253
----	----	----
0xFE	254	2
0xFF	255	1

FIFO CONFIGURATION 2 (0x10)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	FLUSH_FIFO	FIFO_STAT_CLR	A_FULL_TYPE	FIFO_RO	–
Reset	–	–	–	0b0	0b0	0b0	0b0	–
Access Type	–	–	–	Write, Read	Write, Read	Write, Read	Write, Read	–

FLUSH_FIFO

Set FIFO_FLUSH to 1 to flush the FIFO. When the FIFO is flushed, FIFO_WR_PTR[7:0] (0x0A), FIFO_RD_PTR[7:0] (0x0B), FIFO_DATA_COUNT[8:0] (0x0D), and OVF_COUNTER[6:0] (0x0C) become 0, and the contents of the FIFO are lost. FIFO_FLUSH is a self-clearing bit.

FIFO_STAT_CLR

FIFO_STAT_CLR defines whether the A_FULL (0x00) and FIFO_DATA_RDY (0x00) interrupt should get cleared by a FIFO_DATA (0x0E) read.

FIFO_STAT_CLR = 0: Clears A_FULL and FIFO_DATA_RDY status bits when STATUS 1 (register 0x00) is read.

FIFO_STAT_CLR = 1: Clears the A_FULL and FIFO_DATA_RDY status bits when STATUS 1 (register 0x00) is read or when FIFO_DATA (0x0E) is read.

A_FULL_TYPE

A_FULL_TYPE defines the behavior of the A_FULL (0x00) status.

A_FULL_TYPE = 0: The A_FULL status bit is asserted when the almost full condition is detected. It is deasserted by a STATUS 1 (register 0x00) read but reasserts for every sample if the almost full condition persists.

A_FULL_TYPE = 1: The A_FULL status bit is asserted when the almost full condition is detected. It is deasserted by a STATUS 1 (register 0x00) read, and does not reassert for every sample until a new almost full condition is detected.

FIFO_RO

The FIFO_RO bit controls the behavior of the FIFO when the FIFO becomes completely filled with data.

FIFO_RO = 0: Stops pushing data to FIFO when the FIFO is full. New samples are lost. FIFO_WR_PTR (0x0A) and FIFO_RD_PTR (0x0B) do not increment for each sample after the FIFO is full.

FIFO_RO = 1: Pushes data to FIFO when the FIFO is full. Old samples are lost. Both FIFO_WR_PTR (0x0A) and FIFO_RD_PTR (0x0B) increment for each sample after the FIFO is full.

SYSTEM CONTROL (0x14)

BIT	7	6	5	4	3	2	1	0
Field	BYPASS_LDO	CLK_SEL	SENSOR_CAL	–	–	–	SHDN	RESET
Reset	0b0	0b0	0b0	–	–	–	0b0	0b0
Access Type	Write, Read	Write, Read	Write, Read	–	–	–	Write, Read	Write, Read

BYPASS_LDO

BYPASS_LDO = 0, the internal LDO is used. The LDO is driven from V_{DD} and its output is nominally set to 1.8V. For optimal operation it is recommend to use a 1.95V minimum V_{DD}.

If the V_{DD} voltage aproaches or is below the LDO output voltage, the supply current increases. For V_{DD} voltages below 1.95V, it is recommend to set BYPASS_LDO = 1.

BYPASS_LDO =1, the internal LDO is disabled, and V_{DD} is connected directly to the internal power bus, bypassing the internal LDO, resulting in a reduction of power consumption. V_{DD} must be in the range of 1.73V to 1.95V when enabling this bit.

Caution: if BYPASS_LDO is enabled and V_{DD} is greater than 2.0V, the IC will be damaged. Use care when setting this bit.

CLK_SEL

The CLK_SEL bit sets the internal clock frequency used to program the sensor ADC conversion rate. The internal clock is also used to generate the sample periods for autonomous mode.

CLK_SEL = 0, selects 34.95kHz.

CLK_SEL = 1, selects 40.96kHz.

During EIS mode ADC conversions and EIS calibrations, CLK_SEL is ignored, and the device uses 40.96kHz.

SENSOR_CAL

Set SENSOR_CAL to 1 to add an offset current defined by register bits Sn_OFFSET_SEL[2:0] (0x23) to each sensor ADC sequentially. The bit gets cleared after the last sensor ADC conversion. This bit is ignored during EIS conversion or when AUTO (0x83) is set to 1. The offset data is stored at each sensor offset registers, Sn_IOFFSET[15:0] (n = 1 to 4) (0x2B, 0x38, 0x45, 0x52). In this mode, the sensors are disconnected from the ADC. See the Offset Gain Calibration section for more details.

SHDN

The SHDN bit is used to put the device into power-save mode by setting this bit to one. While in power-save mode, all configuration registers retain their values and write/read operations function as normal. All interrupts are cleared to zero, and the FIFO is reset to its power on default state.

RESET

When RESET is set to 1, the device undergoes a forced power-on-reset sequence. All configuration, threshold, and data registers are reset to their power-on state. This bit then automatically becomes 0 after the reset sequence is completed.

SENSOR CONFIGURATION (0x1F)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	–	SHARED_CA	DETECTOR_BIAS[1:0]	
Reset	–	–	–	–	–	0b0	0b00	
Access Type	–	–	–	–	–	Write, Read	Write, Read	

SHARED_CA

Set SHARED_CA to 1 to enable the shared CE amplifier mode to use a sensor with multiple WE electrodes and a single pair of RE and CE electrodes. When using this mode, connect the common sensor RE and CE to RE1 and CE1. This allows the AFE to perform EIS measurement between different WE electrodes and RE1 and CE1.

DETECTOR_BIAS

The DETECTOR_BIAS[1:0] bits select the sensor bias when the sensor detect is enabled.

DETECTOR_BIAS[1:0]	DETECTOR BIAS VOLTAGE (mV)
00	200
01	400
10	600
11	800

SENSOR 1 CONFIGURATION 1 (0x20)

BIT	7	6	5	4	3	2	1	0
Field	S1_WE_AMP_EN	S1_CE_AMP_EN	S1_WE_DAC_MX[1:0]		S1_CE_DAC_MX[1:0]		S1_CP_EN	S1_CHOP_EN
Reset	0b0	0b0	0b00		0b00		0b0	0b0
Access Type	Write, Read	Write, Read	Write, Read		Write, Read		Write, Read	Write, Read

S1_WE_AMP_EN

(n = 1 to 4)

Sn_WE_AMP_EN = 0: Powers down the sensor n working amplifier.

Sn_WE_AMP_EN = 1: Powers up the sensor n working amplifier.

S1_CE_AMP_EN

(n = 1 to 4)

Sn_CE_AMP_EN = 0: Powers down the sensor n counter amplifier.

Sn_CE_AMP_EN = 1: Powers up the sensor n counter amplifier.

S1_WE_DAC_MX

(n = 1 to 4)

Sn_WE_DAC_MX[1:0] selects which DAC is connected to the sensor n working amplifier non-inverting input.

See the Sn_WE_DAC_MX[1:0] table for the programmable sensor n working amplifier input mux selections.

Sn_WE_DAC_MX[1:0] (n = 1 to 4)	DESCRIPTION
00	DACA
01	DACB
10	DACC (2- and 4-ch versions only)
11	DACD (2- and 4-ch versions only)

S1_CE_DAC_MX

(n = 1 to 4)

Sn_CE_DAC_MX[1:0] selects which DAC is connected to the sensor n counter amplifier noninverting input.

See the Sn_CE_DAC_MX[1:0] table for the programmable sensor n counter amplifier input mux selections.

Sn_CE_DAC_MX[1:0] (n = 1 to 4)	DESCRIPTION
00	DACA

01	DACB
10	DACC (2- and 4-ch versions only)
11	DACD (2- and 4-ch versions only)

S1_CP_EN

(n = 1 to 4)

Sn_CP_EN = 0: When WEn and REn are equal or less than V_{DD} - 1.1V.

Sn_CP_EN = 1: Enables the charge pump for sensor n.

S1_CHOP_EN

(n = 1 to 4)

Sn_CHOP_EN = 0: Disables the chopper for sensor n.

Sn_CHOP_EN = 1: Enables the chopper for sensor n. Enabling the chopper reduces the AFE offset, but adds ripple on the sensor bias.

SENSOR 1 CONFIGURATION 2 (0x21)

BIT	7	6	5	4	3	2	1	0
Field	S1_SWB	S1_SWA	S1_SC	S1_SRB	S1_SRA	S1_ILIM_EN	S1_RS	S1_SWO
Reset	0b0	0b0	0b0	0b0	0b0	0b0	0b0	0b0
Access Type	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read

S1_SWB

(n = 1 to 4)

Sn_SWB = 0: Opens the analog switch between the working amplifier n inverting input and WEn. Opening the analog switch enables the Sensor n working amplifier inverting input to be connected to the REn pin when Sn_SRA = 1 and Sn_SRB = 0. In this mode, current can be measured in the opposite direction by flipping the external working and counter sensor connections.

Sn_SWB = 1: Closes the analog switch between the Sensor n working amplifier inverting input and the WEn pin. Closing the analog switch enables the WEn pin to be biased to the voltage at the non-inverting input of the Sensor n working amplifier and measure current on WEn when Sn_SWA = 0.

See the Sn_Sxx table for common sensor switch configurations.

Sn_SWA (n = 1 to 4)	Sn_SWB (n = 1 to 4)	Sn_SRA (n = 1 to 4)	Sn_SRB (n = 1 to 4)	Sn_SC (n = 1 to 4)	DESCRIPTION
Open	Closed	Open	Closed	Open	Use this switch configuration for a 3-terminal sensor with positive current out of the WEn pin and into the working electrode of the connected sensor. Connect the WEn, REn, and CEn pins to the working, reference, and counter electrodes of the connected sensor, respectively.
Open	Open	Closed	Open	Closed	Use this switch configuration for a 3-terminal sensor with positive current out of the working electrode of the sensor and into the WEn pin. Connect the CEn, REn, and WEn pins to the working, reference, and counter electrodes of the connected sensor, respectively.

Open	Closed	Open	Open	Closed	Use this switch configuration for a 2-terminal sensor with positive current out of the WEn pin and into the working electrode of the connected sensor and both electrodes actively driven. Connect the WEn and CEn pins to the working and counter electrodes of the connected sensor, respectively. Alternatively, the counter amplifier can be powered down and the counter electrode of the connected sensor can be connected directly to ground.
Closed	Closed	Open	-	-	Use this switch configuration to use the working amplifier as a unity gain follower or as a guard ring driver to protect sensitive nodes from leakage current on the printed circuit board.
-	-	-	Open	Closed	Use this switch configuration to use the counter amplifier as a unity gain follower or as a guard ring driver to protect sensitive nodes from leakage current on the printed circuit board.

S1_SWA

(n = 1 to 4)

Sn_SWA = 0: Opens the analog switch between the Sensor n working amplifier output and WEn. Opening the analog switch enables current measurement on WEn with the corresponding Sensor ADC.

Sn_SWA = 1: Closes the analog switch between the sensor n working amplifier output and the WEn pin. Closing the analog switch bypasses the NMOS transistor and disables current measurement capability on WEn. In this mode, the sensor n working amplifier can be used as a unity gain follower or as a guard ring driver.

See S1_SWB description for common sensor switch configurations.

S1_SC

(n = 1 to 4)

Sn_SC = 0: Opens the analog switch between the sensor n counter amplifier inverting input and CEn.

Sn_SC = 1: Closes the analog switch between the sensor n counter amplifier inverting input and the sensor n CEn pin. Closing the analog switch configures the sensor n counter amplifier as a unity gain follower.

See S1_SWB description for common sensor switch configurations.

S1_SRB

(n = 1 to 4)

Sn_SRB = 0: Opens the analog switch between the sensor n counter amplifier inverting input and REn.

Sn_SRB = 1: Closes the analog switch between the sensor n counter amplifier inverting input and the sensor n REn pin.

See S1_SWB description for common sensor switch configurations.

S1_SRA

(n = 1 to 4)

Sn_SRA = 0: Opens the analog switch between the sensor n working amplifier inverting input and REn.

Sn_SRA = 1: Closes the analog switch between the sensor n working amplifier inverting input and the sensor n REn pin.

See S1_SWB description for common sensor switch configurations.

S1_ILIM_EN

(n = 1 to 4)

Sn_ILIM_EN = 0: Disables the current limiter on the WEn pin.

Sn_ILIM_EN = 1: Enables the current limiter on the WEn pin. The current limit is between 20μA and 50μA.

S1_RS

(n = 1 to 4)

Sn_RS = 0: Sensor n ADC curcuitry is connected directly to the WEn output.

Sn_RS = 1: Add a 60kΩ resistor in series with WEn. Adding the resistor improves amplifier stability when the sensor current is low, and the capacitance is high.

S1_SWO

(n = 1 to 4)

Sn_SWO = 0: Opens the analog switch between the sensor n working amplifier output and the GPIOn pin.

Sn_SWO = 1: Closes the analog switch between the sensor n working amplifier output and the GPIOn pin.

The switch allows the user to add an external bypass capacitor between WE and WO to filter 50Hz/60Hz noise.

When Sn_SWO = 1 and Sn_CP_EN (0x20, 0x2D, 0x3A, 0x47) = 0, the maximum WE voltage is V_{DD} - 1.5V.

When Sn_SWO = 1 and Sn_CP_EN = 1, the maximum WE voltage is V_{DD} - 1.1V.

SENSOR 1 CONFIGURATION 3 (0x22)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	S1_IOS_MODE	S1_DETECTOR_EN	S1_DETECTOR_THRESHOLD[1:0]	
Reset	–	–	–	–	0b1	0b0	0b00	
Access Type	–	–	–	–	Write, Read	Write, Read	Write, Read	

S1_IOS_MODE

(n = 1 to 4)

Sn_IOS_MODE = 0: Enables the offset current on Sensor n ADC only during ADC conversion.

Sn_IOS_MODE = 1: Enables the offset current on the sensor n ADC always.

S1_DETECTOR_EN

(n = 1 to 4)

Sn_DETECTOR_EN = 0: Disables and resets the detect circuit for Sensor n. This should be done for all operating modes other than senor detect mode.

Sn_DETECTOR_EN = 1: Enables the detect circuit for the sensor n. Sn_WE_AMP_EN and Sn_CE_AMP_EN (0x20, 0x2D, 0x3A, 0x47) should be set to 0 (disabled) when using the sensor detect function. The WEn pin is biased at the voltage set by Sn_DETECTOR_BIAS while the CEn pin is connected to ground.

S1_DETECTOR_THRESHOLD

(n = 1 to 4)

Sn_DETECTOR_THRESHOLD[1:0] selects the sensor detect threshold current when the sensor detect is enabled.

Sn_DETECTOR_THRESHOLD[1:0]	THRESHOLD CURRENT (nA)
00	20
01	40
02	80
03	160

See Figure 11 for the programmable threshold currents.

SENSOR 1 CONFIGURATION 4 (0x23)

BIT	7	6	5	4	3	2	1	0
Field	S1_FSR[2:0]			–	–	S1_OFFSET_SEL[2:0]		
Reset	0b000			–	–	0b000		
Access Type	Write, Read			–	–	Write, Read		

S1_FSR

(n = 1 to 4)

Sn_FSR[2:0] sets the full scale current range of the Sensor n ADC. The sensor n ADC can measure input current range up to 99.6% of the ADC full scale current range.

See the Sn_FSR[2:0] table for the programmable Sensor n ADC full-scale currents.

Sn_FSR[2:0] (n = 1 to 4)	SENSOR n ADC FULL SCALE CURRENT RANGE (nA) (n = 1 to 4)
000	50
001	100
010	250
011	500
100	1000
101	2000
110	Reserved. Not used
111	Reserved. Not used

S1_OFFSET_SEL

(n = 1 to 4)

Sn_OFFSET_SEL[2:0] programs the sensor n offset current for the sensor n ADC. Programming other than zero allows pseudo-bipolar-current measurements on the WEn pin. Programming the offset current to zero (unipolar) is not recomended as there must alwas be some current flow for the WE ampifier circuity to function properly.

See the Sn_OFFSET_SEL[2:0] table for the Sensor n ADC offset current values.

Sn_OFFSET_SEL[2:0] (n = 1 to 4)	DESCRIPTION
000	0% offset (unipolar)
001	10% of the full scale current
010	20% of the full scale current
011	50% of the full scale current
100	10nA
101	20nA
110	40nA
111	80nA

SENSOR 1 CONFIGURATION 5 (0x24)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	S1_CONV_TIME[3:0]				S1_SELECT
Reset	–	–	–	0x0				0b0
Access Type	–	–	–	Write, Read				Write, Read

S1_CONV_TIME

(n = 1 to 4)

Sn_CONV_TIME[3:0] sets the conversion time of the sensor n ADC.

There are two internal clocks that can be selected using CLK_SEL for sensor ADC conversions. The selected clock is common for all sensor channels. The ADC conversion runs for a minimum of 4,095 clocks to a maximum of 8,388,607 clocks. For conversions longer than 65,535 clocks, the result is decimated to limit the output to 65,535 or 16-bits.

When Sn_FSR[2:0] (0x23, 0x30, 0x3D, 0x4A) for all four Sensor ADCs is less than 4, the Sensor ADC channels use 34.952kHz/40.96kHz clock. When Sn_FSR[2:0] for at least one of the four sensor ADCs is greater than 3, all four ADC channels use 4 times clock frequency (139.808kHz/163.84kHz).

See the Sn_CONV_TIME[3:0] tables for the programmable sensor n ADC conversion times. It assumes the nominal 246 slow clock cycles for the sensor n ADC precharge phase.

When IOFFSET_CONV (0x80) = 2, ((Sensor + Offset) - Offset), two separate measurements are made, and the time to complete the measurement will be twice as long as listed in the tables.

Sn_FSR[2:0] for all four sensor ADCs is less than 4:

Sn_CONV_TIME[3:0]	INTEGRATION TIME PER ADC CONVERSION			CONVERSION TIME PER ADC CONVERSION			RESOLUTION
	COUNTER	CLK_SEL = 0	CLK_SEL = 1	COUNTER	CLK_SEL = 0	CLK_SEL = 1	DECIMATED
	(clocks)	(seconds)	(seconds)	(clocks)	(seconds)	(seconds)	(bits)
0x0	4,095	0.117	0.1	4,342	0.124	0.106	12
0x1	8,191	0.234	0.2	8,438	0.241	0.206	13
0x2	16,383	0.469	0.4	16,630	0.476	0.406	14
0x3	32,767	0.937	0.8	33,014	0.945	0.806	15
0x4	65,535	1.875	1.6	65,782	1.882	1.606	16
0x5	131,071	3.75	3.2	131,318	3.757	3.206	16
0x6	262,143	7.5	6.4	262,390	7.507	6.406	16
0x7	524,287	15	12.8	524,534	15.007	12.806	16
0x8	1,048,575	30	25.6	1,048,822	30.007	25.606	16
0x9	2,097,151	60.001	51.2	2,097,398	60.008	51.206	16
0xA	4,194,303	120.002	102.4	4,194,550	120.009	102.406	16
0xB to 0xF	8,388,607	240.004	204.8	8,388,854	240.011	204.806	16

Sn_FSR[2:0] for all at least one of the four sensor ADCs is greater than 3:

Sn_CONV_ TIME[3:0]	**INTEGRATION TIME PER ADC CONVERSION**			**CONVERSION TIME PER ADC CONVERSION**			**RESOLUTION**
	COUNTER	**CLK_SEL = 0**	**CLK_SEL = 1**	**COUNTER**	**CLK_SEL = 0**	**CLK_SEL = 1**	**DECIMATED**
	(clocks)	**(seconds)**	**(seconds)**	**(clocks)**	**(seconds)**	**(seconds)**	**(bits)**
0x0	4,095	0.029	0.025	4,342	0.031	0.027	12
0x1	8,191	0.059	0.05	8,438	0.06	0.052	13
0x2	16,383	0.117	0.1	16,630	0.119	0.102	14
0x3	32,767	0.234	0.2	33,014	0.236	0.202	15
0x4	65,535	0.469	0.4	65,782	0.471	0.402	16
0x5	131,071	0.938	0.8	131,318	0.939	0.802	16
0x6	262,143	1.875	1.6	262,390	1.877	1.602	16
0x7	524,287	3.75	3.2	524,534	3.752	3.202	16
0x8	1,048,575	7.5	6.4	1,048,822	7.502	6.402	16
0x9	2,097,151	15	12.8	2,097,398	15.002	12.802	16
0xA	4,194,303	30	25.6	4,194,550	30.002	25.602	16
0xB to 0xF	8,388,607	60.001	51.2	8,388,854	60.003	51.202	16

S1_SELECT

(n = 1 to 4)

Sn_SELECT = 0: Excludes sensor n from data conversions.

Sn_SELECT = 1: Includes sensor n in manual or automatic data conversions.

See CONVERT for more information.

SENSOR 1 ALARM LOW SETUP (0x25)

BIT	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Field	S1_LO_MODE	S1_LO_TRIP	S1_LO_TRIP_CNT[1:0]		S1_LO_DET_CNTR[2:0]			S1_RST_LO_CNTR
Reset	0b0	0b0	0b00		0b000			0b0
Access Type	Write, Read	Write, Read	Write, Read		Read Only			Write, Read

S1_LO_MODE

(n = 1 to 4)

Sn_LO_MODE = 0: Programs the alarm low mode to be absolute. When in absolute mode, the sensor n ADC result is compared directly with the alarm low threshold value.

Sn_LO_MODE = 1: Programs the alarm low mode to be differential. When in differential mode, the difference between the last and the previous sensor n ADC result is compared with the alarm low threshold value. The difference mode is used to detect the negative slope or rate of change between successive sensor ADC results.

S1_LO_TRIP

(n = 1 to 4)

Sn_LO_TRIP = 0: Programs the alarm low trip type to consecutive. When the trip type is consecutive, the number of trips programmed with Sn_LO_TRIP_CNT[2:0] needs to be consecutive to assert the Sn_ADC_DATA_LO (n = 1 or 2;

0x02) (n = 3 or 4; 0x03) status bit.

Sn_LO_TRIP = 1: Programs the alarm low trip type to be nonconsecutive. When the trip type is nonconsecutive, the number of trips programmed with Sn_LO_TRIP_CNT[1:0] does not need to be consecutive to assert the Sn_ADC_DATA_LO status bit.

S1_LO_TRIP_CNT

(n = 1 to 4)

Sn_LO_TRIP_CNT[1:0] programs the number of trip counts required to assert the Sn_ADC_DATA_LO (n = 1 or 2; 0x02) (n = 3 or 4; 0x03) status bit.

See the Sn_LO_TRIP_CNT[1:0] table for the programmable Sensor 1 alarm low trip counts.

Sn_LO_TRIP_CNT[1:0] (n = 1 to 4)	**TRIP COUNT**
00	1
01	2
10	3
11	4

S1_LO_DET_CNTR

(n = 1 to 4)

Sn_LO_DET_CNTR[2:0] is a read only register that holds the count for the number of times the sensor n ADC data went below the sensor n alarm low threshold after the counter was cleared.

S1_RST_LO_CNTR

(n = 1 to 4)

Sn_RST_LO_CNTR is a self clearing bit. When set to 1, it clears the count in Sn_LO_DET_CNTR[2:0] register and is cleared itself.

SENSOR 1 ALARM HIGH SETUP (0x26)

BIT	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Field	S1_HI_MODE	S1_HI_TRIP	S1_HI_TRIP_CNT[1:0]		S1_HI_DET_CNTR[2:0]			S1_RST_HI_CNTR
Reset	0b0	0b0	0b00		0b000			0b0
Access Type	Write, Read	Write, Read	Write, Read		Read Only			Write, Read

S1_HI_MODE

(n = 1 to 4)

Sn_HI_MODE = 0: Programs the alarm high mode to be absolute. When in absolute mode, the Sensor n ADC result is compared directly with the alarm high threshold value.

Sn_HI_MODE = 1: Programs the alarm high mode to be differential. When in differential mode, the difference between the last and the previous sensor n ADC result is compared with the alarm high threshold value. The difference mode is used to detect the positive slope or rate of change between successive ADC results.

S1_HI_TRIP

(n = 1 to 4)

Sn_HI_TRIP = 0: Programs the alarm high trip type to consecutive. When the trip type is consecutive, the number of trips programmed with Sn_HI_TRIP_CNT[2:0] needs to be consecutive to assert the Sn_ADC_DATA_HI (n = 1 or 2; 0x02) (n = 3 or 4; 0x03) status bit.

Sn_HI_TRIP = 1: Programs the alarm high trip type to be nonconsecutive. When the trip type is nonconsecutive, the number of trips programmed with Sn_HI_TRIP_CNT[1:0] trip count does not need to be consecutive to assert the Sn_ADC_DATA_HI status bit.

S1_HI_TRIP_CNT

(n = 1 to 4)

Sn_HI_TRIP_CNT[1:0] programs the number of trip counts required to assert the Sn_ADC_DATA_HI (n = 1 or 2; 0x02) (n = 3 or 4; 0x03) status bit.

See the Sn_HI_TRIP_CNT[1:0] table for the programmable Sensor n alarm high trip counts.

Sn_HI_TRIP_CNT[1:0] (n = 1 to 4)	**TRIP COUNT**
00	1
01	2
10	3
11	4

S1_HI_DET_CNTR

(n = 1 to 4)

Sn_HI_DET_CNTR[2:0] is a read only register that holds the count for the number of times the sensor n ADC data went above the sensor n alarm high threshold after the counter was cleared.

S1_RST_HI_CNTR

(n = 1 to 4)

Sn_RST_HI_CNTR = 1 is a self clearing bit. When set to 1, it clears the count in Sn_HI_DET_CNTR[2:0] register and is cleared itself.

SENSOR 1 ALARM LOW MSB (0x27)

BIT	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Field	S1_LO_THRESH[15:8]							
Reset	0x00							
Access Type	Write, Read							

S1_LO_THRESH

(n = 1 to 4)

Sn_LO_THRESH[15:8] has the upper byte of the Sensor n ADC Alarm Low Threshold register, Sn_LO_THRESH[15:0]. The lower byte is in the Sn_LO_THRESH[7:0] register.

Sn_LO_THRESH[15:0] is an unsigned number that sets the alarm low threshold to compare to the Sensor n ADC results.

Sn_LO_THRESH[15:0] = 0x0000: Disables the alarm.

SENSOR 1 ALARM LOW LSB (0x28)

BIT	7	6	5	4	3	2	1	0
Field	S1_LO_THRESH[7:0]							
Reset	0x00							
Access Type	Write, Read							

S1_LO_THRESH

(n = 1 to 4)

Sn_LO_THRESH[7:0] has the lower byte of the Sensor n ADC Alarm Low Threshold register, Sn_LO_THRESH[15:0]. The upper byte is in the Sn_LO_THRESH[15:8] register.

See S1_LO_THRESH[15:8] for more details.

SENSOR 1 ALARM HIGH MSB (0x29)

BIT	7	6	5	4	3	2	1	0
Field	S1_HI_THRESH[15:8]							
Reset	0xFF							
Access Type	Write, Read							

S1_HI_THRESH

(n = 1 to 4)

Sn_HI_THRESH[15:8] has the upper byte of the Sensor n ADC Alarm High Threshold register, Sn_HI_THRESH[15:0]. The lower byte is in the Sn_HI_THRESH[7:0] register.

Sn_HI_THRESH[15:0] is an unsigned number that sets the alarm high threshold to compare to the Sensor n ADC results.

Sn_HI_THRESH[15:0] = 0xFFFF: Disables the alarm.

SENSOR 1 ALARM HIGH LSB (0x2A)

BIT	7	6	5	4	3	2	1	0
Field	S1_HI_THRESH[7:0]							
Reset	0xFF							
Access Type	Write, Read							

S1_HI_THRESH

Sn_HI_THRESH[7:0] (n = 1 to 4) has the lower byte of the Sensor n ADC Alarm High Threshold register, Sn_HI_THRESH[15:0]. The upper byte is in the Sn_HI_THRESH[15:8] register.

See S1_HI_THRESH[15:8] for more details.

SENSOR 1 OFFSET CURRENT MSB (0x2B)

BIT	7	6	5	4	3	2	1	0
Field	S1_IOFFSET[15:8]							
Reset	0x00							
Access Type	Read Only							

S1_IOFFSET

(n = 1 to 4)

Sn_IOFFSET[15:8] holds the upper byte of the Sn_IOFFSET[15:0] offset current for sensor n ADC. Sn_IOFFSET[7:0] holds the lower byte of Sn_IOFFSET[15:0]. The offset current is measured when IOFFSET_CONV[1:0] (0x80) is set to 01 or 10. Sn_IOFFSET[15:0] also gets updated when calibration is done using the SENSOR_CAL bit.

SENSOR 1 OFFSET CURRENT LSB (0x2C)

BIT	7	6	5	4	3	2	1	0
Field	S1_IOFFSET[7:0]							
Reset	0x00							
Access Type	Read Only							

S1_IOFFSET

(n = 1 to 4)

Sn_IOFFSET[7:0] is the lower byte of Sn_IOFFSET[15:0]. See S1_IOFFSET[15:8] for details.

SENSOR 2 CONFIGURATION 1 (0x2D)

BIT	7	6	5	4	3	2	1	0
Field	S2_WE_AMP_EN	S2_CE_AMP_EN	S2_WE_DAC_MX[1:0]		S2_CE_DAC_MX[1:0]		S2_CP_EN	S2_CHOP_EN
Reset	0b0	0b0	0b00		0b00		0b0	0b0
Access Type	Write, Read	Write, Read	Write, Read		Write, Read		Write, Read	Write, Read

S2_WE_AMP_EN

See S1_WE_AMP_EN for details.

S2_CE_AMP_EN

See S1_CE_AMP_EN for details.

S2_WE_DAC_MX

See S1_WE_DAC_MX[1:0] for details.

S2_CE_DAC_MX

See S1_CE_DAC_MX[1:0] for details.

S2_CP_EN

See S1_CP_EN for details

S2_CHOP_EN

See S1_CHOP_EN for details

SENSOR 2 CONFIGURATION 2 (0x2E)

BIT	7	6	5	4	3	2	1	0
Field	S2_SWB	S2_SWA	S2_SC	S2_SRB	S2_SRA	S2_ILIM_EN	S2_RS	S2_SWO
Reset	0b0	0b0	0b0	0b0	0b0	0b0	0b0	0b0
Access Type	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read

S2_SWB

See S1_SWB for details

S2_SWA

See S1_SWA for details.

S2_SC

See S1_SC for details.

S2_SRB

See S1_SRB for details.

S2_SRA

See S1_SRA for details.

S2_ILIM_EN

See S1_ILIM_EN for details.

S2_RS

See S1_RS for details.

S2_SWO

See S1_SWO for details.

SENSOR 2 CONFIGURATION 3 (0x2F)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	S2_IOS_MODE	S2_DETECTOR_EN	S2_DETECTOR_THRESHOLD[1:0]	
Reset	–	–	–	–	0b1	0b0	0b00	
Access Type	–	–	–	–	Write, Read	Write, Read	Write, Read	

S2_IOS_MODE

See S1_IOS_MODE for details.

S2_DETECTOR_EN

See S1_DETECTOR_EN for details.

S2_DETECTOR_THRESHOLD

See S1_DETECTOR_THRESHOLD for details.

SENSOR 2 CONFIGURATION 4 (0x30)

BIT	7	6	5	4	3	2	1	0
Field	S2_FSR[2:0]			–	–	S2_OFFSET_SEL[2:0]		
Reset	0b000			–	–	0b000		
Access Type	Write, Read			–	–	Write, Read		

S2_FSR

See S1_FSR[1:0] for details.

S2_OFFSET_SEL

See S1_OFFSET_SEL[2:0] for details.

SENSOR 2 CONFIGURATION 5 (0x31)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	S2_CONV_TIME[3:0]				S2_SELECT
Reset	–	–	–	0x0				0b0
Access Type	–	–	–	Write, Read				Write, Read

S2_CONV_TIME

See S1_CONV_TIME[3:0] for details.

S2_SELECT

See S1_SELECT for details.

SENSOR 2 ALARM LOW SETUP (0x32)

BIT	7	6	5	4	3	2	1	0
Field	S2_LO_MODE	S2_LO_TRIP	S2_LO_TRIP_CNT[1:0]		S2_LO_DET_CNTR[2:0]			S2_RST_LO_CNTR
Reset	0b0	0b0	0b00		0b000			0b0
Access Type	Write, Read	Write, Read	Write, Read		Read Only			Write, Read

S2_LO_MODE

See S1_LO_MODE for details.

S2_LO_TRIP

See S1_LO_TRIP for details.

S2_LO_TRIP_CNT

See S1_LO_TRIP_CNT[1:0] for details.

S2_LO_DET_CNTR

See S1_LO_DET_CNTR[2:0] for details.

S2_RST_LO_CNTR

See S1_RST_LO_CNTR for details.

SENSOR 2 ALARM HIGH SETUP (0x33)

BIT	7	6	5	4	3	2	1	0
Field	S2_HI_MODE	S2_HI_TRIP	S2_HI_TRIP_CNT[1:0]		S2_HI_DET_CNTR[2:0]			S2_RST_HI_CNTR
Reset	0b0	0b0	0b00		0b000			0b0
Access Type	Write, Read	Write, Read	Write, Read		Read Only			Write, Read

S2_HI_MODE

See S1_HI_MODE for details.

S2_HI_TRIP

See S1_HI_TRIP for details.

S2_HI_TRIP_CNT

See S1_HI_TRIP_CNT[1:0] for details.

S2_HI_DET_CNTR

See S1_HI_DET_CNTR[2:0] for details.

S2_RST_HI_CNTR

See S1_RST_HI_CNTR for details.

SENSOR 2 ALARM LOW MSB (0x34)

BIT	7	6	5	4	3	2	1	0
Field	S2_LO_THRESH[15:8]							
Reset	0x00							
Access Type	Write, Read							

S2_LO_THRESH

See S1_LO_THRESH[15:8] for details.

SENSOR 2 ALARM LOW LSB (0x35)

BIT	7	6	5	4	3	2	1	0
Field	S2_LO_THRESH[7:0]							
Reset	0x00							
Access Type	Write, Read							

S2_LO_THRESH

See S1_LO_THRESH[15:8] for details.

SENSOR 2 ALARM HIGH MSB (0x36)

BIT	7	6	5	4	3	2	1	0
Field	S2_HI_THRESH[15:8]							
Reset	0xFF							
Access Type	Write, Read							

S2_HI_THRESH

See S1_HI_THRESH[15:8] for details.

SENSOR 2 ALARM HIGH LSB (0x37)

BIT	7	6	5	4	3	2	1	0
Field	S2_HI_THRESH[7:0]							
Reset	0xFF							
Access Type	Write, Read							

S2_HI_THRESH

See S1_HI_THRESH[15:8] for details.

SENSOR 2 OFFSET CURRENT MSB (0x38)

BIT	7	6	5	4	3	2	1	0
Field	S2_IOFFSET[15:8]							
Reset	0x00							
Access Type	Read Only							

S2_IOFFSET

See S1_IOFFSET[15:8] for details.

SENSOR 2 OFFSET CURRENT LSB (0x39)

BIT	7	6	5	4	3	2	1	0
Field	S2_IOFFSET[7:0]							
Reset	0x00							
Access Type	Read Only							

S2_IOFFSET

See S1_IOFFSET[15:8] for details.

SENSOR 3 CONFIGURATION 1 (0x3A)

BIT	7	6	5	4	3	2	1	0
Field	S3_WE_AMP_EN	S3_CE_AMP_EN	S3_WE_DAC_MX[1:0]		S3_CE_DAC_MX[1:0]		S3_CP_EN	S3_CHOP_EN
Reset	0b0	0b0	0b00		0b00		0b0	0b0
Access Type	Write, Read	Write, Read	Write, Read		Write, Read		Write, Read	Write, Read

S3_WE_AMP_EN

See S1_WE_AMP_EN for details.

S3_CE_AMP_EN

See S1_CE_AMP_EN for details.

S3_WE_DAC_MX

See S1_WE_DAC_MX[1:0] for details.

S3_CE_DAC_MX

See S1_CE_DAC_MX[1:0] for details.

S3_CP_EN

See S1_CP_EN for details.

S3_CHOP_EN

See S1_CHOP_EN for details

SENSOR 3 CONFIGURATION 2 (0x3B)

BIT	7	6	5	4	3	2	1	0
Field	S3_SWB	S3_SWA	S3_SC	S3_SRB	S3_SRA	S3_ILIM_EN	S3_RS	S3_SWO
Reset	0b0	0b0	0b0	0b0	0b0	0b0	0b0	0b0
Access Type	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read

S3_SWB

See S1_SWB for details.

S3_SWA

See S1_SWA for details.

S3_SC

See S1_SC for details.

S3_SRB

See S1_SRB for details.

S3_SRA

See S1_SRA for details.

S3_ILIM_EN

See S1_ILIM_EN for details.

S3_RS

See S1_RS for details.

S3_SWO

See S1_SWO for details.

SENSOR 3 CONFIGURATION 3 (0x3C)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	S3_IOS_MODE	S3_DETECTOR_EN	S3_DETECTOR_THRESHOLD[1:0]	
Reset	–	–	–	–	0b1	0b0	0b00	
Access Type	–	–	–	–	Write, Read	Write, Read	Write, Read	

S3_IOS_MODE

See S1_IOS_MODE for details.

S3_DETECTOR_EN

See S1_DETECTOR_EN for details.

S3_DETECTOR_THRESHOLD

See S1_DETECTOR_THRESHOLD for details.

SENSOR 3 CONFIGURATION 4 (0x3D)

BIT	7	6	5	4	3	2	1	0
Field	S3_FSR[2:0]			–	–	S3_OFFSET_SEL[2:0]		
Reset	0b000			–	–	0b000		
Access Type	Write, Read			–	–	Write, Read		

S3_FSR

See S1_FSR[2:0] for details.

S3_OFFSET_SEL

See S1_OFFSET_SEL[2:0] for details.

SENSOR 3 CONFIGURATION 5 (0x3E)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	S3_CONV_TIME[3:0]				S3_SELECT
Reset	–	–	–	0x0				0b0
Access Type	–	–	–	Write, Read				Write, Read

S3_CONV_TIME

See S1_CONV_TIME[3:0] for details.

S3_SELECT

See S1_SELECT for details.

SENSOR 3 ALARM LOW SETUP (0x3F)

BIT	7	6	5	4	3	2	1	0
Field	S3_LO_MODE	S3_LO_TRIP	S3_LO_TRIP_CNT[1:0]		S3_LO_DET_CNTR[2:0]			S3_RST_LO_CNTR
Reset	0b0	0b0	0b00		0b000			0b0
Access Type	Write, Read	Write, Read	Write, Read		Read Only			Write, Read

S3_LO_MODE

See S1_LO_MODE for details.

S3_LO_TRIP

See S1_LO_TRIP for details.

S3_LO_TRIP_CNT

See S1_LO_TRIP_CNT for details.

S3_LO_DET_CNTR

See S1_LO_DET_CNTR[2:0] for details.

S3_RST_LO_CNTR

See S1_RST_LO_CNTR for details.

SENSOR 3 ALARM HIGH SETUP (0x40)

BIT	7	6	5	4	3	2	1	0
Field	S3_HI_MODE	S3_HI_TRIP	S3_HI_TRIP_CNT[1:0]		S3_HI_DET_CNTR[2:0]			S3_RST_HI_CNTR
Reset	0b0	0b0	0b00		0b000			0b0
Access Type	Write, Read	Write, Read	Write, Read		Read Only			Write, Read

S3_HI_MODE

See S1_HI_MODE for details.

S3_HI_TRIP

See S1_HI_TRIP for details.

S3_HI_TRIP_CNT

See S1_HI_TRIP_CNT[1:0] for details.

S3_HI_DET_CNTR

See S1_HI_DET_CNTR[2:0] for details.

S3_RST_HI_CNTR

See S1_RST_HI_CNTR for details.

SENSOR 3 ALARM LOW MSB (0x41)

BIT	7	6	5	4	3	2	1	0
Field	S3_LO_THRESH[15:8]							
Reset	0x00							
Access Type	Write, Read							

S3_LO_THRESH

See S1_LO_THRESH[15:8] for details.

SENSOR 3 ALARM LOW LSB (0x42)

BIT	7	6	5	4	3	2	1	0
Field	S3_LO_THRESH[7:0]							
Reset	0x00							
Access Type	Write, Read							

S3_LO_THRESH

See S1_LO_THRESH[15:8] for details.

SENSOR 3 ALARM HIGH MSB (0x43)

BIT	7	6	5	4	3	2	1	0
Field	S3_HI_THRESH[15:8]							
Reset	0xFF							
Access Type	Write, Read							

S3_HI_THRESH

See S1_HI_THRESH[15:8] for details.

SENSOR 3 ALARM HIGH LSB (0x44)

BIT	7	6	5	4	3	2	1	0
Field	S3_HI_THRESH[7:0]							
Reset	0xFF							
Access Type	Write, Read							

S3_HI_THRESH

See S1_HI_THRESH[15:8] for details.

SENSOR 3 OFFSET CURRENT MSB (0x45)

BIT	7	6	5	4	3	2	1	0
Field	S3_IOFFSET[15:8]							
Reset	0x00							
Access Type	Read Only							

S3_IOFFSET

See S1_IOFFSET[15:8] for details.

SENSOR 3 OFFSET CURRENT LSB (0x46)

BIT	7	6	5	4	3	2	1	0
Field	S3_IOFFSET[7:0]							
Reset	0x00							
Access Type	Read Only							

S3_IOFFSET

See S1_IOFFSET[15:8] for details.

SENSOR 4 CONFIGURATION 1 (0x47)

BIT	7	6	5	4	3	2	1	0
Field	S4_WE_AMP_EN	S4_CE_AMP_EN	S4_WE_DAC_MX[1:0]		S4_CE_DAC_MX[1:0]		S4_CP_EN	S4_CHOP_EN
Reset	0b0	0b0	0b00		0b00		0b0	0b0
Access Type	Write, Read	Write, Read	Write, Read		Write, Read		Write, Read	Write, Read

S4_WE_AMP_EN

See S1_WE_AMP_EN for details.

S4_CE_AMP_EN

See S1_CE_AMP_EN for details.

S4_WE_DAC_MX

See S1_WE_DAC_MX[1:0] for details.

S4_CE_DAC_MX

See S1_CE_DAC_MX[1:0] for details.

S4_CP_EN

See S1_CP_EN for details

S4_CHOP_EN

See S1_CHOP_EN for details

SENSOR 4 CONFIGURATION 2 (0x48)

BIT	7	6	5	4	3	2	1	0
Field	S4_SWB	S4_SWA	S4_SC	S4_SRB	S4_SRA	S4_ILIM_EN	S4_RS	S4_SWO
Reset	0b0	0b0	0b0	0b0	0b0	0b00	0b0	0b0
Access Type	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read

S4_SWB

See S1_SWB for details.

S4_SWA

See S1_SWA for details.

S4_SC

See S1_SC for details.

S4_SRB

See S1_SRB for details.

S4_SRA

See S1_SRA for details.

S4_ILIM_EN

See S1_ILIM_EN for details.

S4_RS

See S1_RS for details.

S4_SWO

See S1_SWO for details.

SENSOR 4 CONFIGURATION 3 (0x49)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	S4_IOS_MODE	S4_DETECTOR_EN	S4_DETECTOR_THRESHOLD[1:0]	
Reset	–	–	–	–	0b1	0b0	0b00	
Access Type	–	–	–	–	Write, Read	Write, Read	Write, Read	

S4_IOS_MODE

See S1_IOS_MODE for details.

S4_DETECTOR_EN

See S1_DETECTOR_EN for details.

S4_DETECTOR_THRESHOLD

See S1_DETECTOR_THRESHOLD for details.

SENSOR 4 CONFIGURATION 4 (0x4A)

BIT	7	6	5	4	3	2	1	0
Field	S4_FSR[2:0]			–	–	S4_OFFSET_SEL[2:0]		
Reset	0b000			–	–	0b000		
Access Type	Write, Read			–	–	Write, Read		

S4_FSR

See S1_FSR[2:0] for details.

S4_OFFSET_SEL

See S1_OFFSET_SEL[2:0] for details.

SENSOR 4 CONFIGURATION 5 (0x4B)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	S4_CONV_TIME[3:0]				S4_SELECT
Reset	–	–	–	0x0				0b0
Access Type	–	–	–	Write, Read				Write, Read

S4_CONV_TIME

See S1_CONV_TIME[3:0] for details.

S4_SELECT

See S1_SELECT for details.

SENSOR 4 ALARM LOW SETUP (0x4C)

BIT	7	6	5	4	3	2	1	0
Field	S4_LO_MODE	S4_LO_TRIP	S4_LO_TRIP_CNT[1:0]		S4_LO_DET_CNTR[2:0]			S4_RST_LO_CNTR
Reset	0b0	0b0	0b00		0b000			0b0
Access Type	Write, Read	Write, Read	Write, Read		Read Only			Write, Read

S4_LO_MODE

See S1_LO_MODE for details.

S4_LO_TRIP

See S1_LO_TRIP for details.

S4_LO_TRIP_CNT

See S1_LO_TRIP_CNT[1:0] for details.

S4_LO_DET_CNTR

See S1_LO_DET_CNTR[2:0] for details.

S4_RST_LO_CNTR

See S1_RST_LO_CNTR for details.

SENSOR 4 ALARM HIGH SETUP (0x4D)

BIT	7	6	5	4	3	2	1	0
Field	S4_HI_MODE	S4_HI_TRIP	S4_HI_TRIP_CNT[1:0]		S4_HI_DET_CNTR[2:0]			S4_RST_HI_CNTR
Reset	0b0	0b0	0b00		0b000			0b0
Access Type	Write, Read	Write, Read	Write, Read		Read Only			Write, Read

S4_HI_MODE

See S1_HI_MODE for details.

S4_HI_TRIP

See S1_HI_TRIP for details.

S4_HI_TRIP_CNT

See S1_HI_TRIP_CNT[1:0] for details.

S4_HI_DET_CNTR

See S1_HI_DET_CNTR[2:0] for details.

S4_RST_HI_CNTR

See S1_RST_HI_CNTR for details.

SENSOR 4 ALARM LOW MSB (0x4E)

BIT	7	6	5	4	3	2	1	0
Field	S4_LO_THRESH[15:8]							
Reset	0x00							
Access Type	Write, Read							

S4_LO_THRESH

See S1_LO_THRESH[15:8] for details.

SENSOR 4 ALARM LOW LSB (0x4F)

BIT	7	6	5	4	3	2	1	0
Field	S4_LO_THRESH[7:0]							
Reset	0x00							
Access Type	Write, Read							

S4_LO_THRESH

See S1_LO_THRESH[15:8] for details.

SENSOR 4 ALARM HIGH MSB (0x50)

BIT	7	6	5	4	3	2	1	0
Field	S4_HI_THRESH[15:8]							
Reset	0xFF							
Access Type	Write, Read							

S4_HI_THRESH

See S1_HI_THRESH[15:8] for details.

SENSOR 4 ALARM HIGH LSB (0x51)

BIT	7	6	5	4	3	2	1	0
Field	S4_HI_THRESH[7:0]							
Reset	0xFF							
Access Type	Write, Read							

S4_HI_THRESH

See S1_HI_THRESH[15:8] for details.

SENSOR 4 OFFSET CURRENT MSB (0x52)

BIT	7	6	5	4	3	2	1	0
Field	S4_IOFFSET[15:8]							
Reset	0x00							
Access Type	Read Only							

S4_IOFFSET

See S1_IOFFSET[15:8] for details.

SENSOR 4 OFFSET CURRENT LSB (0x53)

BIT	7	6	5	4	3	2	1	0
Field	S4_IOFFSET[7:0]							
Reset	0x00							
Access Type	Read Only							

S4_IOFFSET

See S1_IOFFSET[15:8] for details.

SYSTEM ADC SETUP (0x54)

BIT	7	6	5	4	3	2	1	0
Field	SYS_AIN_GAIN[1:0]		SYS_PWR_GAIN[1:0]		SYS_SENSV_GAIN[1:0]		OPA_BYPASS_EN	–
Reset	0b01		0b01		0b01		0b0	–
Access Type	Write, Read		Write, Read		Write, Read		Write, Read	–

SYS_AIN_GAIN

SYS_AIN_GAIN[1:0] sets the input voltage gain to the 12-bit system ADC for the AIN1, AIN2, AIN3, and AIN4 external inputs.

See the SYS_AIN_GAIN[1:0] table for the programmable gain values.

SYS_AIN_GAIN[1:0]	AINx (1 = 0 to 4) INPUT GAIN VOLTAGE(V/V)
00	2.0
01	1.0
10	0.5
00	0.25

SYS_PWR_GAIN

The SYS_PWR_GAIN[1:0] bits set the input voltage gain to the 12-bit system ADC for the V_{DD} and GND internal inputs.

See the SYS_PWR_GAIN[1:0] table for the programmable gain values.

SYS_PWR_GAIN[1:0]	SUPPLY INPUT VOLTAGE GAIN (V/V)
00	2.0
01	1.0
10	0.5
00	0.25

SYS_SENSV_GAIN

The SYS_SENSV_GAIN[1:0] bits set the input voltage gain to the 12-bit system ADC for the internal WOn, WEn, REn, and CEn (n = 1 to 4) sensor voltages.

See the SYS_SENSV_GAIN[1:0] table for the programmable gain values.

SYS_SENSV_GAIN[1:0]	SENSOR INPUT VOLTAGE GAIN (V/V)
00	2.0
01	1.0
10	0.5
11	0.25

OPA_BYPASS_EN

OPA_BYPASS_EN = 0: Enables the input voltage buffer. The input signal has a high-z load.

OPA_BYPASS_EN = 1: Bypasses the input voltage buffer (0 - V_{DD} - 0.2V) and the input needs to drive an on-chip 14MΩ resistor.

SYSTEM ADC IN SEL1 (0x55)

BIT	7	6	5	4	3	2	1	0
Field	AIN4_SYS_SEL	AIN3_SYS_SEL	AIN2_SYS_SEL	AIN1_SYS_SEL	VDD_SYS_SEL	GND_SYS_SEL	–	SYS_SELECT
Reset	0b0	0b0	0b0	0b0	0b0	0b0	–	0b0
Access Type	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	–	Write, Read

AIN4_SYS_SEL

AIN4_SYS_SEL = 0: Excludes the AIN4 external analog input from conversions.

AIN4_SYS_SEL = 1: Selects the AIN4 external analog input for conversion sequences for the system ADC.

AIN3_SYS_SEL

AIN3_SYS_SEL = 0: Excludes the AIN3 external analog input from conversions.

AIN3_SYS_SEL = 1: Selects the AIN3 external analog input for conversion sequences for the system ADC.

AIN2_SYS_SEL

AIN2_SYS_SEL = 0: Excludes the AIN2 external analog input from conversions.

AIN2_SYS_SEL = 1: Selects the AIN2 external analog input for conversion sequences for the system ADC.

AIN1_SYS_SEL

AIN1_SYS_SEL = 0: Excludes the AIN1 external analog input from conversions.

AIN1_SYS_SEL = 1: Selects the AIN1 external analog input for conversion sequences for the system ADC.

VDD_SYS_SEL

VDD_SYS_SEL = 0: Excludes the V_{DD} supply voltage from conversions.

VDD_SYS_SEL = 1: Selects the V_{DD} supply voltage for conversion sequences for the system ADC.

GND_SYS_SEL

GND_SYS_SEL = 0: Excludes the GND supply voltage from conversions.

GND_SYS_SEL = 1: Selects the GND supply voltage for conversion sequences for the system ADC.

SYS_SELECT

SYS_SELECT = 0: Excludes the system ADC from voltage conversions.

SYS_SELECT = 1: Includes the system ADC in manual or automatic voltage conversions.

See CONVERT (0x83) description for more information.

SYSTEM ADC IN SEL2 (0x56)

BIT	7	6	5	4	3	2	1	0
Field	S2_WO_SYS_SEL	S2_WE_SYS_SEL	S2_RE_SYS_SEL	S2_CE_SYS_SEL	S1_WO_SYS_SEL	S1_WE_SYS_SEL	S1_RE_SYS_SEL	S1_CE_SYS_SEL
Reset	0b0	0b0	0b0	0b0	0b0	0b0	0b0	0b0
Access Type	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read

S2_WO_SYS_SEL

S2_WO_SYS_SEL = 0: Excludes the WO2 sensor voltage from conversions.

S2_WO_SYS_SEL = 1: Selects the WO2 sensor voltage for conversion sequences for the system ADC.

S2_WE_SYS_SEL

S2_WE_SYS_SEL = 0: Excludes the WE2 sensor voltage from conversions.

S2_WE_SYS_SEL = 1: Selects the WE2 sensor voltage for conversion sequences for the system ADC.

S2_RE_SYS_SEL

S2_RE_SYS_SEL = 0: Excludes the RE2 sensor voltage from conversions.

S2_RE_SYS_SEL = 1: Selects the RE2 sensor voltage for conversion sequences for the system ADC.

S2_CE_SYS_SEL

S2_CE_SYS_SEL = 0: Excludes the CE2 sensor voltage from conversions.

S2_CE_SYS_SEL = 1: Selects the CE2 sensor voltage for conversion sequences for the system ADC.

S1_WO_SYS_SEL

S1_WO_SYS_SEL = 0: Excludes the WO1 sensor voltage from conversions.

S1_WO_SYS_SEL = 1: Selects the WO1 sensor voltage for conversion sequences for the system ADC.

S1_WE_SYS_SEL

S1_WE_SYS_SEL = 0: Excludes the WE1 sensor voltage from conversions.

S1_WE_SYS_SEL = 1: Selects the WE1 sensor voltage for conversion sequences for the system ADC.

S1_RE_SYS_SEL

S1_RE_SYS_SEL = 0: Excludes the RE1 sensor voltage from conversions.

S1_RE_SYS_SEL = 1: Selects the RE1 sensor voltage for conversion sequences for the system ADC.

S1_CE_SYS_SEL

S1_CE_SYS_SEL = 0: Excludes the CE1 sensor voltage from conversions.

S1_CE_SYS_SEL = 1: Selects the CE1 sensor voltage for conversion sequences for the system ADC.

SYSTEM ADC IN SEL3 (0x57)

BIT	7	6	5	4	3	2	1	0
Field	S4_WO_SYS_SEL	S4_WE_SYS_SEL	S4_RE_SYS_SEL	S4_CE_SYS_SEL	S3_WO_SYS_SEL	S3_WE_SYS_SEL	S3_RE_SYS_SEL	S3_CE_SYS_SEL
Reset	0b0	0b0	0b0	0b0	0b0	0b0	0b0	0b0
Access Type	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read

S4_WO_SYS_SEL

S4_WO_SYS_SEL = 0: Excludes the WO4 sensor voltage from conversions.

S4_WO_SYS_SEL = 1: Selects the WO4 sensor voltage for conversion sequences for the system ADC.

S4_WE_SYS_SEL

S4_WE_SYS_SEL = 0: Excludes the WE4 sensor voltage from conversions.

S4_WE_SYS_SEL = 1: Selects the WE4 sensor voltage for conversion sequences for the system ADC.

S4_RE_SYS_SEL

S4_RE_SYS_SEL = 0: Excludes the RE4 sensor voltage from conversions.

S4_RE_SYS_SEL = 1: Selects the RE4 sensor voltage for conversion sequences for the system ADC.

S4_CE_SYS_SEL

S4_CE_SYS_SEL = 0: Excludes the CE4 sensor voltage from conversions.

S4_CE_SYS_SEL = 1: Selects the CE4 sensor voltage for conversion sequences for the system ADC.

S3_WO_SYS_SEL

S3_WO_SYS_SEL = 0: Excludes the WO3 sensor voltage from conversions.

S3_WO_SYS_SEL = 1: Selects the WO3 sensor voltage for conversion sequences for the system ADC.

S3_WE_SYS_SEL

S3_WE_SYS_SEL = 0: Excludes the WE3 sensor voltage from conversions.

S3_WE_SYS_SEL = 1: Selects the WE3 sensor voltage for conversion sequences for the system ADC.

S3_RE_SYS_SEL

S3_RE_SYS_SEL = 0: Excludes the RE3 sensor voltage from conversions.

S3_RE_SYS_SEL = 1: Selects the RE3 sensor voltage for conversion sequences for the system ADC.

S3_CE_SYS_SEL

S3_CE_SYS_SEL = 0: Excludes the CE3 sensor voltage from conversions.

S3_CE_SYS_SEL = 1: Selects the CE3 sensor voltage for conversion sequences for the system ADC.

SYSTEM ADC ALARM LOW SETUP (0x58)

BIT	7	6	5	4	3	2	1	0
Field	–	SYS_LO_TRIP	SYS_LO_TRIP_CNT[1:0]		SYS_LO_DET_CNTR[2:0]			SYS_RST_LO_CNTR
Reset	–	0b0	0b00		0b000			0b0
Access Type	–	Write, Read	Write, Read		Read Only			Write, Read

SYS_LO_TRIP

SYS_LO_TRIP = 0: Programs the alarm low trip type to consecutive. When the trip type is consecutive, the number of trips programmed with SYS_LO_TRIP_COUNT[1:0] need to be consecutive to assert the SYS_ADC_DATA_LO (0x01) status bit.

SYS_LO_TRIP = 1: Programs the alarm low trip type to be nonconsecutive. When the trip type is nonconsecutive, the number of trips programmed with SYS_LO_TRIP_COUNT[1:0] does not need to be consecutive to assert the SYS_ADC_DATA_LO status bit.

SYS_LO_TRIP_CNT

SYS_LO_TRIP_CNT[1:0] programs the number of trip counts required to assert the SYS_ADC_DATA_LO (0x01) status bit.

See the SYS_LO_TRIP_CNT[1:0] table for the programmable system ADC alarm low trip counts.

SYS_LO_TRIP_CNT[1:0]	TRIP COUNT
00	1
01	2
10	3
11	4

SYS_LO_DET_CNTR

SYS_LO_DET_CNTR[2:0] is a read only register that holds the count for the number of times the system ADC data went below the system alarm low threshold after the counter was cleared.

SYS_RST_LO_CNTR

SYS_RST_LO_CNTR is a self clearing bit. When set to 1, it clears the count in SYS_LO_DET_CNTR[2:0] and is cleared itself.

SYSTEM ADC ALARM HIGH SETUP (0x59)

BIT	7	6	5	4	3	2	1	0
Field	–	SYS_HI_TRIP	SYS_HI_TRIP_CNT[1:0]		SYS_HI_DET_CNTR[2:0]			SYS_RST_HI_CNTR
Reset	–	0b0	0b00		0b000			0b0
Access Type	–	Write, Read	Write, Read		Read Only			Write, Read

SYS_HI_TRIP

SYS_HI_TRIP = 0: Programs the alarm high trip type to consecutive. When the trip type is consecutive, the number of trips programmed with SYS_HI_TRIP_COUNT[2:0] need to be consecutive to assert the SYS_ADC_DATA_HI (0x01) status bit.

SYS_HI_TRIP = 1: Programs the alarm high trip type to be nonconsecutive. When the trip type is nonconsecutive, the number of trips programmed with SYS_HI_TRIP_COUNT[1:0] does not need to be consecutive to assert the SYS_ADC_DATA_HI status bit.

SYS_HI_TRIP_CNT

SYS_HI_TRIP_CNT[1:0] programs the number of trip counts required to assert the SYS_ADC_DATA_HI (0x01) status bit.

See the SYS_HI_TRIP_CNT[1:0] table for the programmable system ADC alarm low trip counts.

SYS_HI_TRIP_CNT[1:0]	TRIP COUNT
00	1
01	2
10	3
11	4

SYS_HI_DET_CNTR

SYS_HI_DET_CNTR[2:0] is a read only register that holds the count for the number of times the system ADC data went above the system alarm high threshold after the counter was cleared.

SYS_RST_HI_CNTR

SYS_RST_HI_CNTR is a self clearing bit. When set to 1, it clears the count in SYS_HI_DET_CNTR[2:0] and is cleared itself.

SYSTEM ADC ALARM LOW MSB (0x5A)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	SYS_LO_THRESH[11:8]			
Reset	–	–	–	–	0x0			
Access Type	–	–	–	–	Write, Read			

SYS_LO_THRESH

SYS_LO_THRESH[11:8] contains the most significant 4 bits of the system ADC alarm low threshold register, SYS_LO_THRESH[11:0]. The lower 7 bits are in the SYS_LO_THRESH[7:0] register.

SYS_LO_THRESH[11:0] sets the alarm low threshold to compare with the system ADC results.

SYS_LO_THRESH[11:0] = 0x000: Disables the alarm.

SYSTEM ADC ALARM LOW LSB (0x5B)

BIT	7	6	5	4	3	2	1	0
Field	SYS_LO_THRESH[7:0]							
Reset	0x00							
Access Type	Write, Read							

SYS_LO_THRESH

SYS_LO_THRESH[7:0] contains the lower 7 bits of the system ADC alarm low threshold register, SYS_LO_THRESH[11:0]. The most significant 4 bits are in the SYS_LO_THRESH[11:8] register.

See SYS_LO_THRESH[11:8] for more details.

SYSTEM ADC ALARM HIGH MSB (0x5C)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	SYS_HI_THRESH[11:8]			
Reset	–	–	–	–	0xF			
Access Type	–	–	–	–	Write, Read			

SYS_HI_THRESH

SYS_HI_THRESH[11:8] contains the most significant 4 bits of the system ADC alarm high threshold register, SYS_HI_THRESH[11:0]. The lower 7 bits are in the SYS_HI_THRESH[7:0] register.

SYS_HI_THRESH[11:0] sets the alarm high threshold to compare with the system ADC results.

SYS_HI_THRESH[11:0] = 0xFFF: Disables the alarm.

SYSTEM ADC ALARM HIGH LSB (0x5D)

BIT	7	6	5	4	3	2	1	0
Field	SYS_HI_THRESH[7:0]							
Reset	0xFF							
Access Type	Write, Read							

SYS_HI_THRESH

SYS_HI_THRESH[7:0] contains the lower 7 bits of the system ADC alarm high threshold register, SYS_HI_THRESH[11:0]. The most significant 4 bits are in the SYS_HI_THRESH[11:8] register.

See SYS_HI_THRESH[11:8] for more details.

SYSTEM OFFSET VOLTAGE MSB (0x5E)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	SYS_VOFFSET[11:8]			
Reset	–	–	–	–	0x0			
Access Type	–	–	–	–	Read Only			

SYS_VOFFSET

SYS_VOFFSET[11:8] contains the most significant 4 bits of the SYS_VOFFSET[11:0] which is the offset voltage for the system ADC. SYS_VOFFSET[7:0] contains the lower byte of SYS_VOFFSET[11:0].

SYSTEM OFFSET VOLTAGE LSB (0x5F)

BIT	7	6	5	4	3	2	1	0
Field	SYS_VOFFSET[7:0]							
Reset	0x00							
Access Type	Read Only							

SYS_VOFFSET

SYS_VOFFSET[7:0] contains the lower 7 bits of the SYS_VOFFSET[11:0] which is the offset voltage for the system ADC. SYS_VOFFSET[11:8] contains most significant 4 byte of SYS_VOFFSET[11:0].

TEMPERATURE CONFIGURATION (0x60)

BIT	7	6	5	4	3	2	1	0
Field	RESERVED[1:0]		–	–	–	–	–	TEMP_SELECT
Reset	0b00		–	–	–	–	–	0b0
Access Type	Write, Read		–	–	–	–	–	Write, Read

RESERVED

These bits are reserved for future use. When writing to this register these bits must always be set to 0b11.

TEMP_SELECT

TEMP_SELECT = 0: Excludes the temperature sensor from data conversions.

TEMP_SELECT = 1: Includes the temperature sensor in manual or automatic temperature conversions. Typical conversion time for a temperature measurement is 15ms.

See the CONVERT (0x83) description for more information.

TEMP ALARM LOW SETUP (0x61)

BIT	7	6	5	4	3	2	1	0
Field	–	TEMP_LO_TRIP	TEMP_LO_TRIP_CNT[1:0]		TEMP_LO_DET_CNTR[2:0]			TEMP_RST_LO_CNTR
Reset	–	0b0	0b00		0b000			0b0
Access Type	–	Write, Read	Write, Read		Read Only			Write, Read

TEMP_LO_TRIP

TEMP_LO_TRIP = 0: Programs the alarm low trip type to consecutive. When the trip type is consecutive, the number of trips programmed with TEMP_LO_TRIP_CNT[1:0] needs to be consecutive to assert the TEMP_DATA_LO (0x01) status bit.

TEMP_LO_TRIP = 1: Programs the alarm low trip type to be nonconsecutive. When the trip type is nonconsecutive, the number of trips programmed with TEMP_LO_TRIP_CNT[1:0] does not need to be consecutive to assert the

TEMP_DATA_LO status bit.

TEMP_LO_TRIP_CNT

TEMP_LO_TRIP_CNT[1:0] programs the number of trip counts required to assert the TEMP_DATA_LO (0x01) status bit.

See the TEMP_LO_TRIP_CNT[1:0] table for the programmable temperature sensor alarm low trip counts.

TEMP_LO_TRIP_CNT[1:0]	TRIP COUNT
00	1
01	2
10	3
11	4

TEMP_LO_DET_CNTR

TEMP_LO_DET_CNTR[2:0] is a read only register that holds the count for the number of times the temperature sensor ADC data went below the temperature alarm low threshold after the counter was cleared.

TEMP_RST_LO_CNTR

TEMP_RST_LO_CNTR is a self clearing bit. When set to 1, it clears the count in TEMP_LO_TRIP_CNT[1:0] and is cleared itself.

TEMP ALARM HIGH SETUP (0x62)

BIT	7	6	5	4	3	2	1	0
Field	–	TEMP_HI_TRIP	TEMP_HI_TRIP_CNT[1:0]		TEMP_HI_DET_CNTR[2:0]			TEMP_RST_HI_CNTR
Reset	–	0b0	0b00		0b000			0b0
Access Type	–	Write, Read	Write, Read		Read Only			Write, Read

TEMP_HI_TRIP

TEMP_HI_TRIP = 0: Programs the alarm high trip type to consecutive. When the trip type is consecutive, the number of trips programmed with the TEMP_HI_TRIP_CNT[1:0] needs to be consecutive to assert the TEMP_DATA_HI (0x01) status bit.

TEMP_HI_TRIP = 1: Programs the alarm high trip type to be nonconsecutive. When the trip type is nonconsecutive, the number of trips programmed with TEMP_HI_TRIP_CNT[1:0] does not need to be consecutive to assert the TEMP_DATA_HI status bit.

TEMP_HI_TRIP_CNT

The TEMP_HI_TRIP_CNT[1:0] bits program the number of trip counts required to assert the TEMP_DATA_HI status bit.

See the TEMP_HI_TRIP_CNT[1:0] table for the programmable temperature sensor alarm low trip counts.

TEMP_HI_TRIP_CNT[1:0]	TRIP COUNT
00	1
01	2
10	3
11	4

TEMP_HI_DET_CNTR

TEMP_HI_DET_CNTR[2:0] is a read only register which holds the count for the number of times the temperature sensor ADC data went above the temperature alarm high threshold after the counter was cleared.

TEMP_RST_HI_CNTR

TEMP_RST_HI_CNTR is a self clearing bit. When set to 1, it clears the count in TEMP_HI_DET_CNTR[3:0] and is cleared itself.

TEMP ALARM LOW MSB (0x63)

BIT	7	6	5	4	3	2	1	0
Field	TEMP_LO_THRESH[15:8]							
Reset	0x80							
Access Type	Write, Read							

TEMP_LO_THRESH

TEMP_LO_THRESH[15:8] contains the upper byte of the temperature sensor ADC alarm low threshold register, TEMP_LO_THRESH[15:0]. The lower byte is in the TEMP_LO_THRESH[7:0] register.

The TEMP_LO_THRESH[15:0] bits set the alarm low threshold to compare with the temperature sensor ADC results.

TEMP_LO_THRESH[15:0] = 0x8000: Disables the alarm and clears the alarm low trip count to zero. The TEMP_DATA_LO (0x01) status bit is asserted when the temperature sensor ADC result is less than the alarm low threshold if the number of trip counts have been reached. For temperature sensor results less than 16-bits, the data is left justified when compared against the alarm low threshold.

TEMP ALARM LOW LSB (0x64)

BIT	7	6	5	4	3	2	1	0
Field	TEMP_LO_THRESH[7:0]							
Reset	0x00							
Access Type	Write, Read							

TEMP_LO_THRESH

TEMP_LO_THRESH[7:0] contains the lower byte of the temperature sensor ADC alarm low threshold register, TEMP_LO_THRESH[15:0]. The upper byte is in the TEMP_LO_THRESH[15:8] register.

See TEMP_LO_THRESH[15:8] for more details.

TEMP ALARM HIGH MSB (0x65)

BIT	7	6	5	4	3	2	1	0
Field	TEMP_HI_THRESH[15:8]							
Reset	0x7F							
Access Type	Write, Read							

TEMP_HI_THRESH

TEMP_HI_THRESH[15:8] contains the upper byte of the temperature sensor ADC alarm high threshold register, TEMP_HI_THRESH[15:0]. The lower byte is in the TEMP_HI_THRESH[7:0] register.

The TEMP_HI_THRESH[15:0] bits set the alarm high threshold to compare with the temperature sensor ADC results.

TEMP_HI_THRESH[15:0] = 0x7FFF: Disables the alarm and clears the alarm high trip count to zero. The TEMP_DATA_HI (0x01) status bit asserts when the temperature sensor ADC result is greater than the alarm high threshold if the number of trip counts have been reached. For temperature sensor results less than 16-bits, the data is left justified when compared against the alarm high threshold.

TEMP ALARM HIGH LSB (0x66)

BIT	7	6	5	4	3	2	1	0
Field	TEMP_HI_THRESH[7:0]							
Reset	0xFF							
Access Type	Write, Read							

TEMP_HI_THRESH

TEMP_HI_THRESH[7:0] contains the lower byte of the temperature sensor ADC alarm high threshold register, TEMP_HI_THRESH[15:0]. The upper byte is in the TEMP_HI_THRESH[15:8] register.

See TEMP_HI_THRESH[15:8] for more details.

REFERENCE CONTROL (0x68)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	REF_MODE	REF_VAL[1:0]		REF_EN
Reset	–	–	–	–	0b0	0b00		0b0
Access Type	–	–	–	–	Write, Read	Write, Read		Write, Read

REF_MODE

REF_MODE = 0: Selects the internal voltage reference (V_{REF}) as the DAC and the system ADC voltage reference.

REF_MODE = 1: Uses an external voltage reference as the DAC and the system ADC voltage reference.

REF_VAL

REF_VAL[1:0] programs the internal voltage reference (V_{REF}) used by the DACs and system ADCs. V_{DD} must be at least 150mV greater than the selected V_{REF} voltage.

REF_VAL[1:0]	VOLTAGE REFERENCE OUTPUT (V_{REF})
00	1.536
01	2.048
10	3.072
11	4.096

REF_EN

REF_EN = 0: Powers down the internal voltage reference (V_{REF}) to minimize power consumption in sensor detection mode.

REF_EN = 1: Enables V_{REF} as the DAC and ADC voltage reference in normal operation modes such as sensor DC bias mode, and DC measurement mode.

DACA MSB CODE (0x69)

BIT	7	6	5	4	3	2	1	0
Field	DACA_CODE[11:4]							
Reset	0x00							
Access Type	Write, Read							

DACA_CODE

(m = A, B, C, D for the four DACs)

DACm_CODE[11:4] contains the upper 8 bits of the DACm_CODE[11:0] register. The lower 4 bits are in DACm_CODE[3:0] register.

The DACm_CODE[11:0] sets the output voltage of the DACm. The output voltage $V_{DACm} = V_{REF} \times$ DACm_CODE[11:0] / 4096.

When SENS_CONV_TYPE (0x80) = 1 for AC conversions, the DACm_CODE[11:0] can be a minimum of 660 codes or 250mV.

DACA EN LSB CODE (0x6A)

BIT	7	6	5	4	3	2	1	0
Field	DACA_CODE[3:0]				–	–	–	DACA_EN
Reset	0x0				–	–	–	0b0
Access Type	Write, Read				–	–	–	Write, Read

DACA_CODE

(m = A, B, C, D for the four DACs)

DACm_CODE[3:0] contains the lower 4 bits of the DACm_CODE[11:0] register. The upper 8 bits are in DACm_CODE[11:4] register.

See DACA_CODE[11:4] for details.

DACA_EN

DACA_EN = 0: Powers down DACA.

DACA_EN = 1: Powers up DACA.

DACB MSB CODE (0x6B)

BIT	7	6	5	4	3	2	1	0
Field	DACB_CODE[11:4]							
Reset	0x00							
Access Type	Write, Read							

DACB_CODE

See DACA_CODE[11:4] for details.

DACB EN LSB CODE (0x6C)

BIT	7	6	5	4	3	2	1	0
Field	DACB_CODE[3:0]				–	–	–	DACB_EN
Reset	0x0				–	–	–	0b0
Access Type	Write, Read				–	–	–	Write, Read

DACB_CODE

See DACA_CODE[11:4] for details.

DACB_EN

DACB_EN = 0: Powers down DACB.

DACB_EN = 1: Powers up DACB.

DACC MSB CODE (0x6D)

BIT	7	6	5	4	3	2	1	0
Field	DACC_CODE[11:4]							
Reset	0x00							
Access Type	Write, Read							

DACC_CODE

See DACA_CODE[11:4] for details.

DACC EN LSB CODE (0x6E)

BIT	7	6	5	4	3	2	1	0
Field	DACC_CODE[3:0]				–	–	–	DACC_EN
Reset	0x0				–	–	–	0b0
Access Type	Write, Read				–	–	–	Write, Read

DACC_CODE

See DACA_CODE[11:4] for details.

DACC_EN

DACC is only available in the 2-channel and 4-channel versions.

DACC_EN = 0: Powers down DACC.

DACC_EN = 1: Powers up DACC.

DACD MSB CODE (0x6F)

BIT	7	6	5	4	3	2	1	0
Field	DACD_CODE[11:4]							
Reset	0x00							
Access Type	Write, Read							

DACD_CODE

See DACA_CODE[11:4] for details.

DACD EN LSB CODE (0x70)

BIT	7	6	5	4	3	2	1	0
Field	DACD_CODE[3:0]				–	–	–	DACD_EN
Reset	0x0				–	–	–	0b0
Access Type	Write, Read				–	–	–	Write, Read

DACD_CODE

See DACA_CODE[11:4] for details.

DACD_EN

DACD is only available in the 2-channel and 4-channel versions.

DACD_EN = 0: Powers down DACD.

DACD_EN = 1: Powers up DACD.

FAST_FREQ_TRIM_ADJ (0x75)

BIT	7	6	5	4	3	2	1	0
Field	FAST_TRIM_ADJ[7:0]							
Reset	0x00							
Access Type	Write, Read, Dual							

FAST_TRIM_ADJ

FAST_TRIM_ADJ[7:0] adjusts the fast oscillator frequency away from its nominal trim. It is a signed, 8-bit number where 0 has no change in the fast oscillator frequency. EIS mode allows up to 16 fine frequencies.

The fast oscillator FAST_TRIM_ADJ[7:0] calibration value for each of the 15 nonzero EIS_FINE_FREQ[3:0] settings is found by setting EIS_FINE_FREQ[3:0] to the desired fine frequency value and then setting EIS_FREQ_TRIM_CAL (0x78) to 1 to initiate a calibration. When trim calibration completes, the trim value corresponding to the EIS_FINE_FREQ[3:0] setting is stored in FAST_TRIM_ADJ[7:0].

To avoid future calibrations, FAST_TRIM_ADJ[7:0] can be written with the correct code associated with each nonzero EIS_FINE_FREQ[3:0] setting (15 of them). FAST_TRIM_ADJ[7:0] is used for synthesized EIS frequencies above 110Hz.

SLOW_FREQ_TRIM_ADJ (0x76)

BIT	7	6	5	4	3	2	1	0
Field	SLOW_TRIM_ADJ[7:0]							
Reset	0x00							
Access Type	Write, Read, Dual							

SLOW_TRIM_ADJ

The SLOW_TRIM_ADJ[7:0] register adjusts the slow oscillator frequency away from its nominal trim. It is a signed, 8-bit number where 0 has no change in the slow oscillator frequency. EIS mode allows up to 16 fine frequencies.

The slow oscillator SLOW_TRIM_ADJ[7:0] calibration value for each of the 15 non-zero EIS_FINE_FREQ[3:0] settings is found by setting EIS_FINE_FREQ[3:0] to the desired fine frequency value and then setting EIS_FREQ_TRIM_CAL to 1 to initiate a calibration. When trim calibration completes, the trim value corresponding to the EIS_FINE_FREQ[3:0] setting is stored in SLOW_TRIM_ADJ[7:0].

To avoid future calibrations, SLOW_TRIM_ADJ[7:0] can be written with the correct code associated with each non-zero EIS_FINE_FREQ[3:0] setting. SLOW_TRIM_ADJ[7:0] is used for synthesized EIS frequencies below 110Hz.

EIS CAL RES VAR (0x77)

BIT	7	6	5	4	3	2	1	0
Field	EIS_CAL_RES_VARIATION[7:0]							
Reset								
Access Type	Read Only							

EIS_CAL_RES_VARIATION

EIS_CAL_RES_VARIATION[7:0] is a read-only register that holds the variation of Actual_Resistance from Ideal_Resistance of the three EIS calibration resistors and the 150Ω EIS WEn series resistor. This device-to-device variation is caused by process variations. The actual resistor values with respect to their ideal resistance is calculated using the formula:

Actual_Resistance = Ideal_Resistance x (1+ EIS_CAL_RES_VARIATION[7:0] x 0.0025)

EIS_CAL_RES_VARIATION[7:0] is a 2's complement representation, e.g., 255 is equivalent to -1. The EIS_CAL_RES_VARIATION[7:0] is determined at the factory using the 13.19kΩ EIS calibration resistor.

EIS_CAL_RES_VARIATION[7:0]	RESISTOR SCALE FACTOR (%)	EIS_CAL_RES_VARIATION[7:0]	RESISTOR SCALE FACTOR (%)
0000 0000	100	1000 0000	68
0000 0001	100.25	1000 0001	68.25
0000 0010	100.5	1000 0010	68.5
0000 0011	100.75	1000 0011	68.75
…		…	
….		….	

0111 1101	131.25	1111 1101	99.25
0111 1110	131.5	1111 1110	99.5
0111 1111	131.75	1111 1111	99.75

EIS SETUP 1 (0x78)

BIT	7	6	5	4	3	2	1	0
Field	EIS_DAC_SEL[1:0]		EIS_NUM_SINEWAVES[2:0]			–	EIS_FREQ_TRIM_CAL	EIS_PH_ADV_CAL
Reset	0b00		0b000			–	0b0	0b0
Access Type	Write, Read		Write, Read			–	Write, Read	Write, Read

EIS_DAC_SEL

EIS_DAC_SEL[1:0] selects the DAC to be used for the DC offset of the AC sine-wave output in EIS mode and the DC offset of the square-wave output in SWV mode and the stair step profile in CV mode.

See the EIS_DAC_SEL[1:0] table for the DAC selection.

EIS_DAC_SEL[1:0]	EIS DAC SELECTION
00	DACA is selected for DC offset
01	DACB is selected for DC offset
10	DACC is selected for DC offset
11	DACD is selected for DC offset

EIS_NUM_SINEWAVES

EIS_NUM_SINEWAVES[2:0] sets the number of sine-wave cycles used in an EIS measurement. The ADC counts are averaged over the number of cycles selected. Increasing the number of sine-wave cycles generally improves the signal-to-noise ratio and interference rejection of the EIS measurement, which improves the measurement accuracy.

EIS_NUM_SINEWAVES[2:0]	# Cycles Averaged
000	1
001	2
010	4
011	8
100	16
101	32
110	64
111	128

EIS_FREQ_TRIM_CAL

Setting the EIS_FREQ_TRIM_CAL bit to 1 initiates fine-frequency trim calibration. When EIS_CLK_DIV[4:0] (0x7A) is programmed for less than 110Hz, the slow oscillator is calibrated using the fast oscillator. When EIS_CLK_DIV[4:0] is programmed for greater than 110Hz, the fast oscillator is calibrated using the slow oscillator.

When the calibration completes, EIS_CAL_DONE (0x00) is set to 1, EIS_FREQ_TRIM_CAL is cleared and the frequency trim value is stored in EIS_FAST_TRIM_ADJ[7:0] (0x75) or SLOW_TRIM_ADJ[7:0] (0x76) depending on the EIS_CLK_DIV[4:0] (0x7A) setting. Because the fine frequency calibration uses the FIFO, it is always necessary to clear the FIFO after the calibration.

The calibrated frequency trim values can be read using FAST_TRIM_ADJ[7:0] and SLOW_TRIM_ADJ[7:0]. When EIS_CLK_DIV[4:0] is programmed for greater than 110Hz, SLOW_TRIM_ADJ[7:0] = 0. When EIS_CLK_DIV is programmed for less than 110Hz, FAST_TRIM_ADJ[7:0] (0x75) = 0. Writing any other value to FAST_TRIM_ADJ[7:0] and SLOW_TRIM_ADJ[7:0] overrides the calibrated values.

Writing 0x0 to EIS_FINE_FREQ[3:0] sets both FAST_TRIM_ADJ[7:0] and SLOW_TRIM_ADJ[7:0] to zero. Writing any other value to FAST_TRIM_ADJ[7:0] and SLOW_TRIM_ADJ[7:0] overrides this.

FAST_TRIM_ADJ[7:0] and SLOW_TRIM_ADJ[7:0] are used only during EIS mode conversions and calibrations. In other modes, these are ignored.

During fine-frequency trim calibrations, all ADC conversions should be disabled.

See EIS_FINE_FREQ[3:0] (0x7F) and the Fine Frequency Extension and Calibration section for additional information.

EIS_PH_ADV_CAL

Setting EIS_PH_ADV_CAL to 1 puts EIS AFE in phase calibration mode, and the device calibrates the phase advance at the frequency set by EIS_CLK_DIV[4:0] (0x7A) and EIS_FINE_FREQ[3:0]. The result is stored in EIS_PHASE_ADVANCE (0x7E).

During an EIS phase calibration, the WEn, CEn, and REn pins are disconnected from the EIS circuity. Both EIS amplifiers are enabled, and an internal resistor is connected between the amplifier outputs. The resistance is selected by EIS_CAL_RES[1:0] (0x7C). The exact value of the resistance can be calculated using the variation value in EIS_CAL_RES_VARIATION[7:0] (0x77), but the phase calibration is independent of the internal load resistor value.

When the calibration completes, the EIS_CAL_DONE status bit (0x00) is set to 1, EIS_PH_ADV_CAL is cleared, and the calibrated phase advance value is stored in EIS_PHASE_ADVANCE[7:0] (0x7E). Because the EIS phase advance calibration uses the FIFO, it is always necessary to clear the FIFO after the calibration.

During EIS phase calibration, all DC AFE sensor outputs are unchanged and remain valid at the device output pins.

For more details, see the Calibrating the Phase Advance section.

EIS SETUP 2 (0x79)

BIT	7	6	5	4	3	2	1	0
Field	EIS_AMPLITUDE[3:0]				–	–	–	–
Reset	0x0				–	–	–	–
Access Type	Write, Read				–	–	–	–

EIS_AMPLITUDE

EIS_AMPLITUDE[3:0] programs the amplitude of the sine-wave output by the EIS DAC. The sine wave sits on top of the DC value programmed by the DAC register selected by EIS_DAC_SEL (0x78).

See the EIS_AMPLITUDE[3:0] table for the available amplitudes.

EIS_AMPLITUDE[3:0]	EIS OUTPUT AMPLITUDE (mV_{P-P} or mV around DAC value)
0x0	5 or ±2.5

0x1	10 or ±5
0x2	15 or ±7.5
0x3	20 or ±10
0x4	25 or ±12.5
0x5	30 or ±15
0x6	35 or ±17.5
0x7	40 or ±20
0x8	45 or ±22.5
0x9	50 or ±25
0xA	55 or ±27.5
0xB	60 or ±30
0xC	65 or ±32.5
0xD	70 or ±35
0xE	75 or ±37.5
0xF	80 or ±40

EIS CLOCK SETUP (0x7A)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	EIS_CLK_DIV[4:0]				
Reset	–	–	–	0b00000				
Access Type	–	–	–	Write, Read, Dual				

EIS_CLK_DIV

In EIS AC conversion mode, EIS_CLK_DIV[1:0] is used in conjunction with EIS_FINE_FREQ[3:0] (0x7F) to set the EIS sine-wave frequency. In CV or SWV mode, it is used to set the step period of the CV or SWV waveform. EIS, CV, and SWV modes are set by AC_MODE[1:0] (0xA0).

See the EIS_CLK_DIV[4:0] (EIS Mode) table for available EIS clock divider settings. Note that the gain changes for the higher frequencies require some adjustment when higher frequencies are used.

In EIS Mode, EIS_CLK_DIV[4:0] and EIS_FINE_FREQ[3:0] (0x07F) program the synthesizer frequency for the EIS AC DAC. The synthesizer uses 256 samples per cycle to generate the EIS DAC sine-wave signal for all frequencies.

When AC_MODE[1:0] (0xA0) is programmed to 00, and if EIS_CLK_DIV[4:0] is less than 0x0B, the EIS ADC conversions are done in continuous mode, and the device uses the Fast Clock for sine-wave generation and ADC conversions.

When AC_MODE[1:0] is programmed to 00, and if EIS_CLK_DIV[4:0] is greater than 0x0A, the EIS ADC conversions are done in incremental mode, and the device uses the slow clock for a sine-wave generation. The fast clock is enabled only during ADC conversions.

Incremental mode is used for low-power operation for slow EIS sine-wave frequencies and is supported only if the on-chip slow oscillator is used. It is not supported if external fast or slow clocks are used.

When AC_MODE[1:0] = 01 or 10 (CV or SWV Modes), EIS_CLK_DIV[3:0] programs the staircase step time period used to generate the waveforms. See EIS_CLK_DIV[4:0] (CV and SWV Mode) for available step periods. EIS_CLK_DIV[4:0] is limited to the codes in the range 0x07 to 0x0E for EIS_INTEG = 0, and 0x08 to 0x0E for EIS_INTEG = 1.

EIS_CLK_DIV[4:0]	EIS SINEWAVE (Hz)	GAIN CIC3	FILTER DELAY	BW (Hz) 1 cycle
0x3	20,000	0.7298	18.8µs	40,000

0x4	10,000	0.8332	31.3µs	20,000
0x5	5,000	0.8831	43.8µs	10,000
0x6	2,500	0.8960	68.8µs	5,000
0x7	1,250	0.8992	119µs	2,500
0x8	625	0.9000	219µs	1,250
0x9	312.5	0.9002	419µs	625
0xA	156.25	0.9003	819µs	312.5
0xB	80.000	1.0000	1.61ms	5,250
0xC	40.000	1.0000	3.21ms	5,250
0xD	20.000	1.0000	6.41ms	5,250
0xE	10.000	1.0000	12.8ms	5,250
0xF	5.0000	1.0000	25.6ms	5,250
0x10	2.5000	1.0000	51.2ms	5,250
0x11	1.2500	1.0000	102ms	5,250
0x12	0.6250	1.0000	205ms	5,250
0x13	0.3125	1.0000	410ms	5,250
0x14	0.15625	1.0000	819ms	5,250
0x15	0.078125	1.0000	1.64s	5,250
0x16	0.0390625	1.0000	3.28s	5,250
0x17	0.0195313	1.0000	6.55s	5,250

EIS_CLK_DIV[4:0]	CV AND SWV STEP PERIOD (ms)
0x07	0.8
0x08	1.6
0x09	3.2
0x0A	6.4

EIS AFE 1 (0x7B)

BIT	7	6	5	4	3	2	1	0
Field	EIS_WE_AMP_EN	EIS_CE_AMP_EN	EIS_SC	EIS_SRB	EIS_RC[1:0]		EIS_DRV	–
Reset	0b0	0b0	0b0	0b0	0b00		0b0	–
Access Type	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read		Write, Read	–

EIS_WE_AMP_EN

EIS_WE_AMP_EN = 0: Powers down the EIS working amplifier.

EIS_WE_AMP_EN = 1: Powers up the EIS working amplifier.

EIS_CE_AMP_EN

EIS_CE_AMP_EN = 0: Powers down the EIS counter amplifier.

EIS_CE_AMP_EN = 1: Powers up the EIS counter amplifier.

EIS_SC

EIS_SC = 0: Opens the analog switch between the EIS counter amplifier inverting input and the CE pin.

EIS_SC = 1: Closes the analog switch between the EIS counter amplifier inverting input and the CE pin. Closing the analog switch configures the EIS counter amplifier as a unity gain follower.

See S1_SWB for common sensor switch configurations.

EIS_SRB

EIS_SRB = 0: Opens the analog switch between the EIS counter amplifier inverting input and the RE pin.

EIS_SRB = 1: Closes the analog switch between the EIS counter amplifier inverting input and the RE pin.

See S1_SWB for common sensor switch configurations.

EIS_RC

EIS_RC[1:0] sets the location of zero in the EIS amplifier. The zero can be used to cancel out the output pole to keep the amplifier stable. The pole location can be calculated as 1.33 x I / C, where C is the effective load capacitance that is not zeroed out by a series resistor at high frequency, and I is the AFE bias current. The AFE bias current is set by EIS_ADC_FS_RANGE[1:0] (0x7D). Match the zero frequency with the pole frequency. If the amplifier oscillates, reduce the zero frequency.

EIS_RC[1:0]	ZERO FREQUENCY
00	10MHz
01	1.3MHz
10	1.3MHz to 150kHz (tracks output current)
11	N/A

EIS_DRV

EIS_DRV selects whether the EIS stimulus is driven by the working amplifier or the counter amplifier. Driving from the counter amplifier can improve the phase accuracy when the load impedance is high.

See the EIS_DRV table for EIS drive selection.

EIS_DRV	DESCRIPTION
0	Drive from working amplifier
1	Drive from counter amplifier

EIS AFE 2 (0x7C)

BIT	7	6	5	4	3	2	1	0
Field	EIS_RS	EIS_OFFSET[2:0]			EIS_ILIM_EN	EIS_I_CAL_EN	EIS_CAL_RES[1:0]	
Reset	0b0	0b000			0b0	0b0	0b00	
Access Type	Write, Read	Write, Read			Write, Read	Write, Read	Write, Read	

EIS_RS

EIS_RS = 0: 0Ω resistor in series with the WEn pins.

EIS_RS = 1: 150Ω resistor in series with the WEn pins.

Adding the 150Ω resistor helps improve amplifier stability. The resistor is subject to process variations. See the EIS_CAL_RES_VARIATION[7:0] (0x77) for determining the actual resistance.

EIS_OFFSET

EIS_OFFSET[2:0] sets the EIS ADC offset current. Increases the EIS ADC offset in case of a low DC current in the sensor. The nominal offset is 50% of the ADC full-scale range. See the EIS_OFFSET[2:0] table for the offset settings as a factor of full-scale range.

EIS_OFFSET[2:0]	EIS DC OFFSET
000	0.5 x ADC FSR
001	0.4375 x ADC FSR
010	0.375 x ADC FSR
011	0.3125 x ADC FSR
100	0.250 x ADC FSR
101	0.1875 x ADC FSR
110	0.125 x ADC FSR
111	N/A

EIS_ILIM_EN

EIS_ILIM_EN = 0: Disables the current limiter on WEn pin.

EIS_ILIM_EN = 1: Enables the current limiter on WEn pin during EIS measurement.

Current limit changes with EIS_ADC_FS_RANGE[1:0] settings as shown in the EIS_ADC_FS_RANGE[1:0] table.

EIS_ADC_FS_RANGE[1:0]	WE SOURCING CURRENT LIMIT (µA)	WE SINKING CURRENT LIMIT (µA)
00	6.9	3
01	12.6	6
10	27.5	15
11	48.5	30

EIS_I_CAL_EN

EIS_I_CAL_EN = 0: Enables normal mode and drive the external impedance.

EIS_I_CAL_EN = 1: Puts the EIS AFE in calibration mode and drives an internal calibration resistor selected by EIS_CAL_RES[1:0].

EIS_CAL_RES

EIS_CAL_RES[1:0] sets the internal calibration resistance used to calibrate the non-ideal gain error due to different EIS_ADC_FS_RANGE[1:0] (0x7D) settings. Resistance values are listed in the EIS_CAL_RES[1:0] table. EIS_ADC_FS_RANGE[1:0] is trimmed at 20µA, and the rest of the full-scale ranges are not trimmed. In order to calibrate the non-ideal gain error due to the other non trimmed full-scale ranges, EIS_CAL_RES[1:0] should be used as follows:

First, select EIS_CAL_RES[1:0] setting of 6.6kΩ, EIS_AMPLITUDE[3:0] (0x79) of 40mV, and EIS_ADC_FS_RANGE[1:0] of 10µA; make the EIS measurement; read the ADC count (n counts) from the FIFO. Then keep the same EIS_CAL_RES[1:0] setting of 6.6kΩ but select EIS_ADC_FS_RANGE[1:0] of 20µA; make the EIS measurement; read the ADC count (m counts) from the FIFO. The ratio of n/m is the true gain between 20µA and 10µA

EIS_ADC_FS_RANGE[1:0]. (ideally, the ratio is 2 in this example).

EIS_CAL_RES[1:0]	CALIBRATION RESISTANCE (kΩ)
00	N/A
01	26.39
10	13.19
11	6.597

EIS ADC FS RANGE (0x7D)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	–	–	EIS_ADC_FS_RANGE[1:0]	
Reset	–	–	–	–	–	–	0b00	
Access Type	–	–	–	–	–	–	Write, Read	

EIS_ADC_FS_RANGE

EIS_ADC_FS_RANGE[1:0] sets the full scale range of the EIS ADC current measurement. Setting are shown in the EIS_ADC_FS_RANGE[1:0] table.

EIS_ADC_FS_RANGE[1:0]	FULL SCALE CURRENT RANGE (μA)
00	4
01	8
10	20
11	40

PHASE_ADVANCE (0x7E)

BIT	7	6	5	4	3	2	1	0
Field	EIS_PHASE_ADVANCE[7:0]							
Reset	0x00							
Access Type	Write, Read, Dual							

EIS_PHASE_ADVANCE

EIS_PHASE_ADVANCE[7:0] sets the phase advance of the sine wave from the EIS DAC. Each LSB (0 to 255) advances the phase by 360 / 256 = ~1.4 degrees. Since sine waves are circular, an advance of 255 LSB is equivalent to a delay of 1 LSB. This allows the EIS_PHASE_ADVANCE[7:0] to be treated as 2's complement code. Code 128 (-128) is equivalent to a delay of 180 degrees, and code 255 (-1) is a delay of 1.4 degrees.

If phase calibration is done using EIS_PH_ADV_CAL (0x78), EIS_PHASE_ADVANCE[7:0] contains the calibrated value upon phase calibration completion. A subsequent write to EIS_PHASE_ADVANCE[7:0] overrides the calibrated value.

EIS SETUP 3 (0x7F)

BIT	7	6	5	4	3	2	1	0
Field	EIS_SETTLE[3:0]				EIS_FINE_FREQ[3:0]			
Reset	0x0				0x0			
Access Type	Write, Read				Write, Read			

EIS_SETTLE

EIS_SETTLE[3:0] sets the number of sine-wave cycles generated at the beginning of an EIS AC measurement before the EIS ADC begins averaging data.

Valid numbers are 0x0 to 0xF, corresponding to 0 to 15 sine-wave cycles.

EIS_FINE_FREQ

EIS_FINE_FREQ[3:0] is used when AC_MODE[1:0] (0x00) = 00 (EIS Mode). The EIS_FINE_FREQ[3:0] bits adjust the synthesis frequencies above and below the coarse frequencies, stepping upward half an octave in 7 steps and downward in 8 steps. A coarse frequency step is one octave (factor of 2) relative to adjacent coarse frequencies and set by EIS_CLK_DIV[4:0] (0x7A).

The synthesis frequency is given by $f_{SYNTH} = 160{,}000 \times 2^{-COARSECODE} \times 2^{(FINECODE / 16)}$(Hz) for Coarse Codes 3 to 10 and $f_{SYNTH} = 80 \times 2^{-(COARSECODE - 11)} \times 2^{(FINECODE / 16)}$(Hz) for Coarse Codes 11 and larger.

See the EIS Mode, Synthesis Frequency tables for all the available frequencies.

COARSE CODE*	FINE FREQUENCY CODE								
	-8	**-7**	**-6**	**-5**	**-4**	**-3**	**-2**	**-1**	**0**
3	14142	14768	15422	16105	16818	17563	18340	19152	20000
4	7071	7384	7711	8052	8409	8781	9170	9576	10000
5	3536	3692	3856	4026	4204	4391	4585	4788	5000
6	1768	1846	1928	2013	2102	2195	2293	2394	2500
7	884	923	964	1007	1051	1098	1146	1197	1250
8	442	462	482	503	526	549	573	599	625
9	221	231	241	252	263	275	287	300	313
10	110	115	120	126	131	137	143	149	156
11	56.6	59.1	61.7	64.4	67.3	70.3	73.4	76.6	80.0
12	28.3	29.5	30.8	32.2	33.6	35.1	36.7	38.3	40.0
13	14.1	14.8	15.4	16.1	16.8	17.6	18.3	19.2	20.0
14	7.07	7.38	7.71	8.05	8.41	8.78	9.17	9.58	10.00
15	3.54	3.69	3.86	4.03	4.20	4.39	4.59	4.79	5.00
16	1.77	1.85	1.93	2.01	2.10	2.20	2.29	2.39	2.50
17	0.884	0.923	0.964	1.007	1.051	1.098	1.146	1.197	1.250
18	0.442	0.462	0.482	0.503	0.526	0.549	0.573	0.599	0.625
19	0.221	0.231	0.241	0.252	0.263	0.274	0.287	0.299	0.313
20	0.110	0.115	0.120	0.126	0.131	0.137	0.143	0.150	0.156
21	0.0552	0.0577	0.0602	0.0629	0.0657	0.0686	0.0716	0.0748	0.0781

22	0.0276	0.0288	0.0301	0.0315	0.0328	0.0343	0.0358	0.0374	0.0391
23	0.0138	0.0144	0.0151	0.0157	0.0164	0.0172	0.0179	0.0187	0.0195

COARSE CODE*	**FINE FREQUENCY CODE**							
	0	**1**	**2**	**3**	**4**	**5**	**6**	**7**
3	20000	20885	21810	22776	23784	24837	25937	27085
4	10000	10443	10905	11388	11892	12419	12968	13543
5	5000	5221	5453	5694	5946	6209	6484	6771
6	2500	2611	2726	2847	2973	3105	3242	3386
7	1250	1305	1363	1423	1487	1552	1621	1693
8	625	653	682	712	743	776	811	846
9	313	327	341	356	372	389	406	424
10	156	163	170	178	186	194	202	211
11	80.0	83.5	87.2	91.1	95.1	99.3	103.7	108.3
12	40.0	41.8	43.6	45.6	47.6	49.7	51.9	54.2
13	20.0	20.9	21.8	22.8	23.8	24.8	25.9	27.1
14	10.00	10.44	10.91	11.39	11.89	12.42	12.97	13.54
15	5.00	5.22	5.45	5.69	5.95	6.21	6.48	6.77
16	2.50	2.61	2.73	2.85	2.97	3.10	3.24	3.39
17	1.250	1.305	1.363	1.423	1.487	1.552	1.621	1.693
18	0.625	0.653	0.682	0.712	0.743	0.776	0.811	0.846
19	0.313	0.326	0.341	0.356	0.372	0.388	0.405	0.423
20	0.156	0.163	0.170	0.178	0.186	0.194	0.203	0.212
21	0.0781	0.0816	0.0852	0.0890	0.0929	0.0970	0.1013	0.1058
22	0.0391	0.0408	0.0426	0.0445	0.0465	0.0485	0.0507	0.0529
23	0.0195	0.0204	0.0213	0.0222	0.0232	0.0243	0.0253	0.0265

*Coarse Code is the code in EIS_CLK_DIV[4:0] (0x7A).

CONVERT SETUP 1 (0x80)

BIT	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Field	SENS_CONV_TYPE	IOFFSET_CONV[1:0]		SYS_CONV_TYPE	SENS_PERIOD[3:0]			
Reset	0b0	0b00		0b0	0x0			
Access Type	Write, Read	Write, Read		Write, Read	Write, Read			

SENS_CONV_TYPE

SENS_CONV_TYP = 0: Performs a DC current conversion using the dedicated 16-bit Sensor ADC for each sensor channel.

SENS_CONV_TYP = 1: Performs an EIS conversion using the shared 16-bit AC Sensor ADC.

When selecting DC current conversion on multiple channels, the measurements are done in parallel and initiated simultaneously. For AC conversion, only one of the four sensors should be selected using Sn_SELECT (n = 1 to 4) (0x24, 0x31, 0x3E, 0x4B). If more than one sensor is selected for AC conversion, measurement is made for only the first selected sensor starting from Sensor 1.

IOFFSET_CONV

IOFFSET_CONV = 00: Measures sensor inputs plus offset.

IOFFSET_CONV = 01: Disconnects the sensor inputs to the ADC and enables offset current measurement on the selected sensors.

IOFFSET_CONV = 10: Measures the sensor inputs plus offset and the offset only in two separate measurements. Then calculates the sensor-only current and reports this calculation as the measured value.

IOFFSET_CONV = 01 or 10: The measured offset data are also written into the corresponding sensors' offset registers, i.e., registers 0x2B and 0x2C for SENSOR1. The resulting measurement ADC counts are saved into the FIFO in all modes.

SYS_CONV_TYPE

SYS_CONV_TYPE = 0: The System ADC completes an offset and offset + signal measurement for each input selected in the system ADC sequence.

SYS_CONV_TYPE = 1: The System ADC completes an offset measurement only once for each category of input signals (supply, sensor, or GPIO input) but completes an offset + signal measurement for each selected input.

GPIO input signals are controlled by AINn_SYS_SEL bits (n = 0, 1, 2, 3) (0x55). Supply input signals are controlled by VDD_SYS_SEL and GND_SYS_SEL bits (0x55). The sensor input signals are controlled by the register bits in registers 0x56 and 0x57.

The system ADC count in the FIFO corresponds to the signal only. The offset counts are automatically canceled out internally. The ADC counts in the offset measurement are saved in the SYS_VOFFSET[11:0] (0x5E,0x5F) bits. SYS_VOFFSET[11:0] is overwritten with a new value each time a system ADC measurement is made.

SENS_PERIOD

SENS_PERIOD[3:0] programs the period between sensor DC current conversions when in autonomous mode. The conversion time for the sensor current (Sensors 1, 2, 3, 4) measurement must be less than or equal to the period for valid conversions. If this condition is not met, then the INVALID_CFG (0x00) status bit is set.

See the SENS_PERIOD[3:0] DC Sensor Sample Period table for the available periods for sensor current measurements. The table values assume the nominal 246 slow clock cycles for the sensor ADC precharge phase.

SENS_PERIOD[3:0]	**DC SENSOR SAMPLE PERIOD**			
	COUNTER	**CLK_SEL = 0 (34.952kHz)**	**CLK_SEL = 1 (40.96kHz)**	**EXT_CLK (32.768kHz)**
	(clocks)	**(seconds)**	**(seconds)**	**(seconds)**
0x0	4,351	0.124	0.106	0.133
0x1	8,447	0.242	0.206	0.258
0x2	16,639	0.476	0.406	0.508
0x3	33,023	0.945	0.806	1.008
0x4	65,791	1.882	1.606	2.008
0x5	131,327	3.757	3.206	4.008
0x6	262,399	7.507	6.406	8.008
0x7	524,543	15.008	12.806	16.008
0x8	1,048,831	30.008	25.606	32.008
0x9	2,097,407	60.008	51.206	64.008

0xA	4,194,559	120.009	102.406	128.008
0xB to 0xF	8,388,863	240.011	204.806	256.008

CONVERT SETUP 2 (0x81)

BIT	7	6	5	4	3	2	1	0
Field	TEMP_PERIOD[3:0]				SYS_PERIOD[3:0]			
Reset	0x0				0x0			
Access Type	Write, Read				Write, Read			

TEMP_PERIOD

TEMP_PERIOD[3:0] programs the period between temperature sensor conversions in autonomous mode. The conversion time for the temperature sensor must be set to be less than or equal to the period for valid conversions. If this condition is not met, then the INVALID_CFG (0x00) status bit is set.

See the TEMP_PERIOD[3:0] Temperature Sensor Sample Period table for the available periods for temperature sensor measurement. It assumes the nominal 246 slow clock cycles for the Sensor ADC precharge phase.

TEMP_PERIOD[3:0]	TEMPERATURE SENSOR SAMPLE PERIOD			
	COUNTER	CLK_SEL = 0 (34.952kHz)	CLK_SEL = 1 (40.96kHz)	EXT_CLK (32.768kHz)
	(clocks)	(seconds)	(seconds)	(seconds)
0x0	4,351	0.124	0.106	0.133
0x1	8,447	0.242	0.206	0.258
0x2	16,639	0.476	0.406	0.508
0x3	33,023	0.945	0.806	1.008
0x4	65,791	1.882	1.606	2.008
0x5	131,327	3.757	3.206	4.008
0x6	262,399	7.507	6.406	8.008
0x7	524,543	15.008	12.806	16.008
0x8	1,048,831	30.008	25.606	32.008
0x9	2,097,407	60.008	51.206	64.008
0xA	4,194,559	120.009	102.406	128.008
0xB to 0xF	8,388,863	240.011	204.806	256.008

SYS_PERIOD

SYS_PERIOD[3:0] programs the period between System ADC conversions when in autonomous mode. If more than one input is selected for conversion, then they are converted in succession at the beginning of each period. The total conversion time for the inputs selected must be less than or equal to the period for valid conversions. If this condition is not met, then the INVALID_CFG (0x00) status bit is set.

See the SYS_PERIOD[3:0] System ADC Sample Period table for the available periods for analog voltage measurements. It assumes the nominal 246 slow clock cycles for the Sensor ADC precharge phase.

SYS_PERIOD[3:0]	SYSTEM ADC SAMPLE PERIOD			
	COUNTER	CLK_SEL = 0 (34.952kHz)	CLK_SEL = 1 (40.96kHz)	EXT_CLK (32.768kHz)
	(clocks)	(seconds)	(seconds)	(seconds)
0x0	4,351	0.124	0.106	0.133

0x1	8,447	0.242	0.206	0.258
0x2	16,639	0.476	0.406	0.508
0x3	33,023	0.945	0.806	1.008
0x4	65,791	1.882	1.606	2.008
0x5	131,327	3.757	3.206	4.008
0x6	262,399	7.507	6.406	8.008
0x7	524,543	15.008	12.806	16.008
0x8	1,048,831	30.008	25.606	32.008
0x9	2,097,407	60.008	51.206	64.008
0xA	4,194,559	120.009	102.406	128.008
0xB to 0xF	8,388,863	240.011	204.806	256.008

CONVERT START (0x83)

BIT	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Field	–	–	–	–	–	–	AUTO	CONVERT
Reset	–	–	–	–	–	–	0b0	0b0
Access Type	–	–	–	–	–	–	Write, Read	Write, Read

AUTO

AUTO = 0: Manual mode

When CONVERT is set to 1, all selected channels complete a single conversion, and data is transferred to the FIFO. In this mode SENS_PERIOD[3:0] (0x80), TEMP_PERIOD[3:0] (0x81) and SYS_PERIOD[3:0] (0x81) are ignored.

AUTO = 1: Autonomous mode

When CONVERT is set to 1, all selected channels are continuously converted at the rate determined by each channels period setting in SENS_PERIOD[3:0], TEMP_PERIOD[3:0], and SYS_PERIOD[3:0]. Conversions continue until CONVERT, or AUTO is set to 0.

In autonomous mode, selected channels and their sampling period are controlled as follows:

Setting Sn_SELECT (n = 1 to 4) (0x24, 0x31, 0x3E, 0x4B) to 1 selects the DC sensor channels that continuously auto-convert at the period set by SENS_PERIOD[3:0].

Setting TEMP_SELECT (0x60) to 1 selects the temperature to be converted at the period set by TEMP_PERIOD[3:0].

Setting SYS_SELECT (0x55) to 1 allows all system channels that have their select bit set to 1 to be converted continuously at the period set by SYS_PERIOD[3:0]. System channels that can be selected are, Sn_CE_SEL, Sn_RE_SEL, Sn_WE_SEL Sn_WO_SEL (n = 1 or 2; 0x56) (n = 3 or 4; 0x57). Power, ground, and GPIO channels can also be selected using VDD_SYS_SEL(0x55), GND_SYS_SEL (0x55), and AINx_SYS_SEL (x = 1 to 4) (0x55).

When more than one system channel is selected, care must be taken to ensure that the total time required to sample all channels in the sequence is less than the period set by SYS_PERIOD[3:0].

When the ADC conversion time for a single channel or the total time for all selected channels is greater than the selected sample period, the INVALID_CFG (0x00) status bit is set. In this case, all conversions proceed as normal up to the end of the sample period then the conversion cycle abruptly restarts before completing all selected channels. Data saved in the FIFO is invalid for the interrupted channel.

When a conversion is in progress (CONVERT = 1), and AUTO is changed, the following occurs.

AUTO is changed from 0 to 0, manual conversion is completed without interruption.

AUTO is changed from 0 to 1, manual aborts all conversions, and new conversions start in auto mode.

AUTO is changed from 1 to 0, conversion stops when the current conversion period completes.

AUTO is changed from 1 to 1, conversions in auto mode continue.

If any of the four GPIOx pins have their mode GPIOx_MODE[3:0] (x = 1 to 4) (0x90, 0x91, 0x92, 0x93) set to modes 2, 3, 4, or 5

AUTO and CONVERT functions are ignored for selected channel groups. See GPIOx_MODE[3:0] for more details.

CONVERT

CONVERT = 0: Immediately aborts all conversions in progress. When writing 0 to the CONVERT bit, it is also important to write 0 to the AUTO bit.

CONVERT = 1: Starts data conversions on the selected sensor channels, temperature sensor, and selected system ADC inputs. This bit stays high while conversions are in progress and are set to zero when the conversions are complete. In manual mode, AUTO = 0, and the conversions are complete when all the selected channels have finished their conversions once. In auto mode, AUTO = 1, the conversions are continuous and do not stop until the CONVERT bit is deasserted.

Set CONVERT to 0 to immediately abort all conversions in progress. When writing 0 to the CONVERT bit, it is also important to write 0 to the AUTO bit.

If CONVERT is changed from 0 to 0, then it does nothing.

If CONVERT is changed from 0 to 1, a conversion cycle is initiated.

If CONVERT is changed from 1 to 0 while conversions are running, then the conversion cycle stops, and any running conversion is aborted.

If CONVERT is changed from 1 to 1 while conversions are running, then it is ignored, and conversions continue.

The CONVERT bit is ignored for any ADC conversion if a GPIO port controls that ADC conversion. See GPIOx_MODE[3:0] (x = 1 to 4) (0x90, 0x91, 0x92, 0x93).

GPIO1 SETUP (0x90)

BIT	7	6	5	4	3	2	1	0
Field	GPIO1_MODE[3:0]				GPIO1_IPU	GPIO1_ICFG	GPIO1_OCFG[1:0]	
Reset	0x0				0b0	0b0	0b00	
Access Type	Write, Read				Write, Read	Write, Read	Write, Read	

GPIO1_MODE

(x = 1 to 4)

GPIOx_MODE[3:0] selects the function of the GPIOx port.

Since more than one GPIO port can be configured in the same input mode (GPIOx_MODE[3:0] = 0x2 to 0xB), there is a priority setting among those ports. For a given GPIO mode selection, GPIO4_MODE has precedence over GPIO3_MODE, GPIO2_MODE, and GPIO1_MODE; GPIO3_MODE has precedence over GPIO2_MODE and GPIO1_MODE; and GPIO2_MODE has precedence over GPIO1_MODE. When two or more GPIO ports have the same input mode in the range 0x2 to 0xB, the input modes of GPIO ports with the lower precedence are ignored.

For GPIOx_MODE[3:0] = 0x2 to 0x5, the GPIO input should remain in the active state after the active edge for at least the minimum pulse width, t_{PLGPIO}, specified under the Electrical Characteristics table.

GPIOx_MODE[3:0] (x = 1 to 4)	PORT TYPE/ DIRECTION	GPIOx (x = 1 to 4)	DESCRIPTION
0x0	Analog Input	Analog Input	Analog Input for System ADC
0x1	Digital Input	Digital input	Digital input that reports logic level on pin when the GPIO INPUT register at 0x94 is read. A weak pullup can be enabled on this input.
0x2	Digital Input	Sensor ADC convert	Rising or falling edge starts the sensor ADC conversions on selected sensor channels. All selected sensor conversions begin at the same time. The active edge can be programmed to be rising or falling. If the active edge is asserted while a conversion is in progress then the current conversion is aborted and a new conversion begins. If this mode is programmed, DC Sensor conversions ignores the AUTO and CONVERT bits in the CONVERT_START register.
0x3	Digital Input	Temperature convert	Rising or falling edge starts the temperature sensor ADC conversion. The active edge can be programmed to be rising or falling. If the active edge is asserted while a conversion is in progress then the current conversion is aborted and a new conversion begins. If this mode is programmed, temperature sensor conversions ignores the AUTO and CONVERT bits in the CONVERT_START register.
0x4	Digital Input	System ADC convert	Rising or falling edge starts the system ADC conversions on selected channels. Conversions are performed in sequence when multiple channels are selected. The active edge can be programmed to be rising or falling. If the active edge is asserted while a conversion is in progress then the current conversion is aborted and a new conversion begins. If this mode is programmed, System ADC conversions ignores the AUTO and CONVERT bits in the CONVERT_START register.
0x5	Digital Input	All convert	Rising or falling edge starts selected sensors, temperature sensor, and system ADC conversions. The active edge can be programmed to be rising or falling. If the active edge is asserted while any of the selected conversions is in progress then all current conversions are aborted and all selected conversion begin again. If this mode is programmed, the AUTO and CONVERT bits in CONVERT_START register are ignored.
0x6	Digital Input	External Period Clock	Drive with an external 32.768kHz clock to override the internal SLOW clock for sample periods used in AUTO mode.
0x7	Hi-Z	Reserved	Reserved

0x8	Hi-Z	Reserved	Reserved
0x9	Hi-Z	Reserved	Reserved
0xA	Digital Input	Open circuit all sensors	Asserting the GPIO input opens the circuit of all the sensor channels from the front end. The front end is high impedance to the sensor and when going open the circuit does not inject charge onto the sensor or change the voltage that the sensor was set to. The System ADC is able to measure the voltage on the three electrode pins for each sensor without disturbing the sensor. The active level can be programmed to be high or low.
0xB	Digital Input	Shut down	Asserting the GPIO input shuts down all the blocks within the chip. The register settings are preserved and when deasserted the chip returns to the previously programmed state. The active level can be programmed to be high or low.
0xC	Digital Output	Logic level Low	Digital output set to a logic low. The output type can be programmed to be actively driven, open drain, or open drain with a weak pullup.
0xD	Digital Output	Logic level High	Digital output set to a logic high. The output type can be programmed to be actively driven, open drain, or open drain with a weak pullup.
0xE	Hi-Z	Reserved	Reserved
0xF	Hi-Z	Reserved	Reserved

GPIO1_IPU

(x = 1 to 4)

GPIOx_IPU = 0: Disables the weak pull-up on GPIOx when configured as a digital input port.

GPIOx_IPU = 1: Enables the weak pull-up on GPIOx when configured as a digital input port.

GPIO1_ICFG

(x = 1 to 4)

GPIOx_ICFG = 0:

Configures GPIOx port to trigger a CONVERT (0x83) command on a falling edge when GPIOx_MODE[3:0] = 0x2 to 0x5. Configures GPIOx to open all sensors during an active low input when GPIOx_MODE[3:0] is set to 0xA and power down the device during an active low input when GPIOx_MODE[3:0] is set to 0xB.

GPIOx_ICFG = 1:

Configures GPIOx port to trigger a CONVERT command on a rising edge when GPIOx_MODE[3:0] = 0x2 to 0x5. Configures GPIOx to open all sensors during an active high input when GPIOx_MODE[3:0] is set to 0xA and power down the device during an active high input when GPIOx_MODE[3:0] is set to 0xB.

GPIOx_ICFG (x = 1 to 4)	DESCRIPTION
0	Active edge is falling or active level is low
1	Active edge is rising or active level is high

GPIO1_OCFG

(x = 1 to 4)

GPIOx_OCFG[1:0] configures GPIOx output drive.

GPIOx_OCFG[1:0], (x = 1 to 4)	GPIOx OUTPUT DRIVE CONFIGURATION
00	Open drain, V_{DD} compliant, active low output
01	Active drive to V_{DD} and GND, active high
10	Active drive to V_{DD} and GND, active low
11	Open Drain with weak pullup

GPIO2 SETUP (0x91)

BIT	7	6	5	4	3	2	1	0
Field	GPIO2_MODE[3:0]				GPIO2_IPU	GPIO2_ICFG	GPIO2_OCFG[1:0]	
Reset	0x0				0b0	0b0	0b00	
Access Type	Write, Read				Write, Read	Write, Read	Write, Read	

GPIO2_MODE

See GPIO1_MODE[3:0] for more details.

GPIO2_IPU

See GPIO1_IPU for more details.

GPIO2_ICFG

See GPIO1_ICFG for more details.

GPIO2_OCFG

See GPIO1_OCFG for more details.

GPIO3 SETUP (0x92)

BIT	7	6	5	4	3	2	1	0
Field	GPIO3_MODE[3:0]				GPIO3_IPU	GPIO3_ICFG	GPIO3_OCFG[1:0]	
Reset	0x0				0b0	0b0	0b00	
Access Type	Write, Read				Write, Read	Write, Read	Write, Read	

GPIO3_MODE

See GPIO1_MODE[3:0] for more details.

GPIO3_IPU

See GPIO1_IPU for more details.

GPIO3_ICFG

See GPIO1_ICFG for more details.

GPIO3_OCFG

See GPIO1_OCFG for more details.

GPIO4 SETUP (0x93)

BIT	7	6	5	4	3	2	1	0
Field	GPIO4_MODE[3:0]				GPIO4_IPU	GPIO4_ICFG	GPIO4_OCFG[1:0]	
Reset	0x0				0b0	0b0	0b00	
Access Type	Write, Read				Write, Read	Write, Read	Write, Read	

GPIO4_MODE

See GPIO1_MODE[3:0] for more details.

GPIO4_IPU

See GPIO1_IPU for more details.

GPIO4_ICFG

See GPIO1_ICFG for more details.

GPIO4_OCFG

See GPIO1_OCFG for more details.

GPIO INPUT (0x94)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	GPIO4_LL	GPIO3_LL	GPIO2_LL	GPIO1_LL
Reset	–	–	–	–	0b0	0b0	0b0	0b0
Access Type	–	–	–	–	Read Only	Read Only	Read Only	Read Only

GPIO4_LL

GPIOx_LL (x = 1 to 4) is a read-only bit, and it returns the logic state of the GPIOx pin.

GPIO3_LL

See GPIO4_LL for more details.

GPIO2_LL

See GPIO4_LL for more details.

GPIO1_LL

See GPIO4_LL for more details.

INTB SETUP (0x95)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	–	EN_VDD_OOR	INTB_OCFG[1:0]	
Reset	–	–	–	–	–	0b0	0b00	
Access Type	–	–	–	–	–	Write, Read	Write, Read	

EN_VDD_OOR

EN_VDD_OOR = 0: Disables V_{DD} out-of-range detection to save power.

EN_VDD_OOR = 1: Enables V_{DD} out-of-range detection.

See VDD_OOR in Status Register 1 for more details.

INTB_OCFG

INTB_OCFG[1:0] configures the INTB output drive.

INTB_OCFG	ENUMERATION	INTB OUTPUT DRIVE CONFIGURATION
0x0	OPEN_DR	Open-drain output, active low
0x1	ACT_DR_HIGH	Push-pull output, active high
0x2	ACT_DR_LOW	Push-pull output, active low
0x3	WEAK_PU	Open-drain output with weak pullup, active low

SWV SETUP 1 (0xA0)

BIT	7	6	5	4	3	2	1	0
Field	EIS_DAC_INC[3:0]				–	EIS_INTEG	AC_MODE[1:0]	
Reset	0b0000				–	0b0	0b00	
Access Type	Write, Read				–	Write, Read	Write, Read	

EIS_DAC_INC

EIS_DAC_INC[3:0] sets the step size as EIS_DAC_INC + 1 LSBs for the staircase for SWV and CV modes. Actual step size in mV depends on V_{REF}, as is given by

V_{STEP} = (EIS_DAC_INC[3:0] + 1) x V_{REF} / 2^{12}

The step size ranges from approximately 1mV to 10mV.

The staircase starts at DACm_CODE[11:0] (m = A, B, C, D) (0x69 to 0x70) for the DC DAC selected by EIS_DAC_SEL[1:0] (0x78), ramps up to EIS_DAC_STOP[11:0] (0xA1), then ramps down until it reaches DACm_CODE[11:0].

If EIS_DAC_STOP[11:0] is not equal to DACm_CODE[11:0] + N x (EIS_DAC_INC[3:0] + 1), where N is an integer for the number of steps in the staircase, the ramping up stops at the largest code below EIS_DAC_STOP[11:0].

EIS_INTEG

EIS_INTEG defines the ADC integration time for SWV and CV modes.

EIS_INTEG	INTEGRATION TIME (μs)
0	50
1	200

AC_MODE

AC_MODE[1:0] selects the AC measurement mode to be used when SENS_CONV_TYPE (0x80) = 1

The AC_MODE[1:0] table shows available AC measurement modes. See the EIS Sensor ADC, Cyclic Voltammetry Mode, or Square-Wave Voltammetry Mode section of the data sheet for detailed information on the different AC measurement modes.

AC_MODE[1:0]	MODE	AC DAC AND SELECTED DC DAC FUNCTIONS
00	EIS Mode (Electrochemical Impedance Spectroscopy)	AC DAC, Sine-waves amplitude DC DAC, DC Offset code
01	CV Mode (Cyclic Voltammetry)	AC DAC, Not used DC DAC, Ramp-Up and Ramp-Down Steps
10	SWV Mode (Square-Wave Voltammetry)	AC DAC, Square-waves amplitude DC DAC, Ramp-Up Steps
11	Reserved	

Note: System ADC and temperature ADC conversions should be disabled before initiating AC Mode conversions, frequency TRIM calibration, or phase advance calibration. Do not read the FIFO during AC Mode conversions, frequency TRIM calibration, or phase advance calibration.

SWV SETUP 2 (0xA1)

BIT	7	6	5	4	3	2	1	0
Field	EIS_DAC_STOP[11:4]							
Reset	0xFF							
Access Type	Write, Read							

EIS_DAC_STOP

EIS_DAC_STOP[11:4] has the upper eight bits of the EIS_DAC_STOP[11:0] DAC code limit used for generating CV and SWV waveforms. EIS_DAC_STOP[3:0] has the lower 4 bits.

See the EIS_DAC_INC[4:0] (0xA0) and the Cyclic Voltammetry Mode or Square-Wave Voltammetry Mode section of the data sheet for more details.

SWV SETUP 3 (0xA2)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	EIS_DAC_STOP[3:0]			
Reset	–	–	–	–	0xF			
Access Type	–	–	–	–	Write, Read			

EIS_DAC_STOP

See the EIS_DAC_STOP[11:4] for more details.

PART IDENTIFIER (0xFF)

BIT	7	6	5	4	3	2	1	0
Field	PART_ID[7:0]							
Reset								
Access Type	Read Only							

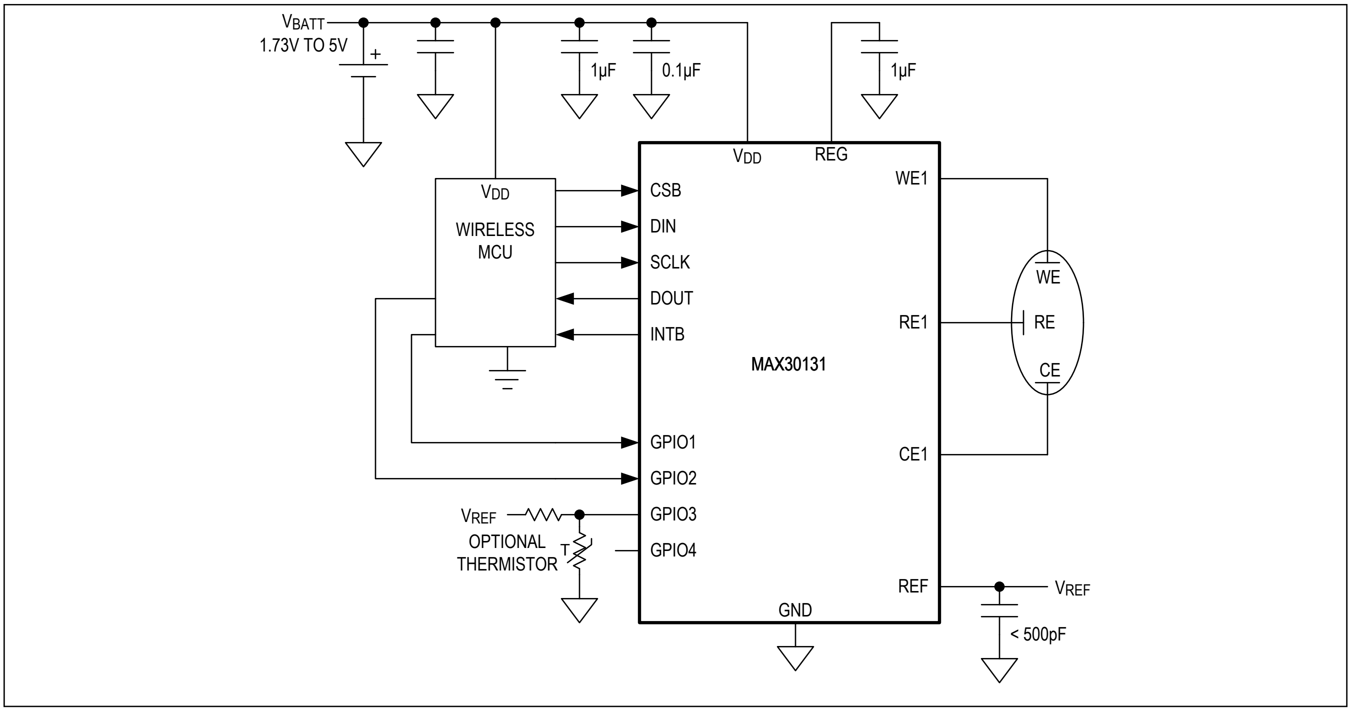
PART_ID

PART_ID[7:0] is a read-only register that has the Part identifier for the chip. See the MAX Part Number table for the MAX Part Number and Part ID codes.

MAX PART NUMBER	PART ID
MAX30131	0x32
MAX30132	0x33
MAX30134	0x34

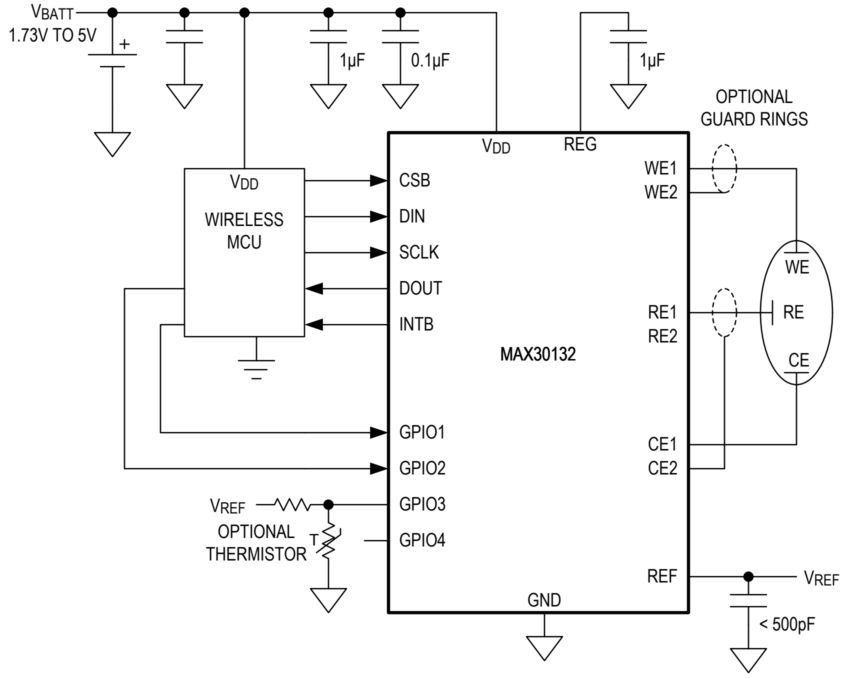
Typical Application Circuits

3-Terminal Electrochemical Sensor with Optional Temperature Sensor and Wireless Interface Powered from a Coin Cell



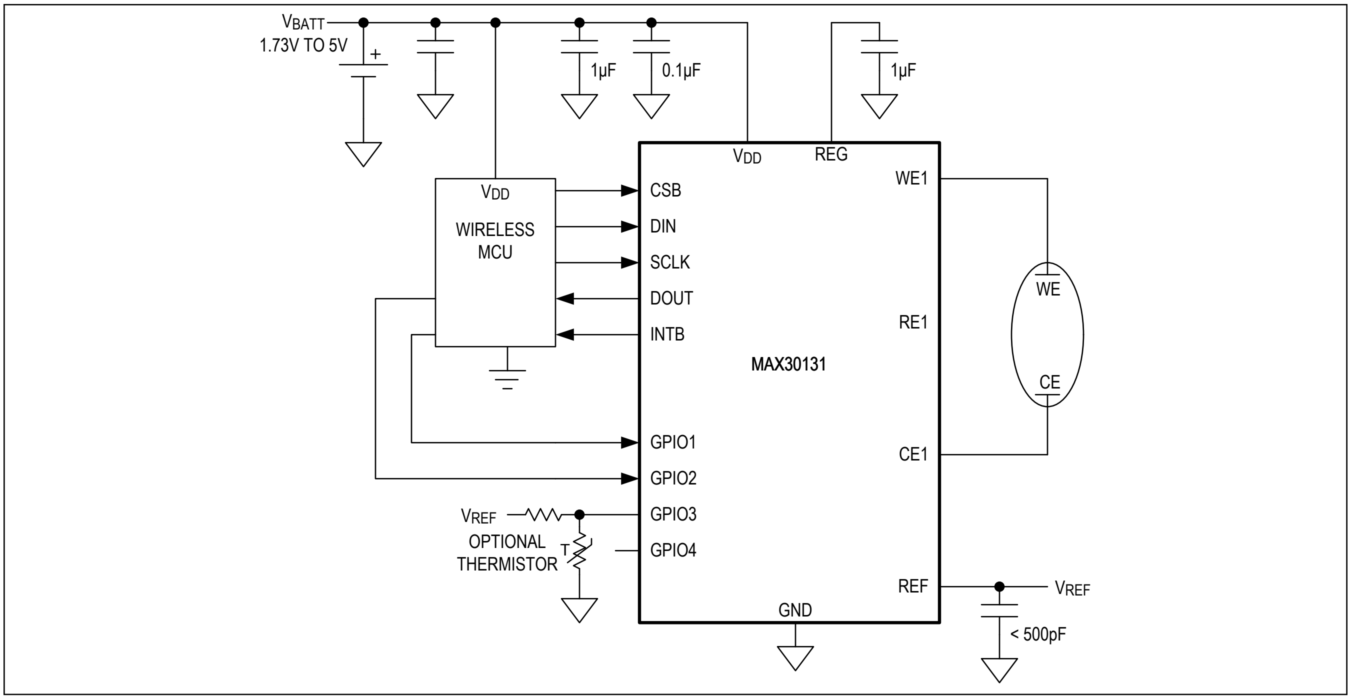
Typical Application Circuits (continued)

3-Terminal Electrochemical Sensor with Optional Guard Rings, Optional Thermistor, and Wireless Interface Powered from a Coin Cell



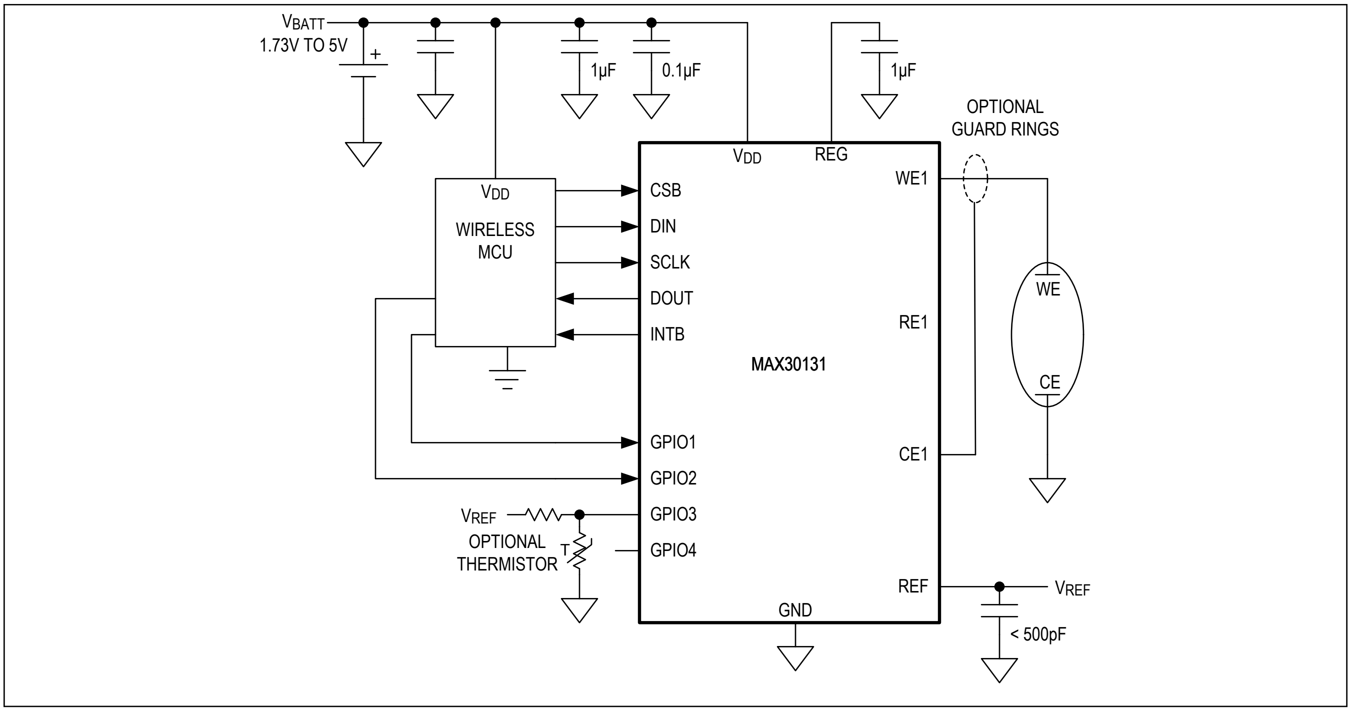
Typical Application Circuits (continued)

2-Terminal Electrochemical Sensor with Driven Counter, Optional Thermistor, and Wireless Interface Powered from a Coin Cell



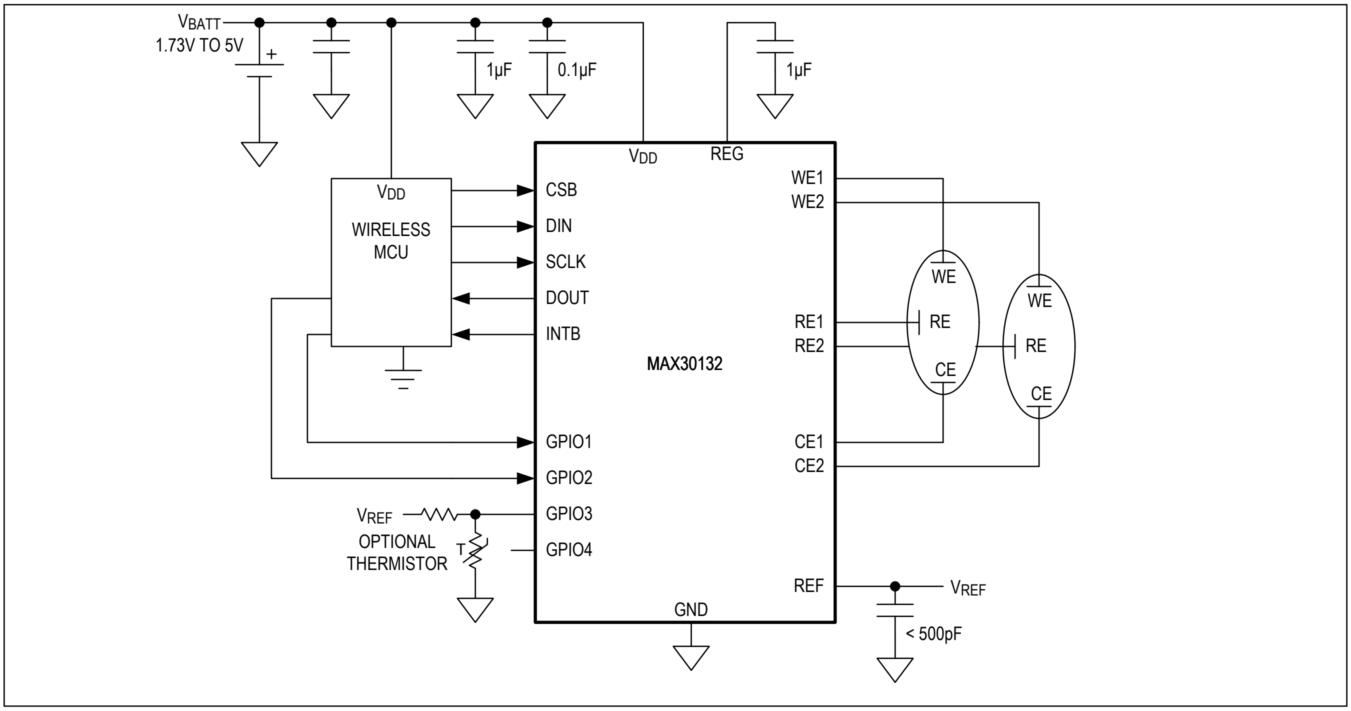
Typical Application Circuits (continued)

2-Terminal Electrochemical Sensor with Optional Guard Ring, Optional Thermistor, and Wireless Interface Powered from a Coin Cell



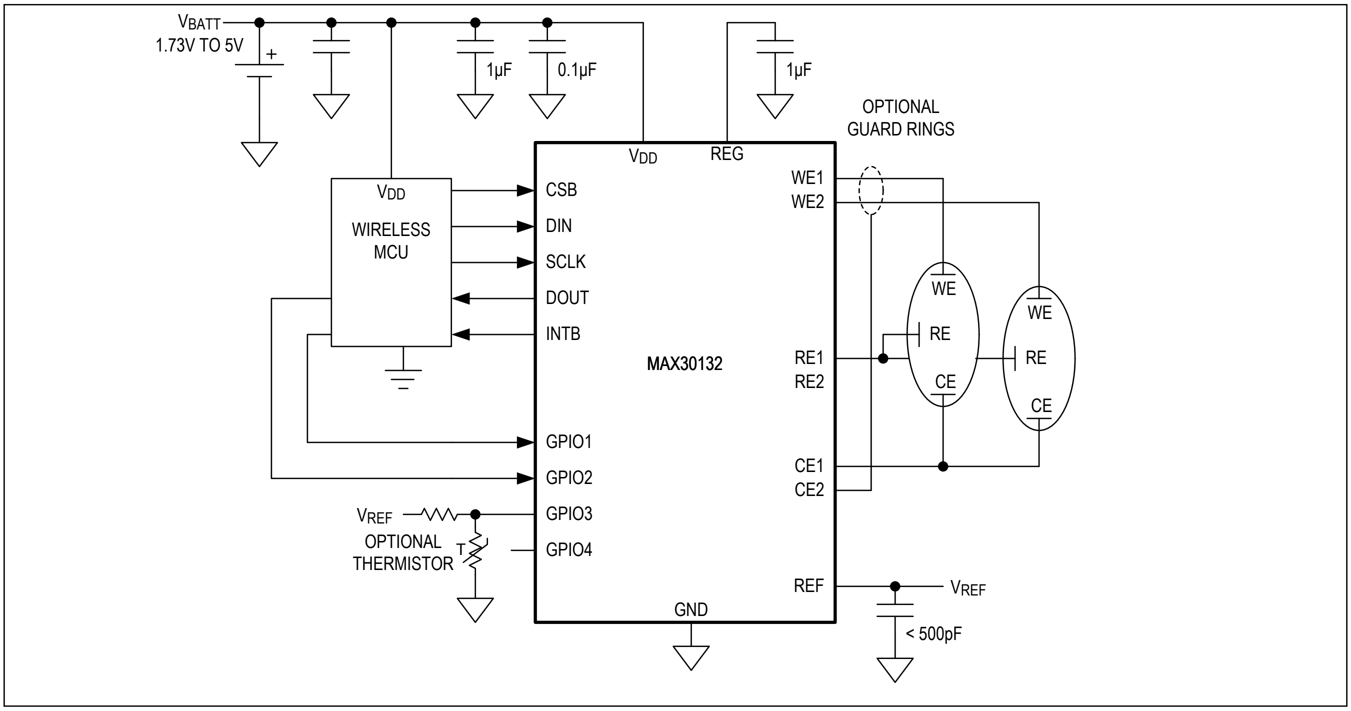
Typical Application Circuits (continued)

Dual 3-Terminal Electrochemical Sensor with Optional Thermistor, and Wireless Interface Powered from a Coin Cell



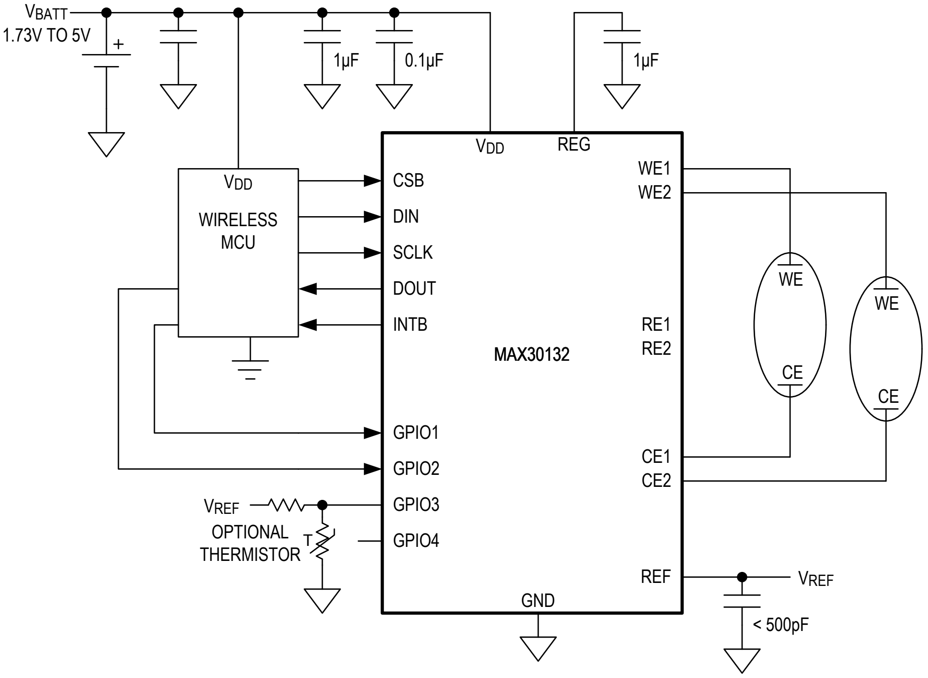
Typical Application Circuits (continued)

Dual 3-Terminal Electrochemical Sensor with Shared Reference/Counter, Optional Guard Ring, Optional Thermistor, and Wireless Interface Powered from a Coin Cell



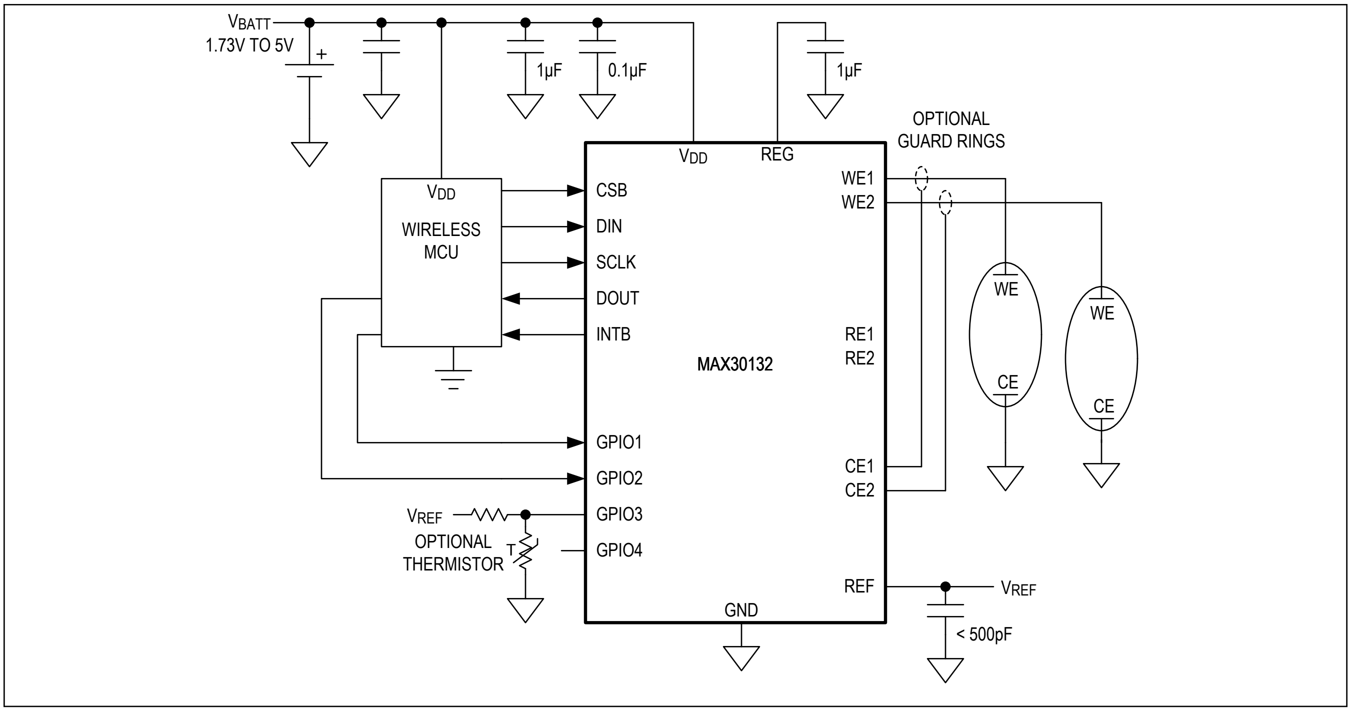
Typical Application Circuits (continued)

Dual 2-Terminal Electrochemical Sensor with Driven Counters, Optional Thermistor, and Wireless Interface Powered from a Coin Cell



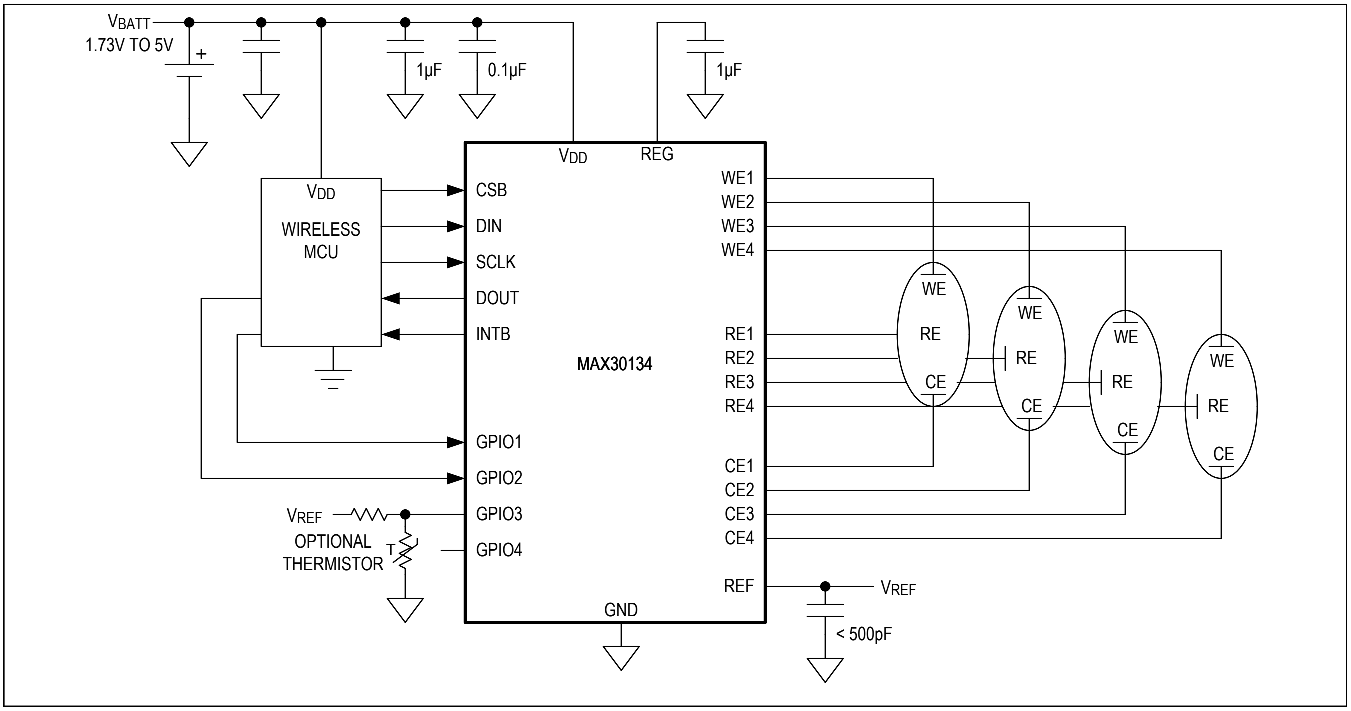
Typical Application Circuits (continued)

Dual 2-Terminal Electrochemical Sensor with Optional Guard Rings, Optional Thermistor, and Wireless Interface Powered from a Coin Cell



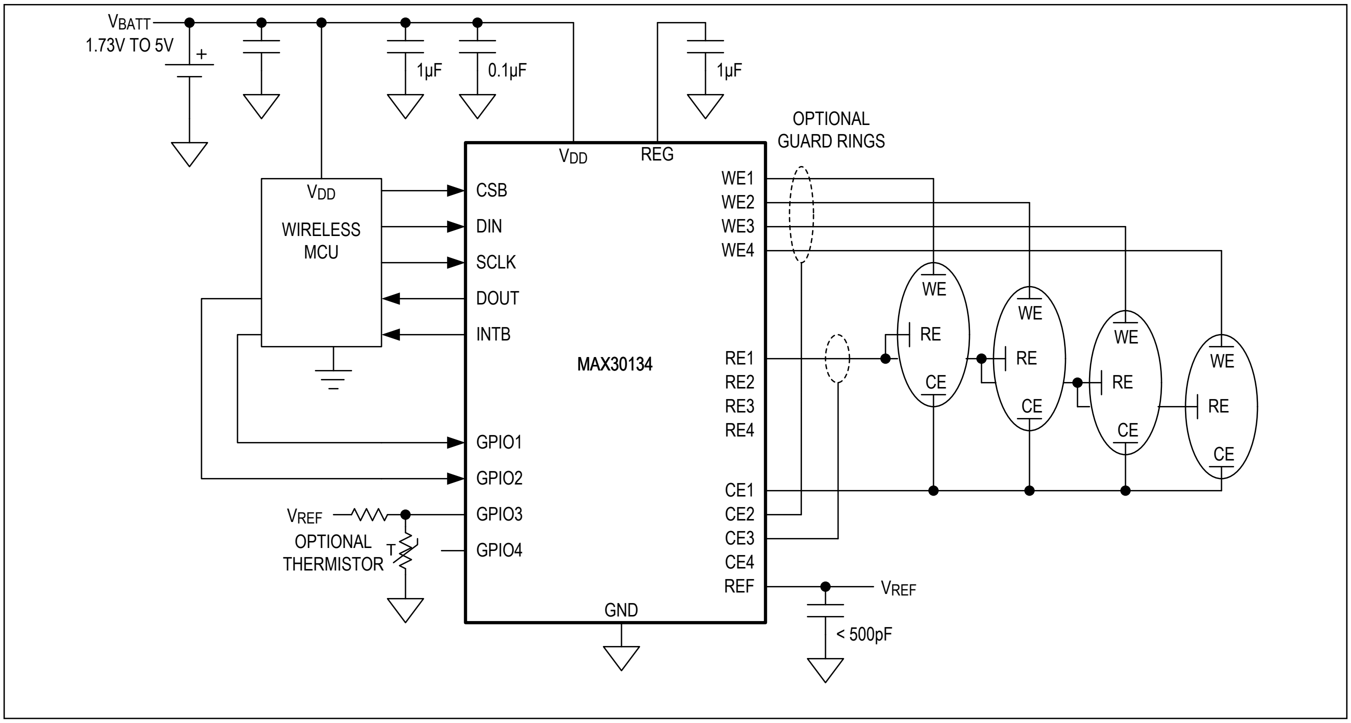
Typical Application Circuits (continued)

Quad 3-Terminal Electrochemical Sensor with Optional Thermistor, and Wireless Interface Powered from a Coin Cell



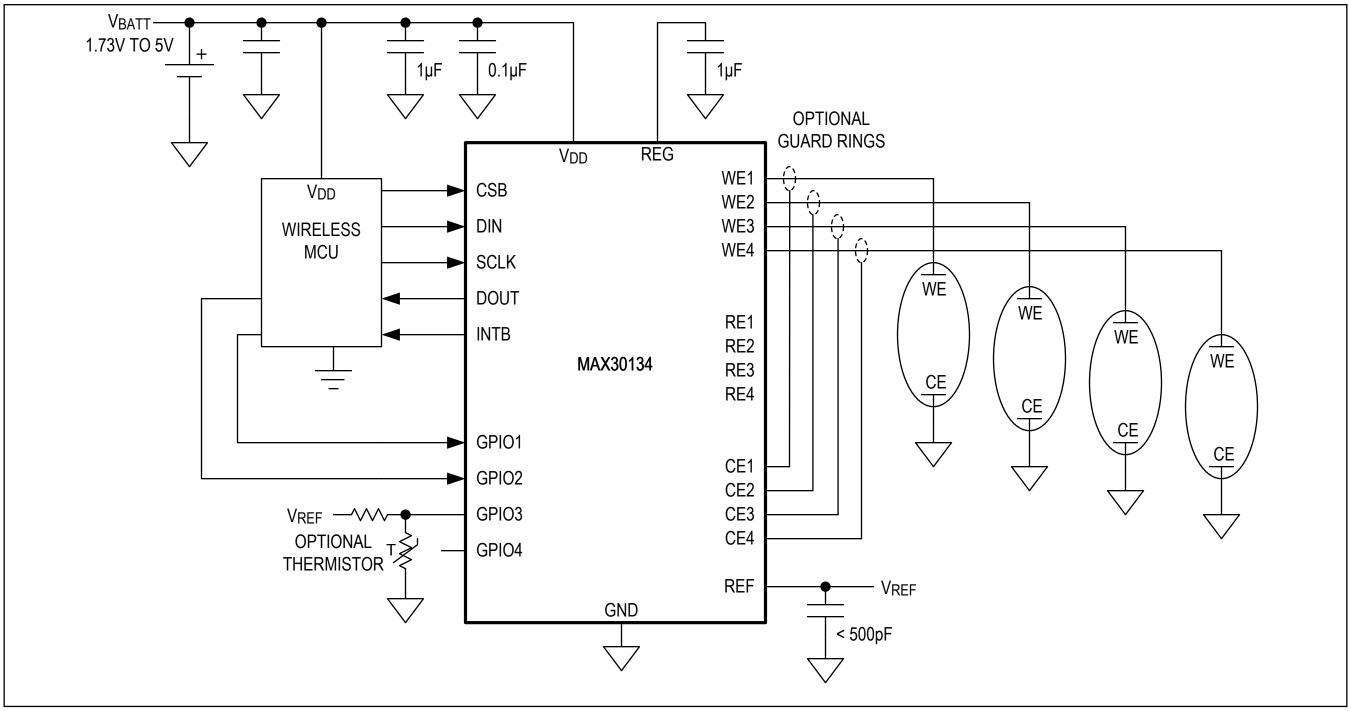
Typical Application Circuits (continued)

Quad 3-Terminal Electrochemical Sensor with Shared Reference/Counter, Optional Guard Ring, Optional Thermistor, and Wireless Interface Powered from a Coin Cell



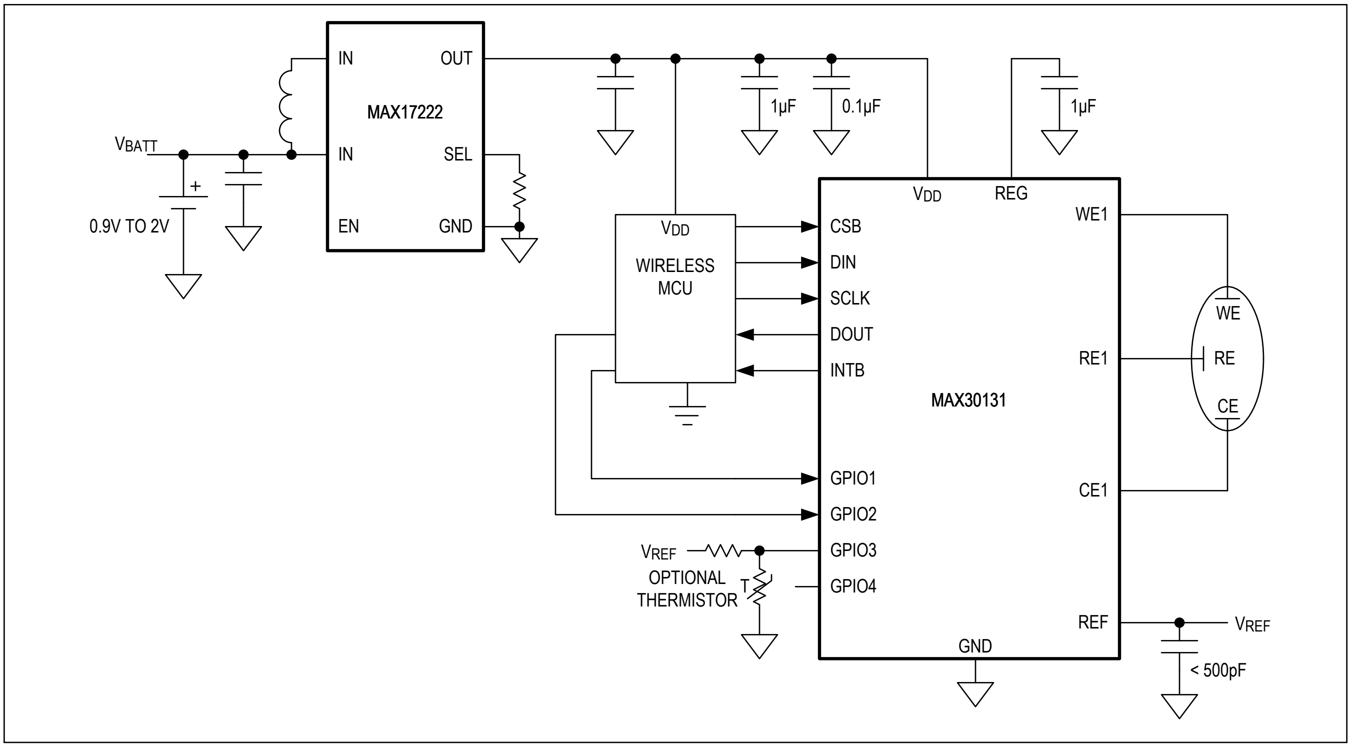
Typical Application Circuits (continued)

Quad 2-Terminal Electrochemical Sensor with Optional Guard Ring, Optional Thermistor, and Wireless Interface Powered from a Coin Cell



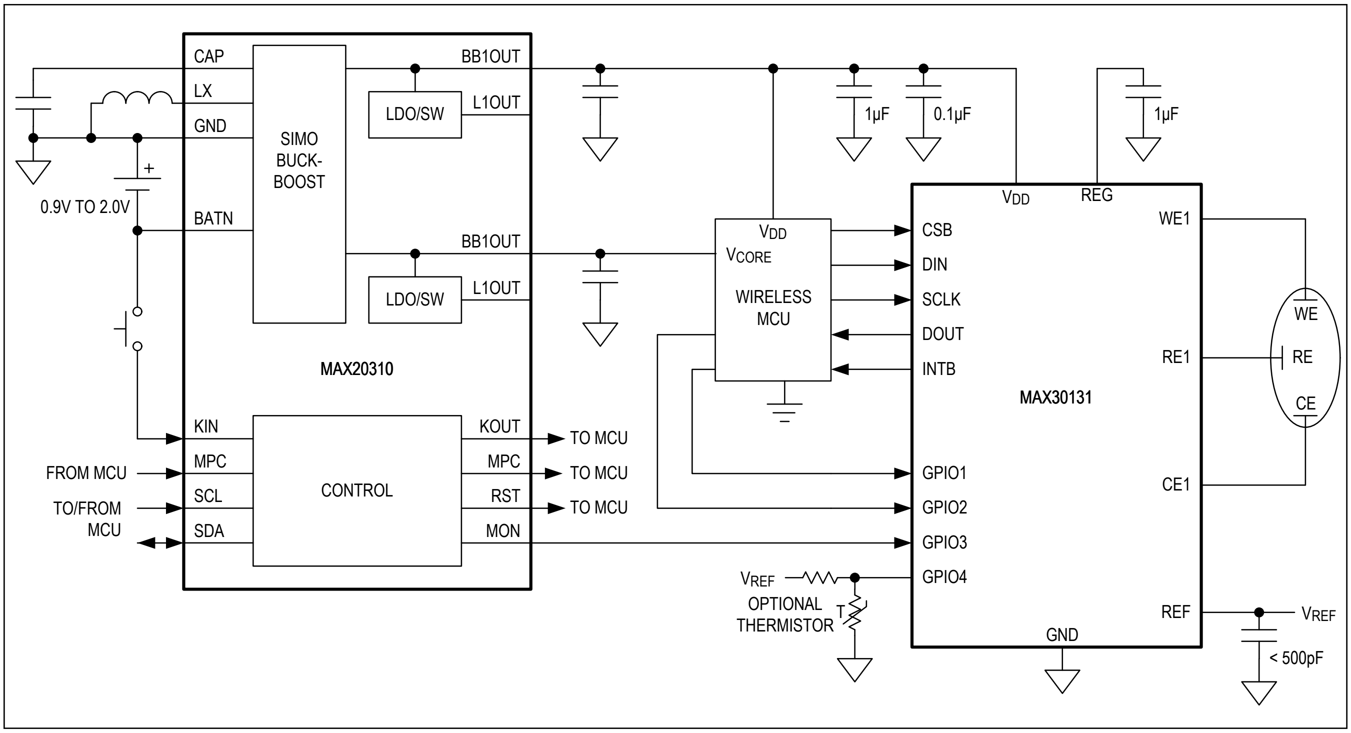
Typical Application Circuits (continued)

MAX30131 and Wireless MCU Powered from a Single Silver Oxide or Zinc Air Button or Alkaline Cell and Nano-Boost Converter



Typical Application Circuits (continued)

MAX30131 and Wireless MCU Powered from a Single Silver Oxide or Zinc Air Button or Alkaline Cell and Nano-Power PMIC



Ordering Information

PART NUMBER	TEMP RANGE	PIN-PACKAGE	CONFIGURATION
MAX30131CWA+T	-0°C to +70°C	25-Bump WLP, 2.93 x 2.93mm, 0.5mm Pitch	One-Channel Electrochemical Sensor AFE
MAX30132CWA+T	-0°C to +70°C	25-Bump WLP, 2.93 x 2.93mm, 0.5mm Pitch	Two-Channel Electrochemical Sensor AFE
MAX30134CWA+T	-0°C to +70°C	25-Bump WLP, 2.93 x 2.93mm, 0.5mm Pitch	Four-Channel Electrochemical Sensor AFE

+Denotes a lead(Pb)-free/RoHS-compliant package.

T = Tape and reel.

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	8/19	Initial release	—
1	10/19	Updated the *Absolute Maximum Ratings, Electrical Characteristics, Voltage Reference, Sensor AFE, Sensor Configurations, Sensor Operating Modes, Offset and Gain Calibration, Sensor Detect, EIS Sensor ADC, EIS Operating Theory Overview, Details with Simplified Block Diagram, Making EIS DC Measurements, Optimizing the EIS Voltage-Drive and Current-Range Settings, Fine Frequency Extension and Calibration, Averaging Cycles, EIS Frequency Response, Placing a Null Near 60Hz, Measurement Repeatability and Noise, EIS Calibration, Calculating or Calibrating the Phase Advance, Extracting Parasitics, Cyclic Voltammetry Mode, Square Wave Voltammetry Mode, System ADC, System ADC Offset, Temperature Sensor, System ADC Alarms, Temperature ADC Alarms, GPIO, Status Bits and Interrupt, SPI Timing, Single Register SPI Read/Write Transaction, Read Pointer (0x0B), FIFO Data Format, FIFO_A_FULL (0x0F), FIFO_RO (0x10),* and *A_FULL_TYPE (0x10)* sections, the *Typical Operating Circuits*, Tables 6 and 7, and the *Register Map* and *Register Details*; replaced the *Simplified Block Diagram, Functional Diagrams*, Figures 1–13, Figures 16–21, Figures 24–25, and the *Sensor ADC Alarms* section; added a new Table 1 and renumbered subsequent tables; removed Figure 23 and Figure 26, and renumbered subsequent figures; corrected typos	2–4, 11, 12, 17, 21, 30–48, 50–58, 59-66, 68, 73, 75–79, 82–83, 96–100, 113–124, 126–146, 150–151, 153–168
2	1/20	Updated the *General Description, Benefits and Features, Package Information, Electrical Characteristics, Detailed Description, Voltage Reference, Sensor ADC, Making EIS DC Measurements, Optimizing the EIS Voltage-Drive and Current-Range Settings, EIS Frequency Response, Placing a Null Near 60Hz, Calculating or Calibrating the Phase Advance, Cyclic Voltammetry Mode, Square Wave Voltammetry Mode*, and the *Register Details* sections; replaced TOC37 and added TOC38; removed future product designations from MAX30131CWA+T and MAX30132CWA+T in the *Ordering Information* table	1, 10, 16, 25, 31, 39, 47, 49, 53–54, 56, 59–60, 78, 90–91, 134, 146, 159
3	7/20	Updated the *General Description, Electrical Characteristics, Pin Description, Voltage Reference, Sensor DACs, Sensor AFE, Sensor ADC, EIS Sensor ADC, System ADC, Temperature ADC Alarms,* and *FIFO Description--Read Format (0x0B) and FIFO Data Format* sections; updated the EIS_CAL_DONE, BYPASS_LDO, IOFFSET_CONV, REF_VAL, FAST_TRIM_ADJ, SLOW__TRIM_ADJ, EIS_FREQ_TRIM_CAL, EIS_PHASE_ADVANCE, EIS_PH_ADV_CAL, CONVERT, and SHDN bits; removed the REF_SW Register; replaced *Typical Application Circuits;* corrected typos	1, 11–12, 14, 16–18, 21, 28, 31–39, 42–62, 65, 68, 71–72, 82, 91, 143, 126, 129–130, 133, 140, 148, 150, 159–169
4	1/23	Updated the *Package Information, Electrical Characteristics, Pin Description, Sensor ADC, Offset and Gain Calibration*, *Sensor Detect, EIS Frequency, EIS Sensor Setup, Calculating Magnitude Correction Factor*, *Applying Calibrations to an EIS Measurement*, *Avoiding Saturation, Cyclic Voltammetry Mode*, *FIFO Description, Register Details*,	2, 12, 14–20, 28–29, 39–40, 42, 45, 50, 55–57, 61–62, 70, 81–151
5	2/25	Updated the *Electrical Characteristics* and *Pin Description* sections, and updated the *BYPASS_LDO* description	16, 17, 27, 91, 92