36V, 4A/5A/6A, Fully Integrated Synchronous Silent Switcher Buck

MAX26404/MAX26405/MAX26406

General Description

The MAX26404/MAX26405/MAX26406 ICs are tiny, low EMI emission, synchronous Silent Switcher® buck converters with integrated high-side and low-side switches. The ICs are designed to deliver up to 6A with wide-input voltages range from 3V to 36V. Voltage quality can be monitored by observing the PGOOD signal. The MAX26404/MAX26405/MAX26406 can operate in dropout by running at 99% duty cycle, which makes it ideal for automotive and industrial applications.

The MAX26404/MAX26405/MAX26406 offer programmable or fixed output voltages of 5V and 3.3V. Frequency is internally fixed at 2.1MHz (or 400kHz), which allows for small external components, reduced output ripple, and guarantees no AM interference. The MAX26404/MAX26405/MAX26406 automatically enter skip mode at light loads with ultra-low quiescent current of 10µA at no load. This family of products (including the MAX26408/MAX26410) offers a pin-to-pin compatible offering from 4A to 10A in a single-phase configuration, and up to 20A in a dual-phase configuration. These devices are also optimized for dual-phase operation with very high-current sharing accuracy. These devices can be ordered with spread-spectrum frequency modulation designed to minimize EMI-radiated emissions due to the modulation frequency.

This device features the MAXQ® power architecture, which provides precision transient performance and phase margin. This allows obtaining maximum power, performance, and precision while minimizing system cost for any specific application.

The MAX26404/MAX26405/MAX26406 are available in a small 3.5mm x 3.75mm, 17-pin FC2QFN package and use very few external components.

Applications

- Point-of-Load Power Supplies
- 12V/24V Industrial Applications
- Telecom, Servers, and Networking Equipment

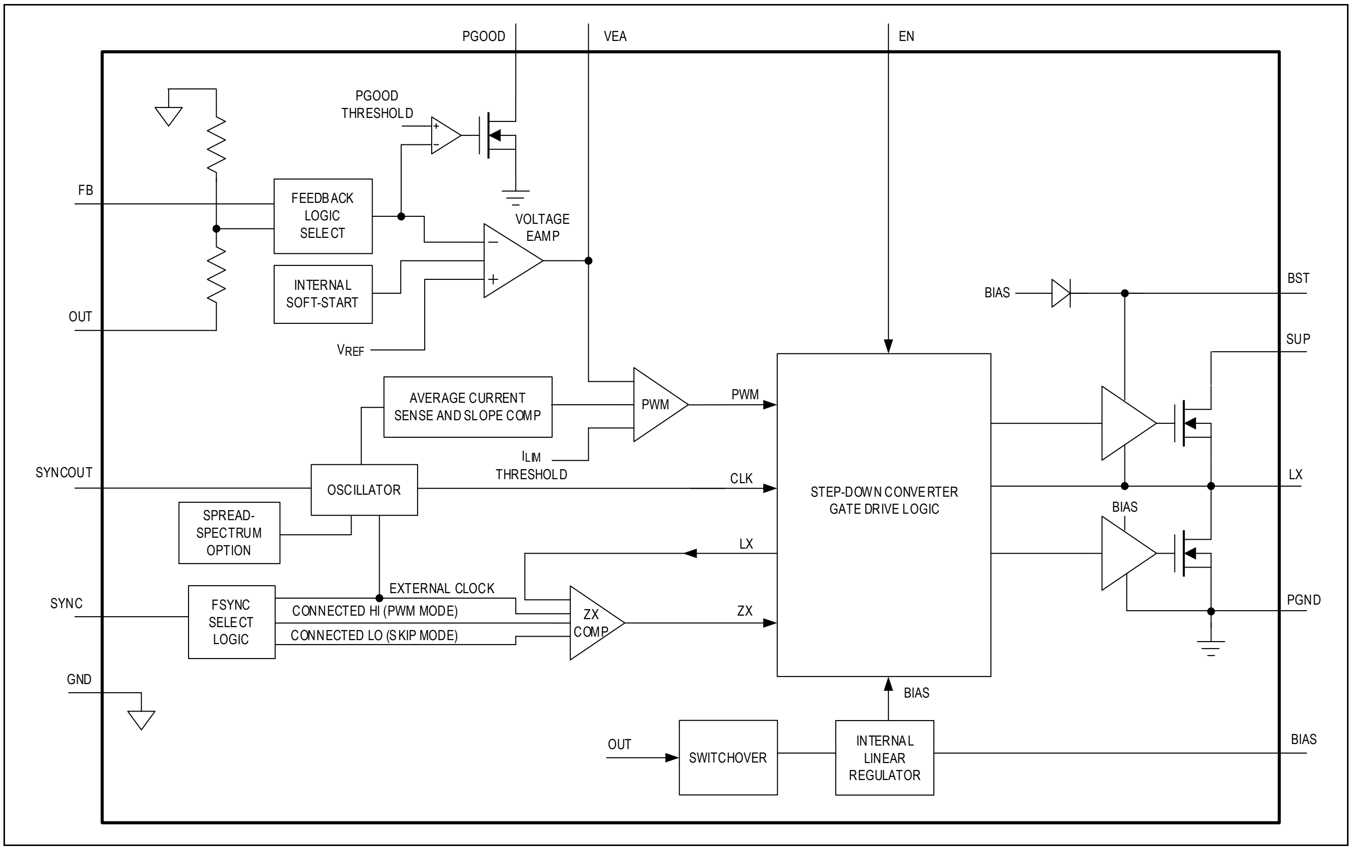
Benefits and Features

- Silent Switcher Converter
  - Enables Compact, Efficient, Low-EMI Solution
  - Spread-Spectrum Frequency Modulation
  - Symmetrical Package Offers Superior EMI Performance
- Multiple Functions for Small Size
  - Operating V_{IN} Range of 3V to 36V
  - 10µA Quiescent Current in Skip Mode
  - Synchronous DC-DC Converter with Integrated FETs
  - 400kHz and 2.1MHz Fixed-Frequency Options
  - Fixed 2.5ms Internal Soft-Start
  - Programmable 0.8V to 10V Output, or Fixed-Output Voltages of 3.3V and 5.0V
  - Other Fixed-Output Options Available between 2.9V to 6V in 100mV Steps
  - 3.5mm x 3.75mm, 17-Pin FC2QFN
- Dual-Phase Capability
  - Can Be Used in Dual-Phase Configuration for High-Power Design
  - Dynamic Current Sharing through Shared VEA Pin
  - Low-I_Q Operation Capability in Dual Phase
- High Precision
  - ±1% Output-Voltage Accuracy in FPWM Mode at No Load
  - Precise Output Voltage Monitoring with PGOOD
  - MAXQ Power Architecture
- Robust for the Environment
  - Forced-PWM and Skip-Mode Operation
  - 99% Duty-Cycle Operation with Low Dropout
  - Overtemperature and Short-Circuit Protection
  - -40°C to +125°C Operating Temperature Range

***Ordering Information* appears at end of data sheet.**

19-101814; Rev 1; 1/25

Simplified Block Diagram



Absolute Maximum Ratings

SUP	-0.3V to +42V
EN	-0.3V to +42V
BST to LX (Note 1)	-0.3V to +2.2V
BST	-0.3V to +44V
LX (Note 1)	-0.3V to SUP+0.3V
SYNCOUT	-0.3V to +6V
SYNC	-0.3V to +6V
VEA	-0.3V to BIAS+0.3V
FB	-0.3V to BIAS+0.3V
OUT	-0.3V to +16V
PGOOD	-0.3V to +6V
BIAS	-0.3V to +2.2V
PGND to AGND	-0.3V to +0.3V
LX Continuous RMS Current	6A
ESD Protection	
Human Body Model	±2kV
Charged Device Model	±750V
Continuous Power Dissipation (T_A = +70°C, derate 34.48mW/°C above +70°C)	2758mW
Operating Temperature Range	-40°C to +150°C
Storage Temperature Range	-65°C to +150°C
Soldering Temperature (Soldering 10sec)	+300°C

Note 1: Self-protected against transient voltages exceeding these limits for ≤50ns under normal operation and loads up to the maximum rated output current.

Recommended Operating Conditions

PARAMETER	SYMBOL	CONDITION	TYPICAL RANGE	UNIT
Ambient Temperature Range	T_A	—	-40 to +125	°C

***Note:** These limits are not guaranteed.*

Package Information

17 FC2QFN

Package Code	F173A3FY+6	
Outline Number	21-100343	
Land Pattern Number	90-100129	
THERMAL PARAMETERS	**JEDEC 4-LAYER BOARD**	**EV KIT 4-LAYER BOARD**
Junction-to-Ambient Thermal Resistance (θ_{JA})	38.4°C/W	28.9°C/W
Junction-to-Case (top) Thermal Resistance (θ_{JCT})	21.4°C/W	—
Junction-to-Case (bottom) Thermal Resistance (θ_{JCB})	10.4°C/W	10.2°C/W
Junction-to-Board Thermal Resistance (θ_{JB})	9.9°C/W	12.0°C/W
Junction-to-Top Characterization Parameter (ψ_{JT})	1.9°C/W	0.86°C/W
Junction-to-Board Characterization Parameter (ψ_{JB})	12.5°C/W	12.2°C/W

For the latest package outline information and land patterns (footprints), go to analog.com/en/resources/packaging-quality-symbols-footprints/package-index.html. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

Package thermal resistances were obtained using both the four-layer EV kit as well as the method described in JEDEC specification JESD51-7. For detailed information on package thermal considerations, refer to analog.com/en/resources/technical-articles/thermal-characterization-of-ic-packages.html.

Electrical Characteristics

(V_{SUP} = V_{EN} =14V, T_J = -40°C to +150°C, unless otherwise noted. Typical values are at T_A = +25°C, under normal conditions, unless otherwise noted. Note 2 and Note 3.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Supply Voltage Range	V_{SUP}		3		36	V
Supply Current	I_{SUP_SHDN}	V_{EN} = 0V, T_A = +25°C		4	6	µA
	I_{SUP}	V_{EN} = high, V_{OUT} = 3.3V, V_{FB} = V_{BIAS}, no load, no switching, T_A = +25°C		10		
SUP Undervoltage Lockout	$V_{SUP\_UVLO\_RISE}$	SUP voltage rising	2.945	3.025	3.175	V
	$V_{SUP\_UVLO\_FALL}$	SUP voltage falling	2.655	2.725	2.870	
BIAS Undervoltage Lockout	V_{BIAS_UVLO}	BIAS voltage falling	1.53	1.58	1.63	V
BIAS Undervoltage Lockout Hysteresis	$V_{BIAS\_UVLO\_HYS}$	BIAS UVLO hysteresis		50		mV
BIAS Voltage	V_{BIAS}			1.8		V
BUCK CONVERTER						
Output Voltage Accuracy	V_{OUT_5V}	Skip mode, no load	4.93	5.0	5.05	V
		PWM mode, no load	4.95	5.0	5.05	
	$V_{OUT\_3.3V}$	Skip mode, no load	3.245	3.3	3.335	
		PWM mode, no load	3.265	3.3	3.335	
Output Voltage Adjustable Range	V_{OUT}		0.8		10	V
Feedback Voltage Accuracy	V_{FB_PWM}	PWM mode, no load	0.787	0.800	0.813	V
Feedback Leakage Current	I_{FB}	V_{FB} = 0.8V, T_A = +25°C			100	nA
High-Side DMOS On-Resistance	R_{DSON_HS}	V_{BIAS} = 1.8V, I_{LX} = 2A		45	90	mΩ
Low-Side DMOS On-Resistance	R_{DSON_LS}	V_{BIAS} = 1.8V, I_{LX} = 2A		22	44	mΩ
High-Side DMOS Current-Limit Threshold	I_{LIM}	MAX26404	5.50	6.25	7.00	A
		MAX26405	6.5	7.5	8.5	
		MAX26406	7.5	8.75	10	
Low-Side DMOS Negative Current-Limit Threshold	I_{NEG}	MAX26404		-2.3		A
		MAX26405		-3		
		MAX26406		-3.5		
LX Leakage	I_{LX_LKG}	V_{SUP} = 36V, V_{LX} = 0V, or V_{LX} = 36V, T_A = +25°C			1	µA
Soft-Start Ramp Time	t_{SS}		2.2		2.8	ms
Minimum On-Time	t_{ON}	(Note 4)		33	55	ns
Maximum Duty Cycle	D_{MAX}	Dropout mode	98	99		%
SWITCHING FREQUENCY						
PWM Switching Frequency	f_{SW}	400kHz	360	400	440	kHz
		2.1MHz	1.925	2.1	2.275	MHz
	f_{SYNC}	f_{SW} = 400kHz	360		600	kHz

(V_{SUP} = V_{EN} =14V, T_J = -40°C to +150°C, unless otherwise noted. Typical values are at T_A = +25°C, under normal conditions, unless otherwise noted. *Note 2* and *Note 3*.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
SYNC External Clock Frequency		f_{SW} = 2.1MHz	1.7		2.6	MHz
Spread Spectrum	SPS	Percentage of f_{SW}		±3		%
PGOOD OUTPUT						
PGOOD Threshold	V_{PGOOD_THR}	V_{OUT} rising	92	94	96	%
	V_{PGOOD_THF}	V_{OUT} falling	91	93	95	
PGOOD Debounce Time	t_{DEB}	Rising		100		μs
		Falling		50		
PGOOD Leakage Current	I_{PGOOD_LKG}	T_A = +25°C			1	μA
PGOOD Low Voltage Level	V_{PGOOD_LOW}	Sinking 1mA			0.4	V
LOGIC LEVELS						
EN High Voltage Level	V_{EN_HIGH}		1.2			V
EN Low Voltage Level	V_{EN_LOW}				0.5	V
EN Input Current	I_{EN}	V_{EN} = V_{SUP} = 36V, T_A = +25°C			1	μA
SYNC High Voltage Level	V_{SYNC_HIGH}		1.4			V
SYNC Low Voltage Level	V_{SYNC_LOW}				0.4	V
SYNCOUT Output Voltage Level	$V_{SYNCOUT}$	No load	2.6	3.3	3.9	V
THERMAL PROTECTION						
Thermal Shutdown	T_{SHDN}			165		°C
Thermal Shutdown Hysteresis	T_{SHDN_HYS}			20		°C

Note 2: Limits are 100% tested at T_A = +25°C. Limits over the operating temperature range and relevant supply voltage are guaranteed by design and characterization. Typical values are at T_A = +25°C.

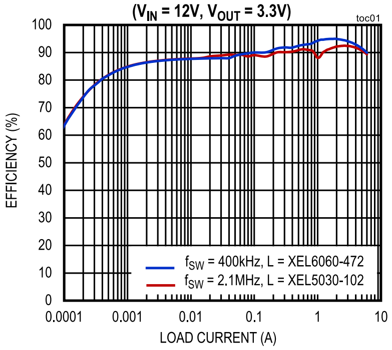
Note 3: The device is designed for continuous operation up to T_J = +125°C for 95,000 hours and T_J = +150°C for 5,000 hours.

Note 4: Guaranteed by design; not production tested.

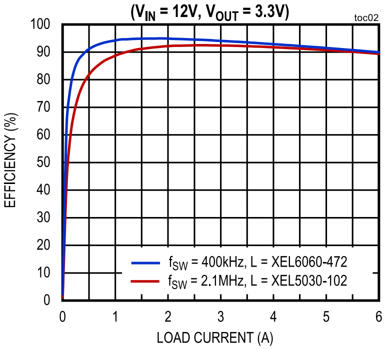
Typical Operating Characteristics

(V_{SUP} = V_{EN} = +14V, T_A = +25°C, unless otherwise noted.)

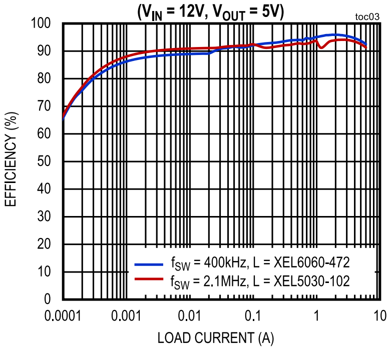
EFFICIENCY vs. LOAD CURRENT
SKIP MODE
(V_{IN} = 12V, V_{OUT} = 3.3V)



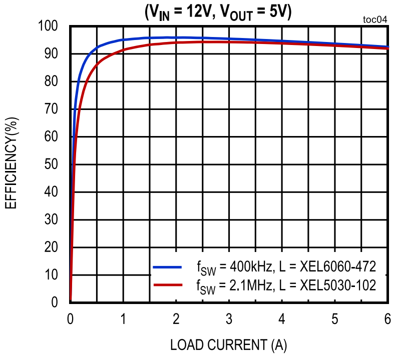
EFFICIENCY vs. LOAD CURRENT
FPWM MODE
(V_{IN} = 12V, V_{OUT} = 3.3V)



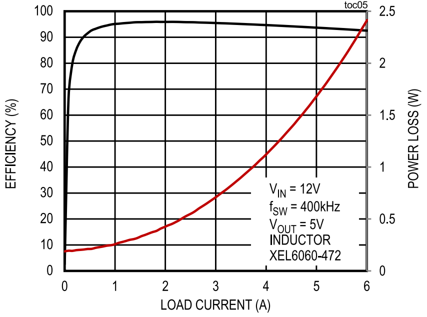
EFFICIENCY vs. LOAD CURRENT
SKIP MODE
(V_{IN} = 12V, V_{OUT} = 5V)



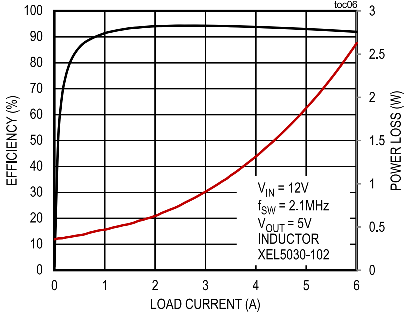
EFFICIENCY vs. LOAD CURRENT
FPWM MODE
(V_{IN} = 12V, V_{OUT} = 5V)



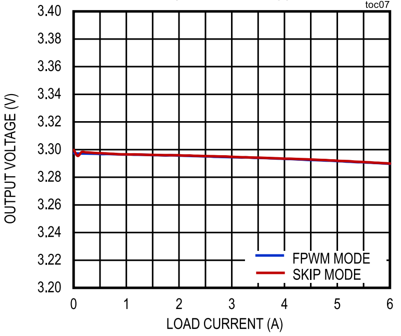
EFFICIENCY AND POWER LOSS
vs. LOAD CURRENT



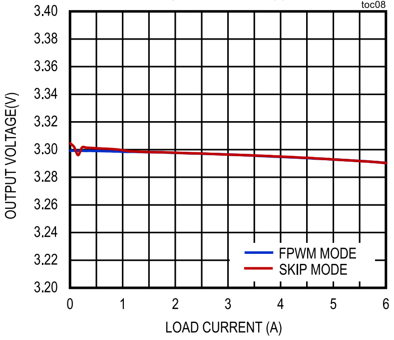
EFFICIENCY AND POWER LOSS
vs. LOAD CURRENT



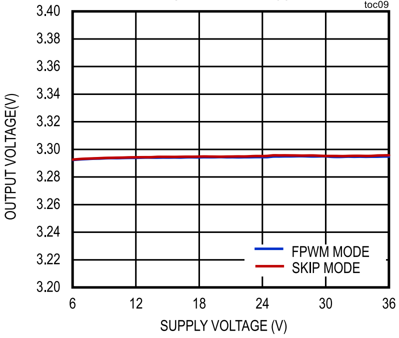
LOAD REGULATION
(V_{IN} = 14V, f_{SW} = 400kHz, V_{OUT} = 3.3V)



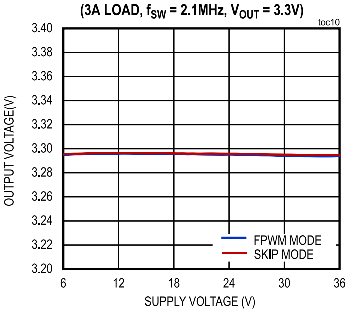
LOAD REGULATION
(V_{IN} = 14V, f_{SW} = 2.1MHz, V_{OUT} = 3.3V)



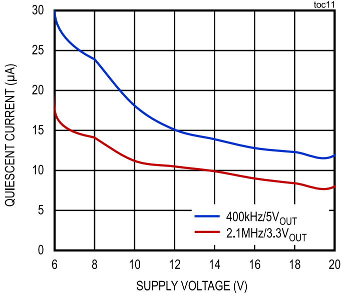
LINE REGULATION
(3A LOAD, f_{SW} = 400kHz, V_{OUT} = 3.3V)



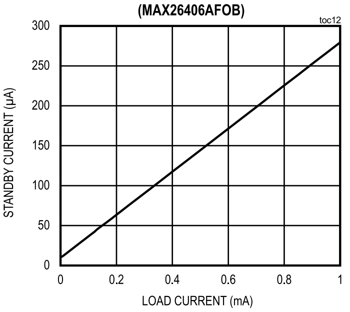
LINE REGULATION
(3A LOAD, f_{SW} = 2.1MHz, V_{OUT} = 3.3V)



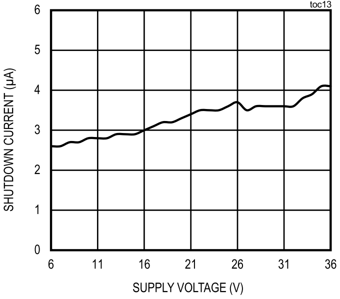
QUIESCENT CURRENT
vs. SUPPLY VOLTAGE



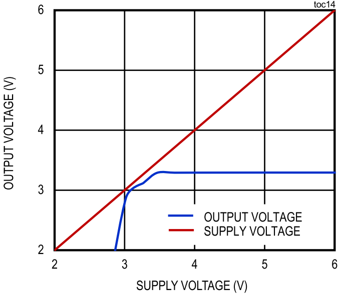
STANDBY CURRENT
vs. LOAD CURRENT
(MAX26406AFOB)



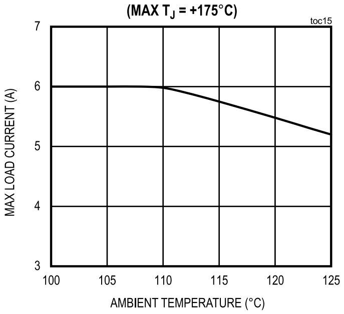
SHUTDOWN CURRENT
vs. SUPPLY VOLTAGE



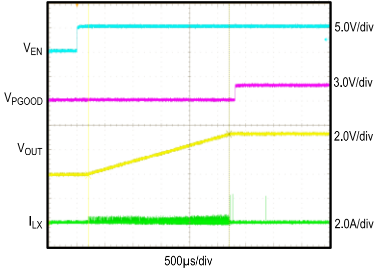
OUTPUT VOLTAGE
vs. SUPPLY VOLTAGE
FPWM MODE



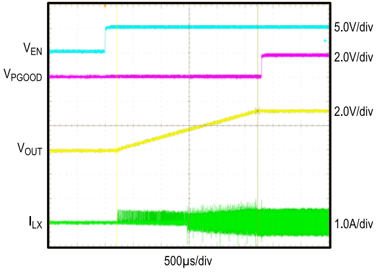
MAX LOAD CURRENT
vs. AMBIENT TEMPERATURE
(MAX T_J = +175°C)



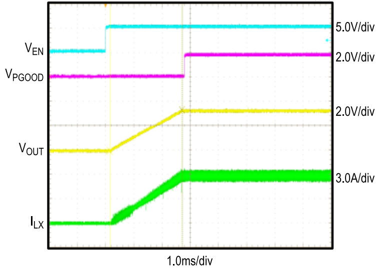
STARTUP INTO NO LOAD
(MAX26406AFOB, SKIP)



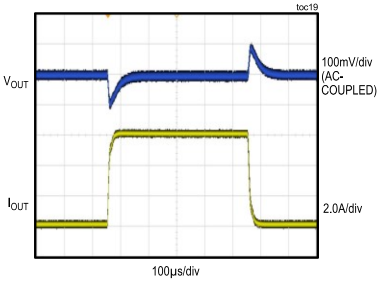
STARTUP INTO NO LOAD
(MAX26406AFOB, FPWM)



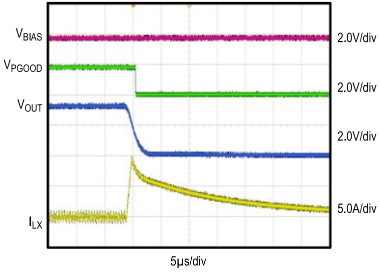
STARTUP INTO FULL LOAD
(MAX26406AFOB, FPWM)



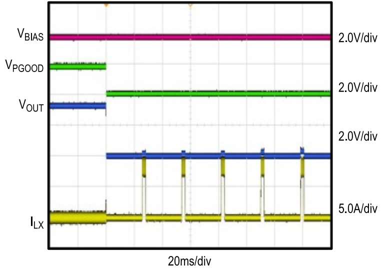
LOAD TRANSIENT
(MAX26406AFOB, C_{OUT} = 42µF EFFECTIVE)



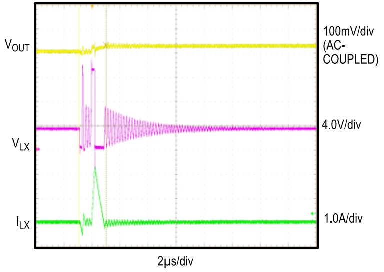
SHORT-CIRCUIT RESPONSE
(MAX26406AFOB)



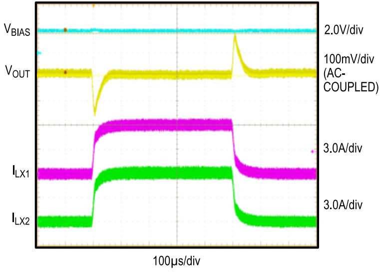
HICCUP MODE
(MAX26406AFOB)



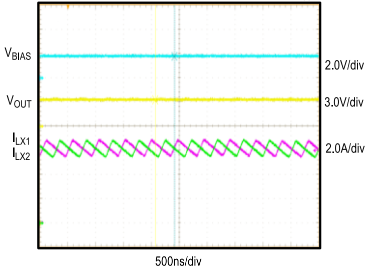
SKIP MODE, NO LOAD OPERATION (MAX26406AFOB)



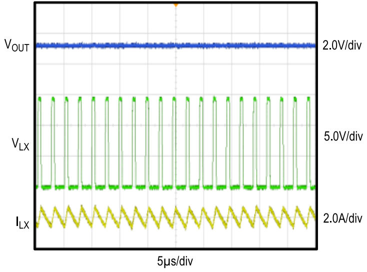
DUAL-PHASE LOAD TRANSIENT (MAX26406AFOB)



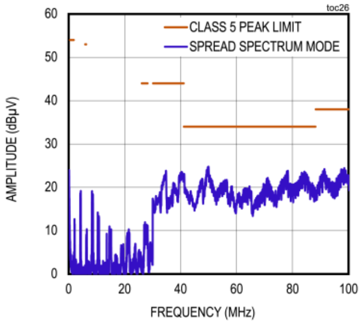
DUAL-PHASE CURRENT SHARING (MAX26406AFOB)



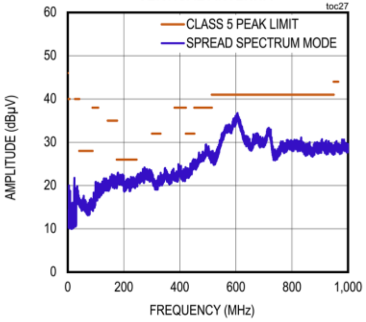
STEADY-STATE SWITCHING WAVEFORM (MAX26406AFOB)



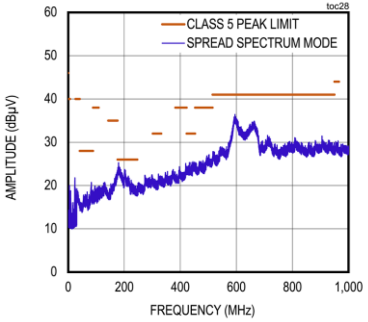
CONDUCTED EMI PERFORMANCE (CISPR25 WITH CLASS 5 PEAK LIMITS)



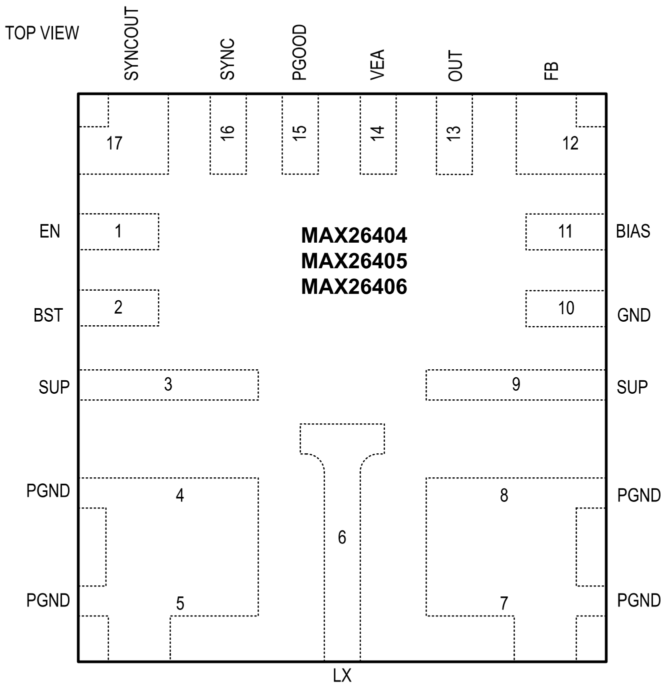
RADIATED EMI PERFORMANCE (CISPR25 WITH CLASS 5 PEAK LIMITS) VERTICAL ANTENNA



RADIATED EMI PERFORMANCE (CISPR25 WITH CLASS 5 PEAK LIMITS) HORIZONTAL ANTENNA



Pin Configurations



17 FC2QFN
(3.5mm x 3.75mm)

Pin Descriptions

PIN	NAME	FUNCTION
1	EN	High-Voltage-Compatible Input for Circuit Activation. If this pin is low, the part is off.
2	BST	High-Side Driver Supply. Connect a 0.1µF capacitor between LX and BST for proper operation.
3,9	SUP	IC Supply Input. Connect a 1µF or larger ceramic capacitor in parallel with a 4.7µF cap from SUP to PGND.
4,5,7,8	PGND	Power Ground. Connect all PGND pins together.
6	LX	BUCK Switching Node. High impedance when part is off. Connect LX to the switched side of the appropriate inductor.
10	GND	Analog Ground.
11	BIAS	1.8V Internal BIAS Supply. Connect a minimum of 2µF ceramic capacitor to PGND.
12	FB	Feedback Pin. Connect a resistor-divider from OUT to FB to GND for external adjustment of output voltage. Connect to BIAS for internal fixed voltages.
13	OUT	Buck Regulator Output Voltage-Sense Input. Connect OUT to the buck output.
14	VEA	Internal Voltage Loop Error-Amplifier Output. Connect to VEA of the target for dual-phase operation. Leave unconnected for single-phase operation.
15	PGOOD	Open-Drain Reset Output. External pull-up required.
16	SYNC	SYNC. If connected to GND, skip-mode operation is enabled under light loads. If connected to BIAS, forced-PWM mode is enabled.
17	SYNCOUT	180° Out-of-Phase Clock Output for Multiphase Operation. Leave SYNCOUT open for single-phase operation.

Detailed Description

The MAX26404/MAX26405/MAX26406 are small, synchronous buck converters with integrated high-side and low-side switches. These devices are designed to deliver up to 6A with input voltages from +3V to +36V while using only 10μA quiescent current at no load (V_{SUP} = 12V, V_{OUT} = 3.3V). Voltage quality can be monitored by observing the PGOOD signal. The ICs can operate in dropout by running at 99% duty cycle, which makes them ideal for automotive and industrial applications.

The MAX26404/MAX26405/MAX26406 offer fixed output voltages (for more details, see the *Ordering Information* table) or an FB pin for an external resistor-divider. The frequency is internally fixed at 2.1MHz or 400kHz, which allows for small external components and reduced output ripple, and guarantees no AM interference. The device automatically enters skip mode (SYNC pin pulled low) at light loads with an ultra-low-quiescent current of 10μA at no load. It can be ordered with spread-spectrum frequency modulation designed to minimize EMI-radiated emissions due to the modulation frequency. The architecture is an average current-mode control that allows much better noise rejection of the current loop. The IC comes with a small minimum on time of 33ns to allow for large step-down ratios in single stage without skipping cycles.

The devices can also be used in a dual-phase configuration with the help of SYNCOUT and VEA. An innovative average current-mode control architecture provides noise immunity and accurate dynamic current sharing during transients. High-power designs with up to 12A of output current can be enabled with integrated switches using the IC's dual-phase capability. FC2QFN provides improved thermal and EMI performance. Symmetrical pinout across V_{IN} and PGND further improves the EMI performance, which enables low-noise designs.

Multiphase Operation

The MAX26404/MAX26405/MAX26406 are capable of dual-phase operation for high-current applications and each IC can be configured as a controller or a target. The multiphase operation is intended for forced-PWM mode only. SYNCOUT is 180° out-of-phase with the controller clock. If the device is in skip mode, then no clock is present on SYNCOUT. To enable low-I_Q operation in dual-phase configuration, disable the EN of the target to turn OFF the IC and save quiescent current.

For a target, connect SYNCOUT to BIAS. When EN is high, there is a procedure to detect if the IC is a controller (SYNCOUT not connected to BIAS) or a target. The VEA pin is the voltage-error amplifier output for the controller or the current-error amplifier input for the target. Connect the controller VEA pin to the target VEA pin to ensure balanced current sharing between two phases. The controller and target FB pins must be connected to their respective BIAS pins for internal fixed V_{OUT} setting. Since the target IC uses the outer voltage loop of the controller (through the VEA pin), the internal resistor-divider of the target IC is not used, and any mismatch in the output voltage is avoided. For a dual-phase configuration setup using the MAX26404/MAX26405/MAX26406, see *Figure 1*.

For external resistor-divider configurations, use two separate resistor-dividers for each IC to avoid the FB pins of the controller and target being connected together at the same point.

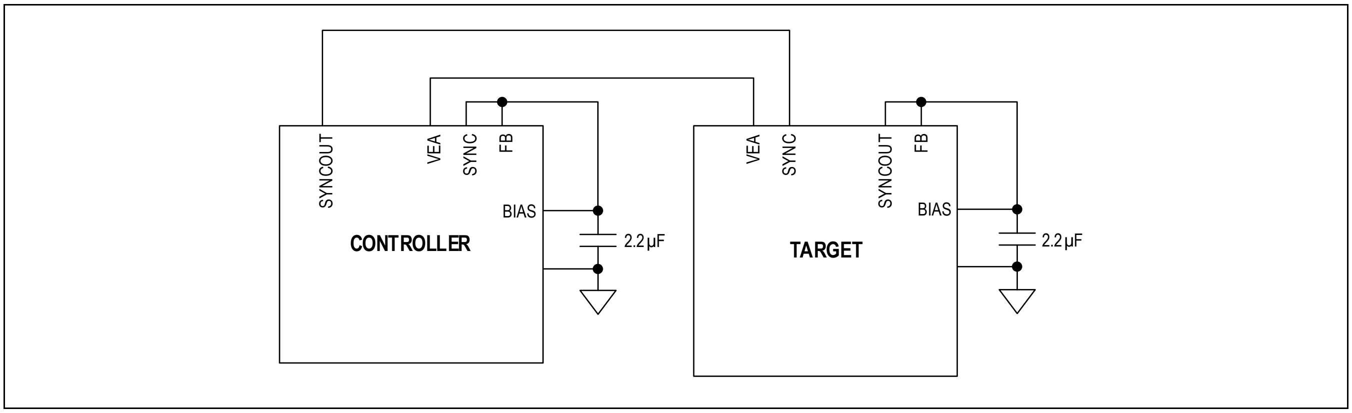


Figure 1. Typical Dual-Phase Configuration Setup Using Fixed Internal V_{OUT} Setting

Linear Regulator Output (BIAS)

The device includes a 1.8V linear regulator (V_{BIAS}) that provides power to the internal circuit blocks. Connect a 2.2μF ceramic capacitor from BIAS to GND. During startup, the bias regulator draws power from the input and switches over to the output after the startup is complete (if V_{OUT} > 2.5V). For output voltages less than 1.8V, the bias regulator is always connected to the input.

System Enable (EN)

An enable control input (EN) activates the devices from their low-power shutdown mode. EN is compatible with inputs from automotive battery level down to 3V. EN turns on the internal linear (BIAS) regulator. Once V_{BIAS} is above the internal lockout threshold (V_{UVBIAS} = 1.63V (typ)), the converter activates and the output voltage ramps up with the programmed soft-start time.

A logic-low at EN shuts down the device. During shutdown, the BIAS regulator and gate drivers turn off. Shutdown is the lowest power state and reduces the quiescent current to 4μA (typ). Drive EN high to bring the device out of shutdown.

Synchronization Input (SYNC)

The MAX26404/MAX26405/MAX26406 include a SYNC pin, which is a logic-level input used for operating-mode selection and frequency control. Connecting SYNC to BIAS or to an external clock enables forced fixed-frequency (FPWM) operation. Connecting SYNC to GND enables automatic skip-mode operation for better light-load efficiency. The ICs synchronize to an external clock at the rising edge applied at the SYNC pin. The devices synchronize to the external clock in two cycles. When the external clock signal at SYNC is absent for more than two clock cycles, the devices use the internal clock.

Soft-Start

The devices include a fixed, internal 2.5ms soft-start. Soft-start limits startup inrush current by forcing the output voltage to ramp up towards its regulation point.

Spread-Spectrum Option

The ICs feature enhanced EMI performance with a spread-spectrum option, which is available as a factory option. When spread spectrum is enabled, the operating frequency is varied at ±3% centered at the switching frequency. The modulation signal is a triangular wave with 4.5kHz frequency at 2.1MHz. Therefore, the switching frequency ramps down 3% and back to 2.1Mhz in 110μs, and also ramps up 3% and back to 2.1MHz in 110μs, after which the cycle repeats. For operation at 400kHz, the modulation signal scales proportionally to 0.4/2.1. The internal spread spectrum is disabled if the devices are synchronized to an external clock. However, the devices do not filter the input clock in SYNC and pass any modulation (including spread spectrum) present on the the driving eternal clock.

Short-Circuit Protection

The devices feature a current limit that protects them against short-circuit and overload conditions at the output. In the event of a short-circuit or overload condition, the high-side MOSFET remains on until the inductor current reaches the specified LX current-limit threshold. The converter then turns the high-side MOSFET off and the low-side MOSFET on to allow the inductor current to ramp down. Once the inductor current crosses below the current-limit threshold, the converter turns on the high-side MOSFET again. This cycle repeats until the short or overload condition is removed.

A hard short is detected when the output voltage falls below 50% of the target (for fixed internal output) or 25% of the target (for external output) while in current limit. If this occurs, hiccup mode activates, and the output turns off for 25ms. The output then enters soft-start and powers back up. This repeats indefinitely while the short circuit is present. Hiccup mode is disabled during soft-start.

Applications Information

Setting the Output Voltage

Connect FB to BIAS for a fixed 5V or 3.3V output voltage. To set the output to other voltages between 0.8V and 10V, connect a resistor-divider from the output (OUT) to GND (see *Figure 2*). Select R_{FB2} (FB to GND resistor) less than or equal to 100kΩ. Calculate R_{FB1} (OUT to FB resistor) with the following equation:

Equation 1:

$$R_{FB1} = R_{FB2} \times \left(\frac{V_{OUT}}{V_{FB}} - 1\right)$$

where V_{FB} is the feedback regulation voltage. For more details, see the *Electrical Characteristics* table.

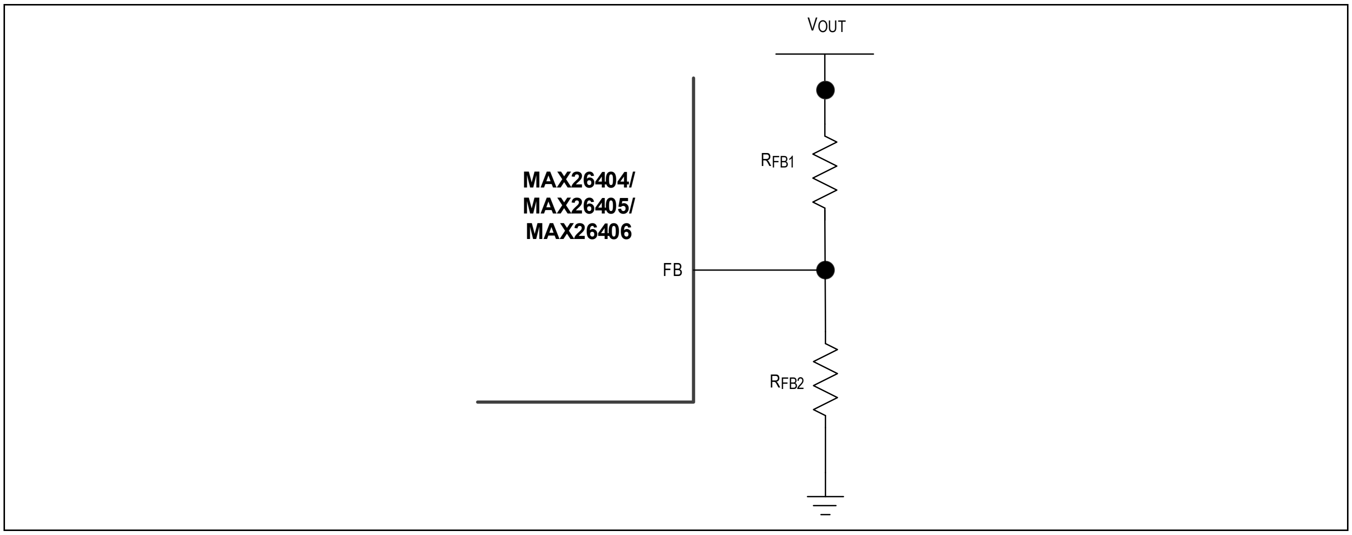


Figure 2. Output Voltage Setting Using External Resistor-Divider

Table 1 provides components selection recommendations for each output range for the adjustable-output configuration. Recommendations can be further optimized for specific applications. The C_{FF} values listed in *Table 1* are recommended based on R_{FB1} = 100kΩ. The C_{FF} recommendation changes with the R_{FB1} selection.

Table 1. Recommended Components for Adjustable Output Voltage

SWITCHING FREQUENCY (kHz)	V_{OUT} (V)	INDUCTOR (µH)	MINIMUM EFFECTIVE C_{OUT} (µF)	C_{FF} (pF)
400	0.8 to 1.8	1.5	440	100
	1.8 to 3	3.3	440	100
	3 to 5	3.3	150	47
	5 to 10	4.7	90	100
2100	0.8 to 3	0.56	235	10
	3 to 5	1	50	15
	5 to 10	1	44	27

Dual-Phase Operation

Low-I_Q Operation in Dual Phase

The MAX26404/MAX26405/MAX26406 come with dual-phase capability where each IC can be either configured as a controller or target. The SYNCOUT pin of the controller outputs a 180° out-of-phase clock when SYNC is connected high (FPWM mode). For low-I_Q mode, the SYNC pin of the controller must be pulled low (skip mode). In this mode, there is no clock present on SYNCOUT pin of the controller, and the controller IC enters skip mode. The internal circuit of the target IC remains ON during this time and actively looks for the SYNCOUT signal from the controller. Since the target IC is ON, the quiescent current is slightly higher, even though both of the ICs skip pulses.

To improve the light-load efficiency and further reduce the I_Q, the target EN must be pulled low. This disables the target and its internal circuits, which further reduces the I_Q. *Table 2* summarizes the truth table for low-I_Q operation.

Table 2. Configurations for Low-I_Q Operation

CONTROLLER	TARGET	MODE
EN = High, SYNC = BIAS	EN = High	FPWM (high I_Q)
EN = High, SYNC = Low	EN = High	Skip mode (low I_Q)
EN = High, SYNC = Low	EN = Low	Standby mode (ultra-low I_Q)
EN = Low	EN = High	Not allowed

Setting Output Voltage

For setting the output voltage to internal fixed voltage, order the same fixed V_{OUT} setting for both controller and target ICs and connect the FB pin to its respective BIAS. Note that do not connect the FB pins of the controller and target together.

For setting the output voltage to a value other than the available fixed V_{OUT} options, connect a resistor-divider between OUT, FB, and GND as shown in Figure 3. An identical but separate resistor-divider for the controller and target is recommended.

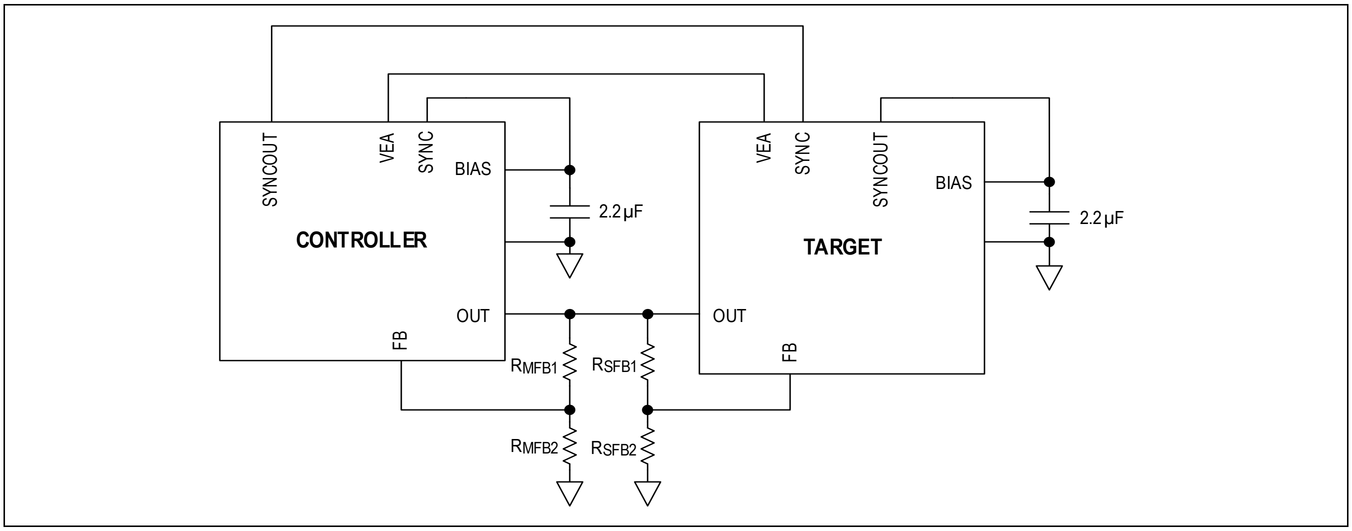


Figure 3. Typical Application Circuit for Dual-Phase Configuration with External Resistor-Divider

Inductor Selection

The inductor design is a compromise between the size, efficiency, control-loop bandwidth, and stability of the converter. An insufficient inductance value increases the inductor current ripple, which causes higher conduction losses and higher output voltage ripple. Since the slope compensation is fixed internally for the MAX26404/MAX26405/MAX26406, it might also cause current-mode-control instability to appear. A large inductor reduces the ripple, but increases the size and cost of the solution and slows the response. Table 3 provides optimized inductance values for each switching frequency. The nominal standard value selected must be within ±30% of the specified inductance.

Table 3. Inductor Selection for Fixed Output Voltage

SWITCHING FREQUENCY	INDUCTOR (μH)
400kHz	4.7
2.1MHz	1.0

Input Capacitor

The input filter capacitor reduces peak currents drawn from the power source and reduces noise and voltage ripple on the input caused by the circuit's switching. The MAX26404/MAX26405/MAX26406 incorporate a symmetrical pinout that can be leveraged for better EMI performance. Connect two high-frequency 0603 or smaller capacitors on two SUP pins on either side of the package for good EMI performance. Connect a high-quality, 4.7μF (or larger) low-ESR ceramic capacitor on the SUP pin for low-input voltage ripple.

A bulk capacitor with higher ESR (such as an electrolytic capacitor) is also typically required to reduce the Q of the front-end circuit and provide the remaining capacitance needed to minimize input-voltage ripple. The input capacitor RMS current requirement (I_{RMS}) is defined by the following equation:

Equation 2:

$$I_{RMS} = I_{LOAD(MAX)} \times \left(\frac{\sqrt{V_{OUT} \times (V_{SUP} - V_{OUT})}}{V_{SUP}} \right)$$

I_{RMS} has a maximum value when the input voltage equals twice the output voltage:

$$V_{SUP} = 2 \times V_{OUT}$$

Therefore:

$$I_{RMS} = \frac{I_{LOAD(MAX)}}{2}$$

Choose an input capacitor that exhibits less than +10°C self-heating temperature rise at the RMS input current for optimal long-term reliability. The input-voltage ripple consists of ΔV_Q (caused by the capacitor discharge) and ΔV_{ESR} (caused by the ESR of the capacitor). Use low-ESR ceramic capacitors with high ripple-current capability at the input. Assume the contribution from the ESR and capacitor discharge equal to 50%. Calculate the input capacitance and ESR required for a specified input voltage ripple using the following equations:

Equation 3:

$$ESR_{IN} = \frac{\Delta V_{ESR}}{I_{OUT} + {}^{\Delta I_L}/_{2}}$$

where:

$$\Delta I_L = \frac{(V_{SUP} - V_{OUT}) \times V_{OUT}}{V_{SUP} \times f_{SW} \times L}$$

and:

$$C_{IN} = \frac{I_{OUT} \times D(1 - D)}{\Delta V_Q \times f_{SW}}$$

$$D = \frac{V_{OUT}}{V_{SUP}}$$

where:

I_{OUT} = Maximum output current

D = Duty cycle

Output Capacitor

Output capacitance is selected to satisfy the output load-transient, output voltage ripple, and closed-loop stability requirements. During a load step, the output current changes almost instantaneously, whereas the inductor is slow to react. During this transition time, the load-charge requirements are supplied by the output capacitor, which causes an undershoot/overshoot in the output voltage. For a buck converter that is controlled by inductor current, as employed in the MAX26404/MAX26405/MAX26406, the output capacitance also affects the control-loop stability. The output ripple is composed of ΔV_Q (caused by the capacitor discharge) and ΔV_{ESR} (caused by the ESR of the output capacitor). Use low-ESR ceramic or aluminum electrolytic capacitors at the output. For an aluminum electrolytic capacitors, the entire output ripple is contributed by ΔV_{ESR}. Use Equation 4 to calculate the ESR requirement and choose the capacitor accordingly. If using ceramic capacitors, assume the contribution to the output-ripple voltage from the ESR and the capacitor discharge to be equal. The following equations show the output capacitance and ESR requirement for specified output-voltage ripple.

Equation 4:

$$ESR = \frac{\Delta V_{ESR}}{\Delta I_{P-P}}$$

$$C_{OUT} = \frac{\Delta I_{P-P}}{8 \times \Delta V_Q \times f_{SW}}$$

where:

$$\Delta I_{P-P} = \frac{(V_{IN} - V_{OUT}) \times V_{OUT}}{V_{IN} \times f_{SW} \times L}$$

$$V_{OUT\_RIPPLE} = \Delta V_{ESR} + \Delta V_Q$$

ΔI_{P-P} is the peak-to-peak inductor current as calculated above, and f_{SW} is the converter's switching frequency.

The output capacitor supplies the step-load current until the converter responds with a greater duty cycle. The resistive drop across the output capacitor's ESR and the capacitor discharge causes a voltage droop during a step load. Use a combination of low-ESR tantalum and ceramic capacitors for better transient-load and ripple/noise performance. Keep the maximum output-voltage deviations below the tolerable limits of the electronics being powered. When using a ceramic capacitor, assume an 80% and 20% contribution from the output-capacitance discharge and the ESR drop, respectively. Use the following equations to calculate the required ESR and capacitance value:

Equation 5:

$$C_{OUT} = \frac{\Delta I}{\Delta V \times 2\pi \times f_C}$$

where ΔI is the load change, ΔV is the allowed voltage droop, and f_C is the loop crossover frequency, which can be assumed to be the lesser of $f_{SW}/10$ or 100kHz. Any calculations involving C_{OUT} should consider capacitance tolerance, temperature, and voltage derating. The values in *Table 4* are actual capacitances after considering these factors.

For optimal phase margin, the recommended output capacitances are shown in *Table 4*. The output capacitance can be optimized for specific applications. If a lower or higher output capacitance is required for the application, contact the factory for an optimized solution.

Table 4. Output Capacitance Selection – Fixed Output Voltage

FREQUENCY	EFFECTIVE C_{OUT} (µF)
400kHz	100
2.1MHz	50

PCB Layout Guidelines

Careful PCB layout is critical to achieve low switching losses and clean, stable operation. For better noise immunity and power dissipation, use a multilayer board whenever possible. For good PCB layout, see Figure 4 and the following guidelines:

1) Use the correct footprint for the IC and place as many copper planes as possible under the IC footprint to ensure the efficient heat transfer.

2) Place the ceramic input-bypass capacitors, C_{BP} and C_{IN}, as close as possible to the SUP and PGND pins on both sides of the IC. Use low-impedance connections (no vias or other discontinuities) between the capacitors and IC pins. C_{BP} must be located closest to the IC and should have very good high-frequency performance (small package size and high capacitance). This provides the best EMI rejection and minimize internal noise on the device, which can degrade performance.

3) Place the inductor (L), output capacitors (C_{OUT}), bootstrap capacitor (C_{BST}), and BIAS capacitor (C_{BIAS}) in such a way as to minimize the area enclosed by the current loops. Place the inductor (L) as close as possible to the IC LX pin and minimize the area of the LX node. Place the output capacitors (C_{OUT}) near the inductor so that the ground side of C_{OUT} is near the C_{IN} ground connection to minimize the current-loop area. Place the BIAS capacitor (C_{BIAS}) next to the BIAS pin.

4) Place the bootstrap capacitor C_{BST} close to the IC and use short wide traces to minimize the loop area to minimize the parasitic inductance. Use the nearest layer for return trace (C_{BST} to LX) to minimize the inductance further. For the optimum design, refer to the *MAX26406 EV kit PCB Layout* section in the MAX26406 Evaluation Kit user guide. High parasitic inductance can impact switching speed (increase switching losses) and cause high dv/dt noise.

5) Use a continuous copper ground plane on the layer next to the IC to shield the entire circuit. Ground must also be poured around the entire circuit on the top side. Ensure that all heat-dissipating components have adequate connections to copper for cooling. Use multiple vias to interconnect ground planes/areas for low impedance and maximum heat dissipation. Place vias at the PGND terminals of the IC and input/output/ bypass capacitors. Do not separate or isolate PGND and ground connections with separate planes or areas.

6) Place the feedback resistor-divider (if used) near the IC and route the feedback and OUT connections away from the inductor and LX node and other noisy signals.

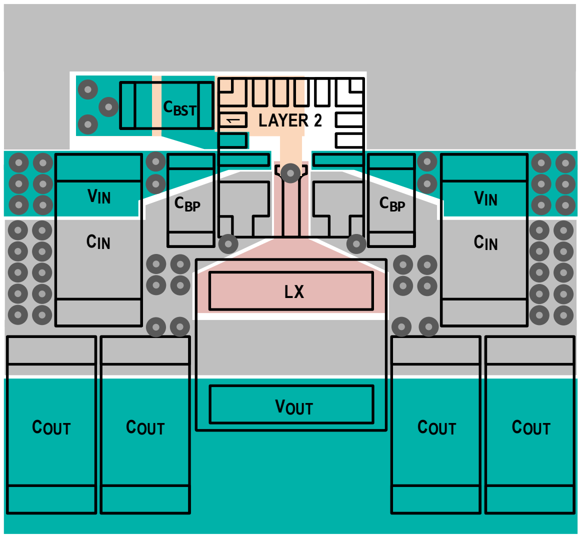
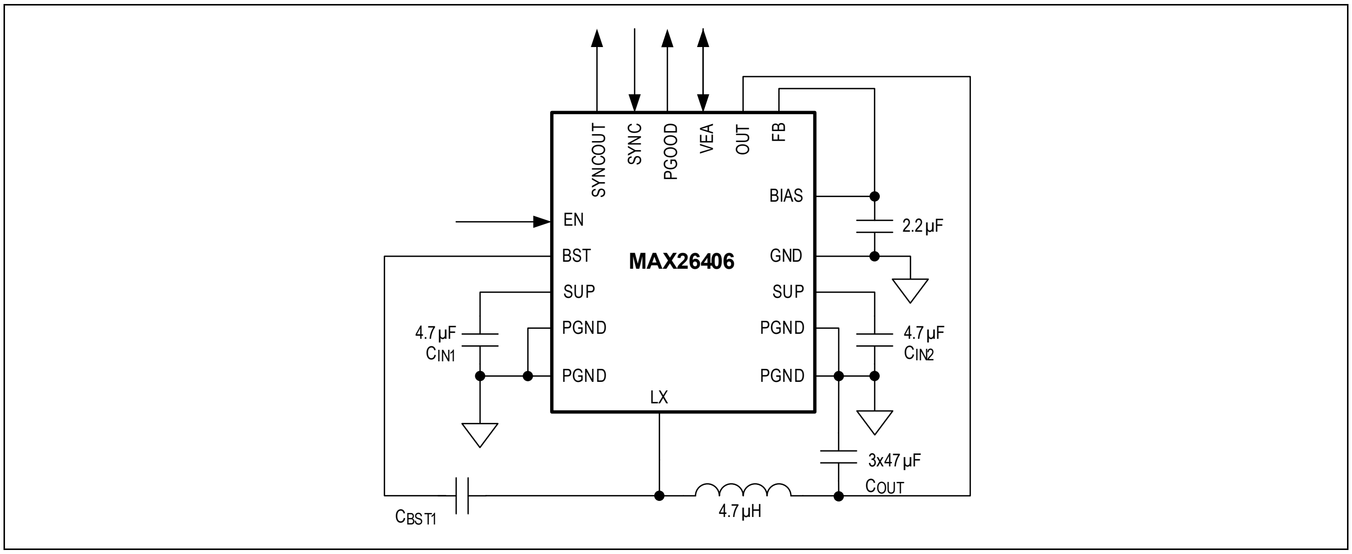


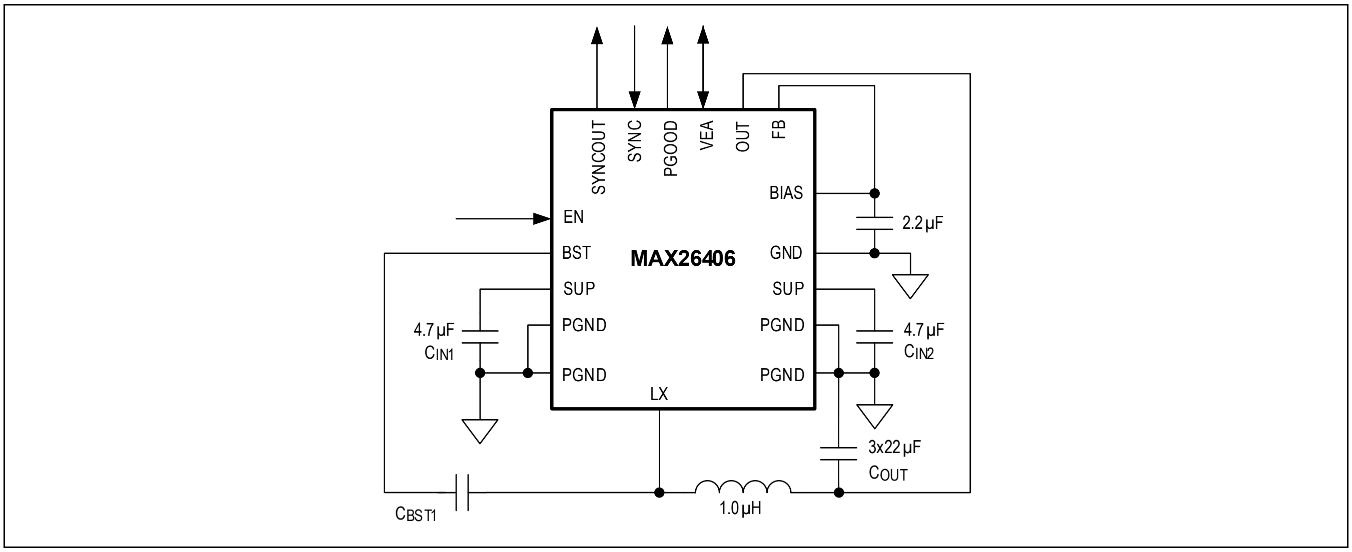
Figure 4. PCB Layout Example

Typical Application Circuits

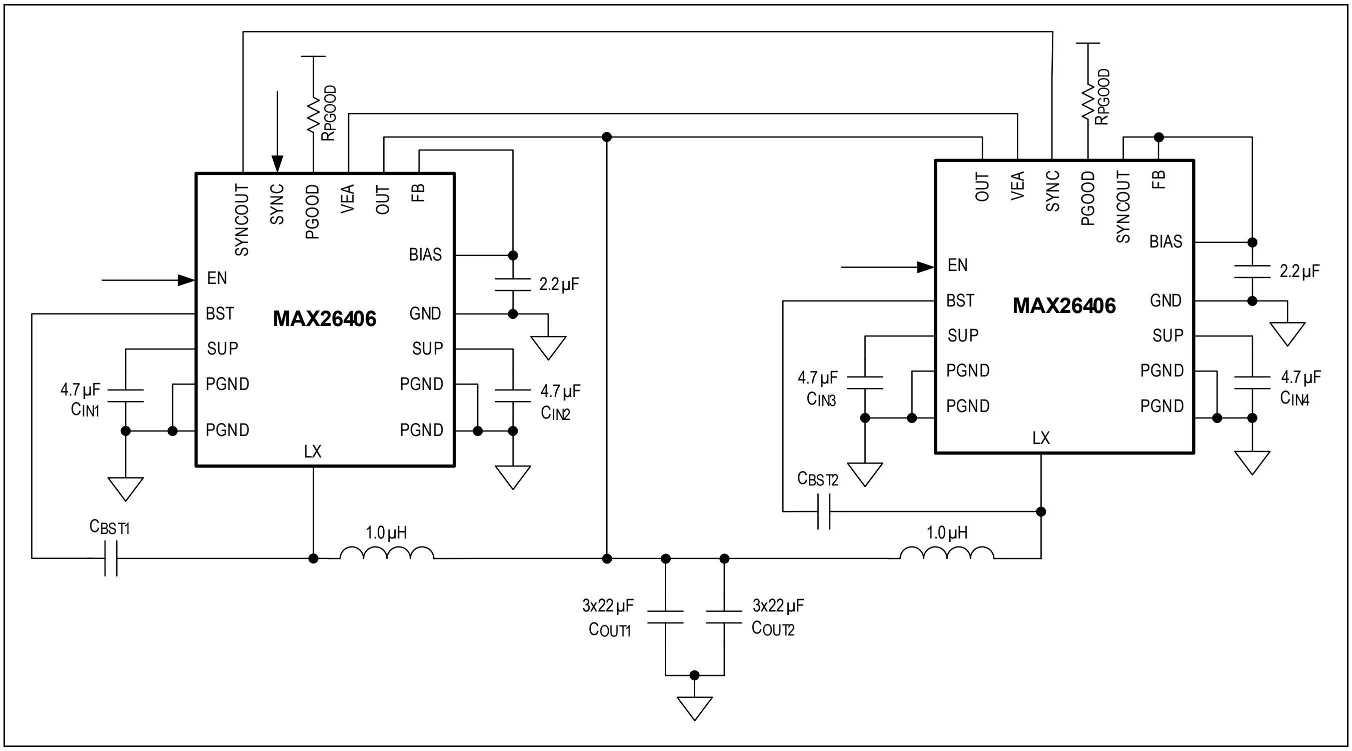
Single-Phase, 400kHz, 6A Operation



Single-Phase, 2.1MHz, 6A Operation



Dual-Phase, Controller-Target 2.1MHz 12A Operation



Ordering Information

PART NUMBER	V_{OUT} (FB TIED TO BIAS)[1]	MAXIMUM LOAD CURRENT (A)	FREQUENCY (kHz)	SPREAD SPECTRUM[2]	PACKAGE CODE
MAX26404AFOAY+	5	4	2100	ON	F173A3FY+6
MAX26404AFOBY+	3.3	4	2100	ON	F173A3FY+6
MAX26404AFOCY+	5	4	400	ON	F173A3FY+6
MAX26404AFODY+	3.3	4	400	ON	F173A3FY+6
MAX26405AFOAY+	5	5	2100	ON	F173A3FY+6
MAX26405AFOBY+	3.3	5	2100	ON	F173A3FY+6
MAX26405AFOCY+	5	5	400	ON	F173A3FY+6
MAX26405AFODY+	3.3	5	400	ON	F173A3FY+6
MAX26406AFOAY+	5	6	2100	ON	F173A3FY+6
MAX26406AFOBY+	3.3	6	2100	ON	F173A3FY+6
MAX26406AFOCY+	5	6	400	ON	F173A3FY+6
MAX26406AFODY+	3.3	6	400	ON	F173A3FY+6

+ Denotes a lead(Pb)-free/RoHS-compliant package.

Y = Side-wettable package.

[1] *Other fixed-output voltages between 2.9V to 6V with 100mV step are available; for custom requests, contact the factory.*

[2] *All ICs have with spread spectrum turned ON as the default. Contact the factory for spread-spectrum OFF parts.*

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	6/24	Release for market intro	—
1	1/25	Added MAXQ	1