Dual 36V, 8A Synchronous Buck Converters with Multiphase Capability and ASIL B Safety Level

MAX25254/MAX25255

General Description

The MAX25254/MAX25255 are small, synchronous dual buck converters with integrated high-side and low-side switches. The ICs are designed to deliver up to 8A per channel with input voltages from 3V to 36V while using only 12µA quiescent current at no load. Voltage quality can be monitored by observing the PGOOD signals. The MAX25254/MAX25255 can regulate the output voltage in the dropout region by running at 99% of the duty cycle, making them ideal for automotive and industrial applications.

The MAX25254/MAX25255 offer fixed and adjustable output voltage options. Four fixed frequency options allow for small external components and reduced output ripple, and also guarantee no AM interference. The MAX25254/MAX25255 can enter skip mode at light loads with ultra-low quiescent current of 12µA at no load. The MAX25254/MAX25255 can be ordered with spread spectrum enabled for optimum EMI performance.

Two buck converters within the MAX25254D and MAX25255D can be configured for dual-phase operation with up to 16A output load capability. Furthermore, the MAX25254D/MAX25255D and the MAX25254Q can be used in parallel to provide quad-phase operation that supports up to 32A (max) output current.

The MAX25254/MAX25255 features the MAXQ® power architecture, which provides precision transient performance and phase margin. This allows obtaining maximum power, performance, and precision while minimizing system cost for any specific application.

The MAX25254/MAX25255 are available in a small, 4.50mm x 5.75mm, 23-pin FC2QFN package and use very few external components.

Applications

- Front-End Power Supply for Head Units
- ASIL Applications
- General-Purpose Dual Buck Converters
- Telematics Modules
- Front Camera Power

Benefits and Features

Dual Buck Converter

- Wide Input Range from 3.0V to 36V (42V, max)
- Low Shutdown Supply Current (6.5µA, max)
- Low Operating Quiescent Current with One Channel ON (12µA, typ)
- Programmable V_{OUT} from 0.8V to 14V
- Up to 8A per Channel
- 180° Out-of-Phase Operation between Two Converters
- 24ns (typ) Minimum On-Time
- MAXQ Power Architecture

Dual/Quad-Phase Operation

- Ability to Operate Two ICs in Parallel for Quad-Phase Operation
- ±10% Current Sharing Accuracy
- Supports up to 16A in Dual-Phase and 32A in Quad-Phase

Diagnostics and Redundant Circuits (MAX25255)

- ASIL B Compliant
- Redundant Reference
- Die Temperature Monitor
- Precision Overvoltage and Undervoltage Protection

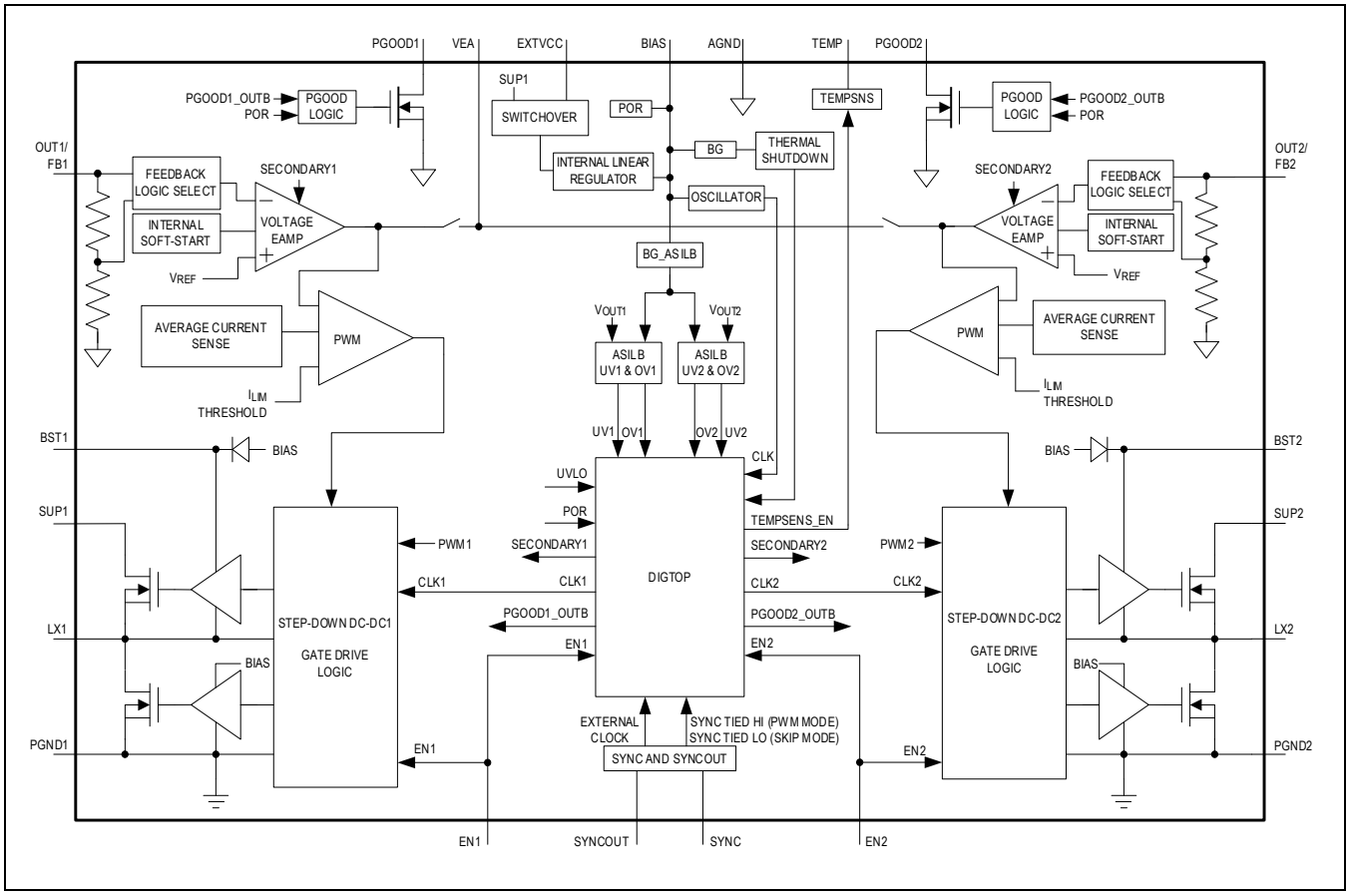
General

- 23-Pin, 4.50mm x 5.75mm FC2QFN Package
- -40°C to +125°C Operating Ambient Temperature
- AEC-Q100 Rating
- 200kHz, 400kHz, 1MHz, or 2MHz Switching Frequency Options
- Spread Spectrum

***Ordering Information* appears at end of data sheet.**

19-101441; Rev 12; 8/25

Simplified Block Diagram



Absolute Maximum Ratings

SUP_, EN_ to PGND_ ..... -0.3V to +42V
BST_ to LX_ ..... -0.3V to +2.2V
BST_ to PGND_ ..... -0.3V to +44V
LX_ to PGND_ ..... -0.3V to SUP_+0.3V
SYNCOUT, SYNC to AGND ..... -0.3V to +6V
PGOOD1, PGOOD2 to AGND ..... -0.3V to +6V
OUT1/FB1, OUT2/FB2 to AGND ..... -0.3V to +6V
VEA, TEMP to AGND ..... -0.3V to BIAS+0.3V
EXTVCC to AGND ..... -0.3V to +16V
PGND_ to AGND ..... -0.3V to +0.3V
BIAS, SPS to AGND ..... -0.3V to +2.2V
LX_ Continuous RMS Current 10A
ESD Protection (Human Body Model) ..... ±2kV
Operating Junction Temperature Range ..... -40°C to +150°C
Storage Temperature Range ..... -65°C to +150°C
Lead Temperature (soldering, 10s) ..... +300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Package Information

23 FC2QFN

Package Code	F234A5FY+1	
Outline Number	21-100477	
Land Pattern Number	90-100168	
THERMAL PARAMETERS	**4-LAYER JEDEC BOARD**	**4-LAYER EV KIT**
Junction-to-Ambient Thermal Resistance (θ_{JA})	27.2°C/W	18.5°C/W
Junction-to-Case (Top) Thermal Resistance (θ_{JCt})	9.7°C/W	—
Junction-to-Case (Bottom) Thermal Resistance (θ_{JCb})	4.8°C/W	5.5°C/W
Junction-to-Board Thermal Resistance (θ_{JB})	6.9°C/W	7.9°C/W
Junction-to-Top Characterization Parameter (Ψ_{JT})	0.56°C/W	0.58°C/W
Junction-to-Board Characterization Parameter (Ψ_{JB})	7.0°C/W	7.9°C/W

For the latest package outline information and land patterns (footprints), go to https://www.analog.com/en/resources/packaging-quality-symbols-footprints/package-index.html. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

Electrical Characteristics

(V_{SUP1} = V_{SUP2} = 14V, V_{EN1} = V_{EN2} = 14V, T_J = -40°C to +150°C, unless otherwise noted. Typical values are at T_A = +25°C)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Supply Voltage Range	V_{SUP1}, V_{SUP2}			3		36	V
Load-Dump Event Supply Voltage	V_{SUP_LD}	t_{LD} < 1s				42	V
Shutdown Supply Current	I_{SHDN}	V_{EN1} = V_{EN2} = 0V, T_A = +25°C				6.5	µA
Supply Current	I_{SUP}	V_{EN1} = V_{SUP1} = V_{SUP2}, V_{OUT1} = 3.3V, V_{EN2} = 0V, V_{OUT2} = 0V, V_{EXTVCC} = V_{OUT1}, no load, non-ASIL, no switching, T_A = +25°C			12		µA
		V_{EN1} = V_{EN2} = V_{SUP1} = V_{SUP2}, V_{OUT1} = V_{OUT2} = 3.3V, V_{EXTVCC} = V_{OUT1}, no load, non-ASIL, no switching, T_A = +25°C			17		
		V_{EN1} = V_{EN2} = V_{SUP1} = V_{SUP2}, V_{OUT1} = 3.3V, V_{OUT2} = 5.0V, V_{EXTVCC} = V_{OUT1}, no load, non-ASIL, no switching, T_A = +25°C			18		
		V_{EN1} = V_{SUP1}, V_{EN2} = 0V, V_{OUT1} = 5.0V, V_{OUT2} = 0V, V_{EXTVCC} = V_{OUT1}, no load, non-ASIL, no switching, T_A = +25°C			18		
		V_{EN1} = V_{SUP1}, V_{OUT1} = 3.3V, V_{EN2} = 0V, V_{OUT2} = 0V, V_{EXTVCC} = V_{OUT1}, no load, ASIL, no switching, T_A = +25°C		100	140	180	
		V_{EN1} = V_{EN2} = V_{SUP1} = V_{SUP2}, V_{FB1} = V_{FB2} = 0.815V, V_{EXTVCC} = 3.3V, no load, non-ASIL, no switching, T_A = +25°C			12		
		V_{EN1} = V_{SUP1} = V_{SUP2}, V_{EN2} = 0V, V_{FB1} = 0.815V, V_{FB2} = floating, V_{EXTVCC} = 5V, no load, non-ASIL, no switching, T_A = +25°C			14		
		V_{EN1} = V_{SUP1} = V_{SUP2}, V_{EN2} = 0V, V_{FB1} = 0.815V, V_{FB2} = floating, V_{EXTVCC} = 3.3V, no load, non-ASIL, no switching, T_A = +25°C			9.7		
SUP Undervoltage Lockout	V_{SUP_UVLO}	Rising threshold		2.93	3.03	3.18	V
		Falling threshold		2.64	2.73	2.88	
BIAS Undervoltage Lockout	V_{BIAS_UVLO}	BIAS falling		1.53	1.59	1.63	V
		BIAS rising		1.62	1.66	1.69	
Voltage Accuracy	V_{OUT_SKIP}	V_{OUT} = 3.3V to 5.0V (internal fixed), skip mode, no load, T_A = -40°C to +125°C		-1		+1	%
	V_{OUT_PWM}	V_{OUT} = 3.3V to 5.0V (internal fixed), PWM mode, T_A = -40°C to +125°C		-1		+1	
Overvoltage Threshold Range		MAX25255	4 options, 2.5% step	102.5		110.0	%
		MAX25254	Fixed output option		107.5		
			External feedback option		110.0		
Undervoltage Threshold Range		MAX25255	4 options, 2.5% step	90.0		97.5	%

(V_{SUP1} = V_{SUP2} = 14V, V_{EN1} = V_{EN2} = 14V, T_J = -40°C to +150°C, unless otherwise noted. Typical values are at T_A = +25°C)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
		MAX25254			92.5		
Overvoltage/ Undervoltage Threshold Accuracy		MAX25255	Percentage of nominal output, V_{OUT} = 3.3V to 5.0V	-1		+1	%
		MAX25254	Percentage of nominal output, V_{OUT} = 3.3V to 5.0V	-3		+3	
Overvoltage/ Undervoltage Propagation Delay		MAX25255		35	50	65	µs
		MAX25254			50		
Active Timeout Period		MAX25255		5.4	6.0	6.5	ms
		MAX25254			0.5		
FB Voltage Accuracy	$V_{FB\_PWM\_EXT}$	Only for external divider IC configuration V_{FB} = 0.8V, PWM mode, T_A = -40°C, +125°C		0.788	0.8	0.812	V
FB Current	I_{FB}	V_{FB} = 0.8V, T_A = +25°C			0.02		µA
High-Side DMOS R_{DSON}	R_{ON_HS}	V_{BIAS} = 1.8V, I_{LX} = 1.8A		10	22	50	mΩ
Low-Side DMOS R_{DSON}	R_{ON_LS}	V_{BIAS} = 1.8V, I_{LX} = 1.8A		6	11	24	mΩ
DMOS High-Side Current-Limit Threshold	I_{HS_ILIM}	f_{SW} = 2MHz		9.0	10.5	12.5	A
		f_{SW} = 400kHz		10.5	12.0	14.0	
DMOS Low-Side Negative Current-Limit Threshold	I_{NEG}	f_{SW} = 2MHz		-3.7	-3.2	-2.5	A
		f_{SW} = 400kHz		-4.1	-3.5	-2.9	
LX Leakage Current	I_{LX_LEAK}	V_{SUP} = 36V, V_{LX} = 0V or V_{LX} = 36V, T_A = +25°C		-5		+5	µA
BST Leakage Current	I_{BST_LEAK}	V_{SUP} = 36V, V_{BST} = 0V or V_{BST} = 36V, T_A = +25°C		-5		+5	µA
Soft-Start Ramp Time	t_{SS}			2.3	2.6	2.8	ms
Minimum On-Time	t_{ON}				24	40	ns
Maximum Duty Cycle		Dropout mode		98.0	99.6		%
PWM Switching Frequency	f_{SW_400kHz}			365	400	435	kHz
	f_{SW_2MHz}			1.9	2.0	2.15	MHz
External Input Clock Frequency	f_{SYNC_400kHz}	f_{SW} = 400kHz		380		620	kHz
	f_{SYNC_2MHz}	f_{SW} = 2.0MHz		1.65		2.5	MHz
Spread-Spectrum Range	SPS				±6		%
INTERNAL BIAS LDO							
BIAS Voltage	V_{BIAS}				1.8		V
BIAS Current Limit		V_{EXTVCC} = 0V		65	107	135	mA
PGOOD1, PGOOD2							
PGOOD_ High Leakage Current	I_{LEAK_PGOOD}				1	12	µA
PGOOD_ Low Level	V_{OUT_PGOOD}	Sinking 1mA				0.4	V

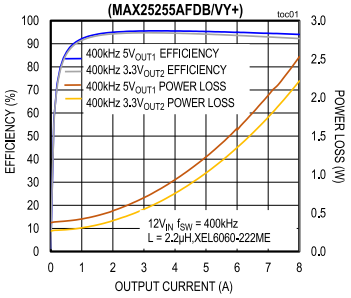
(V_{SUP1} = V_{SUP2} = 14V, V_{EN1} = V_{EN2} = 14V, T_J = -40°C to +150°C, unless otherwise noted. Typical values are at T_A = +25°C)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
LOGIC LEVELS						
EN_ High Level	V_{IH_EN}		1.2			V
EN_ Low Level	V_{IL_EN}				0.5	V
EN_ Input Current	I_{IN_EN}	$V_{EN\_}$ = V_{SUP} = 36V, T_A = +25°C			1	µA
SYNC_ High Threshold	V_{IH_SYNC}		1.4			V
SYNC_ Low Threshold	V_{IL_SYNC}				0.4	V
EXTVCC						
EXTVCC Operating Range	V_{EXTVCC}		2.7		14.0	V
EXTVCC Rising Threshold	V_{EXTVCC_RTH}	EXTVCC rising	2.36	2.50	2.63	V
EXTVCC Falling Threshold	V_{EXTVCC_FTH}	EXTVCC falling	2.25	2.41	2.54	V
SYNCOUT						
SYNCOUT Voltage Level	$V_{SYNCOUT}$	5mA max load current	2.55	3.30	3.85	V
TEMP AND THERMAL PROTECTION						
Temperature Monitoring Range			20		160	°C
TEMP Voltage Range			0.7		1.2	V
TEMP Voltage Accuracy		T_J = +25°C	0.73	0.75	0.77	V
		T_J = +125°C	0.95	1.00	1.06	
Thermal Shutdown	T_{SHDN}			175		°C
Thermal Shutdown Hysteresis	T_{SHDN_HYS}			15		°C

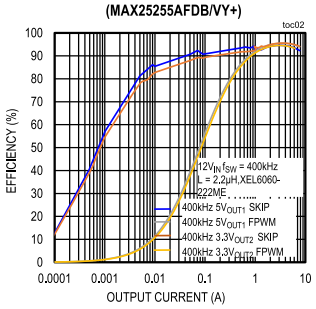
Typical Operating Characteristics

(V_{SUP} = V_{EN} = 12V, T_A = +25°C, unless otherwise noted.)

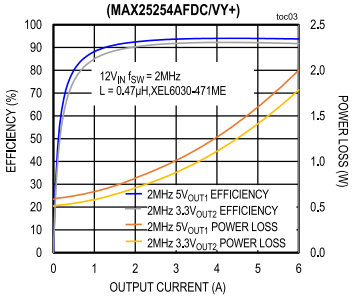
EFFICIENCY AND POWER LOSS vs. OUTPUT CURRENT (MAX25255AFDB/VY+)



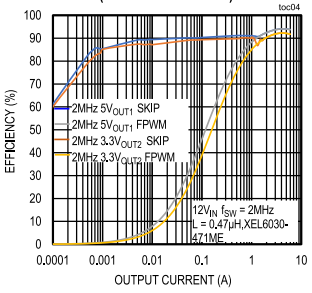
EFFICIENCY vs. OUTPUT CURRENT (MAX25255AFDB/VY+)



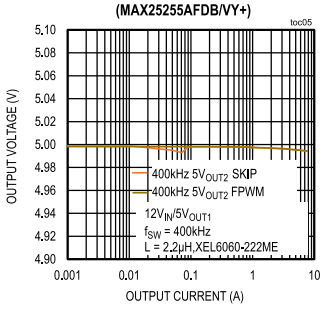
EFFICIENCY AND POWER LOSS vs. OUTPUT CURRENT (MAX25254AFDC/VY+)



EFFICIENCY vs. OUTPUT CURRENT (MAX25254AFDC/VY+)



OUTPUT LOAD REGULATION (MAX25255AFDB/VY+)



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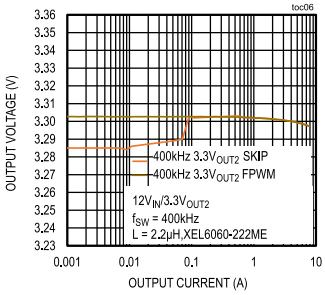
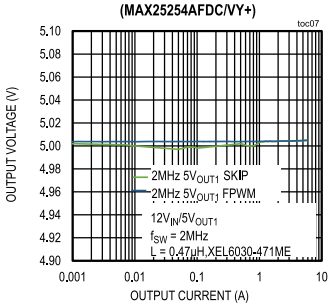
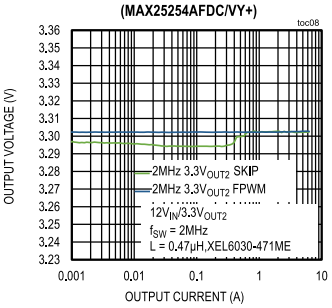


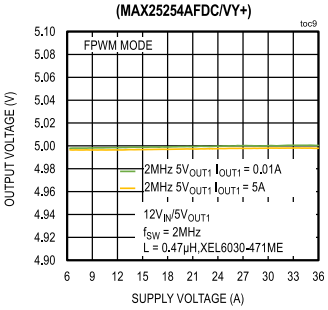
OUTPUT LOAD REGULATION (MAX25254AFDC/VY+)

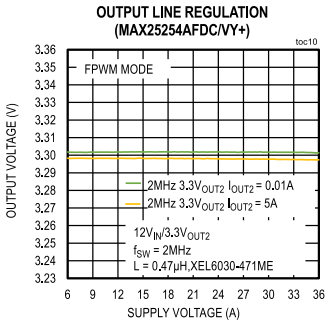


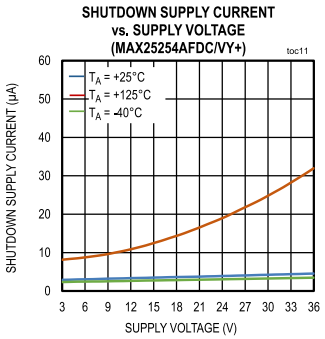
OUTPUT LOAD REGULATION (MAX25254AFDC/VY+)

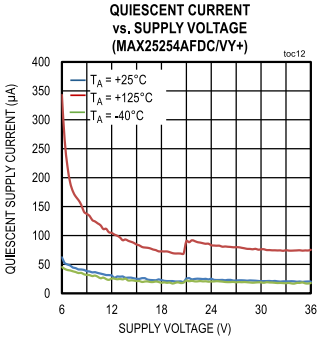


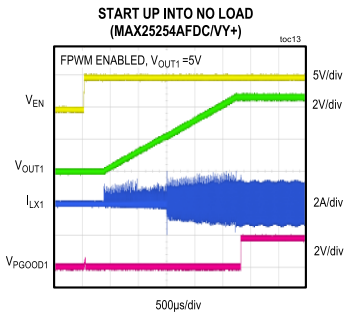
OUTPUT LINE REGULATION (MAX25254AFDC/VY+)

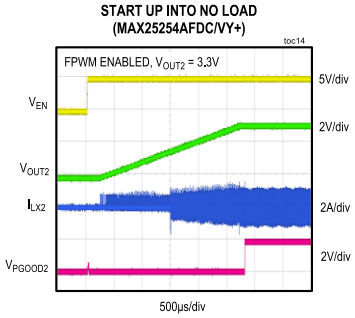


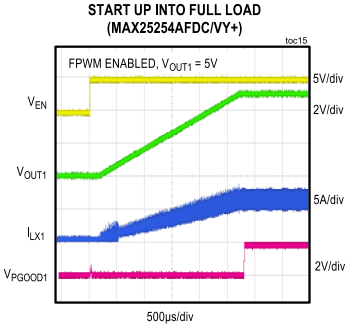

OUTPUT LINE REGULATION
(MAX25254AFDC/VY+)
toc10
FPWM MODE
2MHz 3.3VOUT2 IOUT2 = 0.01A
2MHz 3.3VOUT2 IOUT2 = 5A
12VIN/3.3VOUT2
fSW = 2MHz
L = 0.47µH,XEL6030-471ME
OUTPUT VOLTAGE (V)
SUPPLY VOLTAGE (A)

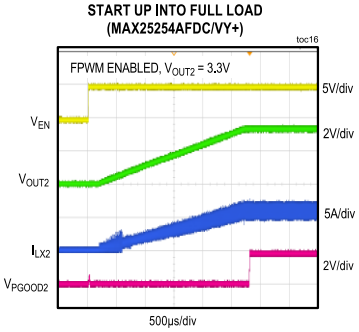

SHUTDOWN SUPPLY CURRENT
vs. SUPPLY VOLTAGE
(MAX25254AFDC/VY+)
toc11
TA = +25°C
TA = +125°C
TA = -40°C
SHUTDOWN SUPPLY CURRENT (µA)
SUPPLY VOLTAGE (V)

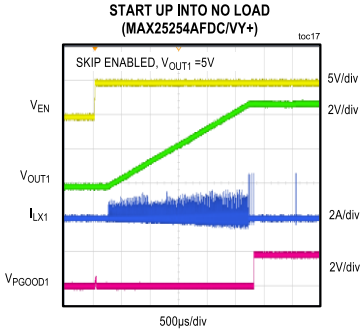

QUIESCENT CURRENT
vs. SUPPLY VOLTAGE
(MAX25254AFDC/VY+)
toc12
TA = +25°C
TA = +125°C
TA = -40°C
QUIESCENT SUPPLY CURRENT (µA)
SUPPLY VOLTAGE (V)

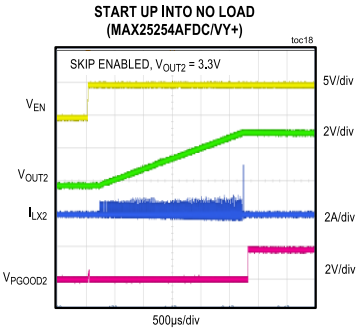

START UP INTO NO LOAD
(MAX25254AFDC/VY+)
toc13
FPWM ENABLED, VOUT1 =5V
VEN
VOUT1
ILX1
VPGOOD1
5V/div
2V/div
2A/div
2V/div
500µs/div


START UP INTO NO LOAD
(MAX25254AFDC/VY+)
toc14
FPWM ENABLED, VOUT2 = 3.3V
VEN
VOUT2
ILX2
VPGOOD2
5V/div
2V/div
2A/div
2V/div
500µs/div

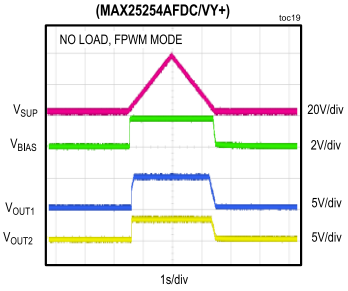

START UP INTO FULL LOAD
(MAX25254AFDC/VY+)
toc15
FPWM ENABLED, VOUT1 = 5V
VEN
VOUT1
ILX1
VPGOOD1
5V/div
2V/div
5A/div
2V/div
500µs/div


START UP INTO FULL LOAD
(MAX25254AFDC/VY+)
toc16
FPWM ENABLED, VOUT2 = 3.3V
VEN
VOUT2
ILX2
VPGOOD2
5V/div
2V/div
5A/div
2V/div
500µs/div

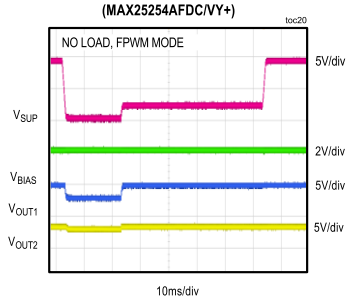

START UP INTO NO LOAD
(MAX25254AFDC/VY+)
toc17
SKIP ENABLED, VOUT1 =5V
VEN
VOUT1
ILX1
VPGOOD1
5V/div
2V/div
2A/div
2V/div
500µs/div


START UP INTO NO LOAD
(MAX25254AFDC/VY+)
toc18
SKIP ENABLED, VOUT2 = 3.3V
VEN
VOUT2
ILX2
VPGOOD2
5V/div
2V/div
2A/div
2V/div
500µs/div

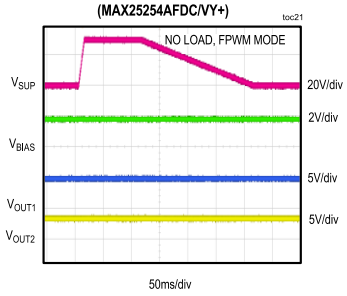
SLOW INPUT VOLTAGE RISING
(MAX25254AFDC/VY+)



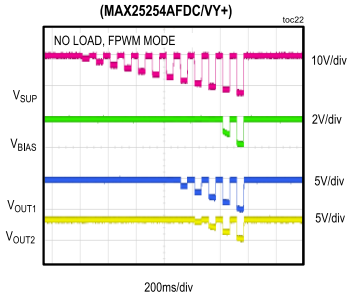
COLD CRANK
(MAX25254AFDC/VY+)



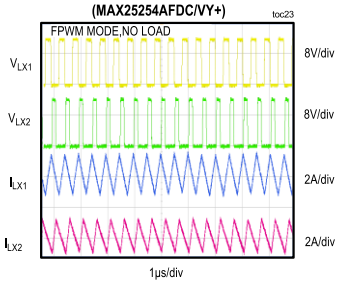
LOAD DUMP
(MAX25254AFDC/VY+)



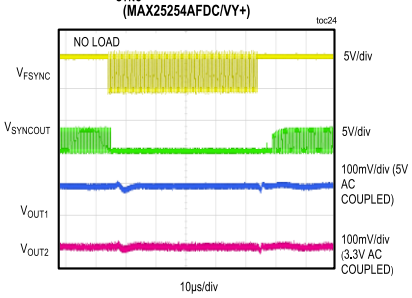
DIPS AND DROPS
(MAX25254AFDC/VY+)



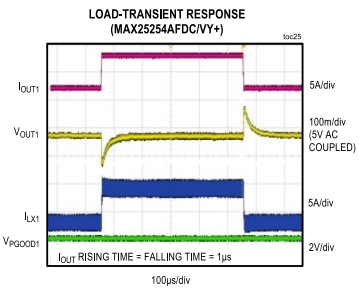
STEADY-STATE
SWITCHING WAVEFORM
(MAX25254AFDC/VY+)



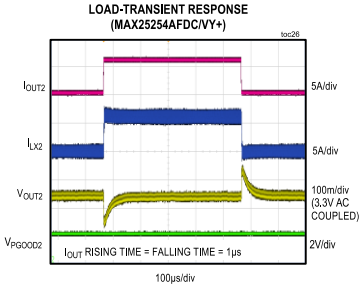
fSYNC SYNCHRONIZATION
(MAX25254AFDC/VY+)



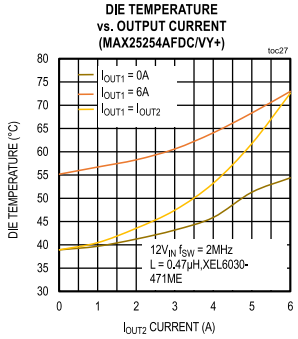
LOAD-TRANSIENT RESPONSE
(MAX25254AFDC/VY+)



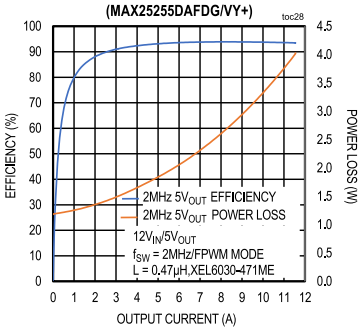
LOAD-TRANSIENT RESPONSE
(MAX25254AFDC/VY+)



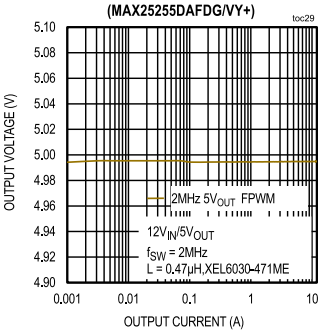
DIE TEMPERATURE
vs. OUTPUT CURRENT
(MAX25254AFDC/VY+)



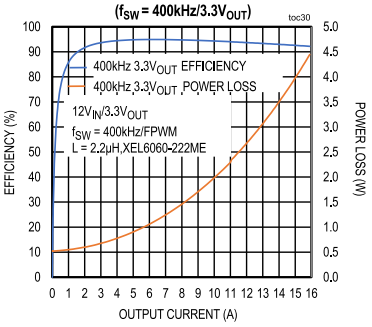
DUAL PHASE EFFICIENCY AND POWER LOSS vs. OUTPUT CURRENT (MAX25255DAFDG/VY+)



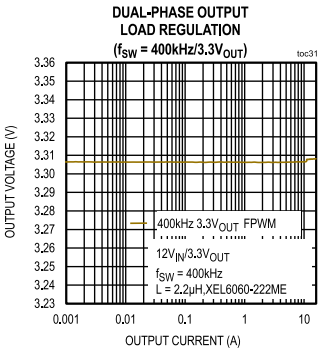
DUAL-PHASE OUTPUT LOAD REGULATION (MAX25255DAFDG/VY+)



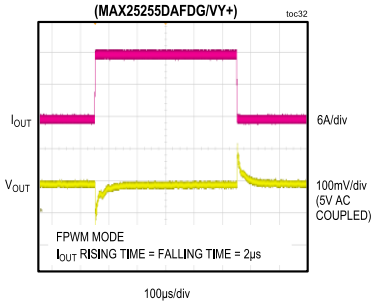
DUAL-PHASE EFFICIENCY AND POWER LOSS vs. OUTPUT CURRENT (f_{SW} = 400kHz/3.3V_{OUT})



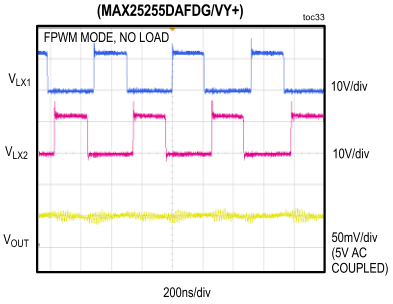
DUAL-PHASE OUTPUT LOAD REGULATION (f_{SW} = 400kHz/3.3V_{OUT})



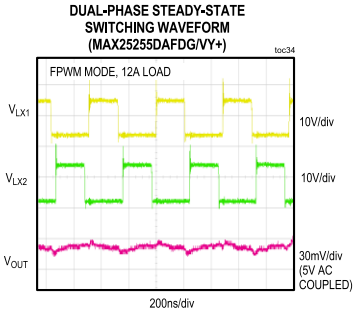
DUAL-PHASE LOAD-TRANSIENT RESPONSE (MAX25255DAFDG/VY+)



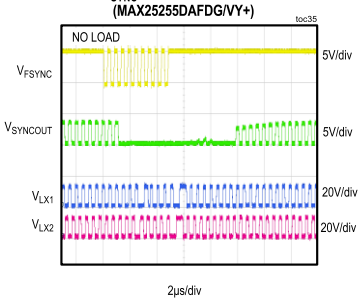
DUAL-PHASE STEADY-STATE SWITCHING WAVEFORM (MAX25255DAFDG/VY+)



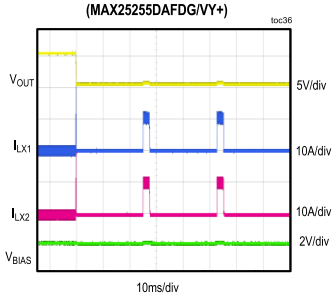
DUAL-PHASE STEADY-STATE SWITCHING WAVEFORM (MAX25255DAFDG/VY+)

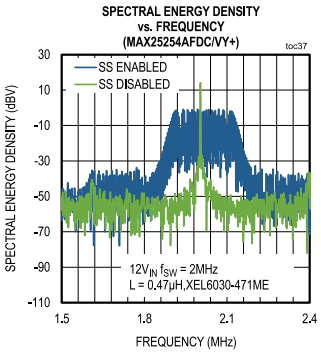


DUAL-PHASE f_{SYNC} SYNCHRONIZATION (MAX25255DAFDG/VY+)

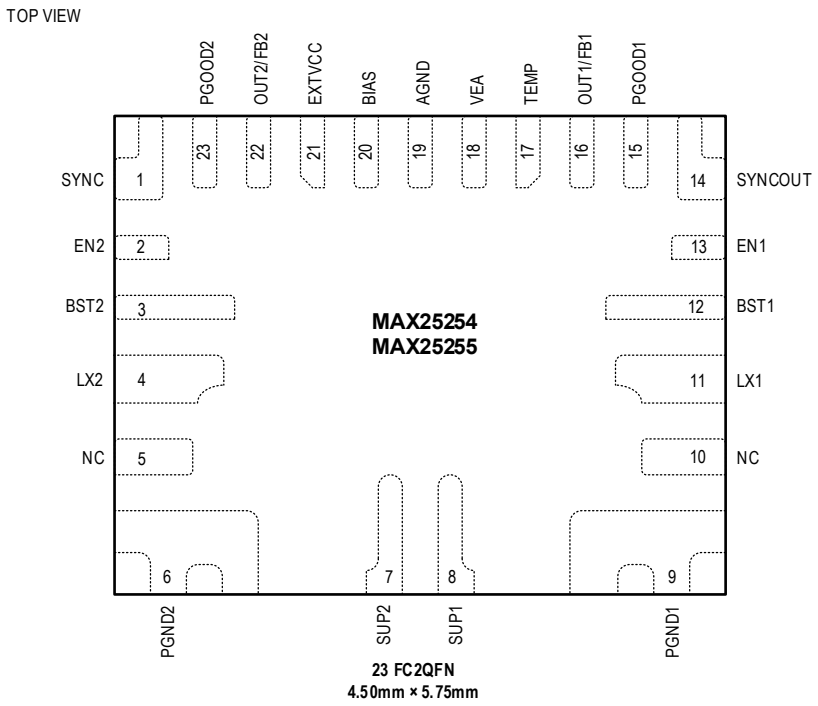


OUTPUT SHORT TO GROUND (MAX25255DAFDG/VY+)




SPECTRAL ENERGY DENSITY
vs. FREQUENCY
(MAX25254AFDC/VY+)
toc37
SS ENABLED
SS DISABLED
12VIN fSW = 2MHz
L = 0.47µH,XEL6030-471ME
SPECTRAL ENERGY DENSITY (dBV)
FREQUENCY (MHz)
30
10
-10
-30
-50
-70
-90
-110
1.5
1.8
2.1
2.4

Pin Configurations



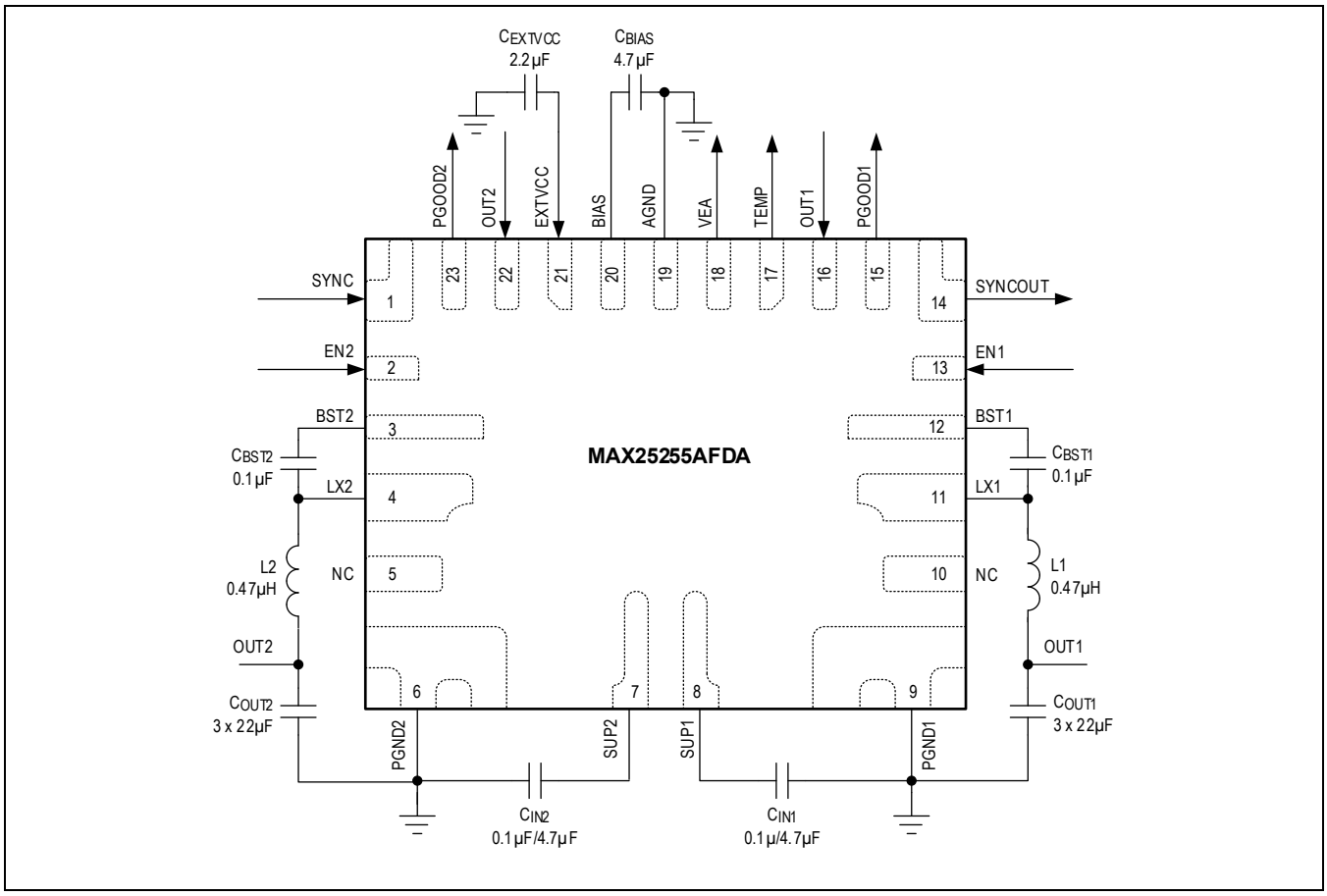
NOTE: OUT1 AND OUT2 FOR FIXED OUTPUT VERSION
FB1 AND FB2 FOR ADJUSTABLE OUTPUT VERSION

Pin Descriptions

PIN	NAME	FUNCTION
1	SYNC	Synchronization Input. Connect SYNC to AGND to enable skip mode. Connect SYNC to high to enable FPWM mode. It can also be used to synchronize to an external clock.
2	EN2	Enable Input for Buck2. Drive EN2 high/low to enable/disable Buck2. EN2 can be connected directly to the battery for always-ON applications.
3	BST2	Integrated High-Side MOSFET Gate Drive Supply. Connect a 0.1µF ceramic capacitor between BST2 and LX2 for proper operation.
4	LX2	Buck2 Inductor Connection. Connect an inductor from LX2 to Buck2 output. LX2 is high impedance when Buck2 is disabled.
5	NC	Not Connected
6	PGND2	Buck2 Power Ground. Make sure that PGND2 is connected to the ground plane with enough vias for optimum thermal performance.
7	SUP2	Buck2 High-Side MOSFET Supply. Bypass SUP2 to PGND2 with 0.1µF and 4.7µF ceramic capacitors as close as possible.
8	SUP1	Buck1 High-Side MOSFET and BIAS LDO Supply. Bypass SUP1 to PGND1 with 0.1µF and 4.7µF ceramic capacitors as close as possible.
9	PGND1	Buck1 Power Ground. Make sure that PGND1 is connected to the ground plane with enough vias for optimum thermal performance.
10	NC	Not Connected

11	LX1	Buck1 Inductor Connection. Connect an inductor from LX1 to the Buck1 output. LX1 is high impedance when Buck1 is disabled.
12	BST1	Integrated High-Side MOSFET Gate Drive Supply. Connect a 0.1µF ceramic capacitor between BST2 and LX2 for proper operation.
13	EN1	Enable Input for Buck1. Drive EN1 high/low to enable/disable Buck1. EN1 can be connected directly to the battery for always-ON applications.
14	SYNCOUT	90° Out-of-Phase Clock Output. Connect SYNCOUT of the primary IC to SYNC of the secondary IC for quad-phase operation. Multiphase operation is designed for PWM mode. No clock is present on SYNCOUT in skip mode or with external clock synchronization.
15	PGOOD1	Buck1 Open-Drain Power-Good Output. Connect PGOOD1 to BIAS or an external voltage rail with a pull-up resistor. PGOOD1 is pulled to ground during startup, Buck1 output undervoltage, or overvoltage.
16	OUT1/FB1	Buck1 Output Sense/Feedback Input. In the fixed output version, connect OUT1 to the Buck1 output to set the fixed output voltage. In the adjustable output version, connect FB1 to a resistor-divider between the Buck1 output and AGND to program the output voltage between 0.8V and 14V. FB1 is regulated to 0.8V (typ) in the adjustable version.
17	TEMP	Die Temperature Monitoring Node. The voltage at TEMP is proportional to the IC die temperature.
18	VEA	Error Amplifier Output for Multiphase Operation. When two ICs are used in parallel for quad-phase operation, tie both VEA nodes together for phase balancing. Leave VEA open in single-IC operation.
19	AGND	Analog Ground. All of the sensitive analog signals are internally referenced to analog ground. Care must be taken during layout to ensure that AGND is routed in the quiet section of the PCB.
20	BIAS	Internal Linear Regulator Output. Bypass BIAS with a 4.7µF (min) capacitor to AGND. BIAS supplies the internal gate drive circuitry and is not for external use.
21	EXTVCC	Switchover Input. When valid voltage is present at EXTVCC, EXTVCC supplies the internal BIAS LDO after soft-start is complete. If the EXTVCC voltage is not valid, or it is tied to ground, the BIAS LDO is supplied by SUP1. Bypass EXTVCC with a 2.2µF ceramic capacitor.
22	OUT2/FB2	Buck2 Output Sense/Feedback Input. In the fixed output version, connect OUT2 to the Buck2 output to set the fixed output voltage. In the adjustable output version, connect FB2 to a resistor-divider between the Buck2 output and AGND to program the output voltage between 0.8V and 14V. FB2 is regulated to 0.8V (typ) in the adjustable output version.
23	PGOOD2	Buck2 Open-Drain Power-Good Output. Connect PGOOD2 to BIAS or an external voltage rail with a pull-up resistor. PGOOD2 is pulled to ground during startup, Buck2 output undervoltage, or overvoltage.

Functional Diagrams



Detailed Description

The MAX25254/MAX25255 are small, dual synchronous buck converters with integrated high-side and low-side MOSFETs. Each buck converter is sized to provide continuous current of 6A at 2MHz. The current capability of the device is increased at lower switching frequency to 8A at 400kHz. These buck converters offer high-voltage-capable individual enable pins that can be tied directly to a car battery in always-ON applications. They also offer a very low quiescent current of 12µA with either one of the buck converters enabled. The voltage quality of the buck converters can be monitored by observing the PGOOD1/PGOOD2 signal. The MAX25254/MAX25255 can operate in dropout by running at 99% of the duty cycle, making them ideal for automotive and industrial applications.

The MAX25254/MAX25255 offer fixed output voltage and adjustable output voltage options. The voltages can be externally set when using the adjustable output version by placing external resistor-dividers between the buck outputs, FB1/FB2, and AGND. The MAX25254/MAX25255 provide an internal oscillator with 200kHz/400kHz/1MHz/2MHz options. Frequency operation at 2MHz optimizes the application for the smallest component size at the cost of lower efficiency. Frequency operation at 200kHz/400kHz offers better overall efficiency at the expense of component size and board space. The buck converters automatically enter skip mode at light loads with 12µA ultra-low quiescent current and SYNC pulled low. The MAX25254/MAX25255 can also be used in dual-phase or quad-phase operation and can output up to 32A in quad-phase operation.

The MAX25255 buck converters are individually designed for the ASIL B safety level. The overvoltage and undervoltage thresholds can be individually programmed to a set level within ±1% accuracy.

Internal 1.8V BIAS LDO

An internal 1.8V BIAS LDO supplies the IC internal circuitry. SUP1 supplies the internal BIAS LDO. Bypass BIAS with a 4.7µF (min) ceramic capacitor. To minimize the LDO power dissipation, enable the EXTVCC switchover circuitry to have the LDO input switch from SUP1 to the buck output.

EXTVCC Switchover

To reduce the IC internal power dissipation, the input of the internal BIAS LDO can be switched from SUP1 to an external supply, or to the output of one of the buck converters, by applying the valid voltage to EXTVCC. If the buck converter output is connected to EXTVCC, light load efficiency is improved as the SUP1 supply current to BIAS LDO is scaled down proportionally to the duty cycle of buck converter.

If V_{EXTVCC} drops below 2.4V (typ), the input supply of the BIAS LDO is automatically switched back to SUP1.

Switching Frequency/External Synchronization

The MAX25254/MAX25255 provide an internal oscillator with 200kHz, 400kHz, 1MHz, and 2MHz options. Drive SYNC high for forced-PWM (FPWM) operation. Drive SYNC low to enable skip mode for better efficiency at a light load. The IC can be synchronized to the external clock with a valid external clock present at SYNC.

Apply an external clock to SYNC to enable frequency synchronization. The Buck1 converter synchronizes its LX1 rising edge to the SYNC rising edge, and Buck1 and Buck2 converters operate 180° out of phase.

Spread-Spectrum Option

The ICs feature enhanced EMI performance with a spread-spectrum option. When spread spectrum is enabled, the operating frequency is varied by ±6% centered at switching frequency. The modulation signal is a triangular wave with a 4.5kHz frequency at 2MHz. Therefore, the switching frequency ramps down 6% and back to 2MHz in 110µs, and ramps up 6% and back to 2MHz in 110µs after which the cycle repeats. For operations at 400kHz, the modulation signal scales proportionally to 4.5kHz x 0.4/2 = 0.9kHz.

The internal spread-spectrum option is disabled if the devices are synchronized to an external clock. However, the devices do not filter the input clock on SYNC and pass any modulation present (including spread spectrum) onto the driving external clock.

Enable Input (EN1/EN2)

Enable inputs EN1 and EN2 enable the corresponding buck converter from its shutdown mode. EN1/EN2 are high-voltage compatible with input from an automotive battery level down to 1.8V. Drive EN1/EN2 high to enable the Buck1/Buck2 converter output. Drive both EN1 and EN2 low to disable the IC into shutdown mode. The quiescent current is reduced to 6.5µA (max) during shutdown.

Soft-Start

Drive EN1/EN2 high to enable the buck converters. The soft-start circuitry gradually ramps up the reference voltage during soft-start time (2.6ms, typ) to reduce input inrush currents.

Power-Good Indicators (PGOOD1/PGOOD2)

The IC features two open-drain power-good outputs (PGOOD1/PGOOD2) to indicate the output voltage status. PGOOD pulls low when the MAX25254 buck converter output voltage drops below 92.5% (typ) of the nominal regulation voltage or above 107.5% (typ). The PGOOD asserts low during soft-start.

The MAX25255 buck converters are individually designed for the ASIL B safety level. Four PGOOD undervoltage threshold options are possible between 90% and 97.5% in 2.5% steps, and four PGOOD overvoltage threshold options are possible between 102.5% and 110% in 2.5% steps. Contact the factory for additional part options.

Short-Circuit Protection

The buck converters feature a cycle-by-cycle current limit and hiccup mode to protect them against a short-circuit or overload condition. In the event of an overload condition, the high-side FET remains on until the inductor current reaches the current-limit threshold. The converter then turns off the high-side FET and turns on the low-side FET to allow the inductor current to ramp down. Once the inductor current decreases to the valley current limit, the converter turns on the high-side FET again. This cycle repeats until the overload condition is removed.

A short-circuit is detected when the output voltage falls below the preset threshold voltage. The threshold voltage is 50% of the output regulation voltage for the fixed output voltage version, or 25% of the output regulation voltage for the

adjustable output voltage version. During hiccup mode, the IC turns off the buck converter for 26ms (10x soft-start time), and then restarts it in case the overcurrent or short-circuit condition is removed. The hiccup repeats when the short-circuit is continuously present.

Die Temperature Monitor

The MAX25254/MAX25255 feature a temperature sensor to monitor die temperature. A voltage proportional to the die temperature is provided at the TEMP node. The relation between the TEMP voltage and die temperature is shown in the following formula:

$V_{TEMP} = 2.6 \times T_J + 685$

where V_{TEMP} is in mV.

The TEMP node outputs 0.75V (typ) at a die temperature of +25°C and 1V at +125°C. The die temperature monitor function is only enabled in FPWM.

Thermal Shutdown Protection

Thermal shutdown protection limits total power dissipation in the IC. When the junction temperature exceeds +175°C, an internal sensor shuts down the IC, allowing it to cool. The thermal sensor turns on the IC again after the junction temperature cools by 15°C.

Multiphase Operation

The MAX25254/MAX25255 can be configured in dual phase and quad-phase to provide higher output current, up to 16A and 32A respectively. In dual-phase operation, two buck converters within the MAX25254D/MAX25255D are operated in parallel with 180° out-of-phase switching to provide an output current up to 16A. Buck1 of the MAX25254D/MAX25255D is programmed as a primary, while Buck2 is treated as secondary in dual-phase operation.

Furthermore, the MAX25254D/MAX25255D and MAX25254Q can be operated in parallel to be configured in quad-phase operation to meet higher current needs. The MAX25254D/MAX25255D is programmed as a primary while MAX25254Q is treated as a secondary. In quad-phase operation, the SYNCOUT of the primary is connected to the SYNC of the secondary to have both ICs switch 90° out of phase to reduce the filter capacitor requirement. FPWM operation is recommended for quad-phase operation. The VEA nodes of the primary and the secondary are connected to ensure balanced current sharing between two ICs and to share primary's voltage control loop with the secondary. In multiphase operation, PGOOD2 of the primary IC is used to report the status of primary buck, while PGOOD1 of the secondary is used for primary status sense. PGOOD2 of the primary is connected to PGOOD1 of the secondary in quad-phase operation.

Applications Information

Setting Output Voltage

The MAX25254 offers an adjustable output version to program the output voltage from 0.8V to 14V. Connect a resistive voltage-divider from the converter output to the FB_ input and then to AGND (see *Figure 1*). Select the bottom-side resistors (R_{BOTTOM} from FB_-to-AGND) close to or equal to 10kΩ. Calculate the top-side resistors (R_{TOP} from output-to-FB_) with the following equation:

$$R_{TOP} = R_{BOTTOM} \times \left(\frac{V_{OUT}}{V_{FB}} - 1\right)$$

where V_{FB} = 0.8V (typ) and R_{BOTTOM} = 10kΩ.

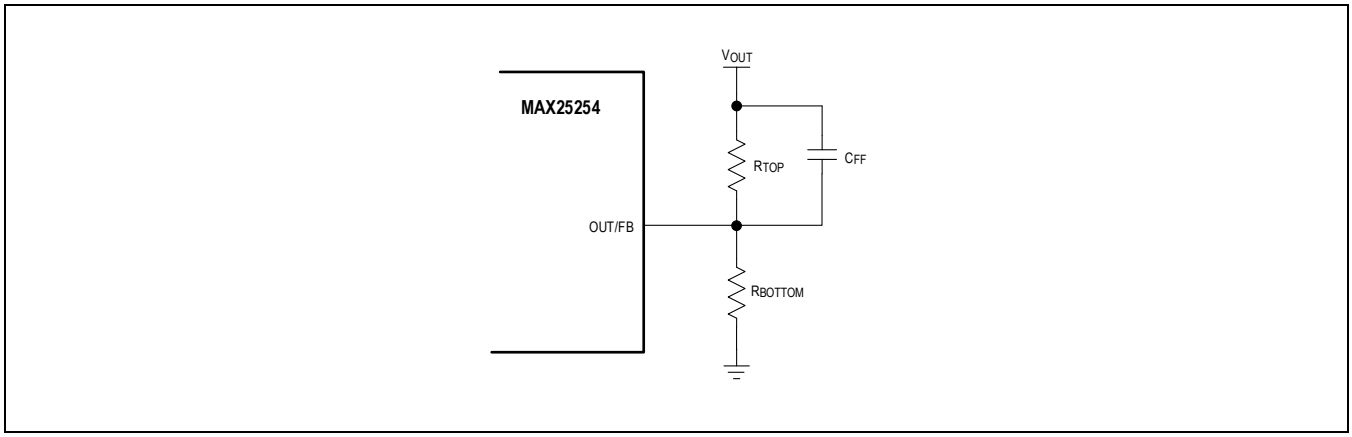


Figure 1. Setting Output Voltage Using External Resistor-Divider

When an external resistor-divider is used to program the buck output voltage, a feed-forward capacitor in parallel with R_{TOP} with a low-pF capacitance can be used to improve control-loop phase margin.

Input Capacitor

The input capacitors reduce peak current drawn from the power source and improve noise and voltage ripple on the SUP1/SUP2 nodes caused by the buck converter switching cycles. Two ceramic input capacitors with 0.1µF and 4.7µF capacitance are recommended in parallel at SUP1/SUP2 for proper buck operation.

Place a 0.1µF ceramic capacitor of a 0402 or 0603 size next to SUP1/SUP2 and PGND to reduce input noise and improve EMI performance. A 4.7µF ceramic capacitor after a 0.1µF capacitor is required on each input side to reduce input voltage ripple. An additional buck capacitor might be required if high impedance exists in the input supply or traces.

The input capacitor RMS current requirement (I_{RMS}) is defined by the following equation:

$$I_{RMS} = I_{LOAD(MAX)} \times \left(\frac{\sqrt{V_{OUT} \times (V_{SUP} - V_{OUT})}}{V_{SUP}}\right)$$

I_{RMS} has a maximum value when the input voltage equals twice the output voltage:

$$V_{SUP} = 2 \times V_{OUT}$$

Therefore:

$$I_{RMS} = \frac{I_{LOAD(MAX)}}{2}$$

Choose an input capacitor that exhibits less than +10°C self-heating temperature rise at the RMS input current for optimal long-term reliability. The input-voltage ripple is composed of ΔV_Q (caused by the capacitor discharge) and ΔV_{ESR} (caused by the ESR of the capacitor). Assume the contribution from the ESR and capacitor discharge to be equal to 50%. Calculate the input capacitance and ESR required for a specified input voltage ripple using the following equations:

$$ESR_{IN} = \frac{\Delta V_{ESR}}{I_{LOAD(MAX)} + {\Delta I_L}/{2}}$$

$$C_{IN} = \frac{I_{LOAD(MAX)} \times D(1-D)}{\Delta V_Q \times f_{SW}}$$

where:

$$\Delta I_L = \frac{(V_{SUP} - V_{OUT}) \times V_{OUT}}{V_{SUP} \times f_{SW} \times L}$$

$$D = \frac{V_{OUT}}{V_{SUP}}$$

and $I_{LOAD(MAX)}$ is the maximum output current, ΔI_L is the peak-to-peak inductor current, f_{SW} is the switching frequency, and D is the duty cycle.

Inductor Selection

Inductor selection is a compromise between component size, efficiency, control loop bandwidth, and loop stability. Insufficient inductance increases the inductor current ripple, conduction losses, and output voltage ripple, and causes loop instability in the worst case. A large inductor reduces the inductor current ripple but sacrifices of component size and slow response. See *Table 1* for optimized inductor values at switching frequencies of 400kHz and 2MHz. The nominal standard value selected should be within ±30% of the specified inductance.

Table 1. Recommended Inductor and Output Capacitor per Phase

SWITCHING FREQUENCY	RECOMMENDED INDUCTANCE (µH)	RECOMMENDED OUTPUT CAPACITANCE (µF)
400kHz	2.2	3 x 47
2MHz	0.47	3 x 22

Output Capacitor

The output capacitor is a critical component for switching regulators. It is selected to meet output voltage ripple, load transient response, and loop stability requirements.

The output voltage ripple is composed of ΔV_Q (caused by the capacitor discharge) and ΔV_{ESR} (caused by the ESR of the output capacitor). Use low-ESR ceramic capacitors. Assume the contribution to the output ripple voltage from ESR and the capacitor discharge to be equal. Use the following equations to get the output capacitance and ESR for a specified output voltage ripple.

$$ESR = \frac{\Delta V_{ESR}}{\Delta I_{P-P}}$$

$$C_{OUT} = \frac{\Delta I_{P-P}}{8 \times \Delta V_Q \times f_{SW}}$$

$$\Delta I_{P-P} = \frac{(V_{SUP} - V_{OUT}) \times V_{OUT}}{V_{SUP} \times f_{SW} \times L}$$

$$V_{OUT_{RIPPLE}} = \Delta V_{ESR} + \Delta V_Q$$

where ΔI_{P-P} is the peak-to-peak inductor current.

During a load step, the output capacitors supply the load current before the converter loop responds with a higher duty cycle, which causes output voltage undershoot. To keep the maximum output voltage deviations below the tolerable limits of the electronics being powered, output capacitance can be calculated with the following equation:

$$C_{OUT} = \frac{\Delta I_{LOAD}}{\Delta V \times 2\pi \times f_C}$$

where ΔI_{LOAD} is the load step, ΔV is the allowed output voltage undershoot, and f_C is the loop crossover frequency, which can be assumed to be $f_{SW}/10$. The calculated C_{OUT} is the actual capacitance after considering capacitance tolerance, temperature effect, and voltage derating. See *Table 1* for recommended output capacitance.

PCB Layout Guidelines

Careful PCB layout is critical to achieve low switching losses, low EMI, and clean, stable operation. See *Figure 2* and the MAX25255 evaluation kit (EV kit) for an example layout.

Place the ceramic input-bypass capacitors (CIN and CBP) as close as possible to SUP1/SUP2 and PGND1/PGND2. Input capacitors should be placed right next to the SUP1/SUP2 and PGND1/PGND2 nodes on the same layer to provide best EMI rejection and minimize the input noise on SUP1/SUP2. The symmetrical input capacitor arrangements generate the SUP1/SUP2 loops with opposite orientation to cancel the magnetic fields and help EMI mitigation.

Minimize the connection from the buck output capacitor's ground terminal to the input capacitor's ground terminal and to the PGND1/PGND2 nodes. Keep the buck's high-current path and power traces wide and short. Minimize the traces from LX node to the inductor and then to the output capacitors. This reduces the buck current loop area and minimizes LX trace resistance and stray capacitance to achieve optimal efficiency.

Place the bootstrap capacitors (CBST) next to the LX1/LX2 and BST1/BST2 nodes. Use short and wide traces from BST1/BST2 and LX1/LX2 to minimize this routing parasitic impedance. High parasitic impedance from BST1/BST2 to LX1/LX2 impacts the switching speed, further increases switching losses, and causes high dv/dt noise. See the MAX25255 EV kit for BST1/BST2 to LX1/LX2 routing.

Place the BIAS capacitor as close to the BIAS node as possible. Noise coupling into BIAS can disturb the reference and bias circuitry if this capacitor is installed away from the IC.

Place the EXTVCC capacitor as close to the EXTVCC node as possible if the EXTVCC switchover is used. Noise coupling into EXTVCC can disturb the reference and bias circuitry if this capacitor is installed away from the IC.

Keep the sensitive analog signals (OUT1/OUT2/FB1/FB2/VEA) away from noisy switching nodes (LX1/LX2 and BST1/BST2) and high-current loops. For a multiphase PCB, minimize the connection between VEAs and the connection from the primary's SYNCOUT to the secondary's SYNC.

Ground is the return path for the full load currents flowing into and out of the MAX25254/MAX25255. It is also the common reference voltage for all of the analog circuits. Improper ground routing can bring extra resistance and inductance into the current loop, causing different voltage reference and worsening voltage ringing or spikes. Place a solid ground plane layer under the power loop components layer to shield the switching noise from other sensitive traces. Isolate the analog ground AGND from the power ground PGND1/PGND2 under the IC area on the component layer. Connect AGND and PGND1/PGND2 together at a single point with a star ground connection to minimize the ground current loops.

PCB layout also plays an important role in power dissipation and thermal performance. The PGND1/PGND2 nodes are main power connection area between the IC and outside the IC. Place as much copper ground area as possible around the PGND1/PGND2 area to ensure efficient heat transfer. Place as many as possible vias around PGND nodes and under the IC area to further transfer the heat down the internal ground plane and other layers to further improve the thermal resistance from the IC package to the ambient area.

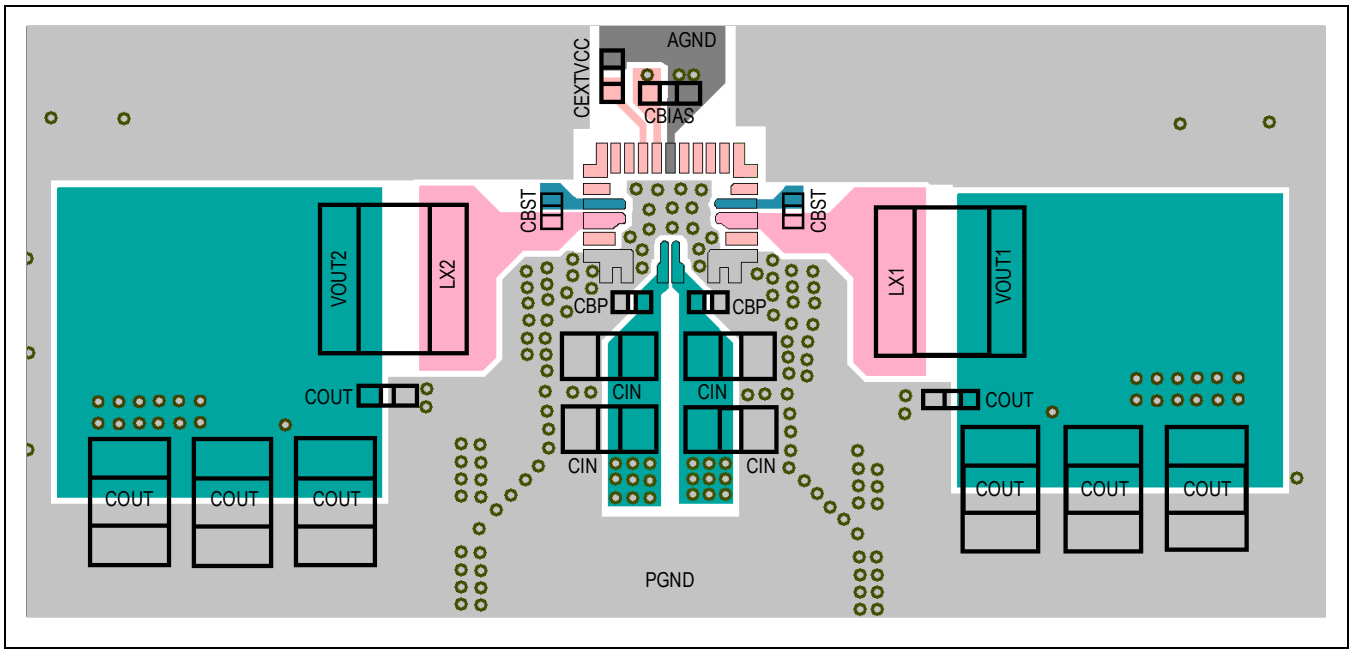
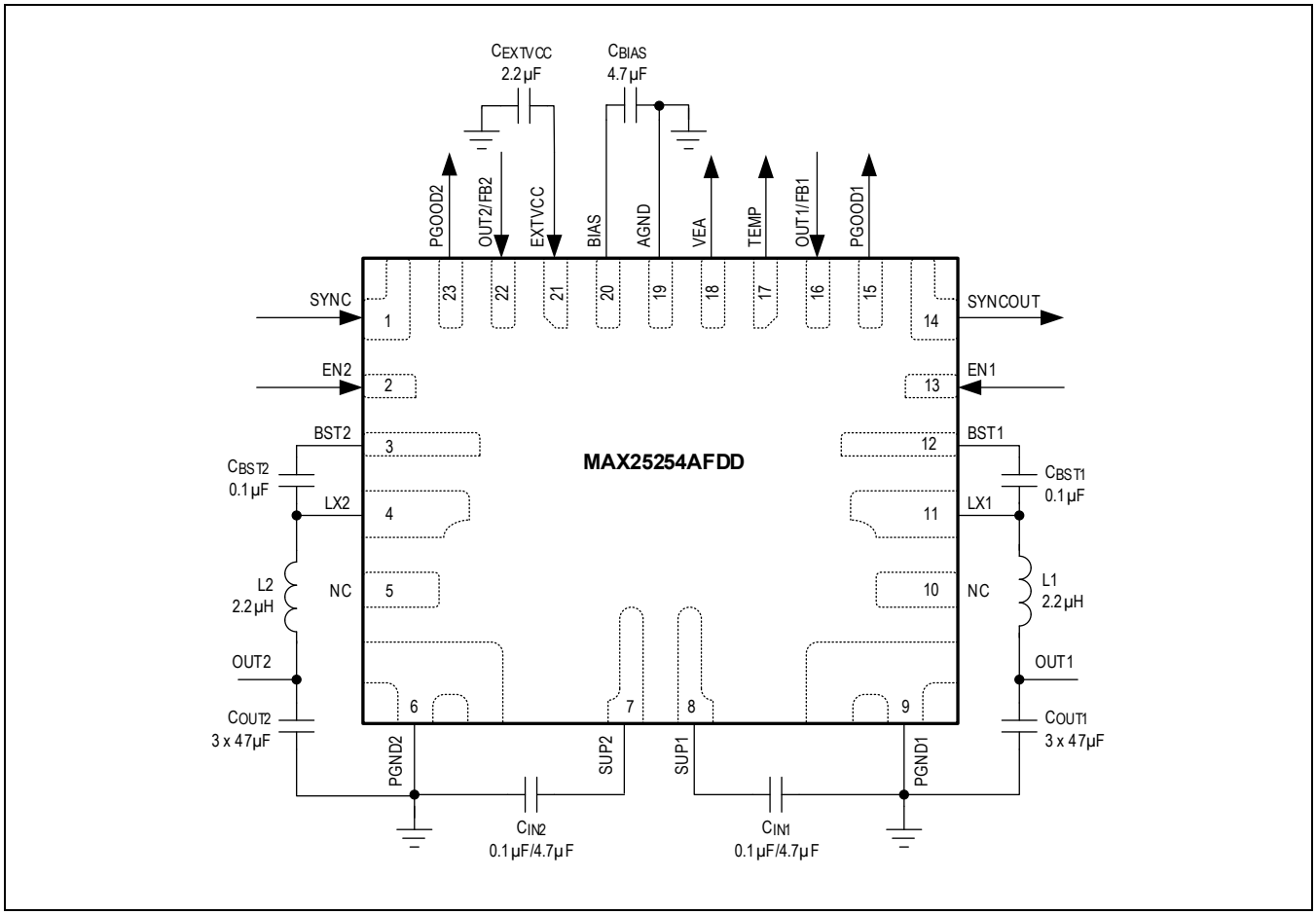


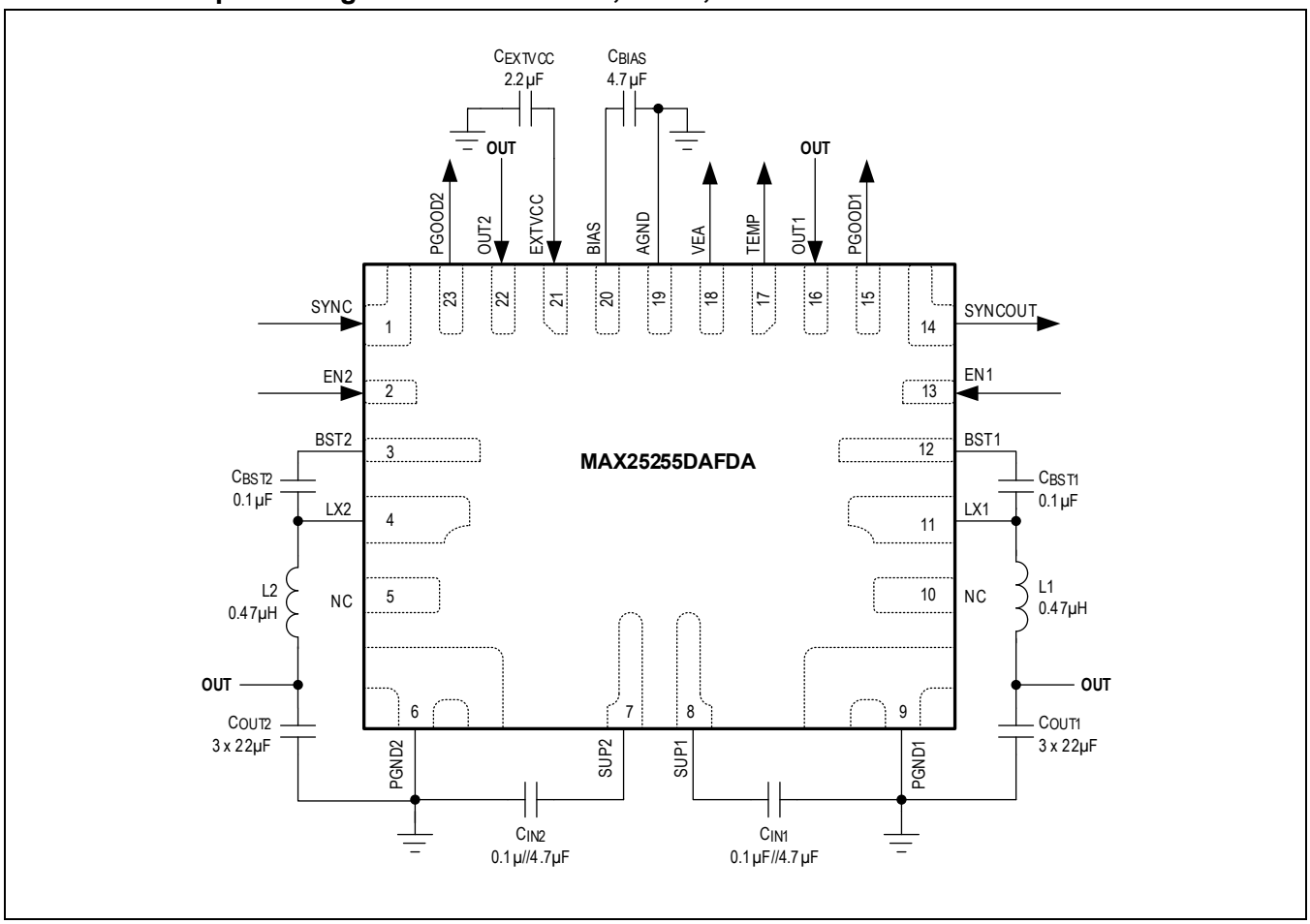
Figure 2. Layout Example

Typical Application Circuits

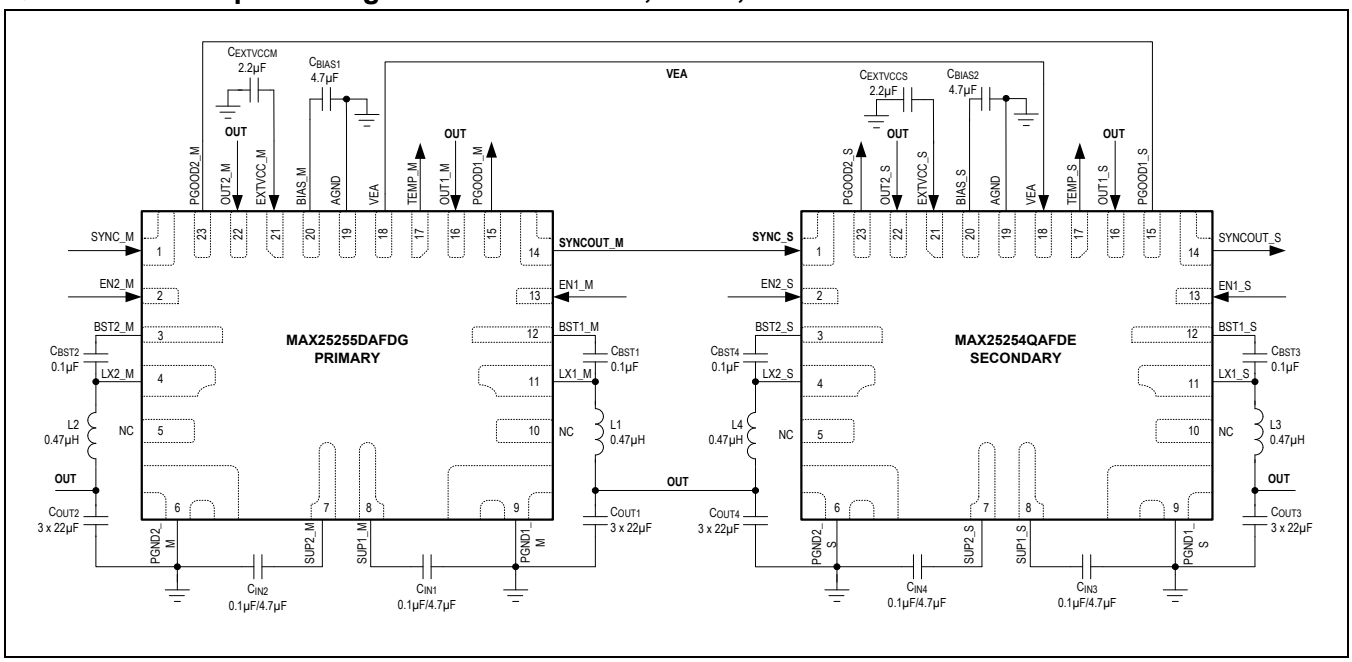
Dual-Output Configuration: MAX25254, 400kHz, 5V/3.3V



Dual-Phase Output Configuration: MAX25255, 2MHz, 3.3V



Quad-Phase Output Configuration: MAX25255, 2MHz, 5V



Ordering Information

PART NUMBER	PHASE CONFIGURATION	I_{LIM} (A)	SWITCHING FREQUENCY	SAFETY	V_{OUT1} (V)	V_{OUT2} (V)	I_{DC} (A)	SPREAD SPECTRUM
DUAL CHANNELS								
MAX25255AFDA/VY+	Two separated outputs	10.5	2MHz	ASIL	5	3.3	6	ON, ±6%
MAX25255AFDB/VY+	Two separated outputs	12	400kHz	ASIL	5	3.3	8	OFF
MAX25254AFDC/VY+	Two separated outputs	10.5	2MHz	Non-ASIL	5	3.3	6	ON, ±6%
MAX25254AFDD/VY+*	Two separated outputs	12	400kHz	Non-ASIL	5	3.3	8	OFF
MAX25254AFDE/VY+	Two separated outputs	10.5	2MHz	Non-ASIL	ADJ	ADJ	6	ON, ±6%
MAX25254AFDF/VY+	Two separated outputs	12	400kHz	Non-ASIL	3.3	3.3	8	ON, ±6%
DUAL PHASE								
MAX25255DAFDA/VY+	Single output, primary	10.5	2MHz	ASIL	3.3	3.3	6	ON, ±6%
MAX25255DAFDB/VY+*	Single output, primary	12	400kHz	ASIL	3.3	3.3	8	ON, ±6%
MAX25254DAFDC/VY+	Single output, primary	10.5	2MHz	Non-ASIL	3.3	3.3	6	ON, ±6%
MAX25254DAFDD/VY+	Single output, primary	12	400kHz	Non-ASIL	3.3	3.3	8	ON, ±6%
MAX25254DAFDE/VY+*	Single output, primary	10.5	2MHz	Non-ASIL	5	5	6	ON, ±6%
MAX25254DAFDF/VY+*	Single output, primary	12	400kHz	Non-ASIL	5	5	8	ON, ±6%
MAX25255DAFDG/VY+	Single output, primary	10.5	2MHz	ASIL	5	5	6	ON, ±6%
MAX25255DAFDH/VY+	Single output, primary	12	400kHz	ASIL	5	5	8	ON, ±6%
MAX25254DAFDJ/VY+	Single output, primary	12	400kHz	Non-ASIL	ADJ	ADJ	8	OFF
MAX25254DAFDK/VY+*	Single output, primary	10.5	2MHz	Non-ASIL	ADJ	ADJ	6	ON, ±6%
QUAD PHASE								
MAX25254QAFDA/VY+	Single output, secondary	10.5	2MHz	Non-ASIL	3.3	3.3	6	Controlled by primary IC
MAX25254QAFDB/VY+	Single output, secondary	12	400kHz	Non-ASIL	3.3	3.3	8	Controlled by primary IC
MAX25254QAFDE/VY+*	Single output, secondary	10.5	2MHz	Non-ASIL	5	5	6	Controlled by primary IC
MAX25254QAFDF/VY+*	Single output, secondary	12	400kHz	Non-ASIL	5	5	8	Controlled by primary IC

** Potential future part.*
+ Denotes a lead(Pb)-free/RoHS-compliant package.
/VY Denotes a side-wettable, automotive-qualified package.
Devices are also available in tape-and-reel packaging. Specify tape and reel by adding "T" to the part number when ordering.

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	4/22	Initial release	—
1	4/22	Updated Ordering Information table	25
2	6/22	Updated Electrical Characteristics, Typical Application Circuits, and Ordering Information table	4, 22, 23
3	9/22	Updated Ordering Information table	23
4	12/22	Updated Ordering Information table	23
5	1/23	Updated Ordering Information table	23
6	4/23	Updated Typical Operating Characteristics and Ordering Information table	10, 23
7	9/23	Updated Package Information and Ordering Information table	3, 23
8	2/24	Updated Ordering Information table	23
9	4/24	Updated General Description, Benefits and Features, Electrical Characteristics, and Ordering Information table	1, 4, 23
10	6/24	Updated General Description, Electrical Characteristics, Detailed Description, Multiphase Operation, PCB Layout Guidelines, and Ordering Information table	1, 14, 16, 23
11	4/25	Updated Title, Electrical Characteristics, and Pin Description	1, 3, 18
12	8/25	Updated Detailed Description	15