Four-Output Mini PMIC for Camera Applications

MAX25250

General Description

The MAX25250 is a high-efficiency, four-output PMIC that integrates three DC-DC converters and a high-PSRR LDO, with OV/UV monitoring on all outputs. OUT1 is a 1A high-voltage synchronous step-down converter operating from power over coax or car battery. OUT2 and OUT3 low-voltage synchronous step-down converters operate from OUT1 and provide a 0.8V to 3.9875V output voltage range. OUT2 can deliver 1.2A for high megapixel cameras and high-speed serializers. OUT3 can deliver 1.2A to power the secondary rails of the imager, serializer, and MCU. OUT4 is a low-voltage, low-noise, high-PSRR LDO for imager power. All buck converters achieve ±1.5% output voltage accuracy over load, line, and temperature range. Overvoltage and undervoltage faults are monitored and errors are communicated through $\overline{\text{RESET}}$.

This device features a 2.2MHz fixed-frequency PWM mode for better noise immunity and load-transient response. The high-frequency operation allows for the use of all ceramic capacitors and minimizes external components. The programmable spread-spectrum frequency modulation minimizes radiated electromagnetic emissions. Integrated low-$R_{DS(ON)}$ switches improve efficiency at heavy loads and make layout simpler than discrete solutions.

Sequencing through the use of EN23 and EN4 pins and factory-settable output voltages increases flexibility for different image sensors and configurations. Other features include soft-start, overcurrent, and overtemperature protection. The MAX25250 is specified for operation over the -40°C to +125°C automotive temperature range.

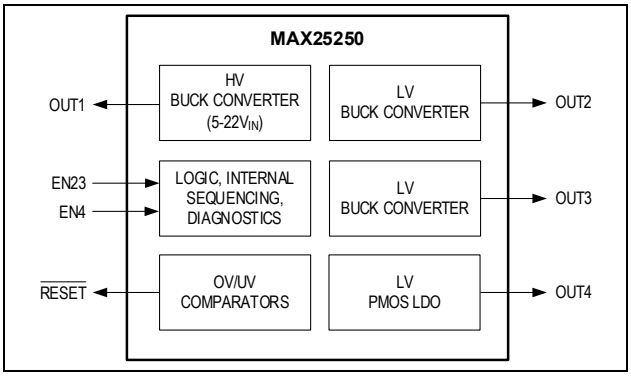
Applications

- Surround-View Cameras
- Rear-View Cameras

Benefits and Features

- Multiple Functions for Small Size
  - 1A Synchronous High-Voltage Buck Converter
    - Input Voltage Range 5V to 22V
    - 3V to 4V, and 5V Output Voltage in 50mV Steps
  - Two Synchronous Low-Voltage Buck Converters
    - OUT2 and OUT3 Provide up to 1.2A
    - 0.8V to 3.9875V in 12.5mV Steps
  - LDO for Camera Sensor; 50dB at 1kHz
  - 2.2MHz Operation
  - $\overline{\text{RESET}}$ Output – Open Drain
  - High Precision
    - ±1.5% Output Voltage Accuracy
    - OV/UV Monitoring
- Robust for the Automotive Environment
  - Current-Mode, Forced-PWM Operation
  - Overtemperature and Short-Circuit Protection
  - 3.5mm x 3.5mm, 20-Pin TQFN
  - -40°C to +125°C Grade 1 Automotive Temperature Range
  - AEC-Q100 Qualified

Simplified Block Diagram



Ordering Information **appears at end of data sheet.**

19-100966; Rev 4; 8/26

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Absolute Maximum Ratings

SUP1, LX1 to PGND_ ..... -0.3V to +24V
BST1 to LX1 ..... -0.3V to +6V
EN23, EN4 to AGND ..... -0.3V to +6V
PV2, PV3, PV4 to PGND_ ..... -0.3V to +6V
BIAS to AGND ..... -0.3V to +6V
$\overline{RESET}$ to AGND (MAX25250) ..... -0.3V to 6V
OUTS1, OUTS2, OUTS3 to AGND ..... -0.3V to +6V
OUTS4 to PGND ..... -0.3V to PV4+0.3V
LX1 to PGND1 (*Note 1*) ..... -0.3V to V_{SUP1}+0.3V
LX2 to PGND2 (*Note 1*) ..... -0.3V to PV2+0.3V
LX3 to PGND3 (*Note 1*) ..... -0.3V to PV3+0.3V
AGND to PGND_ ..... -0.3V to +0.3V
LX1 Short-Circuit Duration ..... Continuous
LX2 Short-Circuit Duration ..... Continuous
LX3 Short-Circuit Duration ..... Continuous
Continuous Power Dissipation (T_A = +70°C) 20 TQFN-EP (derate 23.8 mW/°C > 70°C) 1904mW
Operating Temperature ..... -40°C to +125°C
Junction Temperature ..... +150°C
Storage Temperature Range ..... -65°C to +150°C
Lead Temperature Range ..... +300°C

Note 1: Self-protected against transient voltages exceeding these limits for ≤ 50ns under normal operation and loads up to the maximum rated output current.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Recommended Operating Conditions

PARAMETER	SYMBOL	CONDITION	TYPICAL RANGE	UNIT
Ambient Temperature Range			-40 to +125	°C

Note: *These limits are not guaranteed.*

Package Information

20 TQFN-EP

Package Code	T203A3Y+1C
Outline Number	*21-100306*
Land Pattern Number	*90-100103*
THERMAL RESISTANCE, FOUR-LAYER BOARD	
Junction to Ambient (θ_{JA})	40.4°C/W
Junction to Case (θ_{JC})	2.4°C/W

For the latest package outline information and land patterns (footprints), go to the Package Index on the Analog Devices website. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to Thermal Characterization of IC Packages.

Electrical Characteristics

(V_{SUP1} = 13.5V, V_{EN23} = V_{EN4} = V_{BIAS}, V_{OUT1} = V_{PV2} = V_{PV3} = V_{PV4} = 3.1V, T_A = -40°C to +125°C, T_J = -40°C to +150°C, unless otherwise noted, Typical values are at T_A = +25°C. (*Note 3* and *Note 4*))

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Supply Voltage Range	V_{SUP}	Fully operational	5		22	V
Supply Current	I_{SUP}	No load, no switching all four channels		3		mA
Supply UVLO	UVLOR	Rising		4.5	4.9	V
	UVLOF	Falling (default)	3.5	4		
BIAS Voltage		5.5V ≤ V_{SUP} ≤ 22V		5		V
BIAS Current Limit			10			mA
OUT1 (HV BUCK)						
Voltage Accuracy		5V ≤ V_{SUP} ≤ 17V, I_{OUT1} = 0 to 1000mA, V_{OUT1} = 3.1V	-1.5		1.5	%
Output Voltage Range		50mV steps (fixed 5V OUT1 available) (*Note 2*)	3		4	V
High-Side nMOS On-Resistance		V_{BIAS} = 5V, I_{LX1} = 0.3A		300		mΩ
Low-Side nMOS On-Resistance		V_{BIAS} = 5V, I_{LX1} = 0.3A		200		mΩ
High-Side Current-Limit Threshold			1.3	1.5	1.7	A
Switching Phase		(*Note 2*)		0		deg
OUT1 Discharge Resistance				50		Ω
Soft-Start				0.75		ms
OUT2 (LV BUCK)						
Voltage Accuracy		3.0V ≤ PV2 ≤ 5V, I_{OUT2} = 0 to 1200mA, V_{OUT2} = 1.8V, 1.1V	-1.5		1.5	%
Output Voltage Range		12.5mV steps (*Note 2*)	0.8		3.9875	V
High-Side pMOS On-Resistance		I_{LX2} = 0.2A		180		mΩ
Low-Side nMOS On-Resistance		I_{LX2} = 0.2A		70		mΩ
High-Side, Current-Limit Threshold		1.2A option	1.00	1.20	1.40	A
		2A option	1.60	2.05	2.50	
LX2 Leakage Current		T_A = +25°C		0.1		µA
Switching Phase		(*Note 2*)		180		deg
LX2 Discharge Resistance				50		Ω
Soft-Start Time				1		ms
Dead Time		I_{OUT} = 500mA (*Note 2*)		2		ns
LX Rise/Fall Time		I_{OUT} = 500mA (*Note 2*)		2		ns
OUT3 (LV BUCK)						
Voltage Accuracy		3.0V ≤ PV3 ≤ 5V, I_{OUT3} = 0 to 500mA, V_{OUT3} = 1.8V, 1.1V	-1.5		+1.5	%
Output Range		12.5mV steps (*Note 2*)	0.8		3.9875	V
High-Side pMOS On Resistance		I_{LX1} = 0.2A		180		mΩ

(V_{SUP1} = 13.5V, V_{EN23} = V_{EN4} = V_{BIAS}, V_{OUT1} = V_{PV2} = V_{PV3} = V_{PV4} = 3.1V, T_A = -40°C to +125°C, T_J = -40°C to +150°C, unless otherwise noted, Typical values are at T_A = +25°C. (Note 3 and Note 4))

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Low-Side nMOS On Resistance		I_{LX1} = 0.2A		70		mΩ
High-Side, Current-Limit Threshold		1A option	0.80	1.07	1.40	A
		2A option	1.60	2.30	2.90	
LX3 Leakage Current		T_A = +25°C		0.1		µA
Switching Phase		In phase with BUCK1 (Note 2)		0		deg
LX3 Discharge Resistance				50		Ω
Soft-Start Time				1		ms
Dead Time		I_{OUT} = 200mA (Note 2)		2		ns
LX Rise/Fall Time		I_{OUT} = 200mA (Note 2)		2		ns
OUT4 (LDO)						
Supply Voltage Range	V_{PV4}		2.7		5.5	V
Output Voltage Range	V_{OUT4}	12.5mV steps (Note 2)	0.8		3.9875	V
Voltage Accuracy	V_{OUT4}	I_{OUT4} = 0A to 150mA, 3.1V ≤ PV4 ≤ 5V (OUT4 voltage accuracy of ±1.5% is guaranteed between 2.5V and 3.5V)	-1.5		+1.5	%
Dropout		I_{OUT4} = 0.15A, V_{LDO4} = 2.7V			180	mV
Current-Limit Threshold			0.35			A
PSRR		V_{PV4} = 3.1V, V_{OUT4} = 2.8V, I_{OUT4} = 0.05A, f = 1kHz (Note 2)		50		dB
OUT4 Discharge Resistance				70		Ω
Soft-Start Time				1		ms
OSCILLATOR						
Frequency	f_{SW}	Internally generated	2	2.2	2.4	MHz
Spread Spectrum		Factory OTP		±3		%
THERMAL OVERLOAD						
Thermal Shutdown Temperature		T_J rising (Note 2)		175		°C
Thermal Shutdown Hysteresis		(Note 2)		15		°C
$\overline{\text{RESET}}$						
OV Threshold		Rising	102.4	105.5	108	%
		Rising (contact factory for option)	102.4	103.7	105	
UV Threshold		Falling	92	94,5	97.6	%
		Falling (contact factory for option)	95	96.3	97.6	
Active Hold Period		Factory OTP = 18ms		18		ms
Output Low Level		3mA			0.2	V
Leakage Current		T_A = +25°C (open-drain)			1	µA
OV/UV Debounce Time				60		µs
ENABLE INPUT (EN23, EN4)						
Input High Level	V_{IH}	Not to exceed V_{BIAS}	1.4			V

(V_{SUP1} = 13.5V, V_{EN23} = V_{EN4} = V_{BIAS}, V_{OUT1} = V_{PV2} = V_{PV3} = V_{PV4} = 3.1V, T_A = -40°C to +125°C, T_J = -40°C to +150°C, unless otherwise noted, Typical values are at T_A = +25°C. (*Note 3* and *Note 4*))

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Input Low Level	V_{IL}				0.5	V
Input Hysteresis	V_{IHYS}			0.1		V
Input Leakage Current	I_{LKG}	$V_{EN_}$ = 5.5V, T_A = +25°C		9.5		µA
Pull-Down Resistance				580		kΩ

Note 2: Guaranteed by design; not production tested.

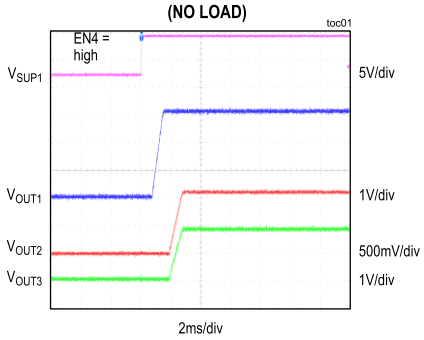
Note 3: Limits are 100% production tested at T_A = +25°C. Limits over the operating temperature range and relevant supply voltage are guaranteed by design and characterization.

Note 4: The device is designed for continuous operation up to T_J = +125°C for 95,000 hours and T_J = +150°C for 5,000 hours.

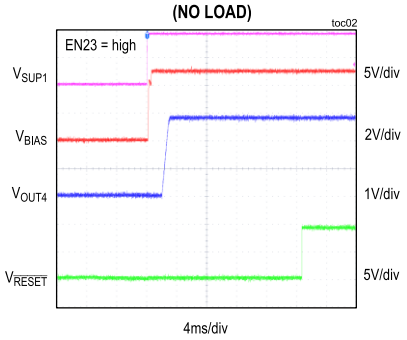
Typical Operating Characteristics

(V_{SUP} = 9V, T_A = +25°C, unless otherwise noted)

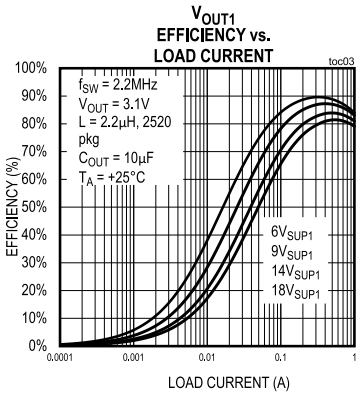
STARTUP WAVEFORM (NO LOAD)



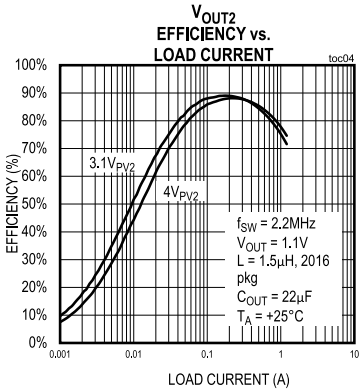
STARTUP WAVEFORM (NO LOAD)



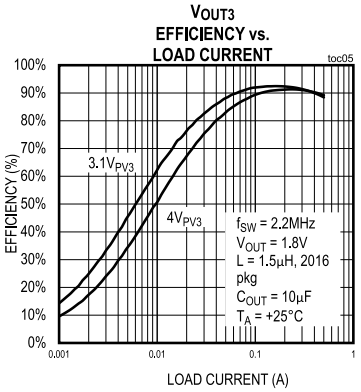
VOUT1 EFFICIENCY vs. LOAD CURRENT



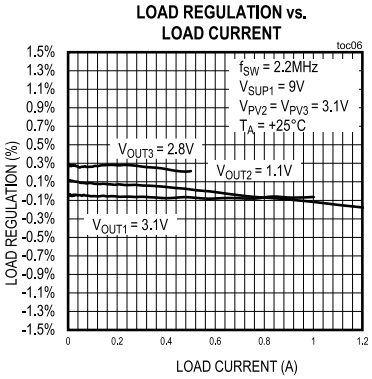
VOUT2 EFFICIENCY vs. LOAD CURRENT



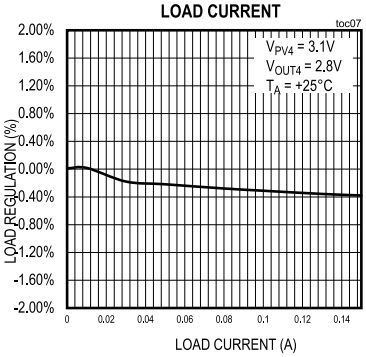
VOUT3 EFFICIENCY vs. LOAD CURRENT



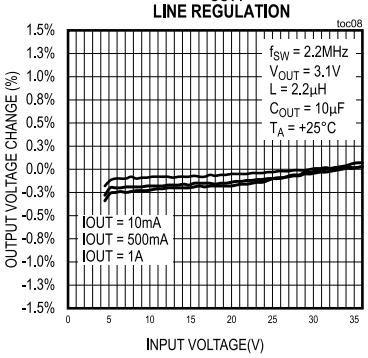
LOAD REGULATION vs. LOAD CURRENT



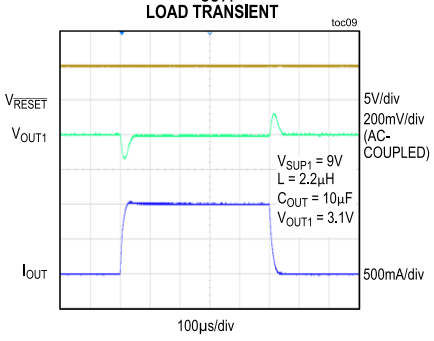
LDO LOAD REGULATION vs. LOAD CURRENT



VOUT1 LINE REGULATION

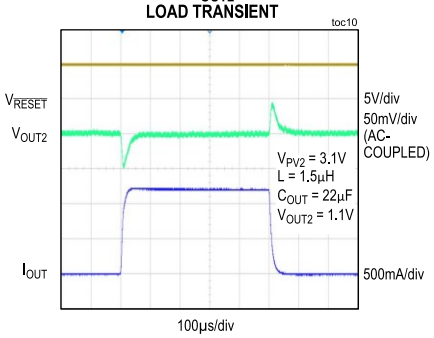


VOUT1 LOAD TRANSIENT

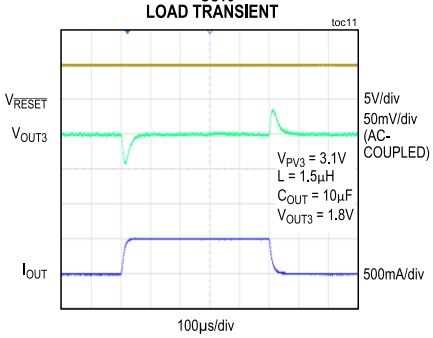


(V_{SUP} = 9V, T_A = +25°C, unless otherwise noted)

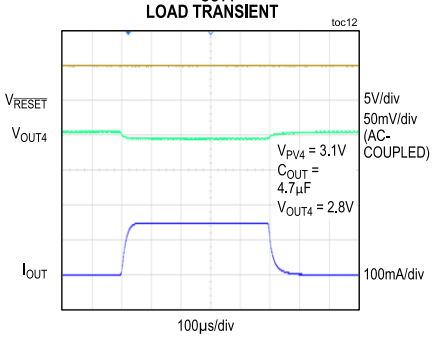
V_{OUT2} LOAD TRANSIENT



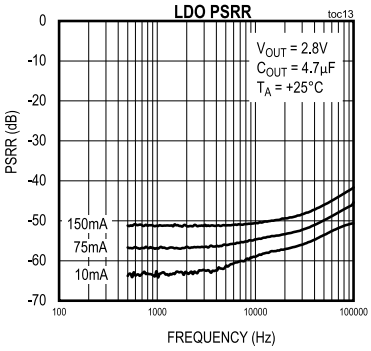
V_{OUT3} LOAD TRANSIENT



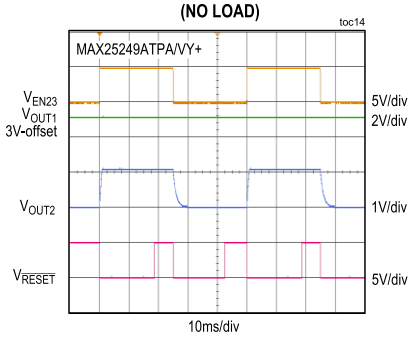
V_{OUT4} LOAD TRANSIENT



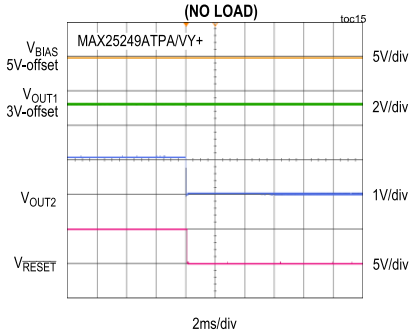
V_{OUT4} VPV4 = 3.3V LDO PSRR



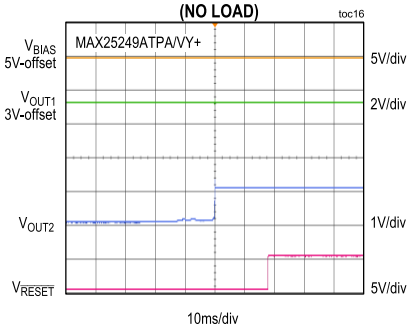
EN TOGGLE SAFE-SHUTDOWN DISABLED (NO LOAD)



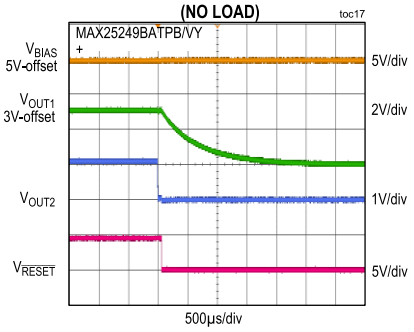
ENTER SHORT CIRCUIT ON V_{OUT2} SAFE-SHUTDOWN DISABLED (NO LOAD)



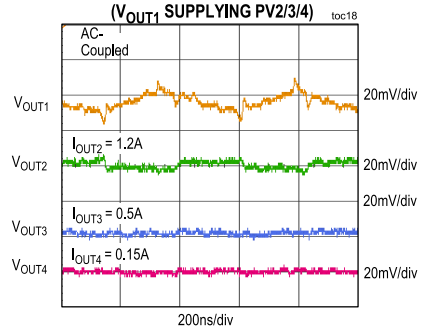
EXIT SHORT-CIRCUIT ON V_{OUT2} SAFE-SHUTDOWN DISABLED (NO LOAD)



ENTER SHORT CIRCUIT ON V_{OUT2} SAFE-SHUTDOWN ENABLED (NO LOAD)

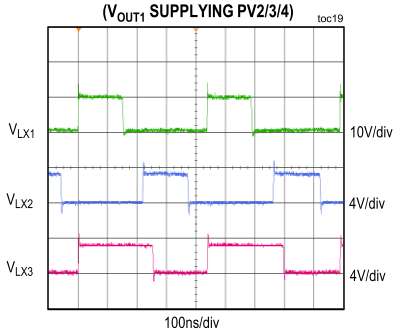


OUTPUT VOLTAGE RIPPLE (FULL LOAD) (V_{OUT1} SUPPLYING PV2/3/4)

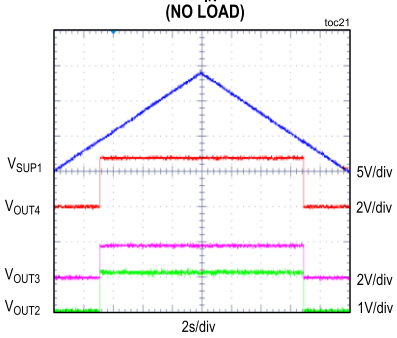


(V_{SUP} = 9V, T_A = +25°C, unless otherwise noted)

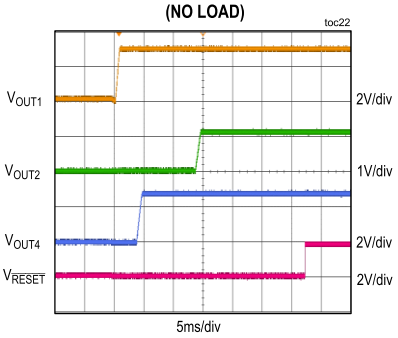
LX SWITCHING WAVEFORM
(NO LOAD)
(V_{OUT1} SUPPLYING PV2/3/4)



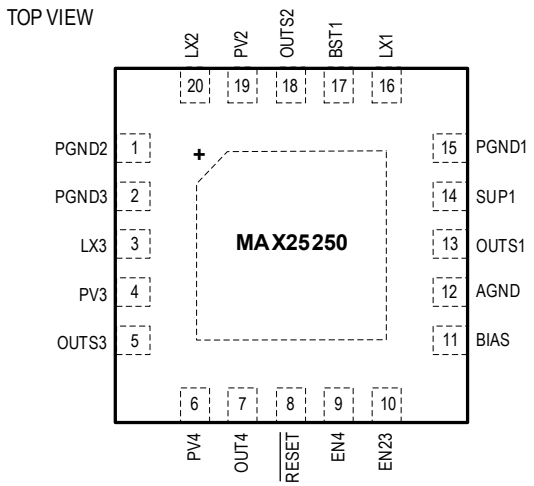
SLOW V_{IN} RAMP
(NO LOAD)



STARTUP EN SEQUENCING
(NO LOAD)



Pin Configuration



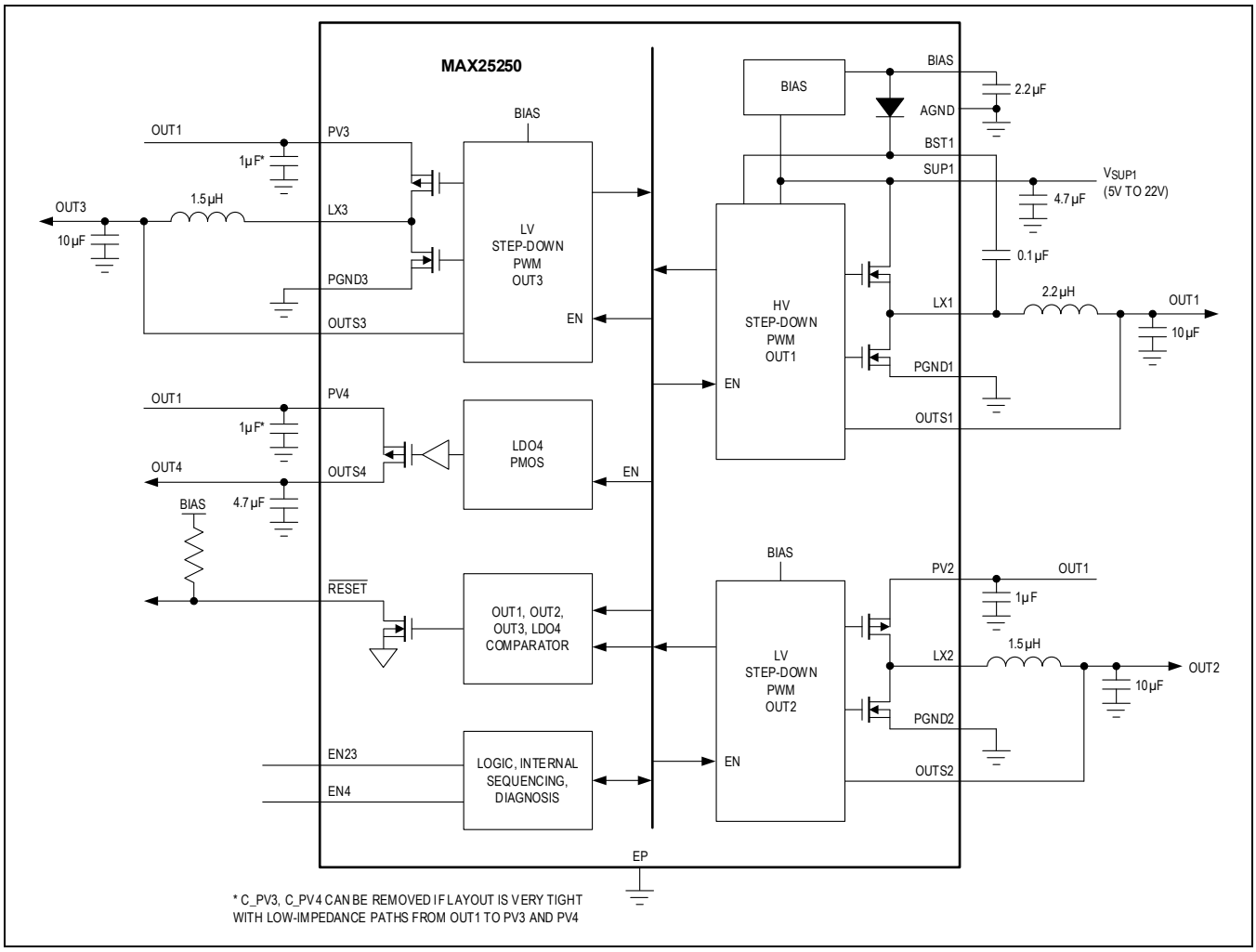
TQFN
3.5mm x 3.5mm

Pin Descriptions

Pin Descriptions

PIN	NAME	FUNCTION
1	PGND2	Power Ground for OUT2. Connect all PGND pins together.
2	PGND3	Power Ground for OUT3. Connect all PGND pins together.
3	LX3	Inductor Connection for BUCK3
4	PV3	Input Voltage for BUCK3
5	OUTS3	BUCK3 Output Voltage-Sense Input
6	PV4	Input Voltage for LDO4
7	OUT4	LDO4 Output. Place a 4.7µF or larger X7R ceramic capacitor as close as possible from OUT4 to PGND.
8	$\overline{\text{RESET}}$	Open-Drain $\overline{\text{RESET}}$ Output. This output remains low for the 18ms hold time (factory OTP) after all outputs have reached their regulation level. (See the *Electrical Characteristics* table.)
9	EN4	Low-Voltage-Compatible Enable Input for LDO4. Pull low to turn off LDO4. Pull high to turn on LDO4.
10	EN23	Low-Voltage-Compatible Enable Input for BUCK2 and BUCK3. Pull low to turn off both bucks. Pull high to turn on both bucks. Delay between BUCK2 and BUCK3 is factory-programmed (0ms, 1ms, 3ms, 10ms).
11	BIAS	5V Regulator Output. Bypass to AGND with a 2.2µF or larger X7R ceramic capacitor.
12	AGND	Analog Ground. Connect to the ground plane near the exposed pad.
13	OUTS1	BUCK1 Output Voltage-Sense Input
14	SUP1	IC Supply-Voltage Input and High-Side Connection for BUCK1. Connect a 4.7µF or larger X7R ceramic capacitor from SUP1 to PGND1.
15	PGND1	Power Ground for BUCK1. Connect all PGND pins together.
16	LX1	Inductor Connection for BUCK1
17	BST1	Bootstrap Capacitor Connection for BUCK1. Connect a 0.1µF X7R ceramic capacitor between BST and LX1.
18	OUTS2	BUCK2 Output Voltage-Sense Input
19	PV2	Voltage Input for BUCK2
20	LX2	Inductor Connection for BUCK2
—	EP	Exposed Pad. Internally connected to GND. Connect to a large ground plane to maximize thermal performance. Not intended as an electrical connection point.

Functional Diagram



Detailed Description

Summary

The MAX25250 is a high-efficiency, four-output PMIC using three DC-DC converters, and a high-PSRR LDO, with OV/UV monitoring on all outputs. OUT1 is a 1A high-voltage synchronous step-down converter that operates from power over coax or car battery. OUT2 and OUT3 low-voltage synchronous step-down converters operate from OUT1 and provide a 0.8V to 3.9875V output voltage range. OUT2 can deliver 1.2A for high megapixel cameras and high-speed serializers. OUT3 can deliver 1.2A to power the secondary rails of the imager, serializer, and micro. OUT4 is a low-voltage, lownoise, high-PSRR LDO for imager power. All buck outputs achieve ±2% output error over load, line, and temperature range. Overvoltage and undervoltage faults are monitored with ±1.3% accuracy around the set voltage and errors are communicated through $\overline{\text{RESET}}$.

Startup Timing and Soft-Start

V_{OUT1} has a soft-start time of 0.75ms and the other channels start up in 1ms. The sequencing is controlled by the EN23 and EN4 pins, as well as the factory OTP set delay time between the V_{OUT2} and V_{OUT3}. For the MAX25250, $\overline{\text{RESET}}$ will toggle high as long as either EN23 or EN4 are high. Whenever an EN pin changes state, $\overline{\text{RESET}}$ will toggle. See *Figure 1*.

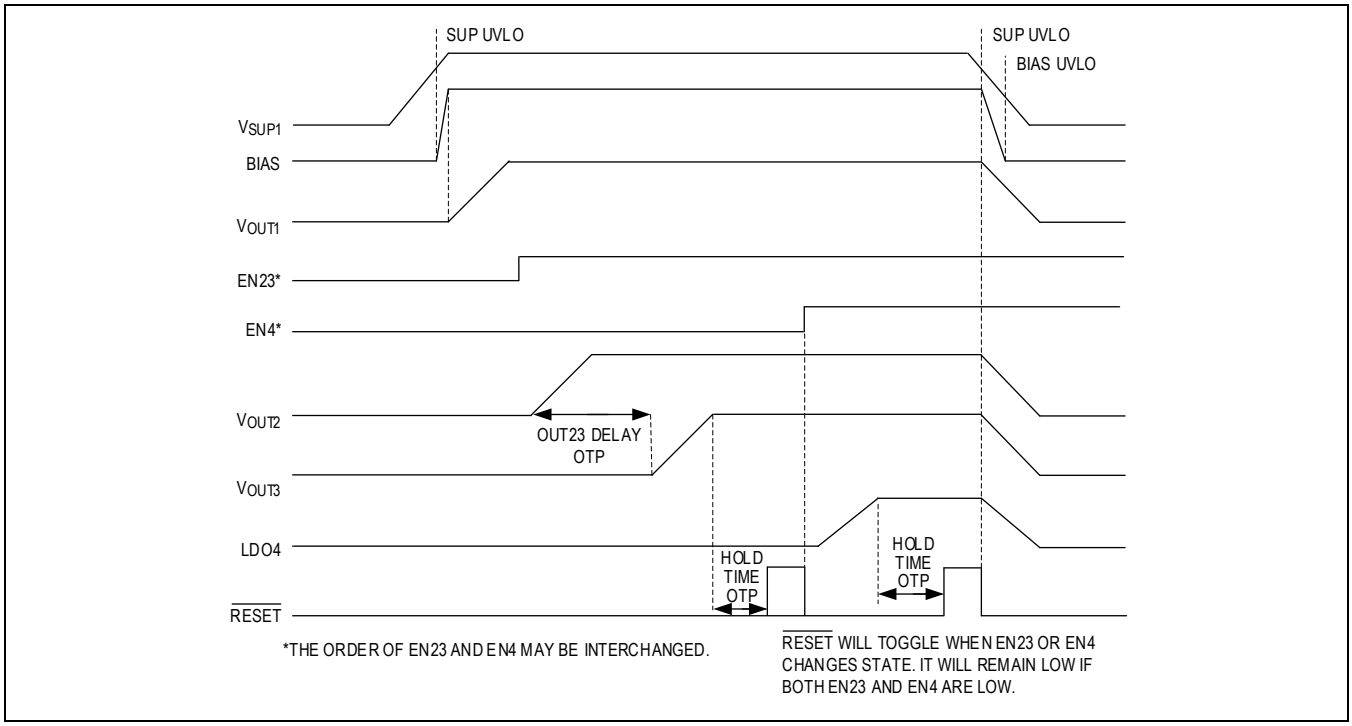


Figure 1. Startup Timing Diagram

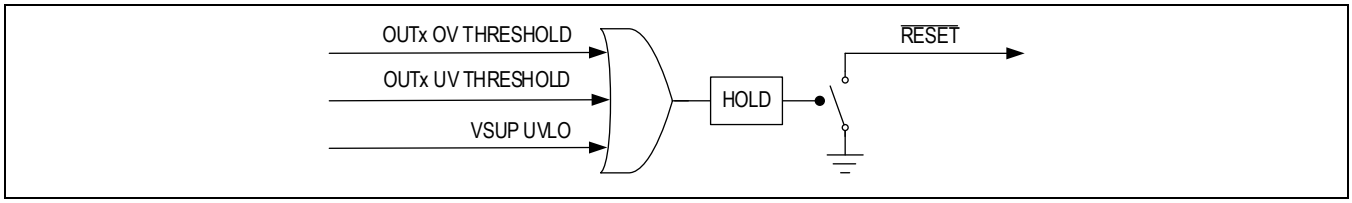


Figure 2. Simplified $\overline{\text{RESET}}$ Logic Diagram

$\overline{\text{RESET}}$ Output

The device is configured with an open-drain $\overline{\text{RESET}}$ output that asserts low when any of the output voltages are outside of the UV/OV window, or when the supply voltage falls below the UV threshold. After all, voltages reach the regulated

voltage during startup, $\overline{\text{RESET}}$ remains asserted low for an 18ms hold time (factory OTP option of 4.5ms, 9ms, or 18ms). Besides, $\overline{\text{RESET}}$ is designed to toggle and remain low for the hold time when one or both of the EN pins are deasserted. The timing is shown in *Figure 3*. This pin can be used as an interrupt for an MCU or error-monitoring device to alert the system that a fault has occurred.

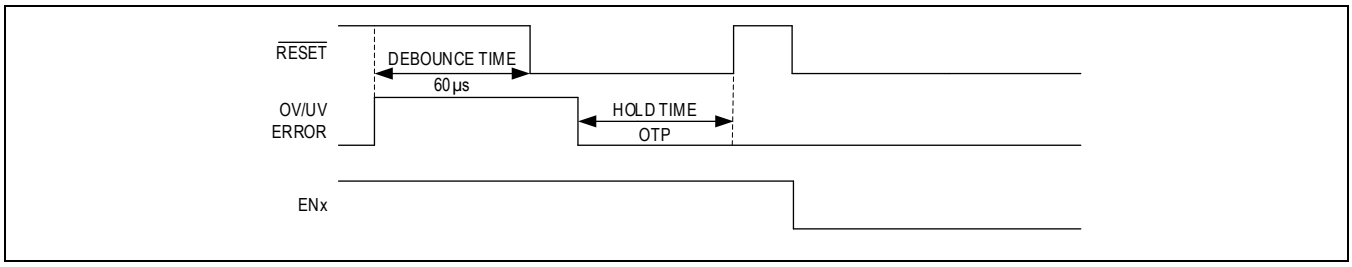


Figure 3. $\overline{\text{RESET}}$ During Normal Operation

Active Pull-Down

OUT2, OUT3, and LDO4 contain pull-down resistors that activate during shutdown when EN23 or EN4 are toggled low, or if there is a fault that triggers safe shutdown. During startup, if one of the outputs is prebiased, the pull-down is activated until the rail drops to 0V, at which point the soft-start of the rails begins. This ensures proper sequencing of the rails if there is a long glitch on SUP1.

OV/UV Comparators

All four rails are monitored with overvoltage and undervoltage comparators at the feedback node. These comparators are tested at startup and provide continuous monitoring of output voltages during normal operation. If an error exists, then $\overline{\text{RESET}}$ is pulled low until the OV/UV condition is resolved. The comparators have a built-in filter time (60µs), which prevents short transient voltages that exceed OV/UV threshold from triggering $\overline{\text{RESET}}$.

Buck Converter Current-Limit/Short-Circuit Protection

The MAX25250 buck converters have current limits to protect the device against short-circuit and overload conditions at the output. During such an event, the high-side MOSFET remains on until the inductor current reaches the high-side MOSFET's current-limit threshold. Then, the converter turns on the low-side MOSFET to allow the inductor current to ramp down. Once the inductor current crosses below the low-side MOSFET's current-limit threshold, the converter turns on the high-side MOSFET again. For OUT2/3, this cycle repeats until the short or overload condition is removed, thermal shutdown is reached, or the channel's UV is met. For OUT1, this cycle repeats until the short or overload condition is removed, thermal shutdown is reached, or the channel's UV is met.

If four consecutive current high-side MOSFET current-limit thresholds are reached on OUT1, the MAX25250 shuts down and pulls $\overline{\text{RESET}}$ low. After the MAX25250 shuts down, the MAX25250 waits for 2.3ms (typ) before restarting and continues to restart until the condition that causes the shutdown is removed or the MAX25250 is turned off.

Spread-Spectrum Option

The MAX25250 has a factory-programmable spread spectrum that varies the internal operating frequency by ±3%, relative to 2.2MHz (typ). Spread spectrum is offered to improve EMI performance of the devices.

Thermal Shutdown

If an overtemperature condition is detected during power sequencing, the startup will cease and outputs will enter thermal shutdown. Once the temperature is reduced, power sequencing will be restarted. The startup check routine is not reinitiated. If safe shutdown is enabled, the IC will shut down when overtemperature is detected and remain in this state even if the part cools down. The device must be restarted through input power cycling.

Applications Information

Output-Voltage Selection

Output voltages are set at the factory. Default configurations can be found in the *Ordering Information* table.

Other options are available as follows:

Table 1. Output Voltage Options

OUTPUT	VOLTAGE (V)	STEP SIZE (mV)
OUT1	3–4, 5	50
OUT2	0.8–3.9875	12.5
OUT3	0.8–3.9875	12.5
LDO4	0.8–3.9875	12.5

Input Capacitor

The input filter capacitor reduces peak currents drawn from the power source and reduces noise and voltage ripple on the input caused by the circuit's switching. A 1µF or larger X7R ceramic capacitor is recommended for PV2, PV3, and PV4 pins. For the SUP1 pin, a 4.7µF or larger X7R ceramic capacitor minimum is recommended, and it can be adjusted based on application input-voltage-ripple requirements.

Output Capacitor

The MAX25250 is designed to be stable with low-ESR ceramic capacitors. Other capacitor types are not recommended, as the ESR zero can affect the stability of the device. The phase margin must be measured on the final circuit to verify that proper stability is achieved. The minimum recommended value for each part number is shown in *Table 2*.

Table 2. Minimum Output Capacitor Selection

PART NUMBER	C_{OUT1} (µF)	C_{OUT2} (µF)	C_{OUT3} (µF)	C_{OUT4} (µF)
MAX25250ATPA/VY+	10	10	10	4.7

Inductor Selection

The MAX25250 is optimized to be used with inductor values shown in *Table 3*. These were selected for power-over-coax and car-battery input voltages and common camera-output voltages. Camera systems are space constrained and require a trade-off in saturation current, case size, and inductor ripple current. The DCR of the inductor plays a major part in the overall system efficiency.

Table 3. Inductor Selection

PART NUMBER	L1	L2	L3
MAX25250ATPA/VY+	2.2	1.5	1.5

PCB Layout Guidelines

Careful PCB layout is critical to achieve low switching-power loss and clean, stable operation. The MAX25250 EV kit layout should be used as a reference when creating the board layout. Use a multilayer board for better noise immunity and thermal performance. Follow the guidelines below for a good PCB layout:

- Place the input capacitor immediately adjacent to the SUP1 and PV1, PV2, and PV3 pins. Since the IC operates at 2.2MHz switching frequency, this placement is critical for effective decoupling of high-frequency noise from the supply pins.
- Solder the exposed pad to a large copper-plane area under the device. To effectively use this copper area as a heat exchanger between the PCB and ambient, expose the copper area on the top and bottom side. Add vias on the copper pad for efficient heat transfer. Connect the exposed pad to the ground plane, ideally at the return terminal of the output capacitor.
- Isolate the power components and high-current paths from sensitive analog circuitry.
- Keep the high-current paths short, especially at the ground terminals. This practice is essential for stable, jitter-free operation.

- Connect PGND and AGND together, preferably at the return terminal of the output capacitor.
- Keep the power traces and load connections short. This practice is essential for high efficiency. Use thick copper PCB to enhance full-load efficiency and power-dissipation capability.
- Route high-speed switching nodes away from sensitive analog areas. Use internal PCB layers as PGND_ to act as EMI shields, keeping radiated noise away from the device and analog bypass capacitor.

Ordering Information

PART NUMBER	V_{OUT1} (V)	V_{OUT2} (V)	V_{OUT3} (V)	V_{OUT4} (V)	I_{LIM} OUT2/3 (A)	SPREAD SPECTRUM	EN TIMER (ms) (1)	OUT23 DELAY (ms) (2)	$\overline{RESET}$ HOLD TIME (ms) (1)	$\overline{RESET}$ OV RISING (%)	$\overline{RESET}$ UV FALLING (%)
MAX25250ATPA/VY+	3.75	1.2	1.8	3.3	1.2 / 1.2	On	N/A	0	18	105.5	94.5
MAX25250ATPC/VY+	3.3	1.8	1.2	2.8	1.2 / 1	On	N/A	0	18	103.7	96.3
MAX25250ATPD/VY+	3.75	1.2	1.8	3.3	1.2 / 1.2	On	N/A	0	18	103.7	96.3
MAX25250ATPG/VY+	5	3.3	1.8	3.9875	1.2 / 1	On	N/A	0	18	105.5	94.5

/V Denotes an automotive-qualified part.

+ Denotes a lead(Pb)-free/RoHS-compliant package.

Y = Side-wettable package.

***Note:** Contact factory for custom configuration. Factory-selectable features include the following:*

(1) Startup EN Timer, $\overline{RESET}$ Hold Time: 5ms, 10ms, 18ms

(2) OUT23 Delay: 0ms, 1ms, 3ms, 10ms

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	4/21	Release for Market Intro	—
1	10/22	Updated Detailed Description and Applications Information, added MAX25250ATPD/VY+ in Ordering Information	14–17
2	11/23	Added MAX25250ATPC/VY+ in Ordering Information and updated Absolute Maximum Ratings, Electrical Characteristics, Detailed Description, Applications Information, and Ordering Information	5-8, 15-18
3	8/26	Added MAX25250ATPG/VY+ in Ordering Information as a potential future product.	16
4	8/26	Removed * from MAX25250ATPG/VY+ in Ordering Information.	16

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