

MAX22215

Motor Brake Driver with Current-Sense Amplifier and Advanced Diagnostics

General Description

The MAX22215 integrates one 36V half-bridge FET, one 65V low-side NFET (brake-release NFET), and one unidirectional low-offset current-sense amplifier (CSA). It is primarily intended to drive electromechanical motor brakes and solenoids.

The coil current can be controlled both during the energization and demagnetization phases using pulse-width modulation (PWM), resulting in accurate control of excitation, hold, and demagnetization currents, as well as energizing and de-energizing timings.

The MAX22215 integrates a robust 55V demagnetization clamp, which allows fast demagnetization and eliminates the need of external clamp devices such as TVSs. The clamp features a safe demagnetization function that ensures safe operation by preventing the junction temperature from exceeding safety levels (SafeDemag™ function).

The half-bridge FETs and brake-release NFET feature extremely low $R_{DS(on)}$ (50mΩ, typ). The high efficiency and low power dissipation make the MAX22215 suitable for space-constrained applications in which high-power density on the PCB is a concern. The MAX22215 can drive up to 3A.

The high-accuracy CSA senses the voltage drop across an external sense resistor both during brake-engaged and brake-released operations. The CSA analog output signal can be used for diagnostic purposes or as feedback signal for an external control loop.

The device operation can be controlled either through a 1MHz I²C serial interface or by using CMOS logic input pins. When I²C is used, several device parameters such as the driver output slew rate and CSA gain can be configured. Moreover, the user has access to fault log registers for diagnostic purposes. Up to 16 devices can share the same I²C bus.

The MAX22215 integrates non-dissipative overcurrent protections (OCPs), undervoltage lockout (UVLO), thermal warning and shutdown, and a brake voltage monitor analog output pin (ODM). Other diagnostic functions have been integrated to detect improper load connections and device malfunctioning. A fault indicator pin (nFAULT) is activated every time a fault occurs.

The MAX22215 is available in a compact 5mm x 7mm, 38-pin TQFN package.

Applications

- Industrial Motor Brake Release
- Robotics Motor Brake Release
- Solenoid Drive

Benefits and Features

- One Half-Bridge Driver Operating up to 36V ($R_{ON} \sim 50m\Omega$)
- One LS FET Operating up to 65V ($R_{ON} \sim 50m\Omega$)
- Embedded Demagnetization Circuitry
 - 55V High-Power Clamp
 - Thermal Control Loop for Safe Operations at High-Demagnetization Energy (SafeDemag Function)
- 1MHz I²C Serial Interface for Configuration and Diagnostics
 - Configurable Half-Bridge Slew-Rate Control through I²C
- Embedded Dead-Time Circuit to Avoid Crossbar Conduction
- 5V Internal Regulator
- Current-Sense Amplifier (CSA)
 - Low Offset for High Accuracy
 - Programmable Voltage Gain
- Protections and Diagnostics
 - Overcurrent Protection (OCP)
 - Three Undervoltage Lockouts (UVLO₁₋₃)
 - Thermal Warning/Shutdown (T_{WARN}/T_{SD})
 - Demagnetization Voltage Analog Output Pin (ODM)
 - Diagnostic Mode for Load Connection Check
 - Internal Monitoring of System Parameters
 - Fault Indicator Pin (nFAULT)

Simplified Block Diagram

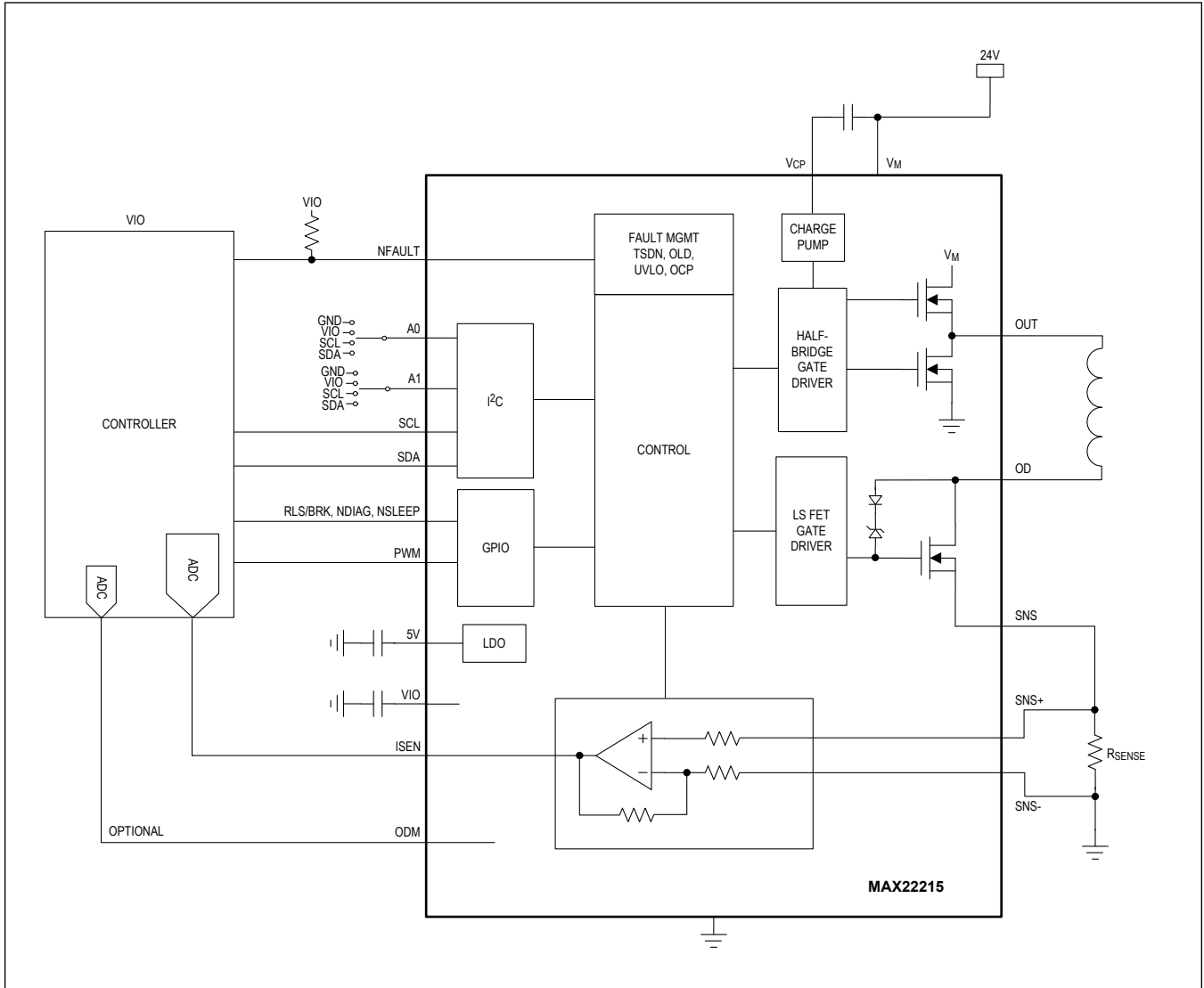


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Absolute Maximum Ratings

V_M to GND	-0.3V to +40V	SNS to GND.....	-0.3V to +0.3V
V_5 to GND	-0.3V to +6V	SNS+, SNS- to GND	-0.3V to +6V
V_{IO} to GND.....	-0.3V to +6V	ISEN to GND.....	-0.3V to $V_5 + 0.3V$
V_{CP} to V_M	-0.3V to +6V	FAULT to GND.....	-0.3V to +6V
OUT to GND	-0.3V to $V_M + 0.3V$	ODM to GND.....	-0.3V to $V_5 + 0.3V$
OD to GND (<i>Note 1</i>).....	-0.3V to +49V	PGND to GND.....	-0.3V to 0.3V
SLEEP, SCL, SDA, A1, A0, RLS/BRK, DIAG, PWM to GND.....	-0.3V to +6V	Operating Temperature Range	-40°C to +125°C

Note 1: Internally protected open-drain output pin. OD is internally clamped at +65V (max); AMV is representative of the minimum internal clamp voltage.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Package Information

38 TQFN (5mm x 7mm)

Package Code	T3857+1C
Outline Number	21-0172
Land Pattern Number	90-0076
Thermal Resistance, Single-Layer Board:	
Junction to Ambient (θ_{JA})	38°C/W
Junction to Case (θ_{JC})	1°C/W
Thermal Resistance, Four-Layer Board:	
Junction to Ambient (θ_{JA})	28°C/W
Junction to Case (θ_{JC})	1°C/W

For the latest package outline information and land patterns (footprints), go to www.analog.com/en/resources/packaging-quality-symbols-footprints/package-index.html. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7. For detailed information on package thermal considerations, refer to www.analog.com/en/resources/technical-articles/thermal-characterization-of-ic-packages.html.

Electrical Characteristics

($V_M = 8V$ to $36V$, $V_{IO} = +1.8V$ to $+5V$, no load connected to V_5 , $\overline{SLEEP} = V_{IO}$, $T_A = -40^\circ C$ to $+125^\circ C$, V_5 bypass capacitor = $1\mu F$, charge pump capacitor = $1\mu F$, Typical values are with $V_M = +24V$, $V_{IO} = +2.5V$, $T_A = +25^\circ C$, Limits are 100% tested at $T_A = +25^\circ C$. Limits over the operating temperature range and relevant supply voltage range are guaranteed by design and characterization. Specifications marked "GBD" are guaranteed by design and not production tested.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
VOLTAGE SUPPLIES						
V_M Supply Voltage Range	V_M		8		36	V
V_{IO} Supply Voltage Range	V_{IO}		1.65		5.5	V
SLEEP Mode Current Consumption	I_{SLEEP}	$V_M = 24V$; $\overline{SLEEP} = 0V$ or unconnected			450	μA

Electrical Characteristics (continued)

($V_M = 8V$ to $36V$, $V_{IO} = +1.8V$ to $+5V$, no load connected to V_5 , $\overline{SLEEP} = V_{IO}$, $T_A = -40^\circ C$ to $+125^\circ C$, V_5 bypass capacitor = $1\mu F$, charge pump capacitor = $1\mu F$, Typical values are with $V_M = +24V$, $V_{IO} = +2.5V$, $T_A = +25^\circ C$, Limits are 100% tested at $T_A = +25^\circ C$. Limits over the operating temperature range and relevant supply voltage range are guaranteed by design and characterization. Specifications marked "GBD" are guaranteed by design and not production tested.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Quiescent Current Consumption	I_{VM}	$V_M = 24V$; $\overline{SLEEP} = V_{IO}$, no output current			4.4	mA
Logic Input Supply Current	I_{IO}	Logic inputs to GND		10	18	μA
LOGIC CMOS INPUTS RLS/BRK, DIAG, PWM, \overline{SLEEP}						
Input Voltage Level - High	V_{IH}		0.8 x V_{IO}			V
Input Voltage Level - Low	V_{IL}		0.2 x V_{IO}			V
Logic Input Pull-down Resistor	R_{PD}	RLS/BRK, PWM, and \overline{SLEEP} pins	65	100	130	k Ω
Logic Input Pull-up Resistor to V_{IO}	R_{PU}	DIAG pin	65	100	130	k Ω
I²C LOGIC INPUTS SCL, SDA, A0, A1						
Input Voltage Level - High	V_{IH}		0.8 x V_{IO}			V
Input Voltage Level - Low	V_{IL}		0.2 x V_{IO}			V
Input Leakage Current	I_{IL}		-1		+1	μA
Input Capacitance	C_{IN}		10			pF
Output Low Voltage	V_{OL}	$I_{LOAD} = -3mA$, $V_{IO} \geq 2V$	0.4			V
		$I_{LOAD} = -3mA$, $V_{IO} < 2V$	0.2 x V_{IO}			
ODM MONITOR PIN						
Divider Ratio ROD1, ROD2	DIV0	ODM[1:0] = 00	15.75	16	16.25	V
	DIV1	ODM[1:0] = 01	20	20.4	20.8	
	DIV2	ODM[1:0] = 10 (default)	23.8	24.5	25	
	DIV3	ODM[1:0] = 11	58	60	62.5	
Equivalent Output Impedance	REQ0	ODM[1:0] = 00, $V_{OD} = V_M$	3.8			k Ω
	REQ1	ODM[1:0] = 01, $V_{OD} = V_M$	3.3			
	REQ2	ODM[1:0] = 10 (default), $V_{OD} = V_M$	3.1			
	REQ3	ODM[1:0] = 11, $V_{OD} = V_M$	2			
TIMINGS						
Power-up Timing	t_{POWUP}	From $V_M = 0$ to 24V, rising edge to normal operation; V_M rise time faster than 1ms		6	10	ms
Time from SLEEP to Any Mode	t_{OPER}				4	ms
Minimum BRAKE Time before Entering into SLEEP Mode from RELEASE Mode	t_{BRK_MIN}	Note 2	35.2	40	44.8	ms

Electrical Characteristics (continued)

($V_M = 8V$ to $36V$, $V_{IO} = +1.8V$ to $+5V$, no load connected to V_5 , $\overline{SLEEP} = V_{IO}$, $T_A = -40^\circ C$ to $+125^\circ C$, V_5 bypass capacitor = $1\mu F$, charge pump capacitor = $1\mu F$, Typical values are with $V_M = +24V$, $V_{IO} = +2.5V$, $T_A = +25^\circ C$, Limits are 100% tested at $T_A = +25^\circ C$. Limits over the operating temperature range and relevant supply voltage range are guaranteed by design and characterization. Specifications marked "GBD" are guaranteed by design and not production tested.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS	
Minimum BRAKE Time before Entering into DIAGNOSTIC Mode from RELEASE Mode	t_{BRK_MIN}	Note 4	35.2	40	44.8	ms	
Diagnostic Blanking Time	t_{BLK_DIAG}	Note 4	0.88	1	1.12	ms	
\overline{SLEEP} Deglitch Time	$t_{DEGLITCH}$		8		15	μs	
\overline{SLEEP} Reset Pulse Time	t_{RES}	Negative pulse	20		40	μs	
5V REGULATOR							
Voltage Output	V_5		4.75	5	5.25	V	
Output Current	I_{OUT}	Output current from pin V_5 (Note 3)			10	mA	
Regulator Output Current Protection	I_{V5}		25			mA	
HALF-BRIDGE DRIVER – OUT PIN							
Output ON-Resistance Low Side	$R_{ON(LS)}$			50		m Ω	
Output ON-Resistance High Side	$R_{ON(HS)}$			50		m Ω	
Pull-up Resistance	R_{PU}	Diagnostic mode	28	42	56	k Ω	
Dead Time – Fast Speed	DTFS	Low-to-high and high-to-low transition		450		ns	
Dead Time – SR1	DTSR1	Low-to-high transition only		650		ns	
Dead Time – SR2	DTSR2	Low-to-high transition only		1000		ns	
BRAKE-RELEASE LS NFET DRIVER – OD PIN							
Output ON-Resistance Low Side	$R_{ON(LS)}$			50		m Ω	
Output OFF-Resistance Low Side	R_{OFF}		28	40	56	k Ω	
Internal Fast Demagnetization Clamp Voltage	V_{FD}	Clamp current = 5mA	49		65	V	
SafeDemag AND ENFORCE DEMAG THRESHOLDS							
Enforce Demag Threshold	V_{DEM}	Falling edge	DEMAG bits = "001"	7.5	8	8.5	V
			DEMAG bits = "011"	11.2	12	12.8	
			DEMAG bits = "101"	15.5	16	17	
Enforce Demag Threshold Hysteresis	$V_{DEM(HYS)}$			1		V	

Electrical Characteristics (continued)

($V_M = 8V$ to $36V$, $V_{IO} = +1.8V$ to $+5V$, no load connected to V_5 , $\overline{SLEEP} = V_{IO}$, $T_A = -40^\circ C$ to $+125^\circ C$, V_5 bypass capacitor = $1\mu F$, charge pump capacitor = $1\mu F$, Typical values are with $V_M = +24V$, $V_{IO} = +2.5V$, $T_A = +25^\circ C$, Limits are 100% tested at $T_A = +25^\circ C$. Limits over the operating temperature range and relevant supply voltage range are guaranteed by design and characterization. Specifications marked "GDB" are guaranteed by design and not production tested.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
SafeDemag Trigger Temperature	T_{JDEM}				160		$^\circ C$
SafeDemag Temperature Hysteresis	T_{JHYS}				20		$^\circ C$
SLEW-RATE CONTROL WITH 1A INDUCTIVE LOAD							
Slew-Rate Control	SR0	SR[1:0] = 00			260		V/ μs
	SR1	SR[1:0] = 01			150		
	SR2	SR[1:0] = 10, default			70		
	SR3	SR[1:0] = 11			35		
PROTECTION CIRCUITS							
Undervoltage Lockout Threshold	UVLO	NFAULT pin		6.5		8	V
V_5 Undervoltage Lockout Threshold	UVLO V_5	Falling		3.55	3.9	4.2	V
Charge-Pump Undervoltage Lockout	UVLO $_{CP}$			2.1	2.8	3.6	V
Overcurrent Protection Threshold	OCPS	NFAULT pin		3			A
Overcurrent Restore Timing	OCPT	From fault reset to normal operation		17.6	20	22.4	ms
OCP Blanking Time	t_{BLK}				2		μs
Load Connection Verification Thresholds	V_{OD}	Diagnostic mode	Lower threshold (0.333 x V_M)	0.318 x V_M	0.333 x V_M	0.39 x V_M	V
			Upper threshold (0.667 x V_M)	0.64 x V_M	0.667 x V_M	0.718 x V_M	
DVD Detection Threshold	V_{DVD}			1.17 x V_M	1.25 x V_M	1.33 x V_M	V
DVD Detection Timing	t_{DVD}			44	50		μs
ISM Detection Threshold	ISM	ISEN threshold for ISM fault detection		34	40	65	mV
ISM Blanking Time	ISM_BLK	From entering in RELEASE mode to ISEN monitoring		176	200	224	ms
ODVM Detection Threshold	ODVM_TH			0.64 x V_M	0.667 x V_M	0.718 x V_M	V
Thermal Warning Temperature	T_{HW}				120		$^\circ C$
Thermal Shutdown Temperature	T_{HSD}				150		$^\circ C$
CURRENT-SENSE AMPLIFIER CSA							
Referred to Input Offset	V_{OS}	Common-mode voltage = 70mV				60	μV
Input Offset Drift	TCV $_{OS}$				0.15		$\mu V/^\circ C$

Electrical Characteristics (continued)

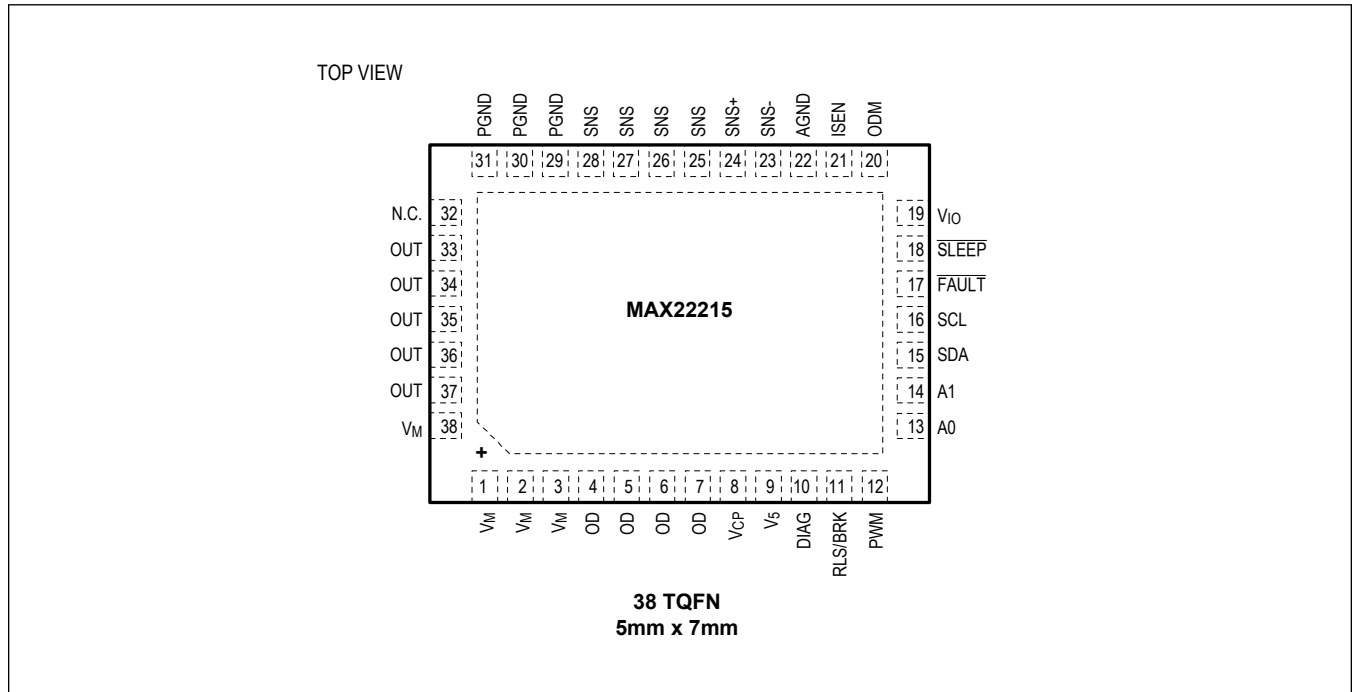
($V_M = 8V$ to $36V$, $V_{IO} = +1.8V$ to $+5V$, no load connected to V_5 , $\overline{SLEEP} = V_{IO}$, $T_A = -40^\circ C$ to $+125^\circ C$, V_5 bypass capacitor = $1\mu F$, charge pump capacitor = $1\mu F$, Typical values are with $V_M = +24V$, $V_{IO} = +2.5V$, $T_A = +25^\circ C$, Limits are 100% tested at $T_A = +25^\circ C$. Limits over the operating temperature range and relevant supply voltage range are guaranteed by design and characterization. Specifications marked "GBD" are guaranteed by design and not production tested.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Input Bias Current	IRS+				1	μA
Input Bias Current Offset	IRS+ - IRS-				1	μA
DIFF Input Resistance	R _{DIFF}		5	7.5	10	k Ω
Input Voltage Range	V _{IN}	GAIN[1:0] = 00	0		160	mV
		GAIN[1:0] = 01 (default)	0		80	
		GAIN[1:0] = 10	0		40	
		GAIN[1:0] = 11	0		20	
Maximum Linear Output Voltage	V _{OUTH}				4	V
Minimum Output Linear Voltage	V _{OUTL}		20			mV
Voltage Gain	GAIN1	GAIN[1:0] = 00	24.6	25	25.4	V/V
	GAIN2	GAIN[1:0] = 01 (default)	49.2	50	50.8	
	GAIN3	GAIN[1:0] = 10	98.8	100	101.2	
	GAIN4	GAIN[1:0] = 11	197.6	200	202.4	
Gain-Bandwidth Product	GBW			6		MHz
Output Capacitance on ISEN	CISEN			50		pF
CSA Output Slew Rate	SR			4		V/ μs
Input Voltage Noise Density (RTI)		At 1kHz		45		nV/ \sqrt{Hz}
I²C INTERFACE (Note 5)						
SCL Clock Frequency	t _{CLK}				1	MHz
Bus Free Time between a STOP and START Condition	t _{BUF}		0.5			μs
Low Period of the SCL Clock	t _{LOW}		0.5			μs
High Period of the SCL Clock	t _{HIGH}		0.26			μs
Data Setup Time	t _{SD}		50			ns
Data Hold Time	t _{HD}		0			ns
Hold Time for Repeated Start Condition	t _{H,STA}				260	ns
Setup Time for Repeated Start Condition	t _{S,STA}				260	ns
Setup Time for Stop Condition	t _{S,STO}				260	ns

- Note 2:** When entering into SLEEP mode from either RELEASE or BRAKE mode, a minimum BRAKE time must be respected (t_{BRK_MIN}) to ensure the coil is fully demagnetized.
If a Go to SLEEP request is issued while the device is in RELEASE mode, the MAX22215 automatically inserts a t_{BRK_MIN} long BRAKE phase before entering in SLEEP mode.
If a Go to SLEEP request is issued while the device has been in BRAKE mode for less than $TBRK_MIN$, the MAX22215 automatically extends the BRAKE phase and enters in SLEEP mode when t_{BRK_MIN} is reached (see [Figure 2](#)).
If a Go to SLEEP request is issued while the device has been in BRAKE mode for longer than $TBRK_MIN$, the MAX22215 immediately enters in SLEEP mode.
- Note 3:** Maximum current the regulator can deliver to an external load.
- Note 4:** Entering in DIAGNOSTIC mode (DIAG) is not allowed directly from RELEASE mode. DIAGNOSTIC mode can be entered either from SLEEP mode or from BRAKE mode.
When entering from BRAKE mode, a minimum BRAKE time must be respected (t_{BRK_MIN}) to ensure the coil is fully demagnetized. If the DIAGNOSTIC command is sent before the t_{BRK_MIN} is ended, the MAX22215 enforces BRAKE conditions to extend the total BRAKE time before entering in DIAGNOSTIC mode, as shown in [Figure 5](#).
- Note 5:** SCL and SDA edges faster than 120ns and line capacitance for SCL and SDA within 100pF.

Pin Configuration

MAX22215



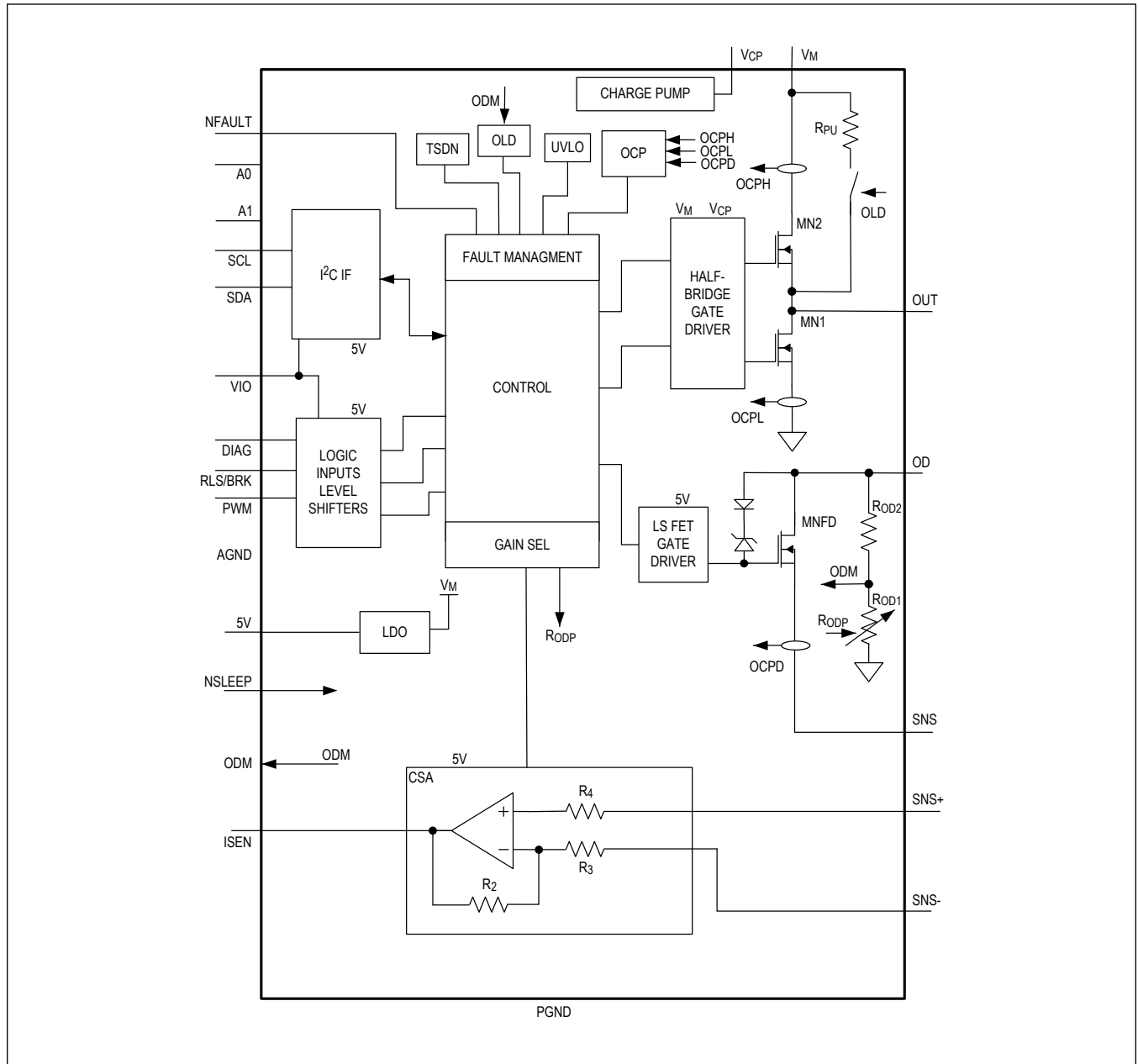
Pin Description

PIN	NAME	FUNCTION
38, 1, 2, 3	V _M	Supply Voltage Input. Bypass with at least a 1μF SMD and 100μF electrolytic capacitor.
33, 34, 35, 36, 37	OUT	Half-Bridge Output. Connect to the brake coil terminal.
4, 5, 6, 7	OD	Open-Drain, Brake-Release NFET Output. Connect to the brake coil terminal.
25, 26, 27, 28	SNS	Sense Resistor. Connect a sense resistor between SNS and GND.
29, 30, 31	PGND	Power GND
24	SNS+	CSA Positive Input
23	SNS-	CSA Negative Input
8	V _{CP}	Charge-Pump Output. Connect a 1μF, 6V SMD capacitor between V _{CP} and V _M .
20	ODM	OD Pin Monitor. ODM outputs the central tap of a resistive divider connected to OD.
22	AGND	Analog Ground
19	V _{IO}	Logic Power Supply Input. V _{IO} can vary from 1.8V to 5V. For 5V operation, V _{IO} can be externally tied to 5V. Connect a 6V, 100nF bypass capacitor to GND close to the V _{IO} pin.
9	V ₅	Internal 5V Regulator Output. Connect a 6V, 1μF bypass capacitor to GND close to the V ₅ pin.
17	FAULT	Fault Indicator, Open-Drain Output. Connect a 10kΩ pull-up resistor to V _{IO} .
16	SCL	I ² C Serial Clock Input. Connect a 1kΩ pull-up resistor to V _{IO} .
15	SDA	I ² C Serial Input/Output Data. Connect a 1kΩ pull-up resistor to V _{IO} .
13	A0	I ² C Device Address Programming Input

Pin Description (continued)

PIN	NAME	FUNCTION
14	A1	I ² C Device Address Programming Input
21	ISEN	Current-Sense Amplifier Output
11	RLS/BRK	Release/Brake CMOS Logic Input. Connect to GND for software control through I ² C.
10	DIAG	Diagnostic CMOS Logic Input. Connect to GND for software control through I ² C.
12	PWM	PWM CMOS Logic Input
18	$\overline{\text{SLEEP}}$	SLEEP Mode. Drive the $\overline{\text{SLEEP}}$ to logic low to enter SLEEP mode and minimize power consumption. Drive $\overline{\text{SLEEP}}$ to logic high to enter normal operation. A pull-down resistor is connected between $\overline{\text{SLEEP}}$ and GND. Connect $\overline{\text{SLEEP}}$ to 5V in order to automatically power up the device when V _{IO} is applied. When the MAX22215 is configured in Software Control mode, the $\overline{\text{SLEEP}}$ logic input pin remains active and connected in OR-ing configuration with the internal $\overline{\text{SLEEP}}$ bit.
32	N.C.	Not Internally Connected. Connect this pin to the exposed pad and ground plane for better heat dissipation.

Functional Diagrams



Detailed Description

The MAX22215 integrates one 36V half-bridge, one 65V low-side NFET (brake-release NFET) and one unidirectional low-offset, current-sense amplifier (CSA). It is primarily intended to drive electromechanical motor brakes and solenoids—one terminal being connected to the half-bridge output and the other terminal connected to the drain of the brake-release NFET. See the [Functional Diagram](#).

The coil current can be controlled both during the energization and de-energization phases using PWM, resulting in accurate control of excitation, hold, and demagnetization currents, as well as energizing and de-energizing timings.

To prevent cross bar conduction, an internal break-before-make circuit ensures that the high-side and low-side FETs are never turned on simultaneously.

During the energization phase, the brake-release FET is on, while the half bridge is PWM'd to get the desired magnetizing current. During the de-energization phase, the half bridge drives the OUT node low, while the brake-release NFET is turned off. The coil gets quickly demagnetized through an internal 55V fast demag clamp.

The internal demagnetization clamp is triggered by a 55V Zener diode connected between the gate and drain of the brake-release NFET. The clamp features a safe demagnetization function, which ensures safe operations by preventing the junction temperature to exceed safety levels. As soon as the junction temperature exceeds a threshold, a thermal controlled loop is activated, and the low-side NFET is pulse-width-modulated to keep the junction temperature below a safety level (SafeDemag function).

The half-bridge FETs and the brake-release NFET feature extremely low $R_{DS(on)}$ (50m Ω , typ). The high efficiency and low power dissipation make the device suitable for space-constrained applications in which high-power density on the PCB is a concern. The MAX22215 can drive up to 3A and is limited by the overcurrent protection circuit. The maximum current that can be effectively delivered is application-dependent and depends on settings such as ambient temperature, heatsinking, PCB layout, air ventilation, chopping frequency, and slew rate.

The embedded, high-accuracy CSA senses the voltage drop across an external sense resistor both during brake-engage (energizing phase) and brake-release (de-energizing) operations. The CSA analog output signal can be used for diagnostic purposes or as feedback signal for an external control loop.

The device operation can be controlled either through a 1MHz I²C serial interface or by using CMOS logic input pins. When I²C is used, several device parameters such as the driver output slew rate and the CSA gain can be configured. Moreover, the user has access to fault log registers for diagnostic purposes. Up to 16 devices can share the same I²C bus.

The MAX22215 integrates nondissipative overcurrent protections (OCP), undervoltage lockout (UVLO), thermal warning and shutdown, and a brake voltage monitor analog output (ODM). Other diagnostic functions have been integrated to detect improper load connections and device malfunctioning. A fault indicator (nFAULT) pin is activated every time a fault occurs.

The MAX22215 is available in a 5mm x 7mm, 38-pin TQFN.

Hardware/Software Control

The MAX22215 supports four operating modes: SLEEP, DIAGNOSTIC, RELEASE, and BRAKE.

- SLEEP mode corresponds to the lowest power consumption mode.
- DIAGNOSTIC mode is used to determine whether the load is properly connected.
- BRAKE and RELEASE modes are the main operating modes and correspond to engage and disengage motor brake conditions, respectively.

The operating mode can be selected either through hardware (logic input pins) or software (I²C interface registers) depending on the status of the SW/HW bit in the I²C Configuration register.

At power-up, the device is controlled through hardware by default. The SW/HW bit status is set logic low (default condition), and the device operating mode depends on the status of the three logic inputs pins: NSLEEP, DIAG, and RLS/BRK.

To enable software control, an I²C command must be sent after power-up to write the SW/HW bit logic high. In Software (SW) Control mode (SW/HW = "1"), the device operating mode depends on the status of three bits in the Configuration

register (NSLEEP, DIAG, and RLS/BRK) while the NSLEEP bit is in OR-ing configuration with the NSLEEP logic input pin. In SW Control mode, the logic input pins DIAG and RLS/BRK are ignored.

SLEEP Mode

SLEEP mode is the lowest power mode for the device. SLEEP mode can be entered either by driving the NSLEEP pin logic low (HW control) or by setting the NSLEEP bit in the configuration register (SW control) (see the [Hardware/Software Control](#) section). In SW control configuration (namely SW/HW = "1"), the NSLEEP logic input pin remains active and connected in OR-ing configuration with the internal NSLEEP bit. This allows the user to enforce an emergency hardware SLEEP mode without having to rely upon software.

When in SLEEP mode, current consumption is minimized. The internal charge pump, current-sense amplifier, protection circuits, and most of the internal references are shut down. The 5V regulator is not shut down and keeps operating in SLEEP mode. This allows using the 5V to supply an external controller. I²C logic is also enabled, and I²C communication with the external controller is still possible during SLEEP mode.

When HW Control mode is used (default SW/HW = "0"), the NSLEEP pin can also be used to reset the Fault register and resume normal operations after a fault. As shown in [Figure 1](#):

- An NSLEEP negative pulse shorter than 8μs ($t_{\text{DEGLITCH_MIN}}$ minimum) is ignored to reject short spurious signals.
- If the NSLEEP is driven low for longer than 20μs, then the FAULT registers are cleared.
- If the NSLEEP is driven low for longer than 40μs, then the FAULT registers are cleared and the device enters in SLEEP mode.

When entering into SLEEP mode, a minimum BRAKE time must be respected ($t_{\text{BRK_MIN}}$) to ensure that the coil is fully demagnetized.

- If a Go to SLEEP request is issued while the device is in RELEASE mode, the MAX22215 automatically inserts a $t_{\text{BRK_MIN}}$ BRAKE time before entering in SLEEP mode.
- If a Go to SLEEP request is issued while the device has been in BRAKE mode for less than $t_{\text{BRK_MIN}}$, the MAX22215 automatically extends the BRAKE phase and enters in SLEEP mode when $t_{\text{BRK_MIN}}$ is reached (see [Figure 2](#))
- If a Go to SLEEP request is issued while the device has been in BRAKE mode for longer than $t_{\text{BRK_MIN}}$, the MAX22215 immediately enters in SLEEP mode.

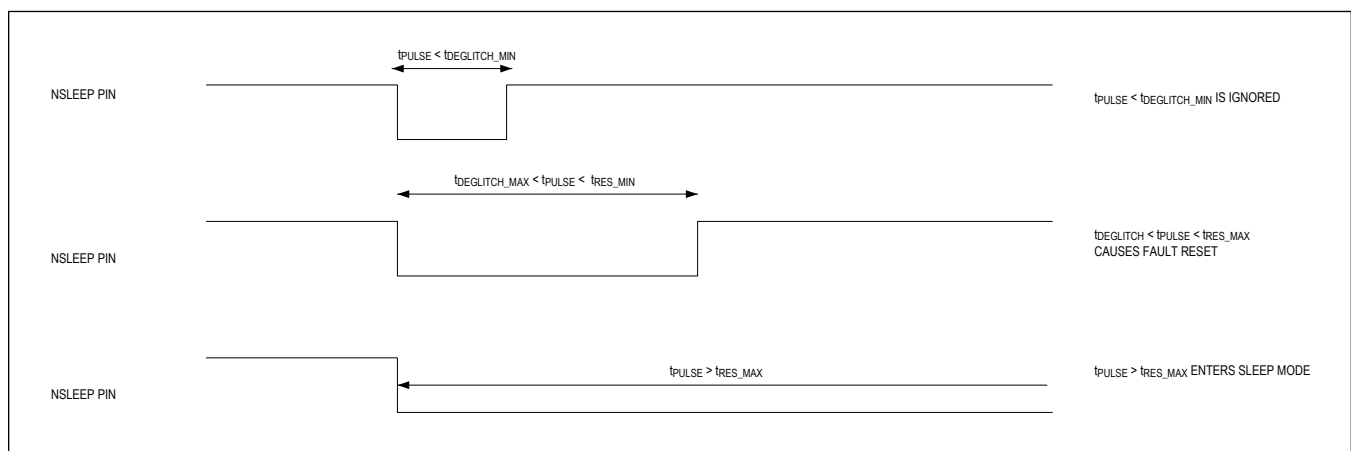


Figure 1. SLEEP Timings

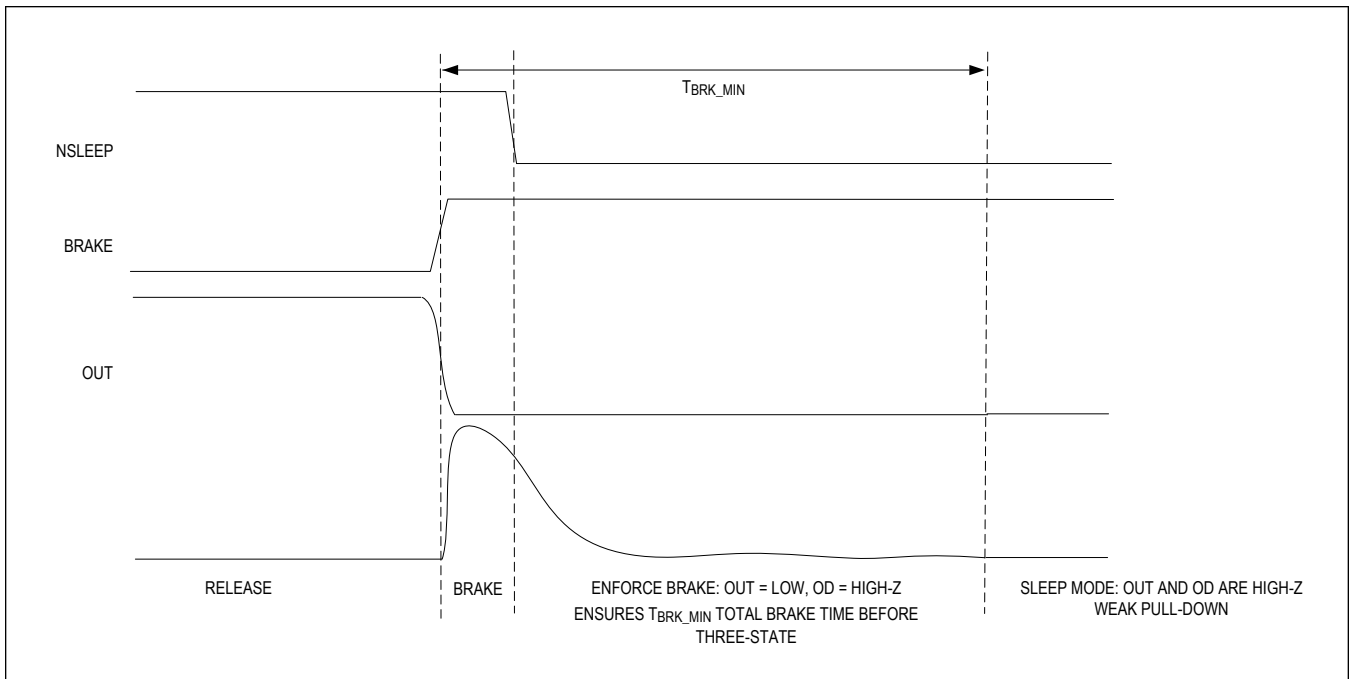


Figure 2. Minimum BRAKE Time before SLEEP

To exit from SLEEP mode and enter in any other operation mode takes 1ms maximum.

A pull-down resistor on the NSLEEP pin ensures that the pin is driven logic low if not actively driven.

MAX22215 Control - Truth Table

Table 1 shows the truth table for the MAX22215. As explained in the [Hardware/Software Control](#) section, NSLEEP, DIAG, and RLS/BRK correspond either to logic input pins in case of HW control or to the configuration register bits in case of SW control.

When NSLEEP is low, the part enters a low-power mode, and both OUT and OD are set to high impedance. When NSLEEP is set high, the device operates in three main operating modes: RELEASE, BRAKE, and DIAGNOSTIC. See the [SLEEP Mode](#) section for further details.

In RELEASE mode, the coil is energized so that the motor brake is disengaged. By applying a PWM signal to the logic input pin PWM, the user can control the actual voltage applied to the coil and hence the excitation and hold current. A break-before-make circuit ensures the high-side and low-side FET of the half bridge are never turned on simultaneously.

In BRAKE mode, the coil is demagnetized so that the motor brake is engaged. When entering BRAKE mode from RELEASE mode, the demagnetization current can be controlled by applying a PWM signal to the logic input pin PWM. This technique can be useful to control the demagnetization timings or to optimize heat dissipation.

Finally, DIAGNOSTIC mode (DIAG) is used to check whether the load is properly connected. It is recommended to enter into DIAGNOSTIC mode before starting to energize the coil. DIAGNOSTIC mode (DIAG) can be entered if the device is in SLEEP mode or has been in BRAKE mode for longer than t_{BRK_MIN} (see the [Electrical Characteristics](#) table).

Table 1. Truth Table

NSLEEP	DIAG	RLS/BRK	PWM	OD	OUT	MODE/STATUS	DESCRIPTION
0	X	X	X	High-Z	High-Z	SLEEP	SLEEP Mode. Lowest power consumption mode.
1	1	0	0	Pull Dw	Pull Up	DIAG	DIAGNOSTIC Mode. Out is pulled UP and OD is pulled down to check load connection.

Table 1. Truth Table (continued)

1	1	X	1	Pull Dw	Pull Up	(Note 1)	Fault LFD3 is triggered (Note 1)
1	1	1	X	Pull Dw	Pull Up	(Note 1)	Fault LFD3 is triggered (Note 1)
1	0	0	0	High-Z	LOW	BRAKE	BRAKE - Fast Demagnetization
1	0	0	1	LOW	LOW	SD_BRAKE	BRAKE - Slow Demagnetization
1	0	1	0	LOW	HIGH	RELEASE	RELEASE - Coil Energization (Magnetization)
1	0	1	1	LOW	LOW	SD_RELEASE	RELEASE - Slow Demagnetization

Note 1: This input configuration can be used to check whether the DIAGNOSTIC mode works and the part is properly connected. It is not intended to be used in normal operation. This input configuration triggers the fault indicator LFD3. See the [FAULT Management Summary](#) section for more details. To enter DIAGNOSTIC mode properly, both RLS/BRK and PWM must be logic low.

Coil Demagnetization and SafeDemag Function

The MAX22215 features robust, internal fast demagnetization circuitry that eliminates the need for bulky and expensive external TVSs in most applications. The internal demagnetization clamp and control circuit is built around the brake-release NFET. When the brake needs to be engaged, the half bridge drives the pin OUT to GND while the brake-release NFET is turned off, causing the voltage on the OD pin to rise up until the internal clamp is triggered (55V, typ). When the internal clamp is triggered, the demagnetization current flows thru the brake-release FET, which operates in saturation mode. The high, instantaneous power dissipation ($V_{CLAMP} \times I_{COIL}$) could heat the silicon up to critical temperatures.

To solve this issue, the MAX22215 features the demagnetization method called "SafeDemag." A temperature sensor is locally integrated inside the power FET. The local FET temperature can be substantially high compared with the average die temperature. When the demagnetization phase initiates, the brake-release FET is turned off to initiate the fast demagnetization of the coil. If the local temperature reaches a critical temperature ($T_{HIGH} \sim 160^{\circ}\text{C}$), then the power FET is turned on (Slow Demagnetization mode) to cool the power FET down to $T_{LOW} \sim 140^{\circ}\text{C}$. At this point, the FET is turned off again and the cycle repeats until the coil is fully demagnetized.

Because the SafeDemag function alternates fast and slow decay, the total demagnetization time is longer than with 100% fast demagnetization. The extension of the total demagnetization time due to the SafeDemag function depends on several parameters including ambient temperature, holding current, coil inductance and resistance, and PCB layout.

By comparing the control PWM signal applied by the controller with the ODM from the MAX22215, the external controller can monitor whether the SafeDemag function has been triggered and get immediate feedback regarding the local temperature of the power FET. The controller can possibly take corrective actions too. For instance, the demagnetization-PWM duty cycle can be reduced to further cool down the device (see [Figure 3](#)).

In addition, the SAFEDEM bit in the FAULT register is set high every time a SafeDemag event occurs. By default, this event is masked and does not activate the nFAULT indicator output. To unmask the SafeDemag function and activate the nFAULT indicator pin, the user can set low the SAFEDEM_MASK bit into the FAULT MASK register (see the [Fault MASK Register \(FAULT MASK\)](#) paragraph for more information).

Thanks to the SafeDemag method, the MAX22215 is self-protected and demagnetizes the coil at the fastest sustainable rate given the power dissipation constraint. In the unlikely case where the internal clamp featuring the SafeDemag function did not meet the timing requirements of the application, an external TVS with a high power rating and a clamp voltage less than 45V could be used to absorb the demagnetization energy instead of the internal clamp.

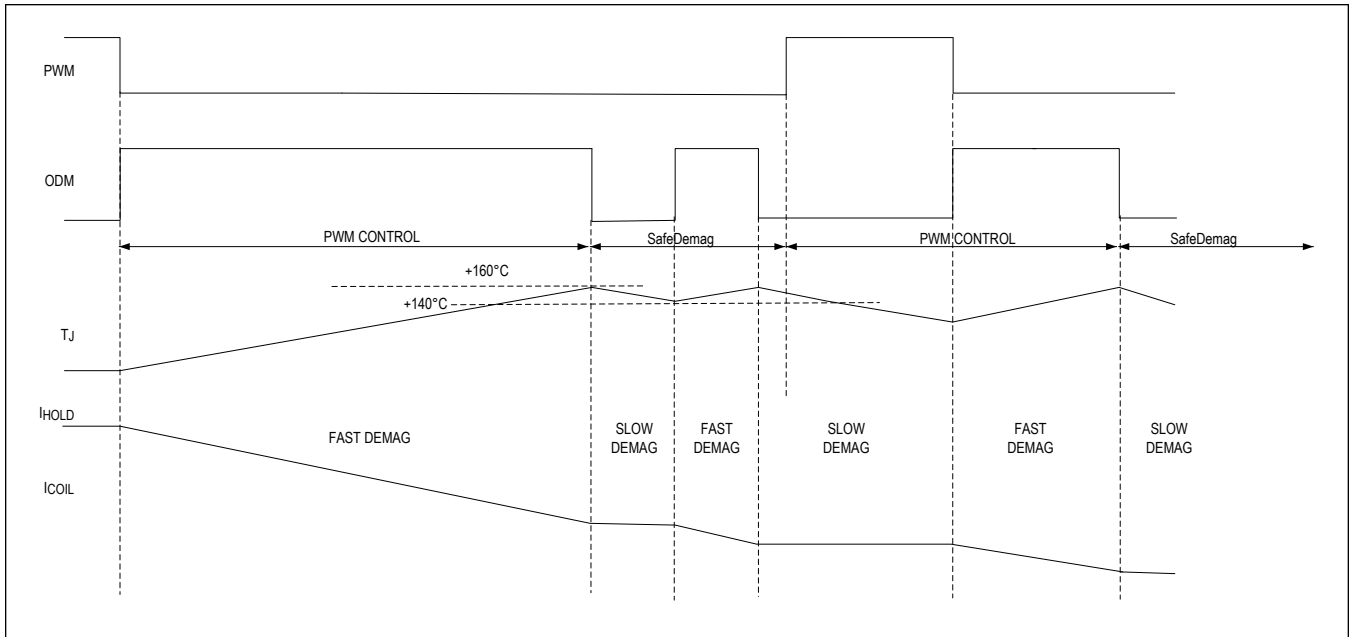


Figure 3. Safe Demagnetization Example

Enforce Demag Mode

The MAX22215 monitors the V_M supply and enforces BRAKE mode and hence the coil demagnetization as soon as the supply drops below an I²C-programmable threshold. This feature enables the use case in which the electromechanical brake is engaged by simply disconnecting the main supply.

When Enforce Brake is triggered, the nFAULT pin is asserted provided that the corresponding mask bit is zeroed (default). The Enforce Brake nFAULT signaling is not latched and disappears as soon as the Enforce Demag time elapses (about 40ms).

Three bits in the CONFIG2 register allow configuring the threshold among eight levels, as shown in [Table 2](#):

Table 2. Enforce Demag Threshold Decode

DEMAG[2:0]	ENFORCE DEMAG THRESHOLD (V_{DEM})
000	No threshold (function disabled)
001	8V
010	10V
011	12V (default)
100	14V
101	16V
110	18V
111	20V

If the supply line is disconnected while the coil is energized, the device supply (V_M) is quickly discharged by the coil current until the Enforce Demag threshold is reached. Below this threshold, the MAX22215 enforces demagnetization and the current consumption from V_M becomes less than $I_Q = 3mA$ (see Quiescent Current Consumption in the [Electrical Characteristics](#) table). Assuming no any other loads are connected to the V_M supply, the device keeps operating and current and voltages are properly monitored until V_M reaches the UVLO threshold. This transitory power-off lasts for:

$$T_{POFF} = C_{TANK} \times (V_{DEM} - UVLO) / I_Q$$

where:

C_{TANK} = Tank capacitor connected to V_M

V_{DEM} = Enforce Demag threshold

UVLO = Undervoltage lockout threshold (8V, max)

I_Q = Quiescent current from V_M

By properly sizing the tank capacitor, the user can set the power off time longer than the maximum demagnetization time ($t_{POFF} > t_{DEMAG}$). This ensures that the part is fully functional and both demagnetization current and voltage are kept monitored until demagnetization is completed. For instance, assuming maximum demagnetization time of 50ms and V_{DEM} set at 16V, then the V_M decoupling capacitor must be greater than $50ms \times 3mA / (16V - 8V) \sim 20\mu F$

Alternatively, the user can consider having a large bypass capacitor connected to the 5V pin instead of to the V_M pin. Since the current-sense amplifier and the ODM circuitry operates from a 5V line, the device continues to monitor the current and OD voltage until the 5V pin drops below the UVLO5V.

Slew-Rate Control

Two bits in the Configuration register allow the user to set the desired slew rate of the half-bridge driver output. Slower edges results in lower electromagnetic emissions, but higher power consumption. A rough estimation of the switching losses due to slew limiting can be calculated using the following formula:

$$P_{SLEW} = V_M^2 \times I_{LOAD} \times (f_{CHOP}/SR)$$

where:

SR = Slew rate

f_{CHOP} = Chopping PWM frequency

I_{LOAD} = Coil current

V_M = Supply voltage

For example, with $I_{LOAD} = 1A$, $V_M = 24V$, $f_{CHOP} = 20kHz$, and slew rate is limited at $SR = 50V/\mu s$, the formula above results in $\sim 230mW$ additional power losses. See the [Configuration Registers CONFIG](#) section for supported slew rate settings.

5V Regulator

The MAX22215 integrates a low-power 5V regulator, which is mostly aimed to supply the internal driver circuitry and the CSA. A minimum bypass capacitor of at least $1\mu F$ must be connected between 5V and ground to ensure regulator stability. The 5V regulator can possibly be used to supply external loads such as an external controller and can deliver up to 10mA maximum. The 5V regulator and the I^2C logic remain active during SLEEP mode.

Current-Sense Amplifier and GAIN Pin Description

The MAX22215 integrates a high-accuracy CSA. The CSA voltage gain can be programmed by mean of two bits in the Configuration register (see the [Configuration Registers \(CONFIG\)](#) section. The CSA features a low offset, resulting in good accuracy. The input voltage range of the CSA depends on the GAIN settings (see the [Electrical Characteristic](#) table). The sense resistor choice is a tradeoff between accuracy and efficiency. The highest accuracy is achieved by selecting an external sense resistor so that the maximum drop is close to the upper limit of the input voltage range. On the other hand, the power dissipated into the external resistor is proportional to its resistance.

MAX22215 Simplified Flow Chart

[Figure 4](#) shows a simplified flow chart of the MAX22215. Only the main statuses of the device and their links are shown.

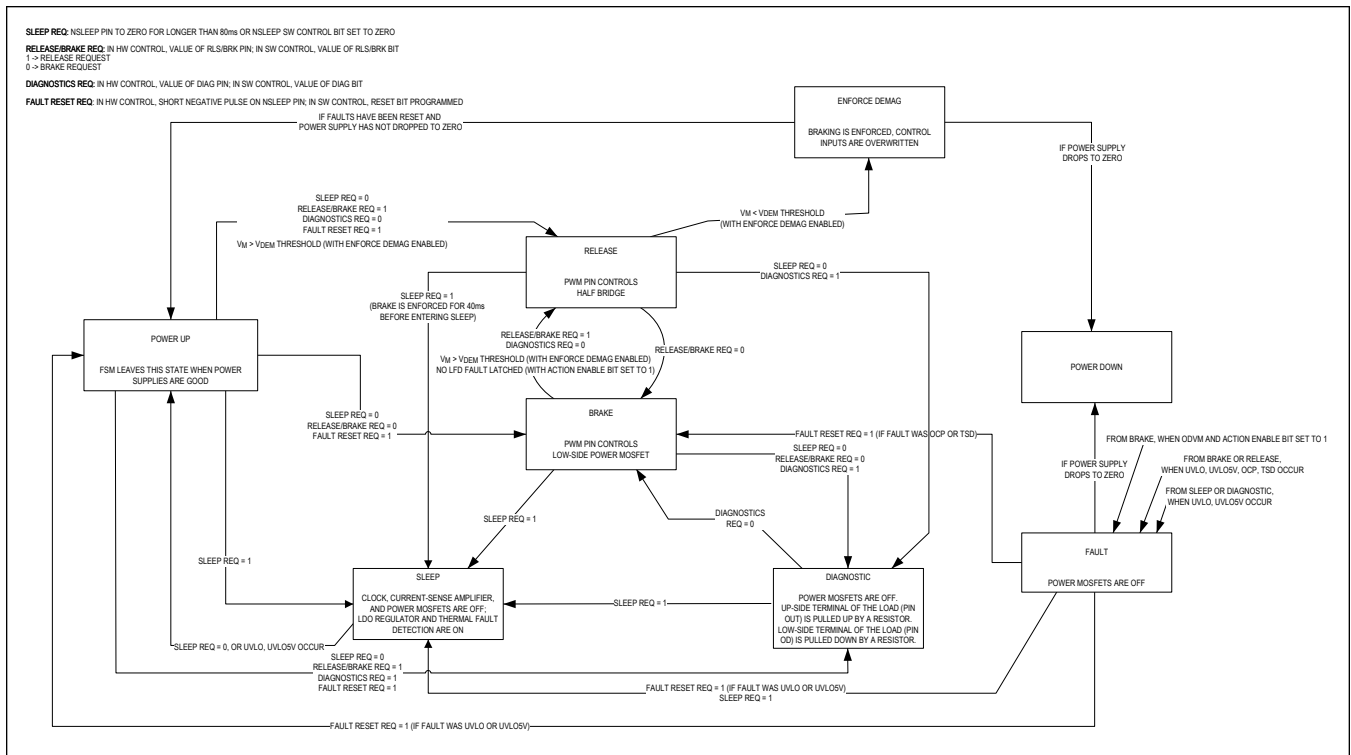


Figure 4. MAX22215 Process Flow Chart

Protections and Diagnostics

FAULT Management Summary

The MAX22215 integrates protection circuits and diagnostic functions to ensure safe operation of the motor brake under fault conditions.

Table 3 summarizes the list of diagnostic and fault management functions integrated into the MAX22215. The FAULT column shows the Fault name. For any specific fault, Table 3 reports the actions taken by the MAX22215 after detected to ensure safe operation of the MAX22215 and of the motor brake. The fault can be latched or not latched (see the TYPE column in Table 3). To resume normal operation when a latched fault is detected, the user must clear the Fault register (see the Restore Normal Operation after a Fault section). The MASK bit in the FAULT MASK register determines whether the NFAULT indicator pin is asserted once the fault is detected. Table 3 shows the default value for the MASK bit. The ENA bits in the ACTION ENABLE register determines whether the MAX22215 takes actions in response to a fault condition. Table 3 shows the default value for the ENA bit for each individual fault. The FAULT MASK register and the ACTION ENABLE register can be programmed through the I²C interface.

Table 3. Fault Summary

FAULT	DESCRIPTION	DETECTION	ACTION	TYPE	MASK BIT DEFAULT	ENA BIT DEFAULT
OCP0	Half Bridge - High-Side FET Overcurrent Protection	Half-bridge - high-side FET current greater than OCP threshold	Both OUT and OD are three-stated; NFAULT asserted if not masked	Latched	Not masked	N/A

Table 3. Fault Summary (continued)

OCP1	Half Bridge - Low-Side FET Overcurrent Protection	Half-bridge - low-side FET current greater than OCP threshold	Both OUT and OD are three-stated; NFAULT asserted if not masked	Latched	Not masked	N/A
OCP2	Release NFET Overcurrent Protection	Release NFET current greater than OCP threshold	Both OUT and OD are three-stated; NFAULT asserted if not masked	Latched	Not masked	N/A
TWARN_UL	Unlatched Thermal Warning	Average die temperature exceeds T_{WARN} threshold ($\sim+120^{\circ}\text{C}$)	NFAULT asserted if not masked	Not latched	Not masked	N/A
TWARN	Latched Thermal Warning	Average die temperature exceeds T_{WARN} threshold ($\sim+120^{\circ}\text{C}$)	—	Latched	Not masked	—
TSD	Thermal Shutdown	Average die temperature exceeds T_{SD} threshold ($\sim+150^{\circ}\text{C}$)	Both OUT and OD are three-stated; NFAULT asserted if not masked	Latched	Not masked	N/A
UVLO	V_M Undervoltage Lockout	V_M below UVLO threshold	Both OUT and OD are three-stated; NFAULT asserted if not masked	Latched	Not masked	N/A
UVLO5V	5V Undervoltage Lockout	5V below UVLO5V threshold	Both OUT and OD are three-stated; NFAULT asserted if not masked	Latched	Not masked	N/A
UVLOCP	CP Undervoltage Lockout	CP below UVLOCP threshold (disabled in SLEEP mode or during power-up)	Both OUT and OD are three-stated; NFAULT asserted if not masked	Latched	Not masked	N/A
DVD	Demag Voltage Detection	Demag voltage less than V_{DVD_TH} during braking	NFAULT asserted if not masked	Latched	Masked	N/A
LFD1	Coil Shorted to V_M	Detected during DIAGNOSTIC mode if $OD > 2/3 \times V_M$	Inhibit RELEASE mode if ENA1 = 1; NFAULT asserted if not masked	Latched	Not masked	ENA1 = 1
LFD2	Coil Shorted to GND or Not Connected	Detected during DIAGNOSTIC mode if $OD < 1/3 \times V_M$	Inhibit RELEASE mode if ENA2 = 1; NFAULT asserted if not masked	Latched	Not masked	ENA2 = 1
LFD3	Either PWM or BRK/RLS Shorted to a Positive Rail	Detects whether either PWM or BRK/RLS are logic high during DIAGNOSTIC mode	NFAULT asserted if not masked	Unlatched	Not masked	—
SAFEDEM	Safe Demag Has Been Triggered	Release NFET junction temperature greater than $+170^{\circ}\text{C}$	NFAULT asserted if not masked	Latched	Masked	N/A
ISM	Lack of Magnetization Current during Release	ISEN voltage $< 40\text{mV}$ during RELEASE mode (200ms filter)	NFAULT asserted if not masked	Latched	Masked	N/A

Table 3. Fault Summary (continued)

ODVM	OD Shorted to V_M	OD pin voltage $>2/3 \times V_M$ in BRAKE mode (400ms filter)	Both OUT and OD are three-stated if ENA3 = 1; NFAULT asserted if not masked	Latched	Not masked	ENA3 = 1
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A detailed description for each fault condition is shown in the following paragraphs.

Restore Normal Operation after a Fault

Once a fault has been detected, normal operation can be restored by mean of a fault-reset procedure. The fault-reset procedure is different depending on whether the MAX22215 is SW or HW controlled (see the [Hardware/Software Control](#) section). In both cases, a fault-reset procedure causes the nFAULT fault indicator output to be released and normal operation to be restored unless the fault condition is still present.

The [Table 4](#) describes the fault-reset procedure in the two cases.

Table 4. Fault-Reset Procedure

CONTROL MODE	FAULT-RESET PROCEDURE
Hardware Control (Logic Inputs)	To apply a negative pulse to the NSLEEP pin (see the Reset Timing specification in the Electrical Characteristics table for min and max duration of the reset pulse).
Software Control (I ² C)	To set the RESET bit to logic high in the Configuration register. This also causes the Fault register to be cleared. Therefore, it is recommended reading the Fault register before the fault-reset is sent. Once the Fault register has been cleared, the RESET bit is internally zeroed.

Diagnostic Mode - Load Fault Detection (LFD)

BRAKE time (t_{BRK_MIN}) must be guaranteed to ensure the coil is fully demagnetized before entering DIAGNOSTIC mode. If the DIAGNOSTIC command is sent before t_{BRK_MIN} is ended, the MAX22215 enforces BRAKE conditions to extend the total BRAKE time before entering DIAGNOSTIC mode, as shown in [Figure 5](#).

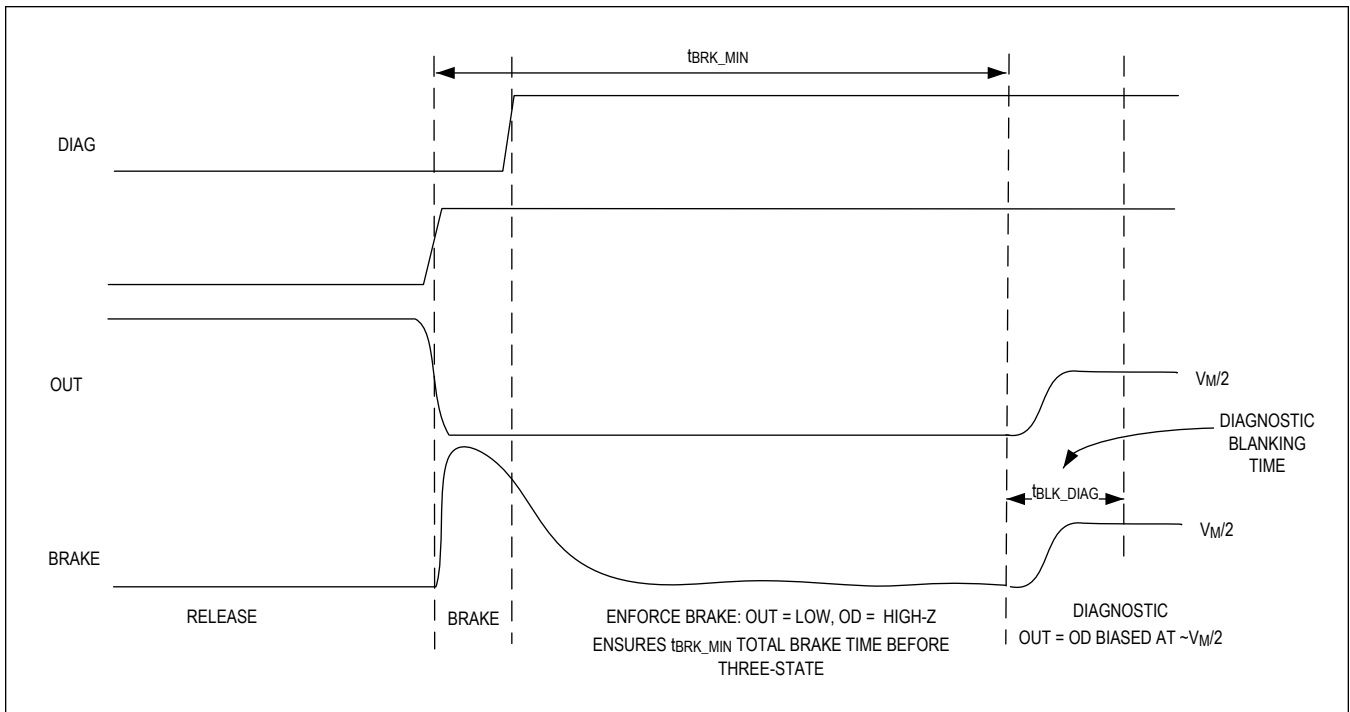


Figure 5. DIAGNOSTIC Mode Timings

When in DIAGNOSTIC mode, the OUT pin is pulled high by a pull-up resistor (R_{PU}), while a programmable resistive divider is connected between OD and GND. The output of the divider is available at the ODM pin and can be monitored by the external controller at all times. The bias network is shown in [Figure 6](#), which also shows typical resistor values for each programming step.

To allow the OUT and OD voltages to settle, the internal diagnostic is activated after a blanking time (t_{BLK_DIAG}) (see [Figure 5](#)).

The embedded diagnostic circuit monitors the voltage on the OD pin. Under normal conditions, the OD node is expected to be around $V_M/2$. If the load is unconnected or one of the terminals is shorted either to GND or V_M , the OD node falls outside the expected range and faults are signaled out if not masked. If $OD > (2/3 \times V_M)$, the LFD1 bit in the FAULT register is set to logic high. If $OD < (1/3 \times V_M)$, the LFD2 bit is set to logic high.

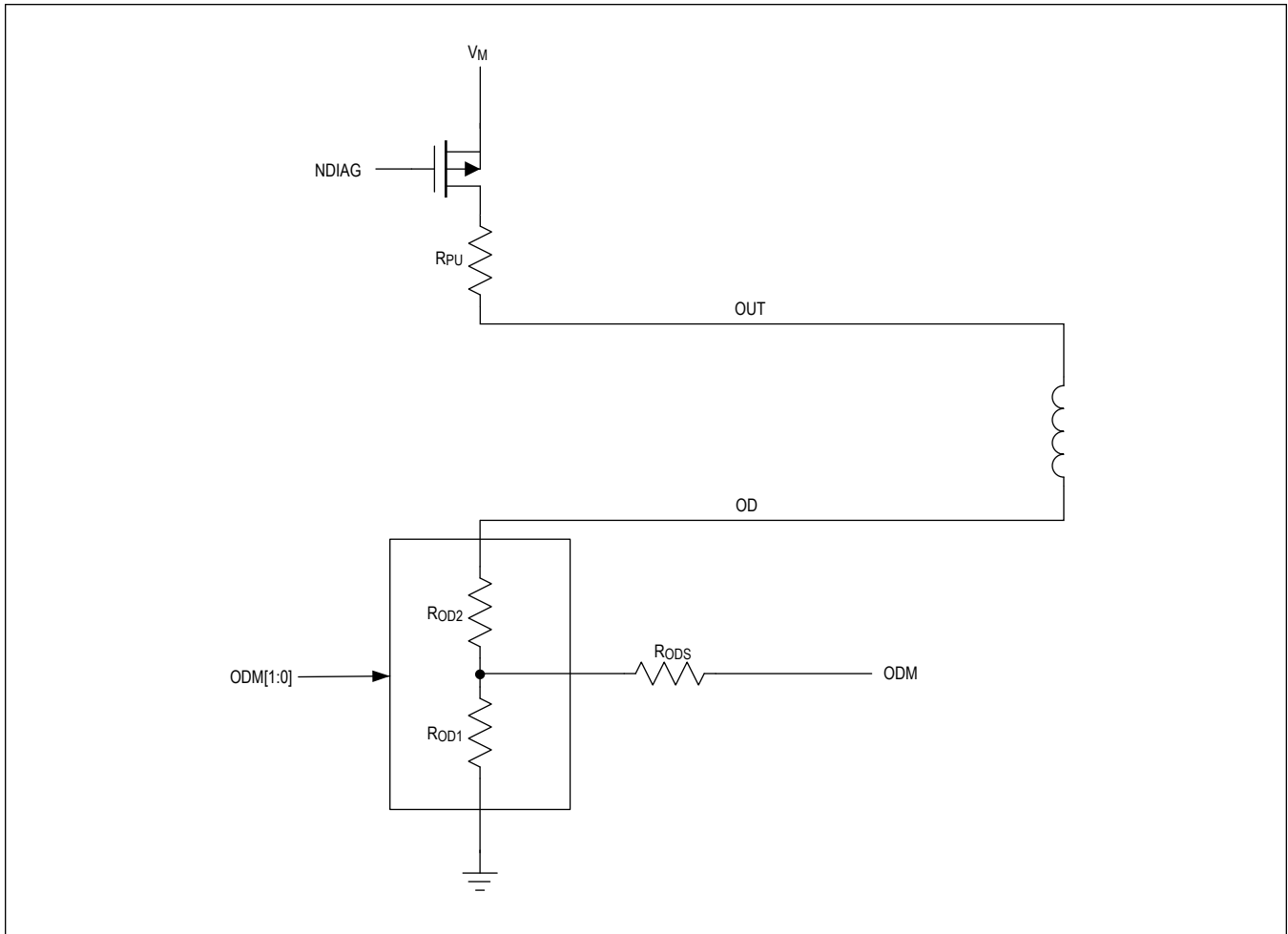


Figure 6. DIAGNOSTIC Bias Network

Table 5. ODM Resistive Network

ODM1	ODM0	R _{PU} (kΩ)	R _{OD1} (kΩ)	R _{OD2} (kΩ)	R _{ODS} (kΩ)	R _{OUT} (kΩ) OUT = OD	DIVIDER RATIO (V _{OD} /V _{ODM})
0	0	42.8	2.6	40.1	0.7	3.2	16.7
0	1	42.8	2.1	40.7	0.7	2.7	20.6
1	0	42.8	1.8	41	0.7	2.4	24.4

Two bits in the ACTION ENABLE register, ENA1 and ENA2, can be used to inhibit the RELEASE mode after LFD1 or LFD2 detection. If ENA_ is set high (default condition), the MAX22215 ignores any attempt to enter RELEASE mode if the LFD_ bit is set high. Normal operation can be restored as explained in the [Restore Normal Operation after a Fault](#) section.

As explained in the [MAX22215 Control - Truth Table](#) section, driving DIAGNOSTIC logic high when either PWM or RLS/BRK are logic high causes the MAX22215 to generate the LFD3 fault. This fault condition is signaled out on the nFAULT indicator pin. This fault is not latched and is cleared as soon as the device exits the DIAGNOSTIC mode.

The purpose of LFD3 fault indicator is twofold:

1. To safely detect whether one of the two logic inputs fails short high, which would be harmful for the application.

2. To provide an easy way to check the Fault indicator (nFAULT) functionality by intentionally causing the LFD3 to occur.

Overcurrent Protection (OCP) and Blanking Time

The MAX22215 features a nondissipative overcurrent protection (OCP) function. The current is internally sensed on each of the three power FETs and compared with an internal fixed threshold.

An internal blanking time ensures the OCP circuits are not triggered by brief overcurrent spikes occurring just after the PWM commutations.

If the current on either the high-side or low-side FET of the half bridge exceeds the OCP threshold, the half bridge and the release NFET are three-stated and the corresponding bit into the FAULT register is set high. The nFAULT pin is asserted provided that the OCP is not masked.

If the current on release NFET exceeds the OCP threshold, the half bridge and the release NFET are three-stated and the corresponding bit in the FAULT register is set high.

For restoring normal operation after an OCP fault has been detected, see the [Restore Normal Operation after a Fault](#) section.

To avoid the device from being overstressed with high-current bursts occurring at an high repetitive frequency, the MAX22215 inserts a delay (see Overcurrent Restore Timing in the [Electrical Characteristics](#) table) to any attempt of recovery from OCP events.

Overtemperature Protection (T_{WARN} and T_{SD})

The MAX22215 features a two-level thermal protection function.

When the junction temperature reaches the first lower warning threshold (T_{HW}) the nFAULT pin is asserted (if not masked), but the device keeps operating normally. If the junction temperature returns below the warning threshold, the nFAULT pin is automatically deasserted. One latched and one unlatched flag bit are available in the NFAULT register for diagnostic purposes.

If the junction temperature keeps increasing and exceeds the higher shutdown threshold (T_{SD}), the nFAULT indicator pin is latched logic low, the MAX22215 enforces BRAKE mode for 40ms and finally three-states both the half-bridge output (OUT) and the release FET output (OD). One latched flag bit is available in the NFAULT register for diagnostic purposes.

Normal operation can be restored as explained in the [Restore Normal Operation after a Fault](#) section, provided that the root cause of the fault has disappeared.

Undervoltage Protection (UVLO, UVLO5V, UVLOCP)

Three different undervoltage lockout circuits sense the V_{M} supply input, the 5V regulator output voltage and the charge-pump voltage.

If the V_{M} supply voltage drops below the undervoltage lockout threshold (UVLO), the MAX22215 enforces BRAKE mode (see the [MAX22215 Control - Truth Table](#)). The UVLO fault flag in the FAULT register is set high and the nFAULT indicator pin is asserted if not masked. In particular, after power-up, the UVLO is flagged and the user must clear the FAULT register to start operations.

If the 5V regulator output drops below the undervoltage lockout threshold (UVLO5V), both the OUT pin and the OD pin are three-stated. The UVLO5V flag in the FAULT register is set high and the nFAULT indicator pin is asserted if not masked.

If the charge-pump voltage regulator output drops below the undervoltage lockout threshold (UVLOCP), both the OUT pin and the OD pin are three-stated. The UVLOCP flag in the FAULT register is set high and the nFAULT indicator pin is asserted if not masked.

Normal operation can be restored as explained in the [Restore Normal Operation after a Fault](#) section, provided that the root cause of the fault has disappeared.

Demag Voltage Detection (DVD)

While the coil is energized, switching OFF the brake-release NFET causes the OD voltage to immediately rise up to the clamping voltage.

The DVD diagnostic function monitors the OD pin and detects whether it gets over the V_{DVD} threshold (see DVD Detection Threshold in the [Electrical Characteristics](#) table) within t_{DVD} (see DVD Detection Timing in the [Electrical Characteristics](#) table). t_{DVD} starts from the internal RLS/BRK signal falling edge. If the threshold is not reached, a fault condition is detected.

When a DVD fault is detected, the NFAULT bit in the FAULT register is set high and the nFAULT indicator pin is asserted, provided that the DVD Mask bit is set logic low.

The DVD Mask bit is set by default high at power up.

In order to avoid false fault interrupts, the DVD Mask bit must be set logic high (default) whenever the energizing current is expected to be low or the load is disconnected.

Normal operation can be restored as explained in the [Restore Normal Operation after a Fault](#) section.

Release Current Not Detected (ISM)

While in RELEASE mode, the MAX22215 monitors the CSA output (ISEN). The ISEN monitoring begins 200ms after entering into RELEASE mode. If the ISEN voltage is found less than a user-configurable threshold (ISMTH), the ISM bit in the FAULT register is flagged and the NFAULT indicator pin is asserted if not masked.

This function enables open load detection during the energizing phase. If the load is abruptly disconnected while the coil is energized, the brake cables can reach very high voltages. Electric arcs or intermittent contacts between cables and the PCB connector can expose the MAX22215 to extremely high and potentially destructive voltages.

The ISM function can also be used as a diagnostic tool to verify the current acquisition signal path (from the external sense resistor to the CSA output) and generate an interrupt in case of anomalous behavior.

The ISM mask bit is set high by default (Fault is masked).

Normal operation after an ISM Fault can be restored as explained in the [Restore Normal Operation after a Fault](#) section.

OD Shorted to V_M Detection (ODVM)

When BRAKE mode is entered from RELEASE mode and a programmable time has elapsed, the OD pin voltage is checked. If its value is found to be greater than $2/3 \times V_M$, the ODVM FAULT is detected. The nFAULT indicator pin is asserted if not masked. Moreover, if ENA3 = 1 (default), both OUT and OD pins are three-stated. This prevents the brake coil from being magnetized with reversed polarity in case the OD pin was shorted to V_M . Typical motor brakes are not sensitive to current coil polarity, so a reversed current would cause the brake to be undesirably released.

The programmable timeout can be set by writing on bits [odvm_time](#). The available time values are:

Table 6. ODVM Timeout Table

CODE	ODVM_TIME
0x0	100ms
0x1	200ms
0x2	400ms
0x3	800ms

Normal operation after an ODVM fault can be restored, as explained in the [Restore Normal Operation after a Fault](#) section.

I²C Logic Description

Programming the MAX22215

The MAX22215 provides an I²C-compatible Interface that can be used to configure device parameters, read diagnostic information, and control the operating mode.

The use of the I²C interface is optional. In case the I²C is not used, default configuration settings are assumed and the MAX22215 is controlled from the logic input pins (see the [Hardware/Software Control](#) section).

Communication is byte oriented. The device features eight 1-byte registers: two R/W Configuration registers, two RO FAULT registers, two R/W FAULTMASK registers, one R/W ACTION ENABLE register, and one STATUS register.

The I²C interface and registers are active in all operating modes. In particular, I²C communication is still possible while in SLEEP mode. However, the FAULT register is cleared while in SLEEP mode.

I²C Interface

Start and Stop Transfer

The MAX22215 contains an I²C-compatible interface for data communication with a host controller (SCL and SDA). The interface supports a clock frequency of up to 1MHz. SCL and SDA require pull-up resistors that are connected to a positive supply.

When writing to the MAX22215 using I²C, the controller sends a START condition (S) followed by the MAX22215 I²C address. After the address, the controller sends the register address of the register that is to be programmed. The controller then ends communication by issuing a STOP condition (P) to relinquish control of the bus, or a REPEATED START condition (Sr) to communicate to another I²C target.

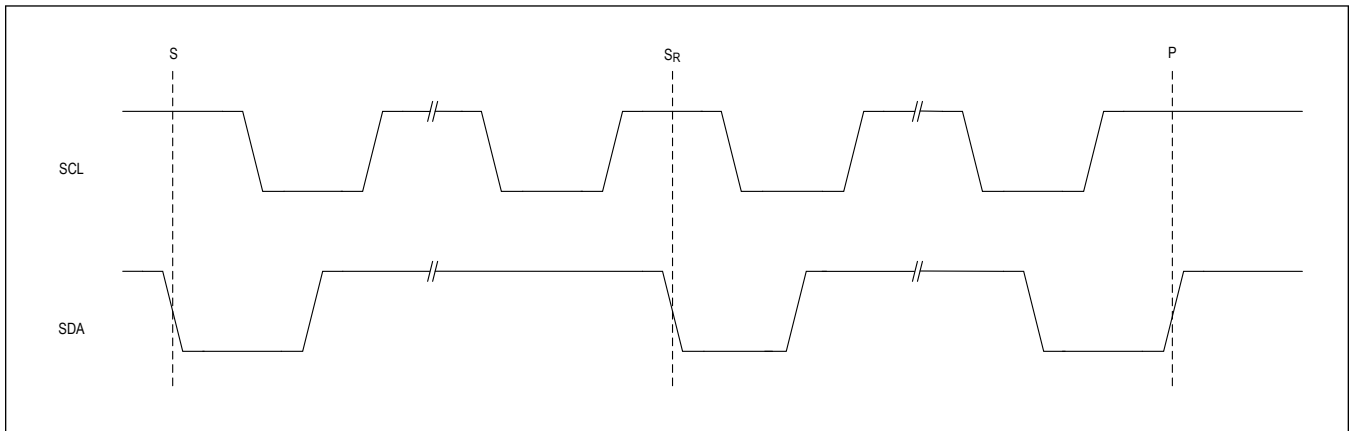


Figure 7. I²C Serial Interface START and STOP Conditions

Bit Transfer

One data bit is transferred on the rising edge of each SCL clock cycle. The data on SDA must remain stable during the high period of the SCL clock pulse. Changes in SDA while SCL is high and stable are considered control signals. Both SDA and SCL remain high when the bus is not active.

Single-Byte Write

In this operation, the controller sends an address and two data bytes to the target device.

The following procedure describes the single-byte write operation:

1. The controller sends a START condition.
2. The controller sends the 7-bit target address plus a write bit (low).
3. The addressed target asserts an ACK if the target ID is correct (NACK if not).
4. The controller sends the 8-bit register address.
5. The target asserts an ACK on the data line.
6. The controller sends 8 data bits.
7. The target asserts an ACK on the data line.
8. The controller generates a STOP condition.

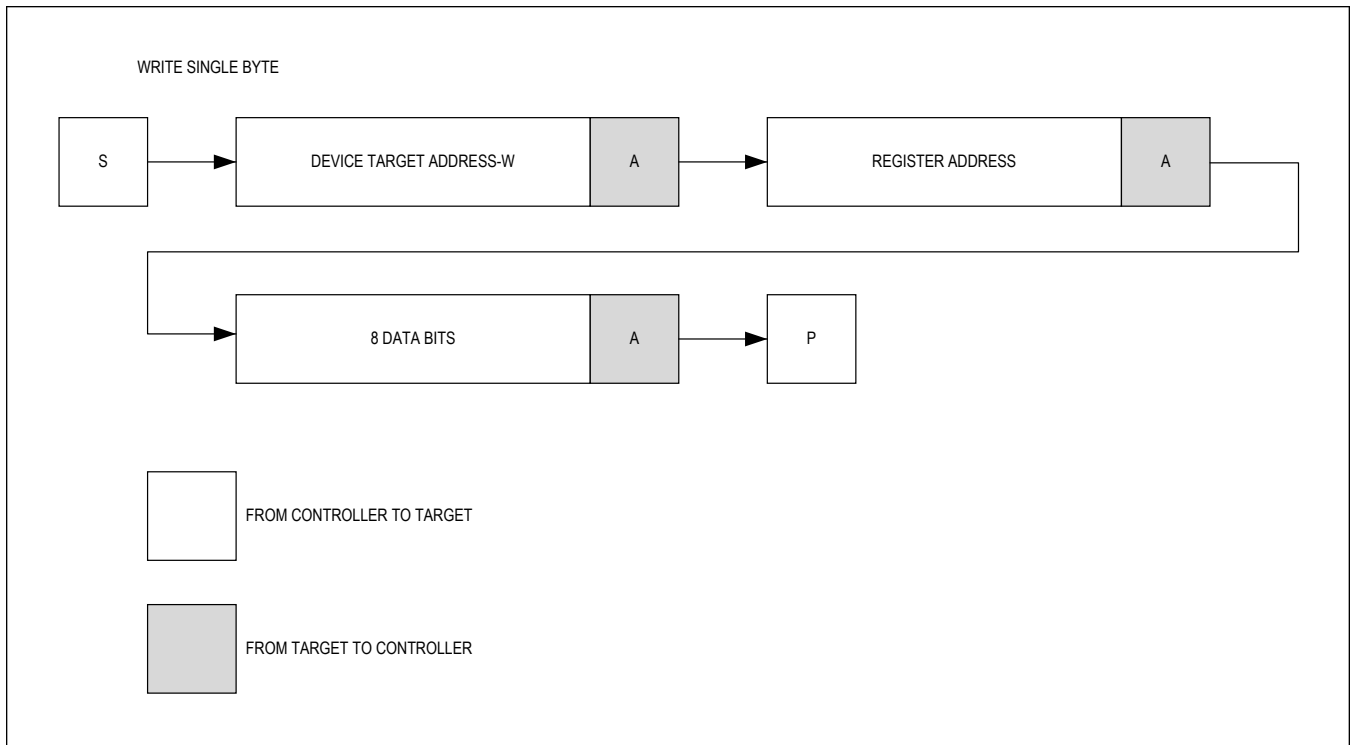


Figure 8. Single-Byte Write Sequence

Burst Write

In this operation, the controller sends an address and multiple data bytes to the target device. The target device automatically increments the register address after each data byte is sent, unless the register being accessed is 0x00, in which case the register address remains the same. The following procedure describes the burst write operation:

1. The controller sends a START condition.
2. The controller sends the 7-bit target address plus a write bit (low).
3. The addressed target asserts an ACK if the target ID is correct (NACK if not).
4. The controller sends the 8-bit register address.
5. The target asserts an ACK on the data line.
6. The controller sends 8 data bits.
7. The target asserts an ACK on the data line.
8. Repeat steps 6 and 7 N-1 times.
9. The controller generates a STOP condition.

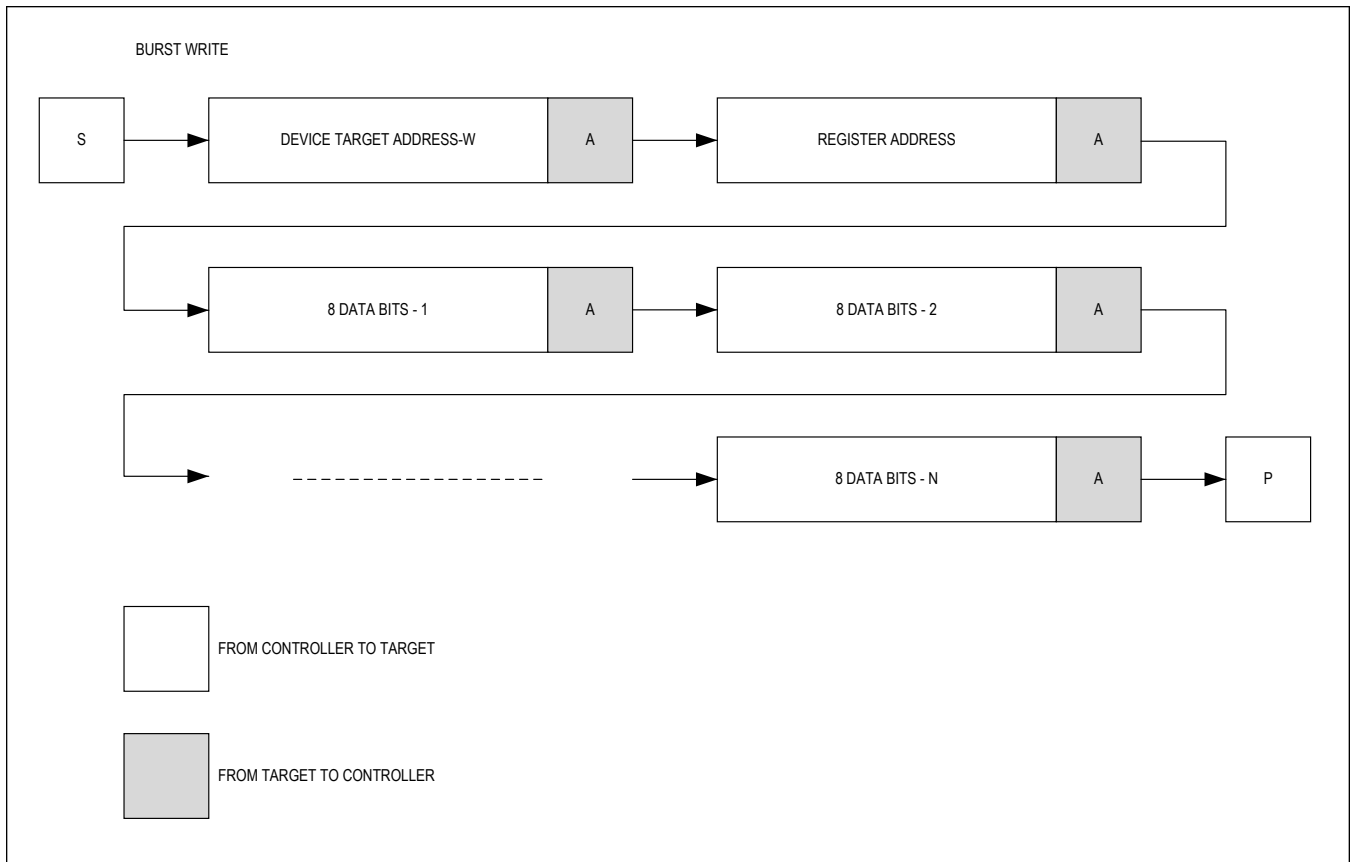


Figure 9. Burst Write Sequence

Single-Byte Read

In this operation, the controller sends an address plus two data bytes and receives one data byte from the target device. The following procedure describes the single-byte read operation:

1. The controller sends a START condition.
2. The controller sends the 7-bit target address plus a write bit (low).
3. The addressed target asserts an ACK if the target ID is correct (NACK if not).
4. The controller sends the 8-bit register address.
5. The target asserts an ACK on the data line.
6. The controller sends a REPEATED START condition.
7. The controller sends the 7-bit target address plus a read bit (high).
8. The addressed target asserts an ACK on the data line.
9. The target sends 8 data bits.
10. The controller asserts a NACK on the data line.
11. The controller generates a STOP condition.

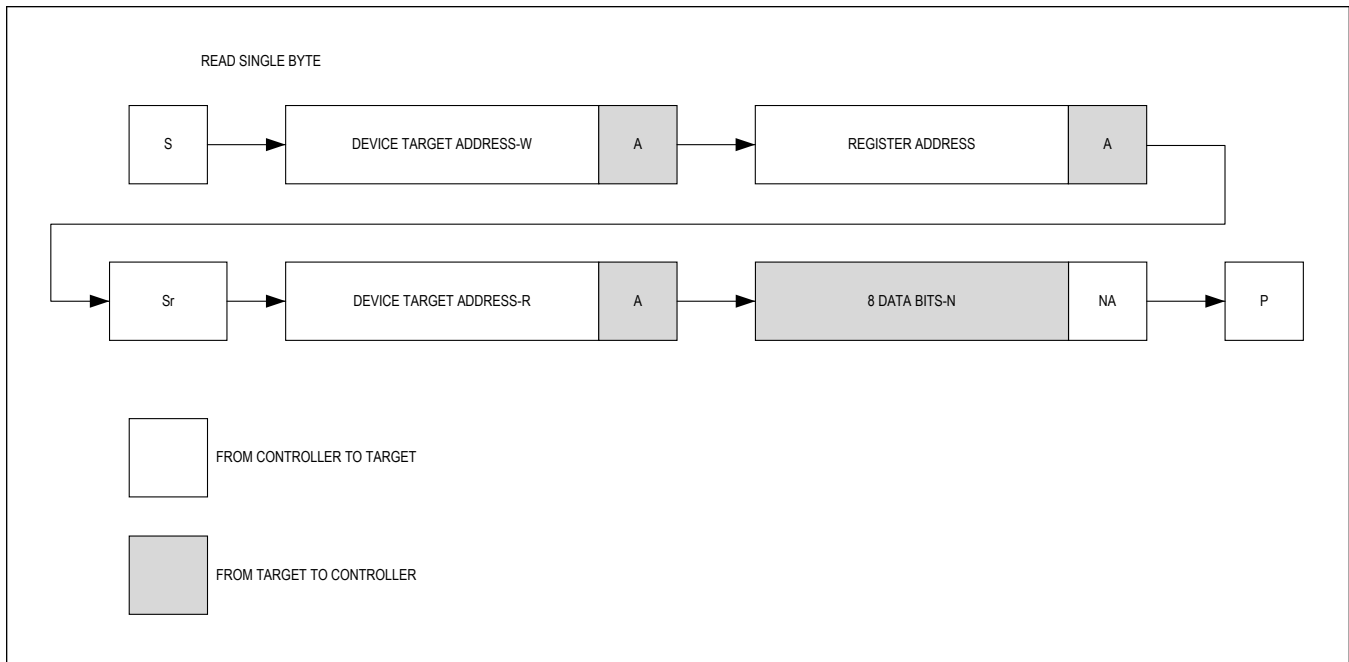


Figure 10. Single-Byte Read Sequence

Burst Read

In this operation, the controller sends an address plus two data bytes and receives multiple data bytes from the target device. The following procedure describes the burst read operation:

1. The controller sends a START condition.
2. The controller sends the 7-bit target address plus a write bit (low).
3. The addressed target asserts an ACK if the target ID is correct (NACK if not).
4. The controller sends the 8-bit register address.
5. The target asserts an ACK on the data line.
6. The controller sends a REPEATED START condition.
7. The controller sends the 7-bit target address plus a read bit (high).
8. The target asserts an ACK on the data line.
9. The target sends 8 data bits.
10. The controller asserts an ACK on the data line.
11. Repeat steps 9 and 10 N-2 times.
12. The target sends the last 8 data bits.
13. The controller asserts a NACK on the data line.
14. The controller generates a STOP condition.

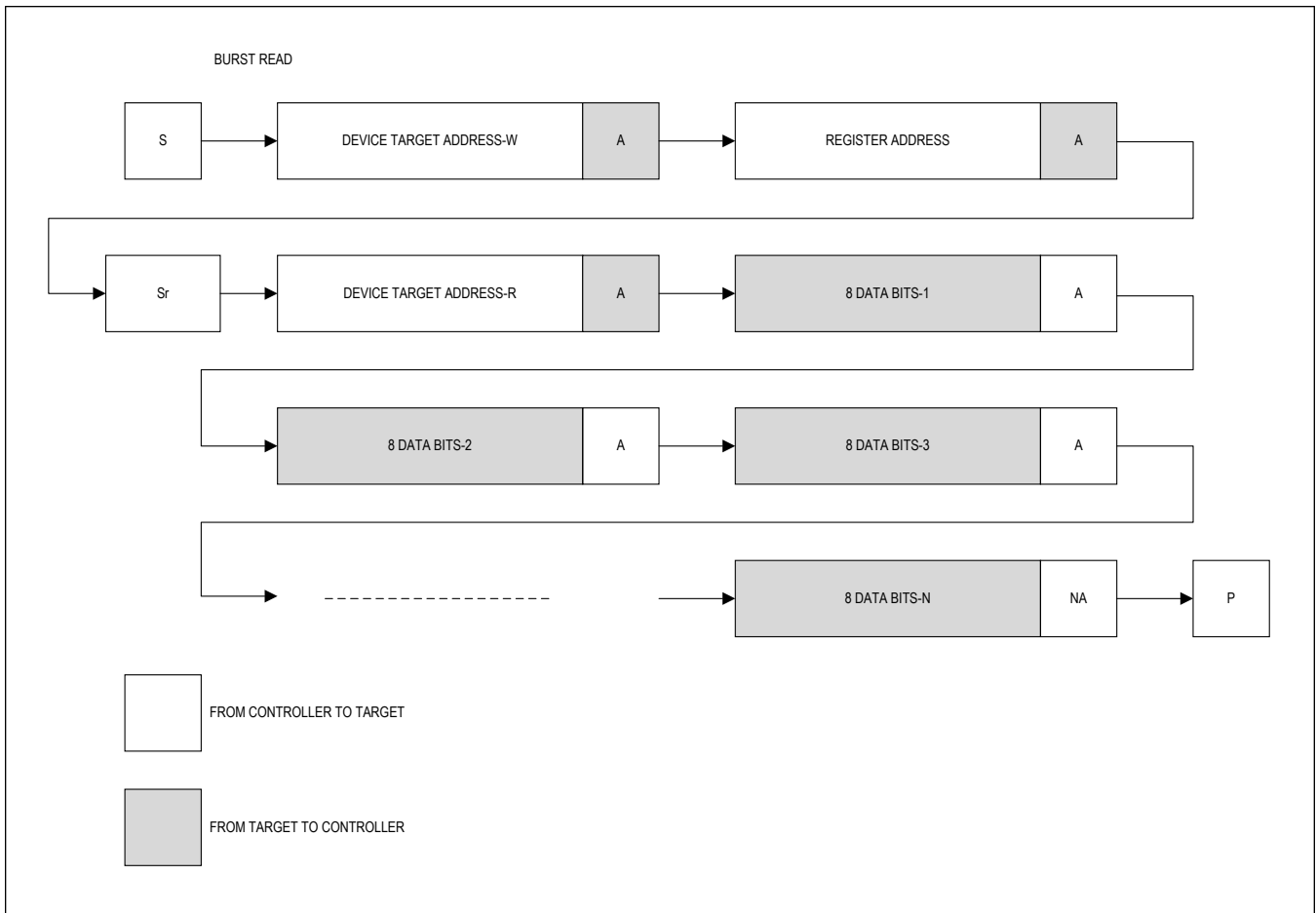


Figure 11. Burst Read Sequence

Acknowledge Bits

Data transfers are acknowledged with an acknowledge bit (ACK) or a not-acknowledge bit (NACK). Both the controller and the MAX22215 generate ACK bits. To generate an ACK, pull SDA low before the rising edge of the ninth clock pulse and hold it low during the high period of the ninth clock pulse. To generate a NACK, leave SDA high before the rising edge of the ninth clock pulse and leave it high for the duration of the ninth clock pulse. Monitoring for NACK bits allows for detection of unsuccessful data transfers.

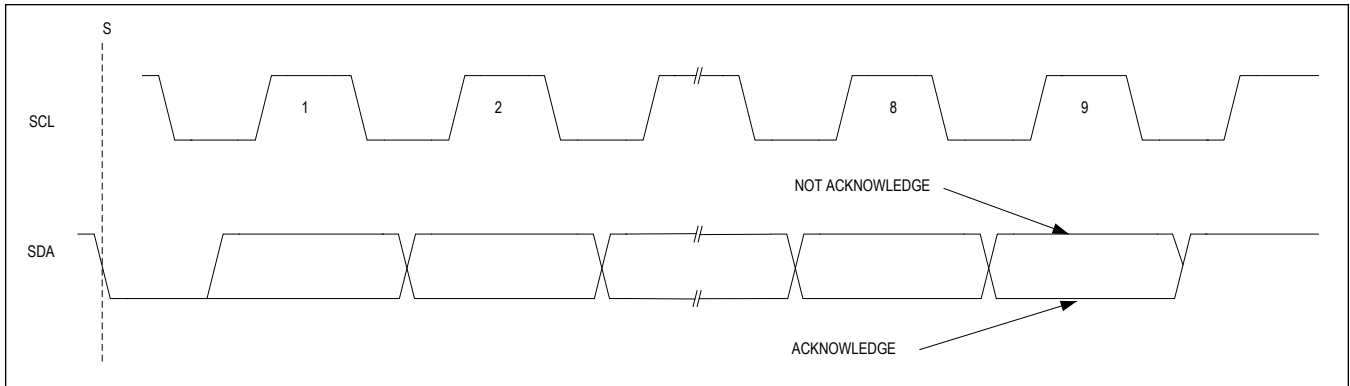


Figure 12. Acknowledge Bits

Target ID Assignment

The MAX22215 contains an I²C-compatible interface for data communication with a host processor (SCL and SDA). The interface supports a clock frequency up to 1MHz. SCL and SDA require pull-up resistors that are connected to VIO.

The I²C interface includes a 7-bit address, allowing up to 16 devices to share the same I²C bus. The address is defined by connecting A1 and A0 inputs to ground, VIO, SDA, and SCL. [Table 7](#) shows the addresses for read/write operation of internal registers for up to 16 different devices identified by the A1, A0 settings.

Notice that A1, A0 set the value of the 4 least significant bits of the target ID. The 3 most significant bits are always 001.

Table 7. I²C Address Table

A1	A0	TARGET ID
GND	GND	0x10
GND	VIO	0x11
GND	SCL	0x12
GND	SDA	0x13
VIO	GND	0x14
VIO	VIO	0x15
VIO	SCL	0x16
VIO	SDA	0x17
SCL	GND	0x18
SCL	VIO	0x19
SCL	SCL	0x1A
SCL	SDA	0x1B
SDA	GND	0x1C
SDA	VIO	0x1D
SDA	SCL	0x1E
SDA	SDA	0x1F

Status Register (STATUS) – Read Only

The STATUS register is an 8-bit, read-only register that provides the internal status of the MAX22215 to allow polling from the MCU.

[Table 8](#) describes each individual bit.

Table 8. STATUS REGISTER

#	BIT	DESCRIPTION
0	SLEEP	"0": Not SLEEP mode "1": SLEEP mode
1	BRAKE	"0": Not BRAKE mode "1": BRAKE mode
2	RELEASE	"0": Not RELEASE mode "1": RELEASE mode
3	DIAGNOSTIC	"0": Not DIAGNOSTIC mode "1": DIAGNOSTIC mode
4	ENFORCE DEMAG	"0": Not Enforce Demag mode "1": Enforce Demag mode
5	SAFE DEMAG	"0": Not Safe Demag mode "1": Safe Demag mode
7	OTHER MODES	"0": Not other modes "1": Other modes (Note 1)

See the Detailed Description paragraphs for further information about the operating modes.

Note 1: "Other modes" includes all other modes of the device (such as Power-up mode or fault modes) in which both OUT and OD are in a high impedance state.

Fault Registers (FAULT) – Read Only

Two 8-bit registers are provided to log fault or diagnostic information. If a fault or diagnostic event occurs, the corresponding bit is set logic high. By reading the FAULT register, the user can determine which fault caused the part to fail (see [Table 9](#) and [Table 10](#) for further details).

To clear the FAULT registers and restore normal operation, see the [Restore Normal Operation after a Fault](#) section.

All faults are latched, except for DLF3 and TWARN_UL.

Table 9. FAULT-1

BIT	NAME	DESCRIPTION
0	OCP0	Half-Bridge HS OCP
1	OCP1	Half-Bridge LS OCP
2	OCP2	LS FET OCP
3	TWARN_UL	Thermal Warning ~ +120°C - Not Latched
4	TSD	Thermal Shutdown ~ +160°C
5	UVLO	Undervoltage Lockout
6	UVLO5V	5V Undervoltage Lockout
7	UVLOCP	Charge-Pump Undervoltage Lockout

"0" = Logic Low = No Fault

"1" = Logic High = Fault Is Detected

Table 10. FAULT-2

BIT	NAME	DESCRIPTION
0	LFD1	Coil Shorted to V_M - Detection Is Enabled in DIAGNOSTIC Mode Only
1	LFD2	Coil Shorted to GND or Disconnected - Detection Is Enabled in DIAGNOSTIC Mode Only
2	SAFEDEM	Safe Demag Has Been Triggered

Table 10. FAULT-2 (continued)

3	ISM	Lack of Magnetization Current during Release
4	ODVM	OD Shorted to V_M
5	DVD	Demag Voltage Detection
6	TWARN	Thermal Warning ~ +120°C - Latched
7	LFD3	Either PWM or RLS Are Found Logic High while in DIAGNOSTIC mode

"0" = Logic Low = No Fault

"1" = Logic High = Fault Is Detected

Fault Diagnostic MASK Register (FAULT MASK) – Read/Write Only

The FAULT MASK register is a read/write register. When the bits are set low, the nFAULT indicator output is asserted when the fault is detected. When the bit is set logic high, the nFAULT indicator output is not asserted.

Table 11. FAULT MASK Register Table 1

BIT	NAME	DESCRIPTION	DEFAULT
0	OCP0	Half-Bridge HS OCP - Fault Mask	0
1	OCP1	Half-Bridge LS OCP - Fault Mask	0
2	OCP2	LS FET OCP - Fault Mask	0
3	TWARN	Thermal Warning ~ +120°C - Fault Mask	0
4	TSDN	Thermal Shutdown ~ +160°C - Fault Mask	0
5	UVLO	V_M Undervoltage Lockout - Fault Mask	0
6	UVLO5V	5V Undervoltage Lockout - Fault Mask	0
7	UVLOCP	Charge-Pump Undervoltage Lockout - Fault Mask	0

"0" = Logic Low = Fault Is Not Masked

"1" = Logic High = Fault Is Masked

Table 12. FAULT Mask Register Table 2

BIT	NAME	DESCRIPTION	DEFAULT
0	LFD1	LFD Fault 1 - Fault Mask	0
1	LFD2	LFD Fault 2 - Fault Mask	0
2	SAFEDEM	Safe Demagnetization - Mask	1
3	ISM	ISM Mask	1
4	ODVM	ODVM Mask	1
5	DVD	DVD Mask	1
6	RFU	Reserved for Future Use	0
7	LFD3	LFD Fault 3 - Fault Mask	0

"0" = Logic Low = Fault Is Not Masked

"1" = Logic High = Fault Is Masked

Action Enable (ACTION ENABLE) – Read/Write Register

The ENA_ bits of the ACTION ENABLE registers enables certain actions after the corresponding fault has been detected. For further information, see the LFD and ODVM descriptions.

Table 13. Action Enable ENA1, ENA2, EN3 Table

BIT	NAME	DESCRIPTION
0	ENA1	Enable Action after LFD1 Detection

Table 13. Action Enable ENA1, ENA2, EN3 Table (continued)

1	ENA2	Enable Action after LFD2 Detection
2	ENA3	Enable Action after ODVM Detection
3:7	RFU	Reserved for Future Use

"0" = Logic Low = Not ENABLED

"1" = Logic High = ENABLED

Configuration Registers (CONFIG) – Read/Write

Two one-byte configuration registers allows the user to configure the device.

- The CONFIG1 byte allows setting the slew rate, the CSA gain, and the ODM divider ratio as shown in [Table 14](#).
- The CONFIG2 byte includes the RESET bit and the Enforce Demag threshold configuration [Table 15](#).

Table 14. Configuration Register CONFIG1

#	BITS	DESCRIPTION	DEFAULT
0	SR0	Slew Rate Settings: "00" = 200V/μs, "01" = 100V/μs, "10" = 50V/μs, "11" = 25V/μs	"01" = 100V/μs
1	SR1		
2	GAIN0	GAIN Settings: "00" = 25, "01" = 50, "10" = 100, "11" = 200	"01" = 50
3	GAIN1		
4	SW/HW	Software/Hardware Control Selection Bit. Set SH/HW = "0" for Hardware Control through login input pins Set SH/HW = "1" for Software Control through I ² C	"0"
5	ODM0	Divider Settings: "00" = 12X, "01" = 18X, "10" = 24X, "11" = 60X	"10" = 24
6	ODM1		
7	RFU	Reserved for Future Use	"0"

Table 15. Configuration Register CONFIG2

#	BITS	DESCRIPTION	DEFAULT
0	RFU	Reserved for Future Use	"0": Normal Operating Mode
1	RESET	RESET Bit. Set RESET bit logic high to clear the FAULT/DIAG register. This bit is automatically reset at "0" once the the FAULT/DIAG register has been cleared	"0": Not Reset
2	DEMAG0	Set the "Enforce DEMAG" Threshold: "000" = disabled, "001" = 8V, "010" = 10V, "011" = 12V, "100" = 14V, "101" = 16V, "110" = 18V, "111" = 20V	"011" = 12V
3	DEMAG1		
4	DEMAG2		
5	NSLEEP	NSLEEP Bit. This bit is active only if SW/HW = "1" (Software Control). See the MAX22215 Control - Truth Table section for more information.	"0"
6	DIAG	DIAG Bit. This bit is active only if SW/HW = "1" (Software Control). See the MAX22215 Control - Truth Table section for more information.	"1"
7	RLS/ BRK	RELEASE/BRAKE Selection Bit. This bit is active only if SW/HW = "1" (Software Control). See the MAX22215 Control - Truth Table section for more information.	"0"

Register Map

RFU

ADDRESS	NAME	MSB							LSB
FUNC_BLOCK									
0x00	CHIP_REV[7:0]	-	-	-	-	CHIP_REV[3:0]			
0x01	CONFIGURATION1[7:0]	-	ODM[1:0]		SW_HW	GAIN[1:0]		SR[1:0]	
0x02	CONFIG2[7:0]	RLS_BRK	DIAG	NSLEEP	DEMAG[2:0]			RESET	-
0x03	FAULT1[7:0]	UVLOCP	UVLO5V	UVLO	TSD	TWARN_UL	OCP2	OCP1	OCP0
0x04	FAULT2[7:0]	LFD3	TWARN	DVD	ODVM	ISM	SAFEDEM	LFD2	LFD1
0x05	FAULT_MASK1[7:0]	UVLO_CP	UVLO_5V	UVLO	TSDN	TWARN	OCP2	OCP1	OCP0
0x06	FAULT_MASK2[7:0]	LFD1	-	DVD	ODVM	ISM	SAFEDEM	LFD2	LFD1
0x07	ACTION_ENABLE[7:0]	-	-	-	ODVM_TIME[1:0]		ENA3	ENA2	ENA1
0x08	CONTROL_STS[7:0]	s_FLT_PWP	-	s_SAFE_DMG	s_ENF_DMG	s_DIAG	s_RLS	s_BRK	s_SLEEP

Register Details

[CHIP_REV \(0x00\)](#)

BIT	7	6	5	4	3	2	1	0
Field	-	-	-	-	CHIP_REV[3:0]			
Reset	-	-	-	-	0x1			
Access Type	-	-	-	-	Read Only			

BITFIELD	BITS	DESCRIPTION
CHIP_REV	3:0	

[CONFIGURATION1 \(0x01\)](#)

BIT	7	6	5	4	3	2	1	0
Field	-	ODM[1:0]		SW_HW	GAIN[1:0]		SR[1:0]	
Reset	-	0x2		0x0	0x1		0x1	
Access Type	-	Write, Read		Write, Read	Write, Read		Write, Read	

BITFIELD	BITS	DESCRIPTION	DECODE
ODM	6:5	Divider Settings	0x0: 12X 0x1: 18X 0x2: 24X 0x3: 60X

BITFIELD	BITS	DESCRIPTION	DECODE
SW_HW	4	Software/Hardware Control Selection Bit	0x0: Hardware control through logic input pins 0x1: Software control through I ² C
GAIN	3:2	GAIN Settings	0x0: 25 0x1: 50 0x2: 100 0x3: 200
SR	1:0	Slew-Rate Settings	0x0: 200V/μs 0x1: 100V/μs 0x2: 50V/μs 0x3: 25V/μs

CONFIG2 (0x02)

BIT	7	6	5	4	3	2	1	0
Field	RLS_BRK	DIAG	NSLEEP	DEMAG[2:0]			RESET	–
Reset	0x0	0x0	0x0	0x3			0x0	–
Access Type	Write, Read	Write, Read	Write, Read	Write, Read			Write Only Clears All	–

BITFIELD	BITS	DESCRIPTION	DECODE
RLS_BRK	7	RELEASE/BRAKE Selection Bit. This bit is active only if SW/HW = "1" (Software Control).	0x0: BRAKE mode request 0x1: RELEASE mode request
DIAG	6	DIAG Bit. This bit is active only if SW/HW = "1" (Software Control).	0x0: No DIAGNOSTIC mode request 0x1: DIAGNOSTIC mode request
NSLEEP	5	NSLEEP Bit. This bit is active only if SW/HW = "1" (Software Control).	0x0: SLEEP mode request 0x1: No SLEEP mode request
DEMAG	4:2	Set the "Enforce DEMAG" Threshold	0x0: Disabled 0x1: 8V 0x2: 10V 0x3: 12V 0x4: 14V 0x5: 16V 0x6: 18V 0x7: 20V
RESET	1	RESET Bit. Set RESET bit logic high to clear the FAULT/DIAG register. This bit is automatically reset at "0" once the the FAULT/DIAG register has been cleared.	

FAULT1 (0x03)

BIT	7	6	5	4	3	2	1	0
Field	UVLOCP	UVLO5V	UVLO	TSD	TWARN_UL	OCP2	OCP1	OCP0
Reset	0x1	0x1	0x1	0x0	0x0	0x0	0x0	0x0
Access Type	Read Only	Read Only	Read Only	Read Only	Read Only	Read Only	Read Only	Read Only

BITFIELD	BITS	DESCRIPTION
UVLOCP	7	Charge-Pump Undervoltage Lockout
UVLO5V	6	5V Undervoltage Lockout
UVLO	5	Undervoltage Lockout

BITFIELD	BITS	DESCRIPTION
TSD	4	Thermal Shutdown ~ +160°C
TWARN_UL	3	Thermal Warning ~ +120°C - Not Latched
OCP2	2	LS FET OCP
OCP1	1	Half-Bridge LS OCP
OCP0	0	Half-Bridge HS OCP

FAULT2 (0x04)

BIT	7	6	5	4	3	2	1	0
Field	LFD3	TWARN	DVD	ODVM	ISM	SAFEDEM	LFD2	LFD1
Reset	0x0	0x0	0x0	0x0	0x0	0x0	0x0	0x0
Access Type	Read Only	Read Only	Read Only	Read Only	Read Only	Read Only	Read Only	Read Only

BITFIELD	BITS	DESCRIPTION
LFD3	7	Either PWM or BRK/RLS Shorted to a Positive Rail. Detection is enabled in DIAGNOSTIC mode only.
TWARN	6	Thermal Warning ~ +120°C - Latched
DVD	5	Demag Voltage Detection
ODVM	4	OD Shorted to V_M
ISM	3	Lack of Magnetization Current during Release
SAFEDEM	2	SafeDemag Has Been Triggered
LFD2	1	Coil Shorted to GND or Disconnected. Detection is enabled in DIAGNOSTIC mode only.
LFD1	0	Coil Shorted to V_M . Detection is enabled in DIAGNOSTIC mode only.

FAULT_MASK1 (0x05)

BIT	7	6	5	4	3	2	1	0
Field	UVLO_CP	UVLO_5V	UVLO	TSDN	TWARN	OCP2	OCP1	OCP0
Reset	0x0	0x0	0x0	0x0	0x0	0x0	0x0	0x0
Access Type	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION
UVLO_CP	7	Charge-Pump Undervoltage Lockout - Fault Mask
UVLO_5V	6	5V Undervoltage Lockout - Fault Mask
UVLO	5	V_M Undervoltage Lockout - Fault Mask
TSDN	4	Thermal Shutdown ~ +160°C - Fault Mask
TWARN	3	Thermal Warning ~ +120°C - Fault Mask
OCP2	2	LS FET OCP - Fault Mask
OCP1	1	Half-Bridge LS OCP - Fault Mask
OCP0	0	Half-Bridge HS OCP - Fault Mask

FAULT_MASK2 (0x06)

BIT	7	6	5	4	3	2	1	0
Field	LFD1	–	DVD	ODVM	ISM	SAFEDEM	LFD2	LFD1
Reset	0x0	–	0x1	0x0	0x1	0x1	0x0	0x0
Access Type	Write, Read	–	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION
LFD1	7	LFD Fault 3 - Fault Mask
DVD	5	DVD - Mask
ODVM	4	ODVM - Mask
ISM	3	ISM - Mask
SAFEDEM	2	Safe Demagnetization - Mask
LFD2	1	LFD Fault 2 - Fault Mask
LFD1	0	LFD Fault 1 - Fault Mask

ACTION_ENABLE (0x07)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	ODVM_TIME[1:0]		ENA3	ENA2	ENA1
Reset	–	–	–	0x2		0x1	0x1	0x1
Access Type	–	–	–	Write, Read		Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
ODVM_TIME	4:3	ODVM Programmable Time	0x0: 100ms 0x1: 200ms 0x2: 400ms 0x3: 800ms
ENA3	2	Enable Action after ODVM Detection	
ENA2	1	Enable Action after LFD2 Detection	
ENA1	0	Enable Action after LFD1 Detection	

CONTROL_STS (0x08)

BIT	7	6	5	4	3	2	1	0
Field	s_FLT_PWP	–	s_SAFE_DMG	s_ENF_DM G	s_DIAG	s_RLS	s_BRK	s_SLEEP
Reset	0x1	–	0x0	0x0	0x0	0x0	0x0	0x0
Access Type	Read Only	–	Read Only	Read Only	Read Only	Read Only	Read Only	Read Only

BITFIELD	BITS	DESCRIPTION
s_FLT_PWP	7	Fault/Power-Up Status Bit
s_SAFE_DMG	5	SafeDemag Bit
s_ENF_DM G	4	Enforce Demag Status Bit
s_DIAG	3	DIAGNOSTIC Mode Status Bit
s_RLS	2	RELEASE Mode Status Bit

BITFIELD	BITS	DESCRIPTION
s_BRK	1	BRAKE Mode Status Bit
s_SLEEP	0	SLEEP Mode Status Bit

Applications Information

Motor Brake Control

The MAX22215 provides high flexibility with an I²C interface to configure all of its unique features. The [Typical Application Circuits](#) diagram shows the typical I²C-based brake application this part is mainly designed for.

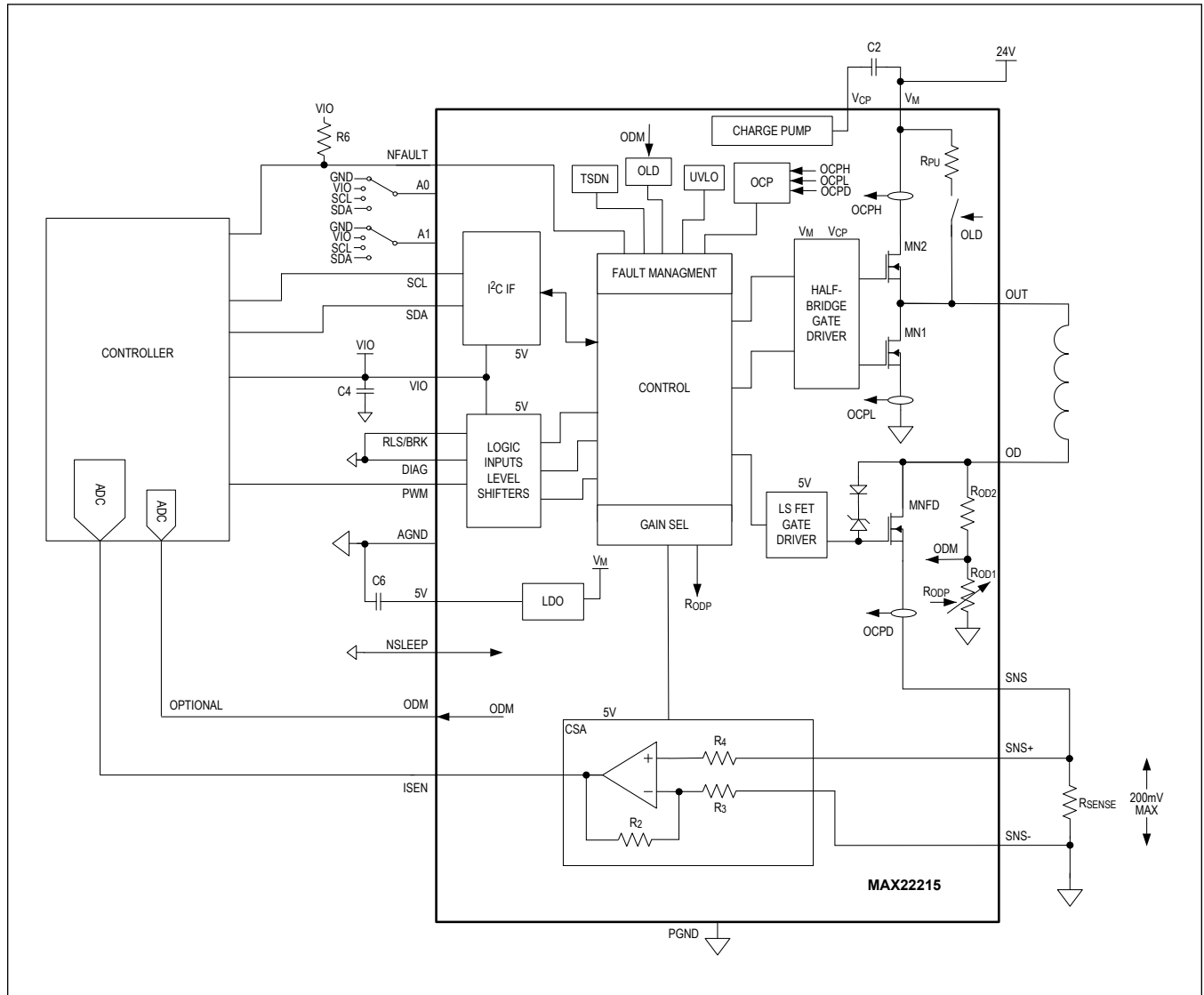
The MCU and the driver communicate through the I²C interface. Up to 16 devices can share the same I²C bus. Configuration settings are written into the device after power up. Status information is exchanged and the condition read out through I²C, such as the dedicated fault and diagnostic output triggering an interrupt.

A PWM input is used to control excitation, hold, and demagnetization currents. With an external sense resistor, a highly accurate current-sense amplifier senses the voltage drop during brake-engaged and brake-released operations. The CSA analog output signal can be used for diagnostic purposes or as feedback signal for an external control loop. The ODM pin can be used to monitor the brake voltage.

It is possible to control the brake status by simply connecting/disconnecting the power supply (V_M). The VDEM function enforces the part in BRAKE mode as soon as the V_M drops below the threshold. When the V_M is disconnected and drops below the UVLO V_M , the 5V LDO is powered OFF. However if a large reservoir capacitor is externally connected to the 5V pin, it is possible to keep monitoring the status of the brake even in absence of the V_M until the mechanical brake event occurs. In a typical hardware configuration, the bypass capacitance on V_M is about 4.4 μ F, while the bypass capacitance on 5V is greater than 100 μ F.

Typical Application Circuits

Application Diagram



Ordering Information

PART NUMBER	TEMP RANGE	PIN-PACKAGE
MAX22215ATU+	-40°C to +125°C	38 TQFN (5mm x 7mm)
MAX22215ATU+T	-40°C to +125°C	38 TQFN (5mm x 7mm)

+ Denotes a lead(Pb)-free/RoHS-compliant package.

T Denotes tape-and-reel.

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	3/26	Initial release	—