15A, 2MHz, 2.7V to 16V Integrated Step-Down Switching Regulator with PMBus

MAX20815

General Description

The MAX20815 is a fully integrated, highly efficient, step-down DC-DC switching regulator with PMBus interface. The device operates from 2.7V to 16V input supplies, and the output can be adjusted from 0.4V to 5.8V, delivering up to 15A of load current.

The switching frequency of the device can be configured from 500kHz to 2MHz, to provide the capability of optimizing the design in terms of size and performance.

The MAX20815 utilizes fixed frequency, current-mode control with internal compensation. The IC features selectable advanced modulation scheme (AMS) to provide improved performance during fast load transients. Operation settings and configurable features can be selected by connecting a pin-strap resistors from PGM_ pins to ground or using PMBus commands.

The MAX20815 has an internal 1.8V LDO output to power the gate drives (V_{CC}) and internal circuitry (AVDD). The device also has an optional LDO input pin (LDOIN), allowing connection from a 2.5V to 5.5V bias input supply for optimized efficiency.

The IC has multiple protections including positive and negative overcurrent protection, output overvoltage protection, and overtemperature protection to ensure robust design.

The device is available in a 4.3mm x 6.55mm FC2QFN package. It supports -40°C to +125°C junction temperature operation. The MAX20815 is footprint compatible with the MAX20810 and MAX20830.

Applications

- Data Center Power
- Communications Equipment
- Networking Equipment
- Servers and Storage
- Point-of-Load (PoL) Voltage Regulators

***Ordering Information* appears at end of data sheet.**

Benefits and Features

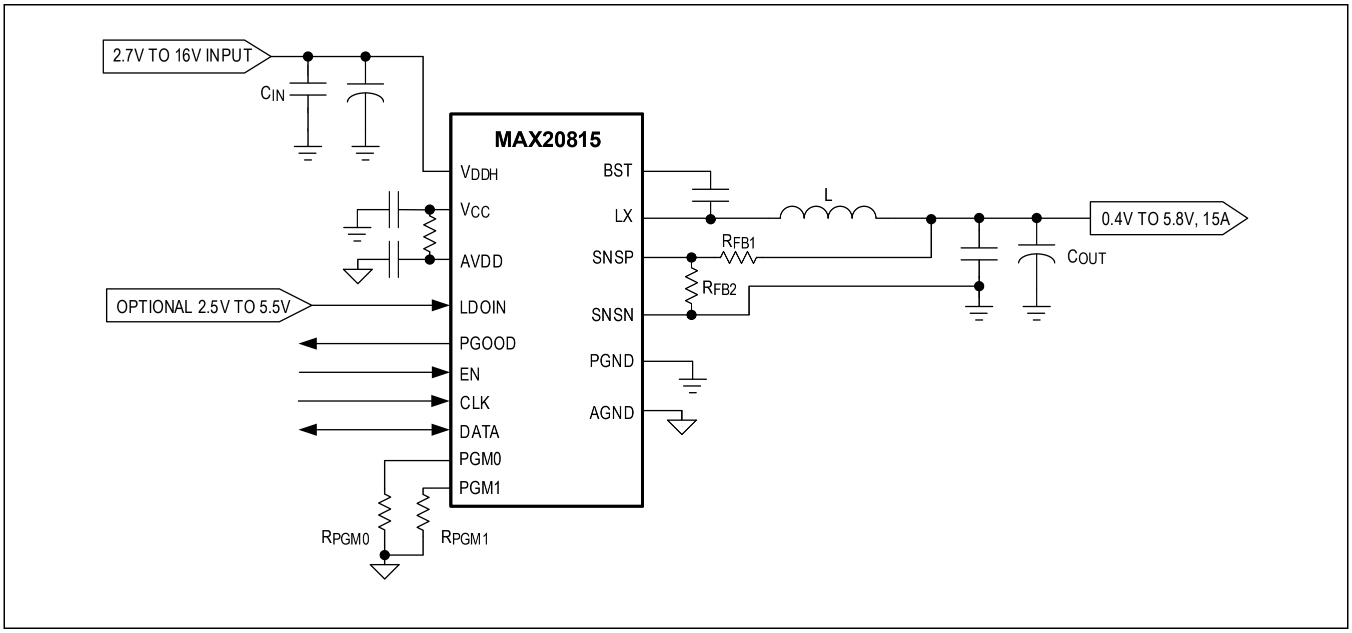
- High Power Density with Low Component Count
  - Compact 4.3mm x 6.55mm, 16-Pin, FC2QFN Package
  - Internal Compensation
  - Single-Supply Operation with Integrated LDO for Bias Generation
- Wide Operating Range
  - 2.7V to 16V Input Voltage Range
  - 0.4V to 5.8V Output Voltage Range
  - 500kHz to 2MHz Configurable Switching Frequency
  - -40°C to +125°C Junction Temperature Range
- Optimized Performance and Efficiency
  - 93.8% Peak Efficiency with V_{DDH} = 12V and V_{OUT} = 1.8V
  - High Efficiency with Optional External Bias Input Supply
  - AMS to Improve Load-Transient Response
  - Differential Remote Sense
- PMBus Interface
  - Adaptive Voltage Scaling of 0.4V to 0.8V Reference Range
  - PMBus Telemetry of Output Current, Output Voltage, Input Voltage, and Junction Temperature

DESCRIPTION	CURRENT RATING* (A)	INPUT VOLTAGE (V)	OUTPUT VOLTAGE (V)
Electrical Rating	15	2.7 to 16	0.4 to 5.8
Thermal Rating T_A = 55°C, 200LFM air flow	15	12	3.3
Thermal Rating T_A = 85°C, no air flow	15	12	1.8

**Maximum T_J = +125°C. For specific operating conditions, see the Safe Operating Area (SOA) curves in the Typical Operating Characteristics section.*

19-101637; Rev 2; 9/25

Simplified Application Circuit



Absolute Maximum Ratings

V_{DDH} to PGND (Note 1) .... -0.3V to +19V
LX to PGND (DC)... -0.3V to +19V
LX to PGND (AC) (Note 2).................................. -10V to +23V
(AC) (Note 3).................................. -10V to +25V
V_{DDH} to LX (DC) (Note 1)................................. -0.3V to +19V
V_{DDH} to LX (AC) (Note 2).................................. -10V to +23V
(AC) (Note 3).................................. -10V to +25V
BST to PGND (DC) .... -0.3V to +21.5V
BST to PGND (AC) (Note 2) .... -7V to +25.5V
(AC) (Note 3)............................... -7V to +27.5V
BST to LX.. -0.3V to +2.5V
PGND to AGND ....-0.3V to +0.3V
V_{CC} to PGND ....-0.3V to +2.5V
AVDD to AGND ....-0.3V to +2.5V
LDOIN to AGND ....-0.3V to +6V
EN, PGOOD, CLK, DATA to AGND ....-0.3V to +4V
SNSP to AGND..-0.3V to AVDD+0.3V
SNSN to AGND ....-0.3V to +0.3V
PGM0, PGM1 to AGND ....-0.3V to AVDD+0.3V
Peak LX Current ....-25A to +34A
Junction Temperature (T_J) ....+150°C
Storage Temperature Range......................... -65°C to +150°C
Peak Reflow Temperature Lead-Free ....+260°C

Note 1: Input HF capacitors placed not more than 40 mils away from the V_{DDH} pin required to keep inductive voltage spikes within Absolute Maximum limits.
Note 2: AC is limited to 25ns per cycle.
Note 3: AC is limited to 2ns per cycle.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Package Information

16 FC2QFN

Package Code	F164A6F+2
Outline Number	21-100528
Land Pattern Number	90-100191
Thermal Resistance	
Junction to Ambient (θ_{JA})	48.5°C/W
Junction to Case (θ_{JC})	10.7°C/W
Junction to Ambient (θ_{JA}) on MAX20815EVKIT# (no heat sink, no airflow)	18.1°C/W

For the latest package outline information and land patterns (footprints), go to www.analog.com/en/design-center/packaging-quality-symbols-footprints/package-index.html. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, Refer to www.analog.com/en/technical-articles/thermal-characterization-of-ic-packages.html.

Electrical Characteristics

(See *Typical Application Circuits*. V_{DDH} = 12V, V_{LDOIN} = 3.3V, T_A = T_J = -40°C to +125°C, unless otherwise noted. Specifications are production tested at T_A = +32°C; limits within the operating temperature range are guaranteed by design and characterization.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
INPUT SUPPLY						
Input Voltage Range	V_{DDH}		2.7		16	V
Input Supply Current	I_{VDDH}	V_{LDOIN} = 3.3V, EN = AGND		0.12		mA
		V_{LDOIN} = AGND, EN = AGND		6.5		
Linear Regulator Input Voltage	V_{LDOIN}		2.5		5.5	V
Linear Regulator Input Current	I_{LDOIN}	V_{LDOIN} = 3.3V, EN = AGND		6.4		mA
Internal LDO Regulated Output	V_{CC}		1.71	1.80	1.95	V
Linear Regulator Current Limit		V_{LDOIN} = AGND	85	170		mA
		V_{LDOIN} = 3.3V	100	230		
		V_{CC} < 1.6V		25		
AVDD Undervoltage Lockout	AVDD	Rising	1.65	1.67	1.70	V
AVDD Undervoltage Lockout Hysteresis				55		mV
V_{DDH} Undervoltage Lockout		Rising	2.4	2.5	2.6	V
V_{DDH} Undervoltage Lockout Hysteresis				100		mV
LDOIN Undervoltage Lockout	V_{LDOIN}	Rising	2.26	2.33	2.40	V
LDOIN Undervoltage Lockout Hysteresis				100		mV
OUTPUT VOLTAGE RANGE AND ACCURACY						
Feedback Voltage Accuracy	V_{SNSP} – V_{SNSN}	V_{REF} = 0.5V	-0.6		+0.6	%
		V_{REF} = 0.4V to 0.8V	-1		+1	
		V_{REF} = 0.4V to 0.8V, T_A = T_J = 0°C to +85°C	-0.6		+0.6	
Positive Voltage Sense Leakage Current	I_{SNSP}		-1		+1	µA
Negative Voltage Sense Input Range	V_{SNSN}		-100		+100	mV
Negative Voltage Sense Bias Current	I_{SNSN}			300	550	µA
SWITCHING FREQUENCY						
Switching Frequency	f_{SW}			500		kHz
				600		
				750		
				1000		
				1200		
				2000		
Switching Frequency Accuracy			-10		+10	%

(See *Typical Application Circuits*. V_{DDH} = 12V, V_{LDOIN} = 3.3V, T_A = T_J = -40°C to +125°C, unless otherwise noted. Specifications are production tested at T_A = +32°C; limits within the operating temperature range are guaranteed by design and characterization.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Minimum Controllable On-Time		Inductor valley current ≤ 0A (*Note 4*)		36	50	ns
		Inductor valley current > 0A (*Note 4*)		30	45	
Minimum Controllable Off-Time		(*Note 4*)		100	140	ns
ENABLE AND STARTUP						
Initialization Time	t_{INIT}			800		µs
EN Threshold		Rising	0.9			V
		Falling			0.6	
EN Filtering Delay		Rising		250		µs
		Falling		2		
Soft-Startup Slew Rate	V_{SNSP} – V_{SNSN}			0.5		V/ms
POWER-GOOD AND FAULT PROTECTIONS						
PGOOD Output Low		I_{PGOOD} = 4mA			0.4	V
Output Undervoltage (UV) Threshold		V_{REF} = 0.5V	-16	-13	-10	%
Output UV Deglitch Delay				2		µs
Output Overvoltage Protection (OVP) Threshold		V_{REF} = 0.5V	10	13	16	%
Output OVP Threshold Deglitch Delay				2		µs
Positive Overcurrent Protection (POCP) Threshold		Inductor peak current, POCP = 20A	18	20	22	A
		Inductor peak current, POCP = 17.3A	15.6	17.3	19	
		Inductor peak current, POCP = 14.6A	13.1	14.6	16.1	
		Inductor peak current, POCP = 12A	10.8	12	13.2	
POCP Deglitch Delay	t_{POCP}			40		ns
Fast Positive Overcurrent Protection (FPOCP) Threshold			22.7	25.3	28.8	A
Negative Overcurrent Protection (NOCP) Threshold to POCP Threshold Ratio				-83		%
NOCP Accuracy			-20		+20	%
BST UVLO Threshold	V_{BST} – V_{LX}		1.48	1.56	1.64	V
BST UVLO Threshold Hysteresis				52		mV
Overtemperature Protection (OTP) Rising Threshold				155		°C
OTP Accuracy				6		%
OTP Hysteresis				20		°C
Hiccup Protection Time		OVP, POCP, or NOCP		20		ms

(See Typical Application Circuits. V_{DDH} = 12V, V_{LDOIN} = 3.3V, T_A = T_J = -40°C to +125°C, unless otherwise noted. Specifications are production tested at T_A = +32°C; limits within the operating temperature range are guaranteed by design and characterization.)

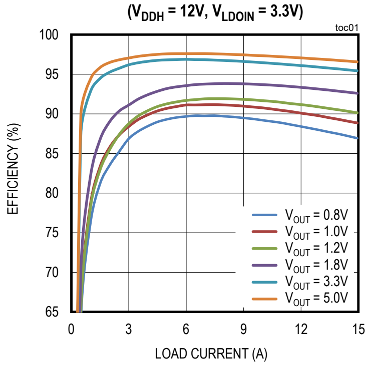
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
DCM OPERATION MODE						
DCM Comparator Threshold to Enter DCM		Inductor valley current, POCP = 20A		-0.75		A
		Inductor valley current, POCP = 17.3A		-0.67		
		Inductor valley current, POCP = 14.6A		-0.6		
		Inductor valley current, POCP = 12A		-0.45		
DCM Comparator Threshold to Exit DCM		Inductor valley current		0.07		A
PMBus INTERFACE						
CLK, DATA Input Logic Low Voltage					0.8	V
CLK, DATA Input Logic High Voltage			1.45			V
CLK, DATA Input Leakage Current			-1		+1	µA
DATA Output Logic Low		Sinking 4mA			0.4	V
PMBus Operating Frequency	f_{CLK}				1000	kHz
DATA Hold Time from CLK	t_{HD_DAT}	(Note 4)	0			ns
DATA Setup Time from CLK	t_{SU_DAT}	(Note 4)	50			ns
CLK High Period	t_{HIGH}	(Note 4)	0.26			µs
CLK Low Period	t_{LOW}	(Note 4)	0.5			µs
PMBus TELEMETRY						
Reading Update Rate		READ_IOUT, READ_VOUT and READ_VIN		1.47		ms
		READ_TEMPERATURE		2.86		
READ_IOUT Range			0		20	A
READ_IOUT Accuracy		I_{OUT} = 0A	-1		+1	A
		0A < I_{OUT} < 20A	-1.5		+1.5	
READ_VOUT Range		Feedback voltage sensed between SNSP and SNSN		V_{REF} ± 200		mV
READ_VOUT Accuracy		Feedback voltage sensed between SNSP and SNSN	-1.5		+1.5	%
READ_VIN Range			2.3		16	V
READ_VIN Accuracy			-350		+350	mV
READ_TEMPERATURE Range			-40		+150	°C
READ_TEMPERATURE Accuracy				±4		°C
PROGRAMMING PINS						
PGM_ Pin Resistor Range			0.095		115	kΩ
PGM_ Resistor Accuracy			-1		+1	%

Note 4: Guaranteed by design.

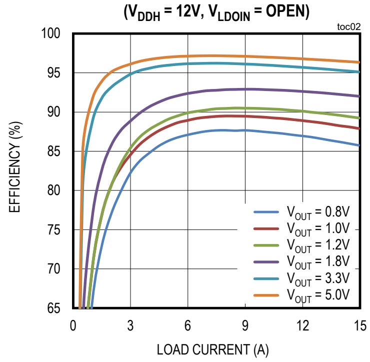
Typical Operating Characteristics

(*Typical Application Circuits*, tested on MAX20815EVKIT#, V_{DDH} = 12V, f_{SW} = 500kHz, T_A = +25°C, inductor = PA5034.XXXHLT or PA4987.102HL for V_{OUT} > 2.5V, unless otherwise noted.)

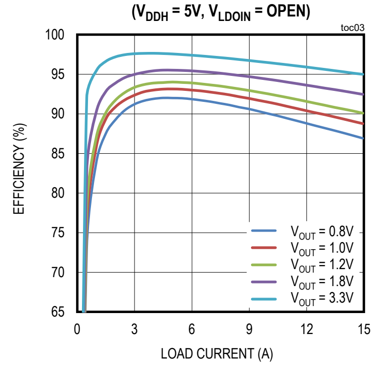
EFFICIENCY
(V_{DDH} = 12V, V_{LDOIN} = 3.3V)



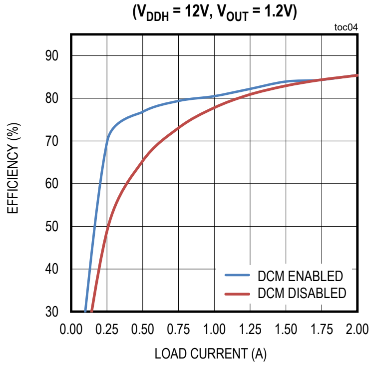
EFFICIENCY
(V_{DDH} = 12V, V_{LDOIN} = OPEN)



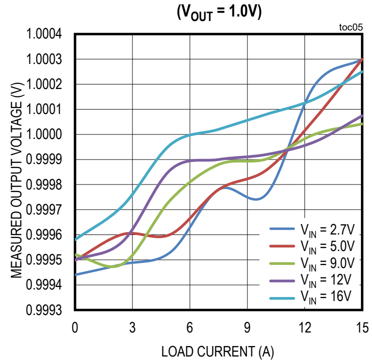
EFFICIENCY
(V_{DDH} = 5V, V_{LDOIN} = OPEN)



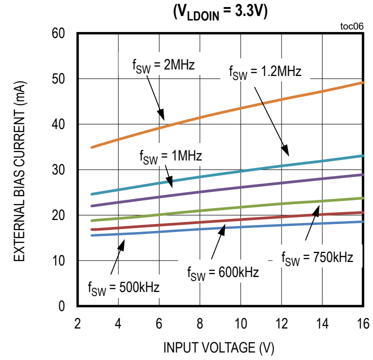
EFFICIENCY (DCM vs CCM)
(V_{DDH} = 12V, V_{OUT} = 1.2V)



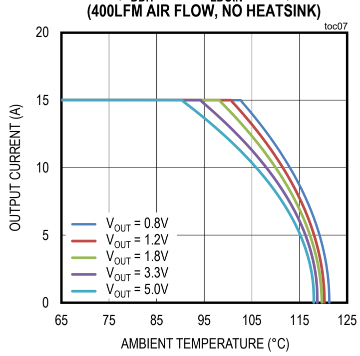
LOAD AND LINE REGULATIONS
(V_{OUT} = 1.0V)



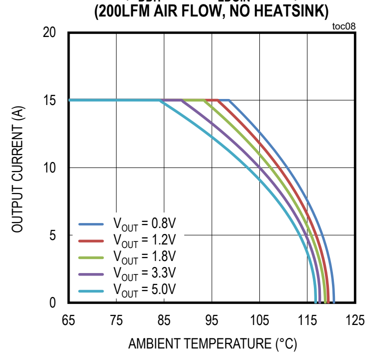
EXTERNAL BIAS SUPPLY CURRENT
(V_{LDOIN} = 3.3V)



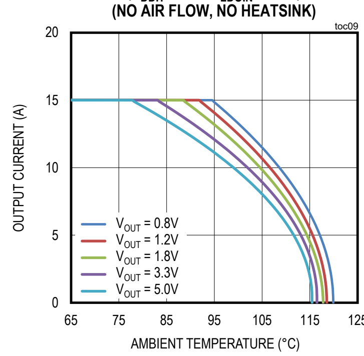
SAFE OPERATING AREA
(V_{DDH} = 12V, V_{LDOIN} = 3.3V)
(400LFM AIR FLOW, NO HEATSINK)



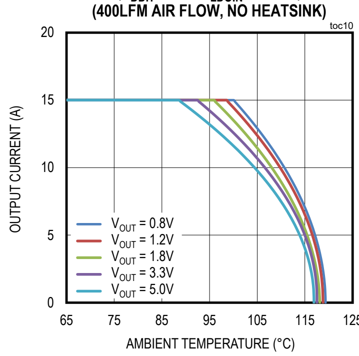
SAFE OPERATING AREA
(V_{DDH} = 12V, V_{LDOIN} = 3.3V)
(200LFM AIR FLOW, NO HEATSINK)



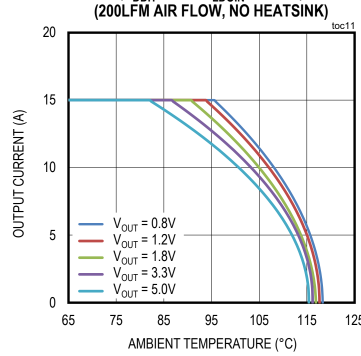
SAFE OPERATING AREA
(V_{DDH} = 12V, V_{LDOIN} = 3.3V)
(NO AIR FLOW, NO HEATSINK)



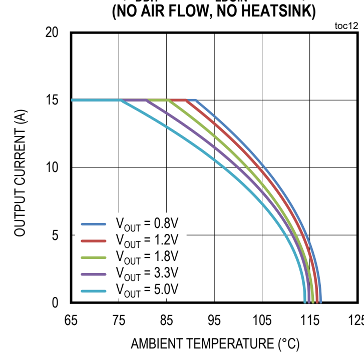
SAFE OPERATING AREA
(V_{DDH} = 12V, V_{LDOIN} = OPEN)
(400LFM AIR FLOW, NO HEATSINK)



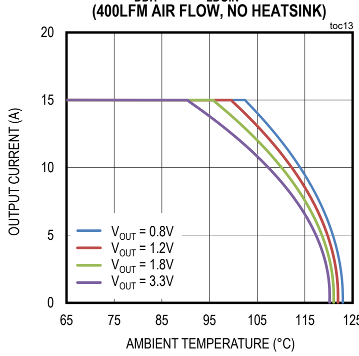
SAFE OPERATING AREA
(V_{DDH} = 12V, V_{LDOIN} = OPEN)
(200LFM AIR FLOW, NO HEATSINK)



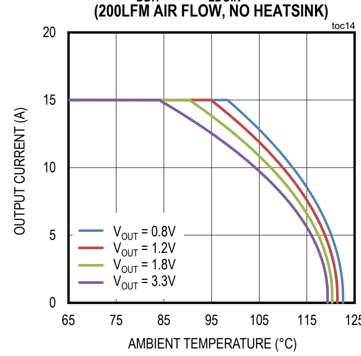
SAFE OPERATING AREA
(V_{DDH} = 12V, V_{LDOIN} = OPEN)
(NO AIR FLOW, NO HEATSINK)



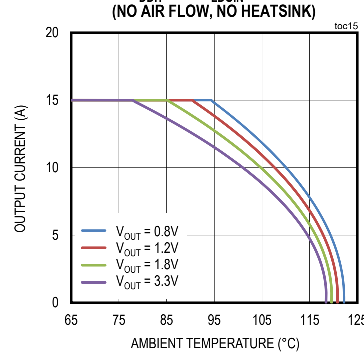
SAFE OPERATING AREA
(V_{DDH} = 5V, V_{LDOIN} = OPEN)
(400LFM AIR FLOW, NO HEATSINK)



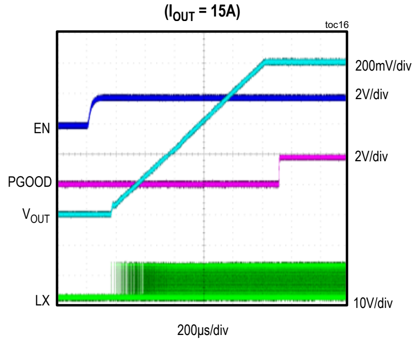
SAFE OPERATING AREA
(V_{DDH} = 5V, V_{LDOIN} = OPEN)
(200LFM AIR FLOW, NO HEATSINK)



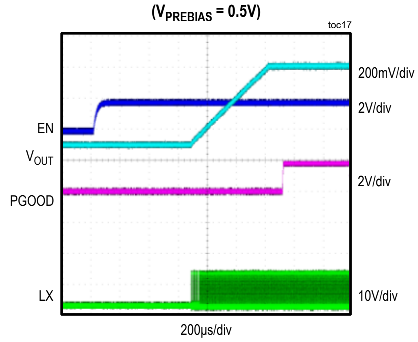
SAFE OPERATING AREA
(V_{DDH} = 5V, V_{LDOIN} = OPEN)
(NO AIR FLOW, NO HEATSINK)



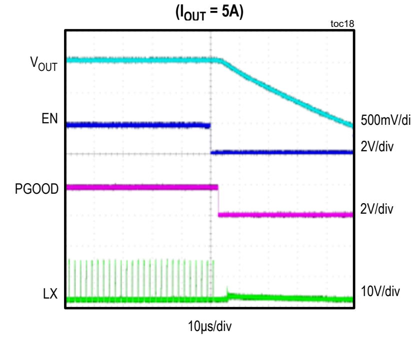
STARTUP
(I_{OUT} = 15A)



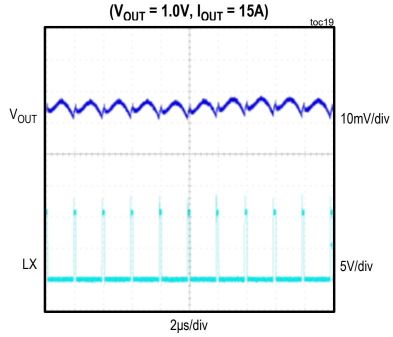
PRE-BIASED STARTUP
($V_{PREBIAS}$ = 0.5V)



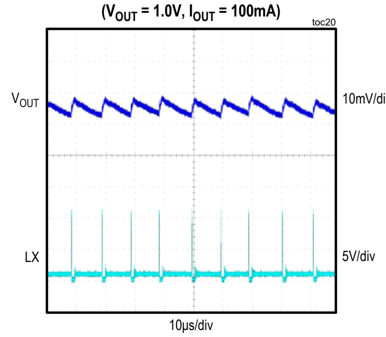
SHUTDOWN
(I_{OUT} = 5A)



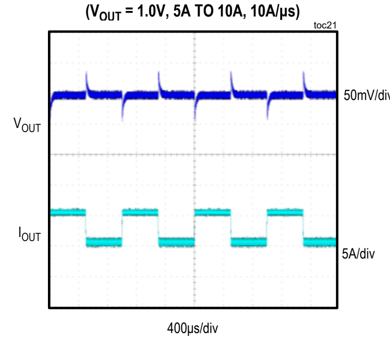
OUTPUT VOLTAGE RIPPLE
(V_{OUT} = 1.0V, I_{OUT} = 15A)

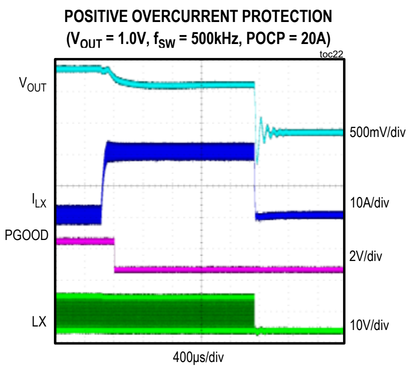


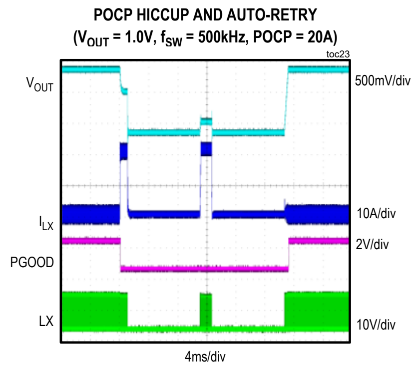
OUTPUT VOLTAGE RIPPLE
(DCM OPERATION)
(V_{OUT} = 1.0V, I_{OUT} = 100mA)

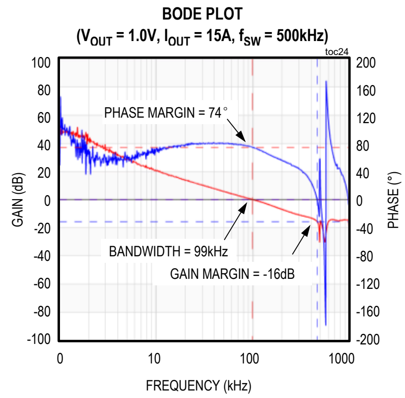


LOAD-TRANSIENT RESPONSE
(V_{OUT} = 1.0V, 5A TO 10A, 10A/µs)

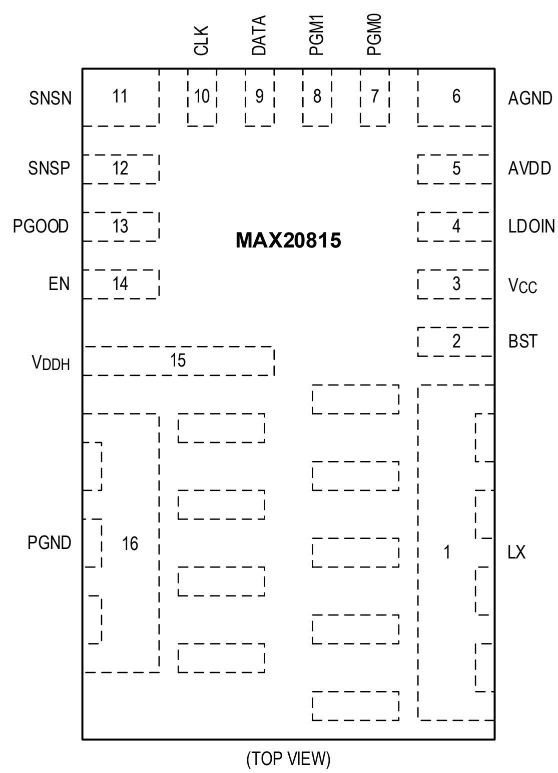








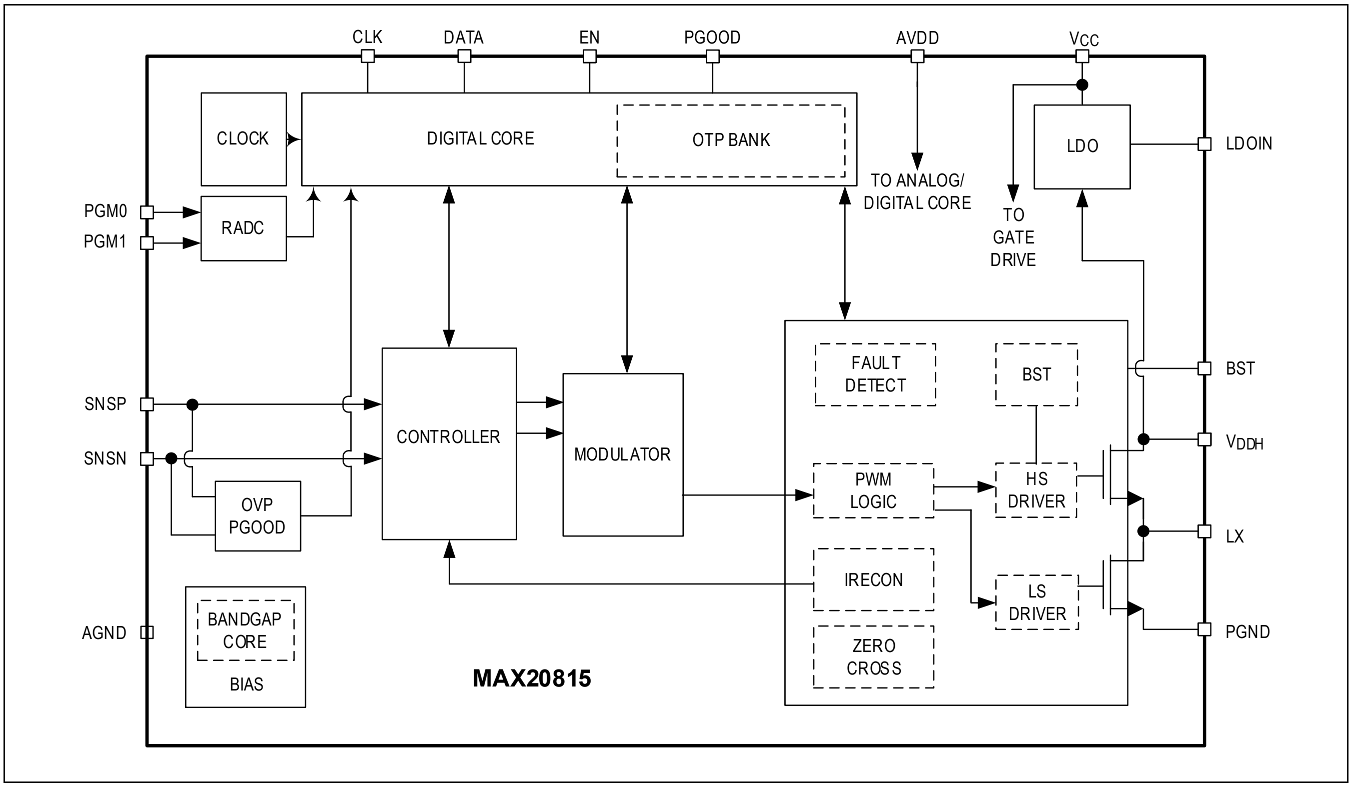
Pin Configurations



Pin Descriptions

PIN	NAME	FUNCTION
1	LX	Switching Node. Connect LX directly to the output inductor.
2	BST	Bootstrap Pin. Connect a 0.47μF ceramic capacitor from BST to LX.
3	V_{CC}	Internal 1.8V LDO Output. Connect a 4.7μF or greater ceramic capacitor from V_{CC} to PGND.
4	LDOIN	Optional 2.5V to 5.5V LDO Input Supply. Leave this pin floating if unused.
5	AVDD	1.8V Supply for Analog Circuitry. Connect a 2.2Ω to 4.7Ω resistor from AVDD to V_{CC}. Connect a 1μF or greater ceramic capacitor from AVDD to AGND.
6	AGND	Analog Ground
7	PGM0	Program Input. Connect this pin to ground though a programming resistor.
8	PGM1	Program Input. Connect this pin to ground though a programming resistor.
9	DATA	PMBus Data
10	CLK	PMBus Clock
11	SNSN	Output Voltage Remote Sense Negative Input
12	SNSP	Output Voltage Remote Sense Positive Input Pin. Connect SNSP to output voltage at the load. A resistive voltage divider can be inserted between the output and SNSP to regulate the output above the reference voltage.
13	PGOOD	Open-Drain, Power-Good Output
14	EN	Output Enable
15	V_{DDH}	Regulator Input Supply
16	PGND	Power Ground

Block Diagram



Detailed Description

Control Architecture

Fixed-Frequency Peak Current Mode Control Loop

The MAX20815 control loop is based on fixed-frequency, peak current-mode control architecture. A simplified control architecture is shown in *Figure 1*. The loop contains an error amplifier stage, internal voltage loop compensation network, current sense, internal slope compensation, and a PWM modulator that generates the PWM signals to drive high-side and low-side MOSFETs. The device has a default 0.5V feedback reference voltage (V_{REF}). The reference voltage can be adjusted by the PMBus VOUT_COMMAND from 0.4V to 0.8V with 1.95mV resolution (refer to the *UG2175: MAX20815 PMBus Command Set User Guide*). The difference of V_{REF} and the sensed output voltage is amplified by the first error amplifier. Its output voltage (V_{ERR}) is used as the input of the voltage loop compensation network. The output of the compensation network (V_{COMP}) is fed to a PWM comparator with a current-sense signal (V_{ISENSE}) and slope compensation (V_{RAMP}). The output of the PWM comparator is the input of the PWM modulator. The turning on of the high-side MOSFET is aligned with an internal clock. It can either be a fixed-frequency clock or a phase-shifted clock, if advanced modulation scheme (AMS) is enabled.

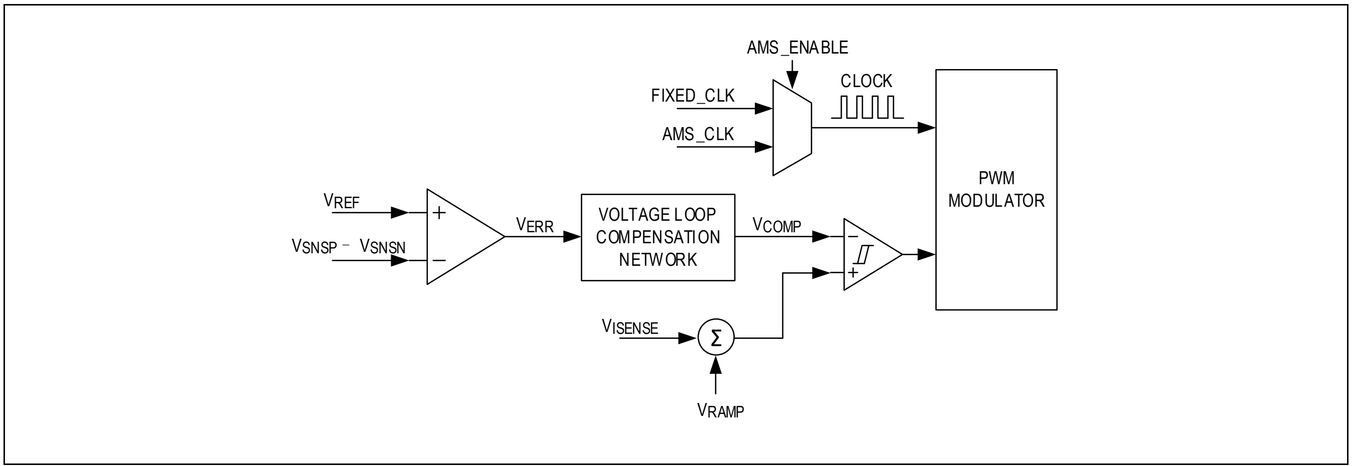


Figure 1. Simplified Control Architecture

Advanced Modulation Scheme (AMS)

The MAX20815 offers a selectable advanced modulation scheme (AMS) to provide improved transient response. AMS provides a significant advantage over conventional fixed-frequency PWM schemes. Enabling the AMS feature allows for modulation at both leading and trailing edges, which results in a temporary increase or decrease of the switching frequency during large load transients. Figure 2 shows the scheme to include leading-edge modulation to the traditional trailing-edge modulation when AMS is enabled in the device. The modulation scheme allows the turn on and off with minimal delay. Since the total inductor current increases very quickly, satisfying the load demand, the current drawn from output capacitors is reduced. With AMS enabled, the system closed-loop bandwidth can be extended without phase-margin penalty. As a result, the output capacitance can be minimized.

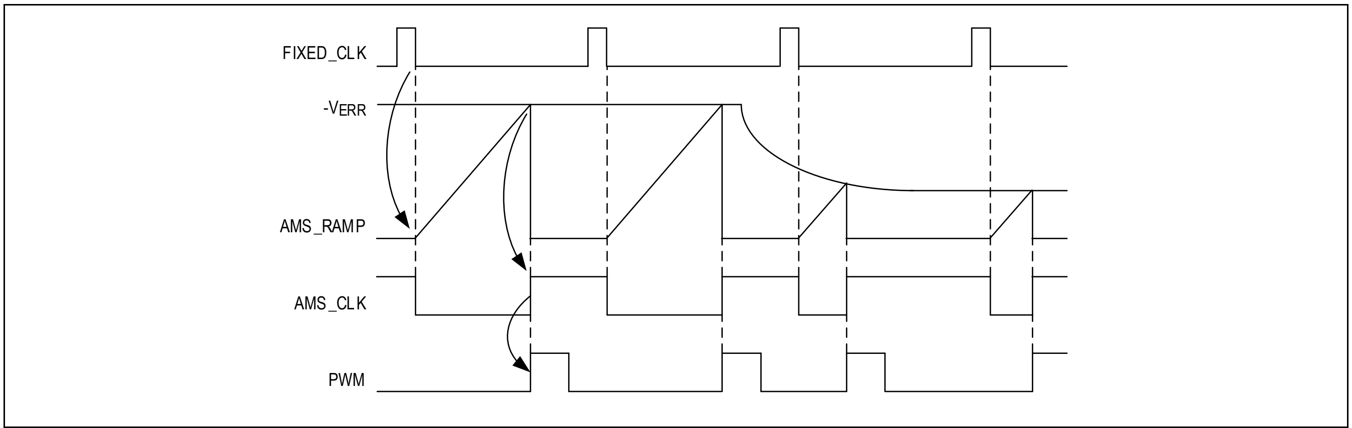


Figure 2. AMS Operation

Discontinuous Current-Mode (DCM) Operation

Discontinuous current mode (DCM) operation is an optional feature to improve light load efficiency. The MAX20815 has a DCM current detection comparator to monitor the inductor valley current while operating in CCM. At light load, if the inductor valley current is below the DCM comparator threshold for 56 consecutive cycles, the device transitions seamlessly to DCM. Once in DCM, the switching frequency decreases as load decreases. The device will transition back to CCM operation as soon as the inductor valley current is higher than 0A.

For the MAX20815, DCM is disabled by default; it can be enabled by PMBus commands (refer to the UG2175: MAX20815 PMBus Command Set User Guide).

Internal Linear Regulator

The device contains an internal 1.8V linear regulator (LDO). The 1.8V LDO output voltage on V_{CC} is derived from the V_{DDH} pin by default. To improve efficiency, an optional 2.5V to 5.5V bias input supply can be applied on the LDOIN pin so that the 1.8V voltage on V_{CC} is converted from the LDOIN pin instead. The optional LDOIN bias input supply can be applied or removed anytime during regulation without affecting operation.

The 1.8V voltage on the V_{CC} pin supplies the current to the MOSFET drivers. A decoupling capacitor of at least 4.7µF must be connected between V_{CC} and PGND. The AVDD pin of the MAX20815 also requires a 1.8V supply to power the device's internal analog circuitry. A 2.2Ω to 4.7Ω resistor must be connected between AVDD and V_{CC}. A 1µF or greater decoupling capacitor must be used between AVDD and AGND.

Startup and Shutdown

The startup and shutdown timing is shown in *Figure 3*. When the AVDD pin voltage is above its rising UVLO threshold, the device goes through an initialization procedure. Configuration settings on the PGM_ pins are read. Once initialization is complete, the device detects V_{DDH} UVLO and EN status. When both are above their rising thresholds, soft-start begins and switching is enabled. The output voltage of the enabled output starts to ramp up. The soft-start ramp time is 1ms. If there are no faults, the open-drain PGOOD pin is released from being held low after the soft-start ramp is complete. The device supports smooth startup with the output prebiased.

During operation, if either the V_{DDH} UVLO or EN falls below their thresholds, switching is stopped immediately. The output voltage is discharged by load current.

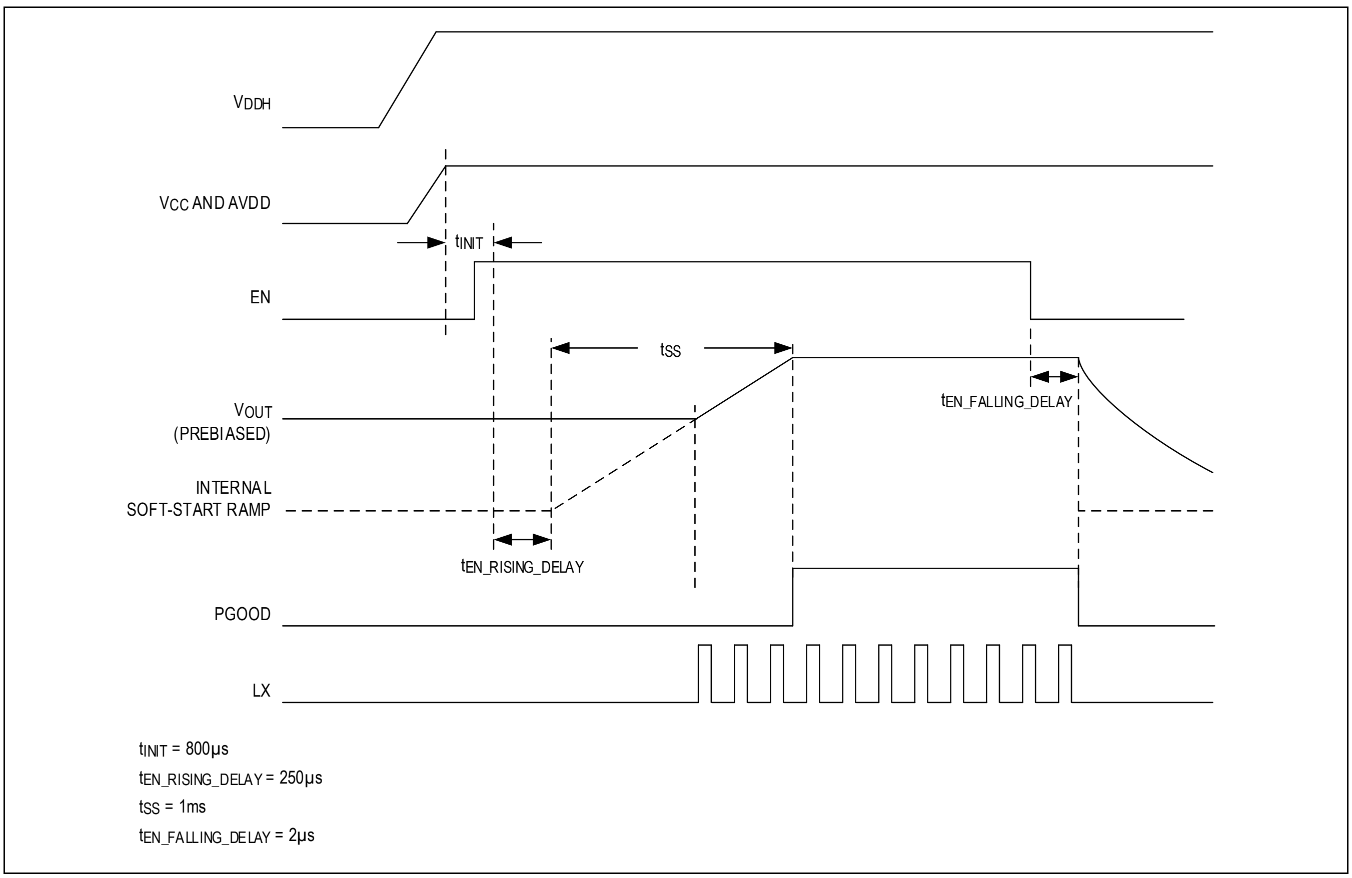


Figure 3. Startup and Shutdown Timing

Fault Handling

Input Undervoltage Lockout (V_{DDH} UVLO)

The MAX20815 internally monitors the V_{DDH} voltage level. When the input supply voltage is below the UVLO threshold, the device stops switching and drives the PGOOD pin low. The device restarts after 20ms if the UVLO status is cleared. See the *Startup and Shutdown* section for the startup sequence.

Output Overvoltage Protection (OVP)

The feedback voltage of $V_{SNSP} – V_{SNSN}$ is monitored for output overvoltage once the soft-start ramp is complete. If the feedback voltage is above the OVP threshold beyond the OVP deglitch filtering delay, the device stops switching and drives PGOOD pin low. The device restarts after 20ms if the OVP status is cleared.

Positive Overcurrent Protection (POCP) and Fast Positive Overcurrent Protection (FPOCP)

The device’s peak current mode control architecture provides inherent current-limiting and short-circuit protection. The inductor current is continuously monitored while switching. The inductor peak current is limit on a cycle-by-cycle basis. In each switching cycle, once the sensed inductor current exceeds the POCP threshold, the device turns off the high-side MOSFET and turns on the low-side MOSFET to allow the inductor current to be discharged by output voltage. An up-down counter is used to accumulate the number of consecutive POCP events for each switching cycle. If the counter exceeds 1024, the device stops switching and drives PGOOD pin low. POCP is a hiccup protection, and the device restarts after 20ms.

The MAX20815 offers four POCP thresholds (20A, 17.3A, 14.6A, and 12A), which can be selected by the PGM0 pin (see the *Pin-Strap Programmability* section). Due to POCP deglitch delay, for a specific application use case, the actual POCP threshold should be higher (see the *Output Inductor Selection* section).

Besides current-limiting POCP, the device also features FPOCP, which is intended to protect against extreme overcurrent conditions including an inductor short or saturation. FPOCP has a threshold of 25.3A. Once the sensed inductor current exceeds the FPOCP threshold, the device stops switching, drives PGOOD pin low, and latches the device. It requires cycling power to clear the latched FPOCP fault and resume operation.

Negative Overcurrent Protection (NOCP)

The device also has NOCP against inductor valley current. The NOCP threshold is -83% of the POCP threshold. In each switching cycle, once the sensed inductor current exceeds the NOCP threshold, the device turns off the low-side MOSFET and turns on the high-side MOSFET for a fixed 180ns time to allow the inductor current to be charged by input voltage. As with POCP, an up-down counter is used to accumulate the number of consecutive NOCP events. If the counter exceeds 1024, the device stops switching and drives PGOOD pin low. NOCP is a hiccup protection, and the device restarts after 20ms.

Bootstrap Voltage Undervoltage (BST UVLO)

A 0.47μF capacitor is required to be connected between the BST pin and the LX pin. The BST-to-LX differential voltage holds the gate drive supply for the high-side MOSFET. Once this voltage falls below the BST UVLO threshold, the device stops switching and drives the PGOOD pin low. The device restarts after 20ms if the BST UVLO status is cleared.

Overtemperature Protection (OTP)

The overtemperature protection threshold is +155°C with 20°C hysteresis. If the junction temperature reaches the OTP threshold during operation, the device stops switching and drives the PGOOD pin low. The device restarts after 20ms if the OTP status is cleared.

Pin-Strap Programmability

The MAX20815 has two program pins (PGM0 and PGM1) to set some of the key configurations of the device. The PGM_ values are read during startup initialization. PGM0 and PGM1 each have 32 detection levels. A pin-strap resistor is connected from the PGM_ pin to AGND to select one of the 32 codes. PGM0 is used to select the POCP level and PMBus address (see *Table 1*). PGM1 is used to select the switching frequency (*Table 2*) and a predefined scenario, which is defined in *Table 3*.

Table 1. PGM0 POCP and PMBus Address Selections

PGM0 CODES	R_{PGM0} (Ω)	POCP (A)	PMBus ADDRESS
0	95.3	20	0x38h
1	200		0x39h
2	309		0x3Ah
3	422		0x3Bh
4	536		0x3Ch
5	649		0x3Dh
6	768		0x3Eh
7	909		0x3Fh
8	1050	17.3	0x38h
9	1210		0x39h
10	1400		0x3Ah
11	1620		0x3Bh
12	1870		0x3Ch
13	2150		0x3Dh
14	2490		0x3Eh
15	2870		0x3Fh
16	3740	14.6	0x38h
17	8060		0x39h
18	12400		0x3Ah
19	16900		0x3Bh
20	21500		0x3Ch
21	26100		0x3Dh
22	30900		0x3Eh
23	36500		0x3Fh
24	42200	12	0x38h
25	48700		0x39h
26	56200		0x3Ah
27	64900		0x3Bh
28	75000		0x3Ch
29	86600		0x3Dh
30	100000		0x3Eh
31	115000		0x3Fh

Table 2. PGM1 Switching Frequency and Scenario Selection

PGM1 CODES	R_{PGM1} (Ω)	SWITCHING FREQUENCY (kHz)	SCENARIO #
0	95.3	500	A
1	200		B
2	309		C
3	422		D
4	536		E
5	649		F
6	768	600	A
7	909		B
8	1050		C
9	1210		D
10	1400		E
11	1620		F
12	1870	750	A
13	2150		B

14	2490		C
15	2870		D
16	3740		E
17	8060		F
18	12400	1000	A
19	16900		B
20	21500		C
21	26100		D
22	30900		E
23	36500		F
24	42200	1200	A
25	48700		B
26	56200		C
27	64900		D
28	75000		E
29	86600		F
30	100000	2000	A
31	115000		B

The MAX20815 has six predefined scenarios, as summarized in *Table 3*, which can be selected by a pin-strap resistor connected from the PGM1 pin to AGND. See the *Voltage Loop Gain* section for information about how to select the voltage loop gain resistance (R_{VGA}) for optimized control loop performance. For each scenario, the AMS option can also be selected.

Table 3. Predefined Scenarios

SCENARIO #	R_{VGA} (kΩ)	AMS OPTION
A	15.7	Disabled
B	22.7	Disabled
C	15.7	Enabled
D	22.7	Enabled
E	31.3	Enabled
F	44.8	Enabled

Besides the pin-strap selectable configurations and predefined scenarios, more device configurations can be selected using the PMBus manufacturer-specific device operating configurations commands (refer to the *UG2175: MAX20815 PMBus Command Set User Guide*).

PMBus Interface

PMBus is an industry standard that defines a means of communication with power conversion devices. It is composed of an industry-standard SMBus serial interface and the PMBus command language. The MAX20815 supports a PMBus interface in order to communicate with a host device. The device PMBus address is selected by a pin-strap resistor connected from the PGM0 pin to AGND (see the *Pin-Strap Programmability* section. *Table 4* shows the supported PMBus commands. For the detailed PMBus command definition and additional information, refer to the *UG2175: MAX20815 PMBus Command Set User Guide*.

Table 4. Supported PMBus Commands

COMMAND CODE	COMMAND NAME	DESCRIPTION	TYPE	DATA FORMAT	FACTORY VALUE
0x01	OPERATION	Output enable/disable	R/W Byte	Bit field	0x80
0x02	ON_OFF_CONFIG	EN pin and PMBus OPERATION command setting	R/W Byte	Bit field	0x1F
0x03	CLEAR_FAULTS	Clear any fault bits that have been set	Send Byte	N/A	N/A
0x10	WRITE_PROTECT	Level of protection provided by the device against accidental changes	R/W Byte	Bit field	0x20
0x19	CAPABILITY	Summary of PMBus optional communication protocols supported by this device	R Byte	Bit field	0xA0
0x20	VOUT_MODE	Output voltage data format and mantissa exponent	R Byte	Bit field	0x17
0x21	VOUT_COMMAND	Feedback reference voltage setpoint	R/W Word	ULINEAR16	0x0100
0x24	VOUT_MAX	Upper limit of reference voltage setpoint	R/W Word	ULINEAR16	0x019A
0x78	STATUS_BYTE	One byte summary of the unit's fault condition	R Byte	Bit field	N/A
0x79	STATUS_WORD	Two bytes summary of the unit's fault condition	R Word	Bit field	N/A
0x7A	STATUS_VOUT	Output voltage fault and warning status	R Byte	Bit field	N/A
0x7B	STATUS_IOUT	Output current fault and warning status	R Byte	Bit field	N/A
0x7C	STATUS_INPUT	Input voltage fault and warning status	R Byte	Bit field	N/A
0x7D	STATUS_TEMPERATURE	IC junction temperature fault and warning status	R Byte	Bit field	N/A
0x7E	STATUS_CML	Communication fault and warning status	R Byte	Bit field	N/A
0x80	STATUS_MFR_SPECIFIC	Manufacturer-specific fault and warning status	R Byte	Bit field	N/A
0x88	READ_VIN	Input voltage telemetry	R Word	LINEAR11	N/A
0x8B	READ_VOUT	Feedback voltage telemetry	R Word	ULINEAR16	N/A
0x8C	READ_IOUT	Output current telemetry	R Word	LINEAR11	N/A
0x8D	READ_TEMPERATURE_1	IC junction temperature telemetry	R Word	LINEAR11	N/A
0xAD	IC_DEVICE_ID	Device root part number	R Block	ASCII	"MAX20815"
0xAE	IC_DEVICE_REV	Device revision code	R Block	ASCII	N/A
0xD0	MFR_PINSTRAP	Manufacturer-specific device operating configurations	R/W Byte	Bit field	N/A
0xD1	MFR_SCENARIO_0	Manufacturer-specific device operating configurations	R/W Byte	Bit field	N/A
0xD2	MFR_SCENARIO_1	Manufacturer-specific device operating configurations	R/W Byte	Bit field	N/A
0xD3	MFR_SCENARIO_2	Manufacturer-specific device operating configurations	R/W Byte	Bit field	N/A

Reference Design Procedure

Output Voltage Sensing

The MAX20815 has a default 0.5V feedback reference voltage (V_{REF}). The reference voltage can be adjusted by the PMBus VOUT_COMMAND from 0.4V to 0.8V with 1.95mV resolution (refer to the *UG2175: MAX20815 PMBus Command Set User Guide*). When the desired output voltage is higher than V_{REF}, it is required to use a resistor-divider (R_{FB1} and R_{FB2}) to sense the output voltage (see the *Simplified Application Circuit*). It is recommended that the value of R_{FB2} does not exceed 5kΩ. The resistor-divider ratio is given by the following equation:

$$V_{OUT} = V_{REF} \times \left(1 + \frac{R_{FB1}}{R_{FB2}}\right)$$

where:

V_{OUT} = Output voltage

V_{REF} = Reference voltage

R_{FB1} = Top resistor-divider

R_{FB2} = Bottom resistor-divider

Switching Frequency Selection

The MAX20815 offers a wide range of selectable switching frequencies from 500kHz to 2MHz. The selection of switching frequency can be optimized for different applications. Higher switching frequencies are recommended for applications prioritizing solution size, so that the value and size of output LC filter can be reduced. Lower switching frequencies are recommended for applications prioritizing efficiency and thermal dissipation, due to reduced switching losses. It is required that the frequency be selected so that the minimum controllable on-time and minimum controllable off-time are not violated. The maximum recommended switching frequency is calculated by the following equation:

$$f_{SW(MAX)} = \mathrm{MIN}\left\{\frac{V_{OUT}}{t_{ON(MIN)} \times V_{DDH(MAX)}}, \frac{V_{DDH(MIN)} - V_{OUT}}{t_{OFF(MIN)} \times V_{DDH(MIN)}}\right\}$$

where:

$f_{SW(MAX)}$ = Maximum selectable switching frequency

$V_{DDH(MAX)}$ = Maximum input voltage

$V_{DDH(MIN)}$ = Minimum input voltage

$t_{ON(MIN)}$ = Minimum controllable on-time

$t_{OFF(MIN)}$ = Minimum controllable off-time

The MAX20815 internally has a slope compensation applied to the current loop during on-time to guarantee stability and improve noise immunity. To avoid the slope compensation saturating the current loop, it is required that the maximum on-time be limited by:

$$t_{ON(MAX)} = \frac{5\mathrm{pF}\left[800\mathrm{mV} - \left(I_{OUT(MAX)} + \frac{I_{RIPPLE}}{2}\right) \times \frac{1.6\Omega}{62.5}\right]}{I_{SLOPE}}$$

where:

$t_{ON(MAX)}$ = Maximum on-time of the high-side MOSFET

$I_{OUT(MAX)}$ = Maximum load current

I_{RIPPLE} = Inductor current ripple peak-to-peak value

I_{SLOPE} = Internal slope compensation amplitude. The default value is 3.78μA and the value can be adjusted by the PMBus MFR_SCENARIO_0 command (refer to the *UG2175: MAX20815 PMBus Command Set User Guide*).

The minimum recommended switching frequency is calculated by the following equation:

$$f_{SW(MIN)} = \frac{V_{OUT}}{t_{ON(MAX)} \times V_{DDH(MIN)}}$$

where:

$f_{SW(MIN)}$ = Minimum selectable switching frequency

Due to system noise injection, even at steady-state operation, typically the LX rising and falling edges would have some random jittering noise. The selection of the switching frequency f_{SW} should consider the jittering and be higher than $f_{SW(MIN)}$ and lower than $f_{SW(MAX)}$. To improve the LX jittering, use smaller inductor values and lower voltage loop gain to minimize the noise sensitivity.

Output Inductor Selection

The output inductor has an important influence on the overall size, cost, and efficiency of the voltage regulator. Since the inductor is typically one of the larger components in the system, a minimum inductor value is particularly important in space-constrained applications. Smaller inductor values also permit faster transient response, reducing the amount of output capacitance needed to maintain transient tolerance. Typically, the output inductor is selected so that the inductor current ripple is 20% to 40% of the maximum load current for optimized performance. To improve current loop noise immunity, it is recommended that the inductor current ripple is at least 2A.The inductor value is calculated by the following equation:

$$L = \frac{V_{OUT}(V_{DDH} - V_{OUT})}{V_{DDH} \times I_{RIPPLE} \times f_{SW}}$$

where:

V_{DDH} = Input voltage

I_{RIPPLE} = Inductor current ripple peak-to-peak value

The inductor should also be selected so that maximum load current delivery can be guaranteed by the selected POCP threshold. The MAX20815 offers four POCP thresholds (20A, 17.3A, 14.6A, and 12A), which can be selected by the PGM0 pin (see the *Pin-Strap Programmability* section). Due to the deglitch delay from the POCP comparator tripping to the high-side MOSFET turning off, for a specific application use case, the adjusted POCP threshold should take into consideration the inductor value, input voltage, and output voltage, which can be calculated by the following equation:

$$POCP_{ADJUST} = POCP + \frac{(V_{DDH} - V_{OUT}) \times t_{POCP}}{L}$$

where：

$POCP_{ADJUST}$ = Adjusted POCP threshold

POCP = POCP level specified in the *Electrical Characteristics* table

t_{POCP} = POCP deglitch delay (40ns, typ)

Verify that the peak inductor current in normal operation does not exceed the minimum adjusted POCP threshold:

$$I_{OUT(MAX)} + \frac{I_{RIPPLE}}{2} < POCP_{ADJUST(MIN)}$$

where:

$POCP_{ADJUST(MIN)}$ = Minimum adjusted POCP threshold, calculated with the minimum value of the POCP threshold

Table 5 shows some suitable inductor part numbers, which are verified on the MAX20815 evaluation kit to offer optimal performance.

Table 5. Recommended Inductors

COMPANY	VALUE (nH)	I_{SAT} (A)	R_{DC} (mΩ)	FOOTPRINT (mm)	HEIGHT (mm)	PART NUMBER
Eaton	220	58	0.17	10.8 × 8.0	8.0	FP1008R5-R220-R
Eaton	270	44	0.17	10.8 × 8.0	8.0	FP1008R5-R270-R
Pulse	330	40	0.4	10.0 × 7.0	10.0	PA5034.331HLT
Pulse	470	30	0.4	10.0 × 7.0	10.0	PA5034.471HLT
Pulse	1000	20.5	0.81	10.0 × 7.0	10.0	PA4987.102HLT

Output Capacitor Selection

One major factor in determining the total required output capacitance is the output voltage ripple. To meet the output voltage ripple requirement, the minimum output capacitance should satisfy the following equation:

$$C_{OUT} \geq \frac{I_{RIPPLE}}{8 \times f_{SW} \times (V_{OUTRIPPLE} - ESR \times I_{RIPPLE})}$$

where:

$V_{OUTRIPPLE}$ = Maximum allowed output voltage ripple

ESR = ESR of output capacitors

The other important factors in determining the total required output capacitance are the maximum allowable output voltage overshoot and undershoot during load transients. For a given loading or unloading current step, the minimum required output capacitance should also satisfy the following equation:

$$C_{OUT} \geq MAX\left\{\frac{\left(\Delta I + \frac{I_{RIPPLE}}{2}\right)^2 \times L}{2 \times \Delta V_{OUT} \times (V_{DDH} - V_{OUT})}, \frac{\left(\Delta I + \frac{I_{RIPPLE}}{2}\right)^2 \times L}{2 \times \Delta V_{OUT} \times V_{OUT}}\right\}$$

where:

C_{OUT} = Output capacitance

$\triangle I$ = Loading or unloading current step

$\triangle V_{OUT}$ = Maximum allowed output voltage undershoot or overshoot

Input Capacitor Selection

The selection of input capacitance is determined by the requirement of input voltage ripple. The minimum required input capacitance is estimated by the following equation:

$$C_{IN} \geq \frac{I_{OUT(MAX)} \times V_{OUT}}{f_{SW} \times V_{DDH} \times V_{INPP}}$$

where:

V_{INPP} = Peak-to-peak input voltage ripple

Besides the minimum required input capacitance, it is recommended to also place 0.1μF and a 1μF high-frequency decoupling capacitors next to the V_{DDH} pin to suppress the high-frequency switching noises.

Voltage Loop Gain

For stability purposes, it is recommended that the voltage loop bandwidth (BW) be lower than 1/5 of the switching frequency. Consider the case of using MLCC output capacitors that have nearly ideal impedance characteristics in the frequency range of interest with negligible ESR and ESL. The voltage loop BW can be estimated by the following equation:

$$BW = \frac{\frac{R_{FB2}}{R_{FB2} + R_{FB1}} \times \frac{R_{VGA}}{10k\Omega}}{2\pi \times 8m\Omega \times C_{OUT}}$$

where:

R_{VGA} = Voltage loop gain resistance, which is set by the scenario selected (see *Table 3*)

Typical Reference Designs

Refer to the *Typical Application Circuits* for examples of reference schematics. Reference design examples for some common output voltages are shown in *Table 6*.

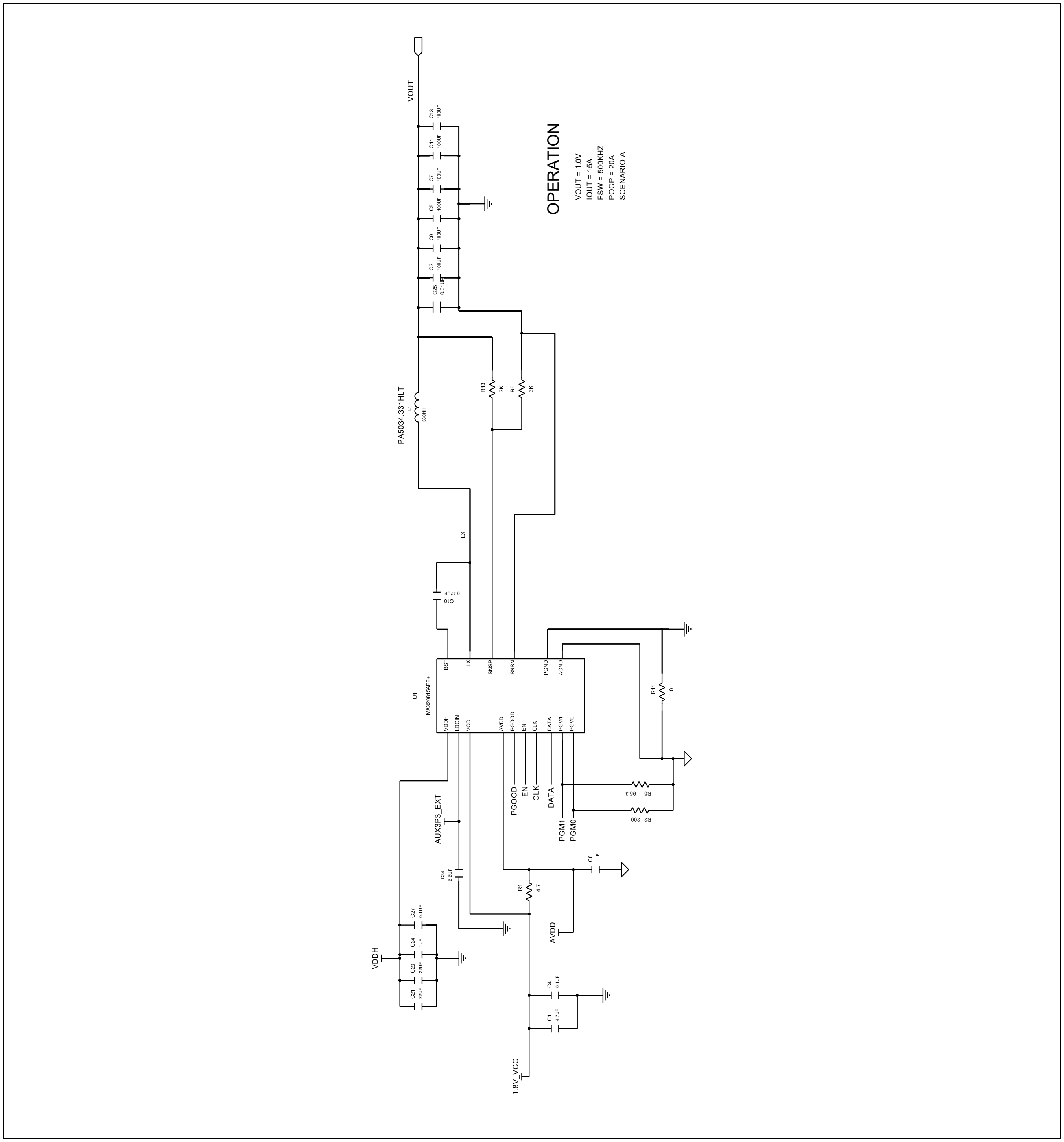
Table 6. Reference Design Examples

V_{OUT} (V)	I_{OUT} (A)	f_{SW} (kHz)	R_{FB1} (kΩ)	R_{FB2} (kΩ)	PGM0 (Ω)	PGM1 (Ω)	L (nH)	C_{IN}	C_{OUT}
0.8	15	750	1.82	3.01	95.3	2150	330	2 × 10μF +1μF +0.1μF	6 × 100μF
0.9	15	750	2.40	3.01	95.3	2150	330	2 × 10μF +1μF +0.1μF	6 × 100μF
1.0	15	750	3.01	3.01	95.3	2150	330	2 × 10μF +1μF +0.1μF	6 × 100μF
1.2	15	750	4.22	3.01	95.3	2150	470	2 × 10μF +1μF +0.1μF	6 × 100μF
1.8	12	1000	7.87	3.01	1050	16900	470	2 × 10μF +1μF +0.1μF	5 × 100μF
3.3	10	1200	16.9	3.01	3740	48700	1000	2 × 10μF +1μF +0.1μF	5 × 100μF
5.0	8	2000	22.6	2.49	42200	115000	1000	2 × 10μF +1μF +0.1μF	5 × 47μF

PCB Layout Guidelines

- For electrical and thermal reasons, the second layer from the top and bottom of the PCB should be reserved for power ground (PGND) planes.
- The input decoupling capacitor should be located the closest to the IC and no more than 40mils from the V_{DDH} pin.
- The V_{CC} decoupling capacitors should be connected to PGND and placed as close as possible to the V_{CC} pin.
- An analog ground copper polygon or island should be used to connect all analog control-signal grounds. This "quiet" analog ground copper polygon or island should be connected to PGND through a single connection close to AGND. The analog ground can be used as a shield and ground reference for the control signals.
- The AVDD decoupling capacitors should be connected to AGND and placed as close as possible to the AVDD pin.
- The boost capacitors should be placed as close as possible to the LX and BST pins, on the same side of the PCB with the IC.
- The feedback resistor-divider and optional external compensation network should be placed close to the IC to minimize noise injection.
- Output voltage should be sensed with differential remote sense lines routed directly from an output capacitor from the load point, shielded by ground plane, and kept away from the switching node and inductor.
- Multiple vias are recommended for all paths that carry high currents and for heat dissipation.
- The input capacitors and output inductors should be placed near the IC, and the traces to the components should be kept as short and wide as possible to minimize parasitic inductance and resistance.

Typical Application Circuits



Ordering Information

PART NUMBER	TEMP RANGE	PIN-PACKAGE
MAX20815AFE+	-40°C to +125°C	16 FC2QFN
MAX20815AFE+T	-40°C to +125°C	16 FC2QFN

+Denotes a lead(Pb)-free/RoHS-compliant package.

T = Tape and reel.

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	8/23	Initial release.	—
1	7/25	Updated Absolute Maximum Ratings	3
2	9/25	Updated Detailed Description	17, 18