# 6A, 3MHz, 2.7V to 16V, Step-Down Switching Regulator

**MAX20806**

## General Description

The MAX20806 is a fully integrated, highly efficient, step-down DC-DC switching regulator. It is able to operate from 2.7V to 16V input supplies, and the output can be regulated from 0.5V to 5.8V, delivering up to 6A of load current.

The switching frequency of this device can be configured from 500kHz to 3.0MHz and provides the capability of optimizing the design in terms of solution size and performance.

The MAX20806 utilizes fixed-frequency, current-mode control with internal compensation. The MAX20806 features a selectable advanced modulation scheme (AMS) to provide improved dynamic load transient performance. The device also features selectable discontinuous current mode (DCM) operation to improve light load efficiency. Operation settings and configurable features can be selected by connecting pin-strap resistors from the PGM_ pins to ground.

The MAX20806 has an internal 1.8V LDO output to power the gate drives and internal circuitry ($V_{CC}$).

The MAX20806 integrates multiple protections including positive and negative overcurrent protection, output overvoltage protection, and overtemperature protection to ensure a robust design.

The MAX20806 is available in a compact 3.0mm x 2.5mm FC2QFN package that supports -40°C to +150°C junction temperature operation.

## Applications

- Communications Equipment
- Networking Equipment
- Servers and Storage Equipment
- Point-of-Load Voltage Regulators

## Benefits and Features

- High Power Density with Low Component Count
  - Single-Supply Operation with Integrated LDO for Bias Generation
  - Compact 3.0mm x 2.5mm, 14-Pin, FC2QFN Package
  - Internal Compensation
- Wide Operating Range
  - 2.7V to 16V Input Voltage Range
  - 0.5V to 5.8V Output Voltage Range
  - 500kHz to 3MHz Configurable Switching Frequency
  - -40°C to +150°C Junction Temperature Range
  - Two Pin-Strap Programming Pins to Select Different Configurations
- Optimized Performance and Efficiency
  - 91.9% Peak Efficiency with $V_{DDH}$ = 12V, $V_{OUT}$ = 1.8V, and $f_{SW}$ = 1MHz
  - Selectable AMS to Improve Load Transients
  - Selectable DCM to Improve Light Load Efficiency

| DESCRIPTION | CURRENT RATING (A) | INPUT VOLTAGE (V) | OUTPUT VOLTAGE (V) |
|---|---|---|---|
| Electrical Rating | 6 | 2.7 to 16 | 0.5 to 5.8 |
| Thermal Rating $T_A$ = +85°C, No Air Flow | 6 | 12 | 1.8 |
| Thermal Rating $T_A$ = +55°C, 200LFM Air Flow | 6 | 12 | 5.0 |

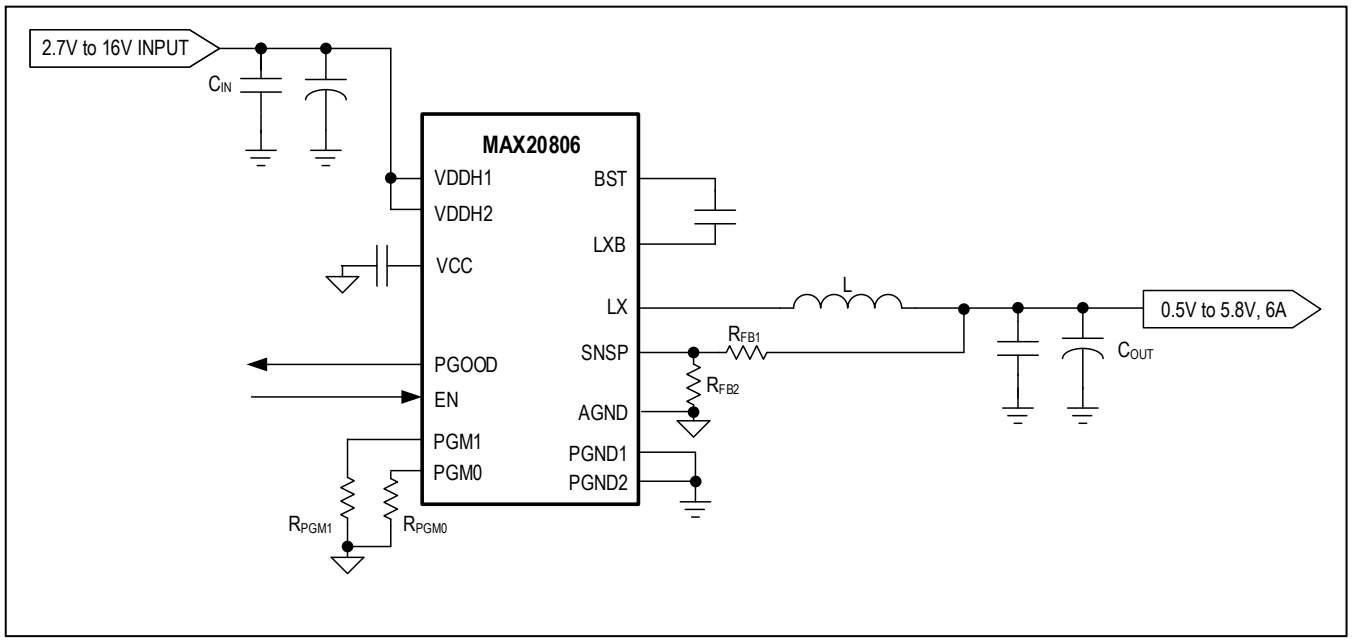
**Maximum $T_J$ = +125°C. For specific operating conditions, see the Safe Operating Area (SOA) curves in the Typical Operating Characteristics.*

***Ordering Information* appears at end of data sheet.**

19-101878; Rev 1; 7/26

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## Simplified Application Circuit



## Absolute Maximum Ratings

$V_{DDH1}$, $V_{DDH2}$ to PGND_ (Note 1) ..... -0.3V to +19V

LX, LXB to PGND_ (DC) ..... -0.3V to +19V

LX, LXB to PGND_ (AC) (Note 2) ..... -10V to +23V

$V_{DDH1}$, $V_{DDH2}$ to LX (DC) (Note 1) ..... -0.3V to +19V

$V_{DDH1}$, $V_{DDH2}$ to LX (AC) (Note 2) ..... -10V to +19V

BST to PGND_ (DC) ..... -0.3V to +21.5V

BST to PGND_ (AC) (Note 2) ..... -7V to +25.5V

BST to LXB ..... -0.3V to +2.5V

LXB to LX ..... -0.3V to +0.3V

PGND_ to AGND ..... -0.3V to +0.3V

$V_{CC}$ to AGND ..... -0.3V to +2.5V

EN to AGND ..... -0.3V to +4V

PGOOD to AGND ..... -0.3V to +4V

SNSP to AGND ..... -0.3V to $V_{CC}$ +0.3V

PGM0, PGM1 to AGND ..... -0.3V to $V_{CC}$ +0.3V

Peak LX Current ..... -12A to +19A

Junction Temperature ($T_J$) (Note 3) ..... +150°C

Storage Temperature Range ..... -65°C to +150°C

Peak Reflow Temperature Lead-Free ..... +260°C

**Note 1:** Input HF capacitors placed not more than 40 mils away from the $V_{DDH_}$ pins are required to keep inductive voltage spikes within Absolute Maximum limits.

**Note 2:** AC is limited to 25ns.

**Note 3:** The MAX20806 is guaranteed over the full -40°C to 150°C operating junction temperature range. High junction temperatures degrade operating lifetimes. Operating lifetime is derated at junction temperatures greater than 125°C. The junction temperature ($T_J$, in °C) is calculated from the ambient temperature ($T_A$, in °C) and power dissipation ($P_D$, in watts) according to the formula:

$T_J = T_A + (P_D \times \theta_{JA})$

where $\theta_{JA}$ (in °C/W) is the package thermal impedance.

*Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

## Package Information

### 14 FC2QFN

| | |
|---|---|
| Package Code | F142A3F+1 |
| Outline Number | *21-100712* |
| Land Pattern Number | *90-100247* |
| **Thermal Resistance** | |
| Junction to Ambient ($\theta_{JA}$) JEDEC | 51.7°C/W |
| Junction to Ambient ($\theta_{JA}$) on MAX20806EVKIT# | 21.0°C/W |
| Junction to Case ($\theta_{JC}$) | 22.6°C/W |

For the latest package outline information and land patterns (footprints), go to *www.analog.com/packages*. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board; the junction to case resistance was obtained using a one-layer board. For detailed information on package thermal considerations, refer to *www.analog.com/thermal-tutorial*.

## Electrical Characteristics

(See the *Typical Application Circuits*. $V_{DDH1}$ = $V_{DDH2}$ = 12V, $T_J$ = -40°C to +150°C, unless otherwise noted. Specifications are production tested at $T_A$ = +32°C; limits within the operating temperature range are guaranteed by design and characterization.)

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|
| **INPUT SUPPLY** | | | | | | |
| Input Voltage Range | $V_{DDH}$ | | 2.7 | | 16 | V |
| Input Supply Current | $I_{VDDH}$ | EN = AGND | | 2 | | mA |
| Internal LDO Regulated Output | $V_{CC}$ | | 1.75 | | 1.95 | V |
| Linear Regulator Current Limit | | | 80 | | | mA |
| | | $V_{CC}$ < 1.6V | | 20 | | |
| $V_{CC}$ Undervoltage Lockout | $V_{CC_UVLO}$ | Rising | 1.65 | 1.67 | 1.74 | V |
| $V_{CC}$ Undervoltage Lockout Hysteresis | | | | 55 | | mV |
| $V_{DDH}$ Undervoltage Lockout | $V_{DDH_UVLO}$ | Rising | 2.4 | 2.5 | 2.6 | V |
| $V_{DDH}$ Undervoltage Lockout Hysteresis | | | | 100 | | mV |
| **OUTPUT VOLTAGE RANGE AND ACCURACY** | | | | | | |
| Feedback Voltage | | $V_{SNSP}$ = 0.5V, $T_J$ = -40°C to +150°C | 0.497 | 0.500 | 0.503 | V |
| Voltage Sense Leakage Current | $I_{SNSP_}$ | $T_J$ = +25°C | -1 | | 1 | µA |
| **SWITCHING FREQUENCY** | | | | | | |
| Switching Frequency | $f_{SW_}$ | | | 500 | | kHz |
| | | | | 750 | | |
| | | | | 1000 | | |
| | | | | 1500 | | |
| | | | | 2000 | | |
| | | | | 3000 | | |
| Switching Frequency Accuracy | | | -10 | | +10 | % |
| Minimum Controllable On-Time | | $I_{OUT}$ = 0A (*Note 4*) | | 24 | 40 | ns |
| | | $I_{OUT}$ = 1A (*Note 4*) | | 22 | 37 | |
| Minimum Controllable Off-Time | | $I_{OUT}$ = 0A (*Note 4*) | | 100 | 110 | ns |
| **ENABLE AND STARTUP** | | | | | | |
| Initialization Time | $t_{INIT}$ | | | 800 | | µs |
| EN Threshold | | Rising | 0.9 | | | V |
| | | Falling | | | 0.6 | |
| EN Filtering Delay | $t_{EN_RISING_DELAY}$ | Rising | | 200 | | µs |
| | $t_{EN_FALLING_DELAY}$ | Falling | | 2 | | |
| EN Leakage | $I_{EN}$ | EN = 0V | | | 250 | nA |
| | | EN = 1.85V | | | 2 | µA |
| | | EN = 4V | | 3.5 | 8 | |

(See the *Typical Application Circuits*. $V_{DDH1}$ = $V_{DDH2}$ = 12V, $T_J$ = -40°C to +150°C, unless otherwise noted. Specifications are production tested at $T_A$ = +32°C; limits within the operating temperature range are guaranteed by design and characterization.)

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|
| Soft-Start Time | $t_{SS}$ | | | 3 | | ms |
| **POWER-GOOD AND FAULT PROTECTIONS** | | | | | | |
| PGOOD Output Low | | $I_{PGOOD}$ = 4mA | | | 0.4 | V |
| PGOOD Leakage | $I_{PGOOD}$ | PGOOD = 3.6V | | 0.01 | 1 | µA |
| Output Undervoltage (UV) Threshold | | | -16 | -13 | -10 | % |
| Output UV Deglitch Delay | | | | 4 | | µs |
| Output Overvoltage Protection (OVP) Threshold | | | 10 | 13 | 16 | % |
| Output OVP Threshold Deglitch Delay | | | | 2 | | µs |
| Positive Overcurrent Protection (POCP) Threshold | POCP | Inductor peak current, POCP = 9A | 8.0 | 9.0 | 10.0 | A |
| | | Inductor peak current, POCP = 6.2A | 5.5 | 6.2 | 6.9 | |
| POCP Deglitch Delay | | | | 36 | | ns |
| Fast Positive Overcurrent Protection (FPOCP) Threshold | FPOCP | | 12.5 | 14.5 | 16.5 | A |
| Negative Overcurrent Protection (NOCP) Threshold to POCP Threshold Ratio | NOCP | With respect to POCP threshold (typ) | | -83 | | % |
| NOCP Accuracy | | | -20 | | +20 | % |
| BST UVLO Threshold | $V_{BST}$ | Rising | 1.47 | 1.59 | 1.66 | V |
| | | Falling | 1.41 | 1.53 | 1.6 | |
| Overtemperature Protection (OTP) Rising Threshold | OTP | (*Note 5*) | | 176 | | °C |
| OTP Accuracy | | | | 6 | | % |
| OTP Hysteresis | | | | 20 | | °C |
| Hiccup Protection Time | $t_{HICCUP}$ | | | 20 | | ms |
| **DCM OPERATION MODE** | | | | | | |
| DCM Comparator Threshold to Enter DCM | | POCP=9A, Inductor Valley Current | | -440 | | mA |
| | | POCP=6.2A, Inductor Valley Current | | -340 | | |
| DCM Comparator Threshold to Exit DCM | | Inductor Valley Current | | 100 | | mA |
| **PROGRAMMING PINS** | | | | | | |
| PGM_ Pin Resistor Range | $R_{PGM_}$ | *Note 6* | 0.095 | | 115 | kΩ |
| PGM_ Resistor Accuracy | | Not Guaranteed Above $T_J$ = 125°C | -1 | | +1 | % |

**Note 4:** Guaranteed by design.

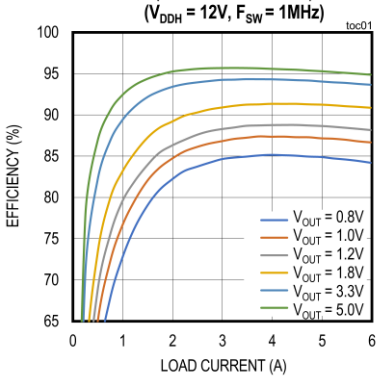
**Note 5:** This IC includes overtemperature protection that is intended to protect the device during overload conditions. Junction temperature will exceed 150°C temperature when overtemperature protection is active. Continuous operation above the specified maximum operating junction temperature will reduce lifetime.

**Note 6:** PGM_ Pin Resistor value is read during startup initialization and the detection is guaranteed below 125°C temperature.

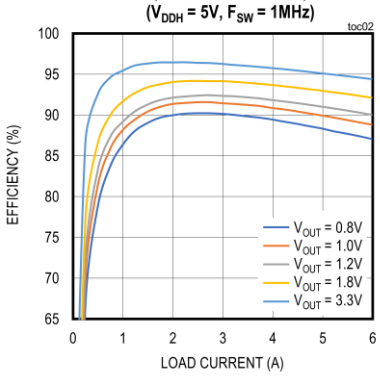
## Typical Operating Characteristics

(Typical Application Circuits, $V_{DDH}$ = 12V, $f_{SW}$ = 1MHz, tested on MAX20806EVKIT#, $T_A$ = +25°C, unless otherwise noted.)

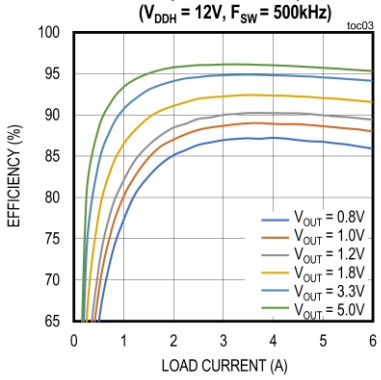
EFFICIENCY
(L = PA5003.XXXNLT)
($V_{DDH}$ = 12V, $F_{SW}$ = 1MHz)



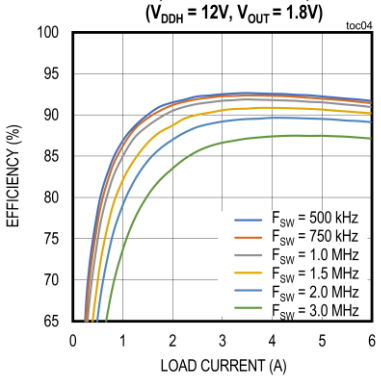

EFFICIENCY
(L = PA5003.XXXNLT)
($V_{DDH}$ = 5V, $F_{SW}$ = 1MHz)



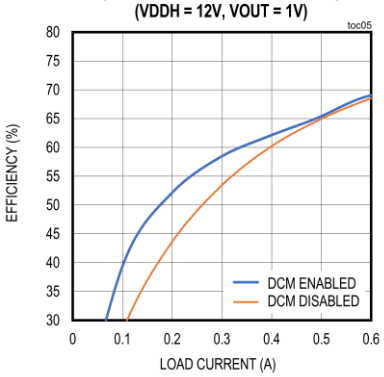

EFFICIENCY
(PA5005.XXXNLT)
($V_{DDH}$ = 12V, $F_{SW}$ = 500kHz)



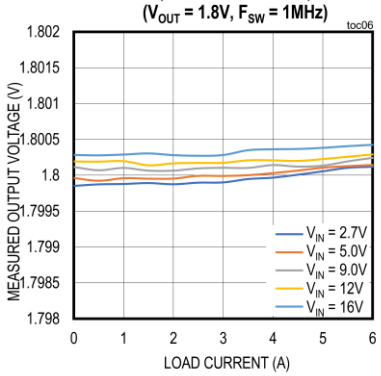

EFFICIENCY
(L = PA5005.152NLT)
($V_{DDH}$ = 12V, $V_{OUT}$ = 1.8V)



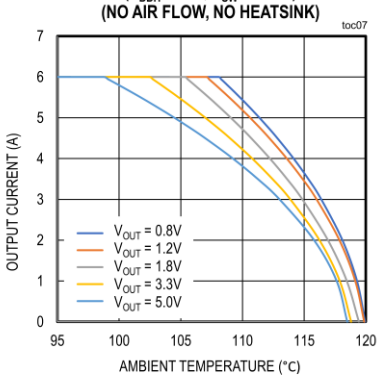

EFFICIENCY
(DCM vs CCM, L = PA5003.471NLT)
(VDDH = 12V, VOUT = 1V)



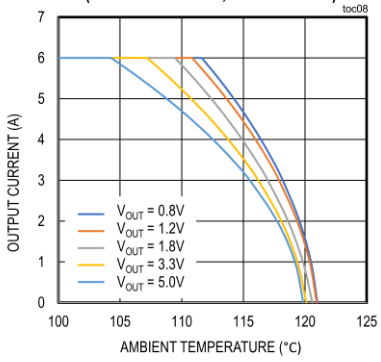

LOAD AND LINE REGULATIONS
(L = PA5003.821NLT)
($V_{OUT}$ = 1.8V, $F_{SW}$ = 1MHz)



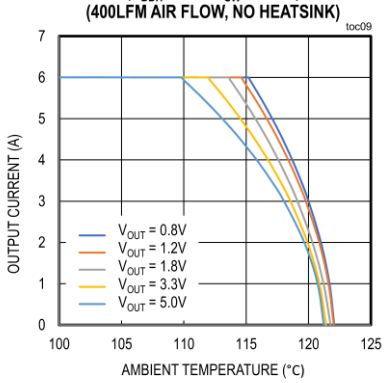

SAFE OPERATING AREA
($V_{DDH}$ = 12V, $F_{SW}$ = 1MHz)
(NO AIR FLOW, NO HEATSINK)



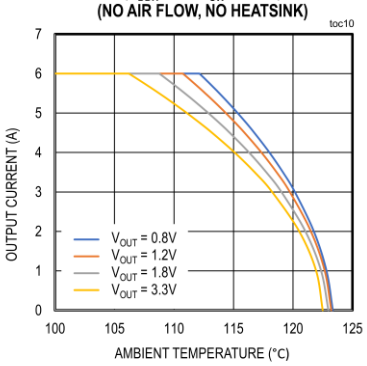

SAFE OPERATING AREA
($V_{DDH}$ = 12V, $F_{SW}$ = 1MHz)
(200LFM AIR FLOW, NO HEATSINK)



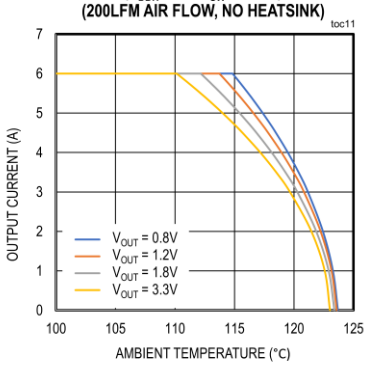

SAFE OPERATING AREA
($V_{DDH}$ = 12V, $F_{SW}$ = 1MHz)
(400LFM AIR FLOW, NO HEATSINK)



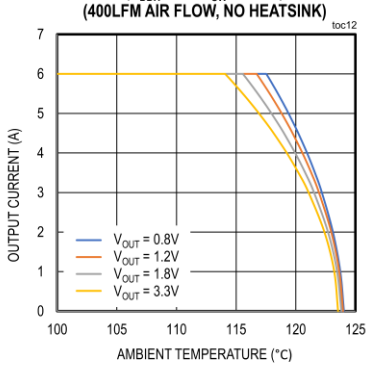
SAFE OPERATING AREA
($V_{DDH}$ = 5V, $F_{SW}$ = 1MHz)
(NO AIR FLOW, NO HEATSINK)



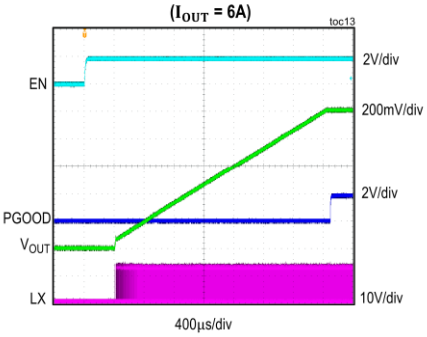

SAFE OPERATING AREA
($V_{DDH}$ = 5V, $F_{SW}$ = 1MHz)
(200LFM AIR FLOW, NO HEATSINK)



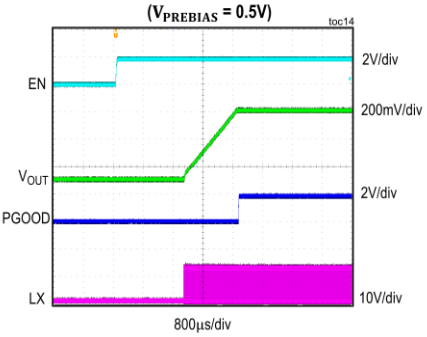

SAFE OPERATING AREA
($V_{DDH}$ = 5V, $F_{SW}$ = 1MHz)
(400LFM AIR FLOW, NO HEATSINK)



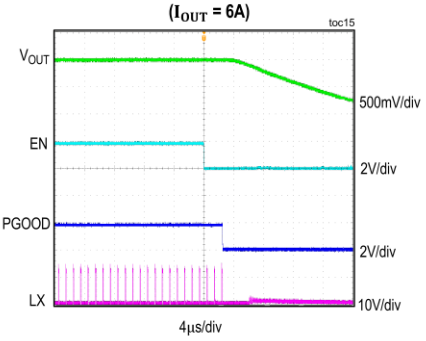

STARTUP
($I_{OUT}$ = 6A)



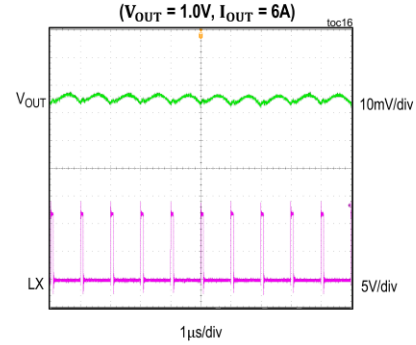

PRE-BIASED STARTUP
($V_{PREBIAS}$ = 0.5V)



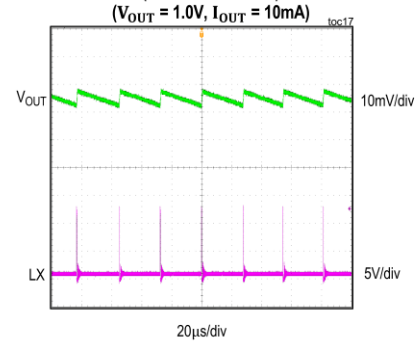

SHUTDOWN
($I_{OUT}$ = 6A)



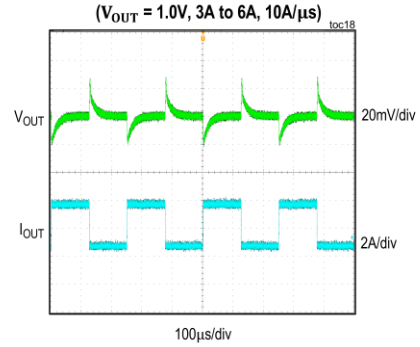

OUTPUT VOLTAGE RIPPLE
($V_{OUT}$ = 1.0V, $I_{OUT}$ = 6A)

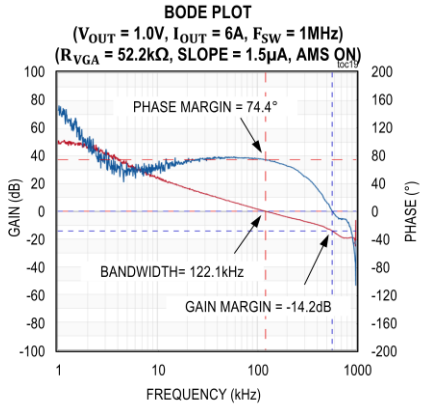


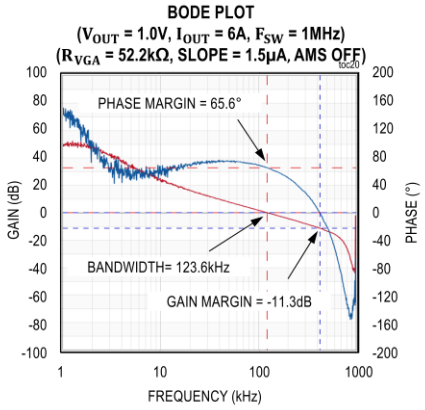

OUTPUT VOLTAGE RIPPLE
(DCM OPERATION)
($V_{OUT}$ = 1.0V, $I_{OUT}$ = 10mA)

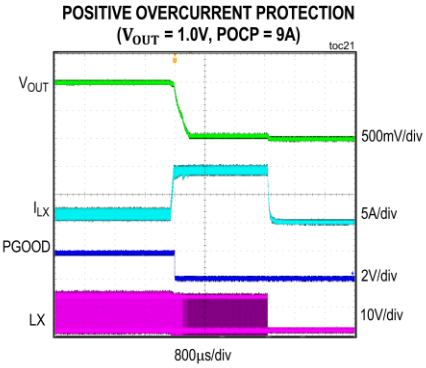


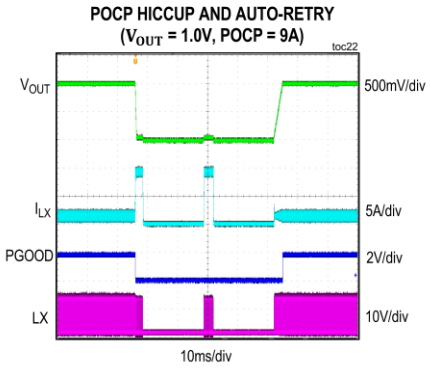

LOAD TRANSIENT RESPONSE
($V_{OUT}$ = 1.0V, 3A to 6A, 10A/µs)



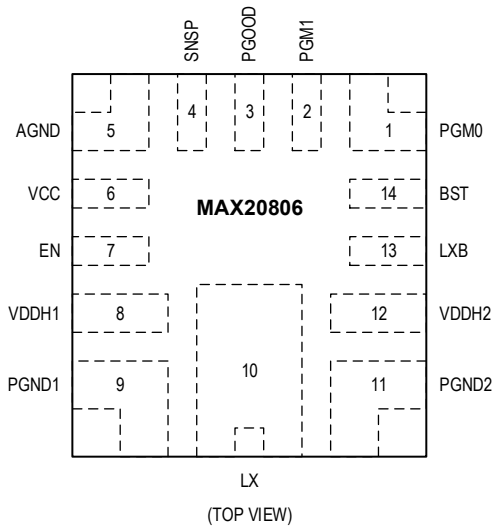

BODE PLOT
($V_{OUT}$ = 1.0V, $I_{OUT}$ = 6A, $F_{SW}$ = 1MHz)
($R_{VGA}$ = 52.2kΩ, SLOPE = 1.5µA, AMS ON)
toc19
PHASE MARGIN = 74.4°
BANDWIDTH= 122.1kHz
GAIN MARGIN = -14.2dB
GAIN (dB)
PHASE (°)
FREQUENCY (kHz)


BODE PLOT
($V_{OUT}$ = 1.0V, $I_{OUT}$ = 6A, $F_{SW}$ = 1MHz)
($R_{VGA}$ = 52.2kΩ, SLOPE = 1.5µA, AMS OFF)
toc20
PHASE MARGIN = 65.6°
BANDWIDTH= 123.6kHz
GAIN MARGIN = -11.3dB
GAIN (dB)
PHASE (°)
FREQUENCY (kHz)


POSITIVE OVERCURRENT PROTECTION
($V_{OUT}$ = 1.0V, POCP = 9A)
toc21
$V_{OUT}$
500mV/div
$I_{LX}$
5A/div
PGOOD
2V/div
LX
10V/div
800µs/div


POCP HICCUP AND AUTO-RETRY
($V_{OUT}$ = 1.0V, POCP = 9A)
toc22
$V_{OUT}$
500mV/div
$I_{LX}$
5A/div
PGOOD
2V/div
LX
10V/div
10ms/div

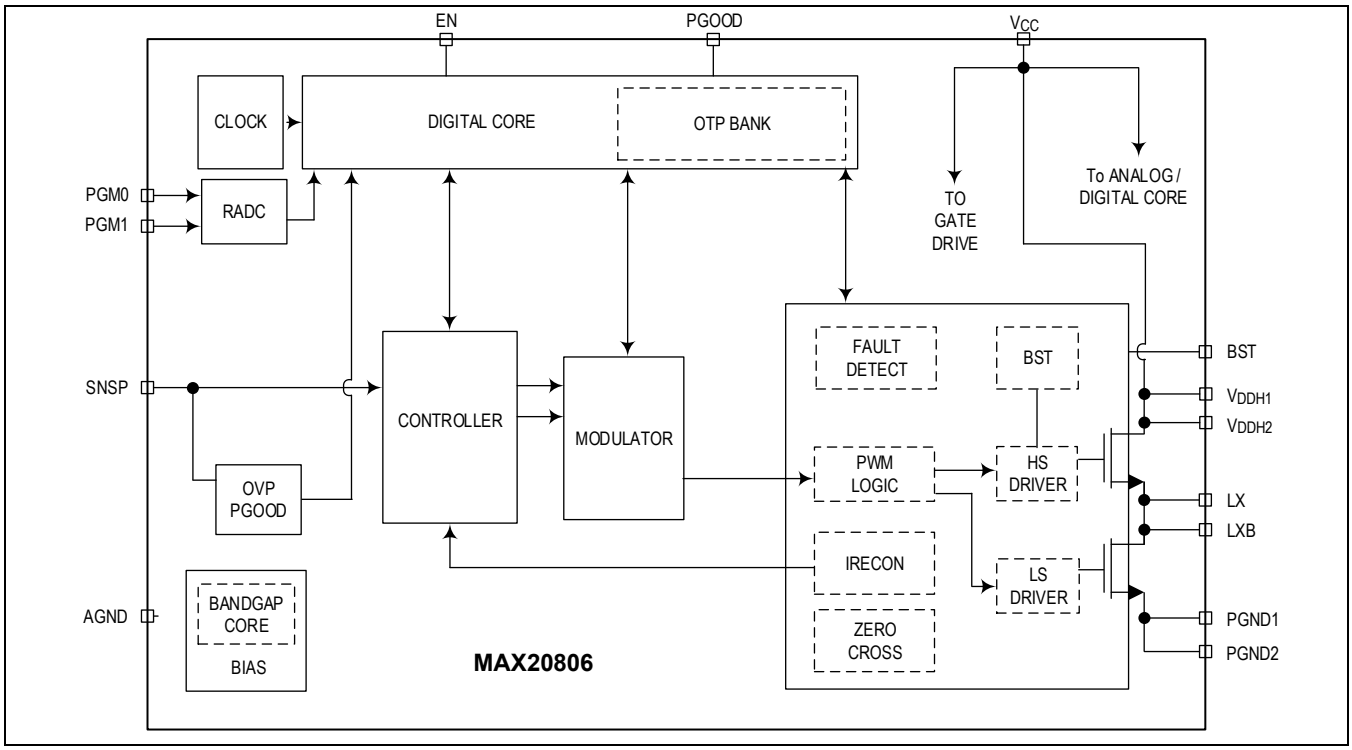
## Pin Configurations




## Pin Descriptions

| PIN | NAME | FUNCTION |
|---|---|---|
| 1 | PGM0 | Program Input. Connect this pin to ground through a programming resistor. |
| 2 | PGM1 | Program Input. Connect this pin to ground through a programming resistor. |
| 3 | PGOOD | Open-Drain Power-Good Output. |
| 4 | SNSP | Output Voltage Sense Feedback Pin. Connect SNSP to VOUT at the load. A resistive voltage-divider can be inserted between the output and SNSP to regulate the output above the 0.5V fixed reference voltage. |
| 5 | AGND | Analog Ground. |
| 6 | $V_{CC}$ | Internal 1.8V LDO Output. Connect a 2.2µF or greater ceramic capacitor from $V_{CC}$ to AGND. |
| 7 | EN | Output Enable. |
| 8 | $V_{DDH1}$ | Regulator Input Supply. $V_{DDH1}$ and $V_{DDH2}$ should be connected on the PCB. |
| 9 | PGND1 | Power Ground. PGND1 and PGND2 should be connected on the PCB. |
| 10 | LX | Switching Node. Connect LX directly to the output inductor. |
| 11 | PGND2 | Power Ground. PGND1 and PGND2 should be connected on the PCB. |
| 12 | $V_{DDH2}$ | Regulator Input Supply. $V_{DDH1}$ and $V_{DDH2}$ should be connected on the PCB. |
| 13 | LXB | Switching Node for bootstrap capacitor connection. LXB and LX are connected internally. |
| 14 | BST | Bootstrap Pin. Connect a 0.22µF ceramic capacitor from BST to LXB. |

## Functional Diagrams



# Detailed Description

## Control Architecture

The MAX20806 control loop is based on fixed-frequency, peak current-mode control architecture. A simplified control architecture is shown in *Figure 1*. The loop contains an error amplifier stage, internal voltage loop compensation network, current sense, internal slope compensation, and a PWM modulator that generates the pulse-width modulation (PWM) signals to drive high-side and low-side MOSFETs. The device has a fixed 0.5V reference voltage ($V_{REF}$). The difference of $V_{REF}$ and the sensed output voltage is amplified by the first error amplifier. Its output voltage ($V_{ERR}$) is used as the input of the voltage loop compensation network. The output of the compensation network ($V_{COMP}$) is fed to a PWM comparator with the current-sense signal ($V_{ISENSE}$) and slope compensation ($V_{RAMP}$). The output of the PWM comparator is the input of the PWM modulator. The turning on of the high-side MOSFET is aligned with an internal clock. It can either be a fixed-frequency clock or a phase-shifted clock if AMS is enabled.

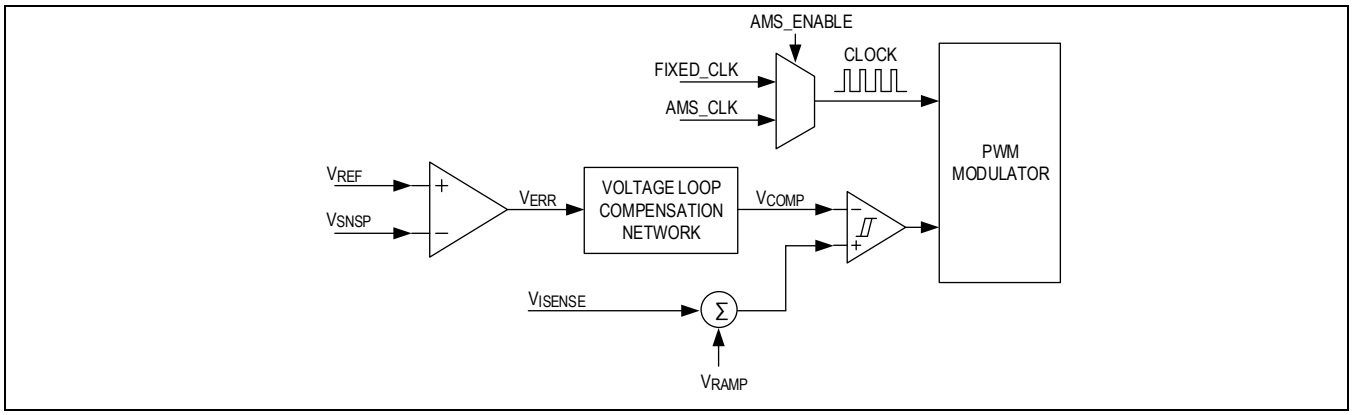



*Figure 1. Simplified Control Architecture*

## Advanced Modulation Scheme (AMS)

The MAX20806 offers a selectable advanced modulation scheme (AMS) to provide improved transient response. AMS provides significant advantage over conventional fixed-frequency PWM schemes. Enabling the AMS feature allows for modulation at both leading and trailing edges, which result a temporary increase or decrease of the switching frequency during large load transients. *Figure 2* shows the scheme to include leading-edge modulation to the traditional trailing-edge modulation when AMS is enabled in the device. The modulation scheme allows the turn on and off with minimal delay. Because the total inductor current increases very quickly, satisfying the load demand, the current drawn from output capacitors is reduced. With AMS enabled, the system closed-loop bandwidth can be extended without phase-margin penalty. As a result, the output capacitance can be minimized.

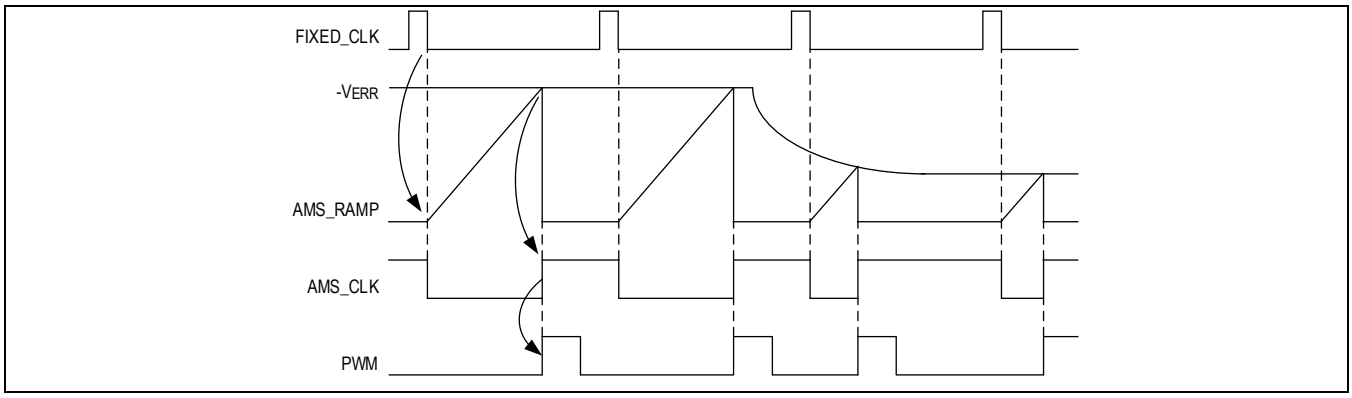



*Figure 2. AMS Operation*

### Discontinuous Current Mode (DCM) Operation

Discontinuous current mode (DCM) operation is an optional feature to improve light load efficiency. It is required that $V_{DDH}$ is at least 2V higher than the desired $V_{out}$ for the device to operate in DCM. The device has a DCM current detection comparator to monitor the inductor valley current while operating in CCM. At light load, if the inductor valley current is below the DCM comparator threshold for at least 48 consecutive cycles, the device transition seamlessly to DCM. Once in DCM, the switching frequency decreases as load decreases. The device will transition back to CCM operation as soon as the inductor valley current is higher than 100mA.

### Internal Linear Regulator

The device contains an internal 1.8V linear regulator (LDO). The 1.8V LDO output voltage on $V_{CC}$ is derived from $V_{DDH_}$ pin by default.

The 1.8V voltage on $V_{CC}$ pin supplies the current to the MOSFET drivers. A decoupling capacitor of at least 2.2µF must be connected between $V_{CC}$ and AGND.

## Startup and Shutdown

The startup and shutdown timing are shown in *Figure 3*. When Vcc pin voltage is above its rising UVLO threshold, the device goes through an initialization procedure. Configuration settings on PGM_ pins are read. Once initialization is complete, the device detects $V_{DDH}$ UVLO and EN status. When both are above their rising thresholds, the soft-start begins and switching is enabled. The output voltage of the enabled output starts to ramp up. The soft-start ramp time is 3ms. If there are no faults, the open drain PGOOD pin is released from being held low after the soft-start ramp is complete. The device supports smooth startup with output pre-biased.

During operation, if either $V_{DDH}$ UVLO or EN falls below their thresholds, switching is stopped immediately. The PGOOD pin is driven low. The output voltage is discharged by load current.

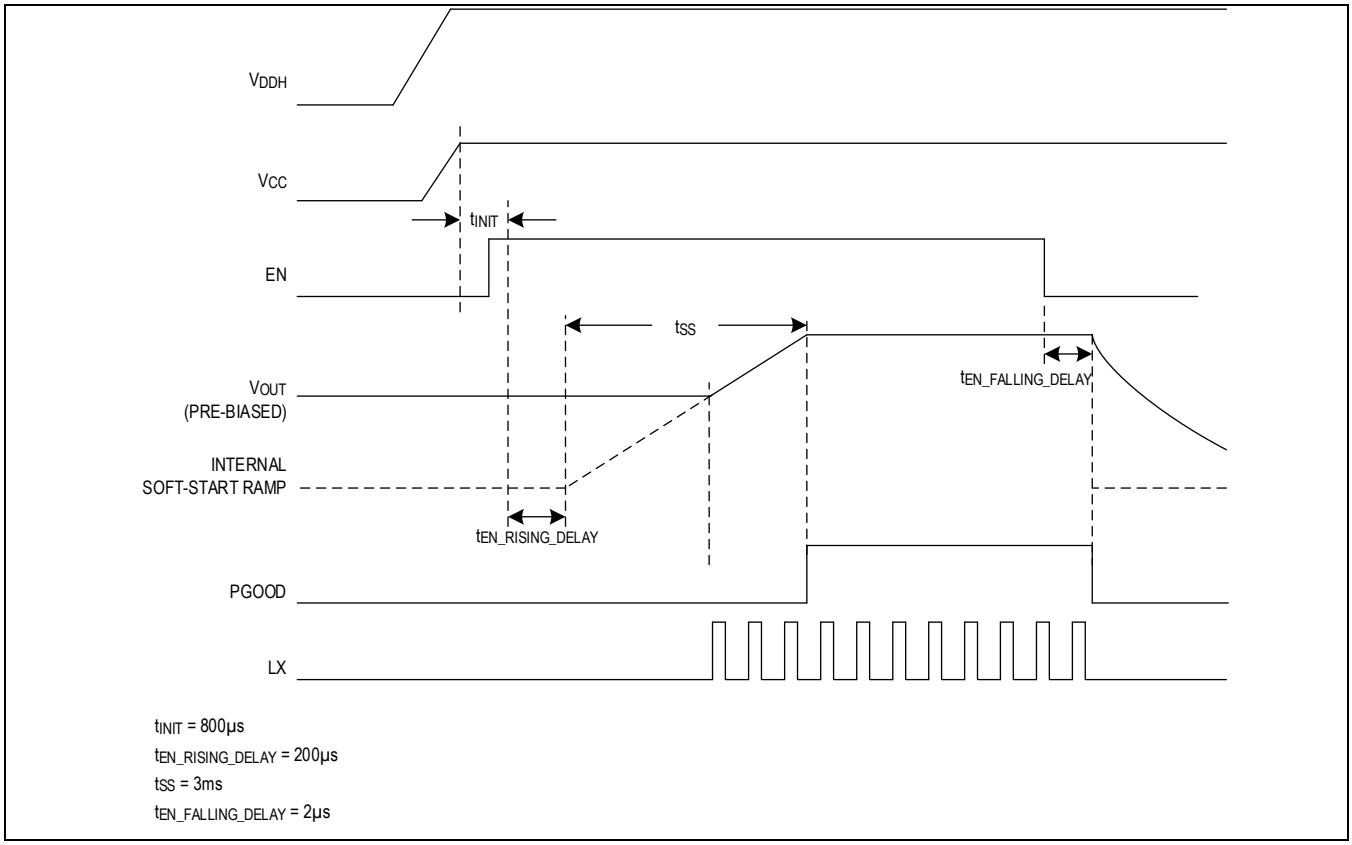



*Figure 3. Startup and Shutdown Timing*

## Fault Handling

### Input Undervoltage Lockout ($V_{DDH}$ UVLO)

The MAX20806 internally monitors the $V_{DDH}$ voltage level. When the input supply voltage is below the UVLO threshold, the device stops switching and drives the PGOOD pin low. The device restarts after 20ms if the UVLO status is cleared. See *Startup and Shutdown* section for startup sequence.

### Output Overvoltage Protection (OVP)

The feedback voltage of $V_{SNSP}$ – AGND is monitored for output overvoltage once the soft-start ramp is complete. If the feedback voltage is above the OVP threshold beyond the OVP deglitch filtering delay, the device stops switching and drives PGOOD pin low. The device restarts after 20ms if the OVP status is cleared.

### Positive Overcurrent Protection (POCP)

The device's peak current mode control architecture provides inherent current limiting and short circuit protection. The inductor current is continuously monitored while switching. The inductor peak current is limit on a cycle-by-cycle basis. In each switching cycle, once the sensed inductor current exceeds the POCP threshold, the device turns off the high-side MOSFET and turns on the low-side MOSFET to allow the inductor current to be discharged by output voltage. An up-down counter is used to accumulate the number of consecutive POCP events each switching cycle. If the counter exceeds 1024, the device stops switching and drives PGOOD pin low. POCP is a hiccup protection and the device restarts after 20ms.

MAX20806 offers 2 POCP thresholds (9A and 6.2A), which can be selected by PGM1 pin (see *Pin-Strap Programmability*). Due to POCP deglitch delay, for a specific application use case, the actual POCP threshold should be higher (see *Output Inductor Selection*).

### Negative Overcurrent Protection (NOCP)

The device also has negative overcurrent protection against inductor valley current. The NOCP threshold is -83% of the POCP threshold. In each switching cycle, once the sensed inductor current exceeds the NOCP threshold, the device turns off the low-side MOSFET and turns on the high-side MOSFET for a fixed 180ns time to allow the inductor current to be charged by input voltage. Same as POCP, an up-down counter is used to accumulate the number of consecutive NOCP events. If the counter exceeds 1024, the device stops switching and drives PGOOD pin low. NOCP is a hiccup protection and the device restarts after 20ms.

### Overtemperature Protection (OTP)

The overtemperature protection threshold is +176°C with 20°C hysteresis. If the junction temperature reaches OTP threshold during operation, the device stops switching and drives PGOOD pin low. The device restarts after 20ms if the OTP status is cleared.

## Pin-Strap Programmability

MAX20806 has two program pins (PGM0 and PGM1) to set some of the key configurations of the device. The PGM_ values are read during startup initialization and the detection is guaranteed below 125°C temperature. PGM0 has 18 detection levels, and PGM1 has 32 detection levels. A pin-strap resistor is connected from PGM_ pin to AGND to select one of the codes. See the *Internal Compensation Selection* section for information about how to select the compensation parameters for optimized control loop performance.

## Table 1. PGM0 Switching Frequency, AMS, and DCM Selections

| PGM0 CODES | $R_{PGM0}$ (Ω) | AMS | DCM | $f_{SW}$ (kHz) |
|---|---|---|---|---|
| 0 | 95.3 | Disable | Disable | 500 |
| 1 | 309 | | | 750 |
| 2 | 649 | | | 1000 |
| 3 | 909 | | | 1500 |
| 4 | 1210 | | | 2000 |
| 5 | 1620 | | | 3000 |
| 6 | 2150 | Enable | | 500 |
| 7 | 2490 | | | 750 |
| 8 | 8060 | | | 1000 |
| 9 | 16900 | | | 1500 |

| | | | | |
|---|---|---|---|---|
| 10 | 26100 | | | 2000 |
| 11 | 36500 | | | 3000 |
| 12 | 42200 | | Enable | 500 |
| 13 | 56200 | | | 750 |
| 14 | 75000 | | | 1000 |
| 15 | 86600 | | | 1500 |
| 16 | 100000 | | | 2000 |
| 17 | 115000 | | | 3000 |

## Table 2. PGM1 Configurations for POCP and Control Loop Selections

| PGM1 CODES | $R_{PGM1}$ (Ω) | POCP | VOLTAGE LOOP GAIN MULTIPLIER | SLOPE (µA) |
|---|---|---|---|---|
| 0 | 95.3 | 9 | 0.4 | 1.5 |
| 1 | 200 | | | 2.6 |
| 2 | 309 | | | 3.7 |
| 3 | 422 | | | 6.0 |
| 4 | 536 | | | 7.0 |
| 5 | 649 | | | 8.0 |
| 6 | 768 | | 0.7 | 1.5 |
| 7 | 909 | | | 2.6 |
| 8 | 1050 | | | 3.7 |
| 9 | 1210 | | | 6.0 |
| 10 | 1400 | | | 7.0 |
| 11 | 1620 | | | 8.0 |
| 12 | 1870 | | 1 | 1.5 |
| 13 | 2150 | | | 2.6 |
| 14 | 2490 | | | 3.7 |
| 15 | 2870 | | | 6.0 |
| 16 | 3740 | | | 7.0 |
| 17 | 8060 | | | 8.0 |
| 18 | 12400 | | 1.5 | 1.5 |
| 19 | 16900 | | | 2.6 |
| 20 | 21500 | | | 3.7 |
| 21 | 26100 | | | 6.0 |
| 22 | 30900 | | | 7.0 |
| 23 | 36500 | 6.2 | 0.4 | 1.5 |
| 24 | 42200 | | | 2.6 |
| 25 | 48700 | | | 7.0 |
| 26 | 56200 | | 0.7 | 1.5 |
| 27 | 64900 | | | 2.6 |
| 28 | 75000 | | | 7.0 |
| 29 | 86600 | | 1 | 1.5 |
| 30 | 100000 | | | 2.6 |
| 31 | 115000 | | | 7.0 |

## Reference Design Procedure

### Output Voltage Sensing

The MAX20806 has an internal 0.5V reference voltage. When the desired output voltage is higher than 0.5V, it is required to use resistor-dividers $R_{FB1}$ and $R_{FB2}$ to sense the output voltage (see *Simplified Application Circuit*). It is recommended that the value $R_{FB2}$ does not exceed 5kΩ. The resistor-divider ratio is given by the following equation:

$$V_{OUT} = V_{REF} \times \left(1 + \frac{R_{FB1}}{R_{FB2}}\right)$$

where:

$V_{OUT}$ = Output voltage

$V_{REF}$ = 0.5V fixed reference voltage

$R_{FB1}$ = Top resistor-divider

$R_{FB2}$ = Bottom resistor-divider

### Switching Frequency Selection

The MAX20806 offers a wide range of selectable switching frequencies from 500kHz to 3MHz. The selection of switching frequencies can be optimized for different applications. Higher switching frequencies are recommended for applications prioritizing solution size so that the value and size of output LC filter can be reduced. Lower switching frequencies are recommended for applications prioritizing efficiency and thermal dissipation due to reduced switching losses. The frequency must be selected so that the minimum controllable on-time and minimum controllable off-time are not violated. The maximum recommended switching frequency is calculated by the following equation:

$$f_{SWMAX} = MIN\left\{\frac{V_{OUT}}{t_{ONMIN} \times V_{DDHMAX}}, \frac{V_{DDHMIN} - V_{OUT}}{t_{OFFMIN} \times V_{DDHMIN}}\right\}$$

where:

$f_{SWMAX}$ = Maximum selectable switching frequency

$V_{DDHMAX}$ = Maximum input voltage

$V_{DDHMIN}$ = Minimum input voltage

$t_{ONMIN}$ = Minimum controllable on-time

$t_{OFFMIN}$ = Minimum controllable off-time

Due to system noise injection, even at steady-state operation, typically the LX rising and falling edges would have some random jittering noise. The selection of the switching frequency ($f_{SW}$) should take into consideration the jittering and be lower than $f_{SWMAX}$. To improve the LX jittering, it is recommended to use smaller inductor values and lower voltage loop gain to minimize the noise sensitivity.

### Output Inductor Selection

The output inductor has an important influence on the overall size, cost, and efficiency of the voltage regulator. Since the inductor is typically one of the larger components in the system, a minimum inductor value is particularly important in space-constrained applications. Smaller inductor values also permit faster transient response, reducing the amount of output capacitance needed to maintain transient tolerance.

To improve current loop noise immunity, typically the output inductor is selected so that the inductor current ripple is at least 1A. The inductor value is calculated by the following equation:

$$L = \frac{V_{OUT}(V_{DDH} - V_{OUT})}{V_{DDH} \times I_{RIPPLE} \times f_{SW}}$$

where:

$V_{DDH}$ = Input voltage

$I_{RIPPLE}$ = Inductor current ripple peak-to-peak value

The inductor should also be selected so that maximum load current delivery can be guaranteed by the selected POCP threshold. The MAX20806 offer two POCP thresholds (9A and 6.2A), which can be selected by the PGM1 pin (see *Pin-Strap Programmability*). Due to deglitch delay from the POCP comparator tripping to the high-side MOSFET turning off for a specific application use case, the adjusted POCP threshold should take into consideration the inductor value, input voltage, and output voltage, which can be calculated by the following equation:

$$POCP_{ADJUST} = POCP + \frac{(V_{DDH} - V_{OUT}) \times t_{POCP}}{L}$$

where:

$POCP_{ADJUST}$ = Adjusted POCP threshold

POCP = POCP level specified in the *Electrical Characteristics* table

$t_{POCP}$ = POCP deglitch delay (36ns, typ)

It needs to be verified that the peak inductor current in normal operation does not exceed the minimum adjusted POCP threshold:

$$I_{OUTMAX} + \frac{I_{RIPPLE}}{2} < POCP_{ADJUST(MIN)}$$

where:

$I_{OUTMAX}$ = Maximum load current

$POCP_{ADJUST(MIN)}$ = Minimum adjusted POCP threshold, calculated with the minimum value of the POCP threshold

*Table 3* shows some suitable inductor part numbers which are verified on the MAX20806 evaluation (EV) kit to offer optimal performance.

## Table 3. Recommended Inductors

| COMPANY | VALUE (µH) | $I_{SAT}$ (A) | $R_{DC}$ (mΩ) | FOOTPRINT (mm) | HEIGHT (mm) | PART NUMBER |
|---|---|---|---|---|---|---|
| TDK | 0.22 | 9 | 8 | 2.5 x 2.0 | 1.2 | TFM252012ALMAR22MTAA |
| TDK | 0.33 | 8.4 | 10 | 3.2 x 2.5 | 1.2 | TFM322512ALMAR33MTAA |
| Pulse | 0.47 | 26 | 3.75 | 5.5 x 5.3 | 2.9 | PA5003.471NLT |
| Pulse | 0.56 | 22.2 | 4.05 | 5.5 x 5.3 | 2.9 | PA5003.561NLT |
| Pulse | 1.0 | 16.5 | 6.9 | 5.5 x 5.3 | 2.9 | PA5003.102NLT |
| Pulse | 2.2 | 10 | 13.2 | 5.5 x 5.3 | 2.9 | PA5003.222NLT |

### Output Capacitor Selection

One major factor in determining the total required output capacitance is the output-voltage ripple. To meet the output-voltage ripple requirement, the minimum output capacitance should satisfy the following equation:

$$C_{OUT} \geq \frac{I_{RIPPLE}}{8 \times f_{SW} \times (V_{OUTRIPPLE} - ESR \times I_{RIPPLE})}$$

where:

$V_{OUTRIPPLE}$ = Maximum allowed output-voltage ripple

ESR = ESR of output capacitors

The other important factors in determining the total required output capacitance are the maximum allowable output voltage overshoot and undershoot during load transients. For a given loading or unloading current step, the minimum required output capacitance can be estimated by the following equation:

$$C_{OUT} \geq MAX\left\{\frac{\left(\Delta I + \frac{I_{RIPPLE}}{2}\right)^2 \times L}{2 \times \Delta V_{OUT} \times (V_{DDH} - V_{OUT})}, \frac{\left(\Delta I + \frac{I_{RIPPLE}}{2}\right)^2 \times L}{2 \times \Delta V_{OUT} \times V_{OUT}}\right\}$$

where:

$C_{OUT}$ = Output capacitance

$\triangle I$ = Loading or unloading current step

$\triangle V_{OUT}$ = Maximum allowed output voltage undershoot or overshoot

### Input Capacitor Selection

The input capacitance selection is determined by the input voltage ripple requirement. The $V_{DDH1}$ and $V_{DDH2}$ pins of the MAX20806 should be connected on the PCB. The minimum required input capacitance is estimated by the following equation:

$$C_{IN} \geq \frac{I_{OUT(MAX)} \times V_{OUT}}{f_{SW} \times V_{DDH} \times V_{INPP}}$$

where:

$C_{IN}$ = Input capacitance

$I_{OUT(MAX)}$ = Maximum output current

$V_{OUT}$ = Output voltage

$f_{SW}$ = Switching frequency

$V_{INPP}$ = Peak-to-peak input voltage ripple

Besides the minimum required input capacitance, it is also recommended to place 0.1µF high-frequency decoupling capacitors next to each $V_{DDH_}$ pin to suppress the high-frequency switching noises.

### Internal Compensation Selection

#### Voltage Loop Gain

For stability purposes, it is recommended that the voltage loop bandwidth (BW) be lower than 1/5 of the switching frequency. Consider the case of using MLCC output capacitors that have nearly ideal impedance characteristics in the frequency range of interest with negligible ESR and ESL. The voltage loop BW can be estimated using the following equation:

$$BW = \frac{\frac{R_{FB2}}{R_{FB2} + R_{FB1}} \times \frac{R_{VGA}}{10k\Omega}}{2\pi \times 20m\Omega \times C_{OUT}}$$

where:

$R_{VGA}$ = The voltage loop gain resistance, which is set by the switching frequency and voltage loop gain multiplier selected by PGM1 resistors (*Table 4*)

## Table 4. Voltage Loop Gain Resistance

| SWITCHING FREQUENCY (kHz) | VOLTAGE LOOP GAIN MULTIPLIER | $R_{VGA}$ (kΩ) |
|---|---|---|
| 500 | 0.4 | 15.6 |
| | 0.7 | 27 |
| | 1 | 37 |
| | 1.5 | 52.2 |
| 750 | 0.4 | 22 |
| | 0.7 | 31 |

| | | |
|---|---|---|
| | 1 | 44.5 |
| | 1.5 | 62.3 |
| 1000 | 0.4 | 22 |
| | 0.7 | 37 |
| | 1 | 52.2 |
| | 1.5 | 74.5 |
| 1500 | 0.4 | 27 |
| | 0.7 | 44.5 |
| | 1 | 62.3 |
| | 1.5 | 104.4 |
| 2000 or 3000 | 0.4 | 31 |
| | 0.7 | 52.2 |
| | 1 | 74.5 |
| | 1.5 | 104.4 |

### Slope Compensation

Slope compensation is applied to guarantee current loop stability when the duty cycle is higher than 50%. For applications where the duty cycle is smaller than 50%, it is also recommended to apply slope compensation to improve current loop noise immunity. The minimum and maximum slope compensation values are calculated using the following equation:

$$\frac{V_{OUT}}{L} \times C_{SLOPE} \times \frac{1.6\Omega}{25} \leq SLOPE \leq \frac{V_{IN} \times f_{SW} \times C_{SLOPE}}{V_{OUT}} \left[800mV - \left(I_{OUTMAX} + \frac{I_{RIPPLE}}{2}\right) \times \frac{1.6\Omega}{25}\right]$$

where:

$C_{SLOPE}$ = 5pF

The slope-compensation options of the MAX20806 can be selected by resistor values on PGM1. A higher slope value is recommended to help reduce duty cycle jittering and improve stability.

### Voltage Loop Zero Compensation

The value of voltage loop zero compensation for the loop stability is depending on the selected switching frequency done by the pinstrap of PGM0 (*Table 5*). The voltage loop zero compensation value is not able to be changed by the user once the switching frequency is selected.

## Table 5. Voltage Loop Zero Compensation Setting

| SWITCHING FREQUENCY (kHz) | ZERO COMPENSATION (kHz) |
|---|---|
| 500 | 5 |
| 750 | 7.5 |
| 1000 | 8.75 |
| 1500 | 10 |
| 2000 | 12.5 |
| 3000 | 17.5 |

## Typical Reference Designs

See the *Typical Application Circuits* section for examples of reference schematics. Reference design examples for some common output voltages are shown in *Table 6*.

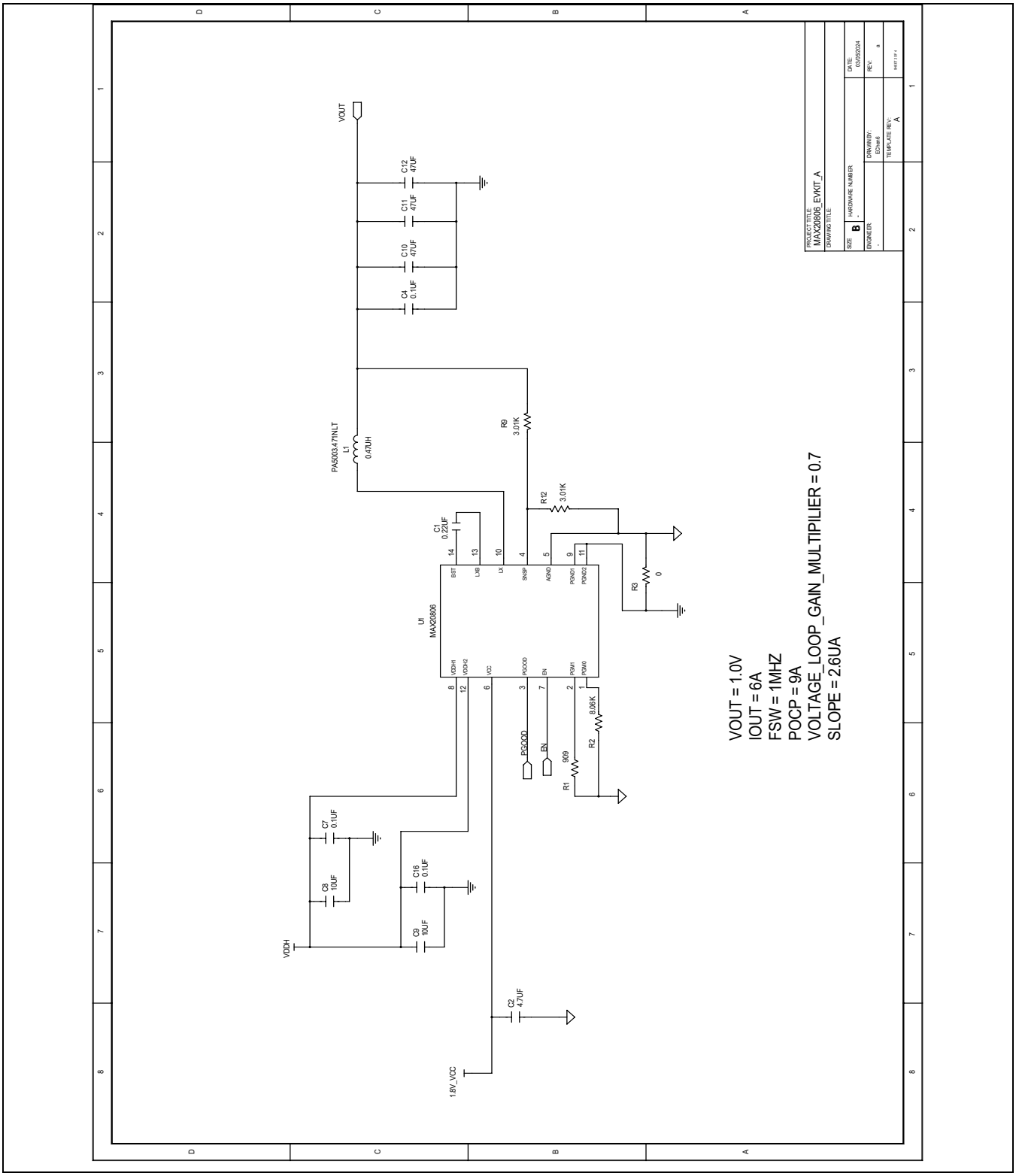
## Table 6. Reference Design Examples

| $V_{OUT}$ (V) | $I_{OUT}$ (A) | $f_{SW}$ (kHz) | $R_{FB1}$ (kΩ) | $R_{FB2}$ (kΩ) | PGM0 (kΩ) | PGM1 (kΩ) | L (µH) | $C_{IN}$ | $C_{OUT}$ |
|---|---|---|---|---|---|---|---|---|---|
| 0.8 | 6 | 750 | 1.82 | 3.01 | 2.49 | 2.49 | 0.47 | 2x10uF+2x0.1uF | 3x47uF |
| 0.9 | 6 | 1000 | 2.40 | 3.01 | 8.06 | 2.49 | 0.47 | 2x10uF+2x0.1uF | 3x47uF |
| 1.0 | 6 | 1000 | 3.01 | 3.01 | 8.06 | 2.49 | 0.47 | 2x10uF+2x0.1uF | 3x47uF |
| 1.2 | 6 | 1000 | 4.22 | 3.01 | 8.06 | 2.49 | 0.56 | 2x10uF+2x0.1uF | 3x47uF |
| 1.8 | 6 | 1500 | 7.87 | 3.01 | 16.9 | 2.49 | 0.56 | 2x10uF+2x0.1uF | 2x47uF |
| 3.3 | 5 | 2000 | 16.9 | 3.01 | 26.1 | 2.15 | 1.0 | 2x10uF+2x0.1uF | 2x47uF |
| 5.0 | 4 | 2000 | 22.6 | 2.49 | 26.1 | 100 | 2.2 | 2x10uF+2x0.1uF | 1x47uF |

### PCB Layout Guidelines

- For electrical and thermal reasons, the second layer from the top and bottom of the PCB should be reserved for power ground (PGND) planes.
- $V_{DDH_}$, PGND_, and LX traces must be as wide as possible to reduce trace impedance and improve heat dissipation.
- The high frequency input decoupling capacitor should be placed on the same side of the PCB as the IC, located the closest to the IC and no more than 40 mils from the $V_{DDH_}$ pins. The remaining ceramic input capacitors can be placed next to these high frequency bypass capacitors. These remaining ceramic input capacitors can also be placed on the other side of the PCB but use as many vias as possible to minimize impedance between the capacitors and the pins of the IC.
- Use vias near both $V_{DDH}$ pins and provide a low impedance connection between them through an internal layer.
- The $V_{CC}$ decoupling capacitors should be connected to AGND and placed as close as possible to $V_{CC}$ pin.
- An analog ground copper polygon or island should be used to connect all analog control-signal grounds. This “quiet” analog ground copper polygon or island should be connected to the PGND through a single connection close to the AGND pin. The analog ground can be used as a shield and ground reference for the control signals.
- Do not place vias between $V_{CC}$ capacitors and AGND pin. These vias will conduct switching currents between the $V_{CC}$ capacitors and PGND. Placing the vias near the AGND pin can add noise to the SNSP divider.
- The boost capacitor should be placed as close as possible to LXB and BST pins on the same side of the PCB as the IC.
- The feedback resistor-divider and optional external compensation network should be placed close to the IC to minimize the noise injection.
- The voltage sense line should be shielded by ground plane and be kept away from switching node and the inductor.
- Multiple vias are recommended for all paths that carry high currents and for heat dissipation.
- The input capacitors and output inductors should be placed near the IC and the traces to the components should be kept as short and wide as possible to minimize parasitic inductance and resistance.

## Typical Application Circuits



## Ordering Information

| PART NUMBER | TEMP RANGE | PIN-PACKAGE |
|---|---|---|
| MAX20806TFD+ | -40°C to +150°C | 14 FC2QFN |
| MAX20806TFD+T | -40°C to +150°C | 14 FC2QFN |

*+ Denotes a lead (Pb)-free/RoHS-compliant package.*
*T = Tape and reel*

## Revision History

| REVISION NUMBER | REVISION DATE | DESCRIPTION | PAGES CHANGED |
|---|---|---|---|
| 0 | 7/24 | Initial release | — |
| 1 | 7/26 | Updated Electrical Characteristics global temperature range | 4 |

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