EVALUATION KIT AVAILABLE

MAX20429

Dual 6A, High-Efficiency, Low-Voltage Buck Converter

General Description

The MAX20429 is a high-efficiency, dual switching regulator that delivers up to 6A (peak) load current per output from 0.5V to 1.5875V in 12.5mV steps and 1.6V to 3.8V in 50mV steps. The IC operates from 3V to 5.5V, making it ideal for on-board point-of-load and post-regulation applications. Total output error is less than ±1.0% over load, line, and temperature.

The MAX20429 features fixed-frequency, PWM mode operation with a switching frequency of 2.1MHz or 3.2MHz. High-frequency operation allows for an all-ceramic capacitor design with small external components.

The low-resistance on-chip switches ensure high efficiency at heavy loads while minimizing critical inductances, making the layout a much simpler task with respect to discrete solutions. Following a simple layout and footprint ensures first-pass success in new designs.

The device features MAXQ™ technology, which provides precision transient performance and phase margin. This allows obtaining the maximum power, performance, and precision from the converter over a very wide range of configurations.

The MAX20429 has separate enable inputs and status outputs for each buck converter. The output voltage is preset at the factory to allow customers to achieve ±1% output-voltage accuracy without using expensive 0.1% resistors. The device offers factory-programmable soft-start and $\overline{\text{RESET}}$ times.

The device includes overtemperature shutdown and overcurrent limiting and is designed to operate over the -40°C to +125°C ambient temperature range.

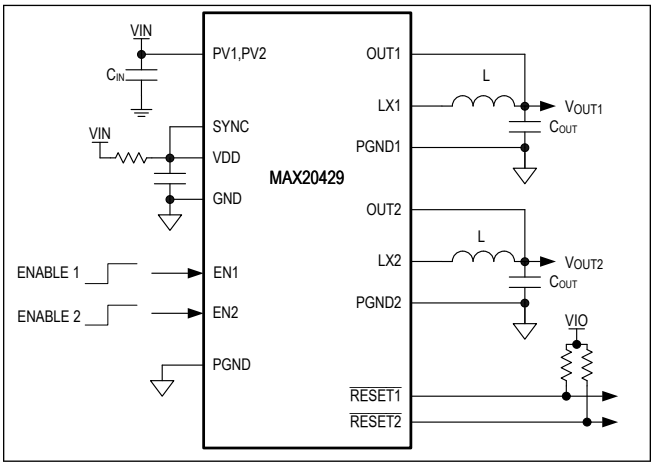
Applications

- Secondary Regulator for SoC/MCU Supply

Benefits and Features

- High-Feature Set in an Ultra-Small Footprint
  - High-Efficiency DC-DC Converter
  - Two Independent Outputs, up to 6A per Output
  - 3.0V to 5.5V Operating Supply Voltage
  - Resistor-Adjustable Output Voltage
  - Optional Factory-Preset Output Voltage
  - 2.1MHz/3.2MHz Options
  - Enable Input
  - Individual $\overline{\text{RESET}}$ Outputs
  - Spread-Spectrum Option
  - Peak Current-Mode Architecture
  - 3mm x 3.5mm FCQFN
- High-Precision
  - 108/92% OV/UV Monitor
  - ±3% UV Accuracy
  - ±4% OV Accuracy
  - ±1% Output Voltage Accuracy
  - Excellent Load-Transient Performance
  - PWM and SKIP Mode Operation
  - MAXQ Power Architecture
- High Efficiency
  - Up to 96% Efficiency 5V to 3.3V
  - Up to 90% Efficiency 5V to 1V
- -40°C to +125°C Operating Temperature Range
- AEC-Q100 Qualified

Simplified Block Diagram



Ordering Information appears at end of data sheet.

19-100842; Rev 2; 5/25

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Absolute Maximum Ratings

PV1, PV2 to GND ..... -0.3V to 6V
V_{DD} to GND..... -0.3V to 6V
OUT1, OUT2 to GND ..... -0.3V to V_{DD}+0.3V
LX1, LX2 to GND..... -0.3 to PV_ + 0.3
EN1, EN2, RESET1, RESET2 to GND ..... -0.3V to 6V
SYNC to GND..... -0.3V to V_{DD}+0.3V
PGND_ to GND ..... -0.3V to +0.3V

Output Short-Circuit Duration.....Continuous
Continuous Power Dissipation (4-Layer Board) (T A = +70°C, derate 51.8 mW/°C above +70°C.) ..... to 4145mW
Ambient Operating Temperature .....-40°C to +125°C
Operating Junction Temperature .....-40°C to +150°C
Storage Temperature Range .....-65°C to +150°C
Lead Temperature Range.....+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Package Information

FCQFN

Package Code	F183A3FY+1
Outline Number	21-100428
Land Pattern Number	90-100155
Thermal Resistance, Four-Layer Board: (Method JEDEC Specification JESD51-7)	
Junction to Ambient (θ_{JA})	39.2°C/W
Junction to Case (θ_{JC})	12.2°C/W
Thermal Resistance, Four-Layer Board: (Simulated on the EV Kit)	
Junction to Ambient (θ_{JA})	19.3°C/W
Junction to Case (θ_{JC})	5.0°C/W

For the latest package outline information and land patterns (footprints), go to *www.analog.com/en/resources/packaging-quality-symbols-footprints/package-index.html*. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

Electrical Characteristics

(PV1 = PV2 = 5V, T_J = -40°C to +150°C, unless otherwise noted. Typical values are at T_A = +25°C under normal conditions unless otherwise noted. (*Note 1*) (*Note 2*))

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
PV Supply Voltage Range	V_{PV}		3.0		5.5	V
Supply Current	I_{VDD}	V_{EN1} = V_{EN2} = low, T_A = +25°C		3	5	µA
		V_{EN1} = high, V_{EN2} = low, no load		440		
V_{DD} UVLO	V_{UVLO}	Falling	2.4	2.6		V
VDD UVLO	V_{UVLO}	Rising		2.7	2.9	V
Oscillator Frequency	f_{SW}	f_{SW} = 2.1MHz	1.9	2.1	2.3	MHz
		f_{SW} = 3.2MHz	2.9	3.2	3.6	
Spread Spectrum Range				+3		%

Electrical Characteristics (continued)

(PV1 = PV2 = 5V, T_J = -40°C to +150°C, unless otherwise noted. Typical values are at T_A = +25°C under normal conditions unless otherwise noted. (Note 1) (Note 2))

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
OUT						
Output Voltage	V_{OUT}	Programmable voltage range, 3.0V ≤ V_{PV} ≤ 5.5V (Note 3)	0.5		3.8	V
		Step size, 0.5V ≤ V_{OUT} ≤ 1.5875V (Note 3)		12.5		mV
		Step size, 1.6V ≤ V_{OUT} ≤ 3.8V (Note 3)		50		
Skip Mode Peak Current	I_{SKIP}	Option 1	0.7	0.825	1	A
		Option 2	0.9	1.1	1.3	
		Option 3	1.15	1.4	1.65	
		Option 4	1.3	1.69	2	
Voltage Accuracy		PWM mode, 0A ≤ I_{LOAD} ≤ I_{MAX}, MAX(3.0V, V_{OUT} + 0.5V) ≤ V_{IN} ≤ 5.5V, 0.6V ≥ V_{OUT} ≥ 3.8V	-1		1	%
		PWM mode, 0A ≤ I_{LOAD} ≤ I_{MAX}, 0.5V ≤ V_{OUT} ≤ 0.5875V	-7		+7	mV
		PWM mode, 0A ≤ I_{LOAD} ≤ I_{MAX}, MAX(3.0V, V_{OUT} + 0.5V) ≤ V_{IN} ≤ 5.5V, V_{OUT} = 0.6V. ADJ variant MAX20429CAFNA/VY+	-1		+1	%
DC Load Regulation		0A ≤ I_{LOAD} ≤ I_{MAX} (PWM mode)		0.1		%
DC Line Regulation		PV_ from 3V to 5.5V		0.05		%/V
High-Side On-Resistance	R_{ON-H}	Including metal and package		18	50	mΩ
		Intrinsic		16		
Low-Side On-Resistance	R_{ON-L}	Including metal and package		12	50	mΩ
		Intrinsic		10		
Efficiency		V_{IN} = 5V, V_{OUT} = 1.8V, L = 220nH, DCR = 13mΩ		92.4		%
Current-Limit Threshold	I_{LIM}	Option 1 (2.0A DC)	2.6	3.5		A
		Option 2 (3.0A DC)	3.9	4.7		
		Option 3 (4.0A DC)	5.2	6.0		
		Option 4 (6.0A DC)	7.8	10		
nMOS Zero-Crossing Threshold	I_{ZX}			100		mA
LX_ Rise/Fall Time		PV = 3.3V, I_{OUT} = 2A (Note 3)		1		ns
Dead Time	t_{DEAD}	PV = 3.3V, I_{OUT} = 2A (Note 3)		3		ns
LX_ Leakage Current				0.01		µA
Max Duty Cycle	D_{MAX}	Effective	100			%
Minimum On-Time	t_{ON}			35	60	ns
LX_ Discharge Resistance	R_{DIS}			50		Ω
LX_ Switching Phase		LX1 rising to LX2 rising (Note 3)		180		°

Electrical Characteristics (continued)

(PV1 = PV2 = 5V, T_J = -40°C to +150°C, unless otherwise noted. Typical values are at T_A = +25°C under normal conditions unless otherwise noted. (Note 1) (Note 2))

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Soft-Start Rate		Option 1 (step = 12.5mV for V_{OUT} < 1.6V, otherwise 50mV)		32		clks/step
		Option 2 (step = 12.5mV for V_{OUT} < 1.6V, otherwise 50mV)		16		
		Option 3 (step = 12.5mV for V_{OUT} < 1.6V, otherwise 50mV)		8		
		Option 4 (step = 12.5mV for V_{OUT} < 1.6V, otherwise 50mV)		4		
Soft-Shutdown Rate	t_{SHDN}	Option 1		Hi-Z		
		Option 2 (step = 12.5mV for V_{OUT} < 1.6V, otherwise 50mV)		32		clks/step
Voltage Accuracy		PWM mode, 0A ≤ I_{LOAD} ≤ I_{MAX}, 0.5V ≤ V_{OUT} ≤ 0.5875V	-7		+7	mV
RESET						
OV Threshold Range		V_{OUT} rising	104	108	112	%
UV Threshold Range		V_{OUT} falling	89	92	95	%
Active Timeout Period	t_{HOLD}	Option 1 (15.6ms at 2.1MHz, 10.2ms at 3.2MHz)		32768		clks
		Option 2 (7.8ms at 2.1MHz, 5.1ms at 3.2MHz)		16384		
		Option 3 (3.9ms at 2.1MHz, 2.5ms at 3.2MHz)		8192		
		Option 4 (488µs at 2.1MHz, 320µs at 3.2MHz)		1024		
Output Low Level		I_{SINK} = 3mA		0.1	0.2	V
Thermal Shutdown Temperature	T_{SHDN}	(Note 3)		165		°C
Thermal Shutdown Hysteresis	T_{HYS}	(Note 3)		15		°C
Leakage Current				0.1		µA
OV/UV Filter				10		µs
ENABLE INPUT (EN)						
Input High		Rising	1.5			V
Input Low		Falling			0.5	V
Hysteresis				0.05		V
Leakage Current				0.1		µA
SYNCHRONIZATION (SYNC)						
Input High			1.8			V
Input Low					0.4	V
SYNC Input Frequency Range	f_{SYNC}	f_{SW} = 2.1MHz	1.8		2.5	MHz
		f_{SW} = 3.2MHz	2.8		3.6	
Pull-down Resistance				100		kΩ

Note 1: All units are 100% production tested at +25˚C. All temperature limits are guaranteed by design.

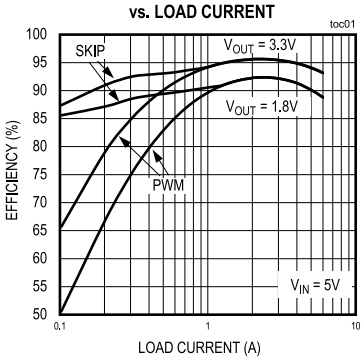
Note 2: The device is designed for continuous operation up to T_J = +125°C for 95,000 hours and T_J = +150°C for 5,000 hours.

Note 3: Guaranteed by design. Not production tested.

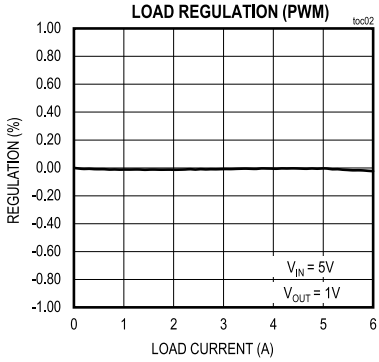
Typical Operating Characteristics

(V_{PV1} = V_{PV2} = 5V; T_A = +25°C unless otherwise noted)

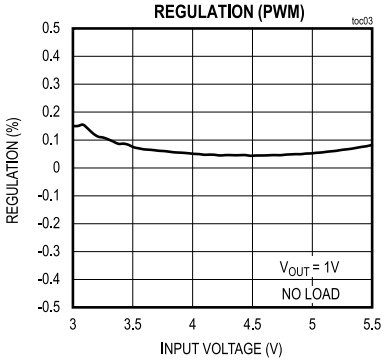
EFFICIENCY vs. LOAD CURRENT



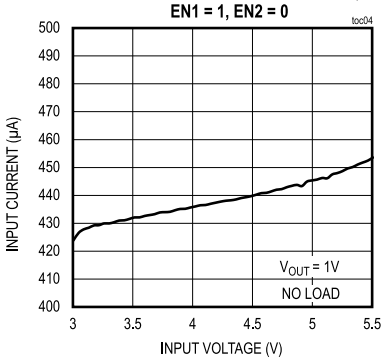
OUT1 LOAD REGULATION (PWM)



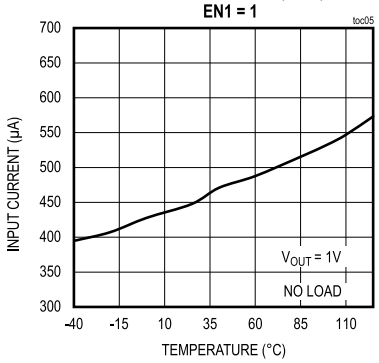
OUT1 LINE REGULATION (PWM)



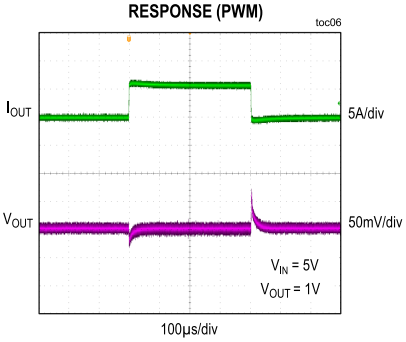
SUPPLY CURRENT vs. INPUT VOLTAGE (SKIP) EN1 = 1, EN2 = 0



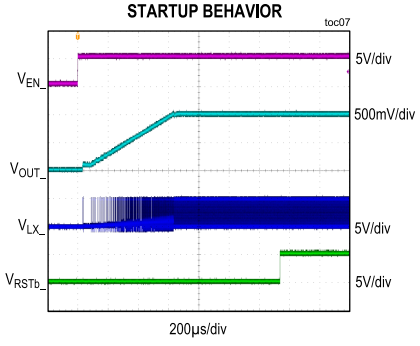
SUPPLY CURRENT vs. TEMPERATURE (SKIP) EN1 = 1



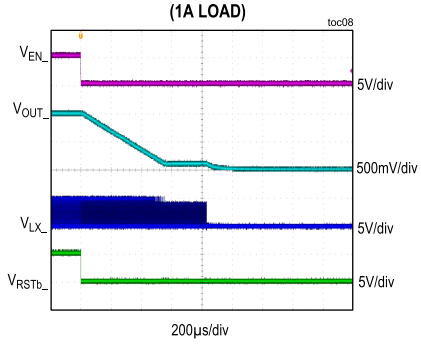
OUT1 LOAD-TRANSIENT RESPONSE (PWM)



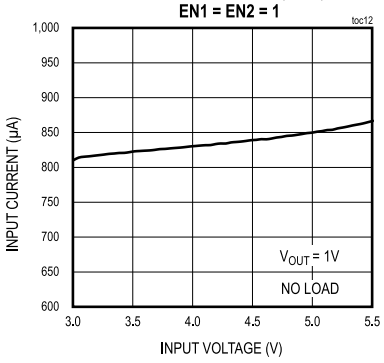
OUT1 STARTUP BEHAVIOR



OUT1 SHUTDOWN (1A LOAD)

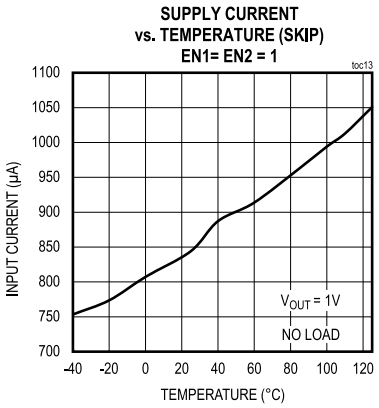


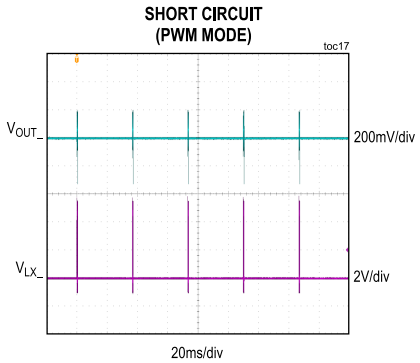
SUPPLY CURRENT vs. INPUT VOLTAGE (SKIP), EN1 = EN2 = 1

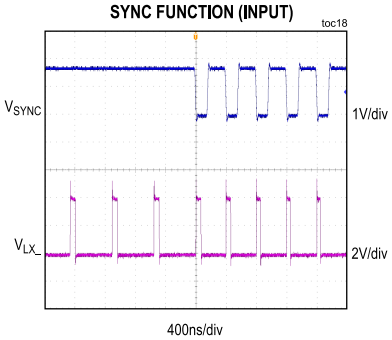


Typical Operating Characteristics (continued)

(V_{PV1} = V_{PV2} = 5V; T_A = +25°C unless otherwise noted)







Pin Configuration

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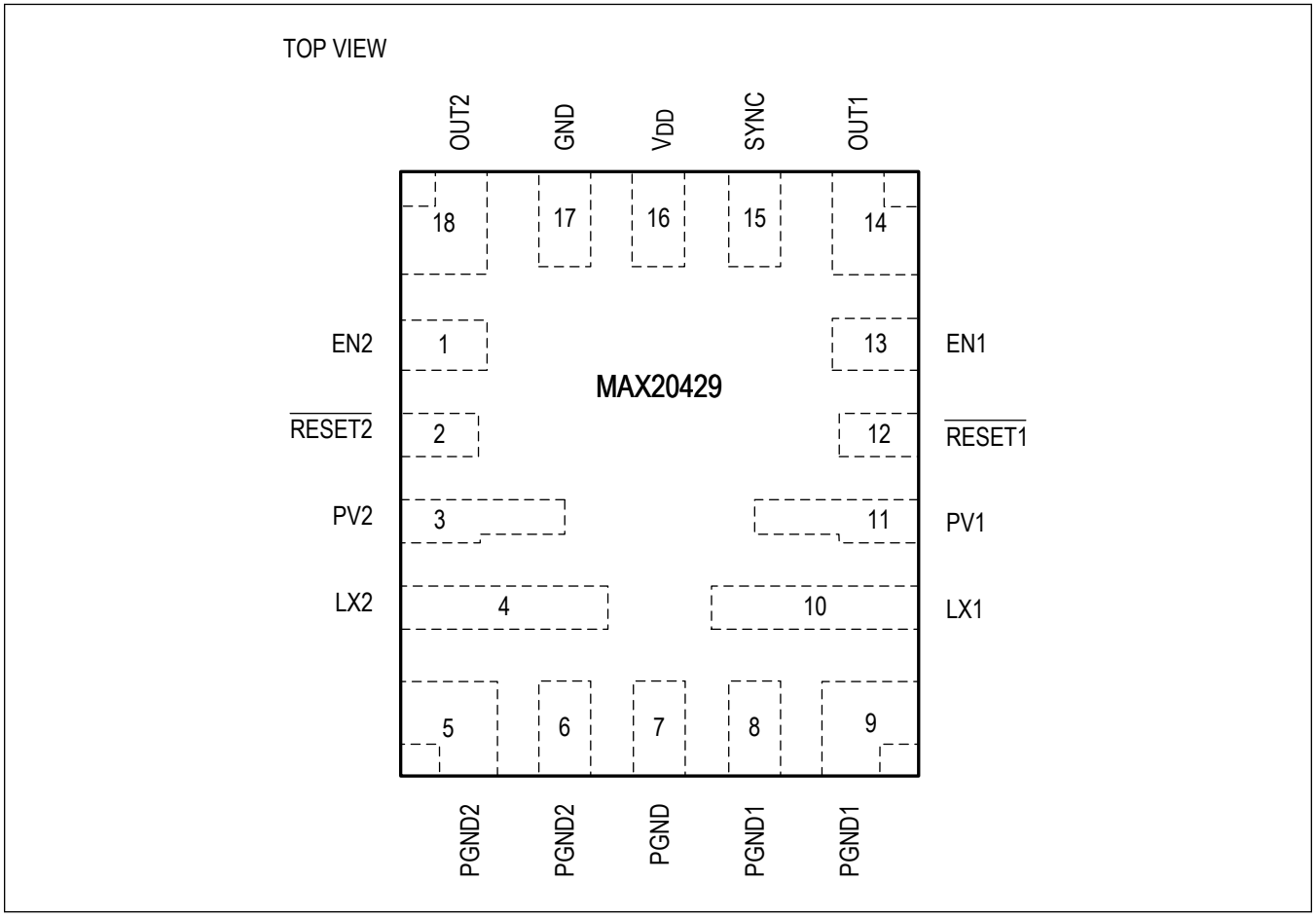


Pin Description

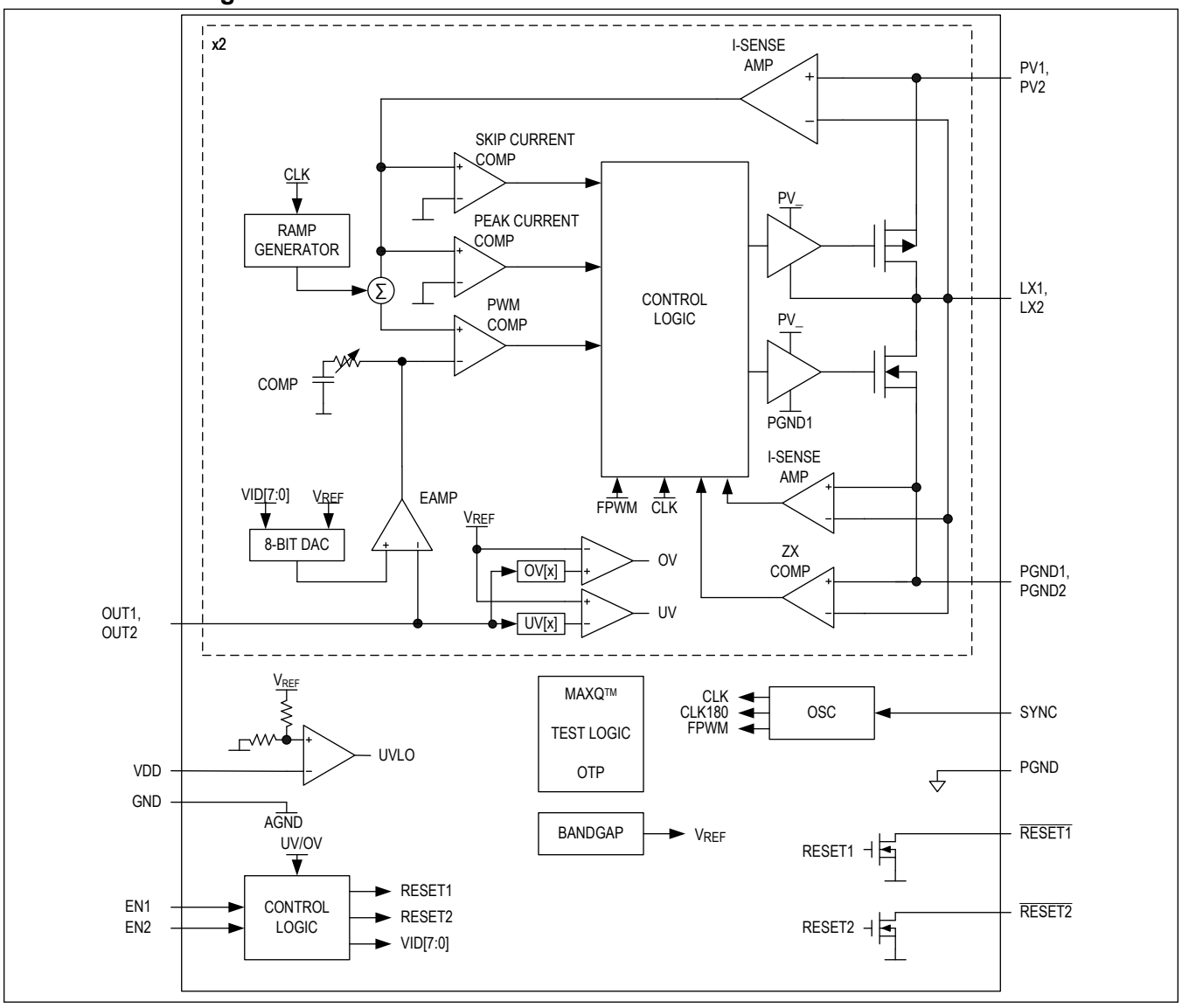
PIN	NAME	FUNCTION
1	EN2	OUT2 Active-High Enable Input. Drive EN2 HIGH for normal operation. The device enters soft-start on the rising edge enters soft-shutdown on the falling edge.
2	$\overline{\text{RESET2}}$	OUT2 Active-Low Open Drain $\overline{\text{RESET}}$ Output. External pull-up resistor required if used.
3	PV2	OUT2 Power Input Supply. Connect a 10µF or larger ceramic capacitor from PV2 to PGND2.
4	LX2	OUT2 Inductor Connection. Connect LX2 to the switched side of the inductor.
5,6	PGND2	OUT2 Power Ground
7	PGND	Power Ground
8,9	PGND1	OUT1 Power Ground
10	LX1	OUT1 Inductor Connection. Connect LX1 to the switched side of the inductor.
11	PV1	OUT1 Power Input Supply. Connect a 10µF or larger ceramic capacitor from PV1 to PGND1.
12	$\overline{\text{RESET1}}$	OUT1 Active-Low Open Drain $\overline{\text{RESET}}$ Output. External pull-up resistor required if used.

Pin Description (continued)

PIN	NAME	FUNCTION
13	EN1	OUT1 Active-High Enable Input. Drive EN1 HIGH for normal operation. The device enters soft-start on the rising edge enters soft-shutdown on the falling edge.
14	OUT1	OUT1 Feedback Input. Connect to the output capacitor of Output 1.
15	SYNC	SYNC Input. Connect SYNC to GND or leave unconnected to enable skip-mode operation under light loads. Connect SYNC to PV or an external clock to enable fixed-frequency FPWM operation.
16	V_{DD}	Internal Analog Supply. The V_{DD} pin is the input to the analog circuitry and should be connected to the same supply as PV1/2 through a series 2Ω resistor IC to a 2.2µF X7R bypass capacitor.
17	GND	Analog Ground
18	OUT2	OUT2 Feedback Input. Connect to the output capacitor of Output 2.

Functional Diagrams

Internal Block Diagram



Detailed Description

MAXQ Power Architecture (No Wasted Performance)

The MAXQ power architecture allows the MAX20429 to achieve the maximum dynamic performance under all worst-case conditions. Without the MAXQ power architecture, typical AC performance must be lowered below the device capabilities to guarantee that the device will be stable under all worst-case application conditions. The MAXQ power architecture keeps the device operating at peak performance.

Enable Input (EN1, EN2)

The enable control input EN1/EN2 activates the device channel from its low-power shutdown state. EN1/EN2 have an input-high threshold of 1.5V (typ), an input-low threshold of 0.5V, and a hysteresis of 50mV (typ). When an enable input goes high, the output voltage ramps up with the soft-start time. When an enable input goes low, the output voltage ramps down with the soft-start time or enters a Hi-Z state depending on the factory programmed setting of the device. See the *Soft-Start and Soft-Shutdown* section for more detail.

$\overline{\text{RESET}}$ Output

The device features open-drain reset outputs that assert low when the corresponding output voltage is outside of the OV/UV window. The OV/UV comparators run from a separate reference to provide drift detection on the outputs. $\overline{\text{RESET}}$_ remains asserted for a fixed timeout period after the corresponding output returns to its regulated voltage. The fixed timeout period for 2.1MHz is selectable between 0.5ms, 3.9ms, 7.8ms, or 15.6ms. The fixed timeout period for 3.2MHz is selectable between 0.3ms, 2.5ms, 5.1ms, or 10.2ms. To obtain a logic signal, place a pull-up resistor between the $\overline{\text{RESET}}$_ pins to the system I/O voltage.

Internal Oscillator

The device has a spread-spectrum oscillator that varies the internal operating frequency by ±3% relative to the internally generated operating frequency of 2.1MHz/3.2MHz (typ). This function does not apply to externally applied oscillation frequency on the SYNC pin.

Synchronization (SYNC)

A logic-high on SYNC enables fixed-frequency, forced-PWM mode. Apply an external clock on the SYNC input to synchronize the internal oscillator to an external clock. The SYNC input accepts signal frequencies in the range of 1.9MHz < f_{SYNC} < 2.3MHz when f_{SW} = 2.1MHz, and 2.9MHz < f_{SYNC} < 3.6MHz when f_{SW} = 3.2MHz. When the pin is open-circuited or logic-low, the SYNC input enables the device to enter a low-power skip mode under light-load conditions if the IC is configured to allow that behavior.

Soft-Start and Soft-Shutdown

The device includes a factory-programmable fixed soft-start time. Soft-start time limits startup inrush current by forcing the output voltage to ramp up towards its regulation point. The soft-start ramp rate can be factory programmed with four different options: 32, 16, 8, or 4 clocks per step, where step size = 12.5mV for V_{OUT} ≤ 1.6V (50mV step size when V_{OUT} > 1.6V).

When an EN pin goes low, the associated output enters shutdown. There are factory programmable options available that will either simply disable switching and activate a 50Ω (typ) discharge resistor, or perform a soft-shutdown by ramping down the reference at a fixed rate until a minimum on-time of 20ns is reached, at which point the switching stops and the discharge resistor is activated. The soft-shutdown ramp rate is fixed at 32 clocks per step, where step size = 12.5mV for V_{OUT} ≤ 1.6V (50mV step size when V_{OUT} > 1.6V) when not configured as a simple discharge resistor.

Current Limit / Short-Circuit Protection

The device features a current limit that protects the device against short-circuit and overload conditions at the output. In the event of a short-circuit or overload condition, the high-side MOSFET remains on until the inductor current reaches the high-side MOSFET's current-limit threshold. The converter then turns on the low-side MOSFET to allow the inductor

current to ramp down. Once the inductor current crosses below the low-side MOSFET current-limit threshold, the converter turns on the high-side MOSFET again. This cycle repeats until the short or overload condition is removed.

If the device crosses the current limit with the output voltage below 50% of the target, hiccup mode will be enabled and the output will turn off for 10ms, then the channel will attempt to power up through soft-start.

PWM/SKIP Modes

The device features an input (SYNC) that puts the converter either in SKIP mode or forced-PWM mode of operation. See *Pin Descriptions* for mode detail. In FPWM mode of operation, the converter switches at a constant frequency with variable on-time. In SKIP mode, the converter's switching frequency is load-dependent until the output load reaches a set threshold. At higher load current, the switching frequency does not change, and the operating mode is similar to the FPWM mode. SKIP mode helps improve efficiency in light-load applications by allowing the converter to turn on the high-side switch only when the output voltage falls below a set threshold. As such, the converter does not switch MOSFETs on and off, as is often the case in the PWM mode. Consequently, the gate charge and switching losses are much lower in SKIP mode.

Overtemperature Protection

Thermal overload protection limits the total power dissipation in the MAX20429. When the junction temperature exceeds 165°C (typ), an internal thermal sensor shuts down both outputs, allowing the IC to cool. The thermal sensor turns on the outputs again after the junction temperature cools by 15°C.

Spread Spectrum

The spread-spectrum option is enabled/disabled based on the part number. See the ordering table. If the spread spectrum is enabled and an external clock is applied to the SYNC pin, then the spread-spectrum circuit is bypassed, effectively disabling the option.

Resistor-Adjustable Output

MAX20429 output voltage can be set by external resistors in addition to the factory programmed V_{OUT} options. See the *Typical Application Diagram* for placement of R1 and R2 external resistors. Desired output voltage can be calculated using the following method:

$$V_{OUT} = \frac{R1 + R2}{R2} * V_{REF}$$

where V_{REF} = 0.6V when using the device specified for adjustable output voltage.

Fixed output voltage devices can use external resistors to achieve output voltages higher than the factory setting. When using a fixed output voltage device, use the factory preset output voltage as V_{REF} to calculate the resistor values.

Applications Information

Input Capacitor Selection

An input filter capacitor reduces peak currents drawn from the upstream power source and reduces noise and voltage ripple on the input (caused by the circuit's switching behavior). One 10µF X7R ceramic capacitor each is recommended for the PV1 and PV2 pins. The V_{DD} pin is the input to the analog circuitry and should be connected to the same supply as PV1/2 through a series 2Ω resistor IC to a 2.2µF X7R bypass capacitor.

Inductor Selection

Three key inductor parameters must be specified for operation with the MAX20429: inductance value (L), peak inductor current (I_{PEAK}), and inductor saturation current (I_{SAT}). The minimum required inductance is a function of operating frequency, input-to-output voltage differential, and the maximum output current capability of the output. A lower inductor value minimizes size and cost, improves large-signal and transient response, but reduces efficiency due to higher peak currents and higher peak-to-peak output-voltage ripple for the same output capacitor. On the other hand, higher inductance increases efficiency by reducing the ripple current. Resistive losses due to extra wire turns can exceed the benefit gained from lower ripple current levels especially when the inductance is increased without also allowing for larger inductor dimensions.

Soft-saturating inductors are recommended for use with the MAX20429. The gradual decrease in inductance means that the IC will respond to overcurrent conditions before the LX current reaches dangerously high levels that might otherwise result in damage to the IC. If a hard-saturating inductor is used, its saturation current must be above the maximum LX current limit. For a soft-saturation inductor, only the current limit for temperature must be above the maximum LX current limit.

The MAX20429 is designed for nominal ΔI_{PK-PK} equal to approximately 33% of the full load current. Use the following equation to calculate the typical inductance with respect to ripple current:

$$L = \frac{\left(V_{IN} - V_{OUT}\right) \times V_{OUT}}{V_{IN} \times f_{SW} \times I_{MAX} \times \Delta_{PK-PK}}$$

The V_{IN} and V_{OUT} terms are typical values to optimize inductor selection for expected operating conditions. The switching frequency f_{SW} is 2.1MHz, 3.2MHz, or a different value if the synchronization function is utilized. The maximum current I_{MAX} is the channel's rated output current (2A, 3A, 4A, or 6A), not the expected application maximum load current. Calculate the minimum inductance L_{MIN1} with Δ_{PK-PK} = 40%, and the typical inductance L_{TYP1} with Δ_{PK-PK} = 30%.

The second bound on minimum inductance is with respect to slope compensation. This applies only to peak current control, not to adaptive COT control. The absolute minimum inductance allowable must ensure that the inductor current downslope is less than twice the downslope of the compensation ramp:

$$-m \geq \frac{m2}{2}$$

Table 1. Slope Compensation Terms

TERM	VALUE
m2	Inductor current downslope: $\frac{V_{OUT}}{L} \times R_{CS}$
-m	Compensating ramp: OTP_SLP * 0.680V/µs
OTP_SLP	1/2, 2/3, 4/3 (factory programmed)
R_{CS}	0.330Ω for 2A channel
	0.240Ω for 3A channel
	0.185Ω for 4A channel
	0.133Ω for 6A channel

For margin of error, the worst-case inductance (largest derating for current and temperature, plus lowest value for percent tolerance) should result in the inductor downslope being 25% greater than half the slope compensation ramp:

$$L_{MIN2} = V_{OUT} \times \frac{R_{CS}}{2 \times m} \times 1.25$$

Nominally, the inductor current downslope should be approximately equal to the compensating ramp. Equal downslopes will result in current waveform perturbations being eliminated in a single switching cycle:

$$L_{TYP2} = V_{OUT} \times \frac{R_{CS}}{m}$$

Two equations must therefore be fulfilled: one equation for minimum worst-case inductance (required) and one for typical inductance (recommended): L_{MIN} > max (L_{MIN1} , L_{MIN2}) and L_{TYP} > max (L_{TYP1} , L_{TYP2}). The maximum inductance should be less than 2 x L_{TYP2} to avoid degrading the control performance.

Output Capacitors

The MAX20429 is designed to be stable with low-ESR ceramic capacitors. Other capacitor types are not recommended as the ESR zero can affect stability of the device. The output capacitor calculations below are guidelines based on nominal conditions. The phase margin must be measured on the final circuit to verify proper stability is achieved.

Conditions:

- Feed-forward zero enabled, GMZ = 116µS, FFR = 300kΩ
- Nominal inductor value based on the *Inductor Selection* section

For V_{OUT} < 1.6V

$$COUT_{MIN} = 11.5\mu sec \times I_{MAX} \times \frac{R_{COMP}}{140k\Omega}$$

$$COUT_{TYP} = 24.5\mu sec \times I_{MAX} \times \frac{R_{COMP}}{140k\Omega}$$

For V_{OUT} ≥ 1.6V

$$COUT_{MIN} = 8.0\mu sec \times I_{MAX} \times \frac{R_{COMP}}{140k\Omega}$$

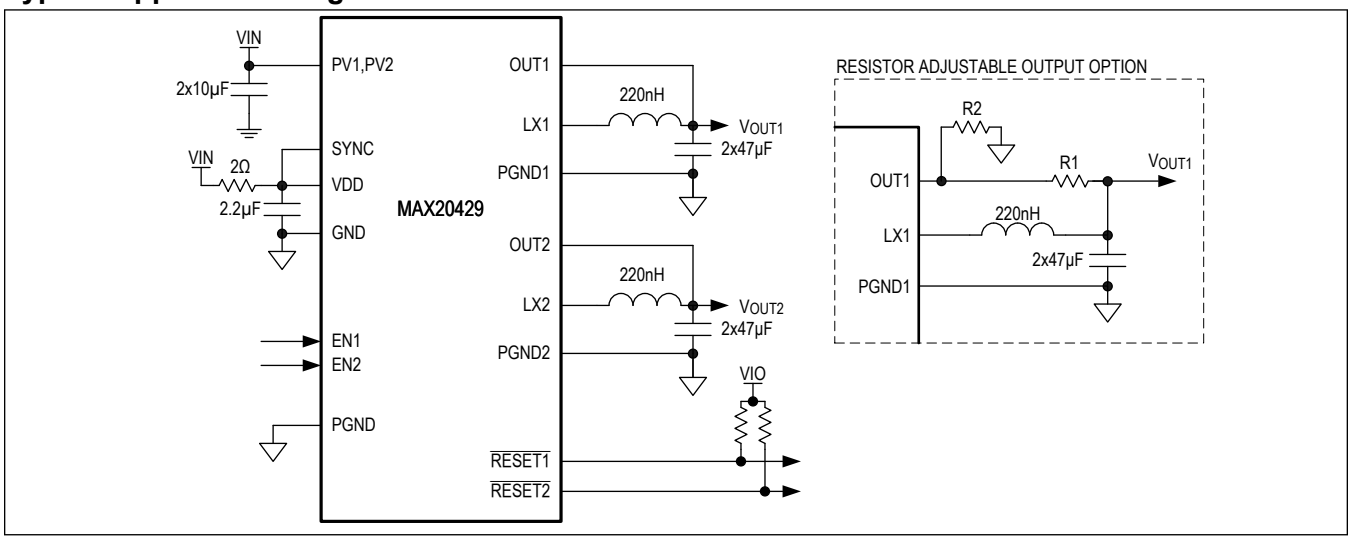
$$COUT_{TYP} = 21.0\mu sec \times I_{MAX} \times \frac{R_{COMP}}{140k\Omega}$$

Table 2. Output Capacitor Terms

TERM	DESCRIPTION
$COUT_{MIN}$	Minimum fully derated capacitance necessary for phase margin of approximately 45 degrees
$COUT_{TYP}$	Nominal output capacitance for a UGBW of 200kHz
I_{MAX}	The IC channel's maximum DC current capability: 2A, 3A, 4A, or 6A
V_{OUT}	Nominal output voltage
R_{COMP}	Compensation Resistor Setting. Default = 140kΩ. Can be factory set from 35kΩ to 297.5kΩ in 17.5kΩ increments.

Typical Application Circuits

Typical Application Diagram



Ordering Information

PART	V_{OUT1} (V) (1)	I_{OUT1} (A) (2)	V_{OUT2} (V) (1)	I_{OUT2} (A) (2)	SPREAD SPECTRUM (3)	f_{SW} (MHz) (4)	t_{HOLD} (ms) (5)	SOFT-START	SOFT-SHUTDOWN	R_{COMP} (kΩ)
MAX20429AAFNA/VY+	0.85	3	0.72	6	ON	2.1	15.6	1.64mv/µs	0.82mv/µs	122.5
MAX20429CAFNA/VY+	ADJ (6)	6	ADJ (6)	6	ON	2.1	3.9	730µs (fixed)	730µs (fixed)	140
MAX20429CAFNC/VY+*	1.1	6	1.5	6	OFF	2.1	15.6	0.82mV/µs	0.82mV/µs	70 87.5
MAX20429CAFND/VY+*	1	6	0.5	6	OFF	2.1	15.6	0.82mV/µs	0.82mV/µs	297.5 297.5
MAX20429CAFNF/VY+	1	6	1	6	ON	2.1	3.9	0.82mV/µs	0.82mV/µs	140 140

For variants with different options, contact the factory.

/V Denotes an AEC-Q100 automotive-qualified part.

+ Denotes lead(Pb)-free/RoHS-compliant package.

T Denotes tape-and-reel.

Y Denotes side-wettable package.

** Potential future product.*

(1) Fixed factory setting, 0.5V to 1.5875V in 12.5mV steps ;or 1.6V to 3.8V in 50mV steps.

(2) 2, 3, 4, or 6

(3) ON or OFF

(4) 2.1 or 3.2

(5) 0.5, 3.9, 7.8, 15.6 for f_{SW} = 2.1MHz or 0.3, 2.5, 5.1, 10.2 for f_{SW} = 3.2MHz.

(6) ADJ (adjustable externally)

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	6/20	Initial release	—
1	12/20	Updated General Description, Benefits and Features, Absolute Maximum Ratings, Electrical Characteristics, Detailed Description, and Ordering Information	1, 4, 5, 12, 13, 16
2	5/25	Updated Benefits and Features, Absolute Maximum Ratings, Package Information, Electrical Characteristics, Pin Description table, Ordering Information table	1, 4, 6, 7, 10, 16