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2.2MHz Sync Boost and Step-Down Converters

MAX20414

General Description

The MAX20414 is a high-efficiency, two-output, low-voltage DC-DC converter. OUT1 boosts the input supply up to 8.5V at up to 750mA, while a synchronous step-down converter (OUT2) operates from a 3.0V to 5.5V input voltage range and provides a 0.8V to 3.8V output voltage range at up to 3A. The boost converter achieves ±2% and the buck converter achieves ±1.5% output error over load, line, and temperature range.

The IC features a 2.2MHz fixed-frequency pulse-width modulation (PWM) mode for better noise immunity and load-transient response, and a pulse-frequency modulation mode (skip) for increased efficiency during light-load operation. The 2.2MHz frequency operation allows for the use of all-ceramic capacitors and minimizes external components footprint. The programmable spread-spectrum frequency modulation minimizes radiated electromagnetic emissions. Integrated low $R_{DS(ON)}$ switches improve efficiency at heavy loads and make the layout a much simpler task with respect to discrete solutions.

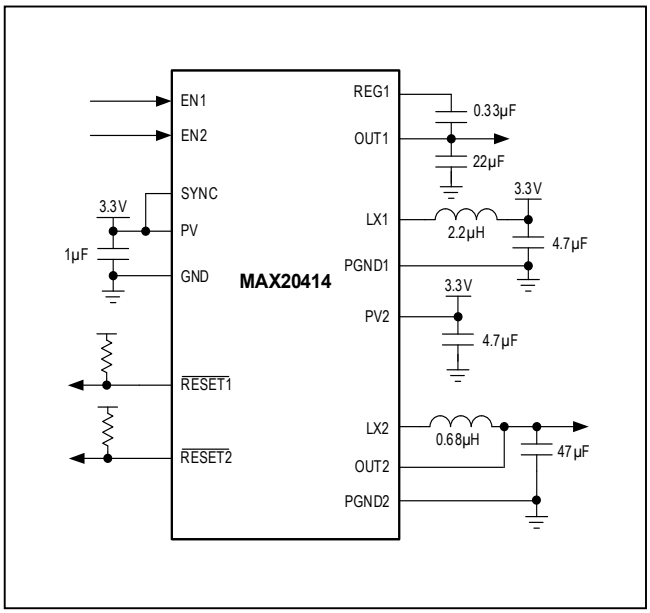
The IC is offered with either a factory-preset or resistor-adjustable output voltage on the step-down converter. The boost converter output voltage is factory-preset. Other features include soft-start, overcurrent, and overtemperature protections. This high-efficiency two-output low-voltage DC-DC converter is available in a lead(Pb)-free, 24-pin TQFN package (see the *Ordering Information* table for options).

***Ordering Information* appears at end of data sheet.**

Benefits and Features

- Multiple Functions for Small Size
  - Synchronous 750mA Boost Converter
    - Fixed from 3.8V to 8.5V in 100mV Steps
  - Synchronous Buck Converter Up to 3A
    - Factory-Configurable Output Voltage from 0.8V to 3.8V in 25mV Steps
    - Resistor-Adjustable
  - 3.0V to 5.5V Operating Supply Voltage
  - 2.2MHz Operation
  - 93% ±3% Undervoltage Threshold
  - 107% ±3% Overvoltage Threshold
  - Individual EN_ Inputs and $\overline{\text{RESET}}$_ Outputs
- High Precision
  - ±2% Output-Voltage Accuracy (OUT1), and ±1.5% Output-Voltage Accuracy (OUT2)
  - Good Load-Transient Performance
- Robust for the Automotive Environment
  - Current-Mode, Forced-PWM, and Skip Operation
  - Overtemperature and Short-Circuit Protection
  - 4mm x 4mm 24-Pin TQFN
  - -40°C to +125°C Automotive Temperature Range

Typical Operating Circuit



19-8781; Rev 0; 2/17

Absolute Maximum Ratings

PV2 to PGND_ .....-0.3V to +6V
PV to GND.....-0.3V to +6V
REG1 to GND.....-0.3V to OUT1 + 0.3V
EN1, EN2, SYNC to GND .....-0.3V to V_{PV} + 0.3V
$\overline{RESET1}$, $\overline{RESET2}$, GND .....-0.3V to +6V
OUT1 to PGND1 .....-0.3V to +10V
OUT2 to PGND2 ..... -0.3V to V_{PV2} + 0.3V
LX1 to PGND1.....-0.3V to V_{OUT1} + 0.3V
LX2 to PGND2..... -0.3V to V_{PV2} + 0.3V
GND to PGND .....-0.3V to +0.3V

LX1 Continuous RMS Current 2A
LX2 Continuous RMS Current 3A
Output Short-Circuit Duration.....Continuous
Continuous Power Dissipation (T_A = +70°C)
24-Pin TQFN-EP (derate 30.3 mW/°C > +70°C).....2222mW
Operating Temperature Range..... -40°C to +125°C
Junction Temperature.....+150°C
Storage Temperature Range..... -65°C to +150°C
Lead Temperature (soldering, 10s) .....+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Package Information

TQFN

TQFN Package Drawing Link

PACKAGE CODE	T2444+4C
Outline Number	21-0139
Land Pattern Number	90-0022
Thermal Resistance, Single-Layer Board:	
Junction-to-Ambient Thermal Resistance (θ_{JA})	48°C/W
Junction-to-Case Thermal Resistance (θ_{JC})	3°C/W
Thermal Resistance, Four-Layer Board:	
Junction-to-Ambient Thermal Resistance (θ_{JA})	36°C/W
Junction-to-Case Thermal Resistance (θ_{JC})	3°C/W

For the latest package outline information and land patterns (footprints), go to www.maximintegrated.com/packages. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to www.maximintegrated.com/thermal-tutorial.

Electrical Characteristics

(V_{PV1}, V_{PV2} = V_{PV} = 3.3V, V_{EN1} = V_{EN2} = 3.3V, T_A = T_J = -40°C to +125°C, unless otherwise noted. Typical values are at T_A = +25°C under normal conditions, unless otherwise noted.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Supply Voltage Range	V_{IN}	Fully operational	3.0		5.5	V
UVLO	$UVLO_R$	Rising		2.7	2.9	V
	$UVLO_F$	Falling	2.4	2.6		V
Shutdown Supply Current	I_{IN}	EN1, EN2 = low		1.7	5	µA
Supply Current	I_{IN1}	EN1 = high, I_{OUT1} = 0mA, skip, V_{OUT1} 104% above regulation point		130	210	µA
	I_{IN2}	EN2 = high, I_{OUT2} = 0mA, skip, V_{OUT2} 104% above regulation point		80	160	

Electrical Characteristics (continued)

(V_{PV1}, V_{PV2} = V_{PV} = 3.3V, V_{EN1} = V_{EN2} = 3.3V, T_A = T_J = -40°C to +125°C, unless otherwise noted. Typical values are at T_A = +25°C under normal conditions, unless otherwise noted.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
PWM Switching Frequency	f_{SW}	Internally generated	2.0	2.2	2.4	MHz
Spread Spectrum		Factory option enabled		±3		%
OUT1						
Voltage Accuracy	V_{OUT1}	I_{LOAD} = 0A to I_{MAX}, 3.0V ≤ V_{IN} ≤ 3.6V	-2		+2	%
pMOS On-Resistance	HS_{CH1}	V_{PV} = V_{PV2} = 3.3V, I_{LX1} = 0.1A		250	500	mΩ
nMOS On-Resistance	LS_{CH1}	V_{PV} = V_{PV2} = 3.3V, I_{LX1} = 0.1A		150	300	mΩ
nMOS Current-Limit Threshold	ILIM1		1.6	2		A
pMOS Turn-Off Threshold	ZX1		15	50	90	mA
LX1 Leakage Current	$LX1_{LKG}$	V_{PV} = V_{PV2} = 6V, LX1 = PGND1 or OUT1, T_A = +25°C	-1	+0.1	+1	µA
Maximum Duty Cycle	MAX_{DC1}			75		%
OUT1 Discharge Resistance	R_{DISCH1}	V_{EN1} = 0V, V_{OUT1} = 1V	200	440	700	Ω
OUT1 Discharge Current	I_{DISCH1}	V_{EN1} = 0V, V_{OUT1} = regulation point	4	10	18	mA
Switching Phase	PH_{LX1}			0		°
REG1 to OUT1	V_{REG1}	V_{OUT1} > 4.5V	-5.1	-4.5	-3.9	V
Skip Threshold	TH_{SKIP1}	Percentage of nMOS current-limit threshold	5	15	30	%
Soft-Start Time	SST_1			1.9		ms
OUT2						
Voltage Accuracy	V_{OUT2}	I_{LOAD} = 0A to I_{MAX}, 3.0V ≤ V_{PV} ≤ 5.5V	-1.5		+1.5	%
pMOS On-Resistance	HS_{CH2}	V_{PV} = V_{PV2} = 3.3V, I_{LX2} = 0.1A		82	150	mΩ
nMOS On-Resistance	LS_{CH2}	V_{PV} = V_{PV2} = 3.3V, I_{LX2} = 0.1A		50	100	mΩ
pMOS Current-Limit Threshold	$ILIM2_{1A}$	Factory option 1 (1A)	1.4	1.9		A
	$ILIM2_{2A}$	Factory option 2 (2A)	2.8	3.8		
	$ILIM2_{3A}$	Factory option 3 (3A)	4.2	5.8		
nMOS Zero-Crossing Threshold	ZX2			150		mA
Maximum Duty Cycle	MAX_{DC2}				100	%
Minimum On-Time	MIN_{TON2}			44	68	ns
LX2 Discharge Resistance	R_{DISCH2}	V_{EN2} = 0V (connected to LX2)		40	80	Ω
Switching Phase	PH_{LX2}			160		°
Skip Threshold	$SKIP_2$	Percentage of pMOS current-limit threshold		20		%
Soft-Start Time	SST_2			2.5		ms
THERMAL OVERLOAD						
Thermal-Shutdown Temperature	TSD	T_J rising		165		°C
Hysteresis				15		°C

Electrical Characteristics (continued)

(V_{PV1}, V_{PV2} = V_{PV} = 3.3V, V_{EN1} = V_{EN2} = 3.3V, T_A = T_J = -40°C to +125°C, unless otherwise noted. Typical values are at T_A = +25°C under normal conditions, unless otherwise noted.) (Note 1)

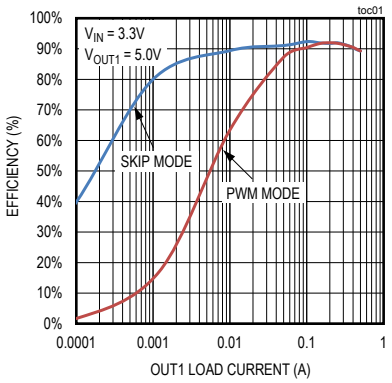
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
$\overline{\text{RESET1}}$, $\overline{\text{RESET2}}$						
Overvoltage Threshold		Rising, percentage of nominal output	104	107	110	%
Undervoltage Threshold		Falling, percentage of nominal output	90	93	96	%
Active Hold Period			6.75	7.5	8.25	ms
Delay Filter		10% below/above threshold		10		µs
Output-High Leakage Current	I_{OZH}		-0.5	+0.1	+0.5	µA
Output Low Level	V_{OL}	3.0V ≤ V_{PV} ≤ 5.5V, sinking -2mA			0.2	V
EN1, EN2 AND SYNC INPUTS						
Input High Level	V_{IH}		1.5			V
Input Low Level	V_{IL}				0.5	V
Input Hysteresis				0.1		V
EN1, EN2 Input Pulldown Current	I_{IL}	V_{PV} = 3.3V	0	0.25	1	µA
SYNC Input Pulldown	$SYNC_{PD}$		50	100	200	kΩ
SYNC Input Frequency Range	f_{SYNC}		1.8		2.6	MHz
SYNC OUTPUT						
Output Low	V_{OL}	V_{PV} = 3.3V, I_{SINK} = 2mA			0.4	V
Output High	V_{OH}	V_{PV} = 3.3V, I_{SOURCE} = 2mA	2.7			V

Note 1: All units are 100% production tested at +25°C. All temperature limits are guaranteed by design.

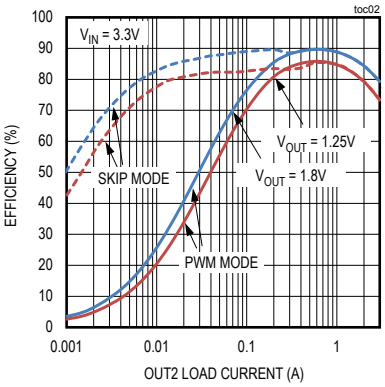
Typical Operating Characteristics

(V_{PV1}, V_{PV2} = V_{PV} = 3.3V, V_{EN1} = V_{EN2} = 3.3V, T_A = T_J = -40°C to +125°C, unless otherwise noted. Typical values are at T_A = +25°C under normal conditions, unless otherwise noted.) (Note 1)

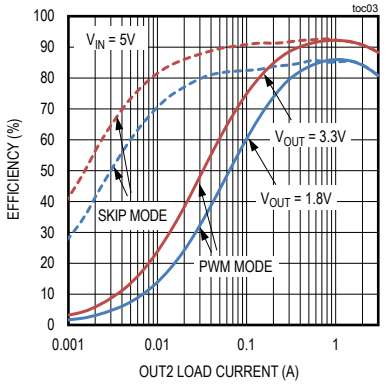
OUT1 EFFICIENCY



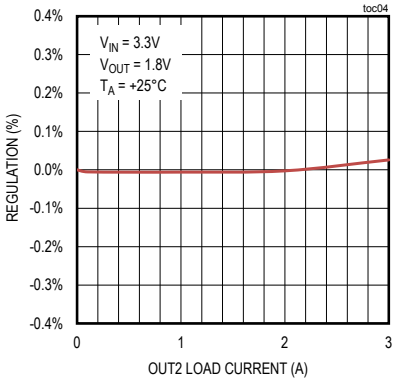
OUT2 EFFICIENCY



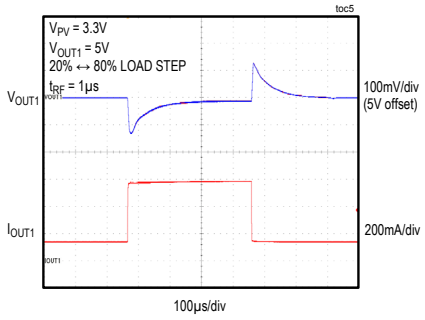
OUT2 EFFICIENCY



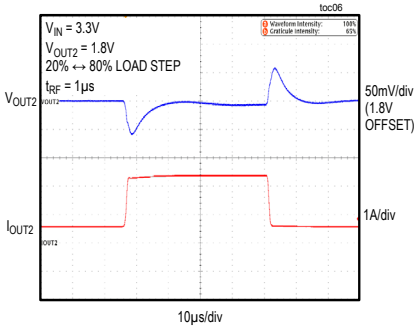
OUT2 LOAD REGULATION



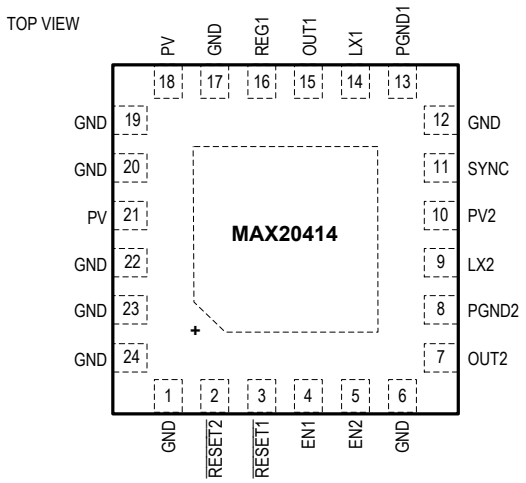
OUT1 LOAD TRANSIENT (PWM MODE)



OUT2 LOAD TRANSIENT (PWM MODE)



Pin Configurations



TQFN
(4mm x 4mm)

Pin Description

PIN	NAME	FUNCTION
1	GND	Ground. Connect all PGND and GND pins together.
2	$\overline{\text{RESET2}}$	Open-Drain RESET Output for OUT2. To obtain a logic signal, pull up $\overline{\text{RESET2}}$ with an external resistor.
3	$\overline{\text{RESET1}}$	Open-Drain RESET Output for OUT1. To obtain a logic signal, pull up $\overline{\text{RESET1}}$ with an external resistor.
4	EN1	Active-High Enable Input for OUT1. Drive EN1 high for normal operation.
5	EN2	Active-High Enable Input for OUT2. Drive EN2 high for normal operation.
6, 17, 19, 20, 22–24	GND	Ground. Connect all PGND and GND pins together.
7	OUT2	OUT2 Voltage-Sense Input/Feedback Pin
8	PGND2	Power Ground for OUT2. Connect all PGND and GND pins together.
9	LX2	Inductor Connection. Connect LX2 to the switched side of the inductor.
10	PV2	Power Input Supply for OUT2. Connect a 4.7µF ceramic capacitor from PV2 to PGND2.
11	SYNC	SYNC I/O. When configured as an input, connect SYNC to GND or leave unconnected to enable skip-mode operation under light loads. Connect SYNC to PV or an external clock to enable fixed-frequency forced-PWM-mode operation. When configured as an output (factory-configured), connect SYNC to other device's SYNC inputs.
12	GND	Unused. Connect to ground.
13	PGND1	Power Ground for OUT1. Connect all PGND and GND pins together.
14	LX1	Inductor Connection. Connect LX1 to the switched side of the inductor.
15	OUT1	OUT1 Voltage Output

Pin Description (continued)

PIN	NAME	FUNCTION
16	REG1	Open Supply for OUT1. Connect a 0.33µF ceramic capacitor from REG1 to OUT1.
18	PV	Analog Input Supply. Connect a 1µF or larger ceramic capacitor from PV to GND.
21	PV	Input Supply. Connect to PV (pin 18) or PV2 (pin 10) through PCB trace.
—	EP	Exposed Pad. Connect the exposed pad to ground. Connecting the exposed pad to ground does not remove the requirement for proper ground connections to PGND. The exposed pad is attached with epoxy to the substrate of the die, making it an excellent path to remove heat from the IC.

Detailed Description

The MAX20414 is a high-efficiency, two-output, low-voltage DC-DC converter. OUT1 is a 750mA synchronous DC-DC boost converter that steps up the 3.0V to 5.5V input supply to a factory-set fixed output voltage between 3.8V and 8.5V in 100mV steps. The boost converter has true shutdown so the output voltage discharges to 0V when off. The synchronous step-down converter (OUT2) operates from a 3.0V to 5.5V input voltage and provides a 0.8V to 3.80V output voltage at up to 3A. OUT2 can be factory-set to a fixed voltage or to be resistor-adjustable. The boost converter achieves ±2% and the buck converter achieves ±1.5% output error over load, line, and temperature range.

The IC features a 2.2MHz fixed-frequency PWM mode for better noise immunity and load-transient response, and a pulse-frequency modulation mode (skip) for increased efficiency during light-load operation. The 2.2MHz frequency operation allows for the use of all-ceramic capacitors and minimizes external components. The programmable spread-spectrum frequency modulation minimizes radiated electromagnetic emissions. The spread modulation can be factory set to pseudorandom. Integrated low $R_{DS(ON)}$ switches improve efficiency at heavy loads and make the layout a much simpler task with respect to discrete solutions.

The IC contains overvoltage/undervoltage thresholds for each output that are mapped to the $\overline{RESET1}$ and $\overline{RESET2}$ pins. In light-load applications, a logic input (SYNC) allows the ICs to operate either in skip mode for reduced current consumption, or fixed-frequency, forced-PWM mode to eliminate frequency variation, and help minimize EMI. Protection features include cycle-by-cycle current limit, and thermal shutdown with automatic recovery.

Enable Inputs (EN1, EN2)

The enable control inputs (EN1, EN2) activate the device channels from their low-power shutdown state. EN1 and EN2 have an input threshold of 1.0V (typ) with a hysteresis of 80mV (typ) and are fully independent, with no timing restrictions between each other. When an enable input goes high, the associated output voltage ramps up with the programmed soft-start time.

Reset Outputs ($\overline{RESET1}$, $\overline{RESET2}$)

The IC features individual open-drain reset outputs for each output that asserts low when the corresponding output voltage is outside of the overvoltage/undervoltage window, and remain asserted for a fixed timeout period after the corresponding output rises up to its regulated voltage. The fixed timeout period is selectable between 0.8ms, 3.7ms, 7.4ms, or 14.9ms (see *Ordering Information*). To obtain a logic signal, place a pullup resistor between the $\overline{RESET1}$/$\overline{RESET2}$ pins and the system I/O voltage.

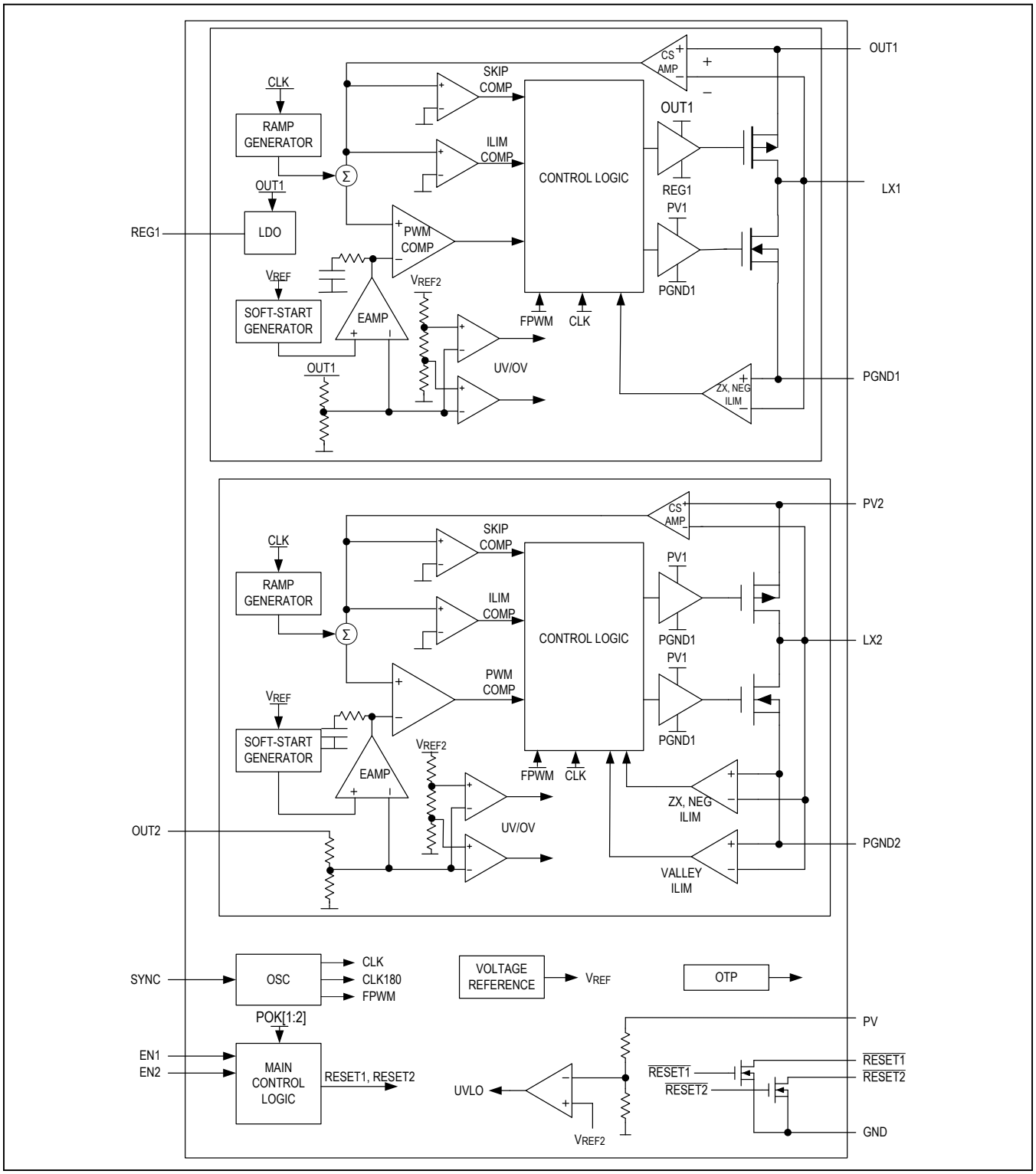
OUT1/OUT2 Feedback

The output voltage is fed back to the coresponding OUT_ feedback pin to close the regulation loop. OUT1 has a fixed output voltage set at the factory. When OUT2 is configured as an adjustable output, the output voltage is set by connecting a resistor-divider network from the output to ground with the center point connected to the OUT2 pin on the IC (when OUT2 is configured as a fixed output voltage, the feedback pin is connected to the output capacitor).

Internal Oscillator

The IC has a spread-spectrum oscillator that varies the internal operating frequency up by ±3% relative to the internally generated operating frequency of 2.2MHz (typ). This function does not apply to externally applied oscillation frequency. The spread frequency generated is pseudorandom with a repeat rate well below the audio band. This feature is programmed at the factory.

Internal Block Diagram



Synchronization (SYNC)

SYNC is factory-programmable I/O (see *Ordering Information* for available options). When configured as an input, a logic-high on SYNC enables fixed-frequency, forced-PWM (FPWM) mode. Apply an external clock on the SYNC input to synchronize the internal oscillator to an external clock. The SYNC input accepts signal frequencies in the range of 1.8MHz < f_{SYNC} < 2.6MHz. When the pin is open or logic-low, the SYNC input enables the device to enter a low-power skip mode under light-load conditions. When configured as an output, SYNC outputs the internally generated 2.2MHz clock that switches from PV to GND. All converters operate in FPWM mode when SYNC is configured as an output.

Soft-Start

The IC includes a fixed 1.9ms soft-start for the boost converter and 2.5ms for the buck converter. Soft-start time limits startup inrush current by forcing the output voltage to ramp up towards its regulation point.

PWM/Skip Modes

The IC features a SYNC input that puts the converter in skip mode for FPWM mode of operation (see the *Pin Description* for more information). In PWM mode, the converter switches at a constant frequency with variable on-time. In skip mode, the converter's switching frequency is load-dependent until the output load reaches a certain threshold. At higher load current, the switching frequency does not change and the operating mode is similar to the PWM mode. Skip mode helps improve efficiency in light-load applications by allowing the converter to turn on the high-side switch only when the output voltage falls below a set threshold. As such, the converter does not switch MOSFETs on and off as often as is the case in the PWM mode. Consequently, the gate charge and switching losses are much lower in skip mode.

Overtemperature Protection

Thermal-overload protection limits the total power dissipation in the IC. When the junction temperature exceeds +165°C (typ), an internal thermal sensor shuts down the internal bias regulator and the step-down controller, allowing the IC to cool. The thermal sensor turns on the IC again after the junction temperature cools by 15°C.

Application Information

Input Capacitors

The input filter capacitor reduces peak currents drawn from the power source and reduces noise and voltage ripple on the input caused by the circuit's switching. A 4.7µF X7R ceramic capacitor is recommended for the boost inductor input and the PV2 pin. A 1.0µF X7R ceramic capacitor is recommended for the PV pin, with PV connected to the same supply as PV2 through a 10Ω resistor.

Inductor Selection

Three key inductor parameters must be specified for operation with the IC: inductance value (L), peak inductor current (I_{PEAK}), and inductor saturation current (I_{SAT}). The minimum required inductance is a function of operating frequency, input-to-output voltage differential, and the maximum output current capability of the output. A lower inductor value minimizes size and cost, improves large-signal and transient response, but reduces efficiency due to higher peak currents and higher peak-to-peak output-voltage ripple for the same output capacitor. On the other hand, higher inductance increases efficiency by reducing the ripple current. Resistive losses due to extra wire turns can exceed the benefit gained from lower ripple current levels, especially when the inductance is increased without also allowing for larger inductor dimensions. The MAX20414 is designed for ΔI_{P-P} equal to ~30% of the full load current. Use the following equation to calculate the inductance:

$$L_{MIN1} = \frac{(V_{IN} - V_{OUT\_}) \times V_{OUT}}{V_{IN} \times f_{SW} \times I_{MAX} \times 30\%}$$

V_{IN} and V_{OUT} are typical values so that efficiency is optimum for typical conditions. The switching frequency (f_{SW}) is 2.2MHz. The maximum output capability (I_{MAX}) is 1A, 2A, or 3A based on the specific part number of the device. See the *Buck Output Capacitor* section to verify that the worst-case output ripple is acceptable. The inductor saturation current is also important to avoid runaway current during continuous output short circuit.

The next equation ensures that the inductor current downslope is less than the internal slope compensation. For this to be the case the following equation needs to be satisfied:

$$-m \geq \frac{m2}{2}$$

where:

m2	The inductor current downslope. $\frac{V_{OUT}}{L} \times R_{CS}$
-m	Slope Compensation. $\left[0.940 \frac{V}{\mu s}\right]$ for V_{OUT} > 3.2V fixed output $\left[0.535 \frac{V}{\mu s}\right]$ for V_{OUT} ≤ 3.2V fixed output or adjustable output version
R_{CS}	0.378Ω for 1A channel 0.263Ω for 2A channel 0.176Ω for 3A channel

Solving for L and adding a 1.3 multiplier to account for tolerances in the system:

$$L_{MIN2} = V_{OUT} \times \frac{R_{CS}}{2 \times m} \times 1.3$$

To satisfy both, L_{MIN1} and L_{MIN2} must be set to the larger of the two:

$$L_{MIN} = \max(L_{MIN1}, L_{MIN2})$$

The maximum inductor value recommended is 2 times the chosen value from the above formula:

$$L_{MAX} = 2 \times L_{MIN}$$

Select a nominal inductor value based on the following formula. For optimal performance, select the first standard inductor value greater than L_{MIN}:

$$L_{MIN} < L_{NOM} < L_{MAX}$$

Boost Output Capacitor

The IC is designed to be stable with low-ESR ceramic capacitors. Other capacitor types are not recommended as the ESR zero can affect stability of the device. The output capacitor calculations below are guidelines based on nominal conditions. The phase margin must be measured on the final circuit to verify that proper stability is achieved:

$$C_{OUT\_MIN} = \frac{50 \times A \times \mu s}{V_{OUT}}$$

$$C_{OUT1\_NOM} = \frac{100 \times A \times \mu s}{V_{OUT}}$$

Boost Output Current

The maximum output-current capability of OUT1 is dependent on the input current limit of the low side FET along with the V_{IN}/V_{OUT} ratio and efficiency. The maximum output current can be estimated based on the minimum input current limit of 1.6A. If the efficiency is not known, then it must be measured or estimated. A good estimate is 90% for V_{IN}/V_{OUT} ratios ≤ 1.5, and 80% for V_{IN}/V_{OUT} ratios of approximately 2.5.

$$I_{OUT1(MIN)} = \left(1.6A - \frac{\Delta I_L}{2}\right) \times (1 - D)$$

$$D = 1 - \frac{V_{IN}}{V_{OUT}} \times \text{Efficiency}$$

As an example the minimum output current boosting from 5V to 6.5V would be approximately:

$$I_{OUT1(MIN)} = \left(1.6A - \frac{0.2A}{2}\right) \times (1 - 0.303) = 1A$$

Assumptions:

Efficiency = 90.6%

L = 3.3µH, DCR = 35mΩ

Buck Output Capacitor

The IC is designed to be stable with low-ESR ceramic capacitors. Other capacitor types are not recommended as the ESR zero can affect stability of the device. The output capacitor calculations below are guidelines based on nominal conditions. The phase margin must be measured on the final circuit to verify proper stability is achieved:

$$C_{OUT2\_MIN} = 10.5\mu s \times \frac{I_{MAX}}{V_{OUT}}$$

$$C_{OUT2\_NOM} = 27.5\mu s \times \frac{I_{MAX}}{V_{OUT}}$$

With C_{OUT2_MIN} defining the minimum fully derated output capacitance required for a stable output and C_{OUT2_NOM} defining the nominal output capacitance for maximum phase margin. I_{MAX} is the maximum DC current capability of the associated output, as defined in the *Ordering Information*. V_{OUT} is the output voltage for the associated channel.

Ordering Information

PART	TEMPERATURE RANGE	PIN-PACKAGE	V_{OUT1} (V)	V_{OUT2} (V)	I_{OUT2} (A)	t_{HOLD} (ms)	SS
MAX20414ATGA/V+	-40°C to +125°C	24 TQFN-EP*	5.0	ADJ	3	7.4	Off
MAX20414ATGA/V+T	-40°C to +125°C	24 TQFN-EP*	5.0	ADJ	3	7.4	Off

Note: *For variants with different options, contact factory.*

/V denotes an automotive qualified part.
+Denotes a lead(Pb)-free/RoHS-compliant package.
**EP = Exposed pad.*
T = Tape and reel.

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	2/17	Initial release	—