Data Sheet

# MAX20363

PPG Optimized Buck-Boost Converter with 500mA Output Current and Ultra-Fast DVS Capability

## FEATURES

- Extend System Runtime
  - Ultra-fast dynamic voltage scaling with direct AFE control
  - Low, 2.5µA (typical) quiescent current
  - 96% peak efficiency
- Low, Continuous Noise Profile
  - No post-filtering LDO required in PPG systems
  - No discontinuities across operating voltage range
- Adaptable Load Transient Response
  - Fast load transient response minimizes AFE settling time
  - FAST mode pre-triggers load response and improves load transient

## APPLICATIONS

- Biometric Optical Sensing (example, PPG)

## GENERAL DESCRIPTION

The MAX20363 is an ultra-low quiescent current, non-inverting buck-boost converter with 500mA output current capability. The MAX20363 is intended for applications that require long run times while also demanding bursts of high current. The device employs a proprietary control algorithm that seamlessly transitions between buck, buck-boost, and boost modes, minimizing discontinuities and subharmonics in the output voltage ripple. The low 1.8V input voltage allows the device to be powered from a variety of sources such as lithium ion rechargeable and lithium primary batteries. The MAX20363 is designed to minimize inductance and capacitance requirements to keep the overall solution size as small as possible.

The MAX20363 is optimized for powering optical photoplethysmogram (PPG) systems. The ultra-fast dynamic voltage scaling (DVS) capability allows the device to transition quickly between output voltages and enable in-frame scaling of LED supply voltage. Additionally, the low output ripple and fast, predictable transient response maximizes the signal-to-noise ratio (SNR) of high-performance optical PPG analog-front-end (AFE).

The MAX20363 is available in an 18-bump, 2.43mm x 1.25mm WLP package, with 0.4mm pitch.



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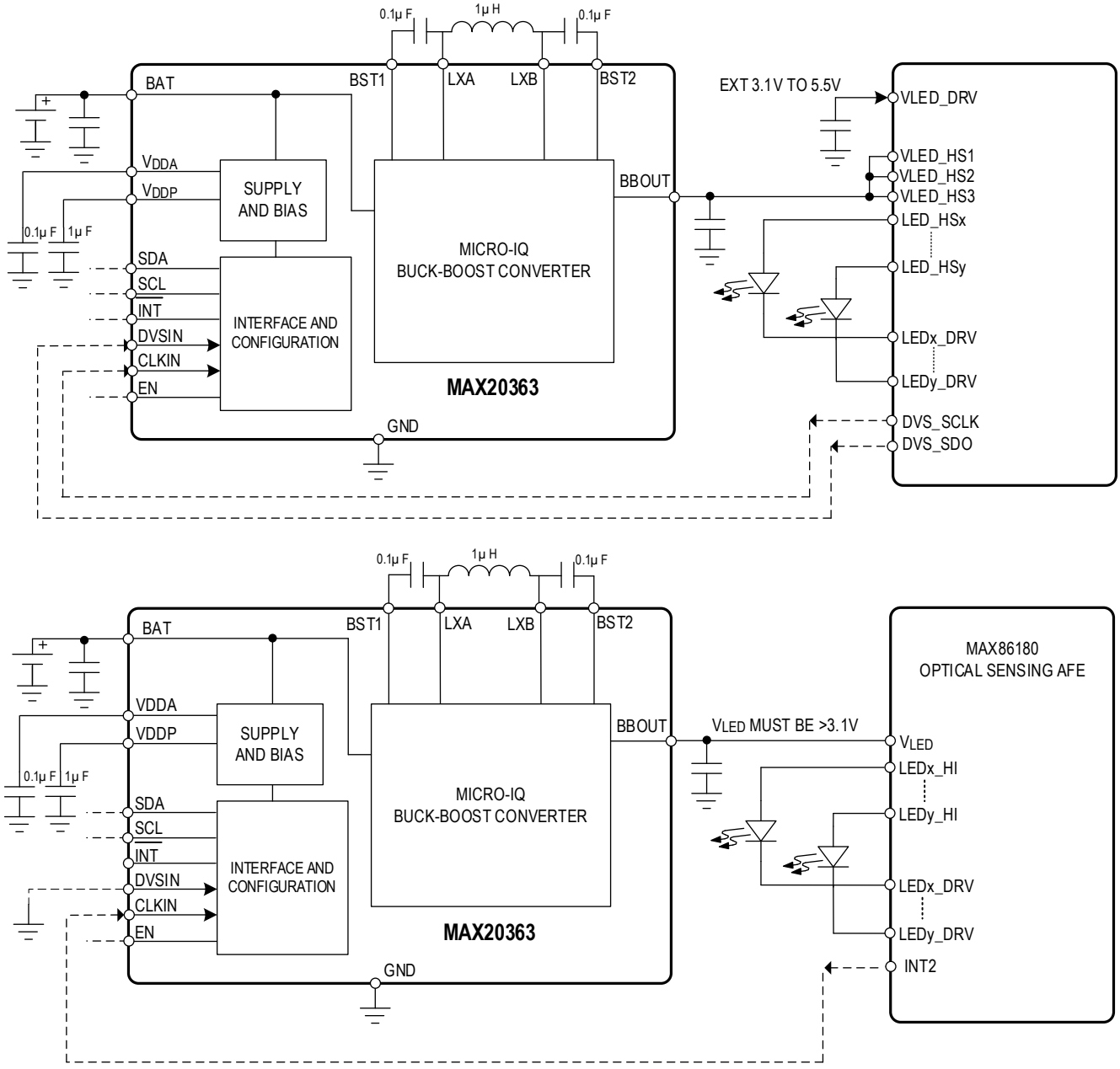
## SIMPLIFIED APPLICATION DIAGRAM



# SPECIFICATIONS

## Table 1. Electrical Characteristics

($V_{BAT}$ = +1.8V to +5.5V, $C_{BAT\_EFF}$ = 5µF, $C_{BBOUT\_EFF}$ = See *Figure 34*, $T_A$ = -40°C to +85°C, unless otherwise noted. Typical values are at $T_A$ = +25°C, $V_{BAT}$ = +3.7V, L = 1µH, limits are 100% tested at $T_A$ = +25°C.) (Note 1))

| PARAMETER | SYMBOL | CONDITIONS/COMMENTS | | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|---|
| Input Voltage Range | $V_{BAT}$ | | | 1.8 | | 5.5 | V |
| Quiescent Supply Current | $I_Q$ | No load, $V_{BBOUT}$ = 5V, $V_{BAT}$ = 3.7V, (Note 2) | | | 2.5 | | µA |
| | $I_{Q\_ROOM}$ | No load, $V_{BBOUT}$ = 5V, $V_{BAT}$ = 3.7V (Note 2), $T_A$ = 25°C | | | | 6 | µA |
| | $I_{Q\_FAST}$ | No load, $V_{BBOUT}$ = 5V, $V_{BAT}$ = 3.7V (Note 2) | FAST = 1 | | 75 | | µA |
| | $I_{Q\_FPWM}$ | No load, $V_{BBOUT}$ = 5V, $V_{BAT}$ = 3.7V | FPWM = 1, L = 1µH (DFE201210U1R0M) | | 11 | | mA |
| Shutdown Supply Current | $I_{SHDN}$ | EN = 1, Disabled by $I^2C$ | | | 1.2 | | µA |
| | | EN = 0 | | | 0.1 | | µA |
| Maximum Output Current | $I_{BBOUT\_MAX}$ | $V_{BAT}$ ≥ 2.5V, 1.5V ≤ $V_{BBOUT}$ ≤ 5.0V | BBFetScale = 00, L = 1µH (DFE201210U-1R0M), BBL2P2Sel = 0, $C_{BBOUT\_EFF}$ = refer to *Figure 34*, $I_{PSET1}$ = default, $I_{PSET2}$ = 300mA, Load Reg ≥ -7.5% | 500 | | | mA |
| | | | BBFetScale = 01 or 10, L = 1µH (DFE201210U-1R0M), BBL2P2Sel = 0, $C_{BBOUT\_EFF}$ = 1/2 of that shown in *Figure 34*, $I_{PSET1}$ = default, $I_{PSET2}$ = | 250 | | | mA |

($V_{BAT}$ = +1.8V to +5.5V, $C_{BAT\_EFF}$ = 5µF, $C_{BBOUT\_EFF}$ = See *Figure 34*, $T_A$ = -40°C to +85°C, unless otherwise noted. Typical values are at $T_A$ = +25°C, $V_{BAT}$ = +3.7V, L = 1µH, limits are 100% tested at $T_A$ = +25°C.) (Note 1))

| PARAMETER | SYMBOL | CONDITIONS/COMMENTS | | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|---|
| | | | 300mA, Load Reg ≥ -7.5% | | | | |
| | | | BBFetScale = 11, L = 1µH (DFE201210U-1R0M), BBL2P2Sel = 0 $C_{BBOUT\_EFF}$ = ¼ of that shown in *Figure 34*, $I_{PSET1}$ = default, $I_{PSET2}$ = 300mA, Load Reg ≥ -7.5% | 125 | | |
| | | $V_{BAT}$ ≥ 2.0V, 1.5V ≤ $V_{BBOUT}$ ≤ 5.0V | BBFetScale = 00, L = 1µH (DFE201210U-1R0M), BBL2P2Sel = 0, $C_{BBOUT\_EFF}$ = refer to *Figure 34*, $I_{PSET1}$ = default, $I_{PSET2}$ = 300mA, Load Reg ≥ -7.5% | 350 | | | |
| Output Voltage Set Range | $V_{BBOUT}$ | 50mV step resolution | | | 1.5 to 5.5 | | V |
| Average Output-Voltage Accuracy | ACC_OUT | $I_{BBOUT}$ = 10mA, FAST = 1, BBL2P2Sel = 0, L = 1µH (DFE201210U-1R0M), $I_{PSET1}$ = default, $I_{PSET2}$ = 300mA, $C_{BBOUT\_EFF}$ = 20µF | | -1 | | +2.5 | % |
| | | $I_{BBOUT}$ = 10mA, FAST = 0, BBL2P2Sel = 0, L = 1µH (DFE201210U-1R0M), $I_{PSET1}$ = default, $I_{PSET2}$ = 300mA, $C_{BBOUT\_EFF}$ = 20µF | | -0.5 | | +3 | |
| Line Regulation Error | $V_{LINE\_REG}$ | $I_{BBOUT}$ = 50mA, $C_{BBOUT\_EFF}$ = 20µF | | -1 | | +1 | %/V |
| Load Regulation Error | $V_{LOAD\_REG}$ | $V_{BAT}$ = 3.7V, $V_{BBOUT}$ = 5V, $I_{BBOUT}$ = 500mA, BBFetScale = 00, $C_{BBOUT}$ = refer to *Figure 34*, $I_{PSET1}$ = default, $I_{PSET2}$ = | | | -2.5 | | % |

($V_{BAT}$ = +1.8V to +5.5V, $C_{BAT\_EFF}$ = 5µF, $C_{BBOUT\_EFF}$ = See *Figure 34*, $T_A$ = -40°C to +85°C, unless otherwise noted. Typical values are at $T_A$ = +25°C, $V_{BAT}$ = +3.7V, L = 1µH, limits are 100% tested at $T_A$ = +25°C.) (Note 1))

| PARAMETER | SYMBOL | CONDITIONS/COMMENTS | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|
| | | 300mA, BBL2P2Sel = 0, L = 1µH (DFE201210U-1R0M) | | | | |
| | | $V_{BAT}$ = 3.7V, $V_{BBOUT}$ = 5V, $I_{BBOUT}$ = 250mA, BBFetScale = 01 or 10, $C_{BBOUT}$ = 1/2 of that shown in *Figure 34*, $I_{PSET1}$ = default, $I_{PSET2}$ = 300mA, BBL2P2Sel = 0, L = 1µH (DFE201210U-1R0M) | | -2.0 | | |
| | | $V_{BAT}$ = 3.7V, $V_{BBOUT}$ = 5V, $I_{BBOUT}$ = 125mA, BBFetScale = 11, $C_{BBOUT}$ = ¼ of that shown in *Figure 34*, $I_{PSET1}$ = default, $I_{PSET2}$ = 300mA, BBL2P2Sel = 0, L = 1µH (DFE201210U-1R0M) | | -2.0 | | |
| Line Transient Response | $V_{LINE\_TRAN}$ | $V_{BBOUT}$ = 3.4V, $V_{BAT}$ from 3.4V to 2.9V, 1µs fall time, $I_{LOAD}$ = 1mA, $C_{BBOUT}$ = refer to *Figure 34* | | 20 | | mV |
| Load Transient Response | $V_{LOAD\_TRAN}$ | $V_{BBOUT}$ = 5V, $V_{BAT}$ = 3.7V, $I_{LOAD}$ = 10µA to 300mA, $I_{PSET1}$ = default, $I_{PSET2}$ = 300mA, BBL2P2Sel = 0, L = 1µH (DFE201210U-1R0M), $C_{BBOUT}$ = refer to *Figure 34* | | 80 | | mV |
| Programmable Inductor Valley Current Limit During Startup | $I_{IVLY\_STUP}$ | BBIPwpMaxP<br>50mA steps | | 0 to 750 | | mA |
| Maximum Output Load Current during Start Up | $I_{PWR\_MAX\_STUP}$ | $V_{BAT}$ > 2.5V, $I_{PSET1}$ = default, $I_{PSET2}$ = 300mA, $I_{VLY\_STUP}$ min setting (BBIPwpMaxP = 0) | | 40 | | mA |
| Startup Time | $t_{STARTUP}$ | Time from enable (BBstEna = 1, EN goes high) to final value. $V_{BAT}$ > 2.5V, $I_{PSET1}$ = default, $I_{PSET2}$ = 300mA, $I_{LOAD}$ = 0, $I_{IVLY\_STUP}$ = 150mA, $C_{BBOUT}$ = refer to *Figure 34* | | 10 | | ms |
| Nominal Valley Inductor Current Limit Range | $I_{VLY\_LIM}$ | BBFetScale = 00, 50mA steps | | 0 to 1600 | | mA |
| | | BBFetScale = 01 or 10, 25mA steps | | 0 to 800 | | |
| | | BBFetScale = 11, 12.5mA steps | | 0 to 400 | | |

($V_{BAT}$ = +1.8V to +5.5V, $C_{BAT\_EFF}$ = 5µF, $C_{BBOUT\_EFF}$ = See *Figure 34*, $T_A$ = -40°C to +85°C, unless otherwise noted. Typical values are at $T_A$ = +25°C, $V_{BAT}$ = +3.7V, L = 1µH, limits are 100% tested at $T_A$ = +25°C.) (Note 1))

| PARAMETER | SYMBOL | CONDITIONS/COMMENTS | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|
| Nominal Falling Dynamic Voltage Scaling Valley Inductor Current Limit Range | $I_{DVSF}$ | BBFetScale = 00, 50mA steps | | -200 to -1800 | | mA |
| | | BBFetScale = 01 or 10, 25mA steps | | -200 to -1000 | | |
| | | BBFetScale = 11, 12.5mA steps | | -100 to -500 | | |
| Active Discharge Current | $I_{ACTD}$ | Applied on BBOUT for 50ms after shutdown if BBstActDsc = 1 | | 20 | | mA |
| Passive Discharge Resistance | $R_{PSVD}$ | Applied on BBOUT after shutdown, if BBstPsvDsc = 1 or EN is low | | 1.3 | | kΩ |
| Output UVLO | $V_{OUT\_UVLO\_F}$ | $V_{BBOUT}$ falling | 1 | 1.1 | | V |
| | $V_{OUT\_UVLO\_R}$ | $V_{BBOUT}$ rising | | 1.13 | 1.25 | |
| VDDA UVLO | $V_{VDDA\_UVLO\_R}$ | $V_{VDDA}$ rising | | 1.658 | 1.7 | V |
| | $V_{VDDA\_UVLO\_F}$ | $V_{VDDA}$ falling | 1.6 | 1.642 | | |
| LXA, LXB Leakage | $I_{LX\_LKG}$ | EN is low | | | 2.5 | µA |
| BST1, BST2 Leakage | $I_{BST\_LKG}$ | EN is low | | | 4.5 | µA |
| BBOUT Leakage | $I_{BBOUT\_LKG}$ | EN is high and BBstEna = 0 | | | 1 | µA |
| **DIGITAL** | | | | | | |
| SDA, SCL, EN, $\overline{INT}$, DVSIN, CLKIN Input Leakage Current | $I_{LK\_IO}$ | | -1 | | +1 | µA |
| SDA, SCL, EN, DVSIN, CLKIN Input Logic High | $V_{IO\_IH}$ | | 1.4 | | | V |
| SDA, SCL, EN, DVSIN, CLKIN Input Logic Low | $V_{IO\_IL}$ | | | | 0.4 | V |
| $\overline{INT}$ Output Logic Low | $V_{IO\_OL\_INT}$ | $I_{OL}$ = 4mA | | | 0.4 | V |
| SDA Output Logic Low | $V_{IO\_OL\_SDA}$ | $I_{OL}$ = 20mA | | | 0.4 | V |
| SCL Clock Frequency | $f_{SCL}$ | | 0 | | 1 | MHz |

($V_{BAT}$ = +1.8V to +5.5V, $C_{BAT\_EFF}$ = 5µF, $C_{BBOUT\_EFF}$ = See *Figure 34*, $T_A$ = -40°C to +85°C, unless otherwise noted. Typical values are at $T_A$ = +25°C, $V_{BAT}$ = +3.7V, L = 1µH, limits are 100% tested at $T_A$ = +25°C.) (Note 1))

| PARAMETER | SYMBOL | CONDITIONS/COMMENTS | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|
| Bus Free Time Between STOP and START Condition | $t_{BUF}$ | | 0.5 | | | µs |
| START Condition (Repeated) Hold Time | $t_{HD\_STA}$ | | 0.26 | | | µs |
| Low Period of SCL Clock | $t_{LOW}$ | | 0.5 | | | µs |
| High Period of SCL Clock | $t_{HIGH}$ | | 0.26 | | | µs |
| Setup Time for a Repeated START Condition | $t_{SU\_STA}$ | | 0.26 | | | µs |
| Data Hold Time | $t_{HD\_DAT}$ | | 0 | | | µs |
| Data Setup Time | $t_{SU\_DAT}$ | | 50 | | | ns |
| Setup Time for STOP Condition | $t_{SU\_STO}$ | | 0.26 | | | µs |
| Spike Pulse Widths Suppressed by Input Filter | $t_{SP}$ | | | 50 | | ns |
| DATA Valid Time | $t_{VD\_DAT}$ | | | | 450 | ns |
| DATA Valid Ack Time | $t_{VD\_ACK}$ | | | | 450 | ns |
| **SPI** | | | | | | |
| CLKIN Frequency | $f_{CLKIN}$ | | | | 20 | MHz |
| DVSIN Setup Time | $t_{DS}$ | | 10 | | | ns |
| DVSIN Hold Time | $t_{DH}$ | | 20 | | | ns |
| CLKIN Pulse Width Low | $t_{LOW\_SPI}$ | | 20 | | | ns |
| CLKIN Pulse Width High | $t_{HIGH\_SPI}$ | | 20 | | | ns |

[1] All devices are 100% production tested at $T_A$ = +25°C. Limits over the operating temperature range are guaranteed by design.

[2] Quiescent current specification is guaranteed only down to 1.9V

# ABSOLUTE MAXIMUM RATINGS

**Table 2. Absolute Maximum Ratings**

| PARAMETER | RATING |
|---|---|
| BAT, BBOUT, SDA, SCL, EN, CLKIN, DVSIN | −0.3V to +6.0V |
| $\overline{INT}$ | −0.3V to 12V |
| LXA | −0.3V to Min ( $V_{BAT}$ + 0.3V, +6.0V) |
| LXB | −0.3V to Min ( $V_{BBOUT}$ + 0.3V, +6.0V) |
| $V_{DDP}$ | -0.3V to 2.2V |
| $V_{DDA}$ | Max (-0.3V, $V_{DDP}$ − 0.1V) to Min (2.2V, $V_{DDP}$ + 0.1V) |
| BST1 | Max ($V_{DDP}$ − 0.3V, $V_{LXA}$ − 0.3V) to Min ($V_{LXA}$ +2.2V, $V_{DDP}$ +7.5V) |
| BST2 | Max ($V_{DDP}$ − 0.3V,$V_{LXB}$ − 0.3V) to Min ($V_{LXB}$ + 2.2V, $V_{DDP}$ + 7.5V) |
| Current into BAT, LXA, LXB (10% utilization for 100k hours) | ±1.6A |
| Current into BBOUT (10% utilization for 100k hours) | ±600mA |
| Continuous Current into Any Other Terminal | ±100mA |
| Continuous Power Dissipation (Multilayer Board, $T_A$ = +70°C) (derate 17.63mW/°C above +70°C) | 1410.72mW |
| Junction Temperature | +150°C |
| Storage Temperature Range | −40°C to +150°C |
| Soldering Temperature (reflow) | +260°C |

Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

## Thermal Resistance

Thermal performance is directly linked to PCB design and operating environment. Close attention to PCB thermal design is required.

| Package Type | $\theta_{JA}$ | Unit |
|---|---|---|
| W181A2+1 | 56.71 | °C/W |

## Electrostatic Discharge (ESD)

The following ESD information is provided for handling of ESD-sensitive devices in an ESD protected area only Human body model (HBM) per ANSI/ESDA/JEDEC JS-001 Field induced charged device model (FICDM) and charged device model (CDM) per ANSI/ESDA/JEDEC JS-002. International Electrotechnical Commission (IEC) electromagnetic compatibility: Part 4-2 (IEC) per IEC 61000-4-2. Machine model (MM) per ANSI/ESD STM5.2. MM voltage values are for characterization only.

## ESD Ratings

**Table 3. MAX20363**

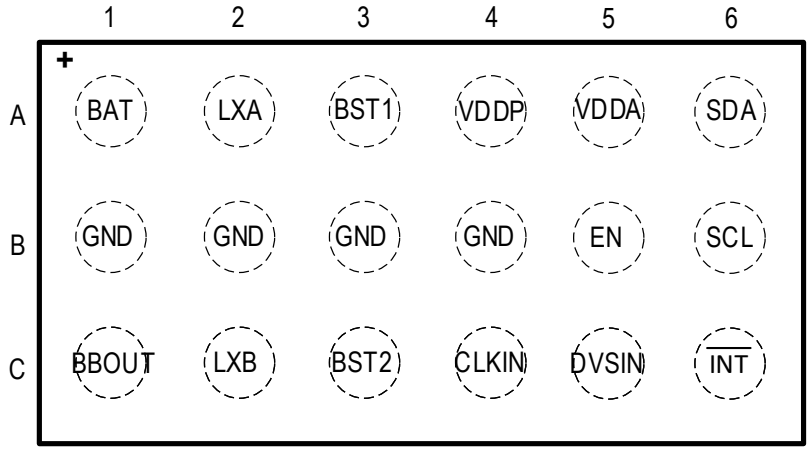
| ESD Model | Withstand Threshold (V) | Class |
|---|---|---|
| HBM | ±2500 | 2 |

## ESD Caution

**ESD (electrostatic discharge) sensitive device.** Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

# PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS

TOP VIEW
(BUMP SIDE DOWN)




18-bump, 0.4mm WLP
(1.25mm x 2.43mm)

**Table 4.** Pin Descriptions

| PIN | NAME | DESCRIPTION |
|---|---|---|
| A1 | BAT | Input Supply. Bypass to GND with effective capacitance at least the maximum between 5µF and the value of the derating curve (*Figure 34*) for a bias voltage $V_{BAT}$, placed as close to the device as possible. |
| A2 | LXA | Switching Node A. Connect through 1µH or 2.2µH inductor to LXB. |
| A3 | BST1 | Boostrap Cap 1. Connect through 100nF capacitor to LXA, placed as close to the device as possible. |
| A4 | $V_{DDP}$ | 1.8V regulator output voltage. Bypass with 1µF capacitor to GND, placed as close to the device as possible. Do not externally load the VDDP pin. |
| A5 | $V_{DDA}$ | 1.8V analog output supply. Internally connected to VDDP through 20 ohm resistance. Bypass with 100nF capacitor to GND, placed as close to the device as possible. Do not externally load the VDDA pin. |
| A6 | SDA | $I^2C$ Serial Data Input/Open-Drain Output. Connect to GND when not in use. |
| B1, B2, B3, B4 | GND | Ground |
| B5 | EN | Enable. Active-high. |
| B6 | SCL | $I^2C$ Serial Clock Input. Connect to GND when not in use. |
| C1 | BBOUT | Buck Boost Output. Bypass to ground with effective capacitance shown in *Figure 34*, place as close to the device as possible. Refer to Input and Output Capacitance section for detail. |
| C2 | LXB | Switching Node B. Connect through 1µH or 2.2µH inductor to LXA. |

| | | |
|---|---|---|
| C3 | BST2 | Boostrap Cap 2. Connect through 100nF capacitor to LXB, placed as close to the device as possible. |
| C4 | CLKIN | Dedicated SPI Clock Input. Connect to GND when not in use. |
| C5 | DVSIN | Dedicated SPI DVS Input. Connect to GND when not in use. |
| C6 | $\overline{INT}$ | Interrupt Open-Drain Output. Active low. Externally connect through pullup resistor to system logic supply. |

# TYPICAL PERFORMANCE CHARACTERISTICS

($V_{BAT}$ = +3.7V, $C_{BAT}$ = $C_{BBOUT}$ = 22µF, refer to *Figure 34* single capacitor derating, L = 1µH, BBstLowEMIB = 1, BBstIpPadPEnb = 0, BBFetScale = 0, $T_A$ = +25°C, unless otherwise noted.)

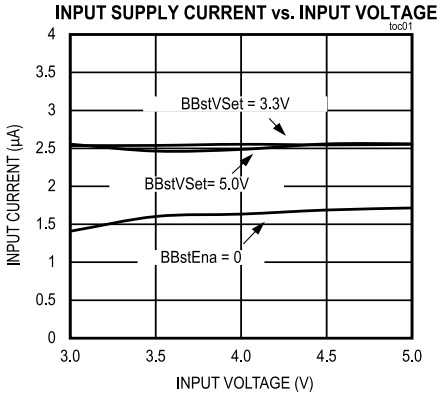



*Figure 1. Input Supply Current vs. Input Voltage*

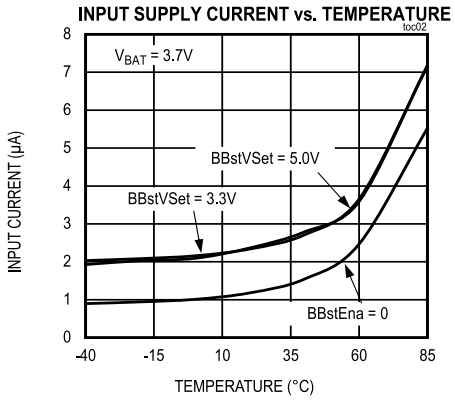



*Figure 2. Input Supply Current vs. Temperature*

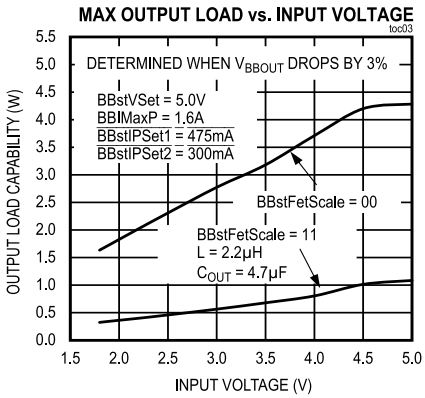



*Figure 3. Max Output Load vs. Input Voltage*

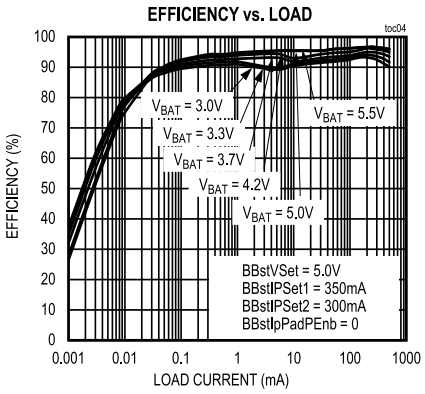



*Figure 4. Efficiency vs. Load*

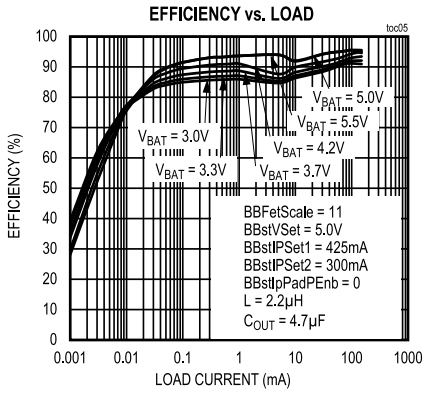



*Figure 5. Efficiency vs. Load*

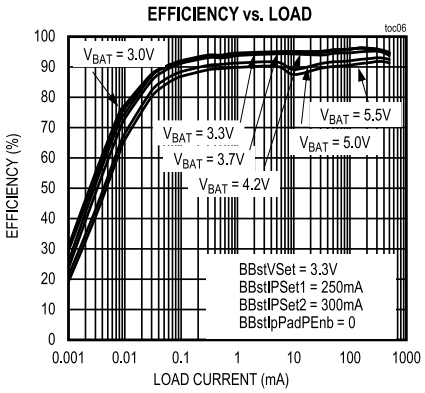



*Figure 6. Efficiency vs. Load*

($V_{BAT}$ = +3.7V, $C_{BAT}$ = $C_{BBOUT}$ = 22µF, refer to *Figure 34* single capacitor derating, L = 1µH, BBstLowEMIB = 1, BBstIpPadPEnb = 0, BBFetScale = 0, $T_A$ = +25°C, unless otherwise noted.)

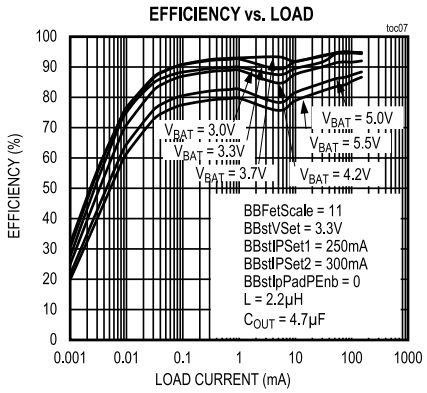



*Figure 7. Efficiency vs. Load*

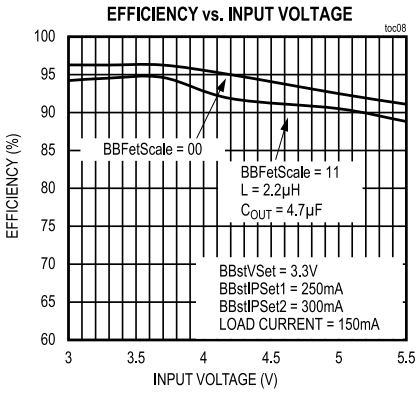



*Figure 8. Efficiency vs. Input Voltage*

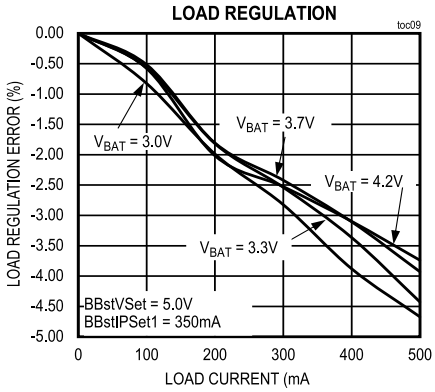



*Figure 9. Load Regulation*

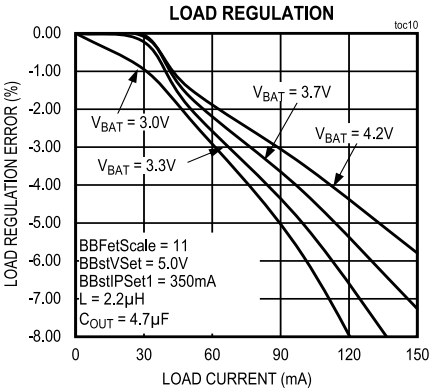



*Figure 10. Load Regulation*

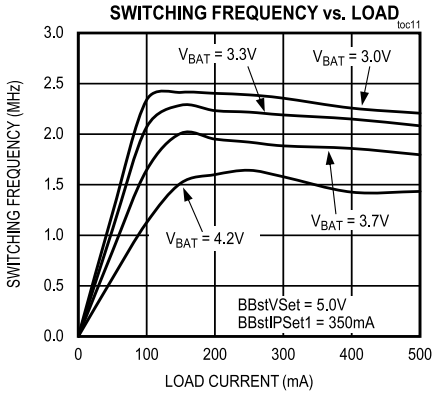



*Figure 11. Switching Frequency vs. Load*

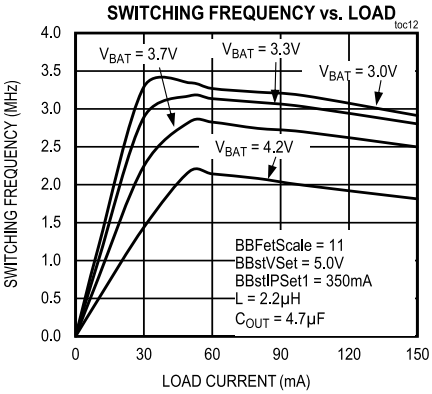



*Figure 12. Switching Frequency vs. Load*

($V_{BAT}$ = +3.7V, $C_{BAT}$ = $C_{BBOUT}$ = 22µF, refer to *Figure 34* single capacitor derating, L = 1µH, BBstLowEMIB = 1, BBstIpPadPEnb = 0, BBFetScale = 0, $T_A$ = +25°C, unless otherwise noted.)

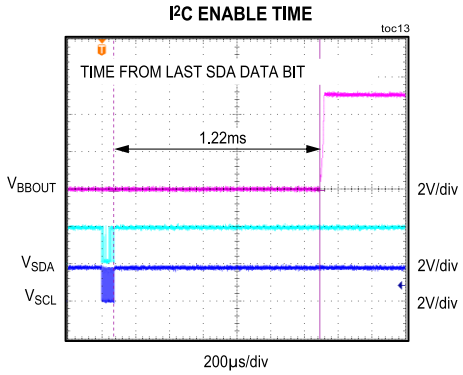



*Figure 13. I²C Enable Time*

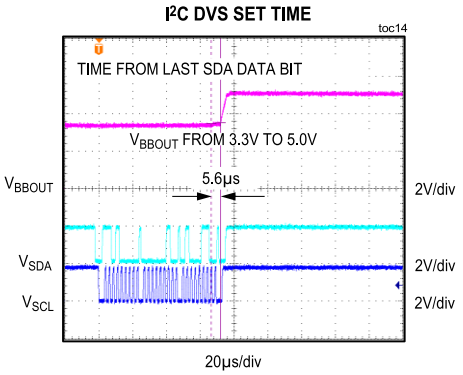



*Figure 14. I²C DVS Set Time*

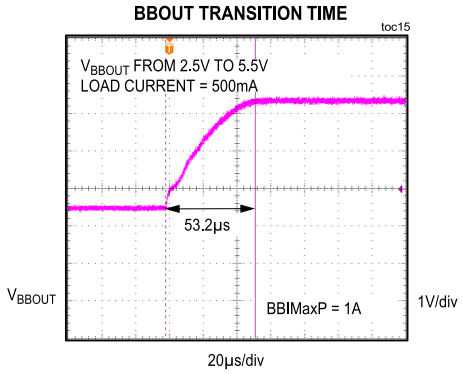



*Figure 15. BBOUT Transition Time*

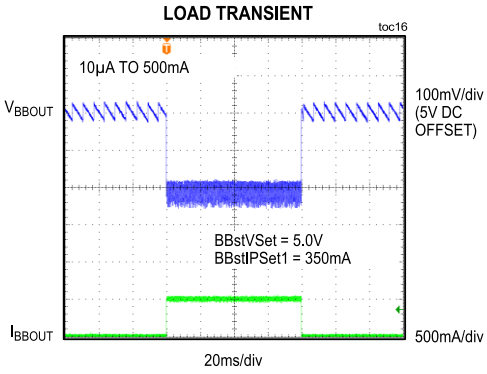



*Figure 16. Load Transient*

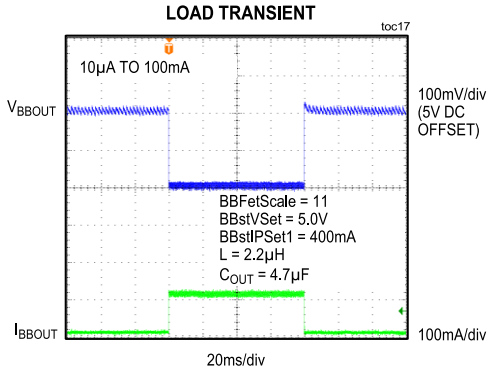



*Figure 17. Load Transient*

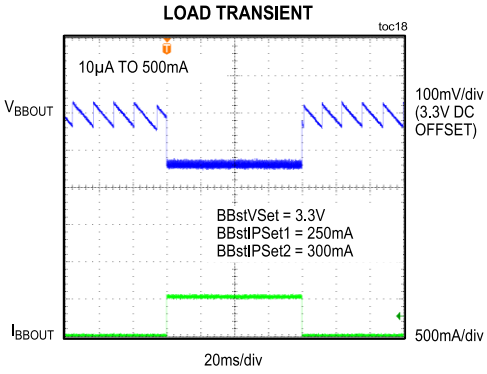



*Figure 18. Load Transient*

($V_{BAT}$ = +3.7V, $C_{BAT}$ = $C_{BBOUT}$ = 22µF, refer to *Figure 34* single capacitor derating, L = 1µH, BBstLowEMIB = 1, BBstIpPadPEnb = 0, BBFetScale = 0, $T_A$ = +25°C, unless otherwise noted.)

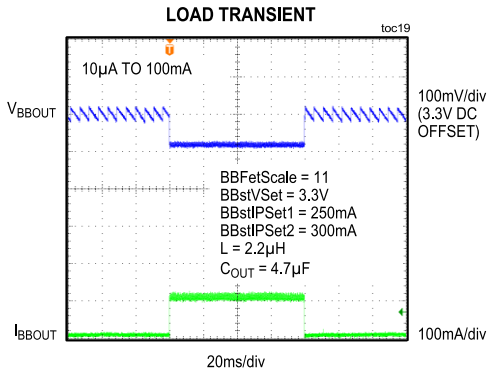



*Figure 19. Load Transient*

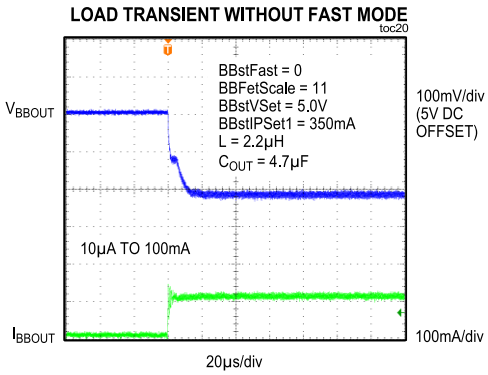



*Figure 20. Load Transient without Fast Mode*

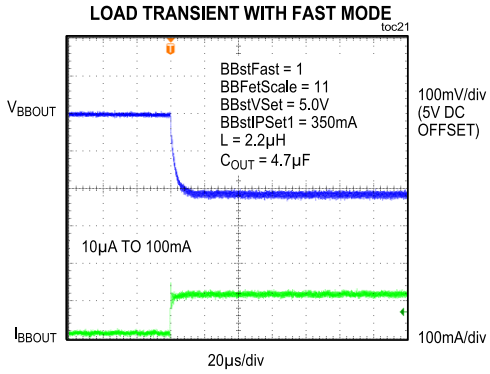



*Figure 21. Load Transient with Fast Mode*

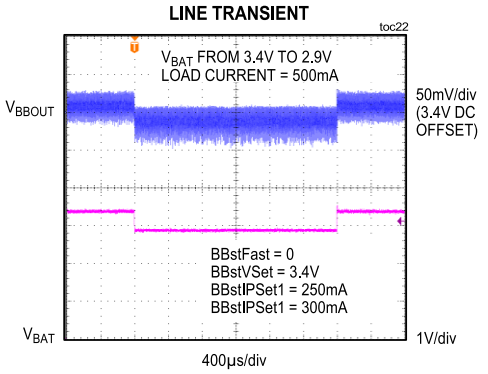



*Figure 22. Line Transient*

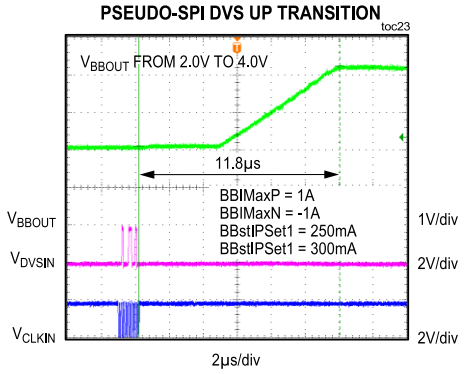



*Figure 23. Pseudo-SPI DVS Up Transition*

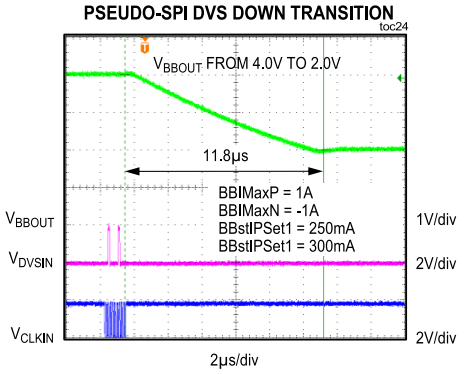



*Figure 24. Pseudo-SPI DVS Down Transition*

($V_{BAT}$ = +3.7V, $C_{BAT}$ = $C_{BBOUT}$ = 22µF, refer to *Figure 34* single capacitor derating, L = 1µH, BBstLowEMIB = 1, BBstIpPadPEnb = 0, BBFetScale = 0, $T_A$ = +25°C, unless otherwise noted.)

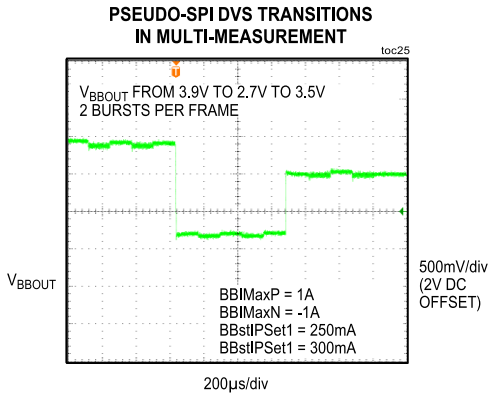



*Figure 25. Pseudo-SPI DVS Transitions in Multi-Measurement*

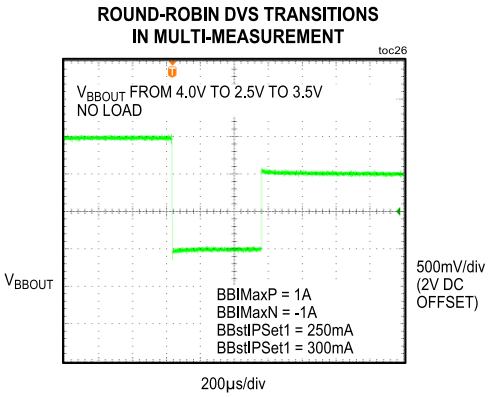



*Figure 26. Round-Robin DVS Transitions in Multi-Measurement*

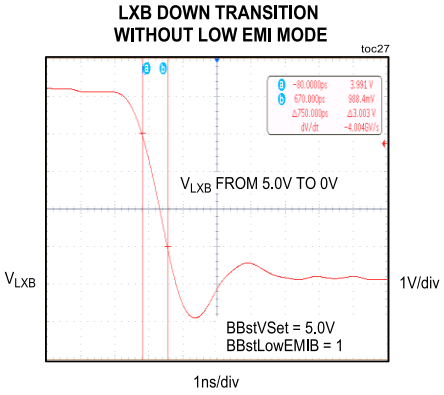



*Figure 27. LXB Down Transition without Low EMI Mode*

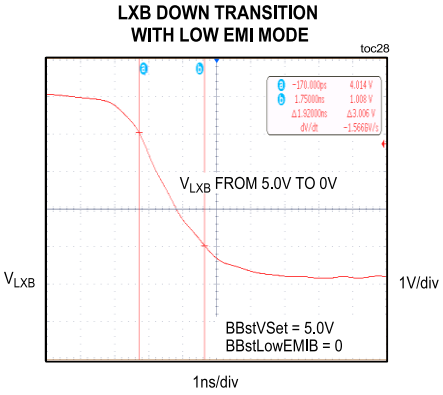



*Figure 28. LXB Down Transition with Low EMI Mode*

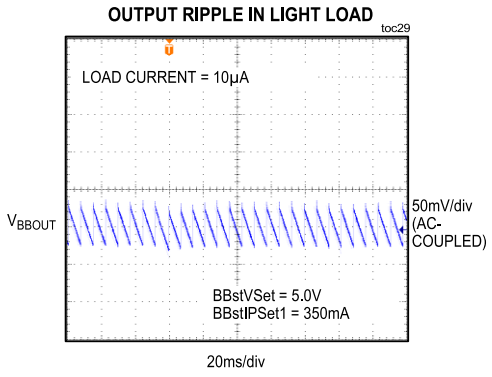



*Figure 29. Output Ripple in Light Load*

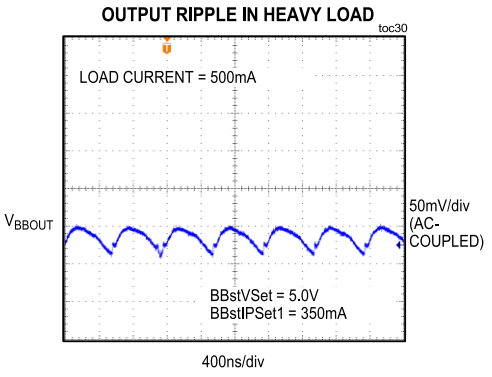



*Figure 30. Output Ripple in Heavy Load*

# THEORY OF OPERATION

The MAX20363 is an ultra-low quiescent current, non-inverting buck-boost converter with 500mA output current capability. The MAX20363 is intended for applications that require long run times while also demanding bursts of high current. The device employs a proprietary control algorithm that seamlessly transitions between buck, buck-boost, and boost modes, minimizing discontinuities and subharmonics in the output voltage ripple. The low 1.8V input voltage allows the device to be powered from a variety of sources such as lithium ion rechargeable and lithium primary batteries. The MAX20363 is designed to minimize inductance and capacitance requirements to keep the overall solution size as small as possible.

The MAX20363 is optimized for powering optical PPG systems. The ultra-fast dynamic voltage scaling (DVS) capability allows the device to transition quickly between output voltages and enable in-frame scaling of LED supply voltage. Additionally, the low output ripple and fast, predictable transient response maximizes the SNR of high-performance optical PPG AFEs.

## Architectural Description

*Figure 31* illustrates the basic structure of the MAX20363 switching regulator with arrows depicting the inductor current flow in each switching phase.

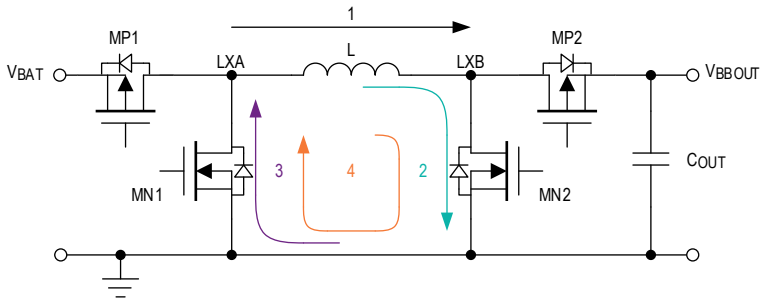



*Figure 31. The Buck-Boost Regulator and Switching Phases*

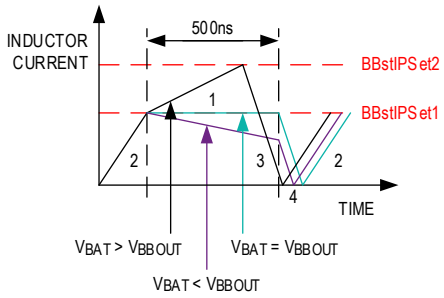



*Figure 32. Buck-Boost Inductor Current in Buck-Boost Mode*

### Switching Phases

Depending on the buck-boost configurations, the topology enters different sequences of phases to generate the desired output voltage. Only two switches are on in each phase.

- Phase 1: MP1 on, MP2 on. Inductor charges.
- Phase 2: MP1 on, MN2 on. Inductor charges.

- Phase 3: MN1 on, MP2 on. Inductor discharges.
- Phase 4: MN1 on, MN2 on. Freewheeling.

## Buck-Boost Mode

The regulator operates in buck-boost mode. The inductor charges in Phase 2 up to BBstIPSet1. The buck-boost then transitions to Phase 1. If $V_{BAT} > V_{BBOUT}$, BBstIPSet1 is gradually reduced to 0 and the inductor charges until either the current reaches BBstIPSet2 or after a 500ns delay. If $V_{BAT} \le V_{BBOUT}$, the buck-boost waits for the 500ns timeout to elapse or until the current drops to the valley limit. Next, the regulator enters Phase 3 to discharge the inductor current to the valley limit. When the inductor current reaches the valley-current crossing threshold or falls below 0, the regulator freewheels in Phase 4 until the next charge phase. When operating in continuous conduction mode (CCM), the buck-boost enters Phase 4 for approximately 30ns. *Figure 32* shows the inductor current in buck-boost mode.

## Inductor Peak and Valley Current Limits

The buck-boost regulator monitors the maximum and minimum values of the inductor current. If BBstIpPadPEnb = 1, the peak currents are fixed to the values in BBstISet and the valley current is fixed to 0mA. If BBstIpPadPEnb = 0, the peak and valley currents are allowed to change based on load requirements.

Peak currents are set in the BBstISet register. BBstIPSet1 controls the peak current when $V_{BAT} < V_{BBOUT}$ and begins the timeout period for Phase 1. BBstIPSet2 sets a secondary current limit in buck-boost mode when $V_{BAT} > V_{BBOUT}$. The buck-boost regulator transitions from Phase 1 to Phase 3 if the inductor current reaches BBstIPSet2 or if the 500ns timeout has elapsed. The MAX20363 gradually reduce BBstIPSet1 in such a way that when BBstIPSet2 is reached, the BBstIPSet1 is 0. Minimizing the settings of BBstIPSet1 and BBstIPSet2 reduces the output ripple but decreases efficiency. Care must be taken to optimize the peak current settings to keep a low output ripple while maximizing efficiency. Minimum BBstIPSet2 should never be lower than 200mA to avoid unwanted behavior. *Figure 33* is a graphical guide to selecting combinations of BBstIPSet1 and BBstIPSet2 to balance efficiency for specific BBstVSet values.

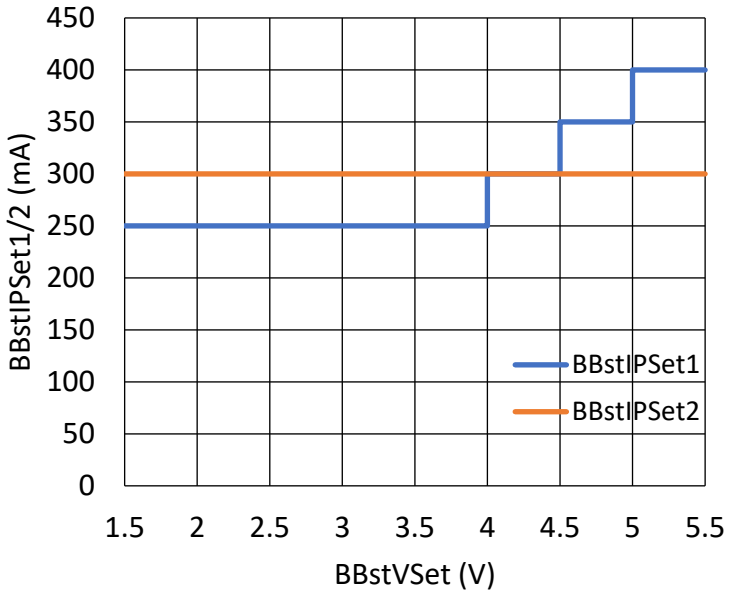



*Figure 33. Recommended BBstIPSet1 and BBstIPSet2 Settings*

To control inrush current during start-up, the MAX20363 startup valley current is limited through BBIPwpMaxP. The peak current is BBIPwpMaxP + max(BBstIPSet1,BBstIPSet2) settings. Once the output reaches its final voltage, the BBIMaxP setting is restored. See BBIPwpMaxP (*Table 5*) for device-specific values.

The MAX20363 behavior when BBstIPAdptDis = 0 can be further defined with a zero current comparator. The device transitions to Phase 4 when its control loop detects a zero current crossing.

## Dynamic Voltage Scaling

The MAX20363 utilizes dynamic voltage scaling (DVS) to rapidly change the output voltage on demand. DVS can significantly reduce the power consumption of PPG systems using LEDs with highly variable forward voltage drops.

DVS voltage transitions can be positive or negative going and the slew-rate of the output voltage is programmable through the positive and negative valley current limits (see $I^2C$ register descriptions.) The programmed valley current should account for the current source/sink capability of the input supply.

## Dynamic Voltage Scaling (DVS) Modes

The MAX20363 features three different DVS control modes:

- $I^2C$: In $I^2C$ mode, a dedicated register (BBstVset, register 0x02) in the regmap can be written with the voltage value required.
- Pseudo-SPI: Two dedicated pins (CLKIN, DVSIN) are used to implement a serial digital interface used to pass the DVS voltages and additional information; this mode requires the use of a compatible analog front end (AFE) device that features the DVS capability and pseudo-SPI controller, such as the Analog Devices MAX86181.
- Round-Robin: Up to 20 FPWM and voltage values are preprogrammed through the $I^2C$ interface. These values are cycled through in succession at each rising/falling edge of the CLKIN pin. This control mode can be utilized with Analog Devices AFEs that feature multiple interrupt output pins, such as the MAX86180, and the ability to set the interrupt to trigger on changes in the 'FIFO Data Ready' status bit.

### $I^2C$ Based DVS Control

If the RREna and DVSSource bits are set to zero, the DVS output voltage is set directly through $I^2C$ using bits 6 to 0 of register 0x02, BBstVset, and can be used to dynamically program the output voltage value. Use bits 6 to 0 of register 0x1E to read back BBstVset value. Bit 7 of register 0x02, BBstFpwm enables the FPWM feature, whereas bit 4 of register 0x01, BBstFast enables the FAST feature. Note that $I^2C$ is the only mode where both these features can be enabled together. Bit FpwmFast of register 0x6E selects the feature for status check (0 = Fast, 1 = FPWM) and bit 7 of register 0x1E, BB_LOWBP reads back the feature status (0 = disabled, 1 = enabled). For example, if FpwmFast = 1 and BBstFpwm = 1, then BB_LOWBP reads back 1 regardless of BBstFast value. On the other hand, if FpwmFast = 1, BBstFpwm = 0 and BBstFast = 1, then BB_LOWBP reads back 0 even the FAST feature is enabled. Note that bit FpwmFast has no effect in setting high performance feature in $I^2C$ mode.

In Round-Robin and in pseudo-SPI, only FPWM or FAST can be enabled. To choose which one, use read-write bit FpwmFast (register 0x06E, bit 0) (0 = Fast, 1 = FPWM). BB_LOWBP reads back 1 if either of the high performance features is enabled. In Round-Robin mode, use each RRLowPBxx bit to disable/enable high performance feature for that cycle. If RRLowPBxx = 0, neither FPWM nor FAST is enabled. If RRLowPBxx = 1, FPWM or FAST is enabled according to FpwmFast bit and BB_LOWPB reads back 1. In pseudo-SPI mode, the serial communication protocol includes a bit (example, bit DVS_MODE_SEL in MAX86181) that has the same function as RRLowPBxx. If

DVS_MODE_SEL in MAX86181 is low, neither FPWM nor FAST is enabled. If DVS_MODE_SEL in MAX86181 is high, FPWM or FAST is enabled according to FpwmFast bit.

The BBstVSet register (0x02) features write protection that can be enabled or disabled by writing 0xAA or 0x55 to register LockUnlock (0x51). For this write operation to take effect, the bit BBLck on register 0x50 must be 0, otherwise the operation on LockUnlock is ignored. The BBstVSet register (0x02) is locked by default.

### DVS Target Mode/Pseudo-SPI

When used with a compatible Analog Devices AFE, such as the MAX86181, the MAX20363 output voltage is controlled by a proprietary serial digital interface on the CLKIN and DVSIN pins. To enable this mode, the register bit DVSSource should be set to 1. Once enabled, 300µs is required until the device is ready to receive a new DVS command from the AFE controller. The default $V_{BBOUT}$ in pseudo-SPI mode is 1.5 V.

In DVS target mode, the MAX20363 acts as a target only. All DVS values are programmed in the corresponding controller AFE. Register 0x13 contains the relevant status bits for DVS target mode, indicating controller requests complete, interface timeout expiration, and parity error.

For additional information on the operation of DVS target mode, reference the data sheet of the relevant DVS controller AFE device, such as MAX86181.

### DVS Round-Robin Interface

The DVS round-robin mode provides allows to preprogram multiple DVS output voltages cycled through on the rising/falling edge of the CLKIN signal (see RRClkPolarity). This mode enables fast DVS output capability on Analog Devices AFEs that do not feature the DVS controller function.

To utilize round-robin mode:

First program up to 20 DVS voltage values into registers 0x20 to 0x33.

If fewer than 20 registers are utilized, write register 0x55, RRSize to define which register location is the last one utilized.

Configure RRWrap bit, in register 0x54, RRWrap, to determine if the round-robin pointer either remains on the final voltage register or returns to location zero after reaching the final voltage value.

Configure the RRTimeoutRes bit, register 0x55 to determine the device behavior after a timeout.

Configure the RRClkPolarity bit for high/low-going edge triggering.

Finally, enable the round-robin mode by writing 1 on the bit RREna (register 0x54, bit 1).

## APPLICATIONS INFORMATION

### Input and Output Capacitance

The MAX20363 is designed to be compatible with small case-size ceramic capacitors. As such, the device has low-input and low-output capacitance requirements to accommodate the steep voltage derating of 0603 and 0402 (imperial) capacitors. *Figure 34* presents the minimum capacitance required at BAT and BBOUT. To ensure stability and low noise, the capacitance value under bias on BAT should be at least the maximum between 5µF and the value of *Figure 34* at the lowest expected $V_{BAT}$. The minimum capacitance value under bias on BBOUT should be equal to the value of *Figure 34* at the lowest expected $V_{BBOUT}$ for BBFetScale = 00, 1/2 of that value for BBFetScale = 01 or 10, and 1/4 of that value for BBFetScale = 11.

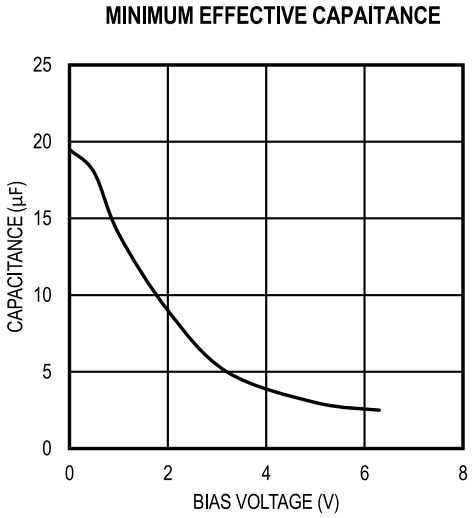



*Figure 34. Buck-Boost Required Minimum Input/Output Capacitance*

## Inductor Selection

Inductor selection for the MAX20363 should be optimized for the intended application. A 1µH is recommended, and a 2.2 µH can be used but can result in worse accuracy, load regulation, and load step response. Aside from the inductor value physical size, DC resistance (DCR), maximum average current, and saturation current are the primary factors to consider. The maximum average inductor current is obtained using the following equation:

$$I_{L\_MAX} = BBIMaxP + (0.5 \times BBstIPSet1)$$

The average inductor current calculated above dictates the required maximum average current for temperature rise on the inductor. To determine the required inductor saturation current, the peak current must be calculated. The peak current for this converter can be calculated as:

$$I_{L\_PEAK} = BBIMaxP + BBstIPSet1$$

where BBstIPSet1 is the peak current setting described in register 0x03. When selecting an inductor, one primary factor in achieving high efficiency is the DCR of the inductor. For maximum efficiency, select an inductor with the lowest DCR possible in the required package size. Another factor to consider is magnetic losses. Generally magnetic losses are lower in inductors with larger physical size and/or higher saturation current ratings. In most cases, ferrite inductors should be avoided as they tend to exhibit poor AC characteristics, especially in discontinuous conduction mode (DCM).

## Soft-Start

Current at start-up is programmable through the start-up inductor current limit register (BBstIPwpMaxP). It can be programmed up to 750mA.

## I²C Interface

The MAX20363 contains an I²C-compatible interface for data communication with a host controller (SCL and SDA). The MAX20363 can support I²C frequencies up to 1MHz. SCL and SDA require pullup resistors connected to a positive supply.

## Peripheral Address

In the MAX20363, the peripheral address is configured at the factory by the i2c_2nd_sid OTP bit to be either 0b1101000 (0x68) plus the Read/Write bit or 0b1101100 (0x6C) plus the Read/Write bit. For versions with the 7-bit peripheral address 0x68, set the Read/Write bit high to configure the MAX20363 to read mode (0xD1) or set the Read/Write bit low to configure the MAX20363 to write mode (0xD0). For versions with the 7-bit peripheral address 0x6C, set the Read/Write bit high to configure the MAX20363 to read mode (0xD8) or set the Read/Write bit low to configure the MAX20363 to write mode (0xD9). See i2c_2nd_sid in *Table 5* for the peripheral address for a given part number. The address is the first byte of information sent to the MAX20363 after the START condition.

## Start, Stop, and Repeated Start Conditions

When writing to the MAX20363 using $I^2C$, the controller sends a START condition (S) followed by the MAX20363 $I^2C$ write address. After the address, the controller sends the register address of the register to be programmed. The controller then ends communication by issuing a STOP condition (P) to relinquish control of the bus, or a REPEATED START condition (Sr) to communicate to another $I^2C$ peripheral. See *Figure 35*.

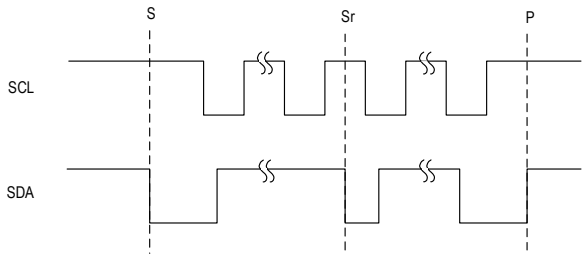



*Figure 35. $I^2C$ START, STOP, and REPEATED START Conditions*

## Bit Transfer

One data bit is transferred on the rising edge of each SCL clock cycle. The data on SDA must remain stable during the high period of the SCL clock pulse. Changes in SDA while SCL is high and stable are considered control signals (see the *Start, Stop, and Repeated Start Conditions* section). Both SDA and SCL remain high when the bus is not active.

## Single-Byte Write

In this operation, the controller sends an address and two data bytes to the peripheral device (*Figure 36*). The following procedure describes the single byte write operation:

1. The controller sends a START condition.
2. The controller sends the 7-bit peripheral address plus a write bit (low).
3. The addressed peripheral asserts an ACK on the data line.
4. The controller sends the 8-bit register address.
5. The peripheral asserts an ACK on the data line.
6. The controller sends 8 data bits.
7. The peripheral asserts an ACK on the data line.
8. The controller generates a STOP condition.

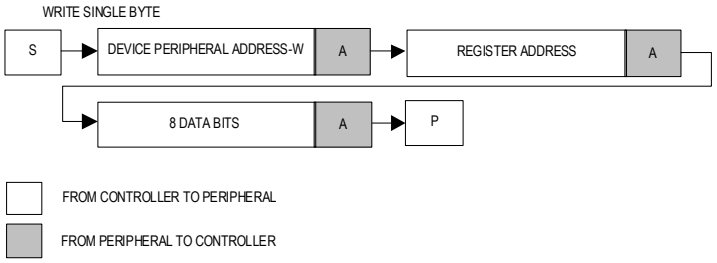



*Figure 36. Write Byte Sequence*

## Burst Write

In this operation, the controller sends an address and multiple data bytes to the peripheral device (*Figure 37*). The peripheral device automatically increments the register address after each data byte is sent, unless the register being accessed reaches 0xFF, in which case the register address remains the same. The following procedure describes the burst write operation:

1. The controller sends a START condition.
2. The controller sends the 7-bit peripheral address plus a write bit (low).
3. The addressed peripheral asserts an ACK on the data line.
4. The controller sends the 8-bit register address.
5. The peripheral asserts an ACK on the data line.
6. The controller sends 8 data bits.
7. The peripheral asserts an ACK on the data line.
8. Repeat 6 and 7 N-1 times.
9. The controller generates a STOP condition.

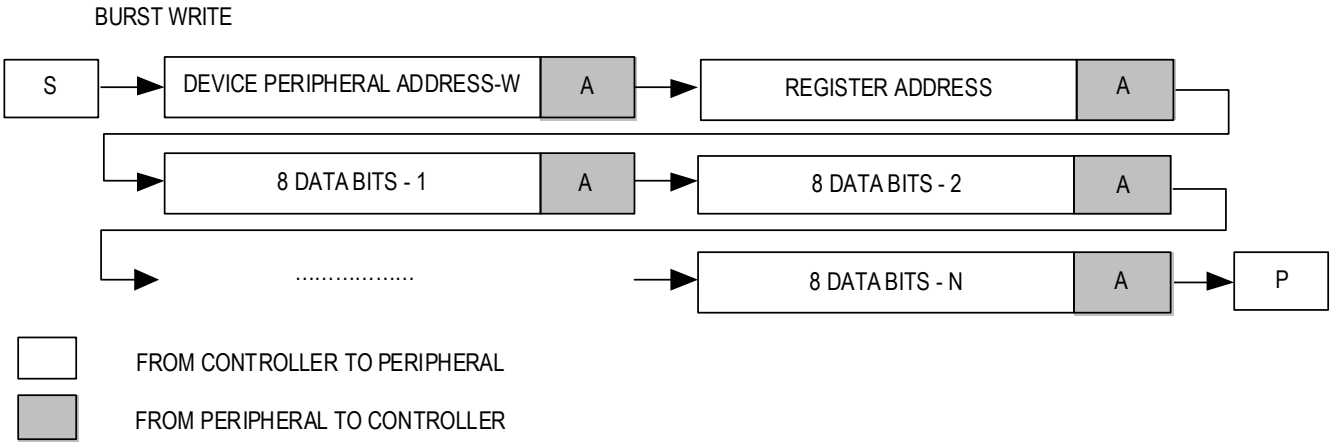



*Figure 37. Burst Write Sequence*

## Single Byte Read

In this operation, the controller sends an address plus two data bytes and receives one data byte from the peripheral device (*Figure 38*). The following procedure describes the single byte read operation:

1. The controller sends a START condition.
2. The controller sends the 7-bit peripheral address plus a write bit (low).
3. The addressed peripheral asserts an ACK on the data line.
4. The controller sends the 8-bit register address.
5. The peripheral asserts an ACK on the data line.
6. The controller sends a REPEATED START condition.
7. The controller sends the 7-bit peripheral address plus a read bit (high).
8. The addressed peripheral asserts an ACK on the data line.
9. The peripheral sends 8 data bits.
10. The controller asserts a NACK on the data line.
11. The controller generates a STOP condition.

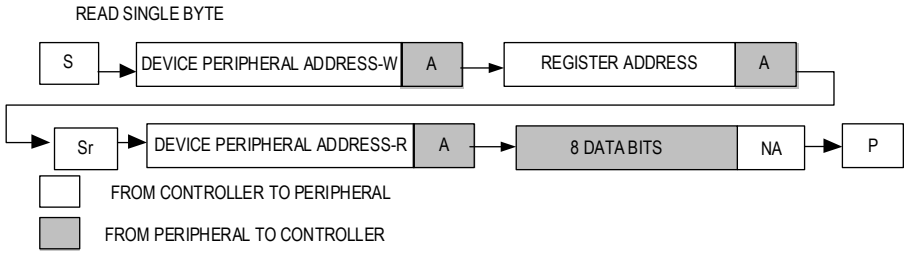



*Figure 38. Read Byte Sequence*

## Burst Read

In this operation, the controller sends an address plus two data bytes and receives multiple data bytes from the peripheral device (*Figure 39*). The following procedure describes the burst byte read operation:

1. The controller sends a START condition.
2. The controller sends the 7-bit peripheral address plus a write bit (low).
3. The addressed peripheral asserts an ACK on the data line.
4. The controller sends the 8-bit register address.
5. The peripheral asserts an ACK on the data line.
6. The controller sends a REPEATED START condition.
7. The controller sends the 7-bit peripheral address plus a read bit (high).
8. The peripheral asserts an ACK on the data line.

9. The peripheral sends 8 data bits.
10. The controller asserts an ACK on the data line.
11. Repeat 9 and 10 N-2 times.
12. The peripheral sends the last 8 data bits.
13. The controller asserts a NACK on the data line.
14. The controller generates a STOP condition.

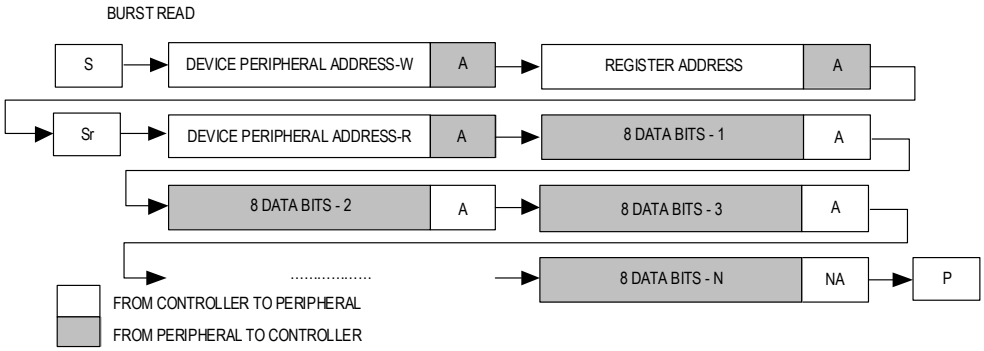



*Figure 39. Burst Read Sequence*

## Acknowledge Bits

Data transfers are acknowledged with an acknowledge bit (ACK) or a not-acknowledge bit (NACK). Both the controller and the MAX20363 generate ACK bits. To generate an ACK, pull SDA low before the rising edge of the ninth clock pulse and hold it low during the high period of the ninth clock pulse (*Figure 40*). To generate a NACK, leave SDA high before the rising edge of the ninth clock pulse and leave it high for the duration of the ninth clock pulse. Monitoring for NACK bits allows detection of unsuccessful data transfers.

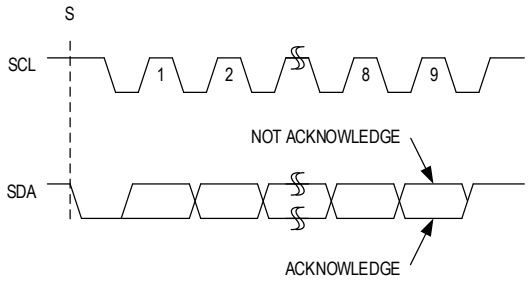



*Figure 40. Acknowledge Bits*

# REGISTER MAP

## MAX20363

| ADDRESS | NAME | MSB | | | | | | | LSB |
|---|---|---|---|---|---|---|---|---|---|
| **USER** | | | | | | | | | |
| 0x00 | ChipID[7:0] | ChipID[7:0] | | | | | | | |
| 0x01 | BBstCfg0[7:0] | BBstLowEMIB[1:0] | | BBstEna | BBstFast | – | BBFHighSh | BBstActDsc | BBstPsvDsc |
| 0x02 | BBstVSet[7:0] | BBstFpwm | BBstVSet[6:0] | | | | | | |
| 0x03 | BBstISet[7:0] | BBstIPSet2[3:0] | | | | BBstIPSet1[3:0] | | | |
| 0x04 | BBstIMaxN[7:0] | – | – | BBIMaxN[5:0] | | | | | |
| 0x05 | BBstIMaxP[7:0] | – | – | BBIMaxP[5:0] | | | | | |
| 0x06 | BBstIPwpMaxP[7:0] | – | – | BBIPwpMaxP[5:0] | | | | | |
| 0x08 | BBstCfg1[7:0] | – | – | – | – | BBL2P2Sel | BBstIpPadPEnb | BBFetScale[1:0] | |
| 0x10 | Status[7:0] | – | – | BBstOnSts | BBstOffSts | VddUvloSts | BBOutUvloSts | BstSts | ThmFltSts |
| 0x11 | Int[7:0] | – | – | BBstOnInt | BBstOffInt | VddUvloInt | BBOutUvloInt | BstFltInt | ThmFltInt |
| 0x12 | Mask[7:0] | – | – | BBstOnMsk | BBstOffMsk | VddUvloMsk | BBoutUvloMsk | BstFltMsk | ThmFltMsk |
| 0x13 | CommInt[7:0] | – | – | ChgModDone | RRTimeout | RRInc | SPIDone | SPITimeout | SPIParErr |
| 0x14 | CommMsk[7:0] | – | – | ChgModDoneMsk | RRTimeoutMsk | RRIncMsk | SPIDoneMsk | SPITimeoutMsk | SPIParErrMsk |
| 0x15 | BBFsmState[7:0] | – | – | BBCtrlState[5:0] | | | | | |
| 0x1E | BBVset[7:0] | BB_LOWPB | BB_VSET[6:0] | | | | | | |
| 0x1F | RRpoint[7:0] | – | – | – | RRPointer[4:0] | | | | |
| 0x20 | RRVset00[7:0] | RRLowPB00 | RRVset00[6:0] | | | | | | |
| 0x21 | RRVset01[7:0] | RRLowPB01 | RRVset01[6:0] | | | | | | |
| 0x22 | RRVset02[7:0] | RRLowPB02 | RRVset02[6:0] | | | | | | |
| 0x23 | RRVset03[7:0] | RRLowPB03 | RRVset03[6:0] | | | | | | |
| 0x24 | RRVset04[7:0] | RRLowPB04 | RRVset04[6:0] | | | | | | |

| ADDRESS | NAME | MSB | | | | | | | LSB |
|---|---|---|---|---|---|---|---|---|---|
| 0x25 | RRVset05[7:0] | RRLowPB05 | RRVset05[6:0] | | | | | | |
| 0x26 | RRVset06[7:0] | RRLowPB06 | RRVset06[6:0] | | | | | | |
| 0x27 | RRVset07[7:0] | RRLowPB07 | RRVset07[6:0] | | | | | | |
| 0x28 | RRVset08[7:0] | RRLowPB08 | RRVset08[6:0] | | | | | | |
| 0x29 | RRVset09[7:0] | RRLowPB09 | RRVset09[6:0] | | | | | | |
| 0x2A | RRVset0A[7:0] | RRLowPB0A | RRVset0A[6:0] | | | | | | |
| 0x2B | RRVset0B[7:0] | RRLowPB0B | RRVset0B[6:0] | | | | | | |
| 0x2C | RRVset0C[7:0] | RRLowPB0C | RRVset0C[6:0] | | | | | | |
| 0x2D | RRVset0D[7:0] | RRLowPB0D | RRVset0D[6:0] | | | | | | |
| 0x2E | RRVset0E[7:0] | RRLowPB0E | RRVset0E[6:0] | | | | | | |
| 0x2F | RRVset0F[7:0] | RRLowPB0F | RRVset0F[6:0] | | | | | | |
| 0x30 | RRVset10[7:0] | RRLowPB10 | RRVset10[6:0] | | | | | | |
| 0x31 | RRVset11[7:0] | RRLowPB11 | RRVset11[6:0] | | | | | | |
| 0x32 | RRVset12[7:0] | RRLowPB12 | RRVset12[6:0] | | | | | | |
| 0x33 | RRVset13[7:0] | RRLowPB13 | RRVset13[6:0] | | | | | | |
| 0x50 | LockMsk[7:0] | – | – | – | – | – | – | – | BBLck |
| 0x51 | LockUnlock[7:0] | PASSWD[7:0] | | | | | | | |
| 0x54 | DVSCfg[7:0] | – | – | – | – | I2CLkptDis | RRWrap | RREna | DVSSource |
| 0x55 | RRCfg1[7:0] | – | RRClkPolarity | RRTimeoutRes | RRSize[4:0] | | | | |
| 0x56 | RRCfg2[7:0] | – | – | – | – | – | RRTimeoutLength[2:0] | | |
| 0x57 | SPICfg[7:0] | – | – | – | – | – | – | – | SPITimeoutEna |

| ADDRESS | NAME | MSB | | | | | | | LSB |
|---|---|---|---|---|---|---|---|---|---|
| 0x6E | ConfOtp[7:0] | – | – | – | – | – | – | – | FpwmFast |
| 0x6F | FuncDef[7:0] | – | – | – | – | LtchOffVddUvlo | LtchOffBBOutUvlo | LtchOffBst | LtchOffThm |

## Register Details

### ChipID (0x0)

| BIT | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| **Field** | ChipID[7:0] | | | | | | | |
| **Reset** | 0x00 | | | | | | | |
| **Access Type** | Read Only | | | | | | | |

| BITFIELD | BITS | DESCRIPTION |
|---|---|---|
| ChipID | 7:0 | ChipID[7:0] indicates the version of the device in use. |

### BBstCfg0 (0x1)

| BIT | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| **Field** | BBstLowEMIB[1:0] | | BBstEna | BBstFast | – | BBFHighSh | BBstActDsc | BBstPsvDsc |
| **Reset** | | | | | – | | | |
| **Access Type** | Write, Read | | Write, Read | Write, Read | – | Write, Read | Write, Read | Write, Read |

| BITFIELD | BITS | DESCRIPTION | DECODE |
|---|---|---|---|
| BBstLowEMIB | 7:6 | Buck-Boost Low EMI Mode Disable<br>Increases the rise/fall time of LXA/LXB to reduce EMI, at the cost of efficiency.<br>It can be changed only when BBstEna = 0.<br>10,11 = Reserved not to be used | 0x0: Increase rise/fall time on LXA/LXB by 4x<br>0x1: Nominal Slopes |
| BBstEna | 5 | Buck-Boost Enable | 0x0: Buck-boost disabled<br>0x1: Buck-boost enabled |
| BBstFast | 4 | Buck-Boost Fast Feature Enable<br>Increases the quiescent current of the buck-boost to improve output regulation during load transients.<br>If 1, $I_{Q\_FAST}$ increased to 75µA (typical). | 0x0: Fast response disabled<br>0x1: Fast response enabled |
| BBFHighSh | 2 | Buck-Boost $f_{HIGH}$ Thresholds<br>Selects the switching frequency threshold $f_{HIGH}$. If the buck-boost switching frequency exceeds the $f_{HIGH}$ rising threshold, all the blocks are kept ON ($I_Q$ | 0x0: 50kHz rising / 25kHz falling<br>0x1: 100kHz rising / 50kHz falling |

| BITFIELD | BITS | DESCRIPTION | DECODE |
|---|---|---|---|
| | | is higher) until the frequency reaches the $f_{HIGH}$ falling threshold. A small glitch on $V_{OUT}$ can be present at the $f_{HIGH}$ crossover.<br>It can be changed only when BBstEna = 0. | |
| BBstActDsc | 1 | Buck-Boost Active Discharge Control | 0x0: Buck-boost not actively discharged<br>0x1: Buck-boost actively discharged when disabled |
| BBstPsvDsc | 0 | Buck-Boost Passive Discharge Control | 0x0: Buck-boost not passively discharged<br>0x1: Buck-boost passively discharged when disabled |

## BBstVSet (0x2)

| BIT | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| **Field** | BBstFpwm | BBstVSet[6:0] | | | | | | |
| **Reset** | | | | | | | | |
| **Access Type** | Write, Read | Write, Read | | | | | | |

| BITFIELD | BITS | DESCRIPTION | DECODE |
|---|---|---|---|
| BBstFpwm | 7 | Buck-Boost Fpwm Feature Enable<br>With FPWM best load regulation/ripple but high quiescent and poor efficiency at light loads. Use it only for ≥70mA loads | 0x0: FPWM is disabled<br>0x1: FPWM is enabled |
| BBstVSet | 6:0 | Buck-Boost Output Voltage Setting<br>1.5V to 5.5V, linear scale, 50mV increments | 0x0: 1.50V<br>0x1: 1.55V<br>...<br>≥0x50: 5.50V |

## BBstISet (0x3)

| BIT | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| **Field** | BBstIPSet2[3:0] | | | | BBstIPSet1[3:0] | | | |
| **Reset** | | | | | | | | |
| **Access Type** | Write, Read | | | | Write, Read | | | |

| BITFIELD | BITS | DESCRIPTION | DECODE |
|---|---|---|---|
| BBstIPSet2 | 7:4 | Buck-Boost Nominal Maximum Peak Current Setting 2.<br>Sets the extra peak current on top of IPSET1 when $V_{BAT}$>$V_{BBOUT}$. See buck-boost operation section for a description of the peak current settings.<br><br>From 0 to 375mA, 25mA step.<br>Suggested value 300mA<br><br>Note1: The values are increased by about 30% when BBL2P2Sel = 0 is set. | 0x0: 0mA<br>0x1: 25mA<br>...<br>0xF: 375mA |

| BITFIELD | BITS | DESCRIPTION | DECODE |
|---|---|---|---|
| | | Note2 : Actual peak current in the inductor is larger because of the delay of peak comparator and power stage. | |
| BBstIPSet1 | 3:0 | Buck-boost Nominal Maximum Peak Current Setting 1<br>Nominal peak current when charging inductor between $V_{BAT}$ and GND. See buck-boost operation section for a description of the peak current settings.<br><br>From 100mA to 475mA, 25mA step.<br>Optimal values are set according to look-up table which is set by OTP register settings of bits IPm50, IPm60M50, IPm70M60 and IPM70.<br>Suggested values to get optimal efficiency:<br>BBstVSet≤4V : IPSET1 = 250mA<br>4V<BBstVSet≤4.5V : IPSET1 = 300mA<br>4.5V<BBstVSet≤5V : IPSET1 = 350mA<br>BBstVSet>5V : IPSET1 = 400mA<br><br>Note1: The values are increased by about 30% when BBL2P2Sel = 0 is set.<br>Note 2: Real IPSET1 is gradually reduced to 0 when $V_{BAT}$>$V_{BBOUT}$. | 0x0: 100mA<br>0x1: 125mA<br>...<br>0xF: 475mA |

## BBstIMaxN (0x4)

| BIT | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Field | – | – | BBIMaxN[5:0] | | | | | |
| Reset | – | – | | | | | | |
| Access Type | – | – | Write, Read | | | | | |

| BITFIELD | BITS | DESCRIPTION | DECODE |
|---|---|---|---|
| BBIMaxN | 5:0 | Maximum Inductor Negative Valley Current Limit when FPWM is Enabled<br>It can be changed only when BBstEna = 0.<br>From -200mA to -1.8A, 50mA step | 0x0: -200mA<br>0x1: -250mA<br>...<br>0x20: -1.8A |

## BBstIMaxP (0x5)

| BIT | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Field | – | – | BBIMaxP[5:0] | | | | | |
| Reset | – | – | | | | | | |
| Access Type | – | – | Write, Read | | | | | |

| BITFIELD | BITS | DESCRIPTION | DECODE |
|---|---|---|---|
| BBIMaxP | 5:0 | Maximum inductor positive valley current limit setting.<br>It can be changed only when BBstEna = 0.<br>From 0 to 1.6A, 50mA step | 0x0: 0mA<br>0x1: 50mA<br>...<br>≥0x20: 1.6A |

## BBstIPwpMaxP (0x6)

| BIT | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Field | – | – | BBIPwpMaxP[5:0] | | | | | |
| Reset | – | – | | | | | | |
| Access Type | – | – | Write, Read | | | | | |

| BITFIELD | BITS | DESCRIPTION | DECODE |
|---|---|---|---|
| BBIPwpMaxP | 5:0 | Start-up Positive Inductor Valley Current Limit<br>It can be changed only when BBstEna = 0.<br>Programmable from 0 to 750mA (50mA step).<br>Below BBOut UVLO at least 150 mA are internally enforced. | 0x0: 0mA<br>0x1: 50mA<br>...<br>≥0xF: 750mA |

## BBstCfg1 (0x8)

| BIT | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Field | – | – | – | – | BBL2P2Sel | BBstIpPadPEnb | BBFetScale[1:0] | |
| Reset | – | – | – | – | | | | |
| Access Type | – | – | – | – | Write, Read | Write, Read | Write, Read | |

| BITFIELD | BITS | DESCRIPTION | DECODE |
|---|---|---|---|
| BBL2P2Sel | 3 | Inductor Select Bit<br>It can be changed only when BBstEna = 0.<br>If 1, worst load regulation in ccm mode. | 0x0: For 1µH inductor<br>0x1: For 2.2µH inductor |
| BBstIpPadPEnb | 2 | Adaptive Peak/Valley Current Adjustment Disable<br>If 1, peak current is fixed to the values set by BBstIPSet1 and BBstIPSet2. Valley current is fixed to 0mA. This setting is equivalent to forcing discontinuous conduction mode and greatly diminishes the output power capability of the device. Generally this is not a recommended setting. | 0x0: Enabled<br>0x1: Disabled |
| BBFetScale | 1:0 | FET Scaling Bits<br>Reduce the loop bandwidth to relax output compensation capacitor requirement if lower output | 0x0: Full power FETS, Full Bandwidth<br>0x1: 50% FET size, 1/2 Bandwidth<br>0x2: 50% FET size, 1/2 Bandwidth<br>0x3: 25% FET size, 1/4 Bandwidth |

| BITFIELD | BITS | DESCRIPTION | DECODE |
|---|---|---|---|
| | | current is needed.<br>It can be changed only when BBstEna = 0. | |

## Status (0x10)

| BIT | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| **Field** | – | – | BBstOnSts | BBstOffSts | VddUvloSts | BBOutUvloSts | BstSts | ThmFltSts |
| **Reset** | – | – | | | | | | |
| **Access Type** | – | – | Read Only | Read Only | Read Only | Read Only | Read Only | Read Only |

| BITFIELD | BITS | DESCRIPTION | DECODE |
|---|---|---|---|
| BBstOnSts | 5 | Status of Buck-Boost ON<br>This bit goes to 1 when the buck-boost turns on, so that DVS operations are possible, and goes back to 0 when the buck-boost is disabled or when a fault occurs. | 0x0: Buck-boost Off<br>0x1: Buck-boost On |
| BBstOffSts | 4 | Status of Buck-Boost OFF<br>This bit goes to 1 when the buck-boost turns off after having been disabled and having gone through safe freewheeling and output discharge, and goes back to 0 when the buck-boost is enabled again. | 0x0: Buck-boost On<br>0x1: Buck-boost Off |
| VddUvloSts | 3 | Status of Vdd or Bat UVLO Fault<br>This bit goes to 1 when Vdd or Bat UVLO fault occurs, and goes back to 0 when either BBstEna is set to 0 or the autoretry time elapses (if OTP bit LtchOffVddUvlo = 0). | 0x0: Normal Vdd and Bat voltage<br>0x1: Vdd or Bat UVLO |
| BBOutUvloSts | 2 | Status of BBOut UVLO Fault<br>This bit goes to 1 when BBOut UVLO fault occurs, and goes back to 0 when either BBstEna is set to 0 or the autoretry time elapses (if OTP bit LtchOffBBOutUvlo = 0). | 0x0: Normal BBOut voltage<br>0x1: BBOut UVLO |
| BstSts | 1 | Status of Bootstrap Fault<br>This bit goes to 1 when bootstrap fault occurs, and goes back to 0 when either BBstEna is set to 0 or the autoretry time elapses (if OTP bit LtchOffBst = 0). | 0x0: Bootstrap operating normally<br>0x1: Bootstrap under fault condition |
| ThmFltSts | 0 | Status of Thermal Fault<br>This bit goes to 1 when thermal fault occurs, and goes back to 0 when either BBstEna is set to 0 or the autoretry time elapses (if OTP bit LtchOffThm = 0). | 0x0: Buck-boost operating normally<br>0x1: Buck-boost in thermal shutdown |

## Int (0x11)

| BIT | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|

| Field | – | – | BBstOnInt | BBstOffInt | VddUvloInt | BBOutUvloInt | BstFltInt | ThmFltInt |
|---|---|---|---|---|---|---|---|---|
| Reset | – | – | | | | | | |
| Access Type | – | – | Write, Read | Write, Read | Write, Read | Write, Read | Write, Read | Write, Read |

| BITFIELD | BITS | DESCRIPTION | DECODE |
|---|---|---|---|
| BBstOnInt | 5 | Change in BBstOnSts caused an interrupt.<br>Read to clear. | 0x0: Not triggered since last read<br>0x1: Triggered |
| BBstOffInt | 4 | Change in BBstOffSts caused an interrupt.<br>Read to clear. | 0x0: Not triggered since last read<br>0x1: Triggered |
| VddUvloInt | 3 | Change in VddUvloSts caused an interrupt.<br>Read to clear. | 0x0: Not triggered since last read<br>0x1: Triggered |
| BBOutUvloInt | 2 | Change in BBOutUvloSts caused an interrupt.<br>Read to clear. | 0x0: Not triggered since last read<br>0x1: Triggered |
| BstFltInt | 1 | Change in BstSts caused an interrupt.<br>Read to clear. | 0x0: Not triggered since last read<br>0x1: Triggered |
| ThmFltInt | 0 | Change in ThmFltSts caused an interrupt.<br>Read to clear. | 0x0: Not triggered since last read<br>0x1: Triggered |

## Mask (0x12)

| BIT | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Field | – | – | BBstOnMsk | BBstOffMsk | VddUvloMsk | BBoutUvloMsk | BstFltMsk | ThmFltMsk |
| Reset | – | – | | 0x1 | | | | |
| Access Type | – | – | Write, Read | Write, Read | Write, Read | Write, Read | Write, Read | Write, Read |

| BITFIELD | BITS | DESCRIPTION | DECODE |
|---|---|---|---|
| BBstOnMsk | 5 | BBstOnMsk masks the BBstOnInt interrupt. | 0x0: Not masked<br>0x1: Masked |
| BBstOffMsk | 4 | BBstOffMsk masks the BBstOffInt interrupt. | 0x0: Not masked<br>0x1: Masked |
| VddUvloMsk | 3 | VddUvloMsk masks the VddUvloInt interrupt. | 0x0: Not masked<br>0x1: Masked |
| BBoutUvloMsk | 2 | BBOutUvloMsk masks the BBOutUvloInt interrupt. | 0x0: Not masked<br>0x1: Masked |
| BstFltMsk | 1 | BstFltMsk masks the BstFltInt interrupt. | 0x0: Not masked<br>0x1: Masked |
| ThmFltMsk | 0 | ThmFltMsk masks the ThmFltInt interrupt. | 0x0: Not masked<br>0x1: Masked |

## CommInt (0x13)

| BIT | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| **Field** | – | – | ChgModDone | RRTimeout | RRInc | SPIDone | SPITimeout | SPIParErr |
| **Reset** | – | – | | | | 0b0 | 0b0 | 0b0 |
| **Access Type** | – | – | Write, Read | Write, Read | Write, Read | Write, Read | Write, Read | Write, Read |

| BITFIELD | BITS | DESCRIPTION | DECODE |
|---|---|---|---|
| ChgModDone | 5 | Change DVS Mode Done Interrupt<br>Read to clear. | 0x0: Not triggered since last read<br>0x1: Triggered |
| RRTimeout | 4 | Round-Robin Timeout Interrupt<br>Read to clear. | 0x0: Not triggered since last read<br>0x1: Triggered |
| RRInc | 3 | Round-Robin Pointer Increase Interrupt<br>The interrupt is raised when a pulse that moves the Round-Robin to next step is detected. Read to clear. | 0x0: Not triggered since last read<br>0x1: Triggered |
| SPIDone | 2 | Pseudo-SPI Operation Done Interrupt<br>If 1, the pseudo-SPI operation is completed. Read to clear. | 0x0: Not triggered since last read<br>0x1: Triggered |
| SPITimeout | 1 | Pseudo-SPI Timeout Interrupt<br>If 1, the pseudo-SPI operation was ended because of timeout fault. Read to clear. | 0x0: Not triggered since last read<br>0x1: Triggered |
| SPIParErr | 0 | Pseudo-SPI Parity Error Interrupt<br>If 1, a parity error was found, and the DVS operation was not executed. Read to clear. | 0x0: Not triggered since last read<br>0x1: Triggered |

## CommMsk (0x14)

| BIT | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| **Field** | – | – | ChgModDoneMsk | RRTimeoutMsk | RRIncMsk | SPIDoneMsk | SPITimeoutMsk | SPIParErrMsk |
| **Reset** | – | – | | | | 0b0 | 0b0 | 0b0 |
| **Access Type** | – | – | Write, Read | Write, Read | Write, Read | Write, Read | Write, Read | Write, Read |

| BITFIELD | BITS | DESCRIPTION | DECODE |
|---|---|---|---|
| ChgModDoneMsk | 5 | ChgModDoneMsk masks the ChgModDone interrupt. | 0x0: Not masked<br>0x1: Masked |
| RRTimeoutMsk | 4 | RRTimeoutMsk masks the RRTimeout interrupt. | 0x0: Not masked<br>0x1: Masked |
| RRIncMsk | 3 | RRIncMsk masks the RRInc interrupt. | 0x0: Not masked<br>0x1: Masked |
| SPIDoneMsk | 2 | SPIDoneMsk masks the SPIDone interrupt. | 0x0: Not masked<br>0x1: Masked |

| BITFIELD | BITS | DESCRIPTION | DECODE |
|---|---|---|---|
| SPITimeoutMsk | 1 | SPITimeoutMsk masks the SPITimeout interrupt. | 0x0: Not masked<br>0x1: Masked |
| SPIParErrMsk | 0 | SPIParErrMsk masks the SPIParErr interrupt. | 0x0: Not masked<br>0x1: Masked |

## BBFsmState (0x15)

| BIT | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| **Field** | – | – | BBCtrlState[5:0] | | | | | |
| **Reset** | – | – | | | | | | |
| **Access Type** | – | – | Read Only | | | | | |

| BITFIELD | BITS | DESCRIPTION |
|---|---|---|
| BBCtrlState | 5:0 | Current state of Buck-Boost control FSM:<br>000001 = Off<br>000010 = Power-up<br>000100 = Functional DVS<br>001000 = Safe Freewheeling<br>010000 = Active Output Discharge<br>100000 = Timeout |

## BBVset (0x1E)

| BIT | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| **Field** | BB_LOWPB | BB_VSET[6:0] | | | | | | |
| **Reset** | | 0x00 | | | | | | |
| **Access Type** | Read Only | Read Only | | | | | | |

| BITFIELD | BITS | DESCRIPTION | DECODE |
|---|---|---|---|
| BB_LOWPB | 7 | High Performance Feature Read Back<br>In Round-Robin mode, this bit indicates if high performance feature is enabled. It reads 1 if RRLowPBxx (register 0x20-0x33 bit 7) is set to 1.<br>In Pseudo-SPI mode, this bit indicates if high performance feature is enabled. It reads 1 if the 4th serial communication protocol bit is set to 1.<br>In $I^2C$ mode, this bit reads 1 in any of the following three conditions.<br>1) FPWM = 1, FAST = 0, FpwmFast = 1<br>2) FPWM = 0, FAST = 1, FpwmFast = 0<br>3) FPWM = 1, FAST = 1, FpwmFast = 0 or 1 | |
| BB_VSET | 6:0 | BBstVset Read Back<br>This is the actual value set to the analog circuitry. | 0x0: 1.50V<br>0x1: 1.55V<br>...<br>0x50: 5.50V |

## RRpoint (0x1F)

| BIT | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| **Field** | – | – | – | RRPointer[4:0] | | | | |
| **Reset** | – | – | – | | | | | |
| **Access Type** | – | – | – | Read Only | | | | |

| BITFIELD | BITS | DESCRIPTION | DECODE |
|---|---|---|---|
| RRPointer | 4:0 | Round-Robin Step Pointer<br>This bitfield displays the number of the step the Round-Robin has reached so far. | 0x0: Step 0 (initial voltage)<br>0x1: Step 1<br>...<br>0x13: Step 19 |

## RRVset00 (0x20)

| BIT | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| **Field** | RRLowPB00 | RRVset00[6:0] | | | | | | |
| **Reset** | | | | | | | | |
| **Access Type** | Write, Read | Write, Read | | | | | | |

| BITFIELD | BITS | DESCRIPTION | DECODE |
|---|---|---|---|
| RRLowPB00 | 7 | DVS Round-Robin High Performance Feature Step 0x00 | 0x0: High performance feature disabled<br>0x1: High performance feature enabled |
| RRVset00 | 6:0 | DVS Round-Robin Voltage Value Step 0x00 | Refer to register 0x02 BBstVSet bit |

## RRVset01 (0x21)

| BIT | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| **Field** | RRLowPB01 | RRVset01[6:0] | | | | | | |
| **Reset** | | | | | | | | |
| **Access Type** | Write, Read | Write, Read | | | | | | |

| BITFIELD | BITS | DESCRIPTION | DECODE |
|---|---|---|---|
| RRLowPB01 | 7 | DVS Round-Robin High Performance Feature Step 0x01 | Refer to register 0x20 RRLowPB00 bit |
| RRVset01 | 6:0 | DVS Round-Robin Voltage Value Step 0x01 | Refer to register 0x02 BBstVSet bit |

## RRVset02 (0x22)

| BIT | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| **Field** | RRLowPB02 | RRVset02[6:0] | | | | | | |
| **Reset** | | | | | | | | |
| **Access Type** | Write, Read | Write, Read | | | | | | |

| BITFIELD | BITS | DESCRIPTION | DECODE |
|---|---|---|---|
| RRLowPB02 | 7 | DVS Round-Robin High Performance Feature Step 0x02 | Refer to register 0x20 RRLowPB00 bit |
| RRVset02 | 6:0 | DVS Round-Robin Voltage Value Step 0x02 | Refer to register 0x02 BBstVSet bit |

## RRVset03 (0x23)

| BIT | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| **Field** | RRLowPB03 | RRVset03[6:0] | | | | | | |
| **Reset** | | | | | | | | |
| **Access Type** | Write, Read | Write, Read | | | | | | |

| BITFIELD | BITS | DESCRIPTION | DECODE |
|---|---|---|---|
| RRLowPB03 | 7 | DVS Round-Robin High Performance Feature Step 0x03 | Refer to register 0x20 RRLowPB00 bit |
| RRVset03 | 6:0 | DVS Round-Robin Voltage Value Step 0x03 | Refer to register 0x02 BBstVSet bit |

## RRVset04 (0x24)

| BIT | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| **Field** | RRLowPB04 | RRVset04[6:0] | | | | | | |
| **Reset** | | | | | | | | |
| **Access Type** | Write, Read | Write, Read | | | | | | |

| BITFIELD | BITS | DESCRIPTION | DECODE |
|---|---|---|---|
| RRLowPB04 | 7 | DVS Round-Robin High Performance Feature Step 0x04 | Refer to register 0x20 RRLowPB00 bit |
| RRVset04 | 6:0 | DVS Round-Robin Voltage Value Step 0x04 | Refer to register 0x02 BBstVSet bit |

## RRVset05 (0x25)

| BIT | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| **Field** | RRLowPB05 | RRVset05[6:0] | | | | | | |
| **Reset** | | | | | | | | |
| **Access Type** | Write, Read | Write, Read | | | | | | |

| BITFIELD | BITS | DESCRIPTION | DECODE |
|---|---|---|---|
| RRLowPB05 | 7 | DVS Round-Robin High Performance Feature Step 0x05 | Refer to register 0x20 RRLowPB00 bit |
| RRVset05 | 6:0 | DVS Round-Robin Voltage Value Step 0x05 | Refer to register 0x02 BBstVSet bit |

## RRVset06 (0x26)

| BIT | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| **Field** | RRLowPB06 | RRVset06[6:0] | | | | | | |
| **Reset** | | | | | | | | |
| **Access Type** | Write, Read | Write, Read | | | | | | |

| BITFIELD | BITS | DESCRIPTION | DECODE |
|---|---|---|---|
| RRLowPB06 | 7 | DVS Round-Robin High Performance Feature Step 0x06 | Refer to register 0x20 RRLowPB00 bit |
| RRVset06 | 6:0 | DVS Round-Robin Voltage Value Step 0x06 | Refer to register 0x02 BBstVSet bit |

## RRVset07 (0x27)

| BIT | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| **Field** | RRLowPB07 | RRVset07[6:0] | | | | | | |
| **Reset** | | | | | | | | |
| **Access Type** | Write, Read | Write, Read | | | | | | |

| BITFIELD | BITS | DESCRIPTION | DECODE |
|---|---|---|---|
| RRLowPB07 | 7 | DVS Round-Robin High Performance Feature Step 0x07 | Refer to register 0x20 RRLowPB00 bit |
| RRVset07 | 6:0 | DVS Round-Robin Voltage Value Step 0x07 | Refer to register 0x02 BBstVSet bit |

## RRVset08 (0x28)

| BIT | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| **Field** | RRLowPB08 | RRVset08[6:0] | | | | | | |
| **Reset** | | | | | | | | |
| **Access Type** | Write, Read | Write, Read | | | | | | |

| BITFIELD | BITS | DESCRIPTION | DECODE |
|---|---|---|---|
| RRLowPB08 | 7 | DVS Round-Robin High Performance Feature Step 0x08 | Refer to register 0x20 RRLowPB00 bit |
| RRVset08 | 6:0 | DVS Round-Robin Voltage Value Step 0x08 | Refer to register 0x02 BBstVSet bit |

## RRVset09 (0x29)

| BIT | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| **Field** | RRLowPB09 | RRVset09[6:0] | | | | | | |
| **Reset** | | | | | | | | |
| **Access Type** | Write, Read | Write, Read | | | | | | |

| BITFIELD | BITS | DESCRIPTION | DECODE |
|---|---|---|---|
| RRLowPB09 | 7 | DVS Round-Robin High Performance Feature Step 0x09 | Refer to register 0x20 RRLowPB00 bit |
| RRVset09 | 6:0 | DVS Round-Robin Voltage Value Step 0x09 | Refer to register 0x02 BBstVSet bit |

## RRVset0A (0x2A)

| BIT | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| **Field** | RRLowPB0A | RRVset0A[6:0] | | | | | | |
| **Reset** | | | | | | | | |
| **Access Type** | Write, Read | Write, Read | | | | | | |

| BITFIELD | BITS | DESCRIPTION | DECODE |
|---|---|---|---|
| RRLowPB0A | 7 | DVS Round-Robin High Performance Feature Step 0x0A | Refer to register 0x20 RRLowPB00 bit |
| RRVset0A | 6:0 | DVS Round-Robin Voltage Value Step 0x0A | Refer to register 0x02 BBstVSet bit |

## RRVset0B (0x2B)

| BIT | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| **Field** | RRLowPB0B | RRVset0B[6:0] | | | | | | |
| **Reset** | | | | | | | | |
| **Access Type** | Write, Read | Write, Read | | | | | | |

| BITFIELD | BITS | DESCRIPTION | DECODE |
|---|---|---|---|
| RRLowPB0B | 7 | DVS Round-Robin High Performance Feature Step 0x0B | Refer to register 0x20 RRLowPB00 bit |
| RRVset0B | 6:0 | DVS Round-Robin Voltage Value Step 0x0B | Refer to register 0x02 BBstVSet bit |

## RRVset0C (0x2C)

| BIT | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| **Field** | RRLowPB0C | RRVset0C[6:0] | | | | | | |
| **Reset** | | | | | | | | |
| **Access Type** | Write, Read | Write, Read | | | | | | |

| BITFIELD | BITS | DESCRIPTION | DECODE |
|---|---|---|---|
| RRLowPB0C | 7 | DVS Round-Robin High Performance Feature Step 0x0C | Refer to register 0x20 RRLowPB00 bit |
| RRVset0C | 6:0 | DVS Round-Robin Voltage Value Step 0x0C | Refer to register 0x02 BBstVSet bit |

## RRVset0D (0x2D)

| BIT | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| **Field** | RRLowPB0D | RRVset0D[6:0] | | | | | | |
| **Reset** | | | | | | | | |
| **Access Type** | Write, Read | Write, Read | | | | | | |

| BITFIELD | BITS | DESCRIPTION | DECODE |
|---|---|---|---|
| RRLowPB0D | 7 | DVS Round-Robin High Performance Feature Step 0x0D | Refer to register 0x20 RRLowPB00 bit |
| RRVset0D | 6:0 | DVS Round-Robin Voltage Value Step 0x0D | Refer to register 0x02 BBstVSet bit |

## RRVset0E (0x2E)

| BIT | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| **Field** | RRLowPB0E | RRVset0E[6:0] | | | | | | |
| **Reset** | | | | | | | | |
| **Access Type** | Write, Read | Write, Read | | | | | | |

| BITFIELD | BITS | DESCRIPTION | DECODE |
|---|---|---|---|
| RRLowPB0E | 7 | DVS Round-Robin High Performance Feature Step 0x0E | Refer to register 0x20 RRLowPB00 bit |
| RRVset0E | 6:0 | DVS Round-Robin Voltage Value Step 0x0E | Refer to register 0x02 BBstVSet bit |

## RRVset0F (0x2F)

| BIT | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| **Field** | RRLowPB0F | RRVset0F[6:0] | | | | | | |
| **Reset** | | | | | | | | |
| **Access Type** | Write, Read | Write, Read | | | | | | |

| BITFIELD | BITS | DESCRIPTION | DECODE |
|---|---|---|---|
| RRLowPB0F | 7 | DVS Round-Robin High Performance Feature Step 0x0F | Refer to register 0x20 RRLowPB00 bit |
| RRVset0F | 6:0 | DVS Round-Robin Voltage Value Step 0x0F | Refer to register 0x02 BBstVSet bit |

## RRVset10 (0x30)

| BIT | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| **Field** | RRLowPB10 | RRVset10[6:0] | | | | | | |
| **Reset** | | | | | | | | |
| **Access Type** | Write, Read | Write, Read | | | | | | |

| BITFIELD | BITS | DESCRIPTION | DECODE |
|---|---|---|---|
| RRLowPB10 | 7 | DVS Round-Robin High Performance Feature Step 0x10 | Refer to register 0x20 RRLowPB00 bit |
| RRVset10 | 6:0 | DVS Round-Robin Voltage Value Step 0x10 | Refer to register 0x02 BBstVSet bit |

## RRVset11 (0x31)

| BIT | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| **Field** | RRLowPB11 | RRVset11[6:0] | | | | | | |
| **Reset** | | | | | | | | |
| **Access Type** | Write, Read | Write, Read | | | | | | |

| BITFIELD | BITS | DESCRIPTION | DECODE |
|---|---|---|---|
| RRLowPB11 | 7 | DVS Round-Robin High Performance Feature Step 0x11 | Refer to register 0x20 RRLowPB00 bit |
| RRVset11 | 6:0 | DVS Round-Robin Voltage Value Step 0x11 | Refer to register 0x02 BBstVSet bit |

## RRVset12 (0x32)

| BIT | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| **Field** | RRLowPB12 | RRVset12[6:0] | | | | | | |
| **Reset** | | | | | | | | |
| **Access Type** | Write, Read | Write, Read | | | | | | |

| BITFIELD | BITS | DESCRIPTION | DECODE |
|---|---|---|---|
| RRLowPB12 | 7 | DVS Round-Robin High Performance Feature Step 0x12 | Refer to register 0x20 RRLowPB00 bit |
| RRVset12 | 6:0 | DVS Round-Robin Voltage Value Step 0x12 | Refer to register 0x02 BBstVSet bit |

## RRVset13 (0x33)

| BIT | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| **Field** | RRLowPB13 | RRVset13[6:0] | | | | | | |
| **Reset** | | | | | | | | |
| **Access Type** | Write, Read | Write, Read | | | | | | |

| BITFIELD | BITS | DESCRIPTION | DECODE |
|---|---|---|---|
| RRLowPB13 | 7 | DVS Round-Robin High Performance Feature Step 0x13 | Refer to register 0x20 RRLowPB00 bit |
| RRVset13 | 6:0 | DVS Round-Robin Voltage Value Step 0x13 | Refer to register 0x02 BBstVSet bit |

## LockMsk (0x50)

| BIT | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| **Field** | – | – | – | – | – | – | – | BBLck |
| **Reset** | – | – | – | – | – | – | – | 0b1 |
| **Access Type** | – | – | – | – | – | – | – | Write, Read |

| BITFIELD | BITS | DESCRIPTION | DECODE |
|---|---|---|---|
| BBLck | 0 | Lock Mask for Buck-Boost Registers | 0x0: Not masked from locking/unlocking<br>0x1: Masked from locking/unlocking |

## LockUnlock (0x51)

| BIT | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| **Field** | PASSWD[7:0] | | | | | | | |
| **Reset** | 0xFF | | | | | | | |
| **Access Type** | Write, Read | | | | | | | |

| BITFIELD | BITS | DESCRIPTION |
|---|---|---|
| PASSWD | 7:0 | Lock/Unlock Password<br>Write 0xAA with BBLck unmasked to lock the BBstVSet register (0x02)<br>Write 0x55 with BBLck unmasked to unlock the BBstVSet register (0x02)<br>All Other Codes: no effect |

## DVSCfg (0x54)

| BIT | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| **Field** | – | – | – | – | I2CLkptDis | RRWrap | RREna | DVSSource |
| **Reset** | – | – | – | – | | | | |
| **Access Type** | – | – | – | – | Write, Read | Write, Read | Write, Read | Write, Read |

| BITFIELD | BITS | DESCRIPTION | DECODE |
|---|---|---|---|
| I2CLkptDis | 3 | Look-up Table Disable<br>Look-up table is used to set optimal BBstIPSet1 in various BBOut ranges according to OTP register settings of bits IPm50, IPm60M50, IPm70M60 and IPM70.<br>Look-up table can be disabled only in I2C mode. When disabled, peak current is determined by bitfield BBstIPSet1 setting. | 0x0: Look-up table enabled for $I^2C$<br>0x1: Look-up table disabled for $I^2C$ |

| BITFIELD | BITS | DESCRIPTION | DECODE |
|---|---|---|---|
| RRWrap | 2 | Round-Robin Wrap<br>Defines if the Round-Robin DVS modes stops at the last value (if set to 0) or wraps back to the first one (if set to 1). | 0x0: Round-Robin does not wrap around<br>0x1: Round-Robin does wrap around |
| RREna | 1 | DVS Round-Robin Enable<br>After changing this value, wait at least 300µs before trying to send another DVS command, regardless of the DVS mode.<br>DVSSource setting is ignored if this bit is set to 1. | 0x0: Round-Robin disabled<br>0x1: Round-Robin enabled |
| DVSSource | 0 | DVS Source<br>Choose interface for DVS. After changing this value, wait at least 300µs before trying to send another DVS command, regardless of the DVS mode. | 0x0: $I^2C$ enabled to set DVS<br>0x1: Dedicated pins enabled to set DVS |

## RRCfg1 (0x55)

| BIT | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| **Field** | – | RRClkPolarity | RRTimeoutRes | RRSize[4:0] | | | | |
| **Reset** | – | | | | | | | |
| **Access Type** | – | Write, Read | Write, Read | Write, Read | | | | |

| BITFIELD | BITS | DESCRIPTION | DECODE |
|---|---|---|---|
| RRClkPolarity | 6 | Round-Robin Clock Polarity<br>If 0 the clock is active low (voltage is updated on its falling edge), if 1 the clock is active high (voltage is updated on its rising edge).<br>This bit should not be changed when Round-Robin is enabled. | 0x0: Falling edge active<br>0x1: Rising edge active |
| RRTimeoutRes | 5 | Round Robin Timeout Reset<br>This bit determines if Round-Robin pointer is reset after timeout.<br>This bit should not be changed when Round-Robin is enabled. | 0x0: Timeout does not reset Round Robin pointer<br>0x1: Timeout resets Round Robin pointer |
| RRSize | 4:0 | Number of Steps in Round-Robin Mode<br>This bit should not be changed when Round-Robin is enabled. | 0x0: 0 Step (initial voltage)<br>0x1: 1 Step<br>...<br>0x13: 19 Steps |

## RRCfg2 (0x56)

| BIT | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| **Field** | – | – | – | – | – | RRTimeoutLength[2:0] | | |
| **Reset** | – | – | – | – | – | | | |

| Access Type | – | – | – | – | – | Write, Read |
|---|---|---|---|---|---|---|

| BITFIELD | BITS | DESCRIPTION | DECODE |
|---|---|---|---|
| RRTimeoutLength | 2:0 | Round Robin Timeout Duration<br>This bit should not be changed when Round-Robin is enabled. | 0x0: Timeout disabled<br>0x1: 500µs<br>0x2: 1ms<br>0x3: 2ms<br>0x4: 4ms<br>0x5: 8ms<br>0x6: 16ms<br>0x7: Reserved |

## SPICfg (0x57)

| BIT | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Field | – | – | – | – | – | – | – | SPITimeoutEna |
| Reset | – | – | – | – | – | – | – | |
| Access Type | – | – | – | – | – | – | – | Write, Read |

| BITFIELD | BITS | DESCRIPTION | DECODE |
|---|---|---|---|
| SPITimeoutEna | 0 | Pseudo-SPI Timeout Enable | 0x0: Pseudo-SPI timeout disabled<br>0x1: Pseudo-SPI timeout enabled |

## ConfOtp (0x6E)

| BIT | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Field | – | – | – | – | – | – | – | FpwmFast |
| Reset | – | – | – | – | – | – | – | |
| Access Type | – | – | – | – | – | – | – | Write, Read |

| BITFIELD | BITS | DESCRIPTION |
|---|---|---|
| FpwmFast | 0 | In Round-Robin and pseudo-SPI modes, this bit sets high performance feature (0 = Fast and 1 = FPWM).<br>In $I^2C$ mode, this bit selects the high performance feature for status check. BB_LOWPB reads 1 in any of the following three conditions.<br>1) FPWM = 1, FAST = 0, FpwmFast = 1<br>2) FPWM = 0, FAST = 1, FpwmFast = 0<br>3) FPWM = 1, FAST = 1, FpwmFast = 0 or 1 |

## FuncDef (0x6F)

| BIT | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Field | – | – | – | – | LtchOffVddUvlo | LtchOffBBOutUvlo | LtchOffBst | LtchOffThm |

| | | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| **Reset** | – | – | – | – | | | | |
| **Access Type** | – | – | – | – | Write, Read | Write, Read | Write, Read | Write, Read |

| BITFIELD | BITS | DESCRIPTION | DECODE |
|---|---|---|---|
| LtchOffVddUvlo | 3 | Latch Off Bit for Vdd or Bat UVLO Fault | 0x0: Fault is cleared at the end of the 1s autoretry time<br>0x1: Operation is resumed only after cycling (writing 0 and then 1) bit BBstEna |
| LtchOffBBOutUvlo | 2 | Latch Off Bit for BBOut UVLO Fault | 0x0: Fault is cleared at the end of the 1s autoretry time<br>0x1: Operation is resumed only after cycling (writing 0 and then 1) bit BBstEna |
| LtchOffBst | 1 | Latch Off Bit for Bootstrap Fault | 0x0: Fault is cleared at the end of the 1s autoretry time<br>0x1: Operation is resumed only after cycling (writing 0 and then 1) bit BBstEna |
| LtchOffThm | 0 | Latch Off Bit for Thermal Fault | 0x0: Fault is cleared at the end of the 1s autoretry time<br>0x1: Operation is resumed only after cycling (writing 0 and then 1) bit BBstEna |

## Register Values

The following tables provide the device and register bit default values for the various available parts.

**Table 5. Register Bit Default Values**

| REGISTER BITS | MAX20363A |
|---|---|
| BBstLowEMIB | Nominal Slope |
| BBstEna | Enabled |
| BBstFast | Disabled |
| BBFHighSh | Enabled |
| BBstActDsc | Enabled |
| BBstPsvDsc | Enabled |
| BBstFpwm | Disabled |
| BBstVSet | 5V |
| BBstIPSet2 | 300mA |
| BBstIPSet1 | 400mA |
| BBIMaxN | -1000mA |
| BBIMaxP | 1000mA |
| BBIPwpMaxP | 750mA |
| ChgModDoneMsk | Not Masked |
| BBstOnMsk | Not Masked |
| BBL2P2Sel | 1µH Inductor |
| BBstIpPadPEnb | Enabled |
| BBFetScale | Full Power FETS |

| | |
|---|---|
| LtchOffVddUvlo | Autoretry enabled |
| LtchOffBBOutUvlo | Autoretry enabled |
| LtchOffBst | Autoretry enabled |
| LtchOffThm | Autoretry enabled |
| FpwmFast | Fast |
| SPITimeoutEna | Enabled |
| DVSSource | $I^2C$ |
| i2c_2nd_sid | 0x68 |
| IPm60M50 | 300mA |
| IPm50 | 250mA |
| IPM70 | 400mA |
| IPm70M60 | 350mA |
| IPPwp2 | 200mA |
| IPPwp1 | 200mA |

**Table 6. Register Default Values**

| REGISTER | NAME | MAX20363A |
|---|---|---|
| 0x00 | ChipID | 0x02 |
| 0x01 | BBstCfg0 | 0x6F |
| 0x02 | BBstVSet | 0x46 |
| 0x03 | BBstISet | 0xCC |
| 0x04 | BBstIMaxN | 0x10 |
| 0x05 | BBstIMaxP | 0x14 |
| 0x06 | BBstIPwpMaxP | 0x0F |
| 0x08 | BBstCfg1 | 0x00 |
| 0x10 | Status | - |
| 0x11 | Int | 0x00 |
| 0x12 | Mask | 0x10 |
| 0x13 | CommInt | 0x00 |
| 0x14 | CommMsk | 0x00 |
| 0x15 | BBFsmState | - |
| 0x1E | BBVset | 0x46 |
| 0x1F | RRpoint | 0x00 |
| 0x20 | RRVset00 | 0x00 |
| 0x21 | RRVset01 | 0x00 |
| 0x22 | RRVset02 | 0x00 |
| 0x23 | RRVset03 | 0x00 |
| 0x24 | RRVset04 | 0x00 |
| 0x25 | RRVset05 | 0x00 |
| 0x26 | RRVset06 | 0x00 |
| 0x27 | RRVset07 | 0x00 |

| | | |
|---|---|---|
| 0x28 | RRVset08 | 0x00 |
| 0x29 | RRVset09 | 0x00 |
| 0x2A | RRVset0A | 0x00 |
| 0x2B | RRVset0B | 0x00 |
| 0x2C | RRVset0C | 0x00 |
| 0x2D | RRVset0D | 0x00 |
| 0x2E | RRVset0E | 0x00 |
| 0x2F | RRVset0F | 0x00 |
| 0x30 | RRVset10 | 0x00 |
| 0x31 | RRVset11 | 0x00 |
| 0x32 | RRVset12 | 0x00 |
| 0x33 | RRVset13 | 0x00 |
| 0x50 | LockMsk | 0x01 |
| 0x51 | LockUnlock | - |
| 0x54 | DVSCfg | 0x00 |
| 0x55 | RRCfg1 | 0x00 |
| 0x56 | RRCfg2 | 0x00 |
| 0x57 | SPICfg | 0x01 |
| 0x6E | ConfOtp | 0x08 |
| 0x6F | FuncDef | 0x00 |

# OUTLINE DIMENSIONS

21-100680

# ORDERING GUIDE

Table 7. Ordering Guide

| MODEL | TEMPERATURE RANGE | PACKAGE DESCRIPTION | PACKAGE OPTION |
|---|---|---|---|
| MAX20363AEWN+ | -40°C to +85°C | 18 WLP (2.43mm x 1.25mm) | W181A2+1 |
| MAX20363AEWN+T | -40°C to +85°C | 18 WLP (2.43mm x 1.25mm) | W181A2+1 |

# REVISION HISTORY

| REVISION NUMBER | REVISION DATE | DESCRIPTION | PAGES CHANGED |
|---|---|---|---|
| 0 | 6/24 | Initial release | — |
| 1 | 6/25 | Updated Table 6 | 47 |