MAX20086–MAX20089

Dual/Quad Camera Power Protectors

General Description

The MAX20086–MAX20089 dual/quad camera power protector ICs deliver up to 600mA load current to each of their four output channels. Each output is individually protected from short-to-battery, short-to-ground, and overcurrent conditions. The ICs operate from a 3V to 5.5V supply and with a 3V to 15V camera supply. The input-to-output voltage drop is only 110mV (typ) at 300mA.

The ICs provide an enable input and I²C interface to read the diagnostic status of the device. An on-board ADC enables reading of the current through each switch. The ASIL B- and ASIL D-compliant versions include support for reading an additional seven diagnostic measurements through the ADC, ensuring high-fault coverage.

The MAX20086–MAX20089 include overtemperature shutdown and overcurrent limiting on each output channel separately. All devices are designed to operate from -40°C to +125°C ambient temperature.

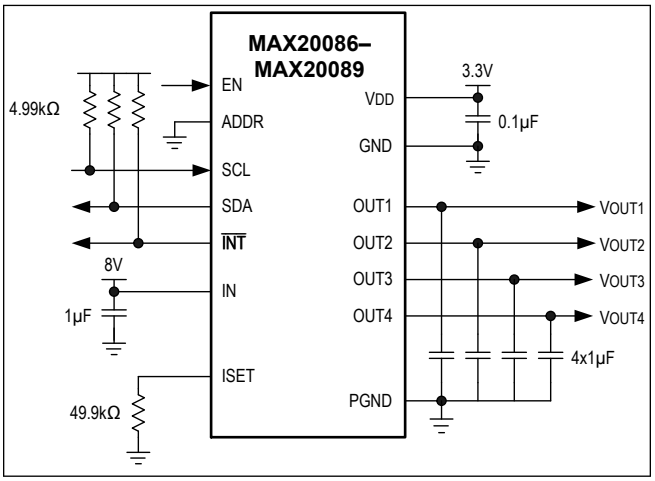
Applications

- Power-over-Coax for Radar and Camera Modules

Benefits and Features

- Small Solution
  - Up to Four 600mA Protection Switches
  - 3V to 15V Input Supply
  - 3V to 5.5V Device Supply
  - 26V Short-to-Battery Isolation
  - Adjustable Current Limit (100mA to 600mA)
  - Parallel Multiple Channels for Higher Current
  - Selectable I²C Addresses
  - Small (4mm x 4mm) 20-Pin SWTQFN and WETQFN Packages
- Precision
  - ±8% Current-Limit Accuracy
  - 0.5ms Soft-Start
  - 0.25ms Soft-Shutdown
  - 0.3µA Shutdown Current
  - 110mV Drop at 300mA
- Designed for Safety Applications
  - ASIL B/D Compliant
  - Short to V_{BAT}/GND Diagnostics
  - Differential Output Over/Undervoltage Diagnostics
  - Input Over/Undervoltage Diagnostics
  - Individual 8-Bit Current, Output Voltage, and Supply Readings over I²C
  - Autoretry on Fault
- AEC-Q100, -40°C to +125°C

Typical Application Diagram



Ordering Information appears at the end of data sheet.

19-100154; Rev 7; 7/23

Absolute Maximum Ratings

IN to PGND ..... -0.3V to +20V
OUT_ to IN ..... -20V to +26V
OUT_ to PGND ..... -0.3V to +26V
V_{DD} to GND ..... -0.3V to +6V
EN, ISET to GND ..... -0.3V to V_{DD} + 0.3V
SDA, SCL, ADDR, $\overline{INT}$ to GND ..... -0.3V to +6.0V
GND to PGND ..... -0.3V to +0.3V

Output Short-Circuit Duration, Continuous
Maximum Continuous Output Current 1A
Continuous Power Dissipation (T_A = +70°C)
20-Pin SWTQFN-EP (derate 30.3 mW/°C > +70°C) ... 2424mW
Operating Temperature ..... -40°C to +125°C
Junction Temperature ..... +150°C
Storage Temperature Range ..... -65°C to +150°C
Lead Temperature Range ..... +300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Package Information

20 TQFN-EP

Package Code	T2044Y+4C (SWTQFN-EP)	T2044Y+5C (WETQFN-EP)
Outline Number	21-100068	21-100318
Land Pattern Number	90-0409	90-100131
THERMAL RESISTANCE, SINGLE-LAYER BOARD		
Junction to Ambient (θ_{JA})	48°C/W	48°C/W
Junction to Case (θ_{JC})	2°C/W	2°C/W
THERMAL RESISTANCE, FOUR-LAYER BOARD		
Junction to Ambient (θ_{JA})	33°C/W	33°C/W
Junction to Case (θ_{JC})	2°C/W	2°C/W

For the latest package outline information and land patterns (footprints), go to *www.maximintegrated.com/packages*. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to *www.maximintegrated.com/thermal-tutorial*.

Electrical Characteristics

(V_{DD} = 5V, V_{IN} = 6.5V. T_A = T_J = -40°C to +125°C, unless otherwise noted. Typical values are at T_A = +25°C under normal conditions, unless otherwise noted.) (*Note 1*)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Supply Voltage Range	V_{DD}		3.0		5.5	V
Shutdown Supply Current	I_{SHDN}	V_{EN} = 0V, T_A = +25°C		3	6.5	µA
Supply Current	I_{VDD}	V_{EN} = 5V		2		mA
V_{DD} Undervoltage Lockout	V_{UVLO}	Falling	2.5	2.7	2.9	V
V_{DD} Undervoltage Hysteresis	V_{UVHYS}			150		mV
V_{DD} Overvoltage Lockout	V_{OVLO}	Rising	5.5	5.7	5.9	V

Electrical Characteristics (continued)

(V_{DD} = 5V, V_{IN} = 6.5V. T_A = T_J = -40°C to +125°C, unless otherwise noted. Typical values are at T_A = +25°C under normal conditions, unless otherwise noted.) (*Note 1*)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
V_{DD} Overvoltage Hysteresis	V_{OVHYS}			100		mV
Thermal-Shutdown Temperature	T_{SHDN}	T_J rising		165		°C
Thermal-Shutdown Hysteresis	T_{HYST}			15		°C
SWITCH						
Input Voltage Range	V_{IN}		3.0		15	V
Input Undervoltage Lockout	V_{INUVLO}	Falling	2.5	2.7	2.9	V
Input Undervoltage-Lockout Hysteresis	V_{INUVH}			150		mV
Input Overvoltage Threshold	V_{INOV}	Rising	15.8	16.5	17.1	V
Input Overvoltage Hysteresis				170		mV
Input Current	I_{IN}	V_{EN} = 0V, T_A = +25°C		0.4		µA
		All switches enabled, no load		1.0		mA
On-Resistance				400	700	mΩ
Soft-Start Ramp Time	I_{URAMP}	0mA to I_{LIM}		0.5		ms
Soft-Shutdown Ramp Time	I_{DRAMP}	From full-on I_{LIM} value to high impedance, any condition that turns off a channel		0.25		ms
Overvoltage Threshold		V_{OUT} - V_{IN}, V_{OUT} rising, output disabled	0.09	0.15	0.25	V
Overvoltage Filter Time		1V above threshold, for short to V_{BAT} detection		1		µs
Undervoltage Threshold		V_{IN} - V_{OUT}, V_{OUT} falling	0.45	0.55	0.65	V
Undervoltage Hysteresis				40		mV
Undervoltage Filter Time		1V below threshold		1		µs
CURRENT LIMIT						
ISET Operating Range			72		672	mA
OUT_ Default Current		ISET out of operating range		600		mA
ISET Pullup Current		V_{ISET} = 1.25V	11.9	12.5	13.1	µA
Forward Current Limit	I_{LIM}	R_{ISET} = 25kΩ		150		mA
		R_{ISET} = 50kΩ, V_{IN} - V_{OUT} = 2V	-8%	300	+8%	
		R_{ISET} = 100kΩ	-8%	600	+8%	
Hard Short-Detection-Comparator Threshold			1.8	1.9	2.0	V
Hard Short-Detection Time		Output in current limit, hard short detected		10		ms
Shorted Output-Detection Time		Output in current limit, UV detected		20		ms

Electrical Characteristics (continued)

(V_{DD} = 5V, V_{IN} = 6.5V. T_A = T_J = -40°C to +125°C, unless otherwise noted. Typical values are at T_A = +25°C under normal conditions, unless otherwise noted.) (*Note 1*)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Shorted Output-Retry Time			225	250	275	ms
ANALOG						
V_{IN} Divide Ratio			-2%	14.328	+2%	V/V
V_{DD} Divide Ratio			-2%	5.1	+2%	V/V
V_{ISET} Divide Ratio			-2%	1.02	+2%	V/V
V_{OUT} Divide Ratio		V_{IN} - V_{OUT} = 200mV, excluding ADC error	-5%	14.328	+5%	V/V
Output-Current Reading		I_{OUT} = 300mA, excluding ADC error	-9%	0.616	+9%	A/V
V_{IN} Voltage LSB				70		mV
V_{DD} Voltage LSB				25		mV
V_{ISET} Voltage LSB				5		mV
V_{OUT} Voltage LSB				70		mV
Output-Current LSB				3		mA
ADC						
Resolution				8		Bits
Relative Accuracy	INL				±1.5	Bits
Differential Accuracy	DNL				±1	Bits
Offset Error					±2.2	Bits
Conversion Time				1		ms
Track-and-Hold Acquisition Time				20		µs
Reference		Full-scale reading	1.23%	1.25	1.27%	V
DIGITAL OUTPUT ($\overline{INT}$)						
Digital Output Low Level		V_{DD} = 3.0V, I_{SINK} = -2mA			0.2	V
Digital Output leakage		ERR, SDA = V_{DD} = 5.5V			1	µA
SDA OUTPUT						
SDA Output Low	V_{OL_SDA}	I_{SINK} = 13mA			0.4	V
DIGITAL INPUTS (EN, SDA, SCL, ADDR)						
Input High Level		Rising	1.3			V
Input Low Level		Falling			0.5	V
Hysteresis				0.1		V
EN Pulldown Current		V_{EN} = 5.0V		1		µA
ADDR Pulldown Current		V_{ADDR} = 5.0V		3		µA
Digital Input Leakage		0 or 5.5V, V_{DD} = 5.5V, T_A = +25°C			1	µA
I^2C INTERFACE						
Clock Frequency	f_{SCL}				1.1	MHz
Setup Time (Repeated) START	$t_{SU:STA}$		260			ns

Electrical Characteristics (continued)

(V_{DD} = 5V, V_{IN} = 6.5V. T_A = T_J = -40°C to +125°C, unless otherwise noted. Typical values are at T_A = +25°C under normal conditions, unless otherwise noted.) (*Note 1*)

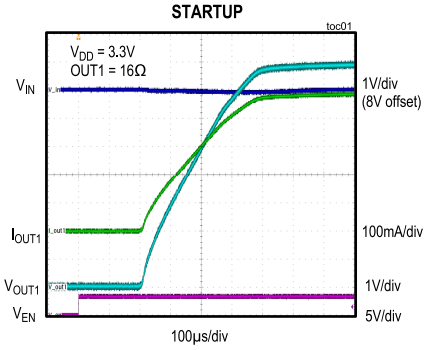
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Hold Time (Repeated) START	$t_{HD:STA}$		260			ns
SCL Low Time	t_{LOW}		350			ns
SCL High Time	t_{HIGH}		260			ns
Data Setup Time	$t_{SU:DAT}$		50			ns
Data Hold Time	$t_{HD:DAT}$		0			ns
Setup Time for STOP Condition	$t_{SU:STO}$		260			ns
Spike Suppression				50		ns

Note 1: All units are 100% production tested at +25°C. All temperature limits are guaranteed by design.

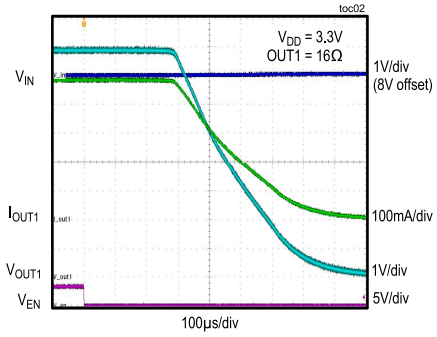
Typical Operating Characteristics

(T_A = +25°C, unless otherwise noted.)

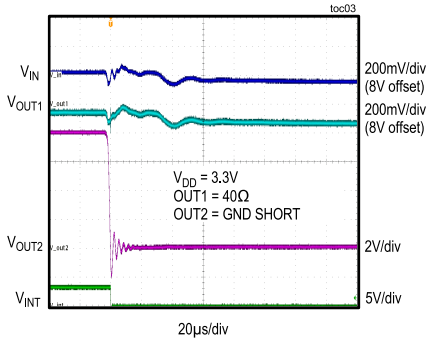
STARTUP



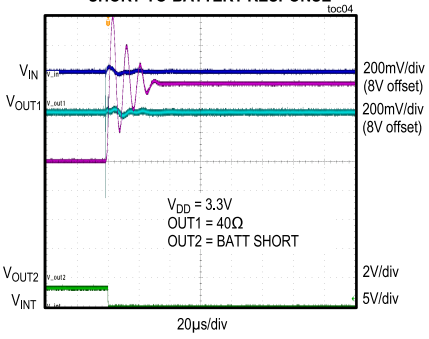
SHUTDOWN



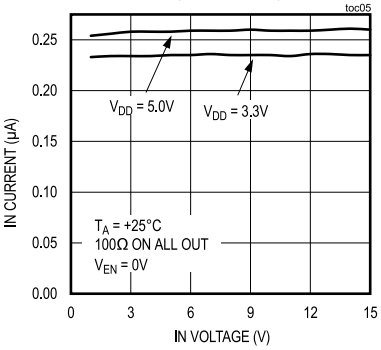
SHORT-TO-GROUND RESPONSE



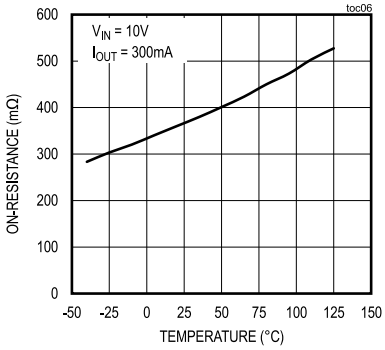
SHORT-TO-BATTERY RESPONSE



IN PIN LEAKAGE vs. VOLTAGE (IC DISABLED)

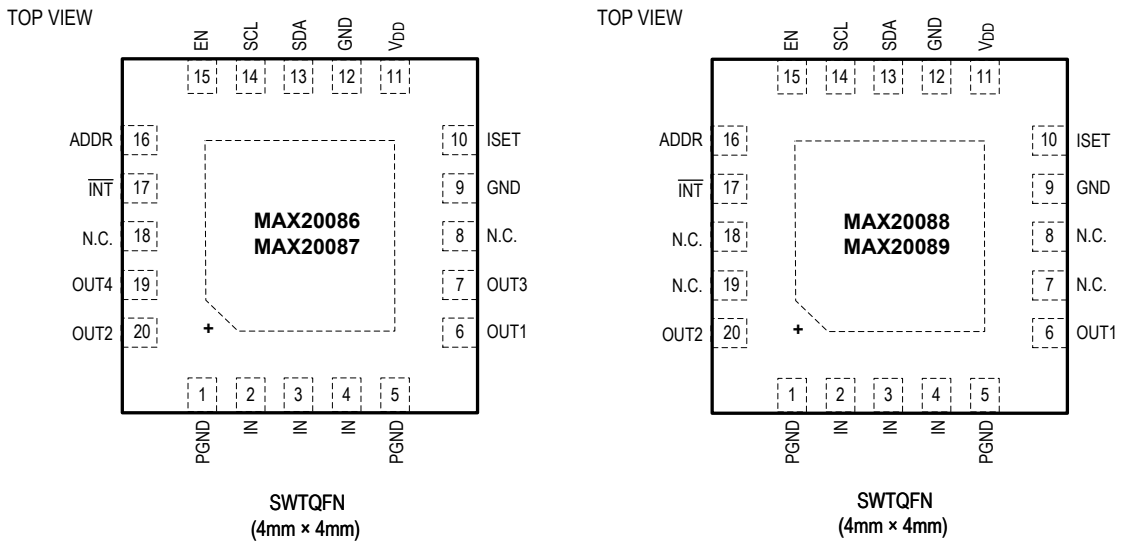


ON-RESISTANCE vs. TEMPERATURE

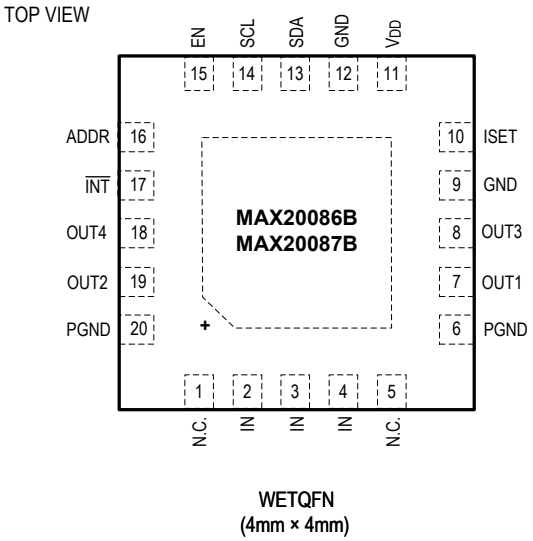


Pin Configurations

T2044Y+4C



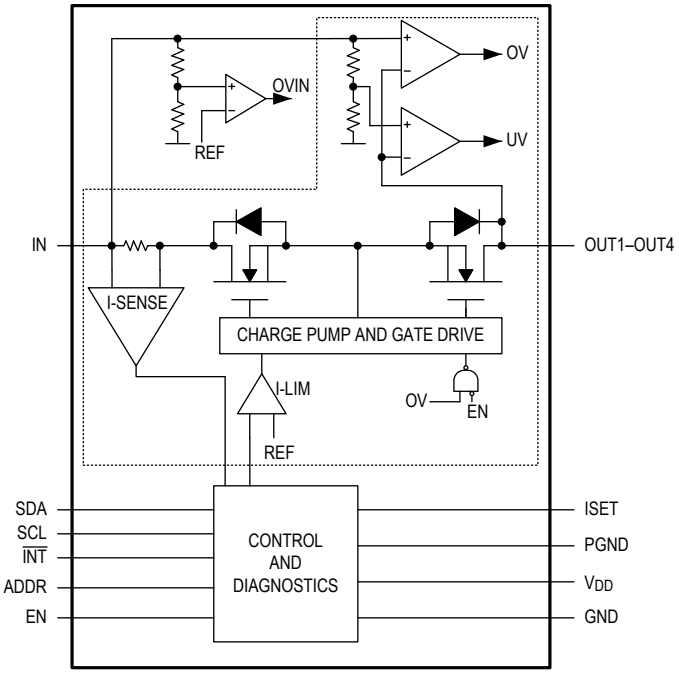
T2044Y+5C



Pin Description

PIN			NAME	FUNCTION
MAX20086 MAX20087	MAX20088 MAX20089	MAX20086B MAX20087B		
1, 5	1, 5	20, 6	PGND	Power Ground. Connect GND and PGND together to the exposed pad (EP).
2–4	2–4	2–4	IN	Camera Supply. Connect to the output of the DC-DC converter feeding the cameras.
6	6	7	OUT1	Protected Camera Supply Output 1. Connect a 1µF or larger ceramic capacitor from OUT1 to PGND.
7	—	8	OUT3	Protected Camera Supply Output 3. Connect a 1µF or larger ceramic capacitor from OUT3 to PGND.
8, 18	7, 8, 18, 19	1, 5	N.C.	Not Connected. Leave unconnected or connect to ground.
9, 12	9, 12	9, 12	GND	Analog Ground
10	10	10	ISET	Output Current-Limit Setting. Connect a resistor from ISET to GND to set the per-channel current limit.
11	11	11	V_{DD}	Device Input Supply. Connect a 100nF or larger ceramic capacitor from V_{DD} to GND.
13	13	13	SDA	I^2C Data I/O
14	14	14	SCL	I^2C Clock Input
15	15	15	EN	Active-High Enable Input. Drive EN high for normal operation. On the rising edge, the enabled channels (in the CONFIG register) enter soft-start and on the falling edge, the channels turn off.
16	16	16	ADDR	I^2C Address Select. Connect to ground or V_{DD} to select between two different I^2C addresses.
17	17	17	$\overline{INT}$	Active-Low, Open-Drain Interrupt Output. External pullup resistor required, if used. See Table 3 and Table 11 for full behavior.
19	—	18	OUT4	Protected Camera Supply Output 4. Connect a 1µF or larger ceramic capacitor from OUT4 to PGND.
20	20	19	OUT2	Protected Camera Supply Output 2. Connect a 1µF or larger ceramic capacitor from OUT2 to PGND.
—	—	—	EP	Exposed Pad. Connect EP to multiple ground planes with a grid of vias for effective thermal dissipation.

Internal Block Diagram



Detailed Description

The MAX20086–MAX20089 ICs are 2-/4-channel high-side isolation/protection switches with internal current limiting and diagnostics. The input supply range is from 3V to 15V, while the output can tolerate up to 26V. Each output has an accurate current limit of ±8% to protect the input supply from overload and short-circuit conditions. In a short-to-battery on the output, the switch opens to prevent back feeding of the battery to the input supply. The internal 8-bit ADC enables reading of the current from each output digitally, simplifying system design. The ICs can be configured and the status read for each channel through the I²C interface. Individual channels can also be turned on/off through I²C.

The ICs are ASIL B compliant, without additional software diagnostics. The internal 8-bit ADC is capable of reading the current and output voltage across each output, along with the voltages of the input supplies and current setting. This can increase the diagnostic coverage to achieve ASIL D compliance.

The ICs include overtemperature shutdown and overcurrent limiting separately on each channel. All devices are designed to operate from -40°C to +125°C ambient temperature.

I²C Interface

The ICs feature an I²C, 2-wire serial interface consisting of a serial-data line (SDA) and a serial-clock line (SCL). SDA and SCL facilitate communication between the ICs and the controller at clock rates up to 1MHz. The controller, typically a microcontroller, generates SCL and initiates data transfer on the bus. Figure 1 shows the 2-wire interface timing diagram.

A controller device communicates to the ICs by transmitting the proper address followed by the data word. Each transmit sequence is framed by a START (S) or Repeated START (Sr) condition, and a STOP (P) condition. Each word transmitted over the bus is 8 bits long and is always followed by an acknowledge clock pulse.

The IC's SDA line operates as both an input and an open-drain output. A pullup resistor greater than 500Ω is required on the SDA bus. The ICs' SCL line operates as an input only. A pullup resistor greater than 500Ω is required on SCL if there are multiple controllers on the bus, or if the controller in a single-controller system has an open-drain SCL output. Series resistors in line with SDA and SCL are optional. The SCL and SDA inputs suppress noise spikes to ensure proper device operation, even on a noisy bus.

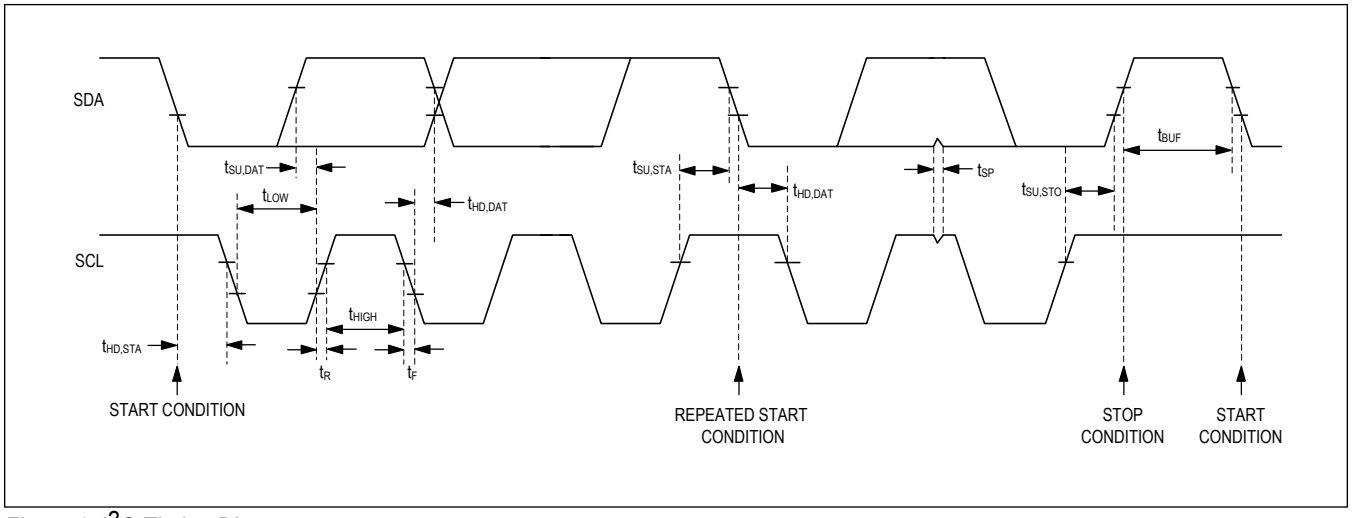


Figure 1. I²C Timing Diagram

Bit Transfer

One data bit is transferred during each SCL cycle. The data on SDA must remain stable during the high period of the SCL pulse. Changes in SDA while SCL is high are control signals (see the *STOP and START Conditions* section). SDA and SCL idle high when the I²C bus is not busy.

STOP and START Conditions

A controller device initiates communication by issuing a START condition. A START condition is a high-to-low transition on SDA with SCL high. A STOP condition is a low-to-high transition on SDA while SCL is high (see Figure 2). A START (S) condition from the controller signals the beginning of a transmission to the IC. The controller terminates transmission, and frees the bus, by issuing a STOP (P) condition. The bus remains active if a Repeated START (Sr) condition is generated instead of a STOP condition.

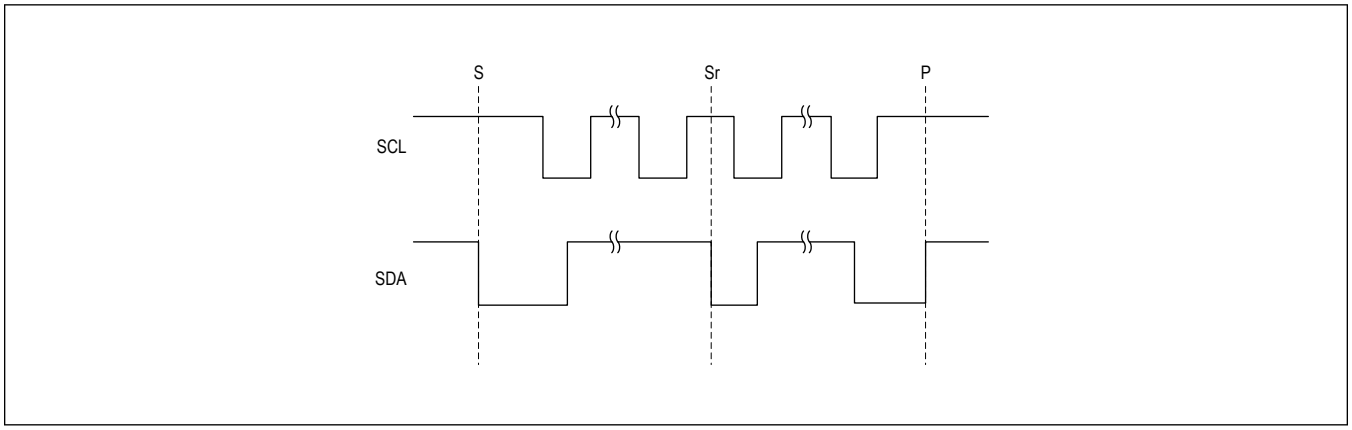


Figure 2. START, STOP, and Repeated START Conditions

Early STOP Condition

The device recognizes a STOP condition at any point during data transmission, except if the STOP condition occurs in the same high pulse as a START condition.

Clock Stretching

In general, the clock-signal generation for the I²C bus is the responsibility of the controller device. The I²C specification allows slow target devices to alter the clock signal by holding down the clock line. The process in which a target device holds down the clock line is typically called “clock stretching.” The ICs do not use any form of clock stretching to hold down the clock line.

I²C General Call Address

The ICs do not implement the I²C specification’s “general call address.” If the device sees the general call address (0b0000_0000), it does not issue an acknowledge.

Target Address

Once the device is enabled, the I²C target address is set by the ADDR pin (see Table 1). The address is defined as the 7 most significant bits (MSBs) followed by the R/W bit. Set the R/W bit to ‘1’ to configure the device to read mode. Set the R/W bit to ‘0’ to configure the device to write mode. The address is the first byte of information sent to the device after the START condition.

Table 1. I²C Target Addresses

ADDR PIN	A6	A5	A4	A3	A2*	A1*	A0	7-BIT ADDRESS	WRITE	READ
0	0	1	0	1	0	0	0	0x28	0x50	0x51
1	0	1	0	1	0	0	1	0x29	0x52	0x53
0	0	1	0	1	0	1	0	0x2A	0x54	0x55
1	0	1	0	1	0	1	1	0x2B	0x56	0x57
0	0	1	0	1	1	0	0	0x2C	0x58	0x59
1	0	1	0	1	1	0	1	0x2D	0x5A	0x5B

Table 1. I²C Target Addresses (continued)

ADDR PIN	A6	A5	A4	A3	A2*	A1*	A0	7-BIT ADDRESS	WRITE	READ
0	0	1	0	1	1	1	0	0x2E	0x5C	0x5D
1	0	1	0	1	1	1	1	0x2F	0x5E	0x5F

*A2 and A1 can be customized at the factory.

Acknowledge

The acknowledge bit (ACK) is a clocked 9th bit that the device uses to handshake receipt each byte of data (see Figure 3). The device pulls down SDA during the controller-generated 9th clock pulse. The SDA line must remain stable and low during the high period of the acknowledge clock pulse. Monitoring ACK allows for detection of unsuccessful data transfers. An unsuccessful data transfer occurs if a receiving device is busy, or if a system fault has occurred. In the event of an unsuccessful data transfer, the bus controller can reattempt communication.

Write Data Format

A write to the device includes transmission of a START condition, the target address with the write bit set to '0', 1 byte of data to the register address, 1 byte of data to the command register, and a STOP condition. Figure 4 illustrates the proper format for one frame.

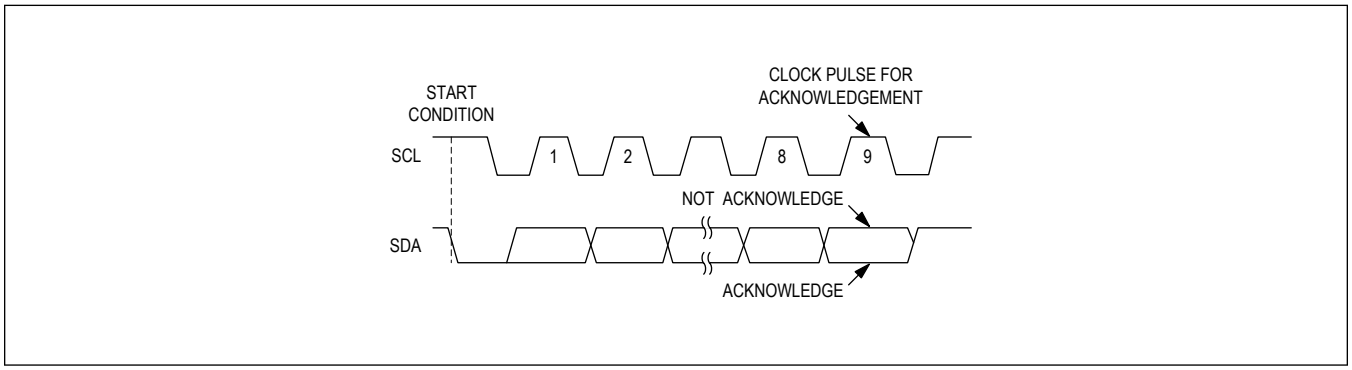


Figure 3. Acknowledge Condition

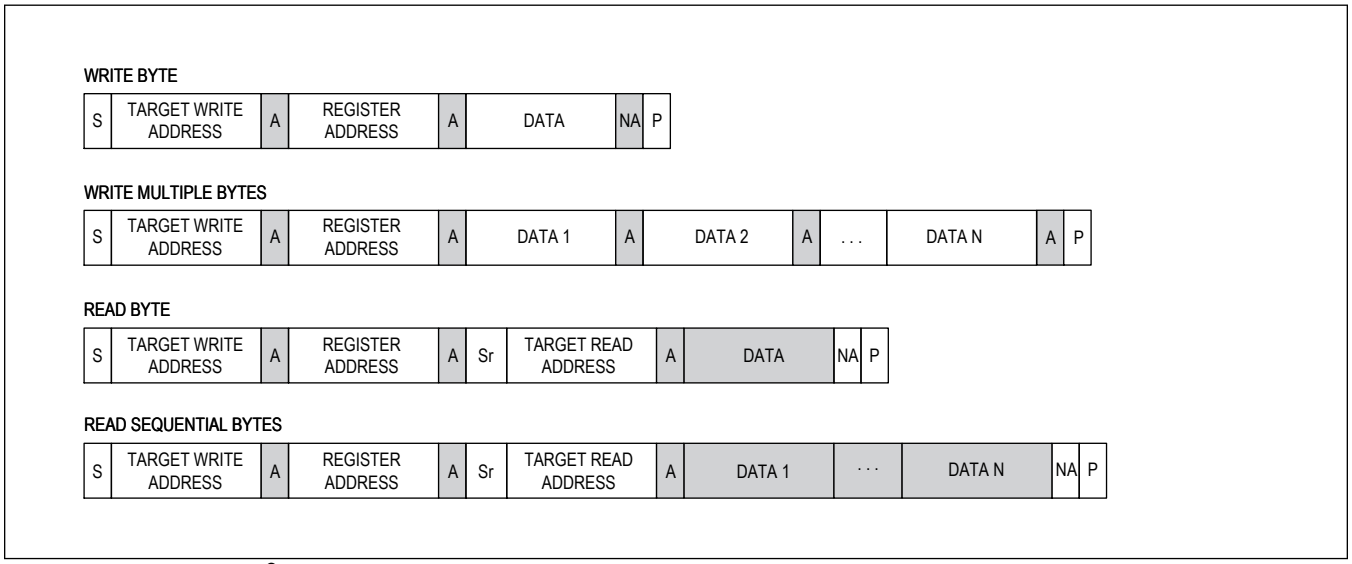


Figure 4. Data Format of I²C Interface

Read Data Format

A read from the device includes transmission of a START condition, the target address with the write bit set to '0', 1 byte of data to the register address, restart condition, the target address with the read bit set to '1', 1 byte of data to the command register, and a STOP condition. Figure 4 illustrates the proper format for one frame.

Enable Control Input (EN)

The EN input activates the device from the low-power shutdown state. The I^2C interface to the device is active when V_{DD} is present, even with the EN pin low. When the the EN input goes high, channels with CONFIG.EN[4:1] bits set are enabled. If the EN pin is toggled low, the STAT1/2 faults continue to hold last value and are cleared after reading. If the EN pin is toggled low, the ADC registers continue to hold the last value (they are not cleared after reading). The EN pin should be high for the diagnostics (STAT1, STAT2, and ADC) to update.

Interrupt Output ($\overline{INT}$)

The ICs feature an open-drain fault-interrupt output that asserts when any unmasked fault status bit is set. After a fault clears, the clearing of the corresponding status bit depends on CLR bit setting. Connect a pullup resistor from $\overline{INT}$ to the system I/O supply. The pullup resistance should normally be ≥ 2kΩ to ensure that device can pull down to the specified voltage level.

Table 2. Register Map

REGISTER	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0	CMD	R/W	POWER-ON RESET
MASK	OVTST	ACCM	TSM	VDDM	VINM	OCM	OVM	UVM	0x00	R/W	0x00
CONFIG	MUX1	MUX0	ENC	CLR	EN4	EN3	EN2	EN1	0x01	R/W	0x1F
ID	—	—	ID[5:4]		R[3:0]				0x02	R	See Table 5 description
STAT1	—	—	ISET	ACC	OVIN	UVIN	OVDD	UVDD	0x03	R	0x00
STAT2	TS2	OC2	OV2	UV2	TS1	OC1	OV1	UV1	0x04	R	0x00
	TS4	OC4	OV4	UV4	TS3	OC3	OV3	UV3	0x05	R	0x00
ADC1	D[7:0]								0x06	R	0x00
ADC2	D[7:0]								0x07	R	0x00
ADC3	D[7:0]								0x08	R	0x00
ADC4	D[7:0]								0x09	R	0x00

Table 3. Interrupt Mask Register (MASK)

MASK								
BIT NO.	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
NAME	OVTST	ACCM	TSM	VDDM	VINM	OCM	OVM	UVM
POR	0	0	0	0	0	0	0	0

BIT	BIT DESCRIPTION
OVTST	**Overvoltage Diagnostics Enable:** The EN[4:1] bits must be low to run the diagnostics. The OVIN and OV[4:1] bits in the status registers are set to '1' to indicate that comparators are operational. 0 = OV comparators function normally 1 = OV comparator diagnostics enable
ACCM	0 = ADC conversion complete (ACC), mapped to $\overline{INT}$ pin 1 = Mask ADC conversion complete (ACC)
TSM	0 = Thermal-shutdown faults TS[4:1] mapped to $\overline{INT}$ pin 1 = Mask thermal-shutdown fault
VDDM	0 = OVDD and UVDD mapped to $\overline{INT}$ pin 1 = Mask OVIN fault

BIT	BIT DESCRIPTION
VINM	0 = OVIN and UVIN mapped to $\overline{INT}$ pin 1 = Mask OVIN fault
OCM	0 = Overcurrent faults OC[4:1] mapped to $\overline{INT}$ pin 1 = Mask short-to-ground fault
OVM	0 = Overvoltage faults OV[4:1] mapped to $\overline{INT}$ pin 1 = Mask short-to-battery fault
UVM	0 = Undervoltage faults UV[4:1] mapped to $\overline{INT}$ pin 1 = Mask UV fault

Table 4. Configuration Register (CONFIG)

CONFIG								
BIT NO.	**BIT 7**	**BIT 6**	**BIT 5**	**BIT 4**	**BIT 3**	**BIT 2**	**BIT 1**	**BIT 0**
NAME	MUX1	MUX0	ENC	CLR	EN4	EN3	EN2	EN1
POR	0	0	0	1	1	1	1	1

BIT	BIT DESCRIPTION
MUX[1:0]	**ADC Mux Select:** 00 = ADC1–ADC4 registers contain current reading of each output **MAX20087/MAX20089 Only:** 01 = ADC1–ADC4 registers contain the output-voltage readings of each output 10 = ADC1–ADC3 registers contain V_{IN}, V_{DD}, and V_{ISET} 11 = Reserved
ENC	**Enable Continuous ADC Reading:** 0 = ADC conversion cycle started by reading ADC1 register; ADC1–ADC4 registers updated sequentially 1 = ADC continuously updates ADC1–ADC4 registers. First conversion is started when EN pin toggles high. A new conversion is started after ADC1 is read.
CLR	**Clear Faults on Read:** 0 = Status registers latch faults until read through I^2C 1 = Status registers show real-time fault information; $\overline{INT}$ pin reflects the real-time status
EN[4:1]	**Individual Enable Control:** Both the EN pin and EN_ bit must be high to enable a channel. 0 = Disabled 1 = Enabled when EN pin is high

Table 5. ID Register 1 (ID)

ID								
BIT NO.	**BIT 7**	**BIT 6**	**BIT 5**	**BIT 4**	**BIT 3**	**BIT 2**	**BIT 1**	**BIT 0**
NAME	—	—	ID[5:4]		R[3:0]			
POR	0	0	See description below		0	0	0	0

BIT	BIT DESCRIPTION
ID[5:4]	**Part ID Information:** 00 = MAX20089 01 = MAX20088 10 = MAX20087 11 = MAX20086
R[3:0]	**Revision Information:** Silicon revision of device indicated by these 4 bits; revision sequential with 0x0 indicating pass 1 silicon

Table 6. Status Register 1 (STAT1)

STAT1								
BIT NO.	**BIT 7**	**BIT 6**	**BIT 5**	**BIT 4**	**BIT 3**	**BIT 2**	**BIT 1**	**BIT 0**

Table 6. Status Register 1 (STAT1) (continued)

STAT1								
NAME	—	—	ISET	ACC	OVIN	UVIN	OVDD	UVDD
POR	0	0	0	0	0	0	0	0

BIT	BIT DESCRIPTION
ISET	**ISET Diagnostics Status:** Use ADC reading to diagnose resistance value. 0 = ISET within operating range 1 = ISET pin open or shorted
ACC	**ADC Conversion Complete:** 0 = Bit is reset reading ADC1; the latest completed ADC readings are always available at ADC1–ADC4 registers 1 = ADC conversions are completed
OVIN	0 = V_{IN} < OVIN threshold 1 = V_{IN} > OVIN threshold
UVIN	**Input Undervoltage Lockout:** If IN voltage is below the UVLO level, this bit is set to indicate device is unable to turn on the output switches. 0 = V_{IN} > UVLO 1 = V_{IN} ≤ UVLO (switches are turned off)
OVDD	**V_{DD} Overvoltage Lockout:** 0 = V_{DD} < OVDD threshold 1 = V_{DD} > OVDD threshold
UVDD	**V_{DD} Undervoltage Lockout:** If V_{DD} voltage is below the UVLO level, this bit is set to indicate device is unable to turn on the output switches. 0 = V_{DD} > UVLO 1 = V_{DD} ≤ UVLO (switches are turned off)

Table 7. ID Status Register 2 (STAT2)

STAT2 (UPPER BYTE)								
BIT NO.	**BIT 7**	**BIT 6**	**BIT 5**	**BIT 4**	**BIT 3**	**BIT 2**	**BIT 1**	**BIT 0**
NAME	TS4	OC4	OV4	UV4	TS3	OC3	OV3	UV3
POR	0	0	0	0	0	0	0	0

STAT2 (LOWER BYTE)								
BIT NO.	**BIT 7**	**BIT 6**	**BIT 5**	**BIT 4**	**BIT 3**	**BIT 2**	**BIT 1**	**BIT 0**
NAME	TS2	OC2	OV2	UV2	TS1	OC1	OV1	UV1
POR	0	0	0	0	0	0	0	0

BIT	BIT DESCRIPTION
TS[4:1]	**Thermal Shutdown on OUT1–OUT4:** Each channel has its own thermal sensor. 0 = No fault 1 = Thermal shutdown occurred on OUT1–OUT4
OC[4:1]	**Overcurrent on OUT1–OUT4:** The OC bit is set when an undervoltage event persists for longer than the shorted output-detection time, If fault latching is not set, the OC bit still remains set for the duration of the 250ms hiccup cycle, and is cleared on restart after hiccup. 0 = No overcurrent present 1 = Overcurrent present
OV[4:1]	**Overvoltage on OUT1–OUT4:** 0 = Output voltage < OV threshold 1 = Output voltage > OV threshold
UV[4:1]	**Undervoltage on OUT1–OUT4:** 0 = Output voltage > UV threshold 1 = Output voltage < UV threshold

Table 8. ADC Reading Registers 1–4 (ADC1–ADC4)

ADC1–ADC4								
BIT NO.	**BIT 7**	**BIT 6**	**BIT 5**	**BIT 4**	**BIT 3**	**BIT 2**	**BIT 1**	**BIT 0**
NAME	D7	D6	D5	D4	D3	D2	D1	D0
POR	0	0	0	0	0	0	0	0

BIT	BIT DESCRIPTION
D[7:0]	**ADC Readings Registers:** 00 = ADC1–ADC4 contain current readings of each output **MAX20087/MAX20089 Only:** 01 = ADC1–ADC4 contain output-voltage readings of each output 10 = ADC1–ADC3 contain V_{IN}, V_{DD}, V_{ISET}

Soft-Start/Soft-Shutdown

The ICs include a fixed 0.5ms soft-start. Soft-start time limits startup inrush current by ramping the output current from 0A to I_{LIM} set by the ISET pin. The ICs also include a soft-shutdown to minimize inductive ringing on the output channels. When disabled or faulted, the current ramps down from I_{LIM} to 0A in 0.25ms.

ADC Operation

The 8-bit ADC can be used for diagnostics of the system. There are three different mux settings that allow switch current, switch voltage, and other system voltages to be read through the on-board ADC. See Table 9 for ADC mux settings and Figure 5 for an ADC flow diagram.

Table 9. ADC Mux Settings

MUX SETTING	DESCRIPTION
00	ADC1–ADC4 readings contain the output current through OUT1–OUT4, respectively. The current can be calculated as: I_{OUT1}–I_{OUT4} = ADC1–ADC4 x 3mA
01*	ADC1–ADC4 readings contain the voltage at the output of the switches of OUT1–OUT4, respectively. The output voltage can be calculated as: V_{OUT1}–V_{OUT4} = ADC1–ADC4 x 70mV
10*	ADC1–ADC4 contain the following voltage readings: ADC1 = V_{IN} (70mV/count) ADC2 = V_{DD} (25mV/count) ADC3 = V_{ISET} (5mV/count) ADC4 = Unused

**Available on the ASIL-compliant versions only.*

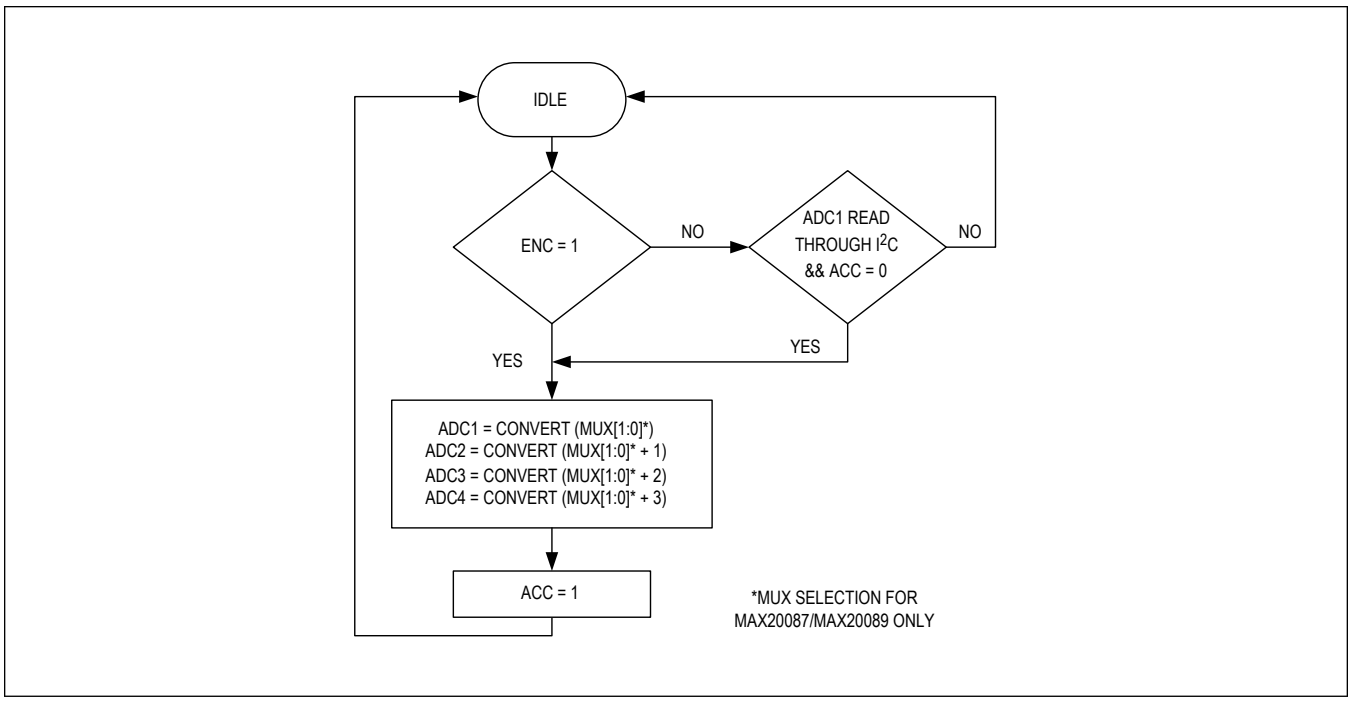


Figure 5. ADC Flow Diagram

Setting the Current Limit

Several factors determine the minimum current-limit setting for proper operation. Each output acts as a current source during the power-up phase. This means that each switch is in current limit, which is a high-power dissipation state. To protect the FETs, they can only be in current limit for a specific amount of time. It is important that the output capacitance is fully charged before this time expires. See Table 10.

The current limit per channel can be set based on the formula in Equation 1.

Equation 1:

$$I_{LIM} = 600mA \times \frac{R_{ISET}}{100k\Omega}$$

(valid between 100mA and 600mA)

Two or more channels can be connected in parallel to supply higher current (two, three, or four times I_{LIM} per channel). When paralleling channels, about 10% margin should be provided for mismatch between individual channel current limits.

Current-Limit/Short-Circuit Protection

The ICs feature current limit that protects the device and remote camera module against short-circuit and overload conditions at the outputs. In the event of a short-circuit or overload condition, the current is limited to the current set by R_{ISET}. When a channel has been in current limit for 20ms (10ms when the output voltage is < 2V), the channel turns off to prevent excessive power dissipation. The channel is reenabled after 250ms, entering soft-start. The actual STAT2.OC[4:1] bits are latched until read by the MCU when CONFIG.CLR = '0'.

Short-to-Battery Protection

The ICs feature a differential overvoltage comparator to detect a short-to-battery condition and prevent back feeding to the input supply. The input voltage is also monitored to provide a redundant path for detection.

If a short-to-battery event occurs before an output is enabled, the output does not turn on, regardless of the enable status. A short-to-battery condition is detected by the differential OV comparator if the part is enabled.

If the short-to-battery event occurs after an output has been enabled, the reverse-blocking FET is forced off, regardless of the enable state. The other FET remains enabled; if the short is temporary, the output remains operational, without having to go through soft-start. After the 100µs (typ) timeout, if the OV fault is not present, the reverse-blocking FET is reenabled.

In short-to-battery condition, the reverse current is limited below 1mA.

Overtemperature Protection

Thermal-overload protection limits the total power dissipation in the device. When the junction temperature exceeds +165°C (typ) at a specific output switch, the output switch is turned off, allowing the IC to cool. All other output channels remain enabled. The thermal sensor allows the output channel to turn on again after the junction temperature cools by 15°C.

OV Comparator Diagnostics

The input and output overvoltage comparators can be tested by using the following procedure:

1. Set EN pin = Low
2. Set CONFIG.EN[4:1] = ‘0’
3. Set EN pin = High
4. IN voltage > IN UV threshold
5. Set MASK.OVTST = ‘1’
6. Read STAT1 and STAT2 registers and verify that the STAT1.OVIN, STAT1.OVDD, and STAT2.OV[4:1] bits are set to ‘1’ (the STAT2.UV[4:1] bits are also set, due to disabling the outputs per step 1.)
7. Set MASK.OVTST = ‘0’

Note: Overvoltage and undervoltage conditions on OUT_, IN, and V_{DD} cannot be detected while the OV comparator diagnostic is enabled.

Fault Detection

The status registers contain information on the device’s status. Table 10 details the different faults and information bits within the status registers.

Table 10. Status Registers (Faults and Information Bits)

STATUS BIT	DIAGNOSTIC COVERAGE
ISET	When ‘1’ indicates the ISET pin does not have the expected resistance range connected to it. This can be a short-to-ground, open, or incorrect resistance value.
UVIN	When ‘1’ indicates that voltage connected to the IN pin is below 2.7V. The outputs are forced off in this condition.
OVIN	When ‘1’ indicates that voltage connected to the IN pin is above 16.5V. The outputs are forced off in this condition.
UVDD	When ‘1’ indicates that voltage connected to the V_{DD} pin is below 2.7V. The outputs are forced off in this condition.
OVDD	When ‘1’ indicates that voltage connected to the V_{DD} pin is above 5.7V. The outputs are forced off in this condition.
TS[4:1]	When any of these are ‘1’, the associated channel(s) are in thermal shutdown. The channel remains off until the temperature drops below the thermal-shutdown hysteresis temperature.
OC[4:1]	When any of these are ‘1’, the associated channel(s) have been in current limit and a shorted output has been detected. The channel(s) open immediately; the real-time status changes back to ‘0’ during the hiccup phase. While the short is present, the associated OC[4:1] bit(s) toggle, but the associated UV[4:1] bit(s) remain ‘1’, indicating the output is not in regulation.
UV[4:1]	When any of these are ‘1’, the associated channel(s) output are in undervoltage. This can occur if the switch is open, either due to the EN[4:1] control bits or to a fault condition such as shorted output or thermal shutdown. The UV[4:1] bits are also ‘1’ during the soft-start phase when the output capacitance is charging; this should not be considered a fault condition.

Table 10. Status Registers (Faults and Information Bits) (continued)

STATUS BIT	DIAGNOSTIC COVERAGE
OV[4:1]	When any of these are '1', the associated channel(s) output is higher than the input voltage. This can occur if there is a short-to-battery condition, or a transient condition due to abrupt input voltage or output current changes. This fault information should be debounced in software to prevent a false fault detection. In a real fault condition, these bit(s) are '1' for the entire time the fault is present.

Fault Coverage

The MAX20087/MAX20089 ICs are ASIL B compliant at the hardware level. This means ASIL B compliance is achieved without any additional external circuits or software processing. For ASIL D compliance for safety-critical applications, the MCU may need to use the ADC readings to increase fault coverage and verify that the MAX20087/MAX20089 ICs and connected camera sensors are operating within their specifications. See Table 11 for a list of faults and the associated diagnostic coverage.

Table 11. Faults and Diagnostic Coverage

FAULT	DIAGNOSTIC COVERAGE
Short-to-Battery on OUT1–OUT4 Pins	There are individual OV comparators on each output that can detect a shorted output to battery and turn off or prevent turning on a shorted output. In the event of a possible failure to the OV comparator, or soft-short conditions that could back feed current to the input supply, there is also an OV comparator on the input that will shut down the device to prevent system damage.
Short-to-Ground or Overcurrent on OUT1–OUT4 Pins	This can be detected by the UV comparator, overcurrent condition, and the ADC reading of the current.
Open on OUT1–OUT4 Pins	This is detected by the ADC current readings.
Open on IN	There are multiple pins on the input supply, so a single-point failure does not cause a failure; therefore, no diagnostic is needed. The ADC reading of the IN voltage can also detect if the IN pin is open.
Incorrect Input Voltage on IN Pin	This is detected by the ADC reading of the input voltage.
Open V_{DD} Pin	This is detected by loss of I^2C communications.
Open/Shorted ISET Pin	This is detected by the ADC reading of the ISET pin.
Open/Shorted $\overline{INT}$ Pin	This fault does not cause a system malfunction, but can delay the detection of faults by the MCU. This fault can be detected by the MCU by monitoring the $\overline{INT}$ pin. The $\overline{INT}$ pin is high when the EN pin is low, and then goes low as soon as EN goes high. If there are no faults, $\overline{INT}$ goes high after all four outputs are up and running.
Open PGND or GND Pin	There are multiple pins, each to eliminate a single-point failure.
Open SDA/SCL Pins	This is detected by loss of I^2C communications.
Open ADDR Pin	Internal pulldown puts it into a known state. Loss of I^2C for device with ADDR high is detectable through loss of communications.
Open EN Pin	All channels are forced off. Detectable through ADC readings of voltage drop and current.

Applications Information

Power-Over-Coaxial Cable

One of the key applications these parts are intended for is protecting power lines that supply remote cameras/radars over coaxial cable with concurrent data transmission. As such, there are several key factors to be considered.

Combining power and communications requires filter inductors in series with the power supply to prevent them from interfering with the data communications, and coupling capacitors at the transmitter/receiver to prevent the data communications from interfering with the power supply. The inductors must have minimal impedance at DC and low frequencies to properly provide power, but much higher impedance at the frequency bands where communication is taking place. Inversely, capacitors for the communication transmitter/receiver block DC and low-frequency signals to avoid disturbing the DC power level supplied by the converter, while passing AC data signals through across the cable. Simulation and bench testing can help determine the proper filter setup to allow for both power and data to be effectively transmitted over a coaxial cable. See Figure 6 for a system architecture diagram example.

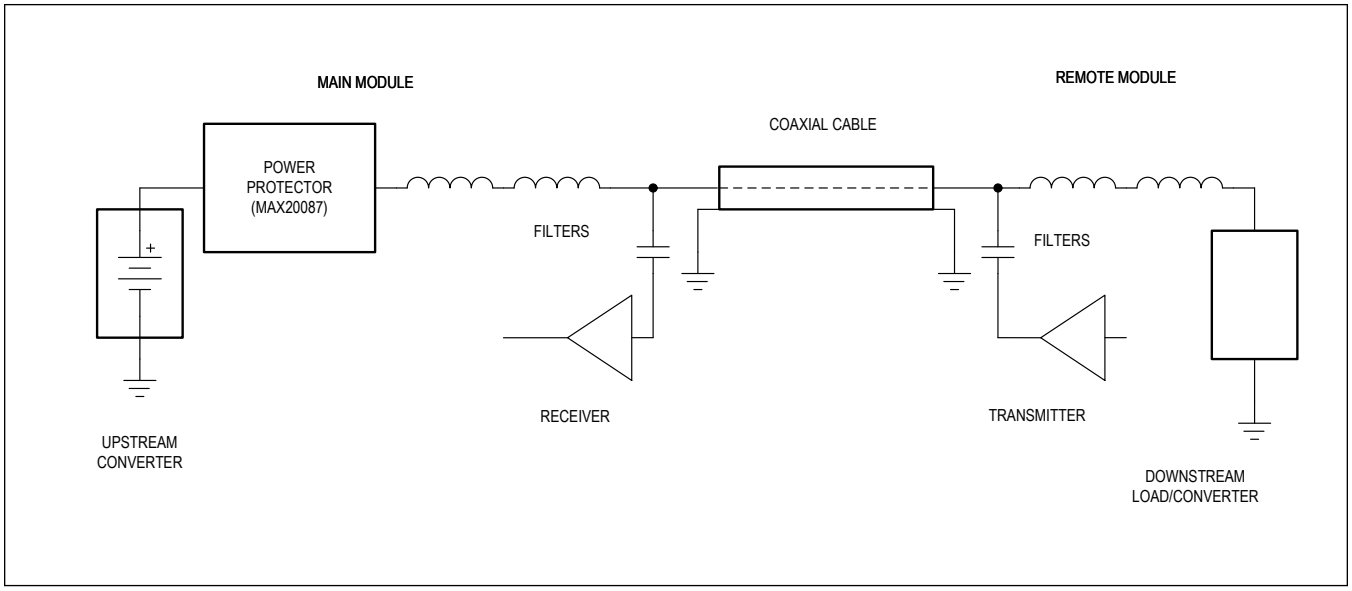
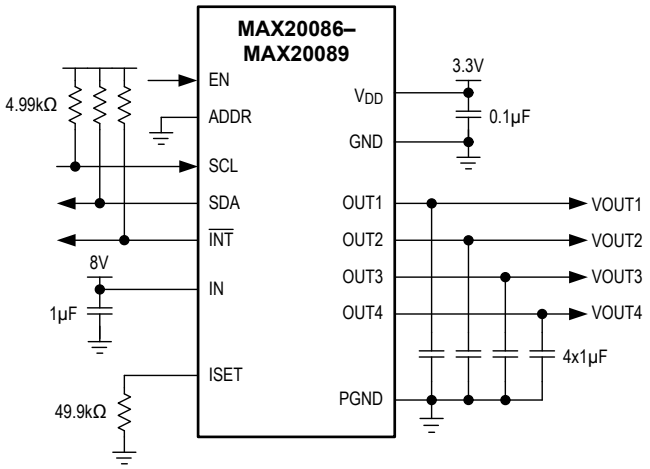


Figure 6. Example of System Architecture Diagram

Typical Application Circuit



Ordering Information

PART	TEMP RANGE	PIN-PACKAGE	OUTPUTS	OPTIONS	I²C (ADDR = 0)
MAX20086ATPA/VY+	-40°C to +125°C	20 SWTQFN-EP	4	—	0 x 28
MAX20086BATPA/VY+*	-40°C to +125°C	20 WETQFN-EP	4	—	0 x 28
MAX20087ATPA/VY+	-40°C to +125°C	20 SWTQFN-EP	4	ASIL	0 x 28
MAX20087ATPB/VY+	-40°C to +125°C	20 SWTQFN-EP	4	ASIL	0 x 2A
MAX20087ATPC/VY+	-40°C to +125°C	20 SWTQFN-EP	4	ASIL	0 x 2C
MAX20087BATPA/VY+	-40°C to +125°C	20 WETQFN-EP	4	ASIL	0 x 28
MAX20088ATPA/VY+	-40°C to +125°C	20 SWTQFN-EP	2	—	0 x 28
MAX20088ATPB/VY+	-40°C to +125°C	20 SWTQFN-EP	2	—	0 x 2C
MAX20089ATPA/VY+	-40°C to +125°C	20 SWTQFN-EP	2	ASIL	0 x 28
MAX20089ATPB/VY+	-40°C to +125°C	20 SWTQFN-EP	2	ASIL	0 x 2A

Note: *For variants with different options, contact factory.*

/V Denotes an automotive-qualified part.

Y Denotes a side-wettable part.

+ Denotes a lead(Pb)-free/RoHS-compliant package.

SW = Side-wettable TQFN package.

WE = Step-cut, side-wettable TQFN package.

EP = Exposed pad.

** Future product—contact factory for availability.*

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	9/17	Initial release	—
1	9/17	Added missing TOCs in *Typical Operating Characteristics* section	6
2	1/18	Removed future product status from MAX20086ATPA/VY, MAX20087ATPB/VY, MAX20087ATPC/VY+, MAX20088ATPA/VY+, MAX20089ATPA/VY+, and MAX20089ATPB/VY+ in *Ordering Information*	21
2.1		Added future product status back to MAX20087ATPC/VY+, MAX20089ATPA/VY+, and MAX20089ATPB/VY+ in *Ordering Information*	21
3	3/18	Removed future product status from MAX20087ATPC/VY+, MAX20089ATPA/VY+, and MAX20089ATPB/VY+ in *Ordering Information*	21
4	11/20	Added bullet on paralleling channel in *Benefits and Features*; clarified overvoltage threshold and undervoltage threshold conditions in *Electrical Characteristics*; corrected typos in "Current Limit/Short-Circuit Protection" section, added reverse current information in "Short-to-Battery Protection" section in *Detailed Description*.	1, 3, 16
5	9/21	Updated the *Pin Description* and *Ordering Information* tables	7, 20
6	6/22	Updated *Benefits and Features*, *Package Information*, *Electrical Characteristics*; added new package and pinout information; updated *Detailed Description* (Table 3) and *Ordering Information*	1–3, 7, 8, 13, 18, 21
7	7/23	Updated I2C Write Data Format (Figure 4), Enable Control Input (EN), Register Map (Table 2, Table 3, Table 4), Soft-Start/Soft-Shutdown, Setting the Current Limit, OV Comparator Diagnostics, Interrupt Output	13, 14, 15, 16, 18