nanoPower Supply Supervisors with Glitch-Free Power-Up

MAX16161/MAX16162

General Description

The MAX16161/MAX16162 are ultra-low current, single-channel supervisory ICs. The devices monitor the power supply voltage and assert a reset when the input voltage falls below the reset threshold. After the monitoring voltage rises above the factory-set threshold voltage (V_{TH}), the reset output remains asserted for the reset timeout period and then deasserts, allowing the target microcontroller or microprocessor to leave the reset state and begin operating.

Unlike conventional supervisors, which are unable to control the reset output state when V_{CC} is very low, the MAX16161/MAX16162 reset output is guaranteed to remain asserted until after a valid V_{CC} is achieved. This is especially important to avoid low-voltage cores leaving the reset state during power-up or power-down. This also improves performance when using the MAX16161/MAX16162 as simple power supply sequencers, because the devices do not cause a transient enable of a downstream power supply due to output glitches.

The MAX16161 features a manual reset (MR) input that asserts a reset when it receives an appropriate input signal, which can be either active-low or active-high, depending on the option. The MAX16162 has no MR input. Instead, it has separate V_{CC} and V_{IN} pins, allowing threshold voltages as low as 0.6V. The reset output is active-low open-drain, and the MAX16161/MAX16162 offer multiple available reset timeout period options.

The MAX16161/MAX16162 are specified over the -40°C to +125°C temperature range and are available in tiny, 1.06mm x 0.73mm, 4-bump WLP and 4-pin SOT23 packages. The MAX16162 is also available in a 5-pin SOT23 package.

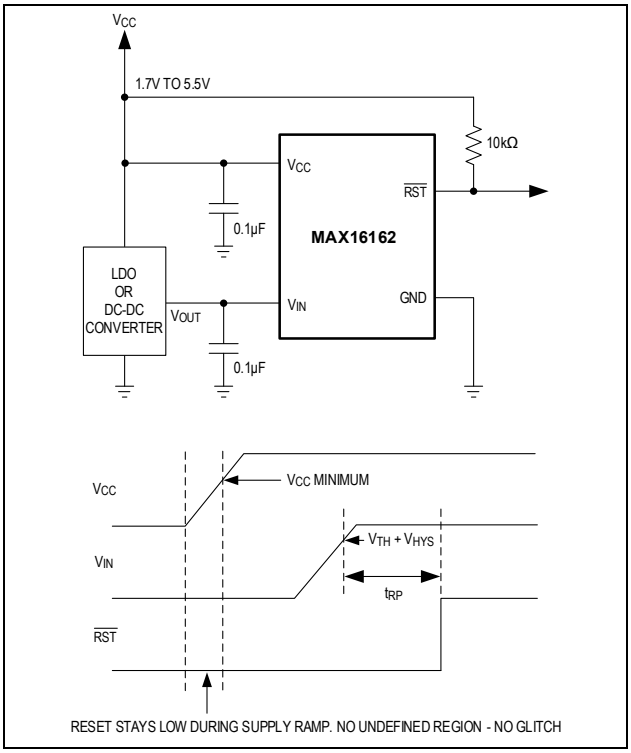
Applications

- Low-Voltage Microcontrollers and Microprocessors
- Portable/Battery-Powered Equipment
- e-Readers/Tablets
- Wearable/Portable Accessories
- Smart Phones

Benefits and Features

- No Powerup Glitch: (See *Reliable Supervisor for Low-Voltage Processor Cores*)
- 825nA (typ) Quiescent Current Extends Battery Life
- Positive and Negative Level-Triggered MR Input Options (MAX16161)
- MR Debounce Circuitry (MAX16161)
- Separate V_{CC} and V_{IN} Inputs (MAX16162)
- Multiple Available Reset Timeout Periods
- Threshold Voltage Options
  - 1.7V to 4.85V (MAX16161)
  - 0.6V to 4.85V (MAX16162)
- 4-Bump WLP, 4-Pin SOT23, and 5-Pin SOT23 Packages
- -40°C to +125°C Operating Temperature Range

Typical Application Circuit



***Ordering Information* appears at end of data sheet.**

19-101083; Rev 4; 3/24

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Absolute Maximum Ratings

V_{CC} to GND ..... -0.3V to +6V

MR, $\overline{RST}$ to GND ..... -0.3V to +6V

Continuous Sink/Source Current (All Pins) -20mA to +20mA

Continuous Power Dissipation (Multilayer Board) (T_A = +70°C, 4-Pump WLP (derate 9.58mW/°C above +70°C)) 766mW

Continuous Power Dissipation (Multilayer Board) (T_A = +70°C, 4-Pin SOT23 (derate 3.40mW/°C above +70°C)) 275.90mW

Continuous Power Dissipation (Multilayer Board) (T_A = +70°C, 5-Pin SOT23 (derate 3.90mW/°C above +70°C)) 312.60mW

Operating Temperature Range ..... -40°C to +125°C

Junction Temperature ..... +150°C

Soldering Temperature (reflow) ..... +300°C

Storage Temperature Range ..... -65°C to +150°C

Note 1: *Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7 using a four-layer board. For detailed information on package thermal considerations see https://www.analog.com/thermal-tutorial*

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Package Information

WLP

Package Code	N40C1+1
Outline Number	21-100478
Land Pattern Number	Refer to Application Note 1891
Thermal Resistance, Four-Layer Board:	
Junction-to-Ambient (θ_{JA})	104.41°C/W
Junction-to-Case Thermal Resistance (θ_{JC})	N/A

4-PIN SOT23

Package Code	U4+1C
Outline Number	21-0052
Land Pattern Number	90-0183
Thermal Resistance, Four-Layer Board:	
Junction-to-Ambient (θ_{JA})	290°C/W
Junction-to-Case Thermal Resistance (θ_{JC})	100°C/W

5-PIN SOT23

Package Code	U5+2
Outline Number	21-0052
Land Pattern Number	90-0174
Thermal Resistance, Four-Layer Board:	
Junction-to-Ambient (θ_{JA})	255.90°C/W
Junction-to-Case Thermal Resistance (θ_{JC})	81°C/W

For the latest package outline information and land patterns (footprints), go to www.analog.com/packages. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to https://www.analog.com/thermal-tutorial.

Electrical Characteristics

(V_{CC} = 1.7V to 5.5V, T_A = T_J = -40°C to +125°C, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
INPUT VOLTAGE						
Input Voltage Range	V_{CC}	Operating range	1.7		5.5	V
		Reset output is guaranteed to be in a known state (*Note 2*) (*Note 3*)	0		5.5	
Maximum Pullup Voltage	V_{PU_MAX}	V_{CC} ≤ 2V			1.8 x V_{CC}	V
		V_{CC} > 2V			3.6V	
Supply Current	I_{CC}	V_{CC} = 3.3V, T_A = -40°C to +85°C, reset not asserted (MAX16161)		920	1800	nA
		Over full supply range, T_A = -40°C to +125°C (MAX16161)			2400	
		V_{CC} = 3.3V, T_A = -40°C to +85°C, reset not asserted (MAX16162)		825	1550	
		Over full supply range, T_A = -40°C to +125°C (MAX16162)			2300	
		V_{CC} = 3.3V, reset asserted (MAX16162)		12		µA
Threshold Voltage Range	V_{TH}	MAX16161	1.7		4.85	V
		MAX16162	0.6		4.85	
Threshold Voltage Accuracy	V_{TH_ACC}	V_{CC} falling (MAX16161), V_{IN} falling (MAX16162)	-1.5		+1.5	$\%V_{TH}$
Threshold Voltage Resolution				50		mV
Threshold Voltage Hysteresis	V_{TH_HYS}	V_{CC} rising (MAX16161), V_{IN} rising (MAX16162)		1		$\%V_{TH}$
RESET OUTPUT						
Reset Output Delay	t_D	Measured with 2.5% threshold overdrive below V_{TH}		50		µs
Reset Timeout Period Accuracy	t_{RP_ACC}	Measured from the time when the monitoring voltage crosses above V_{TH} + V_{HYS} (*Note 4*)	-25		+25	%
Reset Output Voltage Low	V_{OL}	V_{PU} = 3.3V, R_{PU} = 10kΩ			0.4	V
Reset Output Leakage Current					1	µA
MANUAL RESET (MAX16161)						
MR Debounce Period	t_{DB}	Level-triggered MR input		20		ms
MR Input Voltage Low	V_{IL}				0.33 x V_{CC}	V
MR Input Voltage High	V_{IH}		0.69 x V_{CC}			V
MR Internal Pullup Resistor		Active-low MR input		50		kΩ
MR Internal Pulldown Resistor		Active-high MR input		50		kΩ

Note 2: V_{CC} slew rate must be greater than 0.004mV/µs for slower power cycles.

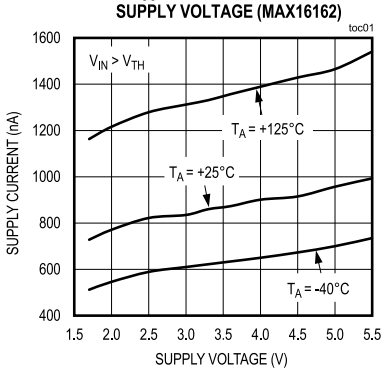
Note 3: For V_{CC} blackout conditions, slew rate should be less than 10mV/µs.

Note 4: The reset timeout period is affected by the V_{CC} rise time during power-up. For a V_{CC} rise time of 10µs or faster, the additional t_{RP} is about 2ms (typ).

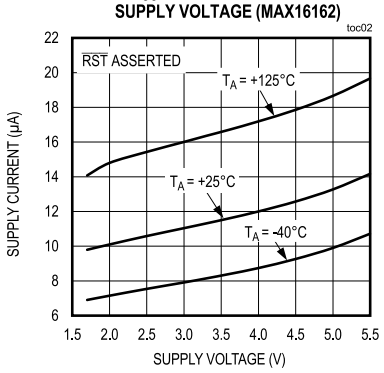
Typical Operating Characteristics

(V_{CC} = 3.3V, V_{IN} = 3.3V, V_{PU} = V_{CC}, T_A = -40°C to +125°C, R_{PU} = 10kΩ unless otherwise noted. Normalized values are with respect to +25°C.)

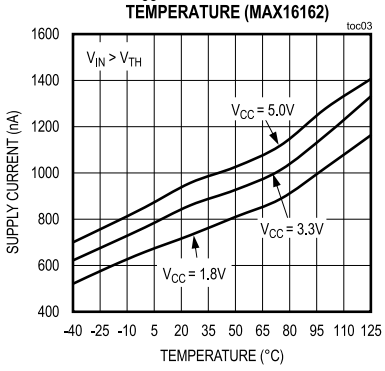
V_{CC} SUPPLY CURRENT vs. SUPPLY VOLTAGE (MAX16162)



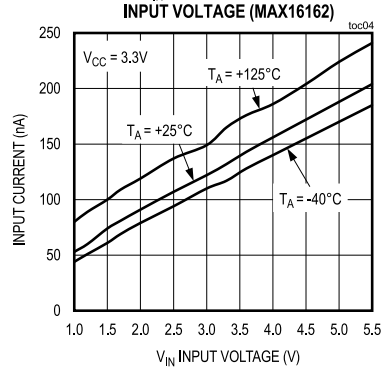
V_{CC} SUPPLY CURRENT vs. SUPPLY VOLTAGE (MAX16162)



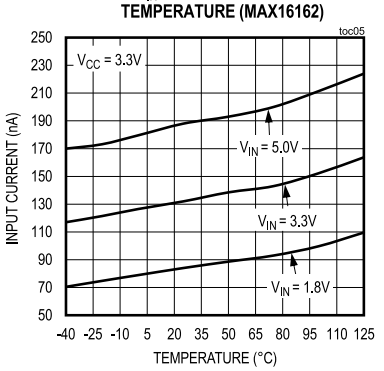
V_{CC} SUPPLY CURRENT vs. TEMPERATURE (MAX16162)



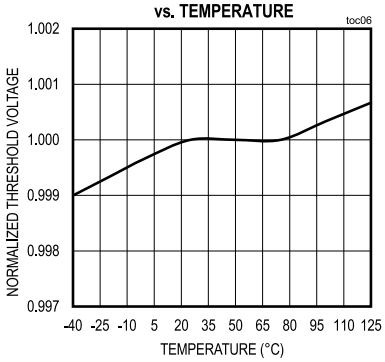
V_{IN} INPUT CURRENT vs. INPUT VOLTAGE (MAX16162)



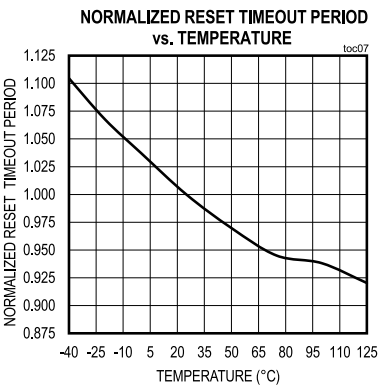
V_{IN} INPUT CURRENT vs. TEMPERATURE (MAX16162)



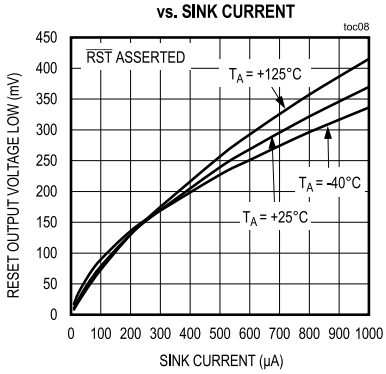
NORMALIZED THRESHOLD VOLTAGE vs. TEMPERATURE



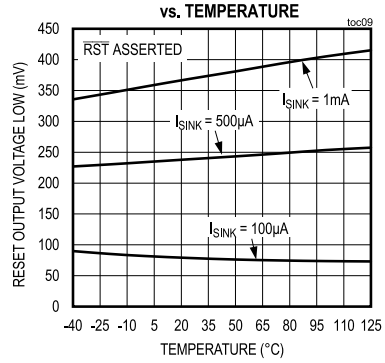
NORMALIZED RESET TIMEOUT PERIOD vs. TEMPERATURE



RESET OUTPUT VOLTAGE LOW vs. SINK CURRENT

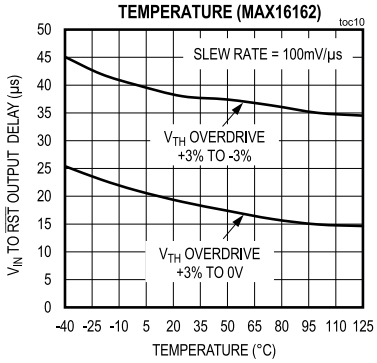


RESET OUTPUT VOLTAGE LOW vs. TEMPERATURE

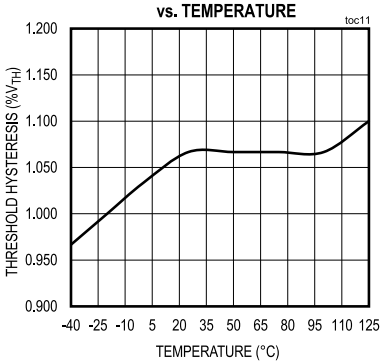


(V_{CC} = 3.3V, V_{IN} = 3.3V, V_{PU} = V_{CC}, T_A = -40°C to +125°C, R_{PU} = 10kΩ unless otherwise noted. Normalized values are with respect to +25°C.)

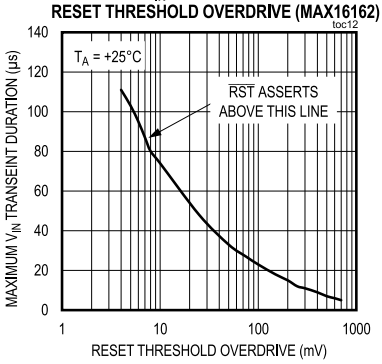
V_{IN} TO $\overline{RST}$ OUTPUT DELAY vs. TEMPERATURE (MAX16162)



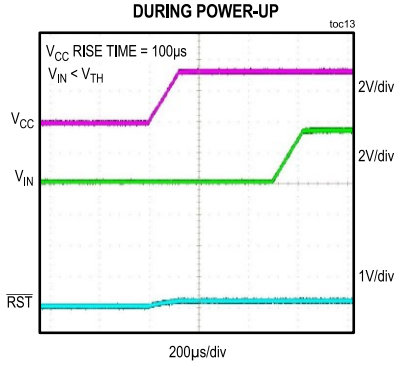
THRESHOLD VOLTAGE HYSTERESIS vs. TEMPERATURE



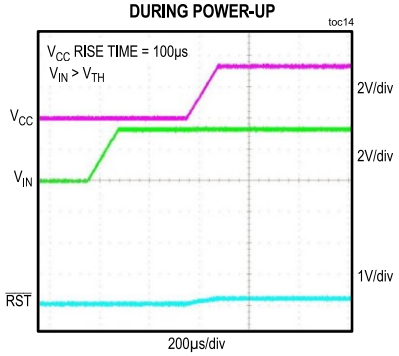
MAXIMUM V_{IN} TRANSIENT DURATION vs. RESET THRESHOLD OVERDRIVE (MAX16162)



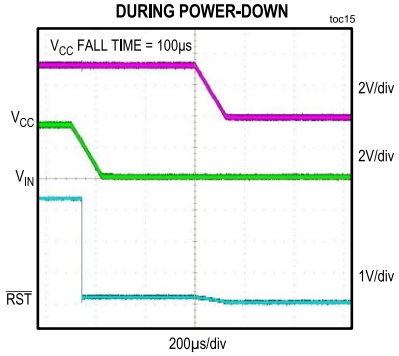
$\overline{RST}$ OUTPUT BEHAVIOR DURING POWER-UP



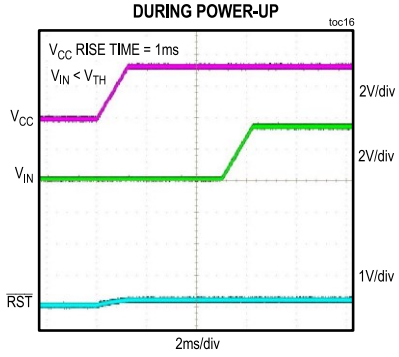
$\overline{RST}$ OUTPUT BEHAVIOR DURING POWER-UP



$\overline{RST}$ OUTPUT BEHAVIOR DURING POWER-DOWN



$\overline{RST}$ OUTPUT BEHAVIOR DURING POWER-UP



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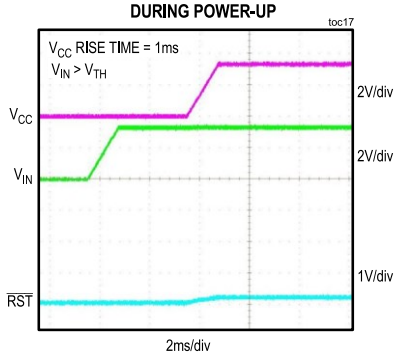

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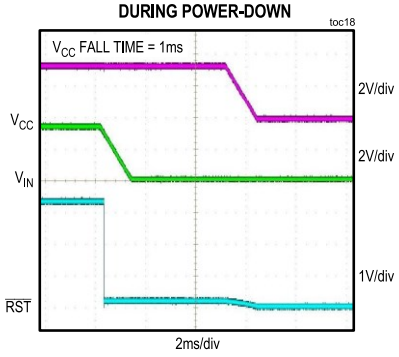

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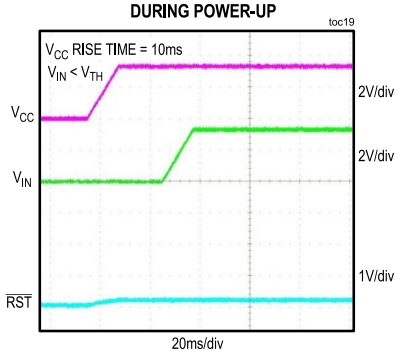
$\overline{RST}$ OUTPUT BEHAVIOR DURING POWER-UP



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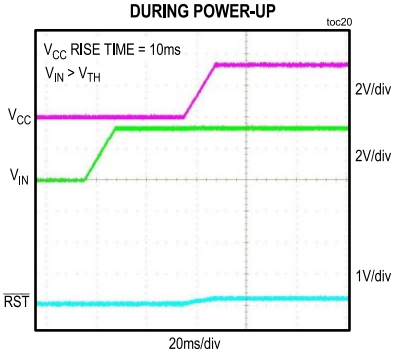

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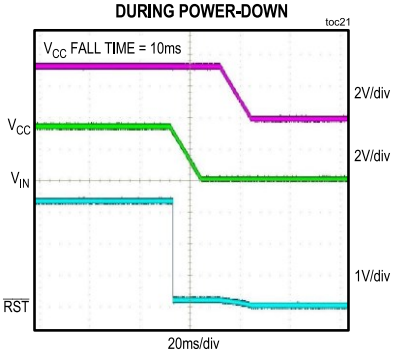

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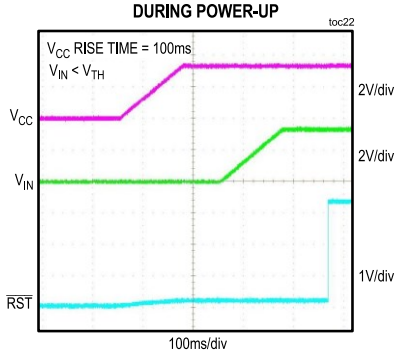

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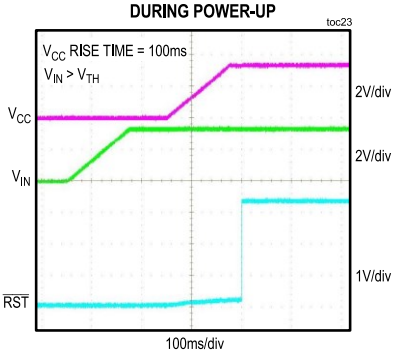

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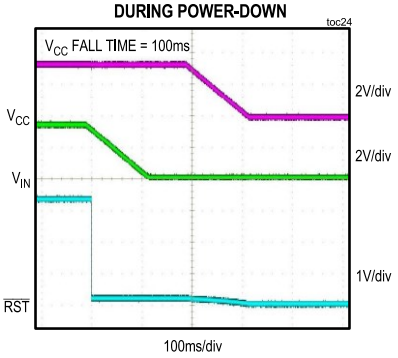
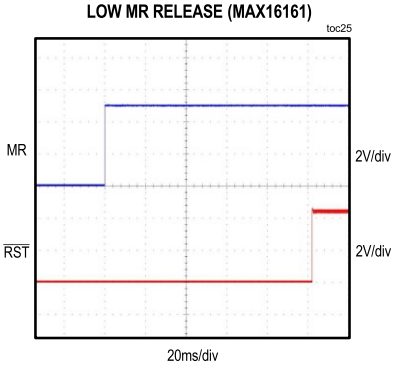
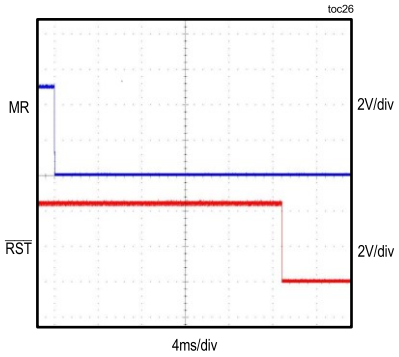


$\overline{RST}$ RESPONSE TO ACTIVE LOW MR RELEASE (MAX16161)

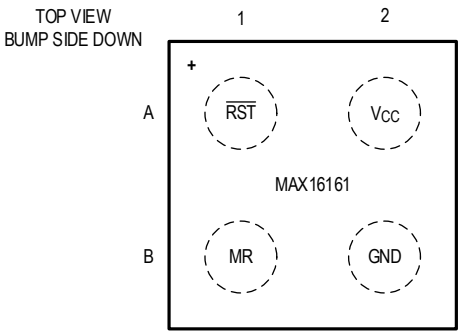


$\overline{RST}$ RESPONSE TO ACTIVE LOW MR ASSERTION (MAX16161)

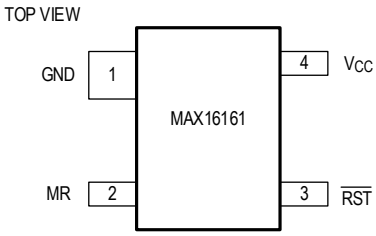


Pin Configurations

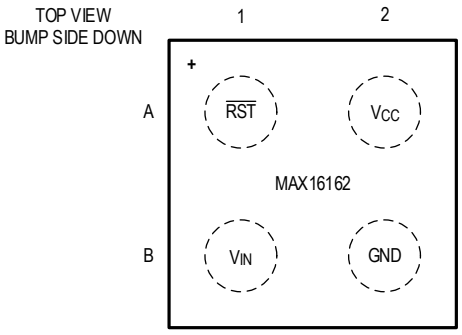
MAX16161 4-Bump WLP



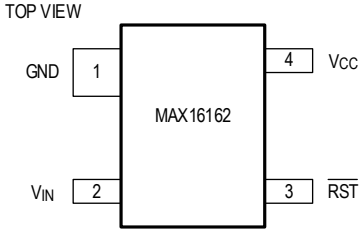
MAX16161 4-Pin SOT23



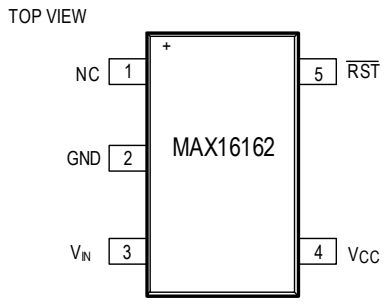
MAX16162 4-Bump WLP



MAX16162 4-Pin SOT23



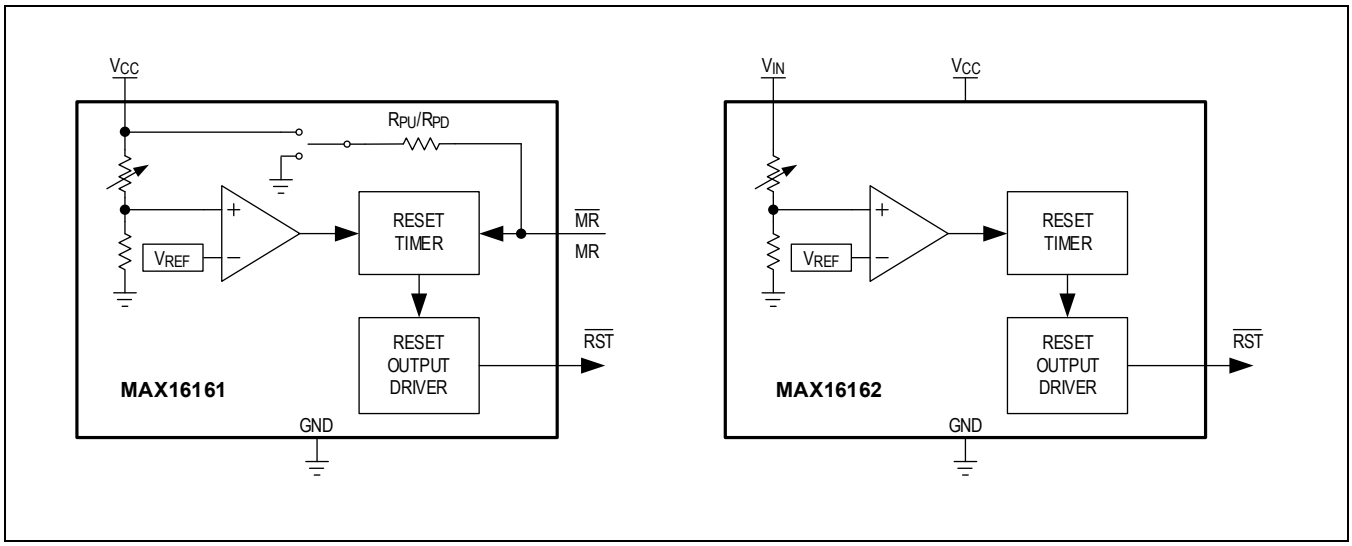
MAX16162 5-Pin SOT23



Pin Descriptions

PIN					NAME	FUNCTION
MAX16161 4-Bump WLP	MAX16161 4-Pin SOT23	MAX16162 4-Bump WLP	MAX16162 4-Pin SOT23	MAX16162 5-Pin SOT23		
A1	3	A1	3	5	$\overline{RST}$	Reset Output. $\overline{RST}$ asserts when V_{CC} /V_{IN} drops below the threshold voltage or when MR receives a valid input signal. $\overline{RST}$ is an active-low open-drain output and requires a pullup resistor.
A2	4	A2	4	4	V_{CC}	Supply Voltage. For the MAX16161, it is also the monitored voltage. Bypass V_{CC} with a 0.1µF ceramic capacitor to GND.
B1	2	-	-	-	MR	Manual Reset Input. See the *MAX16161 Manual Reset Input* section for further details.
-	-	B1	2	3	V_{IN}	Monitored Voltage Input. When V_{CC} is 1.7V or greater, the MAX16162 monitors the voltage at this pin to generate a reset output.
B2	1	B2	1	2	GND	Ground
-	-	-	-	1	NC	No Connection.

Functional Diagrams



Detailed Description

The MAX16161 is an ultra-low-current supervisor IC that monitors the V_{CC} voltage from 1.7V to 4.85V. It also features a manual reset input to assert the reset output using a low or high level-trigger input. The MAX16162 has separate V_{CC} and V_{IN} inputs, and it monitors the input voltage from 0.6V to 4.85V.

During normal operation when the monitored voltage falls below the factory-set threshold, the reset output asserts and remains asserted for the reset timeout period after the voltage rises above the threshold voltage.

MAX16161 V_{CC} Threshold

The MAX16161 monitors V_{CC} from 1.7V to 4.85V. The reset output asserts when V_{CC} falls below V_{TH}. Note that, unlike typical supervisors, the reset output never deasserts when the supply voltage is less than the minimum operating voltage. It always remains asserted until the correct supply voltage has been applied.

After V_{CC} rises above V_{TH} + V_{HYST}, the reset output remains asserted until the reset timeout period has elapsed, at which point the reset output deasserts. See the timing diagram in *Figure 1*, which shows the behavior of an active-low reset output. Note that there is no glitch or undetermined region when the supply voltage is low.

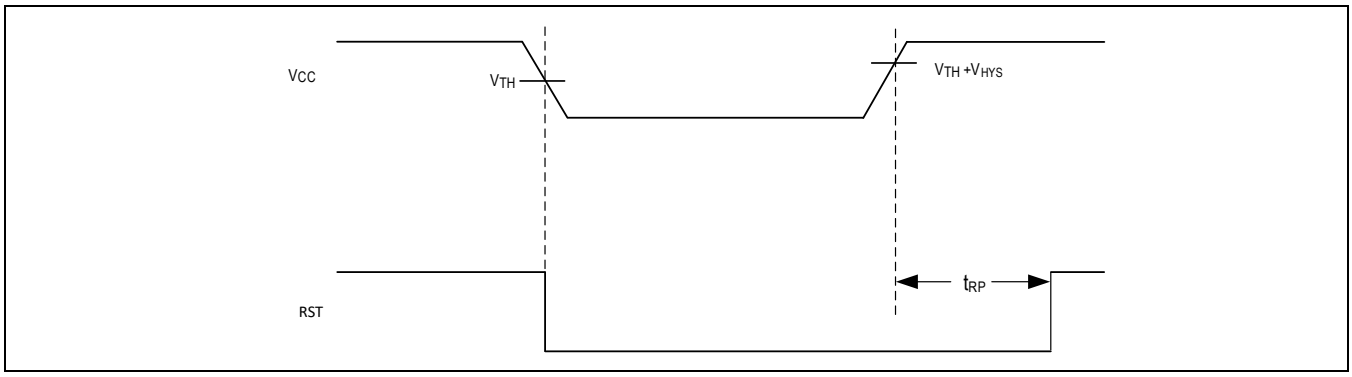


Figure 1. Active-Low Reset Response to V_{CC} Falling and Rising Edges

MAX16161 Manual Reset Input

Many systems require manual reset capability, which allows an operator, test technician, or logic signal to initiate a reset. Two manual reset input polarities are available, as shown in *Table 2*.

The MAX16161 asserts the reset output after MR stays in the active state longer than the debounce period (t_{DB}). Once MR becomes inactive, the reset output deasserts after the reset timeout period has elapsed. See *Figure 2* and *Figure 3* for more details.

Reset Input Configurations

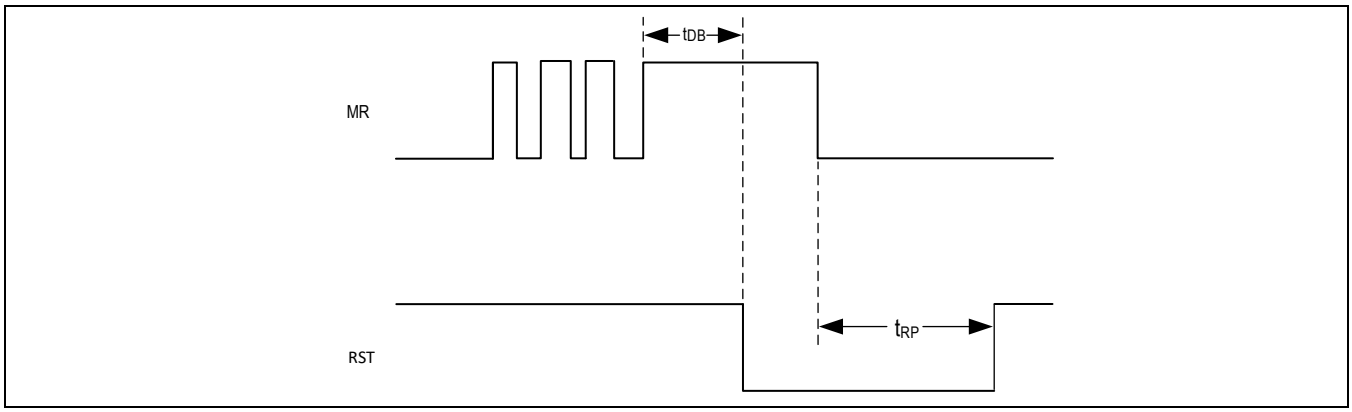


Figure 2. Active-High-Triggered Manual Reset Input Behavior

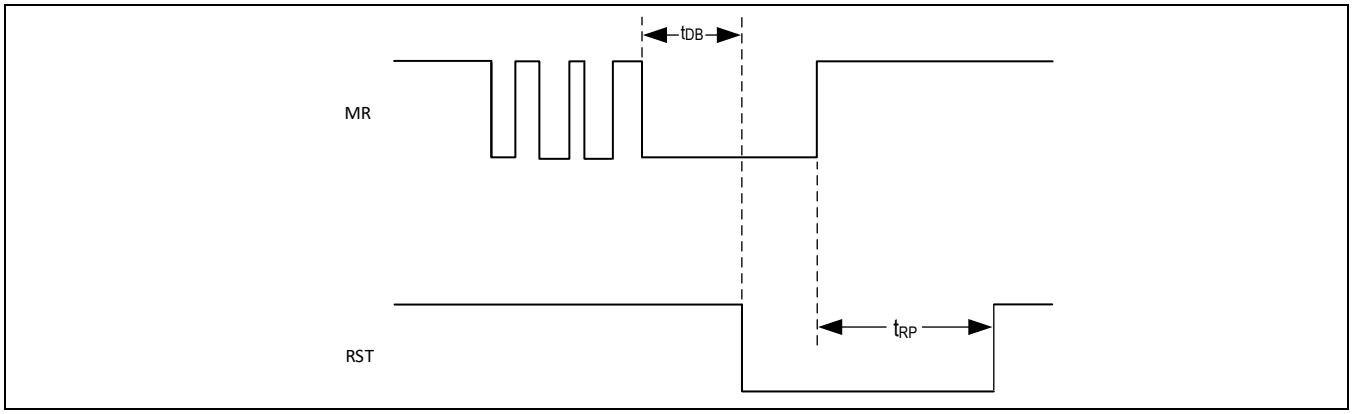


Figure 3. Active-Low-Triggered Manual Reset Input Behavior

MAX16162 V_{IN} Threshold

The MAX16162's operating supply voltage range is from 1.7V to 5.5V. V_{IN} can be connected to V_{CC} to monitor the MAX16162's supply voltage, or it can be connected to a separate supply voltage for monitoring. The threshold voltage (V_{TH}) range is from 0.6V to 4.85V. The reset output asserts when V_{IN} falls below V_{TH}. Note that, unlike typical supervisors, the reset output never deasserts to an invalid reset voltage level when the supply voltage is less than the minimum operating voltage. It always remains in a valid logic state until the correct supply voltage has been applied and the input voltage rises above the threshold.

After V_{IN} rises above V_{TH} + V_{HYST}, the reset output remains asserted until the reset timeout period has elapsed, at which point the reset output deasserts. See the timing diagram in the *Typical Application Circuit*, which shows the behavior of an active-low reset output. Note that there is no glitch or undetermined region when the supply voltage is low.

Reset Output

When the supply voltage is less than the internal threshold voltage, the MAX16161/MAX16162 supervisors assert the reset output ($\overline{RST}$) to prevent code execution errors during power-up, power-down, and brownout conditions. In contrast to conventional supervisors, which cannot guarantee the correct reset output state when the input voltage is low, the MAX16161/MAX16162 reset output state is correct for supply voltages as low as ground. Note that the reset output voltage depends on the sink current. When using a pullup resistor, ensure that its value is large enough that the reset

sink current is sufficiently low to maintain the reset output voltage (V_{OL}) below the threshold voltage of the following logic input. A 100kΩ pullup resistor limits the current sufficiently to keep the output low voltage below 400mV.

When V_{CC} is below 2.0V, the reset pullup voltage (V_{PU}) is limited to 1.8 x V_{CC}; when V_{CC} is above 2.0V, the reset pullup voltage (V_{PU}) is limited to 3.6V. Select a pullup supply properly to avoid high current flow through the pullup resistor.

Eight different reset timeout period options are available with nominal values ranging from from 310µs to 2s. See *Table 1* for available options. See the *Selector Guide* for more details.

Glitch-Free Power-Up/-Down

Conventional voltage supervisors require a minimum supply at V_{CC} to guarantee the correct state of RESET. Below the minimum supply, RESET voltage tracks V_{CC} voltage and causes a power-up glitch at RESET. The MAX16161/MAX16162 can sink the current through the RESET pin even if V_{CC} is 0V; this assures the valid state of RESET at a zero supply voltage and provides glitch-free power-up/-down operation.

Applications Information

Power Supply Bypassing and Grounding

Bypass V_{CC} to ground with a 0.1µF capacitor as close to the device as possible. The bypass capacitor improves transient immunity. For fast transients (>3mV/µs) with a large voltage excursion (>500mV), a filter resistor in series with the bypass capacitor is recommended for proper device operation. See *Figure 4* for more detail.

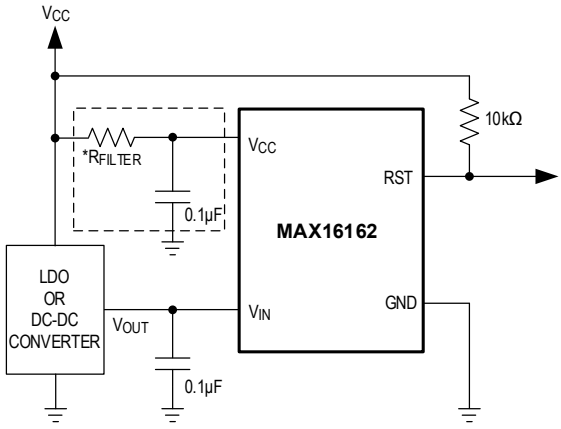


Figure 4. Power Supply Bypassing/Input Filter

Configuration Tables

Table 1. Reset Timeout Period Options

SUFFIX	RESET TIMEOUT PERIOD			UNITS
	T_A = +25°C	T_A = -40°C to +125°C		
	TYP	MIN	MAX	
A	0.31	0.24	0.39	ms
B	10	7.50	12.5	ms
C	50	38.5	62.5	ms
D	100	75.0	125	ms
E	250	187.5	312.5	ms
F	500	375	625	ms
G	1000	750	1250	ms
H	2000	1500	2500	ms

Table 2. Manual Reset Input Options

SUFFIX	MR TRIGGER INPUT
K	Active Low
L	Active High

Table 3. Threshold Voltage Options

SUFFIX	V_{TH} (V)	SUFFIX	V_{TH} (V)	SUFFIX	V_{TH} (V)
060	0.60	210	2.10	360	3.60
065	0.65	215	2.15	365	3.65
070	0.70	220	2.20	370	3.70
075	0.75	225	2.25	375	3.75
080	0.80	230	2.30	380	3.80
085	0.85	235	2.35	385	3.85
090	0.90	240	2.40	390	3.90
095	0.95	245	2.45	395	3.95
100	1.00	250	2.50	400	4.00
105	1.05	255	2.55	405	4.05
110	1.10	260	2.60	410	4.10
115	1.15	265	2.65	415	4.15
120	1.20	270	2.70	420	4.20
125	1.25	275	2.75	425	4.25
130	1.30	280	2.80	430	4.30
135	1.35	285	2.85	435	4.35
140	1.40	290	2.90	440	4.40
145	1.45	295	2.95	445	4.45
150	1.50	300	3.00	450	4.50
155	1.55	305	3.05	455	4.55
160	1.60	310	3.10	460	4.60
165	1.65	315	3.15	465	4.65
170	1.70	320	3.20	470	4.70
175	1.75	325	3.25	475	4.75
180	1.80	330	3.30	480	4.80
185	1.85	335	3.35	485	4.85
190	1.90	340	3.40	—	—
195	1.95	345	3.45	—	—
200	2.00	350	3.50	—	—
205	2.05	355	3.55	—	—

Selector Guide

MAX1616_ _ _ _ _ _ _ +T

SUF	MR Input	VIN Input
1	Yes	No
2	No	Yes

SUF	PACKAGE
N	4 WLP
U	4 SOT23
K	5 SOT23

SUF	RESET TIMEOUT (TYP)
A	0.31ms
B	10ms
C	50ms
D	100ms
E	250ms
F	500ms
G	1000ms
H	2000ms

SUF	MR INPUT
K	MAX16161 ACTIVE-LOW TRIGGER
	MAX16162 (NO MR)
L	MAX16161 ACTIVE-HIGH TRIGGER

SUF	V_{TH}(V)	SUF	V_{TH}(V)	SUF	V_{TH}(V)
060	0.60	205	2.05	350	3.50
065	0.65	210	2.10	355	3.55
070	0.70	215	2.15	360	3.60
075	0.75	220	2.20	365	3.65
080	0.80	225	2.25	370	3.70
085	0.85	230	2.30	375	3.75
090	0.90	235	2.35	380	3.80
095	0.95	240	2.40	385	3.85
100	1.00	245	2.45	390	3.90
105	1.05	250	2.50	395	3.95
110	1.10	255	2.55	400	4.00
115	1.15	260	2.60	405	4.05
120	1.20	265	2.65	410	4.10
125	1.25	270	2.70	415	4.15
130	1.30	275	2.75	420	4.20
135	1.35	280	2.80	425	4.25
140	1.40	285	2.85	430	4.30
145	1.45	290	2.90	435	4.35
150	1.50	295	2.95	440	4.40
155	1.55	300	3.00	445	4.45
160	1.60	305	3.05	450	4.50
165	1.65	310	3.10	455	4.55
170	1.70	315	3.15	460	4.60
175	1.75	320	3.20	465	4.65
180	1.80	325	3.25	470	4.70
185	1.85	330	3.30	475	4.75
190	1.90	335	3.35	480	4.80
195	1.95	340	3.40	485	4.85
200	2.00	345	3.45		

Typical Application Circuits

Typical Application Circuit

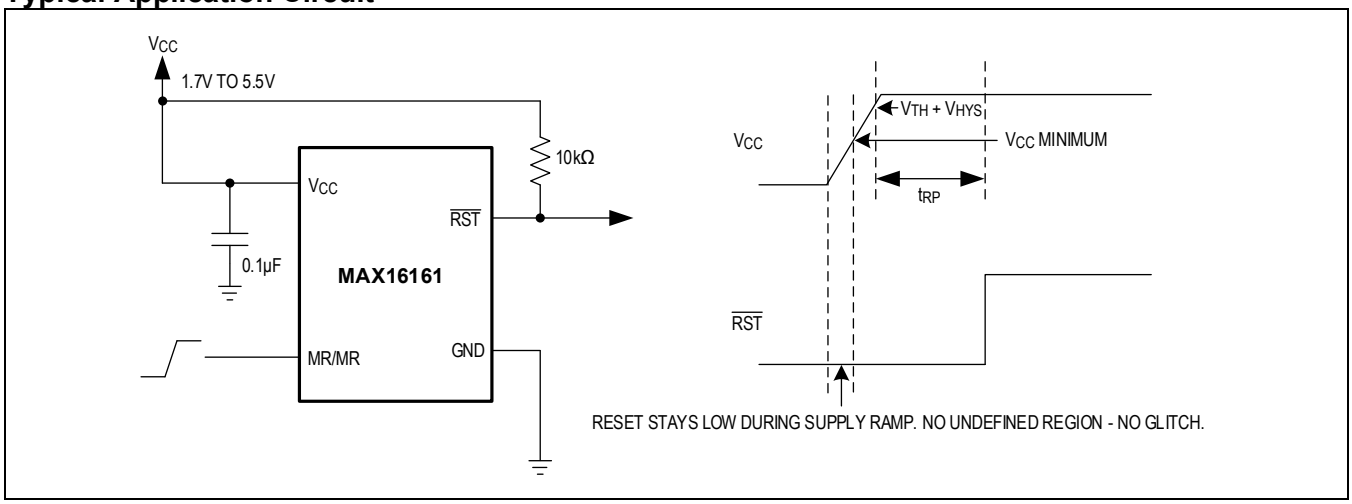


Figure 5. Typical Application Circuit (MAX16161)

Reliable Supervisor for Low-Voltage Processor Cores

The MAX16162 is capable of monitoring supply voltages from 0.6V to 4.85V. In the *Figure 6* typical application diagram, the MAX16162 is used to monitor the core voltage of low-power microcontrollers or FPGAs, where glitch-free power-up is necessary for reliable operation. Conventional supervisors cannot guarantee the correct reset output state when the supply voltage is low.

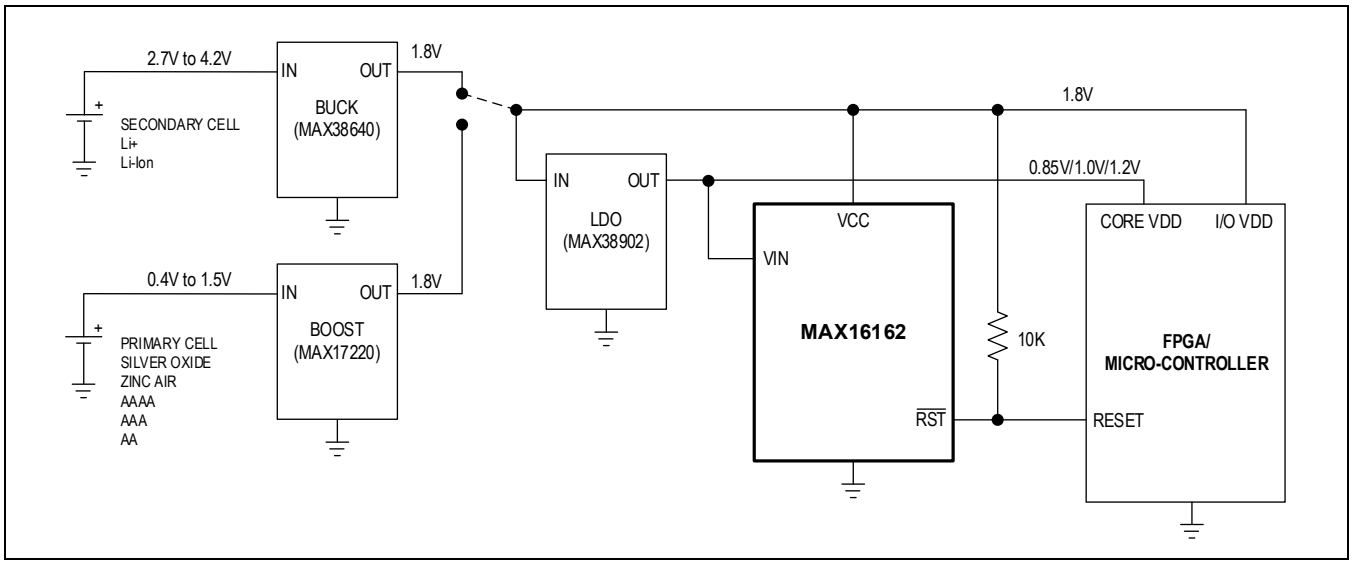


Figure 6. Low-Voltage Processor Core Application (MAX16162)

Simple Power Supply Sequencer

After the output voltage of the first regulator becomes valid, the MAX16161/MAX16162 insert a delay and generate the enable signal for the second regulator after the reset timeout period. Because the MAX16161/MAX16162 never deassert $\overline{RST}$ until the supply voltage is correct, the controlled supply is never incorrectly enabled. A typical application circuit is shown in *Figure 7*.

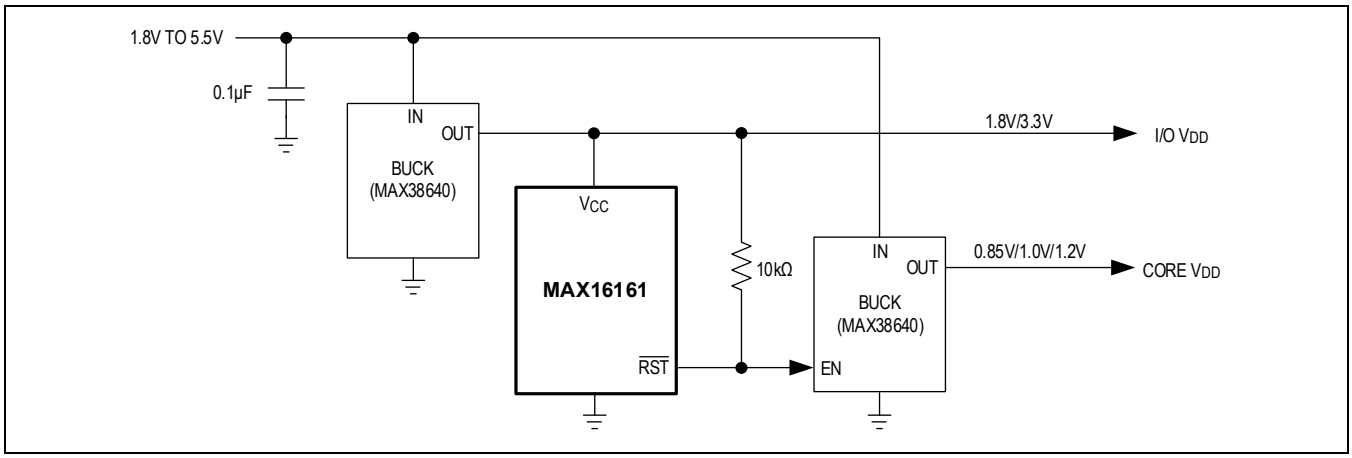


Figure 7. MAX16161 as a Simple Power Supply Sequencer

Ordering Information

PART NUMBER	TEMPERATURE RANGE	PIN-PACKAGE
MAX16162NDK300+T	-40°C to +125°C	4 WLP
MAX16162NGK190+T	-40°C to +125°C	4 WLP
MAX16162NGK175+T	-40°C to +125°C	4 WLP
MAX16162NBK280+T	-40°C to +125°C	4 WLP
MAX16162NDK290+T	-40°C to +125°C	4 WLP
MAX16162KEK310+T	-40°C to +125°C	5 SOT23
MAX16161NDK300+T	-40°C to +125°C	4 WLP
MAX16161NDK250+T	-40°C to +125°C	4 WLP

+Denotes a lead(Pb)-free/RoHS-compliant package.

T Denotes tape-and-reel.

Contact the factory for the availability of future variants in three package options.

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	04/21	Initial release	—
1	6/21	Updated Ordering Information table	19
2	12/21	Updated Ordering Information table and Typical Operating Characteristics	9, 18
3	4/22	Updated General Description, Benefits and Features, Absolute Maximum Ratings, Package Description, Pin Configuration, Pin Description, Selector Guide, and Ordering Information table	1, 5, 12, 18, 21
4	3/24	Updated Ordering Information table	22

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