

Half-Duplex RS-485 Transceivers in μ DFN

MAX13485E/MAX13486E

General Description

The MAX13485E/MAX13486E +5V, half-duplex, $\pm 15\text{kV}$ ESD-protected RS-485 transceivers feature one driver and one receiver. These devices include fail-safe circuitry, guaranteeing a logic-high receiver output when receiver inputs are open or shorted. The receiver outputs a logic-high if all transmitters on a terminated bus are disabled (high impedance). The MAX13485E/MAX13486E include a hot-swap capability to eliminate false transitions on the bus during power-up or live-insertion.

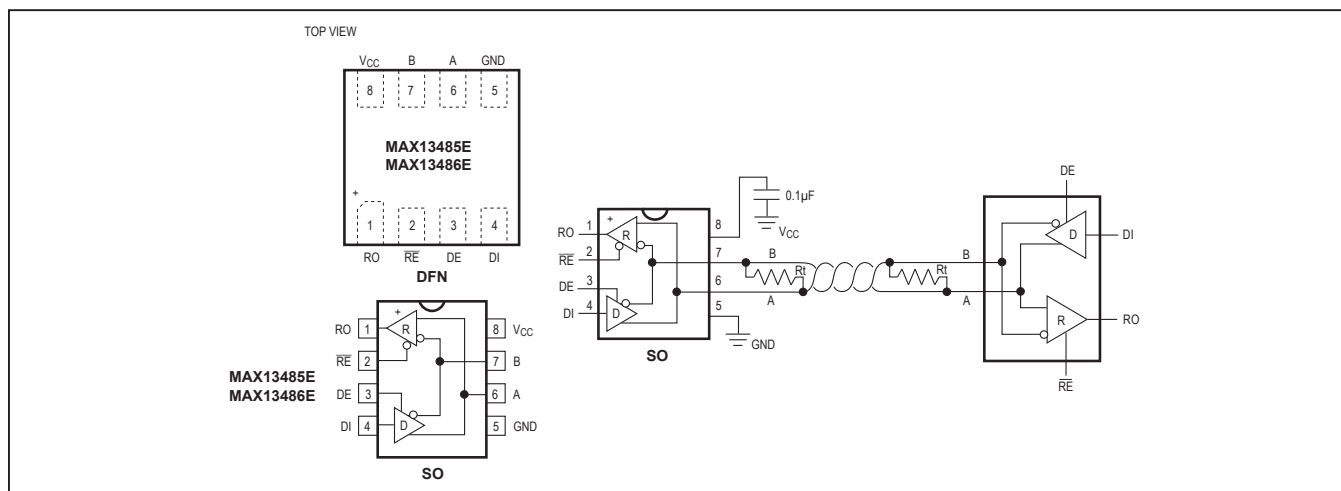
The MAX13485E features reduced slew-rate drivers that minimize EMI and reduce reflections caused by improperly terminated cables, allowing error-free transmission up to 500kbps. The MAX13486E driver slew rate is not limited, allowing transmit speeds up to 16Mbps.

The MAX13485E/MAX13486E feature a 1/4-unit load receiver input impedance, allowing up to 128 transceivers on the bus. These devices are intended for half-duplex communications. All driver outputs are protected to $\pm 15\text{kV}$ ESD using the Human Body Model. The MAX13485E/MAX13486E are available in 8-pin SO and space-saving 8-pin μ DFN packages. The devices operate over the extended -40°C to $+85^{\circ}\text{C}$ temperature range.

Applications

- Utility Meters
- Industrial Controls
- Industrial Motor Drives
- Automated HVAC Systems

Pin Configurations



19-0742; Rev 1; 8/24

Features

- +5V Operation
- True Fail-Safe Receiver While Maintaining EIA/TIA-485 Compatibility
- Hot-Swappable for Telecom Applications
- Enhanced Slew-Rate Limiting Facilitates Error-Free Data Transmission (MAX13485E)
- High-Speed Version (MAX13486E) Allows for Transmission Speeds Up to 16Mbps
- Extended ESD Protection for RS-485 I/O Pins $\pm 15\text{kV}$ Using Human Body Model
- 1/4 Unit Load, Allowing Up to 128 Transceivers on the Bus
- Available in Space-Saving 8-Pin μ DFN or Industry Standard 8-Pin SO Packages

Ordering Information

PART	PIN-PACKAGE	SLEW-RATE LIMITED	PKG CODE
MAX13485EELA+T	8 FDFN	Yes	L822-1
MAX13485EESA+	8 SO	Yes	S8-2
MAX13486EELA+T	8 FDFN	No	L822-1
MAX13486EESA+	8 SO	No	S8-2

+Denotes a lead-free package.

Note: All devices are specified over the -40°C to $+85^{\circ}\text{C}$ operating temperature range.

Absolute Maximum Ratings

(All voltages referenced to GND.)

VCC	+6V
DE, RE, DI	-0.3V to +6V
A, B	-8V to 13V
Short-Circuit Duration (RO, A, B) to GND	Continuous
Continuous Power Dissipation (TA = +70°C)	
8-Pin SO (derate 5.9mW/°C above +70°C)	471mW
8-Pin μ DFN (derate 4.8mW/°C above +70°C)	380.6mW

Operating Temperature Range	-40°C to +85°C
Junction Temperature	+150°C
Storage Temperature Range	-65°C to +150°C
Lead Temperature (soldering, 10s)	+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Electrical Characteristics

(VCC = +5V \pm 5%, TA = TMIN to TMAX, unless otherwise noted. Typical values are at VCC = +5V and TA = +25°C.) (Notes 1, 2)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
DRIVER							
Differential Driver Output	V _{OD}	R _{DIFF} = 54Ω, Figure 1		1.5		V	
		No load		V _{CC}			
Change in Magnitude of Differential Output Voltage	ΔV _{OD}	R _{DIFF} = 54Ω, Figure 1 (Note 3)		0.2		V	
Driver Common-Mode Output Voltage	V _{OC}	R _{DIFF} = 54Ω, Figure 1		V _{CC} / 2		3	V
Change in Magnitude of Common-Mode Voltage	ΔV _{OC}	R _{DIFF} = 54Ω, Figure 1 (Note 3)		0.2		V	
Input-High Voltage	V _{IH}	DI, DE, \overline{RE}		2.0		V	
Input-Low Voltage	V _{IL}	DI, DE, \overline{RE}		0.8		V	
Input Current	I _{IN}	DI, DE, \overline{RE}		±1		μA	
Driver Short-Circuit Output Current (Note 4)	I _{OSD}	0V ≤ V _{OUT} ≤ +12V		+50		+250	mA
		-7V ≤ V _{OUT} ≤ 0V		-250		-50	
Driver Short-Circuit Foldback Output Current Note 3)	I _{OSDF}	(V _{CC} - 1V) ≤ V _{OUT} ≤ +12V		20		mA	
		-7V ≤ V _{OUT} ≤ 0V		-20			
RECEIVER							
Input Current (A and B)	I _{A, B}	DE = GND, V _{CC} = GND or +5V	V _{IN} = +12V	250		μA	
			V _{IN} = -7V	-200			
Receiver-Differential-Threshold Voltage	V _{TH}	-7V ≤ V _{CM} ≤ +12V		-200		-50	mV
Receiver Input Hysteresis	ΔV _{TH}	V _A + V _B = 0V		25		mV	
Output-High Voltage	V _{OH}	I _O = -1.6mA, V _A - V _B > V _{TH}		V _{CC} - 1.5		V	

Electrical Characteristics (continued)

($V_{CC} = +5V \pm 5\%$, $T_A = T_{MIN}$ to T_{MAX} , unless otherwise noted. Typical values are at $V_{CC} = +5V$ and $T_A = +25^\circ C$.) (Notes 1, 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Output-Low Voltage	V_{OL}	$I_O = 1mA$, $V_A - V_B < -V_{TH}$			0.4	V
Tri-State Output Current at Receiver	I_{OZR}	$0V \leq V_O \leq V_{CC}$			± 1	μA
Receiver Input Resistance	R_{IN}	$-7V \leq V_{CM} \leq +12V$	48			k Ω
Receiver-Output Short-Circuit Current	I_{OSR}	$0V \leq V_{RO} \leq V_{CC}$	± 7		± 95	mA
POWER SUPPLY						
Supply Voltage	V_{CC}		4.75		5.25	V
Supply Current	I_{CC}	$DE = 1$, $\overline{RE} = 0$, no load			4.5	mA
Shutdown Supply Current	I_{SHDN}	$DE = 0$, $\overline{RE} = 1$			10	μA
ESD PROTECTION						
ESD Protection (A, B)		Air Gap Discharge IEC61000-4-2 (MAX13485E)		± 15		kV
		Human Body Model		± 15		
ESD Protection (All Other Pins)		Human Body Model		± 2		kV

Switching Characteristics—MAX13485E

($V_{CC} = +5V \pm 5\%$, $T_A = T_{MIN}$ to T_{MAX} , unless otherwise noted. Typical values are at $V_{CC} = +5V$ and $T_A = +25^\circ C$.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
DRIVER						
Driver Propagation Delay	t_{DPLH}	$R_{DIFF} = 54\Omega$, $C_L = 50pF$, Figures 2 and 3	200		1000	ns
	t_{DPLH}		200		1000	
Driver-Differential Output Rise or Fall Time	t_{HL}	$R_{DIFF} = 54\Omega$, $C_L = 50pF$, Figures 2 and 3	250		900	ns
	t_{LH}		250		900	
Driver-Differential Output Skew $ t_{DPLH} - t_{DPLH} $	t_{DSKEW}	$R_{DIFF} = 54\Omega$, $C_L = 50pF$, Figures 2 and 3			140	ns
Maximum Data Rate			500			kbps
Driver Enable to Output High	t_{DZH}	Figures 4 and 5			2500	ns
Driver Enable to Output Low	t_{DZL}	Figures 4 and 5			2500	ns
Driver Disable Time from High	t_{DHZ}	Figures 4 and 5			100	ns
Driver Disable Time from Low	t_{DLZ}	Figures 4 and 5			100	ns
Driver Enable from Shutdown to Output High	$t_{DZH(SHDN)}$	Figures 4 and 5			5500	ns
Driver Enable from Shutdown to Output Low	$t_{DZL(SHDN)}$	Figures 4 and 5			5500	ns
Time to Shutdown	t_{SHDN}		50	340	700	ns
RECEIVER						
Receiver Propagation Delay	t_{RPLH}	$C_L = 15pF$, Figures 6 and 7			80	ns
	t_{RPHL}				80	
Receiver Output Skew	t_{RSKEW}	$C_L = 15pF$, Figure 7			13	ns
Maximum Data Rate			500			kbps

Switching Characteristics—MAX13485E (continued)

(V_{CC} = +5V \pm 5%, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at V_{CC} = +5V and T_A = +25°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Receiver Enable to Output High	t _{RZH}	Figure 8			50	ns
Receiver Enable to Output Low	t _{RZL}	Figure 8			50	ns
Receiver Disable Time from High	t _{RHZ}	Figure 8			50	ns
Receiver Disable Time from Low	t _{RLZ}	Figure 8			50	ns
Receiver Enable from Shutdown to Output High	t _{RZH(SHDN)}	Figure 8			2200	ns
Receiver Enable from Shutdown to Output Low	t _{RZL(SHDN)}	Figure 8			2200	ns
Time to Shutdown	t _{SHDN}		50	340	700	ns

Switching Characteristics—MAX13486E

(V_{CC} = +5V \pm 5%, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at V_{CC} = +5V and T_A = +25°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
DRIVER						
Driver Propagation Delay	t _{DPLH}	R _{DIFF} = 54 Ω , C _L = 50pF, Figures 2 and 3			50	ns
	t _{DPLH}				50	
Driver Differential Output Rise or Fall Time	t _{HL}	R _{DIFF} = 54 Ω , C _L = 50pF, Figures 2 and 3			15	ns
	t _{LH}				15	
Differential Driver Output Skew t _{DPLH} - t _{DPLH}	t _{DSKEW}	R _{DIFF} = 54 Ω , C _L = 50pF, Figures 2 and 3			8	ns
Maximum Data Rate			16			Mbps
Driver Enable to Output High	t _{DZH}	Figures 4 and 5			50	ns
Driver Enable to Output Low	t _{DZL}	Figures 4 and 5			50	ns
Driver Disable Time from High	t _{DHZ}	Figures 4 and 5			50	ns
Driver Disable Time from Low	t _{DLZ}	Figures 4 and 5			50	ns
Driver Enable from Shutdown to Output High	t _{DZH(SHDN)}	Figures 4 and 5			2200	ns
Driver Enable from Shutdown to Output Low	t _{DZL(SHDN)}	Figures 4 and 5			2200	ns
Time to Shutdown	t _{SHDN}		50	340	700	ns
RECEIVER						
Receiver Propagation Delay	t _{RPLH}	C _L = 15pF, Figures 6 and 7			80	ns
	t _{RPHL}				80	
Receiver Output Skew	t _{RSKEW}	C _L = 15pF, Figure 7			13	ns
Maximum Data Rate			16			Mbps

Switching Characteristics—MAX13486E (continued)

($V_{CC} = +5V \pm 5\%$, $T_A = T_{MIN}$ to T_{MAX} , unless otherwise noted. Typical values are at $V_{CC} = +5V$ and $T_A = +25^\circ C$.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Receiver Enable to Output High	t_{RZH}	Figure 8			50	ns
Receiver Enable to Output Low	t_{RZL}	Figure 8			50	ns
Receiver Disable Time from High	t_{RHZ}	Figure 8			50	ns
Receiver Disable Time from Low	t_{RLZ}	Figure 8			50	ns
Receiver Enable from Shutdown to Output High	$t_{RZH(SHDN)}$	Figure 8			2200	ns
Receiver Enable from Shutdown to Output Low	$t_{RZL(SHDN)}$	Figure 8			2200	ns
Time to Shutdown	t_{SHDN}		50	340	700	ns

Note 1: μ DFN devices production tested at $+25^\circ C$. Overtemperature limits are generated by design.

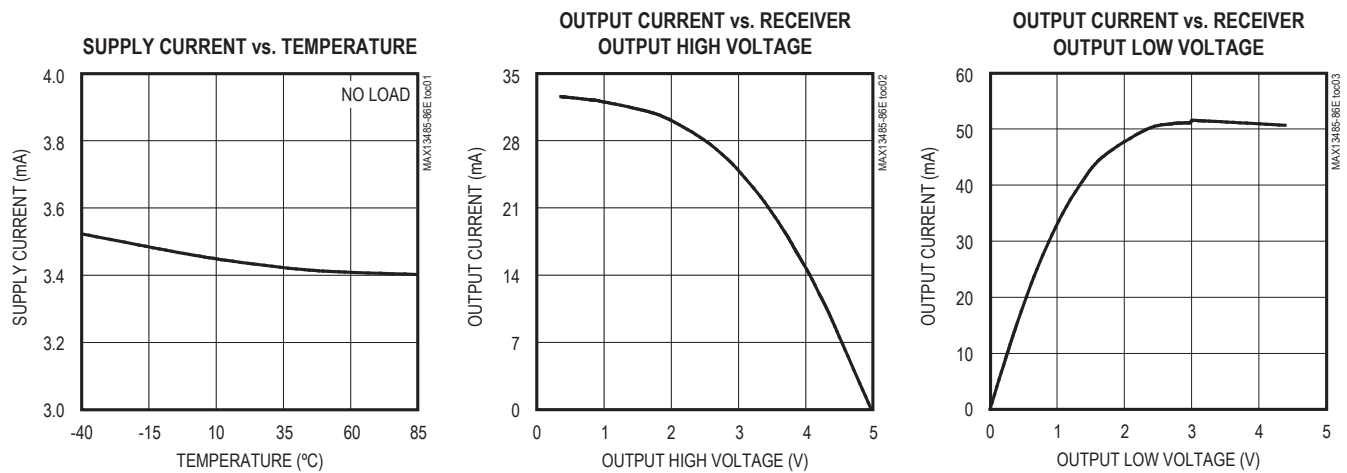
Note 2: All currents into the device are positive. All currents out of the device are negative. All voltages referred to device ground, unless otherwise noted.

Note 3: ΔV_{OD} and ΔV_{OC} are the changes in V_{OD} and V_{OC} when the DI input changes states.

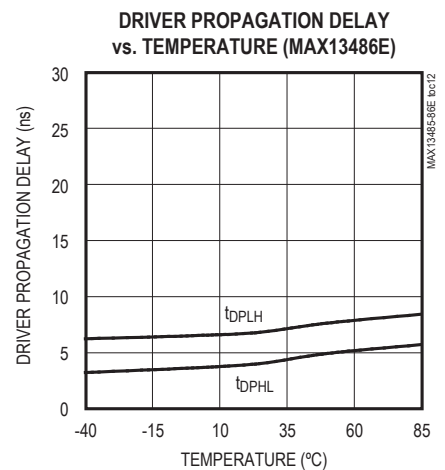
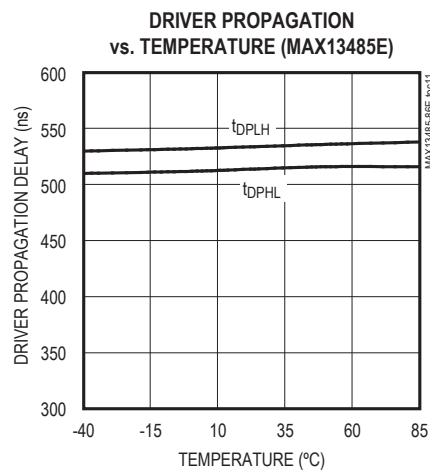
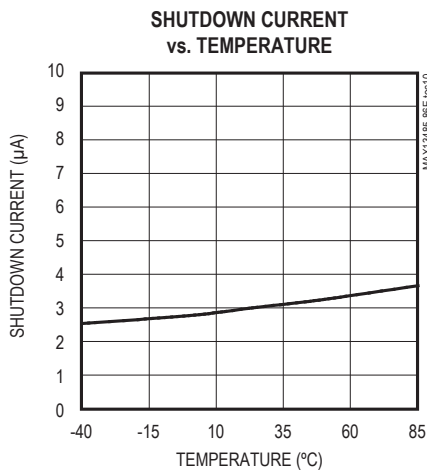
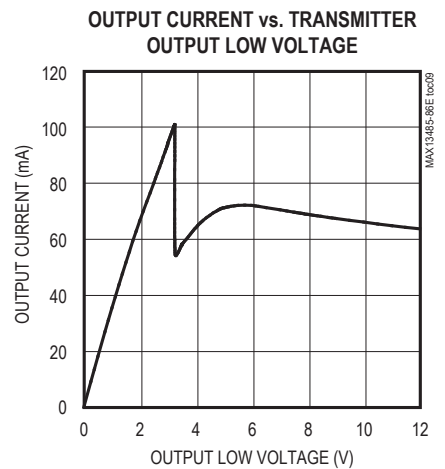
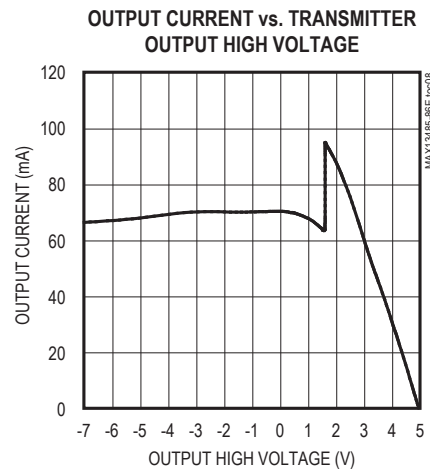
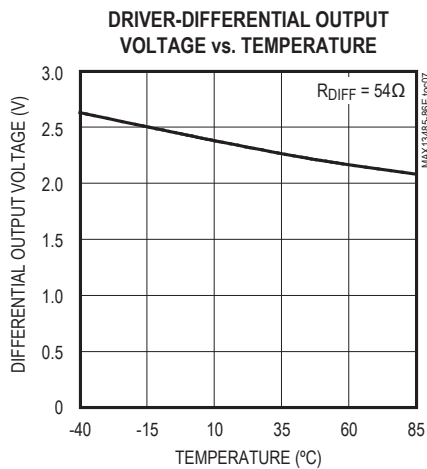
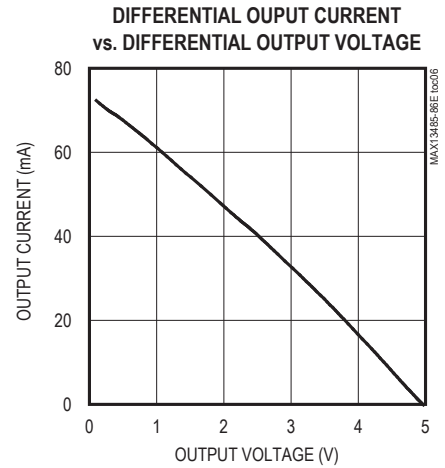
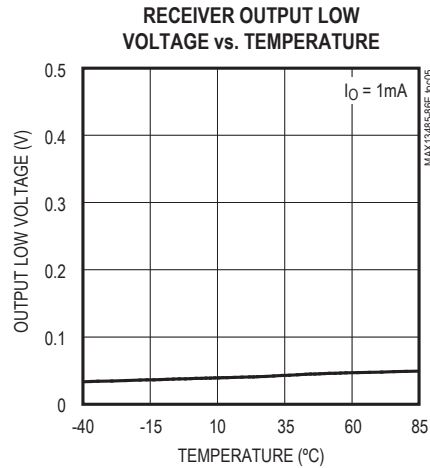
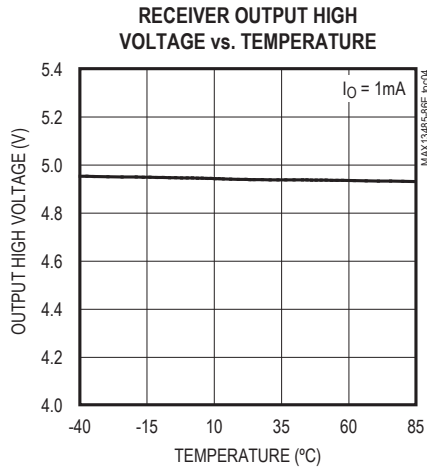
Note 4: The short-circuit output current applied to peak current just prior to foldback current limiting. The short-circuit foldback output current applies during current limiting to allow a recovery from bus contention.

Typical Operating Characteristics

($V_{CC} = +5V$, $T_A = +25^\circ C$, unless otherwise noted.)

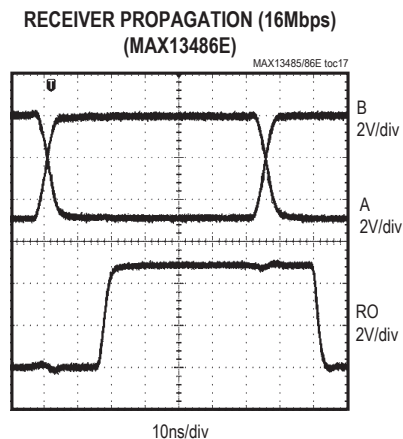
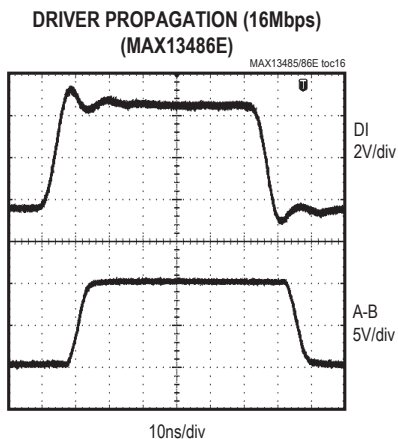
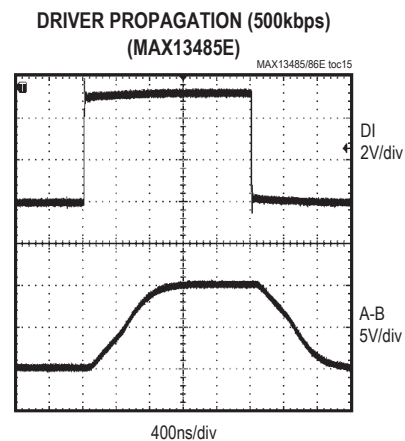
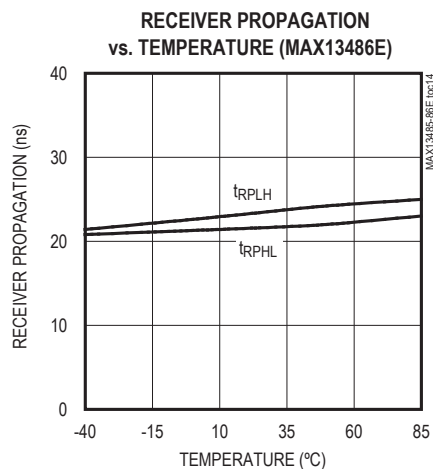
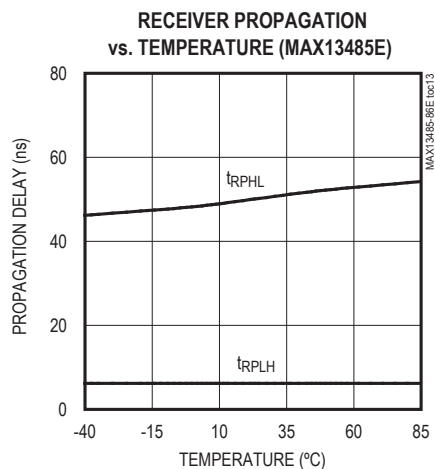


Typical Operating Characteristics (continued)

(V_{CC} = +5V, T_A = +25°C, unless otherwise noted.)

Typical Operating Characteristics (continued)

($V_{CC} = +5V$, $T_A = +25^\circ C$, unless otherwise noted.)



Test Circuits and Waveforms

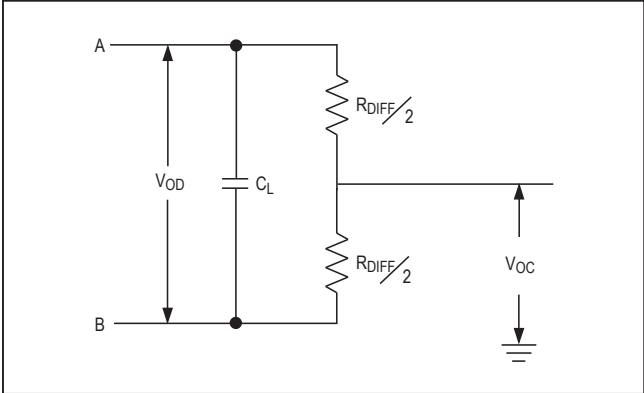


Figure 1. Driver DC Test Load

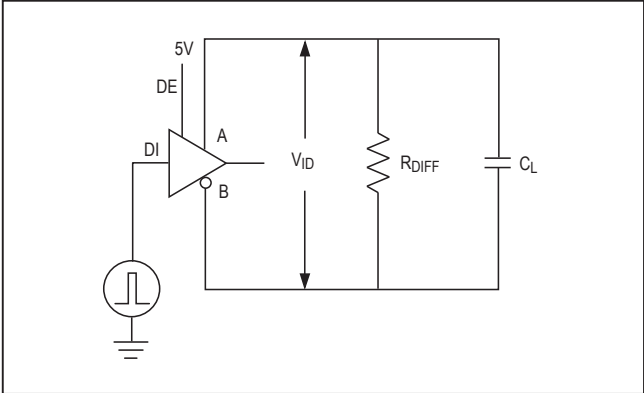


Figure 2. Driver Timing Test Circuit

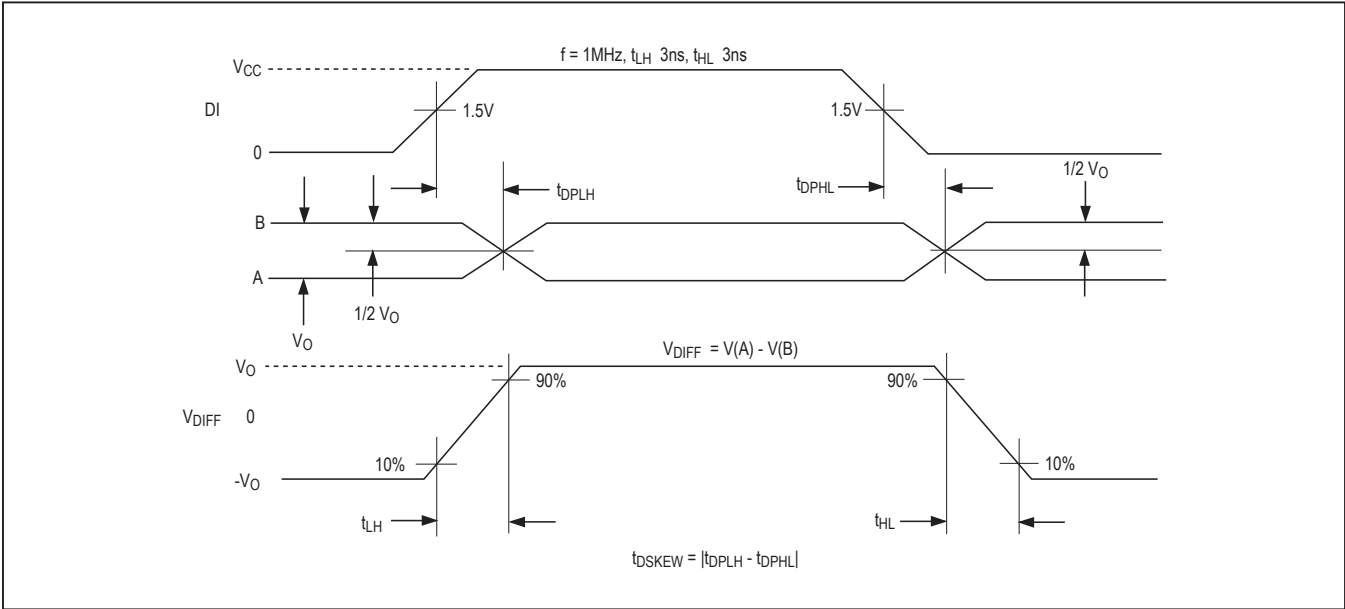


Figure 3. Driver Propagation Delays

Test Circuits and Waveforms (continued)

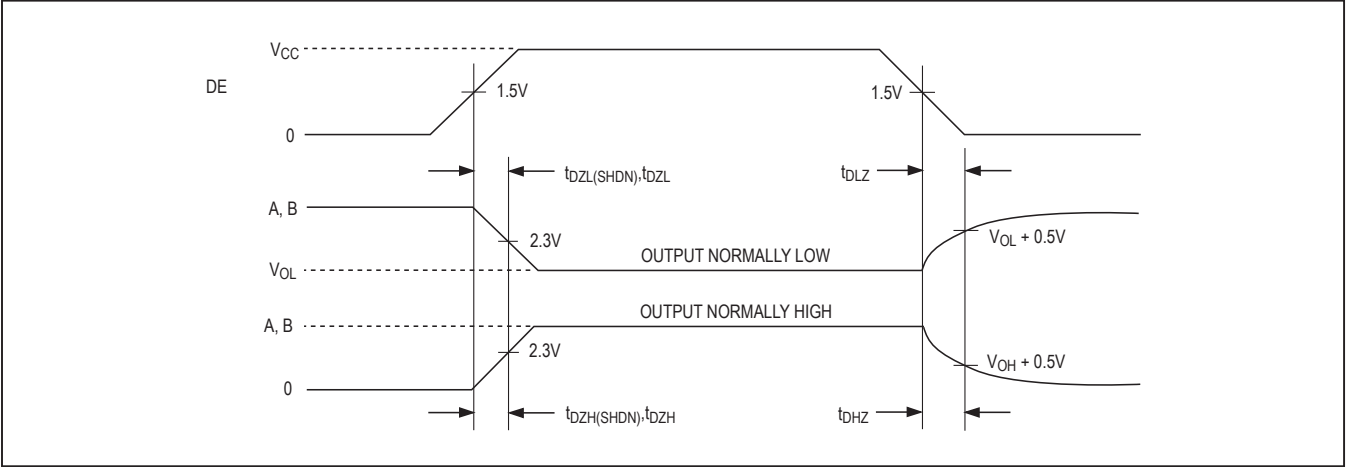


Figure 4. Driver Enable and Disable Times

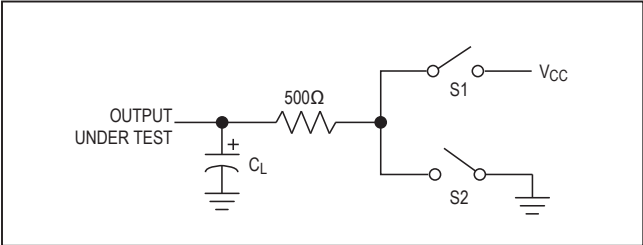


Figure 5. Driver-Enable and -Disable-Timing Test Load

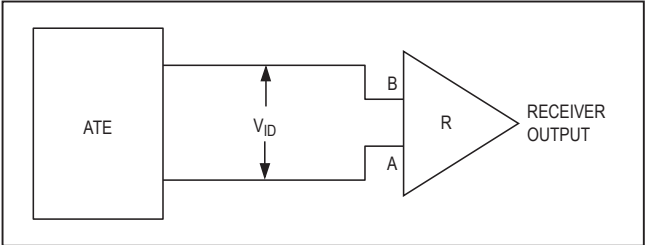


Figure 6. Receiver Propagation Delay Test Circuit

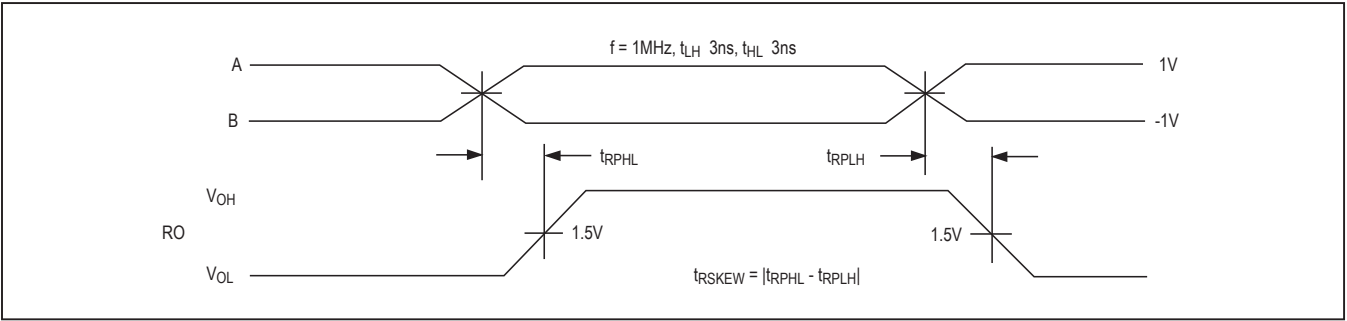


Figure 7. Receiver Propagation Delays

Pin Description

PIN	NAME	FUNCTION
1	RO	Receiver Output
2	\overline{RE}	Receiver Output Enable. Drive \overline{RE} low to enable RO. RO is high impedance when \overline{RE} is high. Drive \overline{RE} high and DE low to enter low-power shutdown mode. \overline{RE} is a hot-swap input (see the <i>Hot-Swap Capability</i> section for more details).
3	DE	Driver Output Enable. Drive DE high to enable the driver outputs. These outputs are high-impedance when DE is low. Drive \overline{RE} high and DE low to enter low-power shutdown mode. DE is a hot-swap input (see the <i>Hot-Swap Capability</i> section for more details).
4	DI	Driver Input. Drive DI low to force noninverting output low and inverting output high. Drive DI high to force noninverting output high and inverting output low (see the <i>Function Tables</i>).
5	GND	Ground
6	A	Noninverting Receiver Input and Noninverting Driver Output
7	B	Inverting Receiver Input and Inverting Driver Output
8	V _{CC}	Positive Supply, V _{CC} = +5V \pm 5%. Bypass V _{CC} to GND with a 0.1 μ F capacitor.

Function Tables

TRANSMITTING				
INPUT			OUTPUT	
\overline{RE}	DE	DI	B	A
X	1	1	0	1
X	1	0	1	0
0	0	X	HIGH IMPEDANCE	HIGH IMPEDANCE
1	0	X	SHUTDOWN	

RECEIVING			
INPUT			OUTPUT
\overline{RE}	DE	A-B	RO
0	X	$\geq -50\text{mV}$	1
0	X	$\leq -200\text{mV}$	0
0	X	OPEN/SHORT	1
1	1	X	HIGH IMPEDANCE
1	0	X	SHUTDOWN

X = Don't care, shutdown mode, driver, and receiver outputs are in high impedance.

Test Circuits and Waveforms (continued)

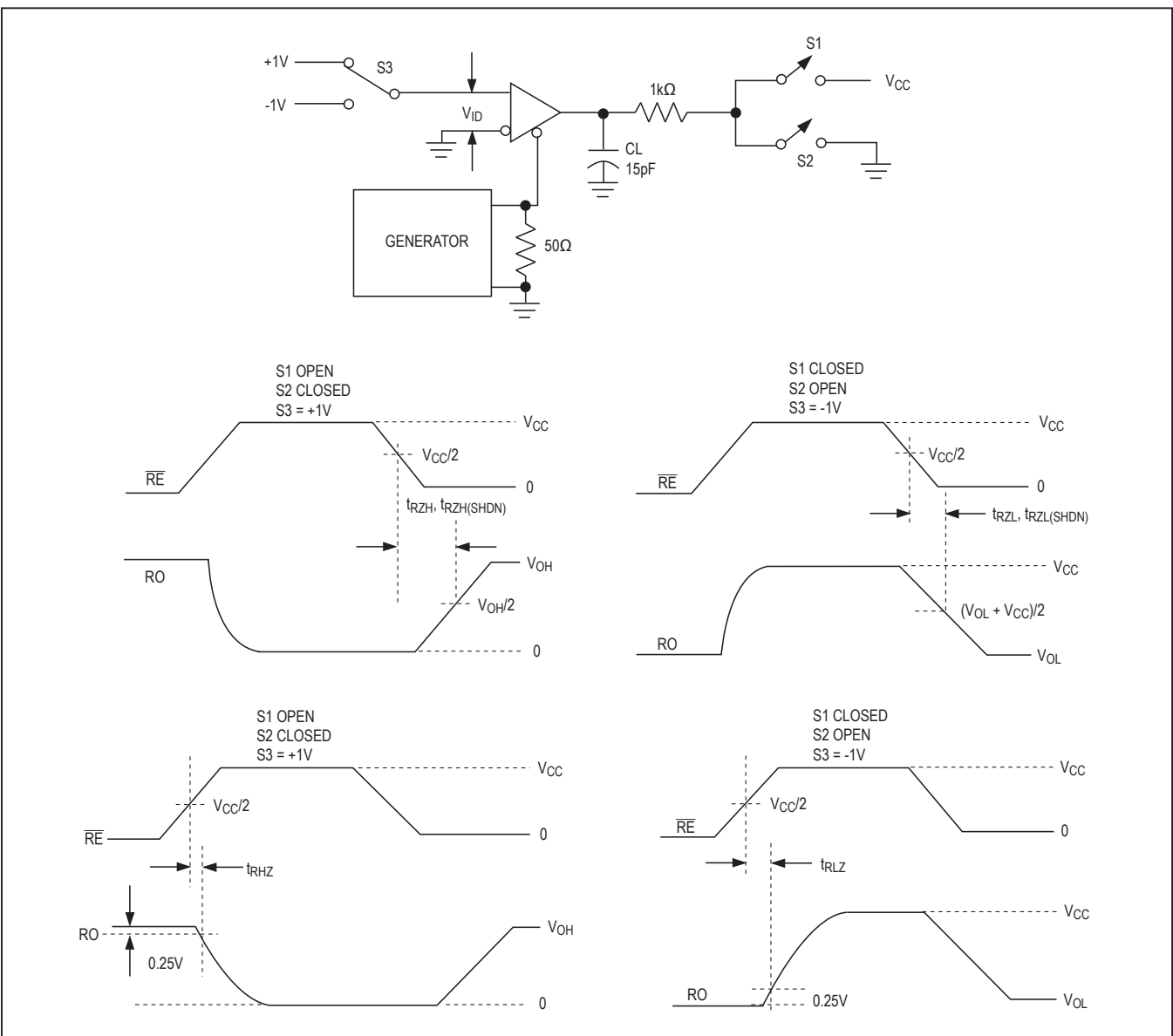


Figure 8. Receiver Enable and Disable Times

Detailed Description

The MAX13485E/MAX13486E half-duplex, high-speed transceivers for RS-485 communication contain one driver and one receiver. These devices feature failsafe circuitry that guarantees a logic-high receiver output when receiver inputs are open or shorted, or when they are connected to a terminated transmission line with all drivers disabled (see the Fail-Safe section). The MAX13485E/MAX13486E also feature a hot-swap capability allowing line insertion without erroneous data transfer (see the Hot-Swap Capability section). The MAX13485E features reduced slew-rate drivers that minimize EMI and reduce reflections caused by improperly terminated cables, allowing error-free transmission up to 500kbps. The MAX13486E driver slew rate is not limited, making transmit speeds up to 16Mbps possible.

Fail-Safe

The MAX13485E/MAX13486E guarantee a logic-high receiver output when the receiver inputs are shorted or open, or when they are connected to a terminated transmission line with all drivers disabled. This is done by setting the receiver input threshold between -50mV and -200mV. If the differential receiver input voltage (A - B) is greater than or equal to -50mV, RO is logic-high. If (A - B) is less than or equal to -200mV, RO is logic-low. In the case of a terminated bus with all transmitters disabled, the receiver's differential input voltage is pulled to 0V by the termination. With the receiver thresholds of the MAX13485E/MAX13486E, this results in a logic-high with a 50mV minimum noise margin. Unlike previous fail-safe devices, the -50mV to -200mV threshold complies with the $\pm 200\text{mV}$ EIA/TIA-485 standard.

Hot-Swap Capability

Hot-Swap Inputs

When circuit boards are inserted into a hot or powered backplane, differential disturbances to the data bus can lead to data errors. Upon initial circuit-board insertion, the data communication processor undergoes its own power-up sequence. During this period, the processor's logic-output drivers are high impedance and are unable to drive the DE and $\overline{\text{RE}}$ inputs of these devices to a defined logic level. Leakage currents up to $\pm 10\mu\text{A}$ from the high impedance state of the processor's logic drivers could cause standard CMOS enable inputs of a transceiver to drift to an incorrect logic level. Additionally, parasitic circuit-board capacitance could cause coupling of V_{CC} or GND to the enable inputs. Without the hot-swap capability, these factors could improperly enable the transceiver's driver or receiver.

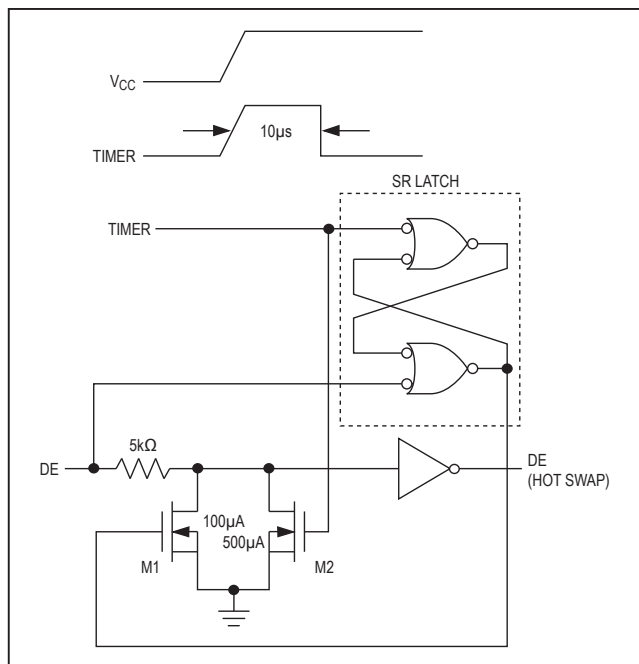


Figure 9. Simplified Structure of the Driver Enable Pin (DE)

When V_{CC} rises, an internal pulldown circuit holds \overline{DE} low and \overline{RE} high. After the initial power-up sequence, the pulldown circuit becomes transparent, resetting the hot-swap tolerable input.

Hot-Swap Input Circuitry

The enable inputs feature hot-swap capability. At the input there are two nMOS devices, M1 and M2 (Figure 9). When V_{CC} ramps from zero, an internal $7\mu s$ timer turns on M2 and sets the SR latch, which also turns on M1. Transistors M2, a 1.5mA current sink, and M1, a $500\mu A$ current sink, pull DE to GND through a $5k\Omega$ resistor. M2 is designed to pull DE to the disabled state against an external parasitic capacitance up to $100pF$ that can drive DE high. After $7\mu s$, the timer deactivates M2 while M1 remains on, holding DE low against tristate leakages that can drive DE high. M1 remains on until an external source overcomes the required input current. At this time, the SR latch resets and M1 turns off. When M1 turns off, DE reverts to a standard highimpedance CMOS input. Whenever V_{CC} drops below 1V, the hot-swap input is reset.

For $\overline{\text{RE}}$ there is a complementary circuit employing two pMOS devices pulling $\overline{\text{RE}}$ to V_{CC} .

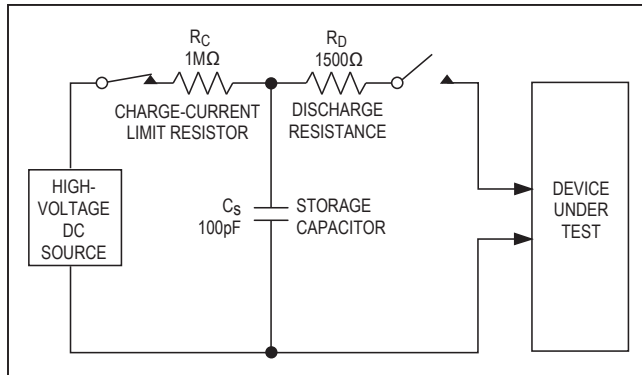


Figure 10a. Human Body ESD Test Model

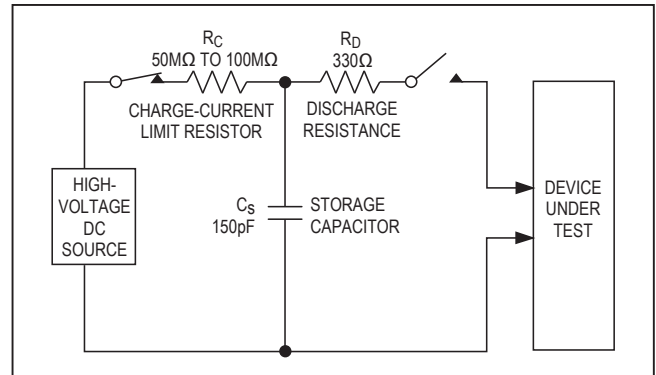


Figure 10c. IEC 61000-4-2 ESD Test Model

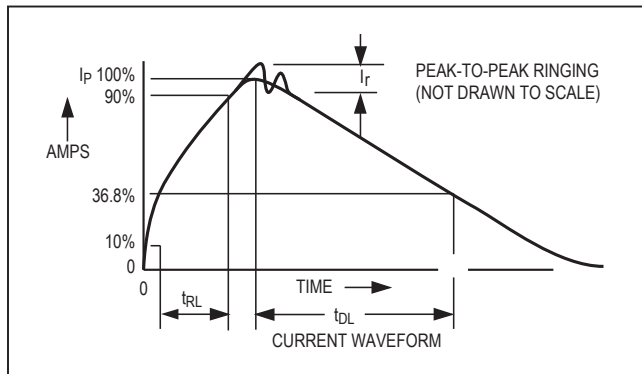


Figure 10b. Human Body Current Waveform

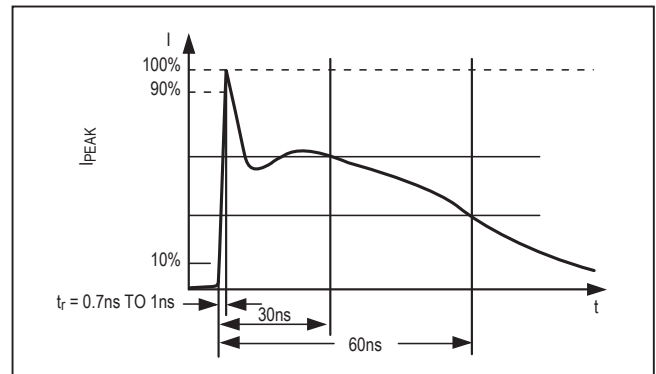


Figure 10d. IEC 61000-4-2 ESD Generator Current Waveform

+15V ESD Protection

As with all Maxim devices, ESD-protection structures are incorporated on all pins to protect against electrostatic discharges encountered during handling and assembly. The driver outputs and receiver inputs of the MAX13485E/MAX13486E have extra protection against static electricity. Maxim's engineers have developed state-of-the-art structures to protect these pins against ESD of $\pm 15\text{kV}$ without damage. The ESD structures withstand high ESD in all states: normal operation, shutdown, and powered down. After an ESD event, the MAX13485E/MAX13486E keep working without latchup or damage.

ESD protection can be tested in various ways. The transmitter outputs and receiver inputs of the MAX13485E/MAX13486E are characterized for protection to the following limits:

- $\pm 15\text{kV}$ using the Human Body Model
- $\pm 15\text{kV}$ using the Air Gap Discharge Method specified in IEC 61000-4-2 (MAX13485E only)

ESD Test Conditions

ESD performance depends on a variety of conditions. Contact Maxim for a reliability report that documents test setup, test methodology, and test results.

Human Body Model

Figure 10a shows the Human Body Model, and Figure 10b shows the current waveform it generates when discharged into a low impedance. This model consists of a 100pF capacitor charged to the ESD voltage of interest, which is then discharged into the test device through a $1.5\text{k}\Omega$ resistor.

IEC 61000-4-2

The IEC 61000-4-2 standard covers ESD testing and performance of finished equipment. However, it does not specifically refer to integrated circuits. The MAX13485E/MAX13486E help equipment designs to meet IEC 61000-4-2, without the need for additional ESD-protection components.

The major difference between tests done using the Human Body Model and IEC 61000-4-2 is higher peak current in IEC 61000-4-2 because series resistance is lower in the IEC 61000-4-2 model. Hence, the ESD

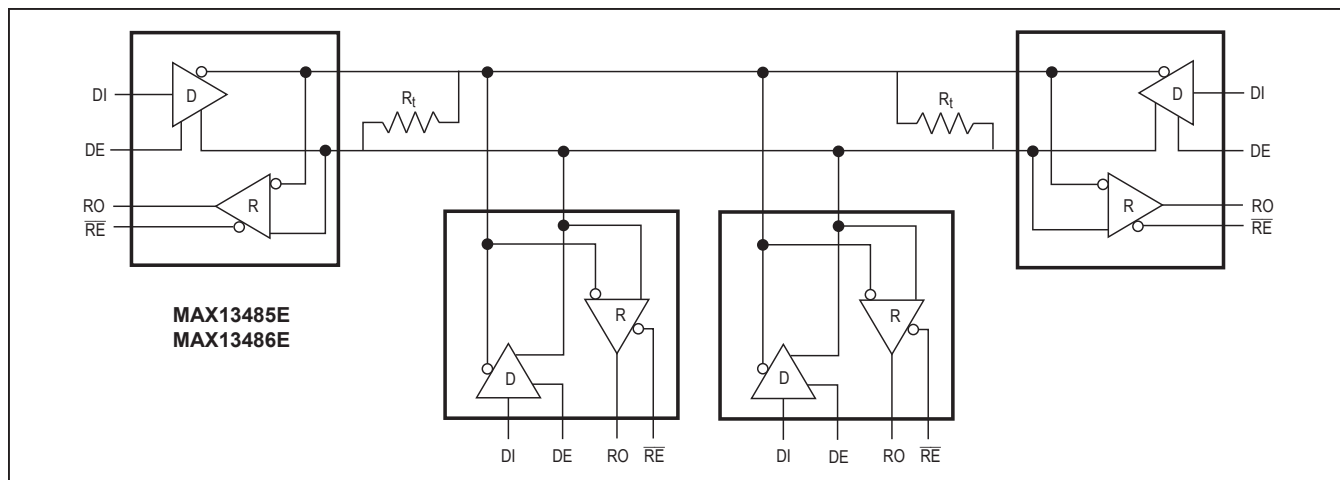


Figure 11. Typical Half-Duplex RS-485 Network

withstand voltage measured to IEC 61000-4-2 is generally lower than that measured using the Human Body Model. Figure 10c shows the IEC 61000-4-2 model, and Figure 10d shows the current waveform for the IEC 61000-4-2 ESD Contact Discharge test.

Machine Model

The machine model for ESD tests all pins using a 200pF storage capacitor and zero discharge resistance. The objective is to emulate the stress caused when I/O pins are contacted by handling equipment during test and assembly. Of course, all pins require this protection, not just RS-485 inputs and outputs.

The air-gap test involves approaching the device with a charged probe. The contact-discharge method connects the probe to the device before the probe is energized.

Applications Information

128 Transceivers on the Bus

The standard RS-485 receiver input impedance is 12k Ω (1-unit load), and the standard driver can drive up to 32-unit loads. The MAX13485E/MAX13486E have a 1/4-unit load receiver input impedance (48k Ω), allowing up to 128 transceivers to be connected in parallel on one communication line. Any combination of these devices, as well as other RS-485 transceivers with a total of 32-unit loads or fewer, can be connected to the line.

Reduced EMI and Reflections

The MAX13485E features reduced slew-rate drivers that minimize EMI and reduce reflections caused by improperly terminated cables, allowing error-free data transmission up to 500kbps.

Low-Power Shutdown Mode

Low-power shutdown mode is initiated by bringing both $\overline{\text{RE}}$ high and DE low. In shutdown, the devices draw a maximum of 10 μ A of supply current.

$\overline{\text{RE}}$ and DE can be driven simultaneously. The devices are guaranteed not to enter shutdown if $\overline{\text{RE}}$ is high and DE is low for less than 50ns. If the inputs are in this state for at least 700ns, the devices are guaranteed to enter shutdown.

Enable times t_{ZH} and t_{ZL} (see the Switching Characteristics) assume the devices were not in a low-power shutdown state. Enable times $t_{ZH}(\text{SHDN})$ and $t_{ZL}(\text{SHDN})$ assume the devices were in shutdown state. It takes drivers and receivers longer to become enabled from lowpower shutdown mode ($t_{ZH}(\text{SHDN})$, $t_{ZL}(\text{SHDN})$) than from driver-/receiver-disable mode (t_{ZH} , t_{ZL}).

Line Length

The RS-485 standard covers line lengths up to 4000ft.

Typical Applications

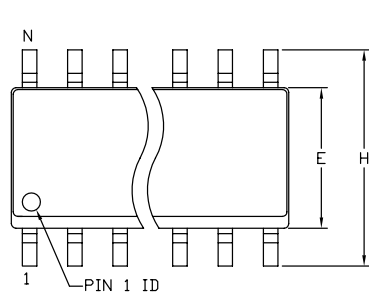
The MAX13485E/MAX13486E transceivers are designed for half-duplex, bidirectional data communications on multipoint bus transmission lines. Figure 11 shows typical network applications circuits. To minimize reflections, terminate the line at both ends in its characteristic impedance, and keep stub lengths off the main line as short as possible. The slew-rate-limited MAX13485E is more tolerant of imperfect termination.

Chip Information

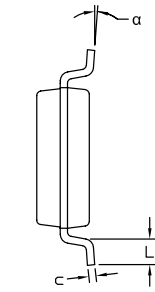
PROCESS: BiCMOS

Package Information

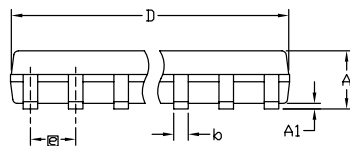
For the latest package outline information and land patterns (footprints), go to www.analog.com/packages. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.



TOP VIEW



END VIEW



SIDE VIEW

COMMON DIMENSIONS				
SYMBOL	INCHES		MM	
	MIN.	MAX.	MIN.	MAX.
A	.053	.069	1.35	1.75
A1	.004	.010	0.10	0.25
b	.014	.019	0.35	0.49
c	.007	.010	0.19	0.25
E	.150	.157	3.80	4.00
e	.050	BSC	1.27	BSC
H	.228	.244	5.80	6.20
L	.016	.050	0.40	1.27
alpha	0°	8°	0°	8°

VARIATION A				
SYMBOL	INCHES		MM	
	MIN.	MAX.	MIN.	MAX.
D	.189	.197	4.80	5.00
N	8			
MS012	AA			
PKG. CODE	S8-2, S8-4, S8-5, S8-6F, S8-7F, S8-8F, S8-10F, S8-11F, S8-16F			

VARIATION B				
SYMBOL	INCHES		MM	
	MIN.	MAX.	MIN.	MAX.
D	.337	.344	8.55	8.75
N	14			
MS012	AB			
PKG. CODE	S14-1, S14-4, S14-5, S14-6, S14M-4, S14M-5, S14M-6, S14M-7			

VARIATION C				
SYMBOL	INCHES		MM	
	MIN.	MAX.	MIN.	MAX.
D	.386	.394	9.80	10.00
N	16			
MS012	AC			
PKG. CODE	S16-1, S16-3, S16-5, S16-6, S16-8, S16-7F, S16-9F, S16-10F, S16M-3, S16M-6			

NOTES:

1. ALL DIMENSIONS ARE IN MILLIMETERS UNLESS OTHERWISE SPECIFIED.
2. MATERIAL MUST COMPLY WITH BANNED AND RESTRICTED SUBSTANCES SPEC # 10-0131.
3. DIMENSIONS D AND E DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE MOLD PROTRUSION IS 0.15 MM (.006") PER SIDE.
4. LEADS TO BE COPLANAR WITHIN 0.10mm (.004").
5. MEETS JEDEC MS012
6. ALL DIMENSIONS APPLY TO BOTH LEADED (-) AND PbFREE (+) PKG. CODES.

-DRAWING NOT TO SCALE-

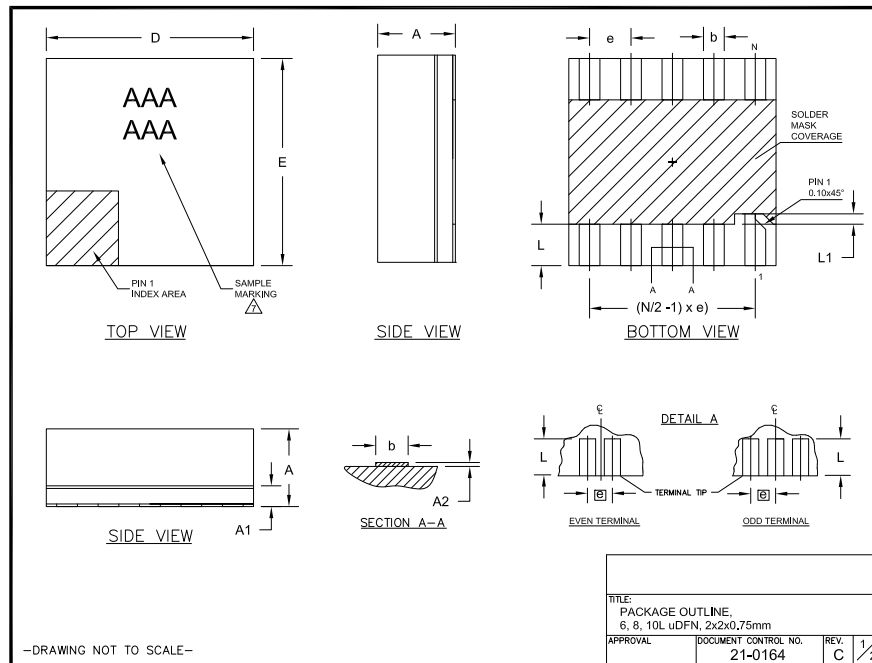


TITLE:
PACKAGE OUTLINE,
8L, 14L, 16L SOIC .150 INCH

APPROVAL	DOCUMENT CONTROL NO.	REV.	1/1
	21-0041	C	

Package Information (continued)

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Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	1/07	Initial release	—
1	8/24	Removed all RS-422 references	1–17



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