Data Sheet

LTM4707

16V_{IN}, 16A Ultralow Noise Silent Switcher 3 µModule Regulator

FEATURES

- Complete Solution in <1cm² (Single-sided PCB) or 0.5cm² (Dual-sided PCB)
- Low Noise Silent Switcher®3 Architecture
  - Ultralow EMI Emissions
  - Ultralow RMS Noise (10Hz to 100kHz): 8µV_{RMS}
- ±1.5% Maximum Total DC Output Voltage Error Over Line, Load, and Temperature
- Input Voltage Range: 3V to 16V
- Output Voltage Range: 0.3V to 6V
- 16A Maximum Continuous Output Current
- Adjustable and Synchronizable: 300kHz to 3MHz
- Current Mode Control, Fast Transient Response
- Forced Continuous Mode (FCM) Capability
- Multiphase Parallel with Current Sharing
- Programmable Power Good
- Available in a *49-Lead, 6.25mm × 6.25mm × 5.07mm, BGA* Package

APPLICATIONS

- Telecom, Networking, and Industrial equipment
- RF power supplies, including PLLs, VCOs, Mixers, LNAs, and PAs
- Low noise Instrumentation
- High-speed and High-precision Data Converters

GENERAL DESCRIPTION

The *LTM4707* is a complete 16A step-down Silent Switcher 3 power µModule® (power micromodule) regulator in a tiny 6.25mm × 6.25mm × 5.07mm BGA package. Included in the package are the switching controller, the power MOSFETs, an inductor, and the supported components. Operating over an input voltage range of 3V to 16V, the LTM4707 supports an output range of 0.3V to 6V. A single resistor sets the output voltage, providing unity-gain operation over the output range, resulting in virtually constant-output noise independent of output voltage. Only bulk input and output capacitors are needed to finish the design.

The LTM4707 employs *Silent Switcher 3* architecture with internal hot loop bypass capacitors to achieve both low electromagnetic interference (EMI) and high efficiency. The LTM4707 has an ultralow noise architecture to obtain exceptional low frequency (<100kHz) output noise. These low EMI and low noise features make the LTM4707 ideal for high current and noise-sensitive applications that benefit from the high efficiency of a synchronous switching regulator. The LTM4707 is available with a RoHS-compliant terminal finish.

TYPICAL APPLICATION

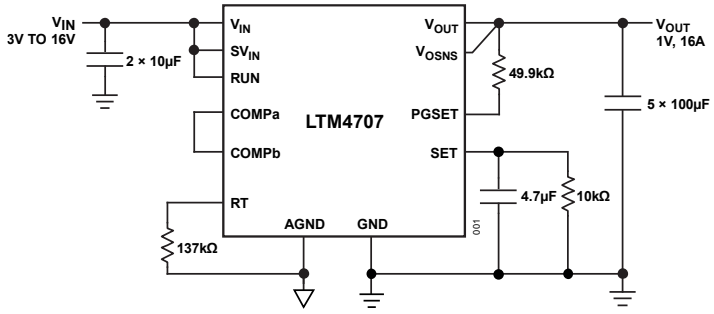

Figure 1. 3V to 16V Input to 1V, 16A Output

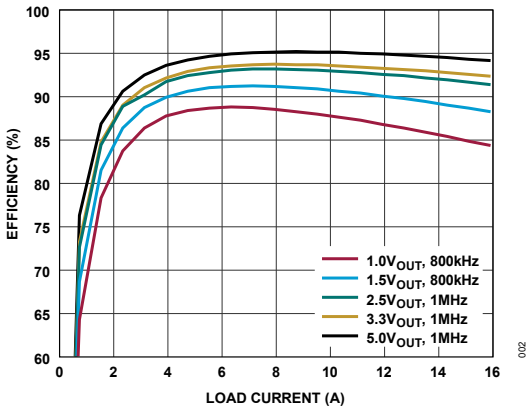

Figure 2. Efficiency, V_{IN} = 12V

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REVISION HISTORY

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGE NUMBER
0	12/24	Initial release.	—
A	7/25	Aligned Table 3. Updated Figure 31. Updated Figure 40. Updated Figure 42.	8 17 30 32

SPECIFICATIONS

Table 1. Electrical Characteristics

(T_A = 25°C, V_{IN} = 12V, See typical application.[1])

PARAMETER	SYMBOL	CONDITIONS	COMMENTS	MIN	TYP	MAX	UNITS
Power input DC voltage	V_{IN}		–40°C ≤ T_J ≤ 125°C	3		16	V
Signal input DC voltage[6]	SV_{IN}		–40°C ≤ T_J ≤ 125°C	3		16	V
Output voltage range	$V_{OUT(RANGE)}$	V_{PGSET} = 0.5V	–40°C ≤ T_J ≤ 125°C	0.3		6	V
Output voltage, total variation with line and load	$V_{OUT(DC)}$	R_T = 47kΩ FCM, V_{IN} = 3V to 16V, I_{OUT} = 100mA to 16A	–40°C ≤ T_J ≤ 125°C	0.985	1	1.015	V
SET pin current	I_{SET}	V_{SET} = 1V, I_{OUT} = 100mA		99.5	100	100.5	µA
Fast startup set pin current	I_{SET_START}	V_{SET} = 1V, V_{PGSET} = 0V		2.2	2.7	3.2	mA
Startup time[2, 7]	t_{START}	V_{OUT} = 1V, C_{SET} = 1µF, V_{PGSET} = 0.5V			25		ms
		V_{OUT} = 1V, C_{SET} = 4.7µF, V_{PGSET} = 0.5V			120		ms
		V_{OUT} = 1V, C_{SET} = 1µF, R_{PGSET} = 49.9kΩ			1		ms
		V_{OUT} = 1V, C_{SET} = 4.7µF, R_{PGSET} = 49.9kΩ			2.5		ms
RUN pin ON threshold	V_{RUN}	V_{RUN} rising	–40°C ≤ T_J ≤ 125°C	1.27	1.32	1.37	V
RUN pin hysteresis	V_{RUN}				44		mV
Internal V_{CC} voltage	V_{INTVCC}	SV_{IN} = 4V to 16V		3.2	3.4	3.6	V
SV_{IN} quiescent current	I_{Q_SVIN}	V_{RUN} = 0V, shutdown			55		µA
		R_T = 47kΩ, FCM			40		mA
Output noise spectral density (2kHz)[2, 3, 4, 5]	$V_{OUT\_SPOTNOISE}$	V_{OUT} = 1V, C_{OUT} = 500µF, R_{SET} = 10kΩ, C_{SET} = 4.7µF, f_{SW} = 2MHz			4		$nV/\sqrt{Hz}$
Output rms noise (10Hz to 100kHz)[2, 3, 4, 5]	$V_{OUT\_RMSNOISE}$	V_{OUT} = 1V, BW = 10Hz to 100kHz, I_{OUT} = 0.5A, C_{OUT} = 500µF, R_{SET} = 10kΩ, C_{SET} = 4.7µF, 2MHz			8		$µV_{RMS}$
Output continuous current range	$I_{OUT(DC)}$	V_{OUT} = 1V				16	A

(T_A = 25°C, V_{IN} = 12V, See typical application.[1])

PARAMETER	SYMBOL	CONDITIONS	COMMENTS	MIN	TYP	MAX	UNITS
Output voltage line regulation	$\Delta V_{OUT(LINE)}/V_{OUT}$	V_{OUT} = 1V, V_{IN} = 3V to 16V, I_{OUT} = 100mA	–40°C ≤ T_J ≤ 125°C			0.15	%
Output voltage load regulation[5]	$\Delta V_{OUT(LOAD)}/V_{OUT}$	V_{OUT} = 1V, I_{OUT} = 100mA to 16A	–40°C ≤ T_J ≤ 125°C			1.2	%
V_{OSNS} output current	I_{VOSNS}	V_{OSNS} = 1V		80	160	240	nA
Output ripple voltage[2]	$V_{OUT(AC)}$	I_{OUT} = 100mA, C_{OUT} = 500µF, V_{OUT} = 1V, R_T = 47kΩ			8		mV
Output current limit	I_{OUT_PK}				27	30	A
Minimum on-time	t_{ON_MIN}	V_{IN} =16V			18		ns
PGSET upper threshold	V_{PGSET}	PGSET rising		525	537.5	550	mV
PGSET upper threshold hysteresis	V_{PGSET}				8		mV
PGSET lower threshold	V_{PGSET}	PGSET falling		455	462.5	475	mV
PGSET lower threshold hysteresis	V_{PGSET}				8		mV
PGSET pin current	I_{PGSET}	V_{PGSET} = 0.5V			10		µA
PG leakage	I_{PG}	V_{PG} = 3.3V, SV_{IN} = 0V		–40		40	nA
PG pull-down resistance	R_{PG}	V_{PG} = 0.5V			380	420	Ω
Oscillator frequency	f_{OSC}	R_T = 392kΩ			300		kHz
		R_T = 47kΩ			2		MHz
		R_T = 28.7kΩ			3		MHz
SYNC threshold	SYNC_LEVEL	SYNC DC and clock low-level voltage		0.7			V
		SYNC DC and clock high-level voltage				1.5	V
PHMODE threshold	V_{PHMODE}	180° phase shift				0.7	V
PHMODE thresholds	V_{PHMODE}	90° phase shift		2.7			V

[1] The LTM4707 is tested under pulsed load conditions such that $T_J \approx T_A$. The LTM4707E is guaranteed to meet performance specifications over the 0°C to 125°C internal operating temperature range. Specifications over the full –40°C to 125°C internal operating temperature range are assured by design, characterization, and correlation with statistical process controls. The LTM4707I is guaranteed to meet specifications over the full –40°C to 125°C internal operating temperature range. Note that the maximum ambient temperature consistent with these specifications is determined by specific operating conditions in conjunction with board layout, the rated package thermal resistance, and other environmental factors.

[2] Not subject to production test. Guaranteed by design.

[3] V_{OSNS} pin connected directly to V_{OUT}.

[4] Adding a capacitor across the SET pin resistor decreases output voltage noise. Adding this capacitor bypasses the SET pin resistor's thermal noise as well as the reference current's noise. The use of a SET pin bypass capacitor also increases startup time.

[5] See output current derating curves in the *Typical Performance Characteristics* section for different V_{IN}, V_{OUT}, and T_A conditions.

[6] The SV_{IN} pin supplies current to the internal circuitry and regulator. The SV_{IN} pin should be above 4V to achieve regulation of ±1.5% maximum total DC output voltage error over line, load, and temperature. Also, the SV_{IN} pin must be 0.4V higher than the desired V_{OUT} to provide sufficient headroom for the SET pin current reference.

[7] The startup time is defined as the time it takes from the RUN pin rising above the RUN threshold to when V_{OUT} has reached 90% of final values.

ABSOLUTE MAXIMUM RATINGS

T_A = 25°C unless otherwise specified.

Table 2. Absolute Maximum Ratings [1]

PARAMETER	RATING
V_{IN}, SV_{IN}, RUN, PG	18V
SYNC, V_{OUT}, V_{OSNS}, SET, PGSET	6V
PHMODE, COMPa, RT	4V
T_{SENSE}^+ to T_{SENSE}^- (current)	5mA
Internal operating temperature range (E-grade and I-grade)	–40°C to 125°C
Storage temperature range	–55°C to 125°C
Peak solder reflow body temperature	250°C

[1] The LTM4707 is tested under pulsed load conditions such that $T_J \approx T_A$. The LTM4707E is guaranteed to meet performance specifications over the 0°C to 125°C internal operating temperature range. Specifications over the full –40°C to 125°C internal operating temperature range are assured by design, characterization, and correlation with statistical process controls. The LTM4707I is guaranteed to meet specifications over the full –40°C to 125°C internal operating temperature range. Note that the maximum ambient temperature consistent with these specifications is determined by specific operating conditions in conjunction with board layout, the rated package thermal resistance, and other environmental factors.

Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

Thermal Resistance

Thermal performance is directly linked to the printed circuit board (PCB) design and operating environment. Close attention to PCB thermal design is required.

Electrostatic Discharge (ESD)

The following ESD information is provided for handling of ESD-sensitive devices in an ESD protected area only Human body model (HBM) per ANSI/ESDA/JEDEC JS-001 Field induced charged device model (FICDM) and charged device model (CDM) per ANSI/ESDA/JEDEC JS-002. International electrotechnical commission (IEC) electromagnetic compatibility: Part 4-2 (IEC) per IEC 61000-4-2. Machine model (MM) per ANSI/ESD STM5.2. MM voltage values are for characterization only.

ESD Ratings

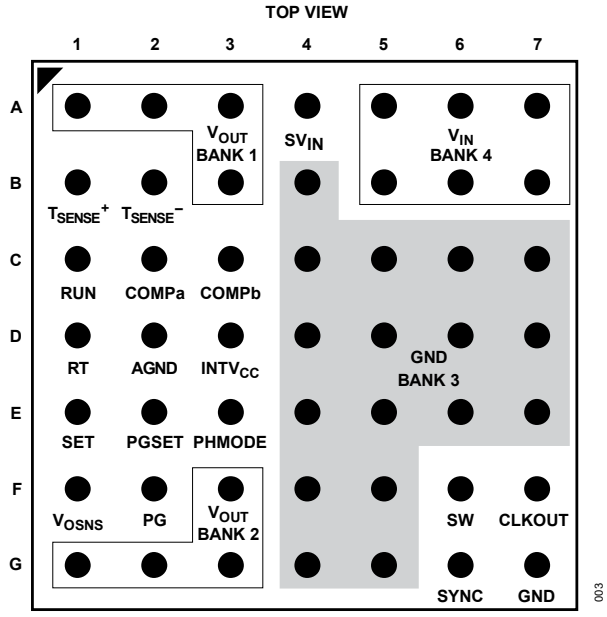
Table 3. LTM4707 ESD Ratings

ESD MODEL	WITHSTAND THRESHOLD (V)	CLASS
HBM	±4000	2
CDM	±1250	C3

ESD Caution

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS



BGA PACKAGE
49-PIN (6.25mm × 6.25mm × 5.07mm)
T_{JMAX} = 125°C, θ_{JA} = 20°C/W, θ_{JCtop} = 23°C/W,
$\theta_{JCbottom}$ = 12°C/W, WEIGHT = 0.7g

θ VALUES ARE DETERMINED BY SIMULATION PER JESD51 CONDITIONS.
θ_{JA} VALUE IS OBTAINED WITH THE EVALUATION BOARD.
SEE THE TYPICAL PERFORMANCE CHARACTERISTICS SECTION FOR LAB MEASUREMENT AND DERATING CURVES.

Figure 3. Pinout Configuration

PACKAGE ROW AND COLUMN LABELING MAY VARY AMONG µModule PRODUCTS. REVIEW EACH PACKAGE LAYOUT CAREFULLY.

Pin Descriptions

Table 4. Pin Descriptions

PIN CFG 1	NAME	DESCRIPTION
A4	SV_{IN}	Signal V_{IN}. This pin supplies current to the LTM4707 internal circuitry and regulator. If connected to a different supply other than V_{IN}, place a 1µF local bypass capacitor on this pin.
Bank 1 and Bank 2	V_{OUT}	Power Output Pins. Apply output load between these pins and GND pins. Recommend placing the output decoupling capacitor directly between these pins and the GND pins.
Bank 3 and G7	GND	Power Ground Pins for both input and output Returns.

PIN CFG 1	NAME	DESCRIPTION
Bank 4	V_{IN}	Power Input Pins. Apply input voltage between these pins and GND pins. Recommend placing input decoupling capacitor directly between V_{IN} pins and GND pins.
B1	T_{SENSE}^+	High-Side of the Internal Temperature Monitor Pin. An internal diode-connected NPN transistor is placed between T_{SENSE}^+ and T_{SENSE}^- pins. See the *Applications Information* section.
B2	T_{SENSE}^-	Low-Side of the Internal Temperature Monitor Pin.
C1	RUN	RUN Control Input. Enables chip operation by tying RUN above 1.32V (typical). Connecting the RUN pin below 0.4V shuts down the device.
C2	COMPa	Output of the Internal Error Amplifier. The voltage on this pin controls the peak switch current. Connect the COMPa pins from different channels together for parallel operation. Connect to COMPb to use the internal compensation or connect to an external RC network to use customized compensation.
C3	COMPb	Internal Compensation Network. Connect to COMPa to use the internal compensation in the majority of applications.
D1	RT	This pin sets the oscillator frequency with an external resistor to AGND.
D2	AGND	Analog Ground. Ground return for SYNC, RT, and COMP pins.
D3	$INTV_{CC}$	Internal 3.4V Regulator Bypass Pin. The internal power drivers and control circuits are powered by this voltage. Do not load the $INTV_{CC}$ pin with external circuitry. This pin should be floated.
E1	SET	Output Voltage Set. This pin is the noninverting input of the error amplifier and the regulation set-point for the LTM4707. The SET pin sources a precision 100µA current, which flows through an external resistor connected between SET and GND. The LTM4707's output voltage is determined by $V_{SET} = I_{SET} \times R_{SET}$. Output voltage ranges from 0.3V to 6V. Adding a capacitor from SET to GND improves noise at the expense of increased startup time. For optimum load regulation, Kelvin connects the ground side of the SET pin resistor directly to the load.
E2	PGSET	Power Good Set. The PG pin pulls low if PGSET increases above 537.5mV or decreases below 462.5mV. Connecting a pull-up resistor between V_{OUT} and PGSET sets the programmable power good threshold with Equation *1*. $$0.5V\ (\pm 7.5\%) \times \left(1 + \frac{R_{PGSET}}{49.9k\Omega}\right) \qquad (1)$$ As discussed in the *Applications Information* section, PGSET also activates the fast startup circuitry. If power good and fast startup functionalities are not needed, the PGSET pin must be connected to 0.5V. Do not float the PGSET pin.
E3	PHMODE	The PHMODE pin sets the phase shift of the clock signal of the CLKOUT pin. Connect PHMODE to ground for 180° phase shift, float for a 120° phase shift, and connect high to $INTV_{CC}$ (~3.4V) or an external supply >3V for a 90° phase shift.
F1	V_{OSNS}	Output Voltage Sense. This pin is the inverting input to the error amplifier. For optimal transient performance and load regulation, Kelvin connect V_{OSNS} directly to the output capacitor and the load. Also, connect the GND connections of the output capacitor and the SET pin capacitor directly together.

PIN CFG 1	NAME	DESCRIPTION
F2	PG	Output Power Good Indicator. The PG pin is the open-drain output of an internal comparator. The PG pin remains low until the V_{OSNS} pin is within ±7.5% of the final regulation voltage, and there are no fault conditions. The PG pin is also pulled low when EN is below 1V, $INTV_{CC}$ has fallen too low, SV_{IN} is too low, or during thermal shutdown. PG is valid when SV_{IN} is above 3V.
F6	SW	Switching Node of LTM4707. This pin is for test purposes only. Do not load the SW pin with external circuitry.
F7	CLKOUT	Output Clock Signal for PolyPhase® Operation. The CLKOUT pin provides a 50% duty-cycle square wave of the switching frequency. The phase of CLKOUT with respect to the LTM4707 internal clock is determined by the state of the PHMODE pin. CLKOUT's peak-to-peak amplitude is $INTV_{CC}$ to GND. Float this pin if the CLKOUT function is not used.
G6	SYNC	This pin programs three different operating modes: 1. Pulse-skipping mode (PSM). Connect this pin to GND for PSM to improve efficiency at light loads. 2. Forced continuous mode (FCM). This mode offers fast transient response and full-frequency operation over a wide load range. Connect this pin high to $INTV_{CC}$ (~3.4V) or to an external supply of greater than 3V for FCM. The device will also operate in this mode by default if this pin is left floating. 3. Synchronization mode. Drive this pin with a clock source to synchronize to an external clock and to put the device in FCM.

TYPICAL PERFORMANCE CHARACTERISTICS

T_A = 25°C, unless otherwise noted.

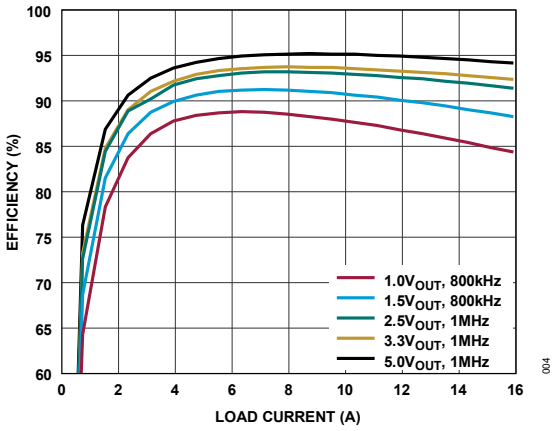


Figure 4. Efficiency vs. Load, V_{IN} = 12V

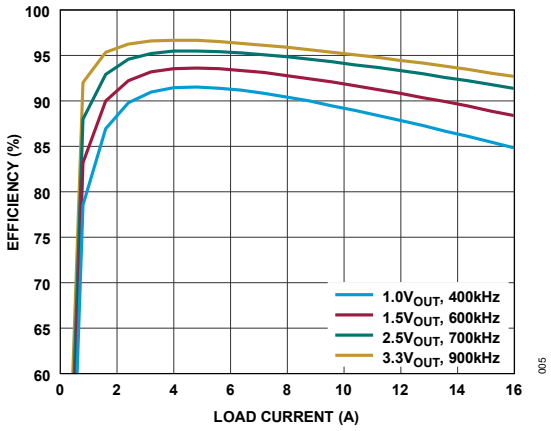


Figure 5. Efficiency vs. Load, V_{IN} = 5V

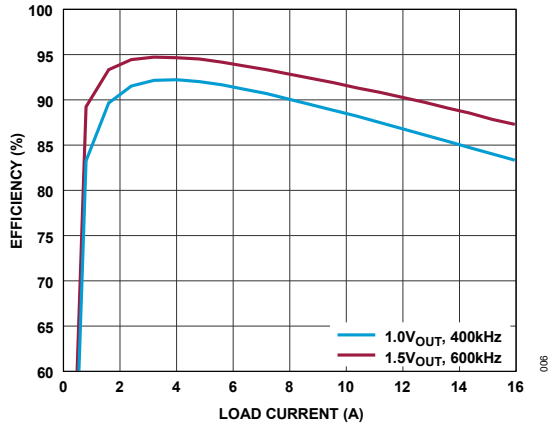


Figure 6. Efficiency vs. Load, V_{IN} = 3.3V

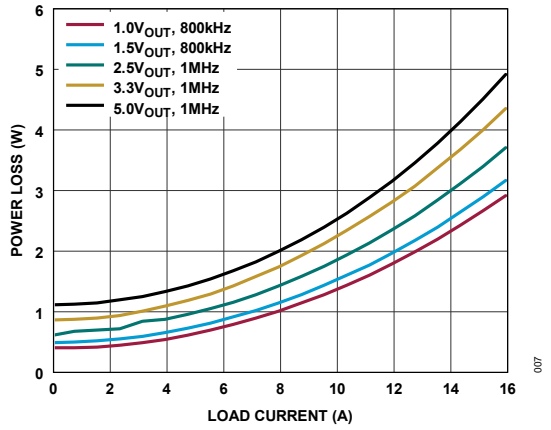


Figure 7. Power Loss vs. Load, V_{IN} = 12V

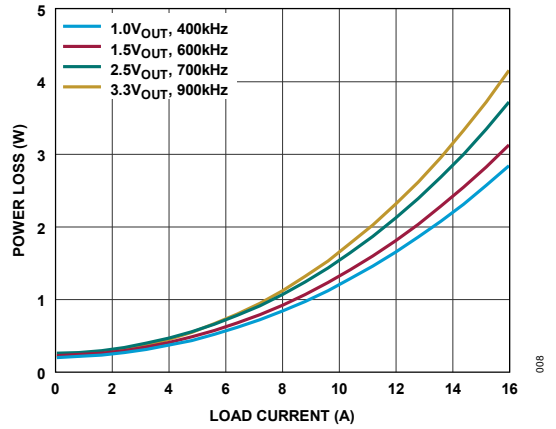


Figure 8. Power Loss vs. Load, V_{IN} = 5V

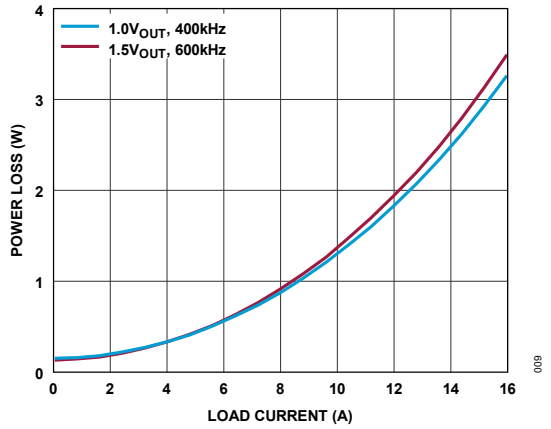


Figure 9. Power Loss vs. Load, V_{IN} = 3.3V

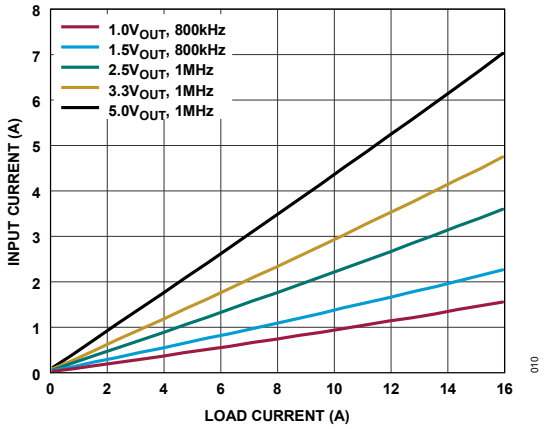


Figure 10. Input vs. Load Current, V_{IN} = 12V

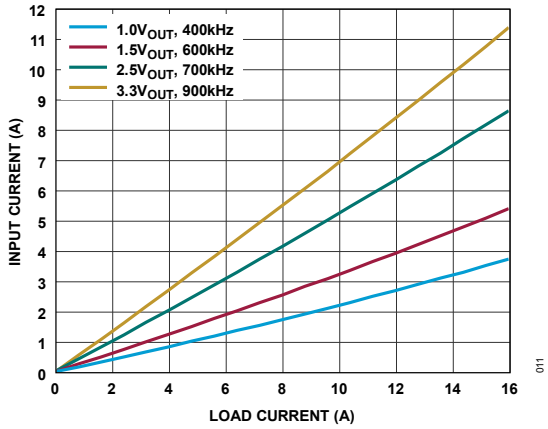


Figure 11. Input vs. Load Current, V_{IN} = 5V

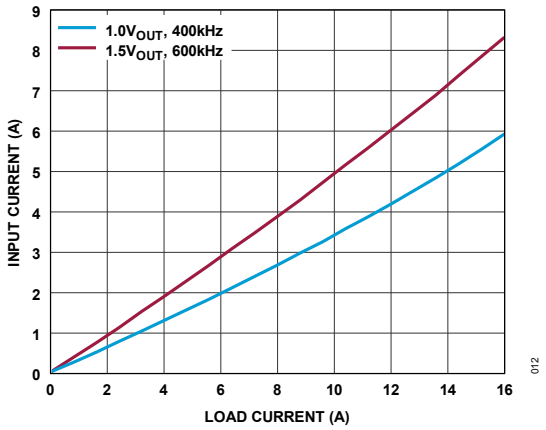


Figure 12. Input vs. Load Current, V_{IN} = 3.3V

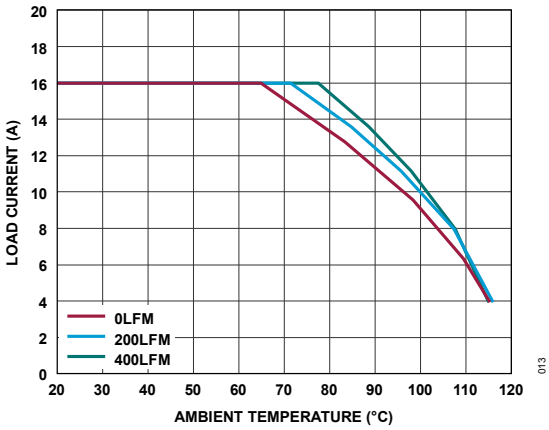


Figure 13. Derating Curve, V_{IN} = 5V, V_{OUT} = 1V, f_{SW} = 600kHz

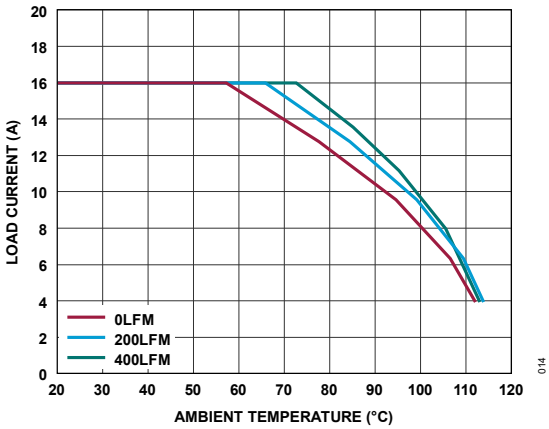


Figure 14. Derating Curve, V_{IN} = 5V, V_{OUT} = 1.5V, f_{SW} = 600kHz

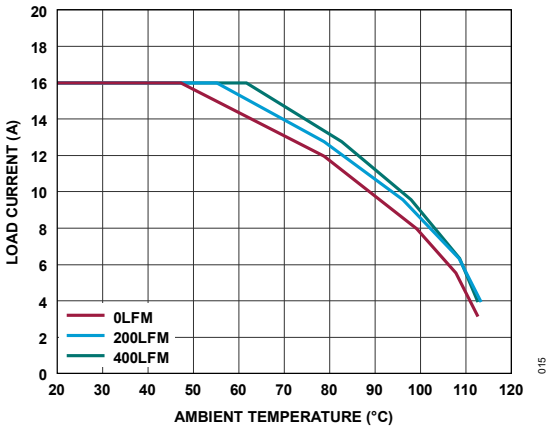


Figure 15. Derating Curve, V_{IN} = 5V, V_{OUT} = 2.5V, f_{SW} = 800kHz

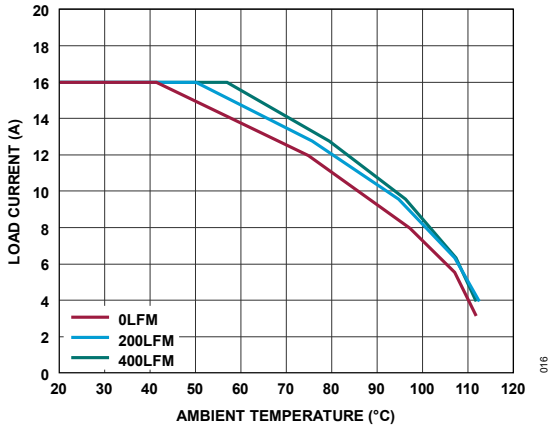


Figure 16. Derating Curve, V_{IN} = 5V, V_{OUT} = 3.3V, f_{SW} = 1MHz

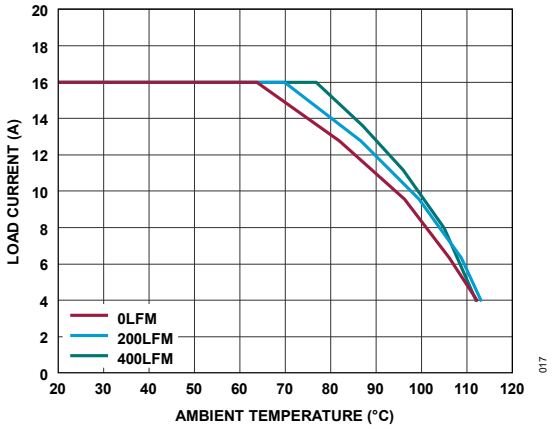


Figure 17. Derating Curve, V_{IN} = 12V, V_{OUT} = 1V, f_{SW} = 800kHz

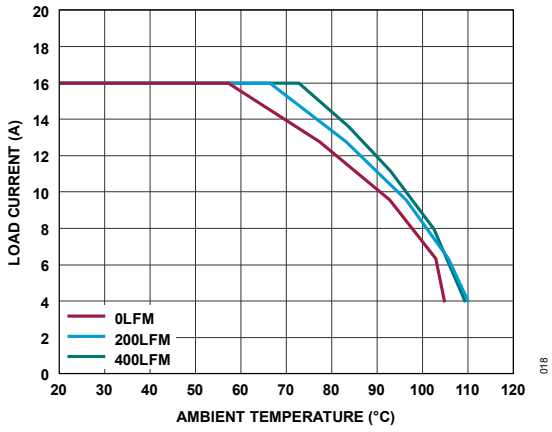


Figure 18. Derating Curve, V_{IN} = 12V, V_{OUT} = 1.5V, f_{SW} = 800kHz

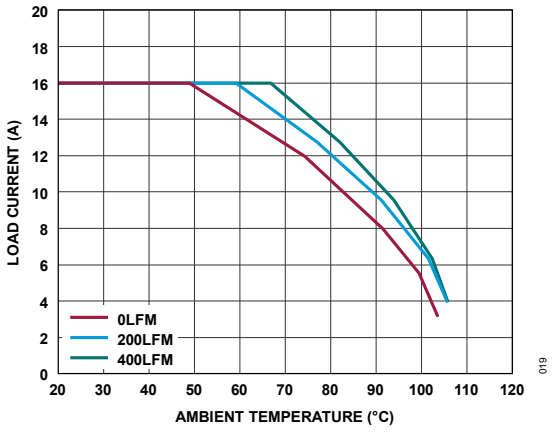


Figure 19. Derating Curve, V_{IN} = 12V, V_{OUT} = 2.5V, f_{SW} = 1MHz

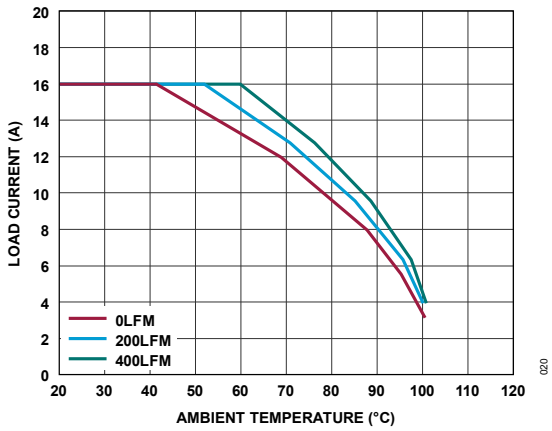


Figure 20. Derating Curve, V_{IN} = 12V, V_{OUT} = 3.3V, f_{SW} = 1MHz

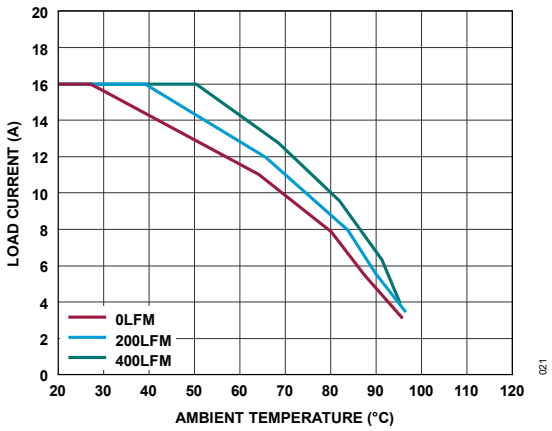


Figure 21. Derating Curve, V_{IN} = 12V, V_{OUT} = 5V, f_{SW} = 1MHz

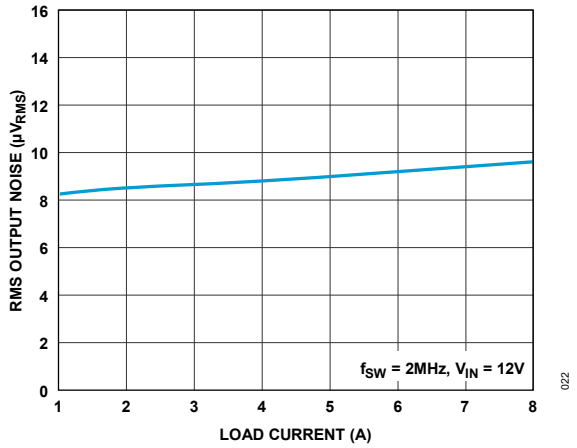


Figure 22. Integrated RMS Output Noise (10Hz to 100kHz) vs. Load

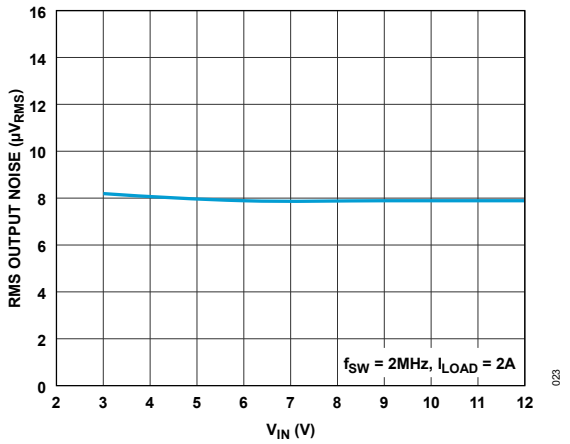


Figure 23. Integrated RMS Output Noise (10Hz to 100kHz) vs. V_{IN}

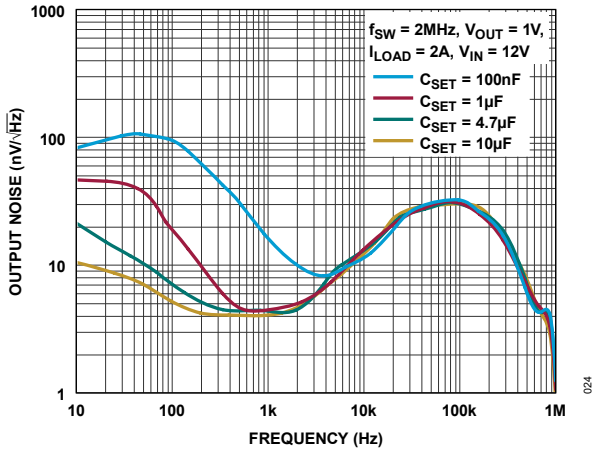


Figure 24. Noise Spectral Density vs. C_{SET}

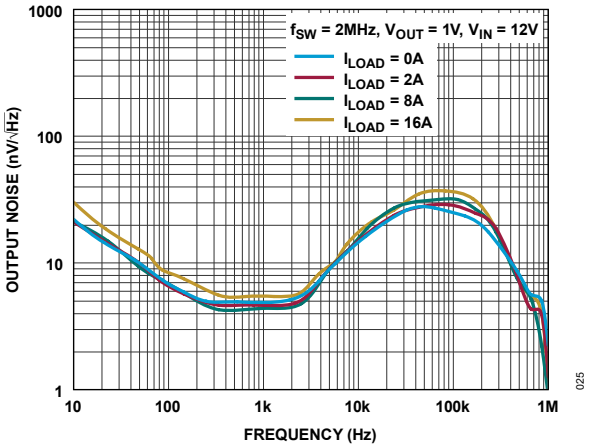


Figure 25. Noise Spectral Density vs. Load

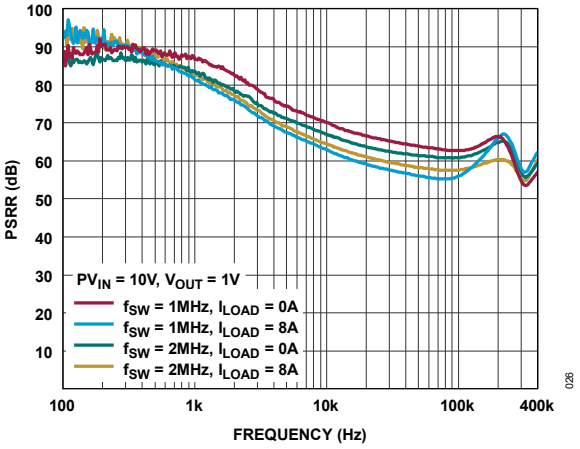
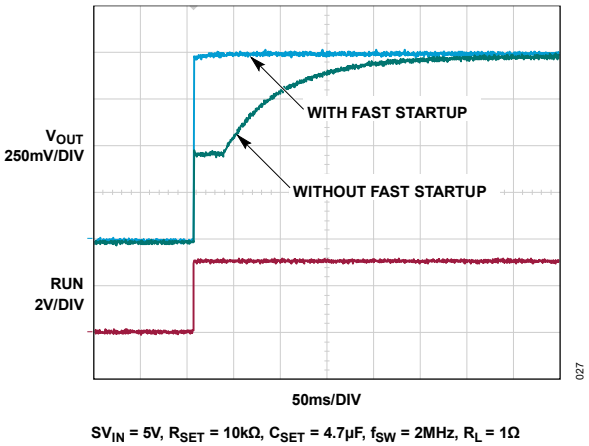
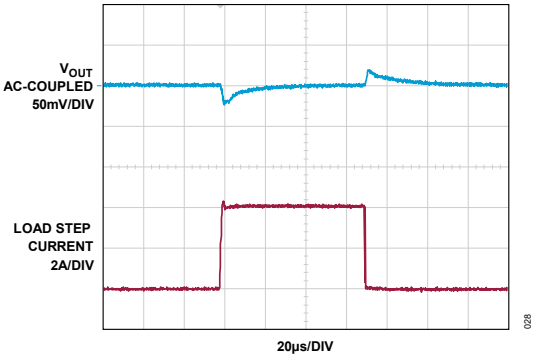


Figure 26. Power Supply Ripple Rejection



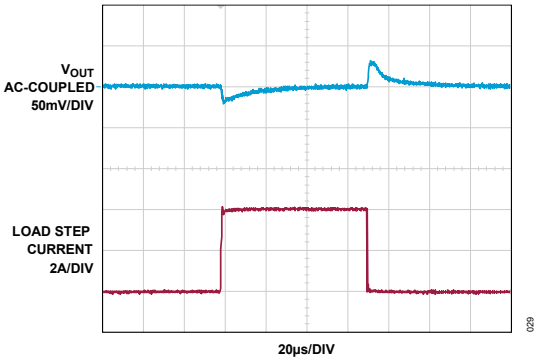
SV_{IN} = 5V, R_{SET} = 10kΩ, C_{SET} = 4.7µF, f_{SW} = 2MHz, R_L = 1Ω

Figure 27. Fast Startup Circuitry (Large C_{SET})



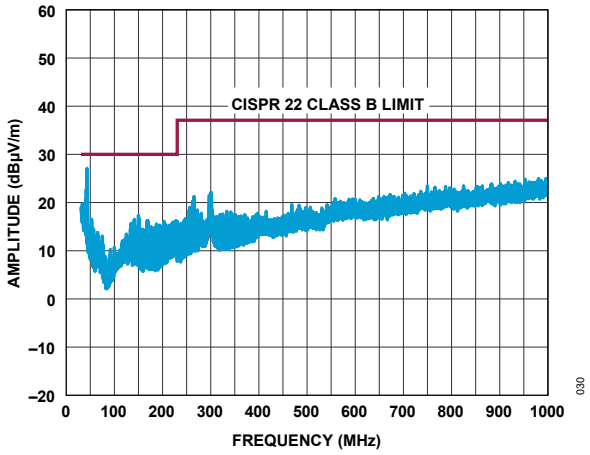
V_{IN} = 12V, V_{OUT} = 1V, I_{OUT} = 4A TO 8A, f_{SW} = 2MHz
C_{OUT} = 5 × 100µF CERAMIC CAPACITOR
INTERNAL COMPENSATION
CONNECT COMPa TO COMPb

Figure 28. 1V Output Transient Response



V_{IN} = 12V, V_{OUT} = 5V, I_{OUT} = 4A TO 8A, f_{SW} = 2MHz
C_{OUT} = 5 × 100µF CERAMIC CAPACITOR
INTERNAL COMPENSATION
CONNECT COMPa TO COMPb

Figure 29. 5V Output Transient Response



EVAL-LTM4707-AZ EVALUATION BOARD
WITH EMI FILTER
V_{IN} = 12V, V_{OUT} = 1V, I_{OUT} = 16A, f_{SW} = 800kHz

Figure 30. CISPR22 Class B Emissions

THEORY OF OPERATION

LTM4707 Overview

The LTM4707 is a standalone, non-isolated switching DC-to-DC power supply that can deliver up to 16A. The continuous current is determined by the internal operating temperature. It provides a precisely regulated output voltage programmable through one external resistor from 0.3V to 6V. The input voltage ranges between 3V to 16V. Given that the LTM4707 is a step-down converter, ensure that the input voltage is high enough to support the desired output voltage and load current. See *Figure 31* (Block Diagram) for more details.

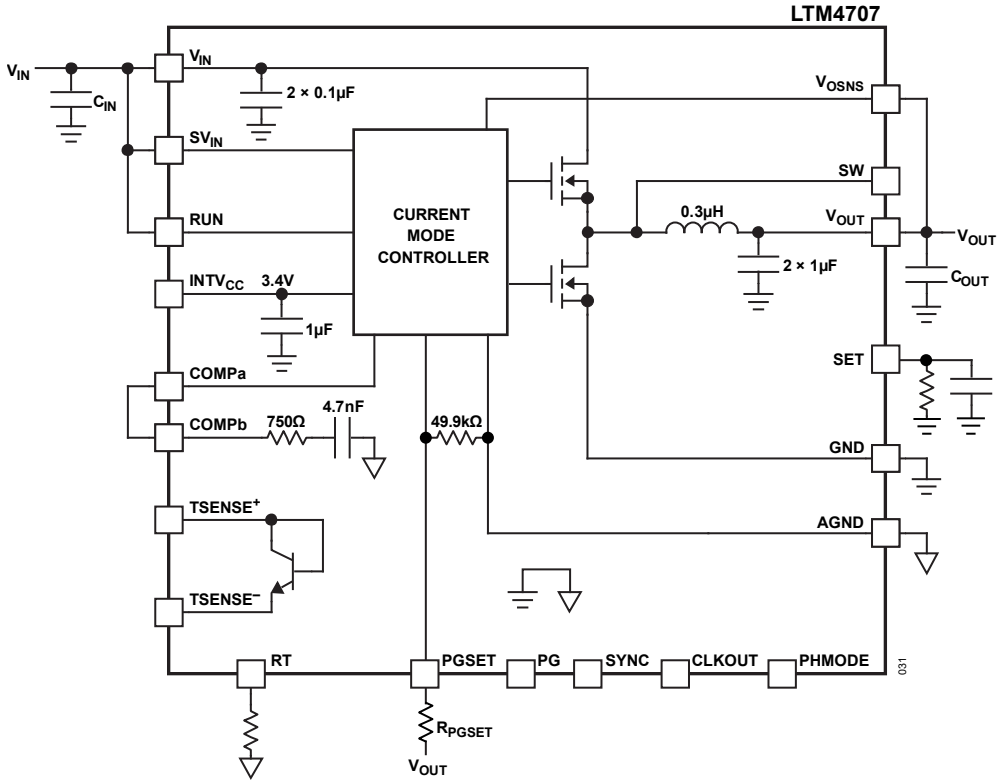


Figure 31. LTM4707 Block Diagram

The LTM4707 contains a current mode controller, power switching elements, a power inductor, and a modest amount of input and output capacitance. The LTM4707 is a fixed-frequency pulse-width modulation (PWM) regulator. The switching frequency is set by simply connecting a resistor from the RT pin to AGND.

An internal regulator provides power to the control circuitry. To improve efficiency across all loads, the SV_{IN} pin can be powered from an independent supply at a voltage lower than V_{IN}. If the RUN pin is below 0.4V, the LTM4707 shuts down and draws 50µA from the input. When the RUN pin rises above 1.32V (typical), the LTM4707 becomes active.

In applications where low output ripple and high efficiency at light load conditions are desired, pulse-skipping mode (PSM) should be used by connecting the SYNC pin to GND. At light loads, the internal current comparator may remain tripped for several cycles and forces the top MOSFET to stay off for several cycles, thus skipping cycles. The inductor current does not reverse in this mode.

In applications where fixed-frequency operation is more critical than low current efficiency, and where the lowest output ripple is desired, FCM operation should be used. The FCM operation can be enabled by connecting the SYNC pin to $INTV_{CC}$. In this mode, the inductor current is allowed to reverse during low output loads, the COMP voltage is

in control of the current comparator threshold throughout, and the top MOSFET always turns on with each oscillator pulse. During startup, FCM is disabled, and the inductor current is prevented from reversing until the LTM4707's output voltage is in regulation.

The LTM4707 incorporates fast startup circuitry, which allows the device to startup at a short time while using a larger value SET pin capacitor for ultralow noise applications. See the *Applications Information* section for more details.

The LTM4707 contains a power good comparator that trips when the PGSET pin is between 462.5mV and 537.5mV. The PG output is an open-drain transistor that is off when the output is in regulation, allowing an external resistor to pull the PG pin high. The PG signal is valid when SV_{IN} is above 3V. If SV_{IN} is above 3V and RUN is low, PG will remain low.

The LTM4707 is equipped with a thermal shutdown, which inhibits power switching at high junction temperatures. The activation threshold of this function is above 125°C to avoid interfering with normal operation, prolonged, or repetitive operation under a condition in which the thermal shutdown activates. This condition may damage or impair the reliability of the device.

Two or more LTM4707 ICs may be operated in parallel to produce higher currents. The COMPa and CLKOUT pins enable multiple LTM4707 to run out-of-phase, reducing the amount of required input and output capacitors. The PHMODE pin selects the phasing of CLKOUT for different multiphase applications. The COMPa pin allows the loop compensation of the LTM4707 to be optimized for a fast-transient response.

APPLICATIONS INFORMATION

For most applications, the design process is straightforward and summarized as follows.

1. See *Table 5* for the row with the desired input range and output voltage.
2. Apply the recommended C_{IN}, C_{OUT}, R_{SET}, and R_T values.
3. Apply the C_{SET} (from SET to GND).

While these component combinations have been tested for proper operation, the user must verify proper operation over the intended system's line, load, and environmental conditions. The maximum output current is limited by the junction temperature, the relationship between the input and output voltage magnitude and polarity, and other factors. See the graphs in the *Typical Performance Characteristics* section for guidance.

The maximum frequency (and attendant R_T value) at which the LTM4707 should be allowed to switch is given in *Table 5* in the Maximum f_{SW} column, while the recommended frequency (and R_T value) for optimal efficiency over the given input condition is given in the f_{SW} column. There are additional conditions that must be satisfied if the synchronization function is used. See the *Synchronization* section for more details.

Capacitor Selection Considerations

The C_{IN} and C_{OUT} capacitor values in *Table 5* are the minimum recommended values for the associated operating conditions. Applying capacitor values below those indicated in *Table 5* is not recommended and may result in undesirable operation. Using a larger value is generally acceptable, and can yield improved dynamic response, if necessary. Again, the user must verify proper operation over the intended system's line, load, and environmental conditions.

Ceramic capacitors are small, robust and have low ESR. However, not all ceramic capacitors are suitable. The X5R and X7R types are stable over temperature and applied voltage and give dependable service. Other types, including Y5V and Z5U have large temperature and voltage coefficients of capacitance. In an application circuit, these capacitors may have only a small fraction of their nominal capacitance, resulting in a much higher output voltage ripple than expected.

Ceramic capacitors are also piezoelectric. Since the LTM4707 operates at a lower current limit during PSM operation, the noise is typically very quiet to a casual ear. If this audible noise is unacceptable, use a high-performance electrolytic capacitor at the output. It may also be a parallel combination of a ceramic capacitor and a low-cost electrolytic capacitor.

A final precaution regarding ceramic capacitors concerns the maximum input voltage rating of the LTM4707. A ceramic input capacitor combined with trace or cable inductance forms a high-Q (underdamped) tank circuit. If the LTM4707 circuit is plugged into a live supply, the input voltage can ring to twice its nominal value, possibly exceeding the device's rating. This situation can be avoided easily (see the *Hot-Plugging Safely* section for more details).

Table 5. Recommended Component Values and Configuration (T_A = 25°C)

V_{IN}[1] (V)	V_{OUT} (V)	R_{SET} (kΩ)	C_{IN}[2]	C_{OUT}	f_{SW} (kHz)	R_T (kΩ)	MAX f_{SW} (kHz)	MIN R_T (kΩ)
3 to 16	1	10	2 × 10µF X7R 25V	5 × 100µF X7R 6.3V	800	137	2500	35.7
3.3 to 16	1.5	15	2 × 10µF X7R 25V	5 × 100µF X7R 6.3V	800	137	2500	35.7
3.9 to 16	2.5	24.9	2 × 10µF X7R 25V	5 × 100µF X7R 6.3V	1000	105	2500	35.7
4.5 to 16	3.3	33.2	2 × 10µF X7R 25V	5 × 100µF X7R 6.3V	1000	105	2500	35.7
9 to 16	5	49.9	2 × 10µF X7R 25V	5 × 100µF X7R 10V	1000	105	3000	28.7

[1] The LTM4707 may be capable to operate at a lower input voltage, but it may skip switching cycles.
[2] A bulk capacitor is required.

Frequency Selection

The LTM4707 uses a constant-frequency PWM architecture, which can be programmed to switch from 300kHz to 3MHz by using a resistor connected from the RT pin to the ground. *Table 6* provides a list of R_T resistor values and their resultant frequencies.

Table 6. Switching Frequency vs. R_T Value

f_{SW} (MHz)	R_T (kΩ)
0.3	392
0.4	287
0.5	226
0.6	187
0.7	154
0.8	137
0.9	118
1.0	105
1.2	86.6
1.4	71.5
1.6	61.9
1.8	53.6
2	47
2.5	35.7
3	28.7

Operating Frequency Trade-Offs

It is recommended that the user apply the optimal R_T value given in *Table 6* for the input and output operating conditions. System-level operation or other considerations, however, may necessitate another operating frequency. While the LTM4707 is flexible enough to accommodate a wide range of operating frequencies, a haphazardly chosen one may result in undesirable operation under certain operating or fault conditions. A frequency that is too high can reduce efficiency, generate excessive heat, or even damage the LTM4707 if the output is overloaded or short-circuited. A frequency that is too low can result in a final design that has too much output ripple or too large of an output capacitor.

Maximum Load

The maximum practical continuous load that the LTM4707 can drive, while rated at 16A, depends upon both the internal current limit and the internal temperature. The internal current limit is designed to prevent damage to the LTM4707 in the case of an overload or a short-circuit. The internal temperature of the LTM4707 depends upon operating conditions such as the ambient temperature, the power delivered, and the heat-sinking capability of the system. For example, if the LTM4707 is configured to regulate at 1V, it may continuously deliver 16A from $12V_{IN}$ if the ambient temperature is controlled to less than 73°C. See the $12V_{IN}$ and $1V_{OUT}$ derating curves in the *Typical Performance Characteristics* section. Similarly, if the output voltage is 5V and the ambient temperature is 85°C, the LTM4707 delivers at most 5.5A from $12V_{IN}$, which is less than the 16A continuous rating.

Load Sharing

Two or more LTM4707 ICs may be paralleled to produce higher currents. To do this, connect the V_{IN}, V_{OUT}, V_{OSNS}, COMPa, and COMPb pins of all the paralleled LTM4707 ICs together. An example of two LTM4707 ICs configured for load sharing is given in *Figure 41* in the *Applications Information* section.

The CLKOUT signal can be connected to the SYNC pin of the following LTM4707 to line up both the frequency and the phase of the entire system. Connecting the PHMODE pin to GND, $INTV_{CC}$, or floating the pin generates a phase difference between LTM4707's internal clock and CLKOUT of 180°, 90°, or 120°, respectively, which corresponds to a 2-phase, 4-phase, or 3-phase operation. A total of 12 phases can be paralleled to run simultaneously out-of-phase with respect to each other by programming the PHMODE pin of each LTM4707 to different voltage levels. *Figure 32* shows a 4-phase application where four LTM4707 ICs are paralleled to get one output capable up to 64A. During FCM and synchronization mode, all devices will operate at the same frequency. When load sharing among a number (n) of units and using a single R_{SET} resistor, the value of the resistor is given by Equation *2*.

$$R_{SET} = \frac{V_{OUT}}{n \times 100\mu A} \quad (2)$$

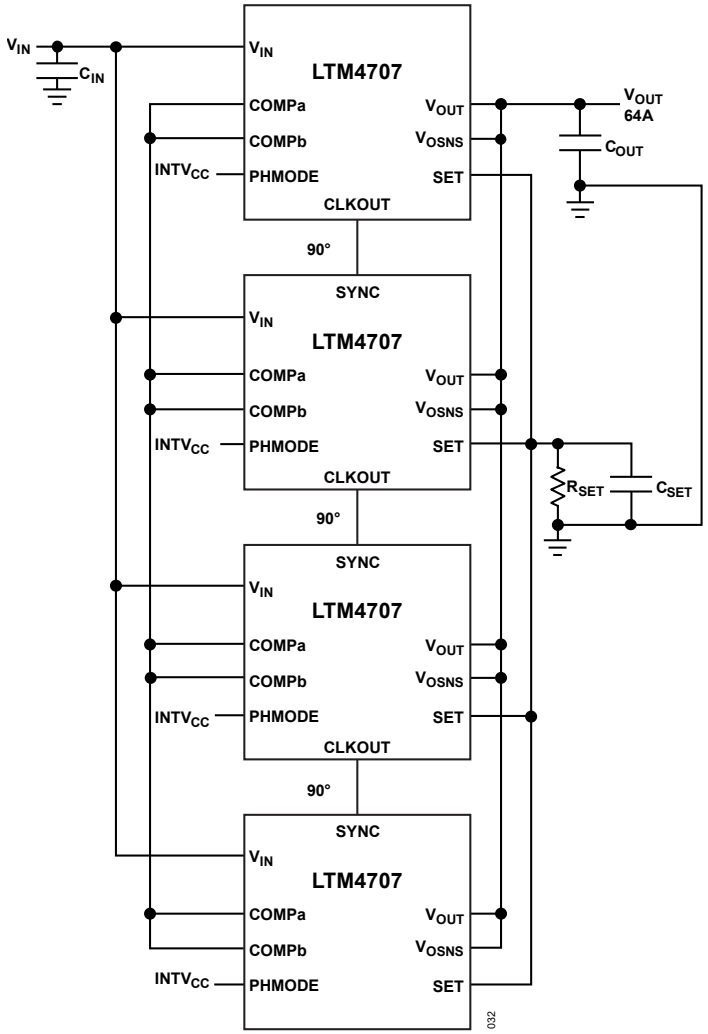


Figure 32. Paralleling Four LTM4707 ICs

Minimum Input Voltage

The LTM4707 is a step-down converter, a minimum amount of headroom is required to keep the output in regulation. Keep V_{IN} above 3V to ensure proper operation. If the SV_{IN} and V_{IN} pins are powered from different sources, keep SV_{IN} above 4V to maintain $INTV_{CC}$ = 3.4V and ensure optimum regulation. The voltage transients or ripple valleys that cause the SV_{IN} to fall below 3V may turn off the LTM4707.

SET Pin (Bypass) Capacitance: Noise, Transient Response, and Soft Start

In addition to reducing output noise, using a SET pin bypass capacitor will reduce sensitivity to any parasitic coupling of voltage spikes onto the SET pin. Note that any bypass capacitor leakage deteriorates the LTM4707 DC regulation. Capacitor leakage of even 100nA is a 0.1% DC error. Therefore, it is recommended that a good quality, low leakage ceramic capacitor be used.

Using a SET pin bypass capacitor also soft starts the output and limits inrush current. Soft starting the output prevents a current surge on the input supply. The SET pin capacitor and the resistor values set the ramp-up time of the reference voltage, and the output voltage will track this voltage. The SET pin resistance is determined by the application's desired output voltage; however, the capacitance may be selected to achieve the desired ramp-up time.

Without fast startup enabled, the RC time constant, formed by the SET pin resistor and capacitor, controls soft start time. Connect the PGSET pin to 0.5V to disable fast startup. The ramp-up rate from 0% to 90% of nominal V_{OUT} is given by Equation *3*.

$$t_{START\_NO\_FAST\_STARTUP} = 2.3 \times R_{SET} \times C_{SET} \qquad (3)$$

With fast startup enabled, the startup time can be significantly reduced with the ramp-up time from 0% to 90% of nominal V_{OUT} is given by Equation *4*.

$$t_{START\_NO\_FAST\_STARTUP} = \frac{100\mu A \times R_{SET} \times C_{SET}}{2.7mA} \qquad (4)$$

In most applications, fast startup is enabled, in which case a minimum 1µF SET capacitor is recommended for preventing reference voltage overcharge and ensuring good noise performance.

Soft Start and Power Sequencing

As discussed in the *SET Pin (Bypass) Capacitance: Noise, Transient Response, and Soft Start* section, soft start is achieved through the controlled ramp-up time of the SET pin voltage. The soft start is guaranteed when V_{IN} and SV_{IN} are connected.

When V_{IN} and SV_{IN} are powered by independent supplies, power sequencing must be considered to guarantee soft start. The SET pin voltage should start at 0V when V_{IN} is applied. To guarantee a soft start, do not power V_{IN} last when sequencing V_{IN}, SV_{IN}, and RUN pins. An example of a specific case to avoid is having SV_{IN} and RUN powered up before V_{IN}; in this instance, the SET pin voltage will have risen to some voltage greater than 0V when V_{IN} is applied, and the LTM4707 will not soft start properly.

Fast Startup

For ultralow noise applications which require low 1/f noise (i.e., at frequencies below 100Hz), a larger value SET pin capacitor is required, up to 22µF. A larger value capacitor can be used, but care should be taken regarding leakage. While normally larger capacitors would significantly increase the regulator's startup time, the LTM4707 incorporates fast startup circuitry, which increases the SET pin current to about 2.7mA during startup.

Upon startup, the 2.7mA current source remains engaged while PGSET is below the power good threshold of 462.5mV, unless the regulator is in thermal shutdown, SV_{IN} is too low, or $INTV_{CC}$ has fallen too low.

The fast startup circuit is disabled permanently once PGSET rises above the power good threshold, until either the part is powered down, or the part is placed into shut down by pulling the RUN pin to GND.

There is one more condition under which the 2.7mA current source is disabled during startup. The purpose of this is to prevent overcharging V_{SET}. Since the LTM4707 assumes that the PGSET pin is an accurate indication of the voltage on the SET pin, it assumes that V_{OSNS} follows V_{SET} closely. However, this may not always be the case—for example, if the output capacitance is very large, or if for some reason the output is shorted to GND. Therefore, fast charge is also disabled whenever the COMPa pin has railed at its maximum value (when V_{SET} has risen significantly above V_{OSNS}). This prevents incorrect behavior where the 2.7mA current sources stay on even if V_{SET} has risen above its intended value.

This means that there is also a minimum SET capacitor requirement for using fast startup without overcharging the reference voltage. This will depend on the compensation network, as the part depends on the COMPa pin voltage rising to its maximum value to inform the part to pause fast charge.

The recommended minimum SET capacitance value to prevent overcharging the reference voltage is given by Equation 5.

$$MIN\ C_{SET} = 27 \times \frac{C_{COMP}}{V_{SET}} \qquad (5)$$

If programmable power good and fast startup capabilities are not required, the PGSET pin must be connected to 0.5V. This 0.5V could be an external voltage reference for PGSET. *Figure 40* circuit shows an example.

Forced Continuous Mode

The LTM4707 can operate in FCM for fast transient response and full frequency operation over a wide load range. When in FCM, the oscillator operates continuously, and positive SW pin transitions are aligned to the clock. A negative inductor current is allowed at light loads or under large transient conditions. The FCM improves load step transient response (see *Figure 33*). At light loads, FCM operation is less efficient than PSM operation but may be desirable in applications where it is necessary to keep switching harmonics out of the signal band. The FCM must be used if the output is required to sink current. To enable FCM, connect the SYNC pin to $INTV_{CC}$ or greater than 3V, or float the pin.

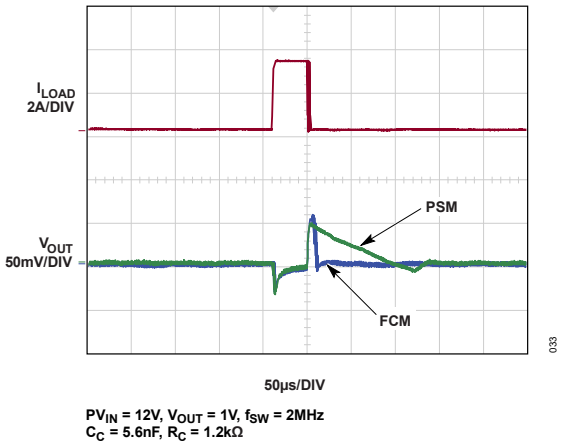


Figure 33. 0.1A to 3.1A Load Step Transient Response with and without FCM

The FCM is disabled under V_{IN} overvoltage conditions (V_{IN} pin is held above 18V), if V_{OUT} is too high (the PGSET pin is held greater than 537.5mV) and is also disabled during startup until the voltage on V_{OUT} has charged up to 92.5% of its final value (as indicated when the PGSET pin rises to above 462.5mV). For the latter two conditions, it is assumed the PGSET pin is connected to the output voltage through an appropriate resistor. When FCM is disabled in these ways, the negative inductor current is not allowed, and the LTM4707 operates in PSM.

Pulse-Skipping Mode

When not operating in FCM, the LTM4707 will operate in PSM. The negative inductor current is not allowed in this mode. Additionally, in PSM, the LTM4707 may also skip switching cycles at very light loads for improved efficiency, or at very high duty cycles to achieve better dropout. To enable PSM, connect the SYNC pin to GND.

Synchronization

To synchronize the LTM4707 oscillator to an external frequency, connect a square wave to the SYNC pin. The square wave amplitude should have valleys, which are below 0.4V, and peaks above 1.5V (up to 6V), with a minimum on-time and off-time of 50ns.

The LTM4707 will run FCM to maintain regulation while synchronized to an external clock. The LTM4707 may be synchronized over a 300kHz to 3MHz range. The R_T resistor should be chosen to set the LTM4707 switching frequency to below the lowest synchronization input by approximately 20%. For example, if the synchronization signal is 500kHz and higher, the R_T resistor should be selected for 400kHz.

Programmable Power Good

The LTM4707 features a programmable power good by using a single resistor across OUT pin and PGSET pin (Equation 6).

$$V_{OUT(PG\_THRESHOLD)} = 0.5 \times \left(1 + \frac{R_{PGSET}}{49.9k\Omega}\right) + I_{PGSET} \times R_{PGSET} \qquad (6)$$

If the PGSET pin increases above 537.5mV or decreases below 462.5mV, the open-drain PG pin de-asserts and becomes low impedance. The power good comparator has 5mV hysteresis. The PGSET pin current (I_{PGSET}) from the *Electrical Characteristics* table must be considered when determining the resistor. Note that the programmable power good and fast startup capabilities are disabled when PGSET is connected to 0.5V or when the device is in shutdown. *Table 7* suggests some 1% R_{PGSET} resistor values for common V_{OUT} configurations.

Table 7. Suggested R_{PGSET} Resistor Values

V_{OUT} (V)	R_{PGSET} (kΩ)
0.8	30.1
0.9	40.2
1	49.9
1.2	69.8
1.5	100
1.8	130
2.5	200
3.3	280
5	453

Shorted or Reversed Input Protection

Care needs to be taken in systems where the output is held high when the power input to the LTM4707 is absent. This may occur in battery charging applications or in battery backup systems where a battery or some other supply is diode OR-ed with the LTM4707's output. If the V_{IN} pin is allowed to float and the RUN pin is held high (either by a logic signal or because it is connected to V_{IN}), then the LTM4707's internal circuitry pulls its quiescent current through its internal power switch. This is fine if your system tolerates a few milliamps in this state. If the RUN pin is grounded, the internal current drops to essentially zero. However, if the V_{IN} pin is grounded while the output is held high, parasitic diodes inside the LTM4707 pull large currents from the output through the V_{IN} pin. *Figure 34* shows a connection of V_{IN} and RUN pins, which allow LTM4707 to run only when the input voltage is present and protects against a shorted or reversed input.

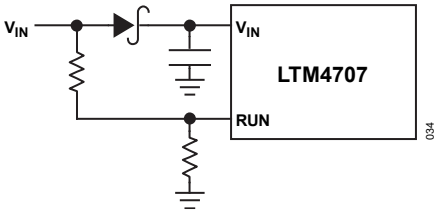


Figure 34.Reverse Input Protection

Temperature Monitoring

Measuring the absolute temperature of a diode is possible due to the relationship between current, voltage, and temperature described by the classic diode Equation *7*.

$$I_D = I_S \times e\left(\frac{V_D}{\eta \times V_T}\right) \; or \; V_D = \eta \times V_T \times In\frac{I_D}{I_S} \qquad (7)$$

where I_D is the diode current, V_D is the diode voltage, η is the ideal factor (typically close to 1.0), and I_S (saturation current) is a process dependent parameter. V_T can be broken out by Equation *8*.

$$V_T = \frac{k \times T}{q} \qquad (8)$$

where T is the diode junction temperature in Kelvin, q is the electron charge, and k is the Boltzmann's constant. The V_T is approximately 26mV at room temperature (298K) and scales linearly with Kelvin temperature. It is this linear temperature relationship that makes diodes suitable temperature sensors. The I_S term in the Equation *8* is the extrapolated current through a diode junction when the diode has zero volts across the terminals. The I_S term varies from process to process, varies with temperature, and it must always be less than I_D. Equation *9* combines all the constants into one term.

$$K_D = \frac{\eta \times T}{q} \qquad (9)$$

where $K_D = 8.26^{-5}$ and knowing that $In \times I_D/I_S$ is always positive because I_D is always greater than I_S, leaves us with Equation *10*.

$$V_D = T_{(KELVIN)} \times K_D \times In\frac{I_D}{I_S} \qquad (10)$$

where V_D appears to increase with temperature. It is common knowledge that a silicon diode biased with a current source has an approximate –2mV/°C temperature relationship (*Figure 35*), which is at odds with the Equation *10*. In fact, the I_S term increases with temperature, reducing the absolute value yielding an approximate –2mV/°C composite diode voltage slope.

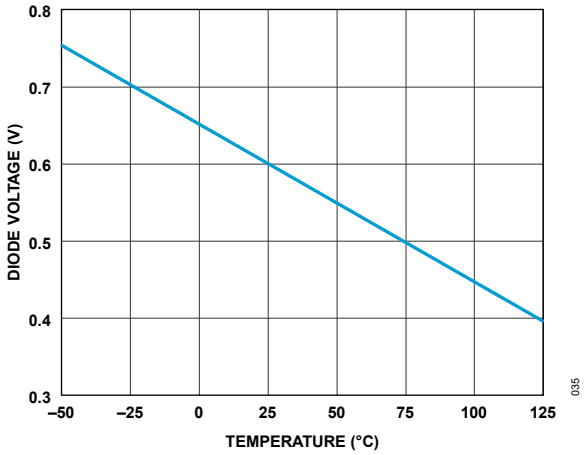


Figure 35. Diode Voltage V_D vs. Temperature

To obtain a linear voltage proportional to temperature, we cancel the I_S variable in the natural logarithm term to remove the I_S dependency from Equation 9. This is accomplished by measuring the diode voltage at two currents I_1, and I_2, where $I_1 = 10 \times I_2$) and subtracting, we get Equation 11.

$$\Delta V_D = T_{(KELVIN)} \times K_D \times In\frac{I_1}{I_S} T_{(KELVIN)} \times K_D \times In\frac{I_2}{I_S} \quad (11)$$

Combining like terms and then simplifying the natural log terms yields Equation 12.

$$\Delta V_D = T_{(KELVIN)} \times K_D \times In \times 10 \quad (12)$$

and redefining the constant given by Equation 13.

$$K_D' = K_D \times In \times 10 = \frac{198\mu V}{K} \quad (13)$$

yields Equation 14.

$$\Delta V_D = K_D \times T_{(KELVIN)} \quad (14)$$

Use Equation 15 for solving for temperature.

$$T_{(KELVIN)} = \frac{\Delta V_D}{K_D'}(CELSIUS) = T_{(KELVIN)} - 273.15 \quad (15)$$

Where, 300°K = 27°C, means that is we take the difference in voltage across the diode measured at two currents with a ratio of 10, the resulting voltage is 198µV per Kelvin of the junction with a zero intercept at 0 Kelvin.

The diode connected NPN transistor across the T_{SENSE}^+ and T_{SENSE}^- pins can be used to monitor the internal temperature of the LTM4707.

Hot-Plugging Safely

The small size, robustness, and low impedance of ceramic capacitors make them an attractive option for the input bypass capacitor of LTM4707. However, these capacitors cause problems if the LTM4707 is plugged into a live supply (Refer to the Analog Devices *Application Note 88* for a complete discussion). The low loss ceramic capacitor combined with stray inductance in series with the power source forms an underdamped tank circuit, and the voltage at the V_{IN} pins of the LTM4707 rings to more than twice the nominal input voltage, possibly exceeding the LTM4707's rating and damaging the part. If the input supply is poorly controlled or the LTM4707 is hot-plugged into

an energized supply, the input network should be designed to prevent this overshoot. This can be accomplished by installing a small resistor in series to V_{IN}, but the most popular method of controlling input voltage overshoot is adding an electrolytic bulk cap to the V_{IN} net. This capacitor's relatively high equivalent series resistance damps the circuit and eliminates the voltage overshoot. The extra capacitor improves low-frequency ripple filtering and slightly improves the efficiency of the circuit, though it is likely to be the largest component in the circuit.

Figure 36 shows a temperature plot of the LTM4707 with 12V input, 1V output at 16A without a heat sink, and a no airflow condition.

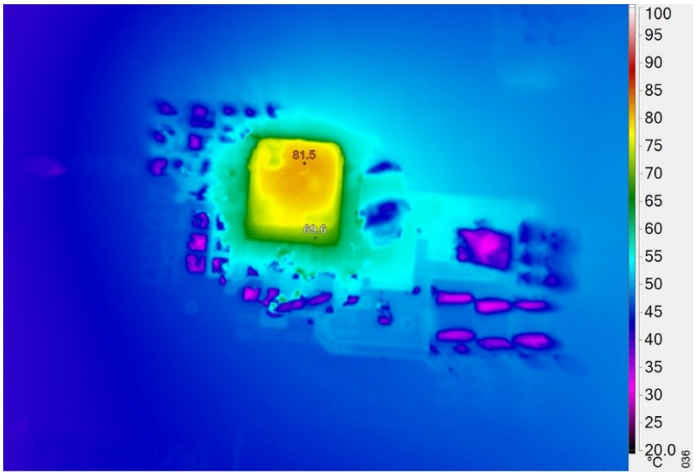


Figure 36. Thermal Image at 12V_{IN}, 1V, 16A Output, No Airflow and Heat Sink

Thermal Considerations

The LTM4707 output current may need to be derated if it is required to operate in a high ambient temperature. The amount of current derating is dependent upon the input voltage, output power, and ambient temperature. The derating curves given in the *Typical Performance Characteristics* section can be used as a guide. These curves were generated by the LTM4707 mounted to a 50cm2 6-layer FR4 PCB. Boards of other sizes and layer counts can exhibit different thermal behavior. The user must verify proper operation over the intended system's line, load, and environmental operating conditions.

For increased accuracy and fidelity to the actual application, many designers use finite element analysis (FEA) to predict thermal performance. Therefore, the following are the thermal coefficients.

1. θ_{JA} – Thermal resistance from the junction to ambient.
2. θ_{JCbot} – Thermal resistance from the junction to the bottom of the product case.
3. θ_{JCtop} – Thermal resistance from the junction to the top of the product case.

While the meaning of each of these coefficients may seem to be intuitive, JEDEC has defined each to avoid confusion and inconsistency. These definitions are given in JESD5112 and are paraphrased as follows.

1. θ_{JA} is the natural convection junction-to-ambient air thermal resistance measured in a one cubic foot sealed enclosure. This environment is sometimes referred to as "still air", although natural convection causes the air to move. This value is determined with the part mounted to a JESD519 defined test board, which does not reflect an actual application or viable operating condition.
2. θ_{JCbot} is the junction-to-board thermal resistance with all the component power dissipation flowing through the bottom of the package. In the typical µModule regulator, the bulk of the heat flows out the bottom of the package, but there is always heat flow out into the ambient environment. As a result, this thermal resistance

value may be useful for comparing packages, but the test conditions do not generally match the user's application.

3. θ_{JCtop} is determined with nearly all the component power dissipation flowing through the top of the package. As the electrical connections of the typical µModule regulator are on the bottom of the package, it is rare for an application to operate such that most of the heat flows from the junction to the top of the part. As in the case of θ_{JCbot}, this value may be useful for comparing packages, but the test conditions do not generally match the user's application.

Given these definitions, it should now be apparent that none of these thermal coefficients reflects an actual physical operating condition of a µModule regulator. Thus, none of them can be individually used to accurately predict the thermal performance of the product. Likewise, it would be inappropriate to attempt to use any one coefficient to correlate to the junction temperature vs. load graphs given in this data sheet. The only appropriate way to use the coefficients is when running a detailed thermal analysis, such as FEA, which considers all the thermal resistances simultaneously.

A graphical representation of these thermal resistances is given in *Figure 37*. Some thermal resistance elements, such as heat flow out the side of the package, are not defined by the JEDEC standard, and are not shown. The blue resistances are contained within the µModule regulator, and the green is outside.

The die temperature of the LTM4707 must be lower than the maximum rating, care should be taken in the layout of the circuit to ensure good heat sinking of the LTM4707. The bulk of the heat flow out of the LTM4707 is through the bottom of the package and the pads into the PCB. Consequently, a poor PCB design can cause excessive heating, resulting in impaired performance or reliability. See the PCB Layout section for PCB design suggestions.

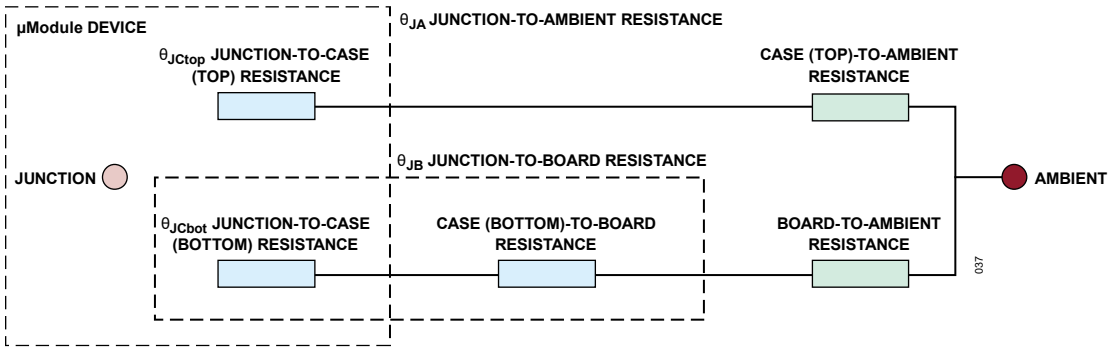


Figure 37. Graphical Representation of Thermal Coefficients, Including JESD5112 Terms

PCB Layout

Most of the headaches associated with the PCB layout have been alleviated or even eliminated by the high level of integration of the LTM4707. The LTM4707 is nevertheless a switching power supply, and care must be taken to minimize EMI and ensure proper operation. Even with a high level of integration, users may fail to achieve specified operations with a haphazard or poor layout. See *Figure 38* for a suggested layout. Ensure that the grounding and heat sinking are acceptable.

Keep in mind the following rules.

1. Place C_{SET}, R_{SET}, and R_T as close as possible to their respective pins.
2. Place the C_{IN} capacitor as close as possible to the V_{IN}/SV_{IN} and GND connection of the LTM4707.
3. Place the C_{OUT} capacitor as close as possible to the V_{OUT} and GND connection of the LTM4707.
4. Place the C_{IN} and C_{OUT} capacitors such that their ground current flows directly adjacent to or underneath the LTM4707.

5. Connect all the GND connections to as large a copper pour or plane area as possible on the top layer. Avoid breaking the ground connection between the external components and the LTM4707.
6. Use vias to connect the GND copper area to the board's internal ground planes. Liberally distribute these GND vias to provide both a good ground connection and a thermal path to the internal planes of the PCB. Pay attention to the location and density of the thermal vias in *Figure 38*. The LTM4707 benefits from the heat sinking afforded by vias which connect to internal GND planes at these locations, due to their proximity to internal power handling components. The optimum number of thermal vias depends upon the PCB design. For example, a board might use small via holes. It should employ more thermal vias than a board, which uses larger holes.

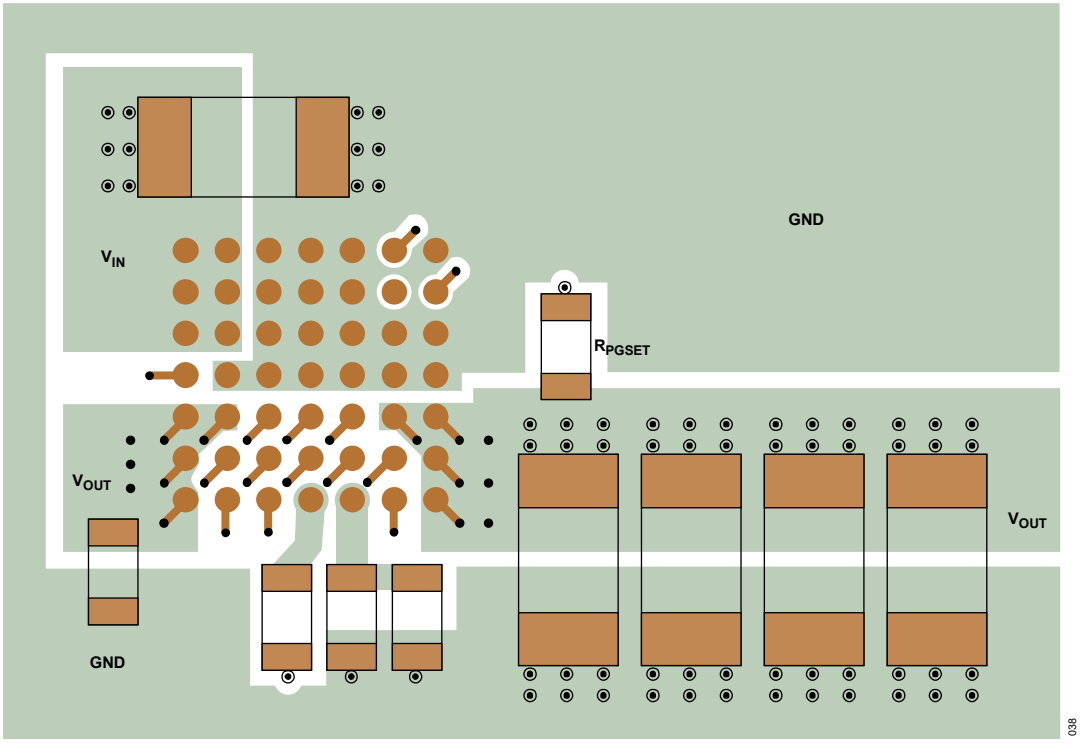
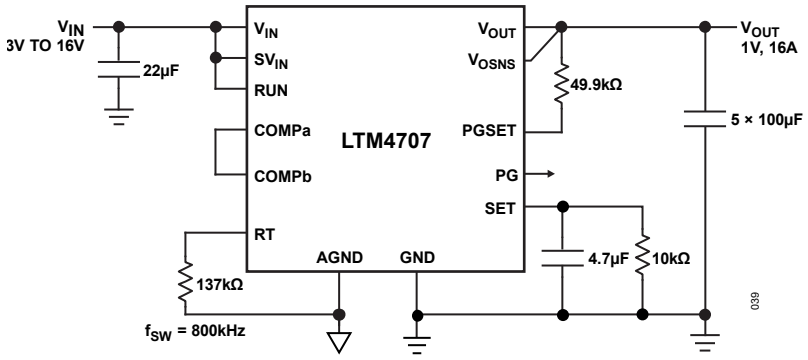


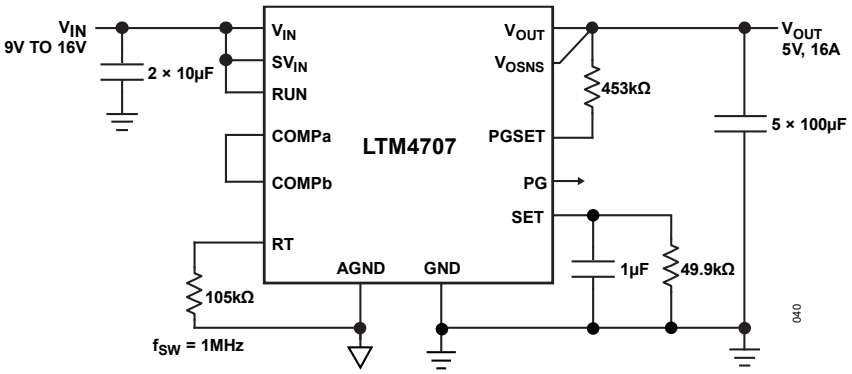
Figure 38. Layout showing suggested External Components, GND Plane and Thermal Vias (Top Layer)

TYPICAL APPLICATIONS



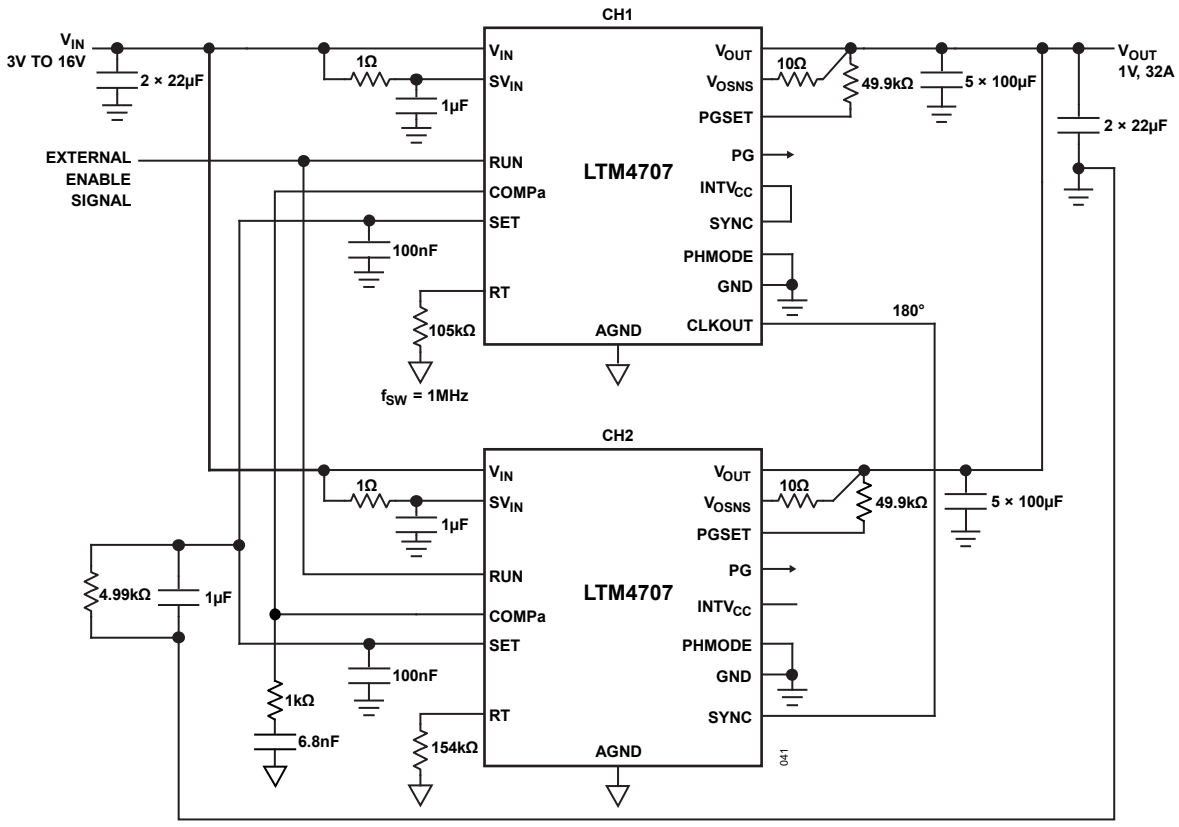
PINS NOT USED: SW, SYNC, PHMODE, CLKOUT, $INTV_{CC}$, T_{SENSE}^+, T_{SENSE}^-.
TO GUARANTEE SOFT START, DO NOT POWER V_{IN} LAST WHEN SEQUENCING V_{IN}, SV_{IN}, AND RUN.

Figure 39. 1V, 16A from 3V to 16V_{IN}, 800kHz with Soft Start, Fast Startup, and Power Good



PINS NOT USED: SW, SYNC, PHMODE, CLKOUT, $INTV_{CC}$, T_{SENSE}^+, AND T_{SENSE}^-.

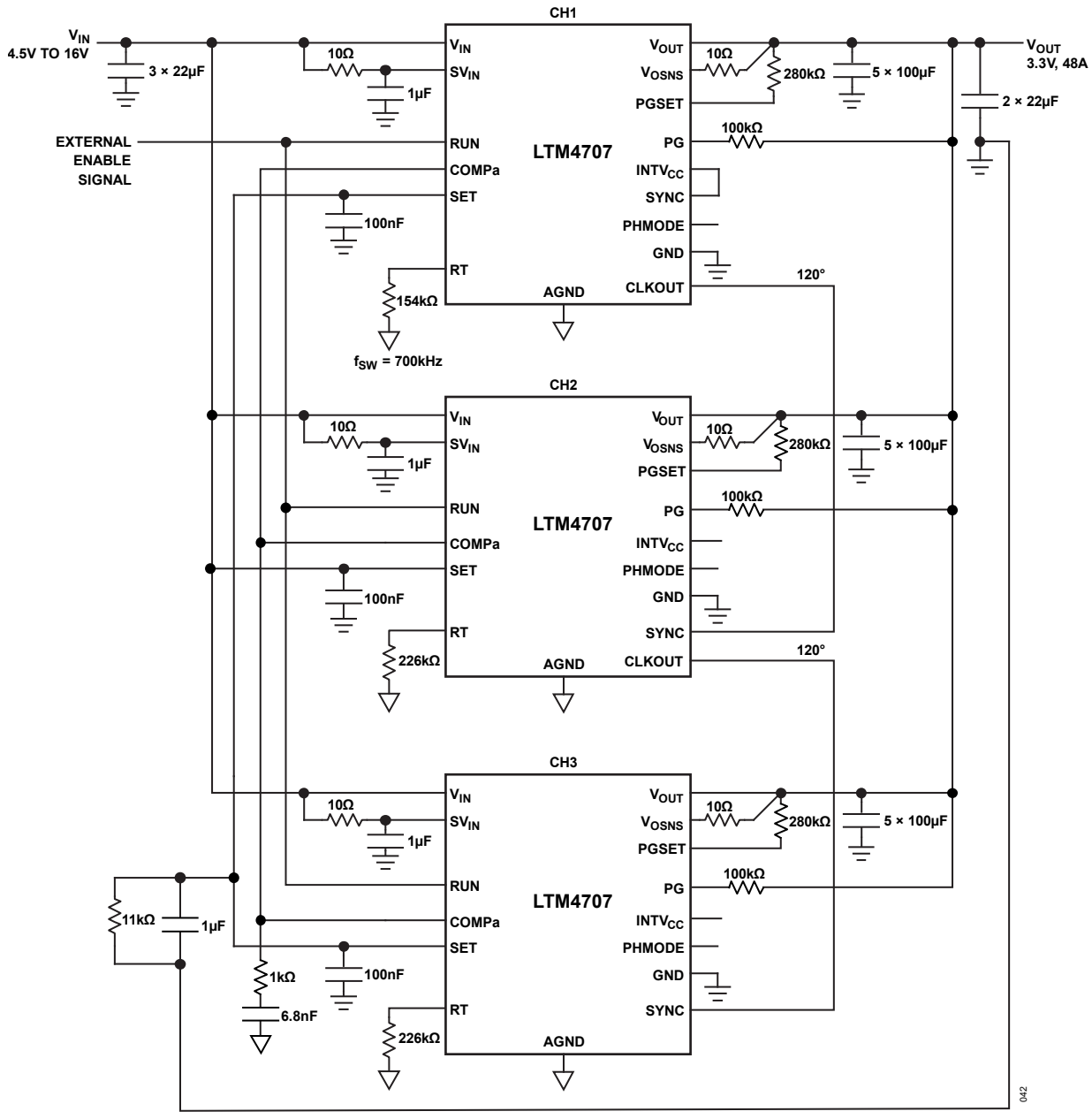
Figure 40. 5V, 16A from 9V to 16V_{IN}, 1MHz with Soft Start, Fast Startup, and Power Good



PINS NOT USED: COMPb, SW, T_{SENSE}^+, AND T_{SENSE}^-.

CH2 IS SYNCHRONIZED TO 1MHz THROUGH THE SYNC PIN. THE R_T RESISTOR VALUE MUST SET INTERNAL OSCILLATOR TO <800kHz (80% OF 1MHz).
THE COMPa PINS ARE CONNECTED TOGETHER.
THE PHMODE PIN IS CONNECTED TO GND FOR 180°. PHASE SHIFT AT CLKOUT.
THE SET PINS CAN BE CONNECTED TOGETHER FOR 200µA CURRENT REFERENCE; THIS PROVIDES LOWER 1/f NOISE AND BETTER CURRENT SHARING.

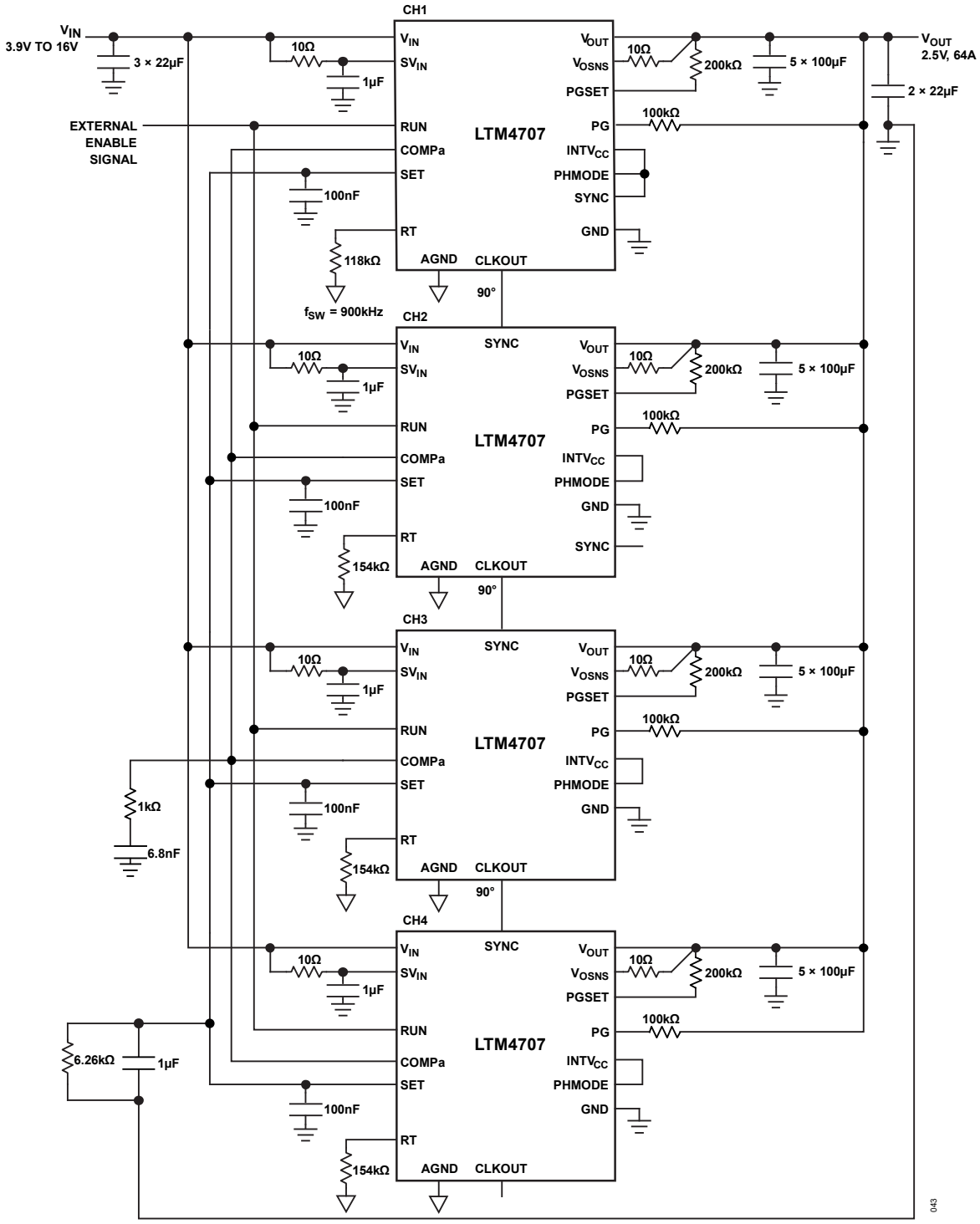
Figure 41. 2-Phase 1V, 32A from 3V to 16V_{IN}, 1MHz with Soft Start, Fast Startup, and Power Good



PINS NOT USED: COMPb, SW, T_{SENSE}^{+}, AND T_{SENSE}^{-}.

CH2 AND CH3 ARE SYNCHRONIZED TO 700kHz THROUGH THE SYNC PIN. THE R_T RESISTOR VALUE MUST SET INTERNAL OSCILLATOR TO <560kHz (80% OF 700kHz).
THE COMPa PINS ARE CONNECTED TOGETHER.
THE PHMODE PIN IS FLOATING FOR 120°. PHASE SHIFT AT CLKOUT.
THE SET PINS CAN BE CONNECTED TOGETHER FOR 300µA CURRENT REFERENCE; THIS PROVIDES LOWER 1/f NOISE AND BETTER CURRENT SHARING.

Figure 42. 3-Phase 3.3V, 48A from 4.5V to 16V_{IN}, 700kHz with Soft Start, Fast Startup, and Power Good



PINS NOT USED: COMPb, SW, T_{SENSE}^+, AND T_{SENSE}^-.

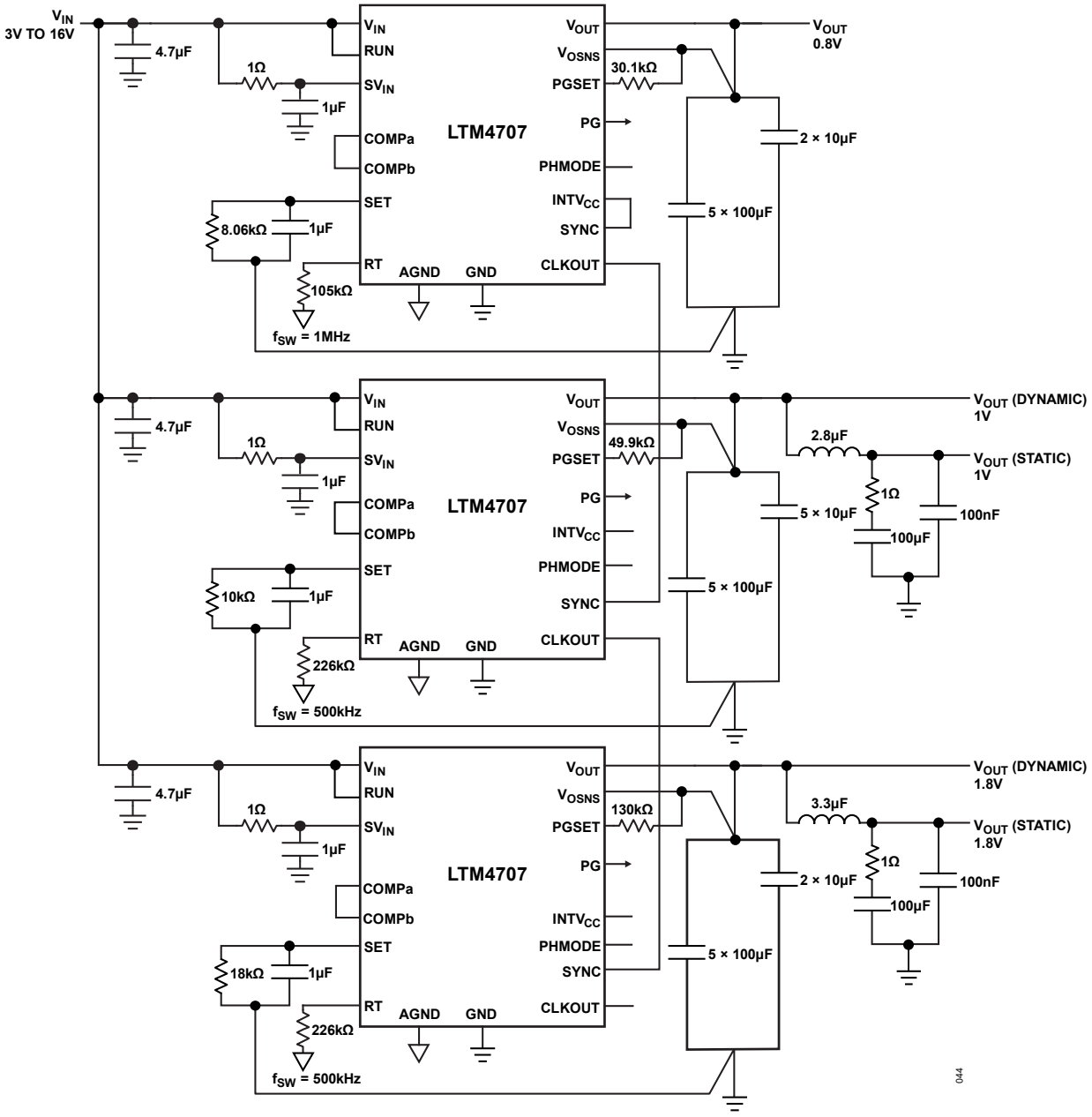
CH2 AND CH3 ARE SYNCHRONIZED TO 900kHz THROUGH THE SYNC PIN. THE R_T RESISTOR VALUE MUST SET INTERNAL OSCILLATOR TO <720kHz (80% OF 900kHz).

THE COMPa PINS ARE CONNECTED TOGETHER.

THE PHMODE PIN IS CONNECTED TO $INTV_{CC}$ FOR 90°. PHASE SHIFT AT CLKOUT.

THE SET PINS CAN BE CONNECTED TOGETHER FOR 400µA CURRENT REFERENCE; THIS PROVIDES LOWER 1/f NOISE AND BETTER CURRENT SHARING.

Figure 43. 4-Phase 2.5V, 64A from 3.9V to 16V_{IN}, 900kHz with Soft Start, Fast Startup, and Power Good



PINS NOT USED: SW, T_{SENSE}^{+}, AND T_{SENSE}^{-}.

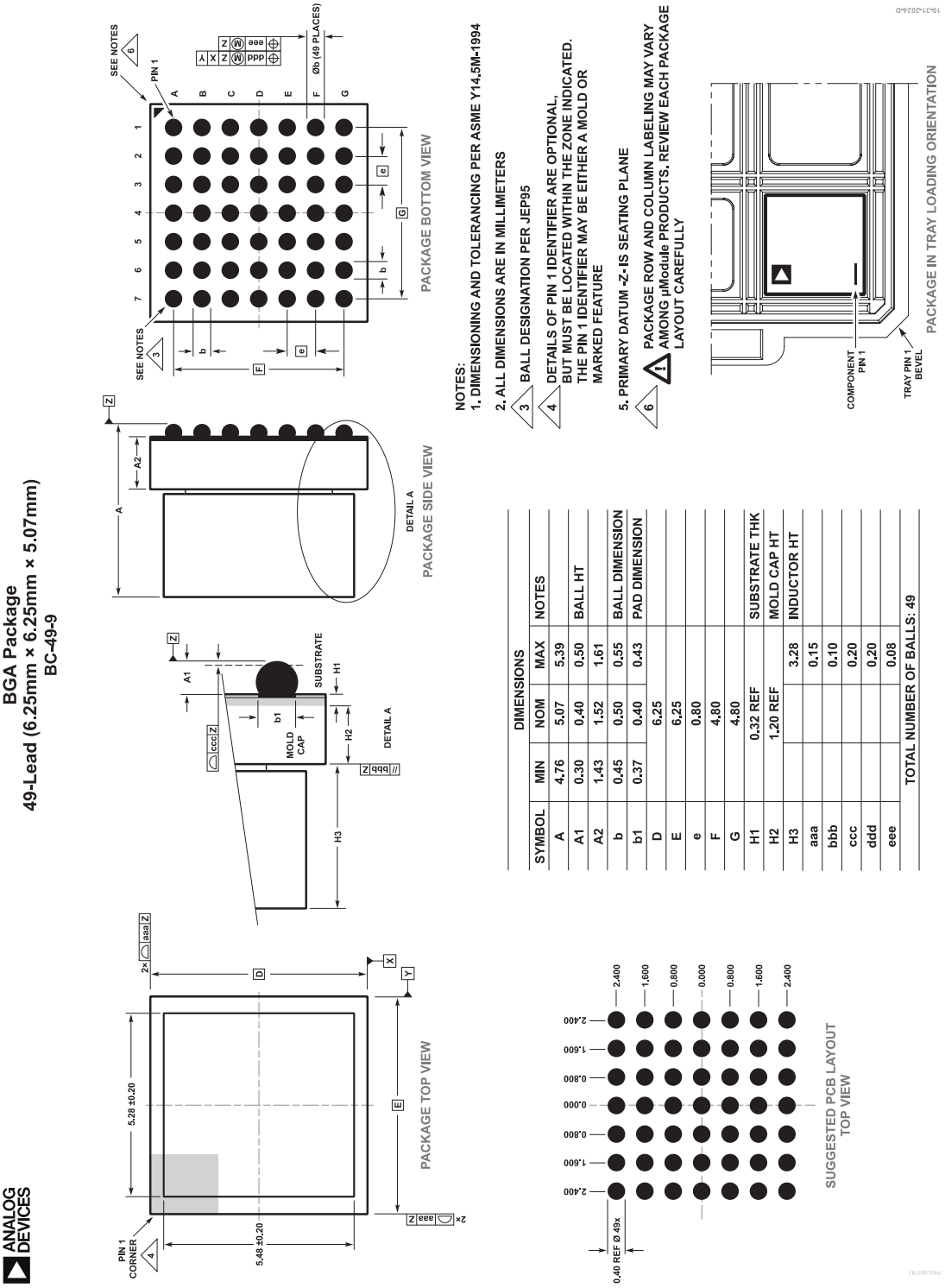
Figure 44. Powering a Transceiver Using 3 × LTM4707

Related Parts

Table 8. Related Parts

PART NUMBER	DESCRIPTION	COMMENTS
LTM®8053	40V, 3.5A low EMI Silent Switcher µModule regulator	3.4V ≤ V_{IN} ≤ 40V, 0.97V ≤ V_{OUT} ≤ 15V, 6.25mm × 9mm × 3.32mm BGA
LTM8065	40V, 2.5A low EMI Silent Switcher µModule regulator	3.4V ≤ V_{IN} ≤ 40V, 0.97V ≤ V_{OUT} ≤ 18V, 6.25mm × 6.25mm × 2.32mm BGA
LTM8063	40V, 2A low EMI Silent Switcher µModule regulator	3.2V ≤ V_{IN} ≤ 40V, 0.8V ≤ V_{OUT} ≤ 15V, 4mm × 6.25mm × 2.22mm BGA
LTM8074	40V, 1.2A low EMI Silent Switcher µModule regulator	3.2V ≤ V_{IN} ≤ 40V, 0.8V ≤ V_{OUT} ≤ 12V, 4mm × 4mm × 1.82mm BGA
LTM8024	40V, dual 3.5A low EMI Silent Switcher µModule regulator	3V ≤ V_{IN} ≤ 40V, 0.8V ≤ V_{OUT} ≤ 8V, 9mm × 11.25mm × 3.32mm BGA
LTM8078	40V, dual 1.4A low EMI Silent Switcher µModule regulator	3V ≤ V_{IN} ≤ 40V, 0.8V ≤ V_{OUT} ≤ 10V, 6.25mm × 6.25mm × 2.32mm BGA
LTM8060	40V, quad 3A low EMI Silent Switcher µModule regulator	3V ≤ V_{IN} ≤ 40V, 0.8V ≤ V_{OUT} ≤ 8V, 11.9mm × 16mm × 3.32mm BGA
LTM8051	40V, quad 1.2A low EMI Silent Switcher µModule regulator	3V ≤ V_{IN} ≤ 40V, 0.8V ≤ V_{OUT} ≤ 8V, 6.25mm × 11.25mm × 2.32mm BGA
LTM8080	40V_{IN}, dual 500mA or single 1A ultralow noise, ultrahigh PSRR µModule regulator	3.5V ≤ V_{IN} ≤ 40V, 0V ≤ V_{OUT} ≤ 8V, 6.25mm × 9mm × 3.32mm BGA
LTM4657	8A µModule regulator, pin compatible with LTM4638 and LTM4626	3.1V ≤ V_{IN} ≤ 20V, 0.5V ≤ V_{OUT} ≤ 5.5V, 6.25mm × 6.25mm × 3.87mm BGA
LTM4626	12A µModule regulator, pin compatible with LTM4638 and LTM4657	3.1V ≤ V_{IN} ≤ 20V, 0.6V ≤ V_{OUT} ≤ 5.5V, 6.25mm × 6.25mm × 3.87mm BGA
LTM4638	15A µModule regulator, pin compatible with LTM4657/LTM4626	3.1V ≤ V_{IN} ≤ 20V. 0.6V ≤ V_{OUT} ≤ 5.5V, 6.25mm × 6.25mm × 5.02mm BGA
LTM4702	16V_{IN} 8A ultralow noise Silent Switcher 3 µModule regulator, pin compatible with LTM4703 and LTM4707	3V ≤ V_{IN} ≤ 16V, 0.3V ≤ V_{OUT} ≤ 5.7V, 6.25mm × 6.25mm × 5.07mm BGA
LTM4703	16V_{IN} 12A ultralow noise Silent Switcher 3 µModule regulator, pin compatible with LTM4702 and LTM4707	3V ≤ V_{IN} ≤ 16V, 0.3V ≤ V_{OUT} ≤ 6V, 6.25mm × 6.25mm × 5.07mm BGA
LTM4709	Triple 3A, ultralow noise, high PSRR, ultrafast µModule linear regulator with configurable output array	0.6V ≤ V_{IN} ≤ 5.5V, 0.5V ≤ V_{OUT} ≤ 4.2V, 6mm × 12mm × 1.92mm BGA

OUTLINE DIMENSIONS



DIMENSIONS				
SYMBOL	MIN	NOM	MAX	NOTES
A	4.76	5.07	5.39	
A1	0.30	0.40	0.50	BALL HT
A2	1.43	1.52	1.61	
b	0.45	0.50	0.55	BALL DIMENSION
b1	0.37	0.40	0.43	PAD DIMENSION
D		6.25		
E		6.25		
e		0.80		
F		4.80		
G		4.80		
H1		0.32 REF		SUBSTRATE THK
H2		1.20 REF		MOLD CAP HT
H3			3.28	INDUCTOR HT
aaa			0.15	
bbb			0.10	
ccc			0.20	
ddd			0.20	
eee			0.08	
TOTAL NUMBER OF BALLS: 49				

Figure 45. 49-Lead, 6.25mm × 6.25mm × 5.07mm, BGA

ORDERING GUIDE

Table 9. Ordering Guide

MODEL	TEMPERATURE RANGE[1]	PACKAGE DESCRIPTION	PACKAGE OPTION
LTM4707EY#PBF	–40°C to 125°C	Part marking: 4707. SAC305 (RoHS) lead finish.* e1 finish code. Moisture sensitivity level 4 (MSL 4) rated device.	*49-Lead, 6.25mm × 6.25mm × 5.07mm, BGA*
LTM4707IY#PBF	–40°C to 125°C	Part marking: 4707. SAC305 (RoHS) lead finish.* e1 finish code. Moisture sensitivity level 4 (MSL 4) rated device.	*49-Lead, 6.25mm × 6.25mm × 5.07mm, BGA*

[1] The LTM4707 is tested under pulsed load conditions such that $T_J \approx T_A$. The LTM4707E is guaranteed to meet performance specifications over the 0°C to 125°C internal operating temperature range. Specifications over the full –40°C to 125°C internal operating temperature range are assured by design, characterization, and correlation with statistical process controls. The LTM4707I is guaranteed to meet specifications over the full –40°C to 125°C internal operating temperature range. Note that the maximum ambient temperature consistent with these specifications is determined by specific operating conditions in conjunction with board layout, the rated package thermal resistance, and other environmental factors.

Contact the factory for parts specified with wider operating temperature ranges. *The lead finish code is per IPC/JEDEC J-STD-609.

Recommended LGA and BGA PCB assembly and manufacturing procedures.

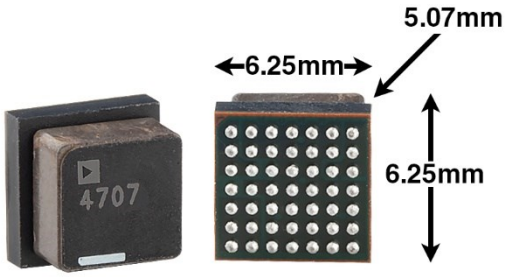
LGA and BGA package and tray drawings.

Table 10.Evaluation Board

PART NUMBER	DESCRIPTION
EVAL-LTM4707-AZ	16V, 16A ultralow noise Silent Switcher 3 µModule regulator.

SELECTOR GUIDE

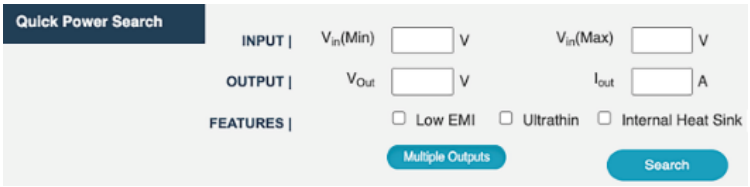
Package Photos



(Part Marking Is Either Ink Mark or Laser Mark)

Design Resources

Table 11.Design Resources

	SUBJECT	DESCRIPTION
µModule Design and Manufacturing Resources	**Design:** ▶ Selector guides ▶ Evaluation (Demo) boards and Gerber files ▶ Free simulation tools	**Manufacturing:** ▶ Quick start guide ▶ PCB design, assembly, and manufacturing guidelines ▶ Package and board level reliability
µModule Regulator Products Search	▶ Sort table of products by parameters and download the result as a spread sheet. ▶ Search using the Quick Power Search parametric table. 	
Digital Power System Management	The Analog Devices family of digital power supply management ICs are highly integrated solutions that offer essential functions, including power supply monitoring, supervision, margining and sequencing, and feature EEPROM for storing user configurations and fault logging.	