100V Low I_Q, Synchronous Boost Controller for GaN FETs

FEATURES

- GaN Drive Technology Fully Optimized for GaN FETs
- Output Voltage Up to 100V
- Wide V_{IN} Range: 4V to 60V and Operates Down to 1V after Start-Up
- No Catch, Clamp, or Bootstrap Diodes Needed
- Internal Smart Bootstrap Switches Prevent Overcharging of High-Side Driver Supply
- Resistor-Adjustable Dead Times
- Split-Output Gate Drivers for Adjustable Turn On and Turn Off Driver Strengths
- Accurate Adjustable Driver Voltage and UVLO
- Low Operating I_Q: 15µA
- Programmable Frequency (100kHz to 3MHz)
- Synchronizable Frequency (100kHz to 3MHz)
- Spread Spectrum Frequency Modulation
- 28-Lead (4mm × 5mm), Side Wettable, QFN Package
- AEC-Q100 Qualified for Automotive Applications

APPLICATIONS

- Automotive and Industrial Power Systems
- Military Avionics and Medical Systems
- Telecommunications Power Systems

GENERAL DESCRIPTION

The *LTC®7893* is a high performance, step-up, dc-to-dc switching regulator controller that drives all N-channel synchronous gallium nitride (GaN) field effect transistor (FET) power stages from output voltages up to 100V. The LTC7893 solves many of the challenges traditionally faced when using GaN FETs. The LTC7893 simplifies the application design while requiring no protection diodes and no other additional external components compared to a silicon metal-oxide semiconductor field effect transistor (MOSFET) solution.

The internal smart bootstrap switches prevent overcharging of the BOOST pin to the SW pin high-side driver supply during dead times, protecting the gate of the top GaN FET. The dead times of the LTC7893 can optionally be optimized with external resistors for margin or to tailor the application for higher efficiency and allowing for high frequency operation.

The gate drive voltage of the LTC7893 can be precisely adjusted from 4V to 5.5V to optimize performance, and to allow the use of different GaN FETs, or even logic level MOSFETs. When biased from the boost converter regulator output, the LTC7893 can operate from an input supply as low as 1V after start-up.

TYPICAL APPLICATION

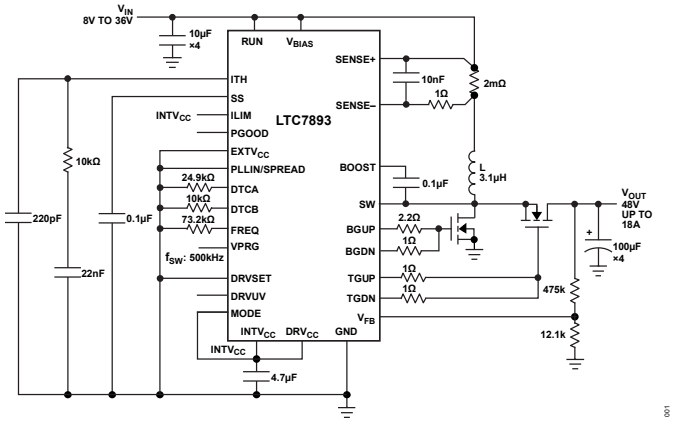


Figure 1. High Efficiency, 48V_{OUT} Output Boost Regulator Driving GaN FETs

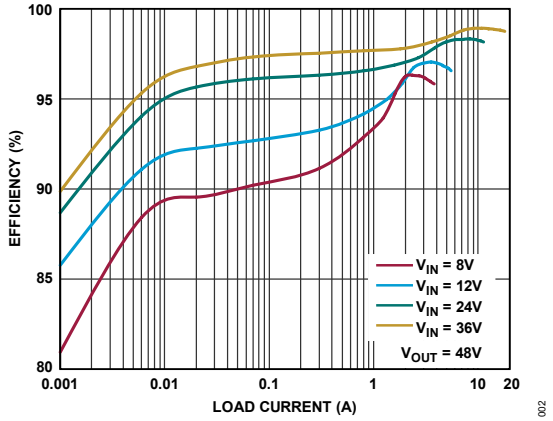


Figure 2. V_{OUT} Efficiency and Power Loss for Figure 1

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REVISION HISTORY

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	10/24	Initial release	—
A	8/26	Updated Inductor Value Calculation section Updated Equation 18	21 31

SPECIFICATIONS

Table 1. Electrical Characteristics

(Specifications are at T_J = -40°C to +125°C for the minimum and maximum values, T_A = 25°C for the typical values, V_{BIAS} = 12V, RUN = 5V, VPRG = Floating, $EXTV_{CC}$ = 0V, DRVSET = 0V, DRVUV = 0V, DTCA and DTCB = 0V, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS/COMMENTS	MIN	TYP	MAX	UNITS
Input Supply						
Bias Input Supply Operating Range	V_{BIAS}		4		100	V
Boost Converter Input Supply Operating Range	V_{IN}	$V_{BIAS} \geq 4V$	1		60	V
Output Voltage Operating Range	V_{OUT}		1.2		100	V
Controller Operation						
Regulated Feedback Voltage[1]	V_{FB}	V_{BIAS} = 4V to 100V, ITH Voltage = 0.6V to 1.2V VPRG = floating, T_A = 25°C VPRG = floating VPRG = 0V VPRG = $INTV_{CC}$	 1.188 1.182 23.45 27.38	 1.2 1.2 24 28	 1.212 1.218 24.55 28.62	 V V V V
Feedback Current[1]		VPRG = floating, T_A= 25°C VPRG = 0V or $INTV_{CC}$	-50	0 2	+50	nA µA
Feedback Overvoltage Threshold		Relative to V_{FB}, T_A = 25°C	7	10	13	%
Transconductance Amplifier[1]	g_m	ITH = 1.2V, Sink and Source Current = 5µA		1.8		mMho
Maximum Current Sense Threshold	$V_{SENSE(MAX)}$	V_{FB} = 1.1V, $SENSE^+$ = 12V ILIM = 0V ILIM = floating ILIM = $INTV_{CC}$	 21 45 67	 26 50 75	 32 56 83	 mV mV mV
$SENSE^-$ Pin Current	I_{SENSE^-}	$SENSE^-$ = 12V, T_A = 25°C	-1		+1	µA
$SENSE^+$ Pin Current	I_{SENSE^+}	$SENSE^+ < 3V$ $3.3V \leq SENSE^+ < INTV_{CC} - 0.5V$ $SENSE^+ > INTV_{CC} + 0.5V$		1 75 725		µA µA µA
Soft-Start Charge Current		SS = 0V	9.5	12	14.5	µA

(Specifications are at T_J = -40°C to +125°C for the minimum and maximum values, T_A = 25°C for the typical values, V_{BIAS} = 12V, RUN = 5V, VPRG = Floating, $EXTV_{CC}$ = 0V, DRVSET = 0V, DRVUV = 0V, DTCA and DTCB = 0V, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS/COMMENTS	MIN	TYP	MAX	UNITS
RUN Pin ON Threshold		RUN rising	1.15	1.20	1.25	V
RUN Pin Hysteresis				120		mV
DC Supply Current						
V_{BIAS} Shutdown Current		RUN = 0V		1.1		µA
V_{BIAS} Sleep Mode Current		$SENSE^+$ < 3.2V, $EXTV_{CC}$ = 0V		15		µA
Sleep Mode Current[2] V_{BIAS} Current V_{BIAS} Current $EXTV_{CC}$ Current $SENSE^+$ Current		 $SENSE^+$ ≥ 3.2V, $EXTV_{CC}$ = 0V $SENSE^+$ ≥ 3.2V, $EXTV_{CC}$ ≥ 4.8V $SENSE^+$ ≥ 3.2V, $EXTV_{CC}$ ≥ 4.8V $SENSE^+$ ≥ 3.2V		 5 1 6 10		 µA µA µA µA
Pulse-Skipping (PS) or Forced Continuous Mode (FCM), V_{BIAS} or $EXTV_{CC}$ Current[2]				2		mA
Gate Drivers						
TGx or BGx On Resistance		DRVSET = $INTV_{CC}$ Pull-Up Pull-Down		 1.0 1.0		 Ω Ω
BOOST to DRV_{CC} Switch On Resistance		DRVSET = $INTV_{CC}$		6		Ω
TGx or BGx Transition Time[3]		Rise Time Fall Time		25 15		ns ns
BGx Off to TGx On Adaptive Delay Time[4]		DTCA = 0V		15		ns
TGx Off to BGx On Adaptive Delay Time[4]		DTCB = 0V		15		ns
BGx Off to TGx On Open-Loop Delay[4]		DTCA = 10kΩ DTCA = 50kΩ DTCA = 100kΩ		7 25 40		ns ns ns

(Specifications are at T_J = -40°C to +125°C for the minimum and maximum values, T_A = 25°C for the typical values, V_{BIAS} = 12V, RUN = 5V, VPRG = Floating, $EXTV_{CC}$ = 0V, DRVSET = 0V, DRVUV = 0V, DTCA and DTCB = 0V, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS/COMMENTS	MIN	TYP	MAX	UNITS
TGx Off to BGx On Open-Loop Delay[4]		DTCB = 10kΩ DTCB = 50kΩ DTCB = 100kΩ		7 25 40		ns ns ns
BGx Minimum On-Time[5]	$t_{ON(MIN)}$			100		ns
Maximum Duty Factor for BGx		V_{FREQ} = 0V		93		%
$INTV_{CC}$ Low Dropout (LDO) Linear Regulators						
$INTV_{CC}$ Voltage for V_{BIAS} and $EXTV_{CC}$ LDOs		$EXTV_{CC}$ = 0V for V_{BIAS} LDO, $EXTV_{CC}$ = 12V for $EXTV_{CC}$ LDO DRVSET = $INTV_{CC}$ DRVSET = 0V DRVSET = 64.9kΩ	 5.2 4.8 4.5	 5.5 5.0 4.75	 5.7 5.2 5.0	 V V V
DRV_{CC} Load Regulation		DRV_{CC} load current = 0mA to 100mA, T_A = 25°C		1	3	%
Undervoltage Lockout	UVLO	DRV_{CC} Rising DRVUV = $INTV_{CC}$ DRVUV = 0V DRVUV = floating DRV_{CC} Falling DRVUV = $INTV_{CC}$ DRVUV = 0V DRVUV = floating	 4.8 3.6 4.2 4.55 3.4 4.0	 5.0 3.8 4.4 4.75 3.6 4.18	 5.2 4.0 4.6 4.95 3.8 4.4	 V V V V V V
$EXTV_{CC}$ LDO Switchover Voltage $EXTV_{CC}$ Rising		DRVUV = $INTV_{CC}$ or floating, T_A = 25°C DRVUV = 0V, T_A = 25°C	5.75 4.6	5.95 4.76	6.15 4.9	V V
$EXTV_{CC}$ LDO Switchover Hysteresis $EXTV_{CC}$ Falling		DRVUV = $INTV_{CC}$ or floating DRVUV = 0V		390 220		mV mV
Spread Spectrum Oscillator and Phase-Locked Loop						
Fixed Frequencies	f_{OSC}	PLLIN/SPREAD = 0V FREQ = 0V, T_A = 25°C FREQ = $INTV_{CC}$ FREQ = 374kΩ	 320 2.0	 370 2.25 100	 420 2.5	 kHz MHz kHz

(Specifications are at T_J = -40°C to +125°C for the minimum and maximum values, T_A = 25°C for the typical values, V_{BIAS} = 12V, RUN = 5V, VPRG = Floating, $EXTV_{CC}$ = 0V, DRVSET = 0V, DRVUV = 0V, DTCA and DTCB = 0V, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS/COMMENTS	MIN	TYP	MAX	UNITS
		FREQ = 75kΩ, T_A = 25°C FREQ = 12.4kΩ	450	500 3	550	kHz MHz
Synchronizable Frequency Range	f_{SYNC}	PLLIN/SPREAD = External Clock	0.1		3	MHz
PLLIN Input High Level			2.2			V
PLLIN Input Low Level					0.5	V
Spread Spectrum Frequency Range (Relative to f_{OSC})		PLLIN/SPREAD = $INTV_{CC}$ Minimum Frequency Maximum Frequency		 0 20		 % %
PGOOD Outputs						
PGOOD Voltage Low		PGOOD = 2mA, T_A = 25°C		0.2	0.4	V
PGOOD Leakage Current		PGOOD = 5V, T_A = 25°C	-1	0	+1	µA
PGOOD Trip Level (V_{FB} with Respect to Set Regulated Voltage)		T_A = 25°C V_{FB} Rising Hysteresis V_{FB} Falling Hysteresis	 7 -13 	 10 1.6 -10 1.6	 13 -7 	 % % % %
PGOOD Delay for Reporting a Fault				25		µs

1 The LTC7893 is tested in a feedback loop that servos ITH voltage (V_{ITH}) to a specified voltage and measures the resultant feedback voltage (V_{FB}).

2 $SENSE^+$ bias current is reflected to the bias supply by the formula $I_{VBIAS} = I_{SENSE}{}^+ \times V_{BIAS}/(V_{OUT} \times \eta)$, where η is the efficiency.

3 Rise and fall times are measured using 10% and 90% levels. Delay times are measured using 50% levels unless otherwise noted.

4 TGx falling to BGx rising and BGx falling to TGx rising delay times are measured at the rising and falling thresholds on TGx and BGx of approximately 1V. See *Figure 40* and *Figure 41*.

5 The minimum on-time condition specified for inductor peak-to-peak ripple current is >40% of the maximum load current (I_{MAX}) (see the *Minimum On-Time Considerations* section).

ABSOLUTE MAXIMUM RATINGS

T_A = 25°C, unless otherwise specified.

Table 2. Absolute Maximum Ratings

PARAMETER	RATING
Bias Input Supply (V_{BIAS})	-0.3V to 100V
RUN	-0.3V to 100V
BOOST	-0.3V to 106V
SW	-5V to 100V
BOOST to SW	-0.3V to 6V
TGUP, TGDN[1]	Not applicable
BGUP, BGDN[1]	Not applicable
$EXTV_{CC}$	-0.3V to 30V
DRV_{CC}, $INTV_{CC}$, $BSTV_{CC}$	-0.3V to 6V
V_{FB}	-0.3V to 65V
PLLIN/SPREAD, FREQ	-0.3V to 6V
SS	-0.3V to 6V
ITH	-0.3V to 6V
DRVSET, DRVUV	-0.3V to 6V
MODE, ILIM, VPRG	-0.3V to 6V
PGOOD	-0.3V to 6V
DTCA, DTCB	-0.3V to 6V
$SENSE^+$, $SENSE^-$	-0.3V to 65V
$SENSE^+$ to $SENSE^-$ Continuous	-0.3V to +0.3V
$SENSE^+$ to $SENSE^-$ <1ms	-100mA to 100mA
Operating Junction Temperature Range[2]	-40°C to 125°C
Storage Temperature Range	-65°C to 150°C

[1] Do not apply a voltage or current source to these pins. They must be connected to capacitive loads only. Otherwise, permanent damage may occur.

[2] The LTC7893 is specified over the –40°C to 125°C operating junction temperature range. High junction temperatures degrade operating lifetimes. Note the maximum ambient temperature consistent with these specifications is determined by specific operating conditions in conjunction with the board layout, rated package thermal impedance, and other environmental factors. The junction temperature (T_J, in °C) is calculated from the ambient temperature (T_A, in °C) and power dissipation (P_D, in Watts) according to the following formula: $T_J = T_A + (P_D \times \theta_{JA})$, where θ_{JA} is the package thermal impedance and equals 43°C/W for the 28-lead (4mm × 5mm), side wettable, quad flat no lead (QFN) package.

PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS

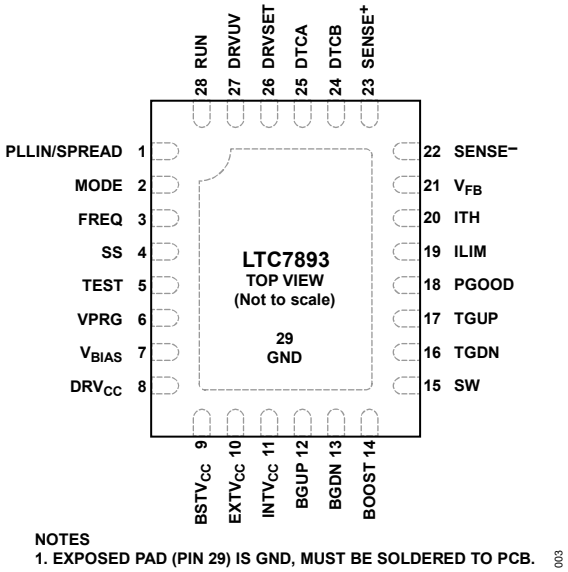


Figure 3. Pin Configuration

Table 3. Pin Descriptions

PIN	NAME	DESCRIPTION
1	PLLIN/ SPREAD	External Synchronization Input to Phase Detector/Spread Spectrum Enable. When an external clock is applied to PLLIN/SPREAD, the phase-locked loop forces the rising BGx signal to synchronize with the rising edge of the external clock. When not synchronizing to an external clock, tie this input to $INTV_{CC}$ to enable spread spectrum dithering of the oscillator, or to GND to disable spread spectrum dithering.
2	MODE	Mode Select Input. This input determines how the LTC7893 operates at light loads. Connect MODE to GND to select the Burst Mode® operation. An internal 100kΩ resistor to GND also invokes Burst Mode operation when MODE is floating. Connect MODE to $INTV_{CC}$ to force continuous inductor current operation. Tying MODE to $INTV_{CC}$ through a 100kΩ resistor selects the pulse-skipping operation.
3	FREQ	Frequency Control Pin for the Internal Voltage Controlled Oscillator (VCO). Connect FREQ to GND for a fixed frequency of 370kHz. Connect FREQ to $INTV_{CC}$ for a fixed frequency of 2.25MHz. Program frequencies between 100kHz and 3MHz by using a resistor between FREQ and GND. Minimize the capacitance on FREQ.
4	SS	External Soft Start Input. SS regulates the V_{FB} voltage to the lesser of 1.2V or the voltage on the SS pin. An internal 12µA pull-up current source is connected to SS. A capacitor to GND at SS sets the ramp time to the final regulated output voltage. The ramp time is equal to 1ms for every 10nF of capacitance.
5	TEST	Test Pin. This pin must be soldered to PCB GND.
6	VPRG	Output Voltage Control Pin. This pin sets the adjustable output mode using the external feedback resistors or the fixed 28V or 24V output mode. Floating VPRG programs the output from 1.2V to 100V with an external resistor divider, regulating V_{FB}

		to 1.2V. Connect VPRG to $INTV_{CC}$ or GND to program the output to 28V or 24V, respectively, through an internal resistor divider on V_{FB}.
7	V_{BIAS}	Main Supply Pin. A bypass capacitor must be tied between V_{BIAS} and GND.
8	DRV_{CC}	Gate Driver Power Supply Pin. The gate drivers are powered from DRV_{CC}. Connect DRV_{CC} to $INTV_{CC}$ by a separate trace to the $INTV_{CC}$ bypass capacitor.
9	$BSTV_{CC}$	Bootstrap diode anode connection pin. An optional external Schottky diode can be placed between the $BSTV_{CC}$ and BOOST pins to bypass most of the 7Ω switch resistance between DRV_{CC} and BOOST.
10	$EXTV_{CC}$	External Power Input to an Internal LDO Regulator Connected to DRV_{CC}. This LDO regulator supplies $INTV_{CC}$ power, bypassing the internal V_{BIAS} LDO regulator whenever $EXTV_{CC}$ is higher than the $EXTV_{CC}$ switchover voltage. See the $EXTV_{CC}$ connection in the *Power and Bias Supplies (VBIAS, EXTVCC, DRVCC, and INTVCC)* section and *INTVCC Regulators (OPTI-DRIVE)* section. Do not exceed 30V on $EXTV_{CC}$. Connect $EXTV_{CC}$ to GND if the $EXTV_{CC}$ LDO regulator is not used.
11	$INTV_{CC}$	Output of the Internal LDO Regulator. The $INTV_{CC}$ voltage regulation point is set by the DRVSET pin. $INTV_{CC}$ must be decoupled to GND with a 4.7µF to 10µF ceramic or other low equivalent series resistance (ESR) capacitor.
12	BGUP	High Current Gate Driver Pull-Up for Bottom FET. BGUP pulls up to DRV_{CC}. Tie BGUP directly to the bottom FET gate for maximum gate drive transition speed on the gate rising edge. Tie a resistor between BGUP and the bottom FET gate to adjust the gate rising slew rate. BGUP also serves as the Kelvin sense of the bottom FET gate during turn off.
13	BGDN	High Current Gate Driver Pull-Down for Bottom FET. BGDN pulls down to GND. Tie BGDN directly to the bottom FET gate for maximum gate drive transition speed on the gate falling edge. Tie a resistor between BGDN and the bottom FET gate to adjust the gate falling slew rate. BGDN also serves as the Kelvin sense of the bottom FET gate during turn on.
14	BOOST	Bootstrapped Supply to the Top Side Floating Driver. Connect a capacitor between the BOOST and SW pins. An internal switch provides power to the BOOST pin from DRV_{CC} when the bottom FET turns on. The voltage swing at the BOOST pin is from DRV_{CC} to (V_{OUT} + DRV_{CC}).
15	SW	Switch Node Connection to Inductor.
16	TGDN	High Current Gate Driver Pull-Down for Top FET. TGDN pulls down to SW. Tie TGDN directly to the top FET gate for maximum gate drive transition speed on the gate falling edge. Tie a resistor between TGDN and the top FET gate to adjust the gate falling slew rate.
17	TGUP	High Current Gate Driver Pull-Up for Top FET. TGUP pulls up to BOOST. Tie TGUP directly to the top FET gate for maximum gate drive transition speed on the gate rising edge. Tie a resistor between TGUP and the top FET gate to adjust the gate rising slew rate.
18	PGOOD	Power Good Open-Drain Logic Output. PGOOD is pulled to GND when the voltage on V_{FB} is not within ±10% of its set point.

19	ILIM	Current Comparator Sense Voltage Range Input. Tying ILIM to GND or $INTV_{CC}$ or floating ILIM sets the maximum current sense threshold to one three different levels (25mV, 75mV, and 50mV, respectively).
20	ITH	Error Amplifier Output and Switching Regulator Compensation Point. The current comparator trip point increases with this control voltage.
21	V_{FB}	Error Amplifier Feedback Input. If VPRG is floating, V_{FB} pin receives the remotely sensed feedback voltage from an external resistive divider across the output. If VPRG is tied to GND or $INTV_{CC}$, the V_{FB} pin receives the remotely sensed output voltage directly.
22	$SENSE^-$	The Negative (-) Input to the Differential Current Comparator. The ITH pin voltage and controlled offset between the $SENSE^+$ and $SENSE^-$ pins, in conjunction with the current sense resistor (R_{SENSE}), set the current trip threshold.
23	$SENSE^+$	The Positive (+) Input to the Differential Current Comparator. The $SENSE^+$ pin supplies current to the current comparator when $SENSE^+$ is greater than $INTV_{CC}$. When $SENSE^+$ is 3.2V or greater, the pin supplies the majority of the sleep mode quiescent current instead of V_{BIAS}, further reducing the input referred quiescent current.
24	DTCB	Dead Time Control Pin for Top Gate Off to Bottom Gate On Delay. Connect DTCB to GND to program an adaptive delay of approximately 15ns. Connect a 10kΩ to 200kΩ resistor between DTCB and GND to program a non-adaptive (open-loop) Top Gate off to Bottom Gate on dead time delay from 7ns to 60ns.
25	DTCA	Dead Time Control Pin for Bottom Gate Off to Top Gate On Delay. Connect DTCA to GND to program an adaptive delay of approximately 15ns. Connect a 10kΩ to 200kΩ resistor between DTCA and GND to program a non-adaptive (open-loop) Bottom Gate off to Top Gate on dead time delay from 7ns to 60ns.
26	DRVSET	$INTV_{CC}$ Regulation Program Pin. DRVSET sets the regulation point for the $INTV_{CC}$ LDO linear regulators. Connect DRVSET to GND to set $INTV_{CC}$ to 5V. Connect DRVSET to $INTV_{CC}$ to set $INTV_{CC}$ to 5.5V. Program voltages between 4V and 5.5V by placing a resistor (43kΩ to 100kΩ) between DRVSET and GND. The resistor and an internal 20µA source current create a voltage used by the $INTV_{CC}$ LDO regulator to set the regulation point.
27	DRVUV	DRV_{CC} UVLO and $EXTV_{CC}$ Switchover Program Pin. DRVUV determines the $INTV_{CC}$ UVLO and $EXTV_{CC}$ switchover rising and falling thresholds, as listed in *Table 1*.
28	RUN	Run Control Input for the Controller. Forcing RUN less than 1.08V disables controller switching. Forcing RUN less than 0.7V shuts down the LTC7893, reducing quiescent current to approximately 1µA. Tie the RUN pin to V_{BIAS} for always on operation.
29	GND (EPAD)	Ground (Exposed Pad). The exposed pad must be soldered to PCB ground for rated electrical and thermal performance.

TYPICAL PERFORMANCE CHARACTERISTICS

T_A = 25°C, unless otherwise noted.

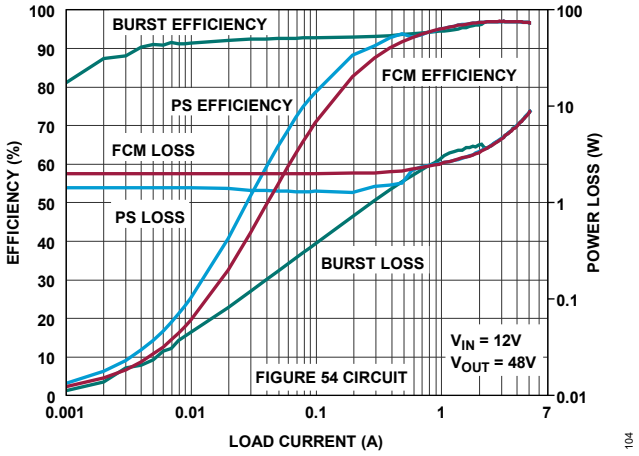


Figure 4. Efficiency and Power Loss vs. Load Current

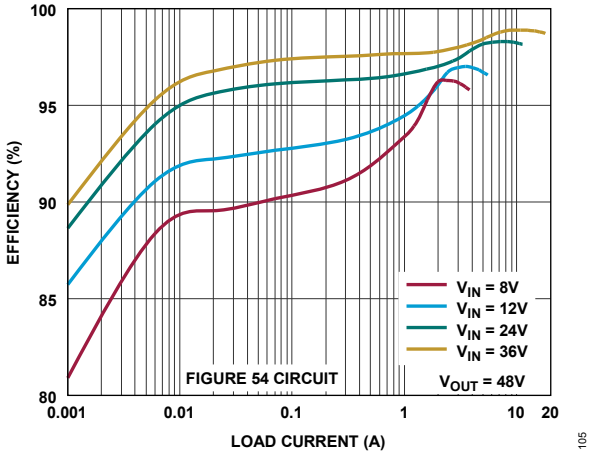


Figure 5. Efficiency vs. Load Current

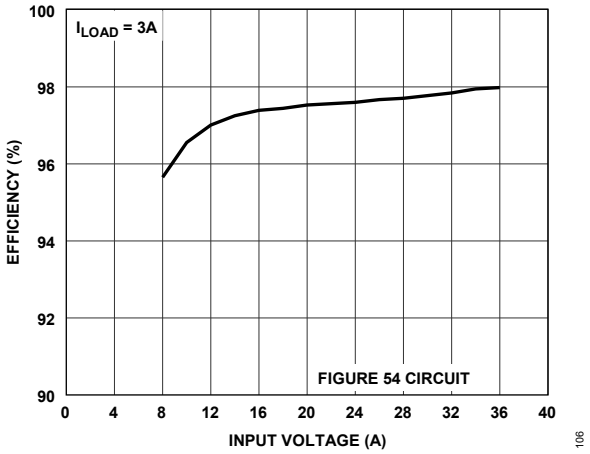


Figure 6. Efficiency vs. Input Voltage

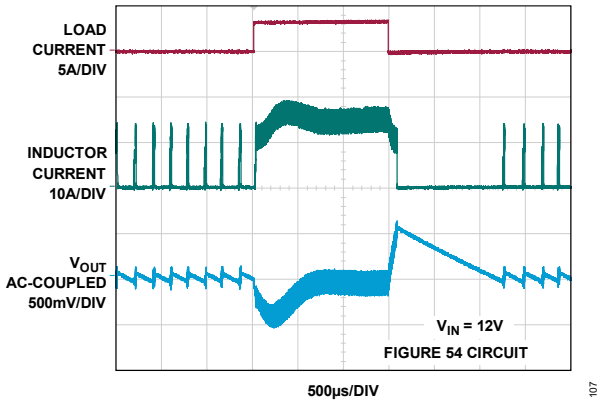


Figure 7. Load Step Burst Mode Operation

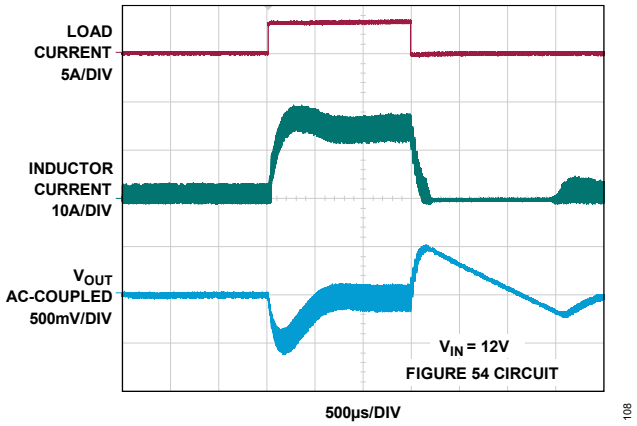


Figure 8. Load Step Pulse-Skipping Mode

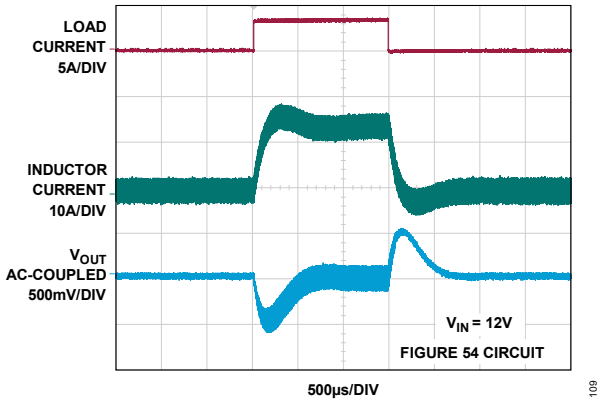


Figure 9. Load Step Forced Continuous Mode

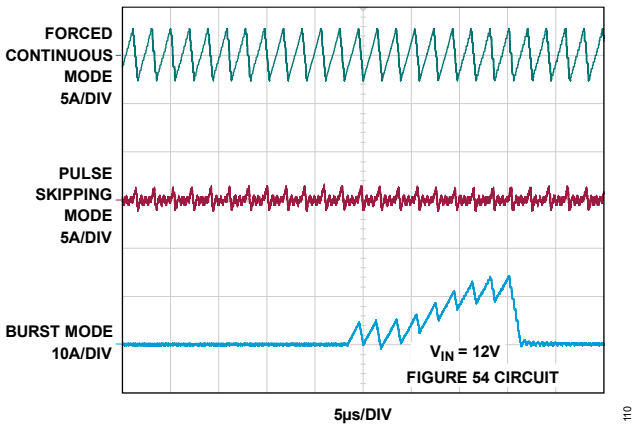


Figure 10. Inductor Current at Light Load

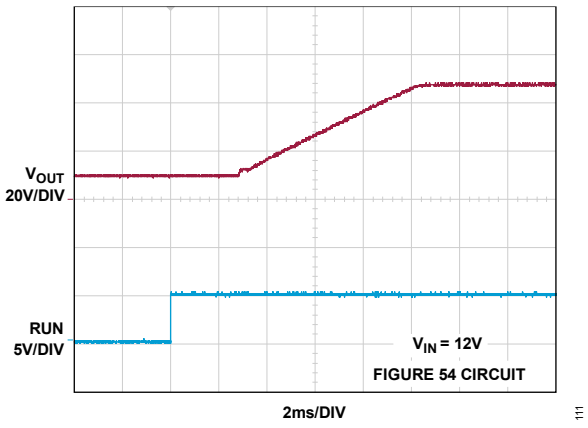


Figure 11. Soft Start-Up

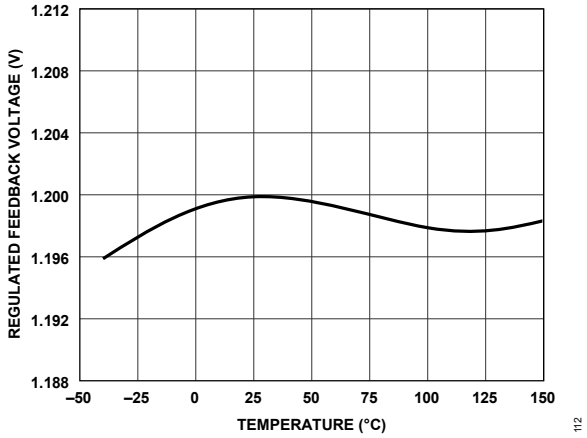


Figure 12. Regulated Feedback Voltage vs. Temperature

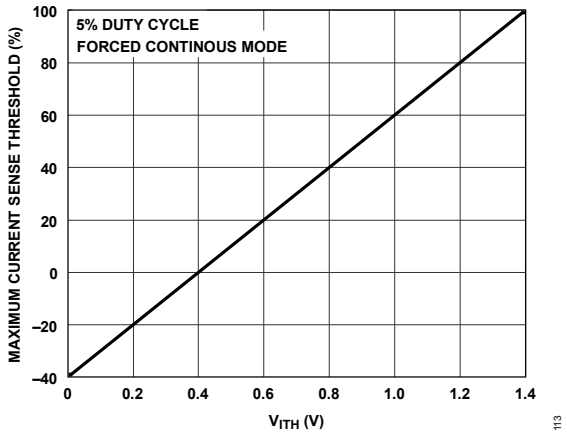


Figure 13. Maximum Current Sense Threshold Relative to $V_{SENSE(MAX)}$ vs. V_{ITH} in Forced Continuous Mode

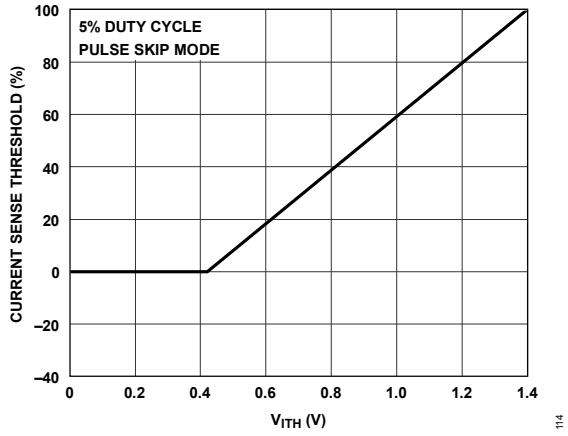


Figure 14. Maximum Current Sense Threshold Relative to $V_{SENSE(MAX)}$ vs. V_{ITH} in Pulse-Skipping Mode

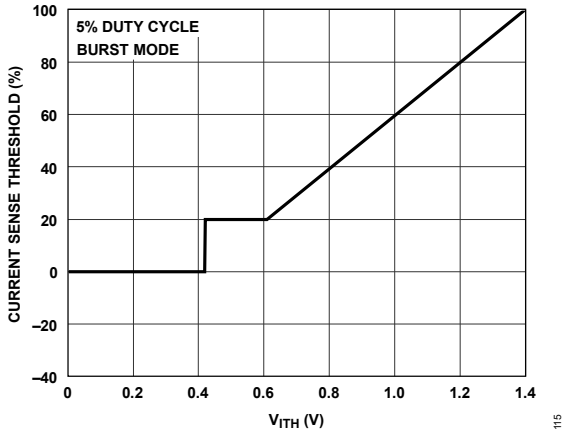


Figure 15. Maximum Current Sense Threshold Relative to $V_{SENSE(MAX)}$ vs. V_{ITH} in Burst Mode

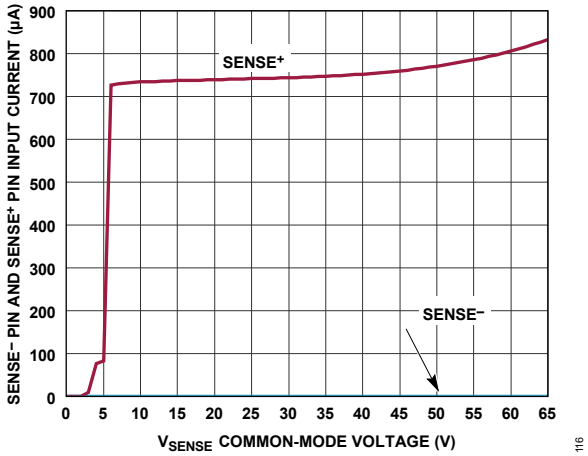


Figure 16. SENSE+ and SENSE- Pin Input Bias Current vs. V_{SENSE} Common-Mode Voltage

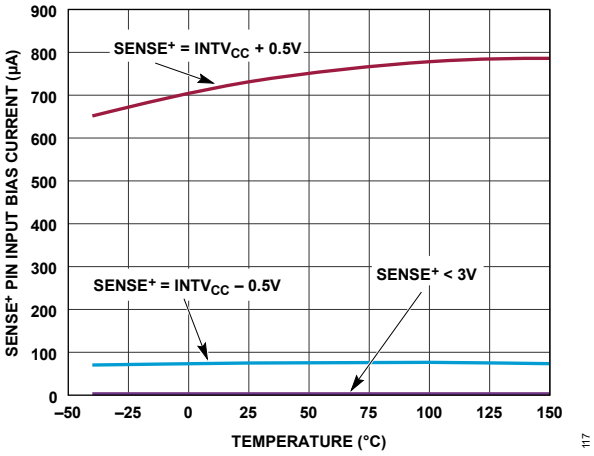


Figure 17. SENSE+ Pin Input Current vs. Temperature

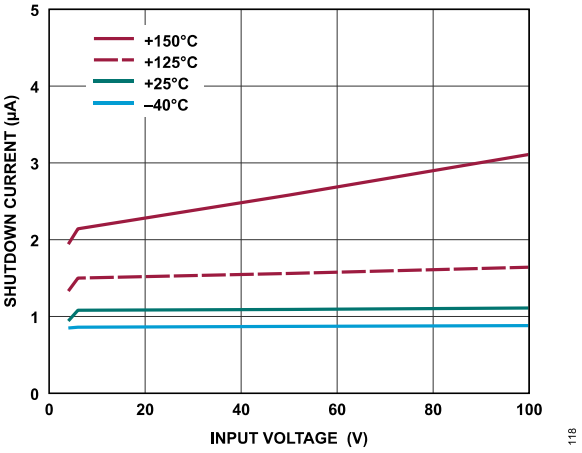


Figure 18. Shutdown Current vs. Input Voltage

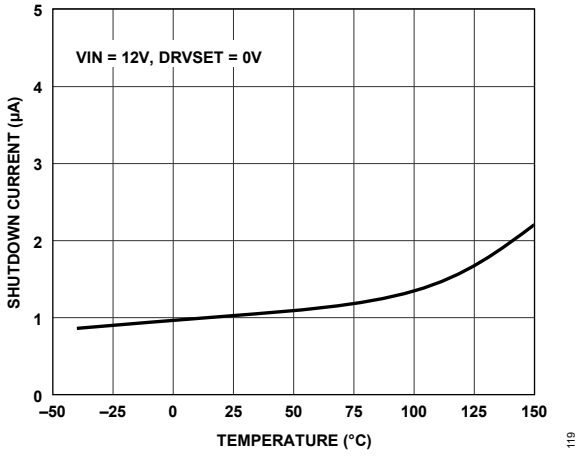


Figure 19. Shutdown Current vs. Temperature

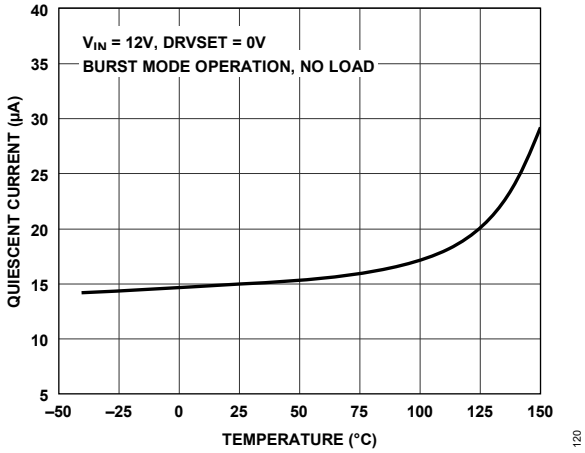


Figure 20. Quiescent Current vs. Temperature

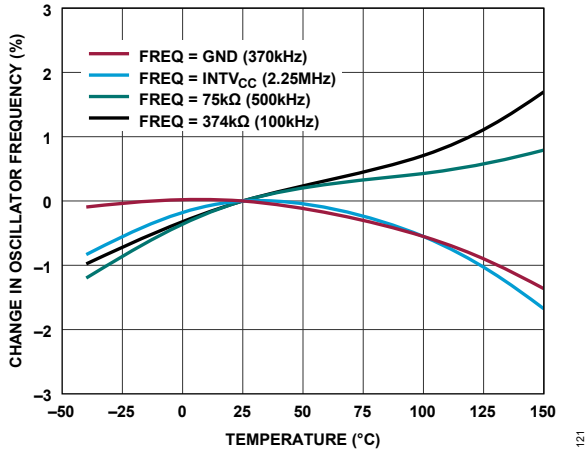


Figure 21. Oscillator Frequency vs. Temperature

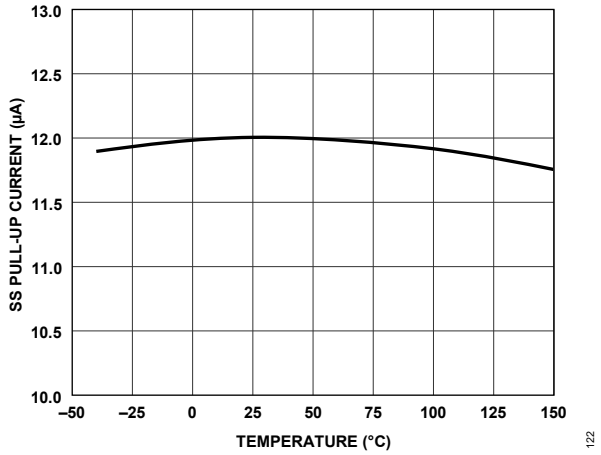


Figure 22. SS Pull-Up Current vs. Temperature

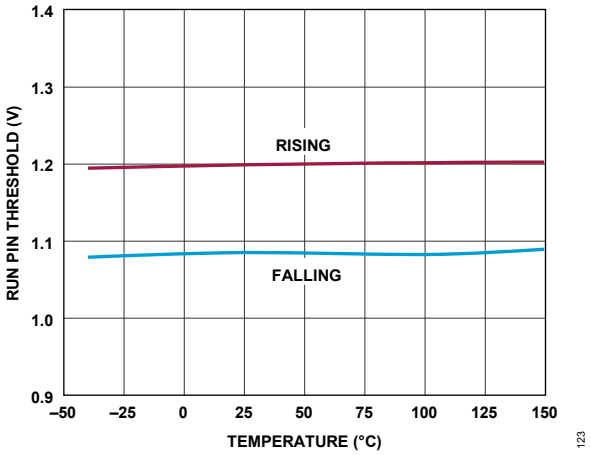


Figure 23. RUN Pin Threshold vs. Temperature

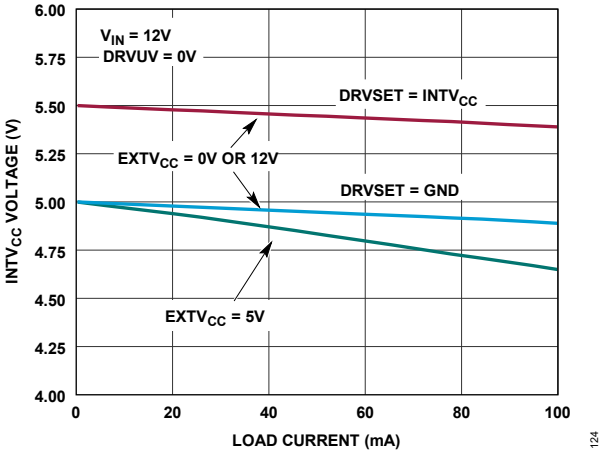


Figure 24. $INTV_{CC}$ Voltage vs. Load Current

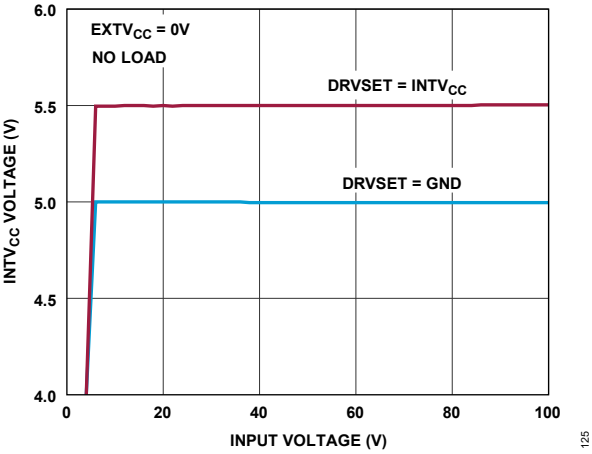


Figure 25. $INTV_{CC}$ Voltage vs. Input Voltage

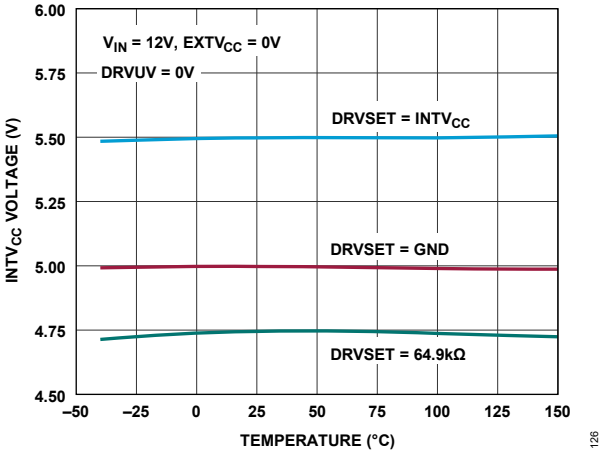


Figure 26. $INTV_{CC}$ Voltage vs. Temperature

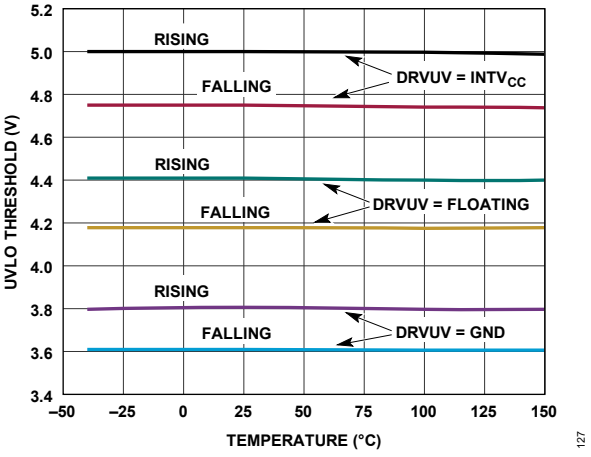


Figure 27. UVLO Threshold vs. Temperature

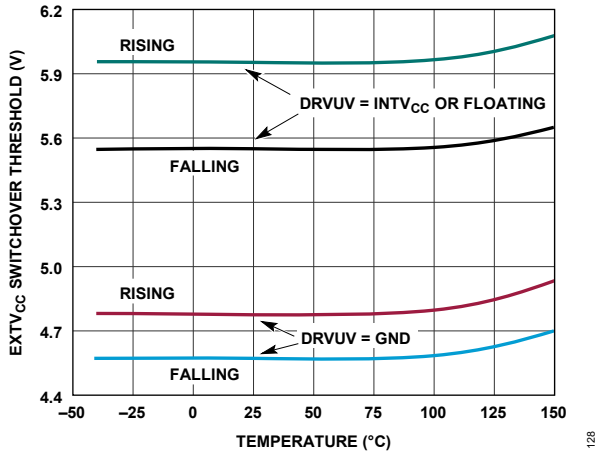


Figure 28. $EXTV_{CC}$ Switchover Threshold vs. Temperature

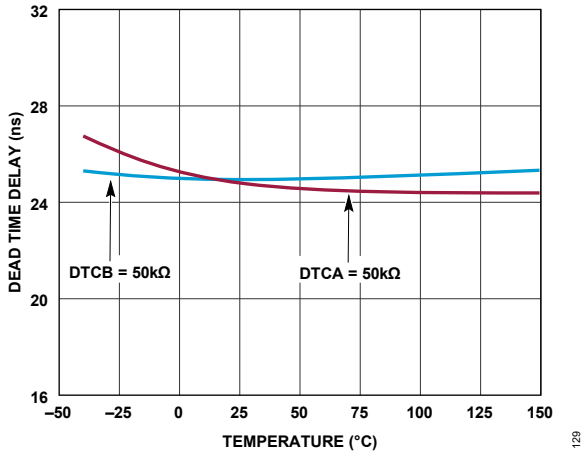


Figure 29. Dead Time Delay vs. Temperature

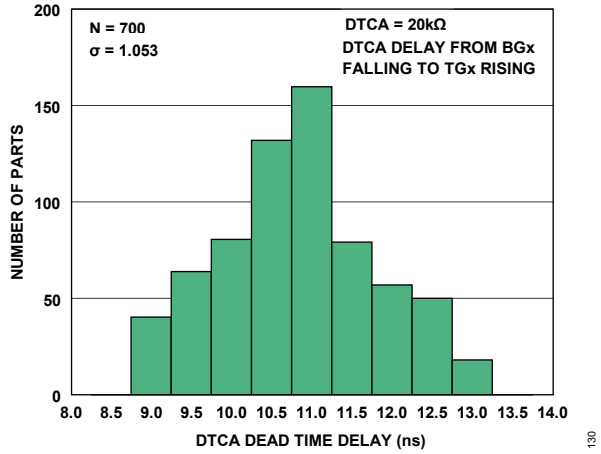


Figure 30. DTCA = 20kΩ Dead Time Delay Histogram

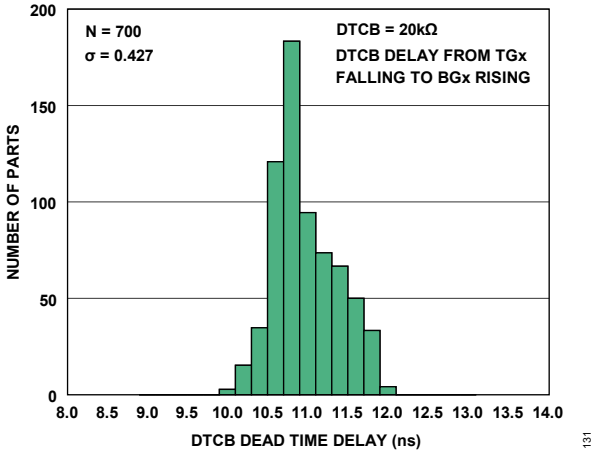


Figure 31. DTCB = 20kΩ Dead Time Delay Histogram

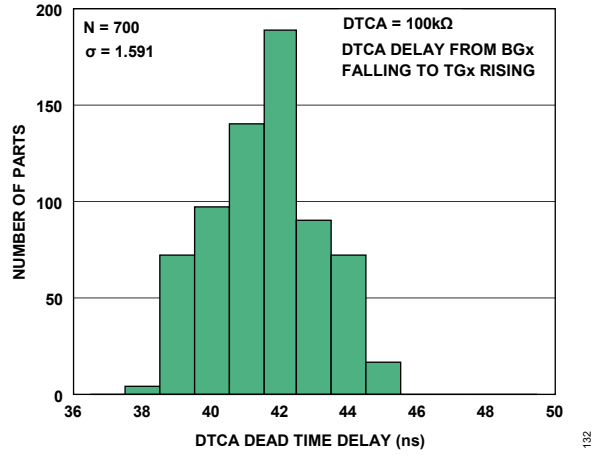


Figure 32. DTCA = 100kΩ Dead Time Delay Histogram

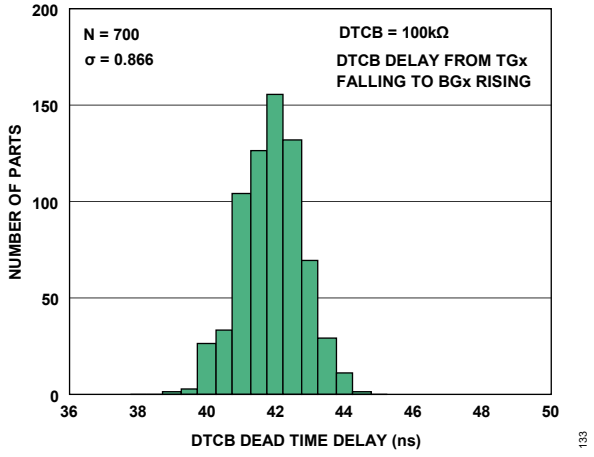
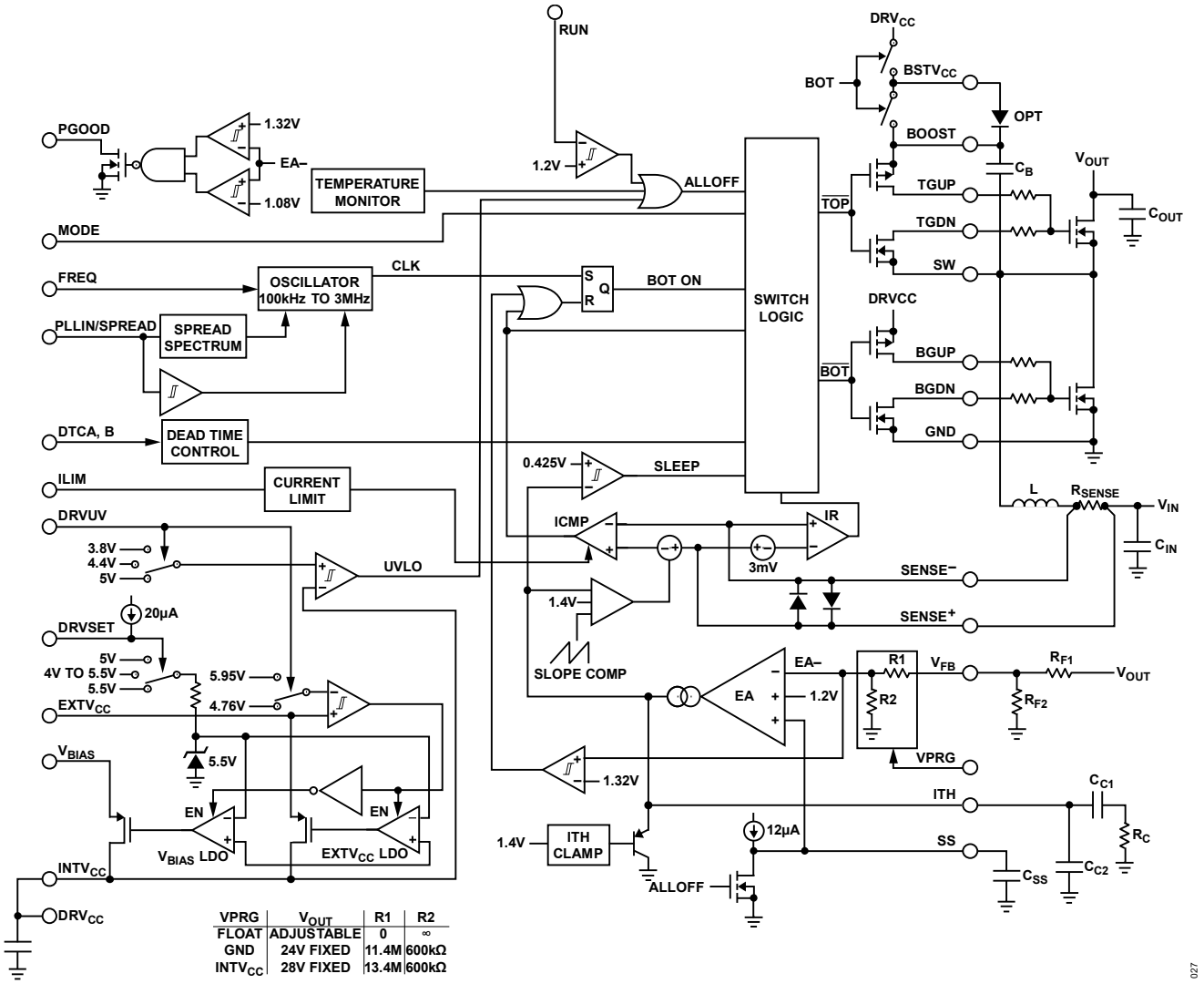


Figure 33. DTCB = 100kΩ Dead Time Delay Histogram

FUNCTIONAL DIAGRAM



VPRG	V_{OUT}	R1	R2
FLOAT	ADJUSTABLE	0	∞
GND	24V FIXED	11.4M	600kΩ
$INTV_{CC}$	28V FIXED	13.4M	600kΩ

Figure 34. Functional Diagram

THEORY OF OPERATION

Main Control Loop

The LTC7893 is a synchronous boost controller using a constant frequency, peak current mode architecture. During normal operation, the external bottom FET turns on when the clock sets the set/reset (SR) latch, causing the inductor current to increase. The main switch turns off when the main current comparator, ICMP, resets the SR latch. After the bottom FET is turned off each cycle, the top FET turns on, which causes the inductor current to decrease until either the inductor current starts to reverse, as indicated by the current comparator (IR), or the beginning of the next clock cycle.

The peak inductor current at which ICMP trips and resets the latch is controlled by the voltage on the ITH pin, which is the output of the error amplifier (EA). The error amplifier compares the output voltage feedback signal at the V_{FB} pin (which is generated with an external resistor divider connected across the output voltage, V_{OUT}, to GND) to the

internal 1.2V reference voltage. When the load current increases, it causes a slight decrease in V_{FB} relative to the reference, which causes the error amplifier to increase the ITH voltage until the average inductor current matches the new load current.

Power and Bias Supplies (V_{BIAS}, $EXTV_{CC}$, DRV_{CC}, and $INTV_{CC}$)

The $INTV_{CC}$ pin supplies power for the top and bottom FET drivers and most of the internal circuitry. The supply for the FET drivers is derived from the DRV_{CC} pin, which must be tied to the $INTV_{CC}$ pin to supply power to the gate drivers. Low-dropout linear regulators (LDOs) are available from both the V_{BIAS} and $EXTV_{CC}$ pins to provide power to $INTV_{CC}$, which can be programmed from 4V to 5.5V through control of the DRVSET pin. When the $EXTV_{CC}$ pin is tied to a voltage less than its switchover voltage, the V_{BIAS} LDO supplies power to $INTV_{CC}$. If $EXTV_{CC}$ is taken above its switchover voltage, the V_{BIAS} LDO regulator turns off and the $EXTV_{CC}$ LDO turns on. When enabled, the $EXTV_{CC}$ LDO regulator supplies power to $INTV_{CC}$. Using the $EXTV_{CC}$ pin allows the $INTV_{CC}$ power to be derived from a high efficiency external source.

High-Side Bootstrap Capacitor

Each top FET driver is biased from the floating bootstrap capacitor (C_B), which normally recharges through an internal switch between BOOST and DRV_{CC} whenever the bottom FET turns on. The internal switch becomes high impedance whenever the bottom FET is off, which prevents the bootstrap capacitor from overcharging whenever SW rings less than GND during the dead times.

If the input voltage increases to a voltage close to its output, the loop may enter dropout and attempt to turn on the top FET continuously. If the bottom FET is not turned on frequently enough to recharge the bootstrap capacitor, the top FET may not be fully enhanced or it may even be completely off when the controller attempts to turn on the top FET.

Dead Time Control (DTCA and DTCB Pins)

The LTC7893 dead time delays can be programmed from 7ns to 60ns by configuring the DTCA and DTCB pins. The DTCA pin programs the dead time associated with the bottom FET turning off and the top FET turning on (SW going from low to high). The DTCB pin programs the dead time associated with top FET turning off and the bottom FET turning on (SW going from high to low).

Tying the DTCA pin to ground programs adaptive dead time control, which means the driver logic waits for the bottom FET to turn off before turning on the top FET. Adaptive dead time control results in dead times of approximately 15ns between BGx falling to TGx rising. Placing a resistor between the DTCA pin and ground programs the open-loop delay between the bottom FET turning off and the top FET turning on. This delay can be programmed between 7ns and 60ns. See the *Dead Time Control (DTCA and DTCB Pins)* section for more information.

Tying the DTCB pin to ground programs adaptive dead time control, which means the driver logic waits for the top FET to turn off before turning on the bottom FET. Adaptive dead time control results in dead times of approximately 15ns between TG falling to BG rising. Placing a resistor between the DTCB pin and ground programs the open-loop delay between the top FET turning off and the bottom FET turning on. This delay can be programmed between 7ns and 60ns. See the *Dead Time Control (DTCA and DTCB Pins)* section for more information.

Startup and Shutdown (RUN and SS Pins)

The LTC7893 can be shut down using the RUN pin. Pulling RUN pin below 1.1V shuts down the main control loop. Pulling the RUN pin below 0.7V disables the controllers and most internal circuits, including the $INTV_{CC}$ LDO regulators. In this shutdown state, the LTC7893 draws only 1µA of current from V_{BIAS}.

The RUN pin needs to be externally pulled up or driven directly by logic. The RUN pin can tolerate up to 100V (absolute maximum). Therefore, the RUN pin can be tied to V_{IN} or V_{BIAS} in always on applications where the controller is enabled continuously and never shut down. Additionally, a resistive divider from V_{IN} to the RUN pin can be used to set a precise input undervoltage lockout so that the power supply does not operate below a user adjustable level.

The startup of the output voltage V_{OUT} is controlled by the voltage on the SS pin. When the voltage on the SS pin is less than the 1.2V internal reference voltage, the LTC7893 regulates the V_{FB} voltage to the SS pin voltage instead of the 1.2V reference voltage. This method allows the SS pin to be used as a soft start, which smoothly ramps the output voltage on startup. An external capacitor from the SS pin to GND is charged by an internal 12µA pull-up current, creating a voltage ramp on the SS pin. As the SS voltage rises linearly from 0V to 1.2V (and beyond), the output voltage V_{OUT} rises smoothly to its final value.

Light Load Operation: Burst Mode Operation, Pulse-Skipping, or Forced Continuous Mode (MODE Pin)

The LTC7893 can be set to enter high efficiency Burst Mode operation, constant frequency pulse-skipping mode, or forced continuous conduction mode at light load currents.

To select Burst Mode operation, tie the MODE pin to GND. To select forced continuous operation, tie the MODE pin to $INTV_{CC}$. To select pulse-skipping mode, tie the MODE pin to a dc voltage greater than 1.2V and less than $INTV_{CC}$ – 1.3V. An internal 100kΩ resistor to ground invokes Burst Mode operation when the MODE pin is floating, and pulse-skipping mode when the MODE pin is tied to $INTV_{CC}$ through an external 100kΩ resistor.

When the controller is enabled for Burst Mode operation, the minimum peak current in the inductor is set to approximately 25% of its maximum value, even though the voltage on the ITH pin may indicate a lower value. If the average inductor current is higher than the load current, the error amplifier decreases the voltage on the ITH pin. When the ITH voltage drops to less than 0.425V, the internal sleep signal goes high (enabling sleep mode) and both external FETs are turned off. The ITH pin is then disconnected from the output of the error amplifier and parked at 0.45V.

In sleep mode, much of the internal circuitry is turned off, reducing the quiescent current (I_Q) drawn by the LTC7893. In sleep mode, the LTC7893 draws only 15µA of I_Q.

In sleep mode, the load current is supplied by the output capacitor. As the output voltage decreases, the output of the error amplifier rises. When the output voltage drops enough, the ITH pin is reconnected to the output of the error amplifier, the sleep signal goes low, and the controller resumes normal operation by turning on the bottom FET on the next cycle of the internal oscillator.

When a controller is enabled for Burst Mode operation, the inductor current is not allowed to reverse. The reverse current comparator (IR) turns off the top FET just before the inductor current reaches zero, preventing it from reversing and going negative. Therefore, the controller operates in discontinuous operation.

In forced continuous operation, the inductor current is allowed to reverse at light loads or under large transient conditions. The peak inductor current is determined by the voltage on the ITH pin, just as in normal operation. In this mode, the efficiency at light loads is lower than in Burst Mode operation. However, continuous operation has the advantage of lower output voltage ripple and less interference to audio circuitry. In forced continuous mode, the output ripple is independent of the load current.

When the MODE pin is connected for pulse-skipping mode, the LTC7893 operates in pulse-width modulation (PWM) pulse-skipping mode at light loads. In this mode, constant frequency operation is maintained down to approximately 1% of the designed maximum output current. At light loads, ICMP can remain tripped for several cycles and force the

bottom FET to stay off for the same number of cycles (that is, skipping pulses). The inductor current is not allowed to reverse (discontinuous operation). This mode, like forced continuous operation, exhibits low output ripple as well as low audio noise and reduced R_F interference, as compared to Burst Mode operation. Pulse-skipping mode provides higher low current efficiency than forced continuous mode, but not nearly as high as Burst Mode operation.

Unlike forced continuous mode and pulse-skipping mode, Burst Mode operation cannot be synchronized to an external clock. Therefore, if Burst Mode operation is selected and the switching frequency is synchronized to an external clock applied to the PLLIN/SPREAD pin, the LTC7893 switches from Burst Mode operation to forced continuous mode.

Frequency Selection, Spread Spectrum, and Phase-Locked Loop (FREQ and PLLIN/SPREAD Pins)

The free running switching frequency of the LTC7893 controller is selected using the FREQ pin. Tying FREQ to GND selects 370kHz whereas tying FREQ to $INTV_{CC}$ selects 2.25MHz. Placing a resistor between FREQ and GND allows the frequency to be programmed between 100kHz and 3MHz.

Switching regulators can be particularly troublesome for applications where electromagnetic interference (EMI) is a concern. To improve EMI, the LTC7893 can operate in spread spectrum mode, which is enabled by tying the PLLIN/SPREAD pin to $INTV_{CC}$. This feature varies the switching frequency within typical boundaries of the frequency set by the FREQ pin and +20%.

A phase-locked loop (PLL) is available on the LTC7893 to synchronize the internal oscillator to an external clock source connected to the PLLIN/SPREAD pin. The PLL of the LTC7893 aligns the turn-on of the external bottom FET to the rising edge of the synchronizing signal.

The PLL frequency is prebiased to the free running frequency set by the FREQ pin before the external clock is applied. If prebiased near the external clock frequency, the PLL only needs to make slight changes in order to synchronize the rising edge of the external clock to the rising edge of BGDN. For more rapid lock in to the external clock, use the FREQ pin to set the internal oscillator to approximately the frequency of the external clock. The PLL of the LTC7893 is guaranteed to lock to an external clock source whose frequency is between 100kHz and 3MHz.

The PLLIN/SPREAD pin is transistor-transistor logic (TTL)-compatible with thresholds of 1.6V (rising) and 1.1V (falling), and this pin is guaranteed to operate with a clock signal swing of 0.5V to 2.2V.

Output Overvoltage Protection

The LTC7893 has an overvoltage comparator that guards against transient overshoots as well as other more serious conditions that can cause output overvoltage. When the V_{FB} pin rises above 10% above its regulation point of 1.2V, the bottom FET turns off and the inductor current is not allowed to reverse.

Power Good

The LTC7893 has a PGOOD pin that is connected to an open drain of an internal N-channel MOSFET. The MOSFET turns on and pulls the PGOOD pin low when the V_{FB} voltage is not within ±10% of the 1.2V reference. The PGOOD pin is also pulled low when the RUN pin is low (shut down). When the V_{FB} voltage is within the ±10% requirement, the MOSFET turns off and the PGOOD pin is allowed to be pulled up by an external resistor to a source no greater than 6V, such as $INTV_{CC}$.

APPLICATIONS INFORMATION

Figure 1 is a basic LTC7893 application circuit. External component selection is largely driven by the load requirement and begins with the selection of the inductor, current sense components, operating frequency, and light load operating mode. The remaining power stage components, consisting of the input and output capacitors, and power FETs can then be chosen. Next, feedback resistors are selected to set the desired output voltage. Then, the remaining external components are selected, such as for soft-start, biasing, and loop compensation.

Inductor Value Calculation

The operating frequency and inductor selection are interrelated in that higher operating frequencies allow the use of smaller inductor and capacitor values. A higher frequency generally results in lower efficiency because of FET switching and gate charge losses. In addition to this trade-off, the effect of the inductor value on the ripple current and low current operation must also be considered. The inductor value has a direct effect on ripple current.

The maximum average inductor current ($I_{L(MAX)}$) in continuous conduction mode is equal to the maximum average output current ($I_{OUT(MAX)}$) multiplied by a factor of V_{OUT}/V_{IN}, or $I_{L(MAX)} = I_{OUT(MAX)} \bullet V_{OUT}/V_{IN}$. Be aware that the maximum output current decreases with decreasing V_{IN}. The choice of $I_{L(MAX)}$ therefore depends on the maximum load current for a regulated V_{OUT} at the minimum normal operating V_{IN}. If the load current for a given V_{IN} is exceeded, V_{OUT} will decrease until the $I_{L(MAX)} = I_{OUT(MAX)} \bullet V_{OUT}/V_{IN}$ equation is satisfied.

The inductor ripple current (ΔI_L) for a boost converter is given by Equation 1:

$$\Delta I_L = \frac{1}{f \bullet L} V_{IN} \left(1 - \frac{V_{IN}}{V_{OUT}}\right) \quad (1)$$

Accepting larger values of ΔI_L allows the use of low inductances, but results in higher output voltage ripple and greater core losses. A reasonable starting point for setting ripple current is $\Delta I_L = 0.3 \bullet I_{L(MAX)}$. The maximum ΔI_L for a boost converter occurs at $V_{IN} = 1/2\ V_{OUT}$.

The inductor value also has secondary effects. The transition to Burst Mode operation begins when the average inductor current required results in a peak current below 25% of the current limit determined by R_{SENSE}. Lower inductor values (higher ΔI_L) cause this transition to occur at lower load currents, which can cause a dip in efficiency in the upper range of low current operation. In Burst Mode operation, lower inductance values cause the burst frequency to decrease.

Inductor Core Selection

When the value for L is known, select the type of inductor. High efficiency regulators generally cannot afford the core loss found in low cost powdered iron cores, forcing the use of more expensive ferrite or molypermalloy cores. Actual core loss is independent of core size for a fixed inductor value, but it is dependent on the inductance value selected. As inductance increases, core losses decrease. However, because increased inductance requires more turns of wire, copper losses increase.

Ferrite designs have very low core loss and are preferred for high switching frequencies. Therefore, design goals can concentrate on copper loss and preventing saturation. Ferrite core material saturates hard, which means that inductance collapses abruptly when the peak design current is exceeded. This collapse results in an abrupt increase in inductor ripple current and consequent output voltage ripple. Do not allow the core to saturate.

Current Sense Selection

The LTC7893 can be configured to use either inductor dc resistance (DCR) sensing or low value resistor sensing. The choice between the two current sensing schemes is a design trade-off between cost, power consumption, and accuracy. DCR sensing is popular because it saves on expensive current sensing resistors and is more power efficient, particularly in high current applications. However, current sensing resistors provide the most accurate current limits for the controller. The selection of other external components begins with the selection of R_{SENSE} (if R_{SENSE} is used) and the inductor value.

The $SENSE^+$ and $SENSE^-$ pins are the inputs to the current comparator. The common-mode voltage range on these pins is 0V to 65V (the absolute maximum), allowing the LTC7893 to operate from inputs over this full range. The $SENSE^-$ pin is high impedance, drawing less than ≈1µA. This high impedance allows the current comparator to be used in inductor DCR sensing.

The impedance of the $SENSE^+$ pin changes depending on the common-mode voltage. When less than $INTV_{CC}$ – 0.5V, the $SENSE^+$ pin is relatively high impedance, drawing ≈ 75µA from $SENSE^+$. When the $SENSE^+$ pin is more than $INTV_{CC}$ + 0.5V, a higher current (≈700µA) flows into the $SENSE^+$ pin. Between $INTV_{CC}$ – 0.5V and $INTV_{CC}$ + 0.5V, the current transitions from the smaller current to the higher current. The $SENSE^+$ pin has an additional ≈ 75µA current when its voltage is above 3.2V to bias internal circuitry from V_{IN} instead of V_{BIAS}, which reduces the input referred supply current.

Filter components mutual to the sense lines must be placed close to the LTC7893, and the sense lines must run close together to a Kelvin connection underneath the current sense element (shown in *Figure 35*). Sensing current elsewhere can effectively add parasitic inductance and capacitance to the current sense element, degrading the information at the sense terminals and making the programmed current limit unpredictable. If DCR sensing is used (see *Figure 37*), the R1 resistor must be placed close to the switching node to prevent noise from coupling into sensitive small signal nodes.

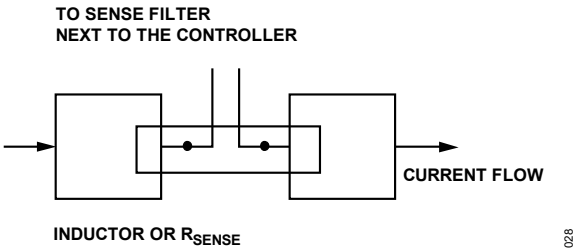


Figure 35. Sense Lines Placement with Inductor or Sense Resistor

Low Value Resistor Current Sensing

Figure 36 shows a typical sensing circuit using a discrete resistor. R_{SENSE} is chosen based on the required output current. The current comparator has a maximum threshold $V_{SENSE(MAX)}$ of 50mV, 25mV, or 75mV, as determined by the state of the of the ILIM pin. The current comparator threshold voltage sets the peak inductor current.

Using the maximum inductor current ($I_{L(MAX)}$) and ripple current (ΔI_L) (as described in the *Inductor Value Calculation* section), the target sense resistor value is given by Equation 2, as follows:

$$R_{SENSE} = \frac{V_{SENSE(MAX)}}{I_{L(MAX)} + \frac{\Delta I_L}{2}} \quad (2)$$

To ensure that the application delivers full load current over the full operating temperature range, choose the minimum value for $V_{SENSE(MAX)}$ in *Table 1*.

The parasitic inductance (ESL) of the sense resistor introduces significant error in the current sense signal for lower inductor value (<3µH) or higher current (>5A) applications. This error is proportional to the input voltage and can degrade line regulation or cause loop instability. Placing an RC filter (filter resistor, R_F and filter capacitor, C_F) into the SENSE$^+$ and SENSE$^-$ pins, as shown in *Figure 36*, can be used to compensate for this error. For optimal cancellation of the ESL, set the RC filter time constant to $R_F \times C_F = ESL/R_{SENSE}$. In general, select C_F to be in the range of 1nF to 10nF and calculate the corresponding R_F. Surface-mount sense resistors in low ESL, wide footprint geometries are recommended to minimize this error. If not specified in the data sheet of the manufacturer, the ESL can be approximated as 0.4nH for a resistor with a 1206 footprint and 0.2nH for a resistor with a 1225 footprint.

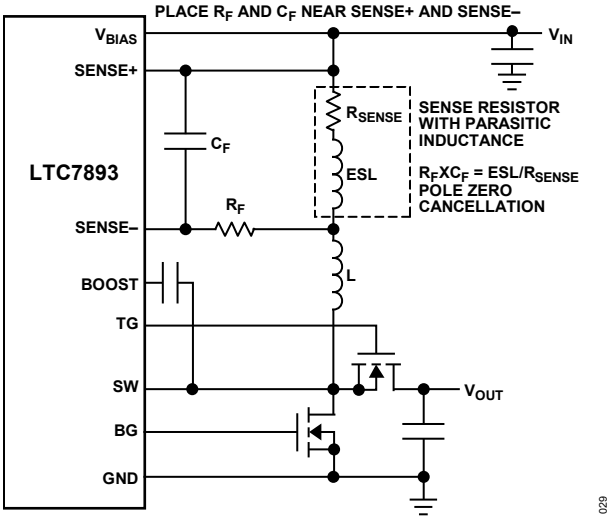


Figure 36. Using a Resistor to Sense Current

Inductor DCR Current Sensing

For applications requiring the highest possible efficiency at high load currents, the LTC7893 is capable of sensing the voltage drop across the inductor DCR, as shown in *Figure 37*. The DCR of the inductor represents the small amount of dc winding resistance of the copper, which can be less than 1mΩ for low value, high current inductors. In a high current application requiring such an inductor, power loss through a sense resistor costs several points of efficiency compared to inductor DCR sensing.

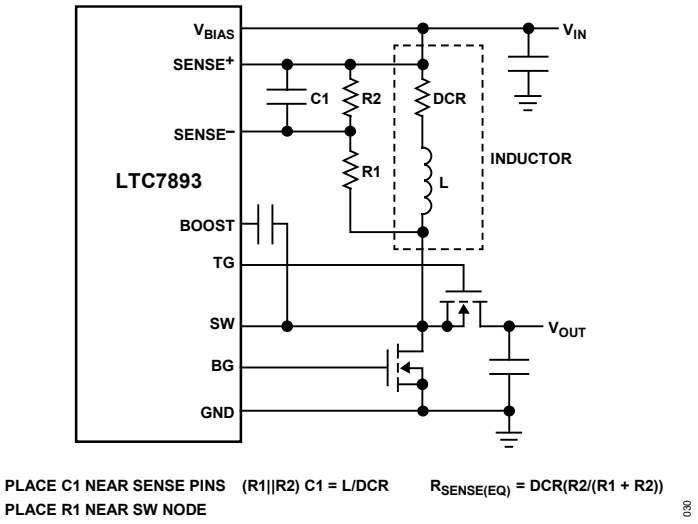


Figure 37. Using the Inductor DCR to Sense Current ($R_{SENSE(EQUIV)}$ is the Equivalent Sensed Resistance)

If the external (R1||R2) × C1 time constant is chosen to be equal to the L/DCR time constant, the voltage drop across the external capacitor is equal to the drop across the inductor DCR multiplied by R2/(R1+R2). R2 scales the voltage across the sense terminals for applications where the DCR is greater than the target sense resistor value. To properly dimension the external filter components, the DCR of the inductor must be known. The DCR can be measured using an inductance, capacitance, and resistance (LCR) meter. However, the DCR tolerance is not always the same and varies with temperature. Consult the data sheet of the manufacturer for more information.

Using $I_{L(MAX)}$ and ΔI_L (as described in the *Inductor Value Calculation* section), the target sense resistor value is given by Equation 3, as follows:

$$R_{SENSE(EQUIV)} = \frac{V_{SENSE(MAX)}}{I_{L(MAX)} + \frac{\Delta I_L}{2}} \quad (3)$$

To ensure that the application delivers full load current over the full operating temperature range, choose the minimum value for $V_{SENSE(MAX)}$ in *Table 1*.

Next, determine the DCR of the inductor. When provided, use the maximum value noted by the manufacturer, typically given at 20°C. Increase this value to account for the temperature coefficient of copper resistance, which is approximately 0.4%/°C. A conservative value for the maximum inductor temperature ($T_{L(MAX)}$) is 100°C. To scale the maximum inductor DCR (DCR_{MAX}) to the desired sense resistor value (R_D), use the divider ratio given by Equation 4, as follows:

$$R_D = \frac{R_{SENSE(EQUIV)}}{DCR_{MAX} \text{ at } T_{L(MAX)}} \quad (4)$$

C1 is typically selected to be in the range of 0.1µF to 0.47µF. This range forces the equivalent resistance (R1||R2) to around 2kΩ, reducing the error that can result from the ≈1µA current of the $SENSE^-$ pin.

R1||R2 is scaled to the room temperature inductance and maximum DCR given by Equation 5, as follows:

$$R1 \parallel R2 = \frac{L}{(DCR \text{ at } 20°C) \bullet C1} \quad (5)$$

The sense resistor values are given by Equation 6 and Equation 7, as follow:

$$R1 = \frac{R1 \parallel R2}{R_D} \quad (6)$$

$$R2 = \frac{R1 \times R_D}{1 - R_D} \quad (7)$$

The maximum power loss (P_{LOSS}) in R1 is related to duty cycle and occurs in continuous mode at V_{IN} = 1/2 V_{OUT} given by Equation 8, as follows:

$$P_{LOSS} \text{ in } R1 = \frac{(V_{OUT} - V_{IN}) \times V_{IN}}{R1} \quad (8)$$

Ensure that R1 has a power rating higher than P_{LOSS} in R1. If high efficiency is necessary at light loads, consider this power loss when deciding whether to use DCR sensing or sense resistors. Light load power loss can be modestly higher with a DCR network than with a sense resistor due to the extra switching losses incurred through R1. However, DCR sensing eliminates a sense resistor, reduces conduction losses, and provides higher efficiency at heavy loads. Peak efficiency is about the same with either method.

Setting the Operating Frequency

Selecting the operating frequency is a trade-off between efficiency and component size. High frequency operation allows the use of smaller inductor and capacitor values. Operation at lower frequencies improves efficiency by reducing gate charge and transition losses but requires larger inductance values and/or more output capacitance to maintain low output ripple voltage.

In higher voltage applications, transition losses contribute more significantly to power loss, and a proper balance between size and efficiency is achieved with a switching frequency between 300kHz and 900kHz. Lower voltage applications benefit from lower switching losses and can operate at switching frequencies up to 3MHz, if desired. The switching frequency is set using the FREQ and PLLIN/SPREAD pins, as shown in *Table 4*.

Table 4. Setting the Switching Frequency Using FREQ and PLLIN/SPREAD

FREQ PIN	PLLIN/SPREAD PIN	FREQUENCY
0V	0V	370kHz
$INTV_{CC}$	0V	2.25MHz
Resistor to GND	0V	100kHz to 3MHz
Any of the Above	External Clock, 100kHz to 3MHz	Phase-locked to external clock
Any of the Above	$INTV_{CC}$	Spread spectrum f_{OSC} modulated 0% to +20%

Tying the FREQ pin to ground selects 370kHz, whereas tying FREQ to $INTV_{CC}$ selects 2.25MHz. Placing a resistor between FREQ and ground allows the frequency to be programmed anywhere between 100kHz and 3MHz. Choose a FREQ pin resistor (R_{FREQ}) from *Figure 38* or Equation 9, as follows:

$$R_{FREQ}(\text{in k}\Omega) = \frac{37\text{MHz}}{f_{osc}} \quad (9)$$

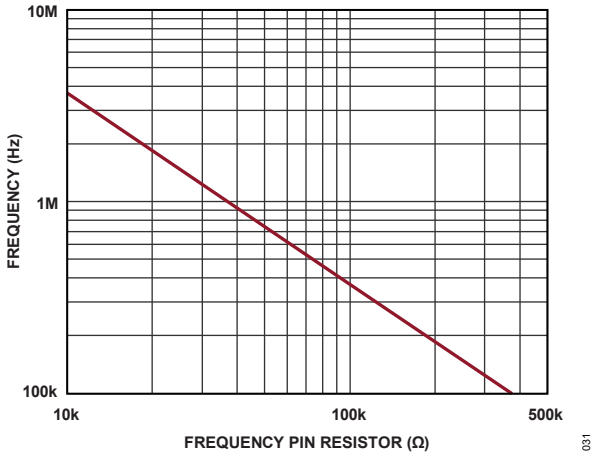


Figure 38. Relationship Between Oscillator Frequency and Resistor Value at the FREQ Pin

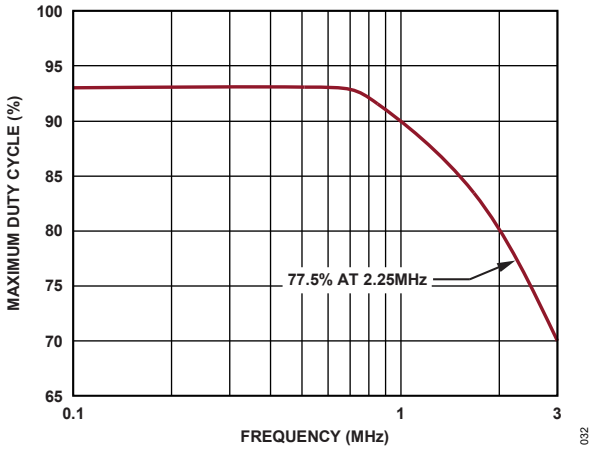


Figure 39. Relationship Between Maximum Duty Cycle and Operating Frequency

A further constraint on the operating frequency is the maximum duty cycle of the boost converter. Maximum duty cycle (DC_{MAX}) is limited, as shown in *Figure 39*, and can be approximated as $DC_{MAX} = (1 - V_{IN(MIN)}/V_{OUT}) \times 100\%$. If the duty cycle is greater than DC_{MAX}, the output can lose regulation and may not maintain constant frequency operation. An operation frequency must be selected so that the boost converter duty cycle is less than DC_{MAX}.

To improve electromagnetic interference (EMI) performance, spread spectrum mode can be selected by tying the PLLIN/SPREAD pin to $INTV_{CC}$. When spread spectrum mode is enabled, the switching frequency modulates within the frequency selected by the FREQ pin and +20%. Spread spectrum mode may be used in any operating mode selected by the MODE pin (Burst Mode, pulse-skipping, or forced continuous mode).

A PLL is also available on the LTC7893 to synchronize the internal oscillator to an external clock source connected to the PLLIN/SPREAD pin. After the PLL locks, the BGDN is synchronized to the rising edge of the external clock signal. See the *Phase-Locked Loop and Frequency Synchronization* section for details.

Selecting the Light-Load Operating Mode

The LTC7893 can be set to enter high efficiency Burst Mode operation, constant frequency pulse-skipping mode or forced continuous conduction mode at light load currents. To select Burst Mode operation, tie the MODE pin to GND. To select forced continuous operation, tie the MODE pin to $INTV_{CC}$. To select pulse-skipping mode, tie the MODE pin to $INTV_{CC}$ through a 100kΩ resistor. An internal 100kΩ resistor from the MODE pin to ground selects Burst Mode if the pin is floating. When synchronized to an external clock through the PLLIN/SPREAD pin, the LTC7893 operates in pulse-skipping mode if it is selected. Otherwise, the LTC7893 operates in forced continuous mode. *Table 5* summarizes the use of the MODE pin to select the light load operating mode.

Table 5. Using the MODE Pin to Select Light Load Operating Mode

MODE PIN	LIGHT-LOAD OPERATING MODE	MODE WHEN SYNCHRONIZED
0V or Floating	Burst Mode	Forced Continuous
100kΩ to $INTV_{CC}$	Pulse-Skipping	Pulse-Skipping
$INTV_{CC}$	Forced Continuous	Forced Continuous

The requirements of each application dictate the appropriate choice for light load operating mode. In Burst Mode operation, the inductor current is not allowed to reverse. The reverse current comparator turns off the top FET before the inductor current reaches zero, preventing it from reversing and going negative. Therefore, the regulator operates in discontinuous operation. In addition, when the load current is light, the inductor current begins bursting at frequencies lower than the switching frequency and enters a low current sleep mode when not switching. As a result, Burst Mode operation has the highest possible efficiency at light load.

In forced continuous mode, the inductor current is allowed to reverse at light loads and switches at the same frequency regardless of load. In this mode, the efficiency at light loads is considerably lower than in Burst Mode operation. However, continuous operation has the advantage of lower output voltage ripple and less interference to audio circuitry. In forced continuous mode, the output ripple is independent of the load current.

In pulse-skipping mode, constant frequency operation is maintained down to approximately 1% of designed maximum output current. At very light loads, the PWM comparator can remain tripped for several cycles and force the bottom FET to remain off for the same number of cycles (that is, skipping pulses). The inductor current is not allowed to reverse (discontinuous operation). This mode, like forced continuous operation, exhibits low output ripple as well as low audio noise and reduced R_F interference as compared to Burst Mode operation. Pulse-skipping mode provides higher light load efficiency than forced continuous mode but not nearly as high as Burst Mode operation. Consequently, pulse-skipping mode represents a compromise between light load efficiency, output ripple, and EMI.

In some applications, it can be desirable to change light load operating mode based on the conditions present in the system. For example, if a system is inactive, the user can select high efficiency Burst Mode operation by keeping the MODE pin set to 0V. When the system wakes, the user can send an external clock to PLLIN/SPREAD or tie MODE to $INTV_{CC}$ to switch to low noise forced continuous mode. These types of mode changes can allow an individual application to benefit from the advantages of each light load operating mode.

Dead Time Control (DTCA and DTCB Pins)

The dead time delays of the LTC7893 can be adjusted from 7ns to 60ns by configuring the DTCA and DTCB pins. See *Figure 40* and *Figure 41*, which show the TG minus SW and BG waveforms for each DTCx pin setting. In the *DTCx Pin Tied to Ground (Adaptive Dead Time Control)* and *DTCx Pin connected with a resistor to GND* sections, TG represents the voltage sensed at the top FET gate (the threshold for TG falling is sensed at the TGUP pin), and BG represents the voltage sensed at the bottom FET (the thresholds for BG rising and falling are sensed at the BGDN and BGUP pins, respectively). The DTCA pin programs the dead time associated with the bottom FET turning off and the top FET turning on (SW transitioning low to high). The DTCB pin programs the dead time associated with top FET turning off and the bottom FET turning on (SW transitioning from high to low).

DTCx Pin Tied to Ground (Adaptive Dead Time Control)

Tying the DTCA and DTCB pins to GND programs adaptive dead time control. In adaptive control (see *Figure 40*), the dead time is measured between one FET turning off and the other FET turning on. Tying the DTCA pin to GND fixes the delay between BG falling and TG minus SW rising to approximately 15ns. Tying the DTCB pin to GND fixes the delay between TG minus SW falling and BG rising to approximately 15ns.

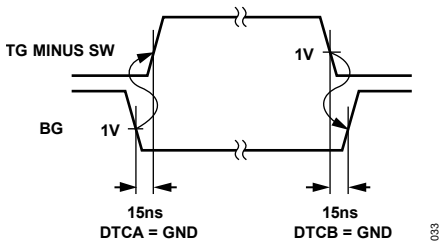


Figure 40. DTCx Pins Tied to GND–Adaptive Dead Time Control

DTCx Pin connected with a resistor to GND

Connecting a resistor between the DTCx pin and GND programs an open-loop dead time delay from 7ns to 60ns between the TG minus SW and BG edges (see *Figure 41*). A resistor tied to the DTCA pin programs an open-loop delay between BG falling and TG minus SW rising. A resistor tied to the DTCB pin and GND programs an open-loop delay between TG minus SW falling and BG rising. *Figure 42* shows the relationship between the DTCx pin resistor value and the programmed delay between TG minus SW and BG edges. This resistor must not be less than 10kΩ or more than 200kΩ.

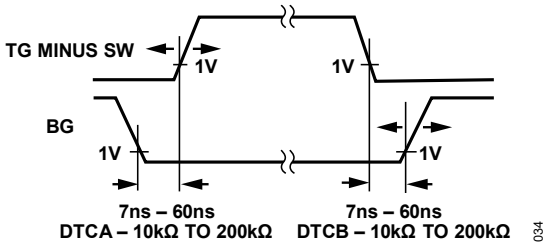


Figure 41. DTCx Pins with Resistor to GND–Adjustable Dead Time Control (non-Adaptive)

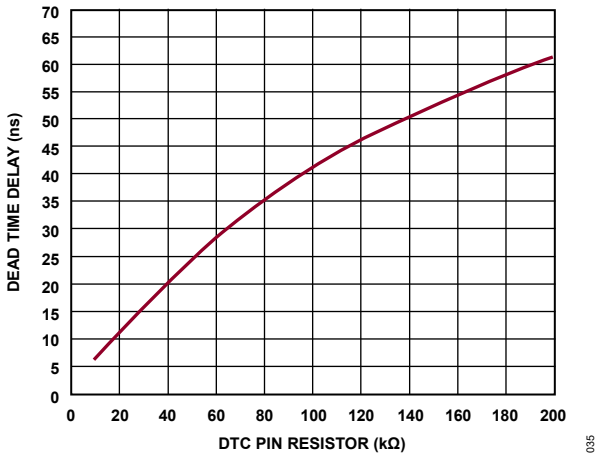


Figure 42. Relationship Between Dead Time Delay and Resistor Value at the DTCx Pin

If one of the DTCx pins is programmed with a resistor, the other DTCx pin must be programmed with a resistor for proper dead time control operation. Unexpected dead time delays can result if one DTCx pin is programmed with a resistor, while the other DTCx pin is tied to GND. The DTCx pins should only be connected to GND or a resistor tied to GND.

Power FET Selection

Two external power FETs must be selected for each controller in the LTC7893: one N-channel FET for the bottom (main) switch and one N-channel FET for the top (synchronous) switch. The peak-to-peak gate drive levels are set by the $INTV_{CC}$ regulation point (4V to 5.5V). Most GaN FETs can be driven comfortably within this $INTV_{CC}$ regulation window. If using silicon MOSFETs, logic level threshold MOSFETs must be used in most applications. Pay close attention to the BV_{DSS} specification for the FETs as well.

Selection criteria for the power FETs include the on resistance ($R_{DS(ON)}$), Miller capacitance (C_{MILLER}), input voltage, and maximum output current. C_{MILLER}, can be approximated from the gate charge curve typically provided in the datasheet of the FET manufacturer. C_{MILLER} is equal to the increase in gate charge along the horizontal axis while the curve is approximately flat divided by the specified change in the voltage difference between the drain and source terminals of the FET (V_{DS}). This result is then multiplied by the ratio of the application applied V_{DS} to the gate charge curve specified V_{DS}. When the IC is operating in continuous mode, the duty cycles for the top and bottom FETs are given by Equation 10 and Equation 11, as follows:

$$\text{Main Switch Duty Cycle} = \frac{V_{OUT}-V_{IN}}{V_{OUT}} \quad (10)$$

$$\text{Synchronous Switch Duty Cycle} = \frac{V_{IN}}{V_{OUT}} \quad (11)$$

The FET power dissipation at maximum output current is given by Equation 12 and Equation 13, as follows:

$$P_{MAIN} = \frac{(V_{OUT}-V_{IN})V_{OUT}}{V_{IN}^2}(I_{OUT(MAX)})^2 \bullet (1+\delta)R_{DS(ON)} + \left(\frac{V_{OUT}^3}{V_{IN}}\right)\left(\frac{I_{OUT(MAX)}}{2}\right) \bullet (R_{DR})(C_{MILLER}) \bullet \left[\frac{1}{V_{INTVCC}-V_{THMIN}} + \frac{1}{V_{THMIN}}\right](f) \quad (12)$$

$$P_{SYNC} = \frac{V_{OUT}}{V_{IN}}\left(I_{OUT(MAX)}\right)^2(1+\delta)R_{DS(ON)} \quad (13)$$

where:

P_{MAIN} is the power dissipation from the main switch
δ is the temperature dependency of $R_{DS(ON)}$ ($\delta \approx 0.005/°C$).
R_{DR} is the effective driver resistance at the FET's Miller threshold voltage ($R_{DR} \approx 2\Omega$).
V_{INTVCC} is the $INTV_{CC}$ voltage.
V_{THMIN} is the typical FET minimum threshold voltage.
P_{SYNC} is the power dissipation from the synchronous switch.

Both FETs have I^2R losses (I^2R is the power loss equation of the FETs when on in steady state), whereas the main N-channel equations include an additional term for transition losses, which are highest at low input voltages. For high input voltages, the high current efficiency generally improves with larger FETs. However, for low input voltages the transition losses rapidly increase to the point that the use of a higher $R_{DS(ON)}$ device with lower C_{MILLER} provides higher efficiency. The synchronous FET losses are greatest at high input voltages when the bottom switch duty factor is low.

C_{IN} and C_{OUT} Selection

The input ripple current in a boost converter is relatively low (compared to the output ripple current) because the input current is continuous. The boost converter input capacitor (C_{IN}) voltage rating should exceed the maximum input voltage. Although ceramic capacitors are tolerant of overvoltage conditions, aluminum electrolytic capacitors are not. Be sure to characterize the input voltage for any possible overvoltage transients that could apply excess stress to the input capacitors.

The value of C_{IN} is a function of the source impedance, and in general, the higher the source impedance, the higher the required input capacitance. The required amount of input capacitance is also greatly affected by the duty cycle. High output current applications that also experience high duty cycles can place great demands on the input supply, both in terms of dc current and ripple current.

The selection of the output capacitance (C_{OUT}) is driven by the output voltage ripple (V_{RIPPLE}) requirement. The output current in a boost converter is discontinuous; therefore, both the effects of equivalent series resistance (ESR) and the bulk capacitance must be considered when choosing C_{OUT}. V_{RIPPLE} due to charging and discharging the bulk capacitance of C_{OUT} is given by Equation 14, as follows:

$$V_{RIPPLE} = \frac{I_{OUT(MAX)} \bullet (V_{OUT} - V_{IN(MIN)})}{C_{OUT} \bullet V_{OUT} \bullet f} \quad (14)$$

The ripple due to the voltage drop across the ESR (ΔV_{ESR}) for C_{OUT} is given by Equation 15, as follows:

$$\Delta V_{ESR} = \left(I_{L(MAX)} + \frac{1}{2}\Delta I_L\right) \bullet ESR \quad (15)$$

Where:

ΔI_L is the ripple current in the inductor.
$I_{L(MAX)}$ is the maximum average inductor current.
$I_{OUT(MAX)}$ is the maximum average output current.
f is the operating frequency.

Multiple capacitors placed in parallel may be needed to meet the ESR and RMS current handling requirements. Dry tantalum, special polymer, aluminum electrolytic, and ceramic capacitors are all available in surface mount packages. Ceramic capacitors have excellent low ESR characteristics but can have a high voltage coefficient. Low ESR and high ripple current rated capacitors such as OS-CON and POSCAP are available.

Setting the Output Voltage

The LTC7893 output voltages are set by an external feedback resistor divider carefully placed across the output, as shown in *Figure 43* and *Figure 44*. The regulated output voltage is determined by Equation 16, as follows:

$$V_{OUT} = 1.2V(1 + \frac{R_B}{R_A}) \quad (16)$$

Place the R_A and R_B resistors close to the V_{FB} pin to minimize PCB trace length and noise on the sensitive V_{FB} node. Take care to route the V_{FB} trace away from noise sources, such as the inductor or the SW trace. To improve frequency response, a feedforward capacitor (C_{FF}) can be used.

The LTC7893 can be programmed to a fixed 28V or 24V output through control of the VPRG pin. *Figure 44* shows how the V_{FB} pin is used to sense the output voltage in fixed output mode. Tying VPRG to $INTV_{CC}$ or GND programs V_{OUT} to 28V or 24V, respectively. Floating VPRG sets V_{OUT} to adjustable output mode using external resistors.

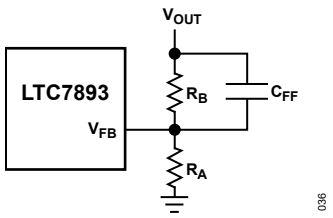


Figure 43. Setting Adjustable Output Voltage

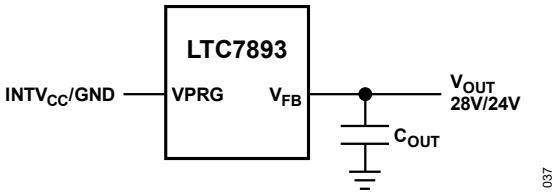


Figure 44. Setting Fixed 28V or 24V Output Voltage

RUN Pin and Undervoltage Lockout

The LTC7893 is enabled using the RUN pin. The RUN pin has a rising threshold of 1.2V with 120mV of hysteresis. Pulling the RUN pin less than 1.08V shuts down the main control loop and resets the soft start. Pulling the RUN pin less than 0.7V disables the controller and most internal circuits, including the $INTV_{CC}$ LDO regulators. In this state, the LTC7893 draws only ≈1µA of current from V_{BIAS}.

The RUN pin is a high impedance, must be externally pulled up or pulled down, and is driven directly by logic. The RUN pin can tolerate up to 100V (the absolute maximum). Therefore, these pins can be conveniently tied to V_{IN} in applications where the controller is enabled continuously and never shut down. Do not float the RUN pins.

The RUN pin can also be configured as precise UVLOs on the input supply with a resistor divider from V_{IN} to ground, as shown in *Figure 45*.

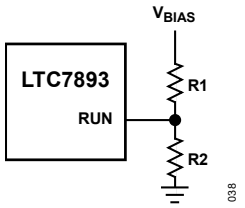


Figure 45. Using the Run Pin as a UVLO

The V_{IN} UVLO thresholds can be computed by Equation 17 and Equation 18, as follows:

$$\text{UVLO RISING} = 1.2\text{V}(1 + \frac{\text{R1}}{\text{R2}}) \quad (17)$$

$$\text{UVLO FALLING} = 1.08\text{V}(1 + \frac{\text{R1}}{\text{R2}}) \quad (18)$$

The current that flows through the R1 and R2 divider adds to the shutdown, sleep, and active current of the LTC7893. Take care to minimize the impact of this current on the overall efficiency of the application circuit. Resistor values in the MΩ range can be required to keep the impact on quiescent shutdown and sleep currents low.

Soft-Start (SS Pin)

The startup of V_{OUT} is controlled by the voltage on the SS pin. When the voltage on the SS pin is less than the internal 1.2V reference, the LTC7893 regulates the V_{FB} pin voltage to the voltage on the SS pin instead of the internal reference.

Soft start is enabled by connecting a capacitor from the SS pin to GND. An internal 12µA current source charges the capacitor, providing a linear ramping voltage at the SS pin. The LTC7893 regulates its feedback voltage (and hence V_{OUT}) according to the voltage on the SS pin, allowing V_{OUT} to rise smoothly from 0V to its final regulated value. For a desired soft-start time (t_{SS}) select a soft-start capacitor (C_{SS}) = t_{SS} × 10nF/msec.

$INTV_{CC}$ Regulators (OPTI-DRIVE)

The LTC7893 features two separate internal LDO linear regulators that supply power at the $INTV_{CC}$ pin from either the V_{BIAS} pin or the $EXTV_{CC}$ pin, depending on the $EXTV_{CC}$ pin voltage and connections to the DRVSET and DRVUV pins. The DRV_{CC} pin is the supply pin for the FET gate drivers and must be connected to the $INTV_{CC}$ pin. The V_{BIAS} LDO regulator and the $EXTV_{CC}$ LDO regulator regulate $INTV_{CC}$ between 4V and 5.5V, depending on how the DRVSET pin is set. Each LDO regulator can provide a peak current of at least 100mA.

Bypass the $INTV_{CC}$ pin with a minimum of 4.7µF ceramic capacitor, and place it as close as possible to the pin. It is recommended to place an additional 1µF ceramic capacitor next to the DRV_{CC} pin and GND pins to supply the high frequency transient currents required by the FET gate drivers.

The DRVSET pin programs the $INTV_{CC}$ supply voltage, and the DRVUV pin selects the different $INTV_{CC}$ UVLO and $EXTV_{CC}$ switchover threshold voltages. *Table 6* summarizes the different DRVSET pin configurations along with the voltage settings that go with each configuration. *Table 7* summarizes the different DRVUV pin configurations and voltage settings. Tying the DRVSET pin to $INTV_{CC}$ programs $INTV_{CC}$ to 5.5V. Tying the DRVSET pin to GND programs $INTV_{CC}$ to 5.0V. Place a 43kΩ to 100kΩ resistor between DRVSET and GND to program the $INTV_{CC}$ voltage between 4V to 5.5V, as shown in *Figure 46*.

Table 6. *DRVSET Pin Configurations and Voltage Settings*

DRVSET PIN	$INTV_{CC}$ VOLTAGE (V)
GND	5.0
$INTV_{CC}$	5.5
Resistor to GND 43kΩ to 100kΩ	4 to 5.5

Table 7. DRVUV Pin Configurations and Voltage Settings

DRVUV PIN	$INTV_{CC}$ UVLO RISING and FALLING THRESHOLDS (V)	$EXTV_{CC}$ SWITCHOVER RISING and FALLING THRESHOLDS (V)
GND	3.8 and 3.6	4.76 and 4.54
Floating	4.4 and 4.18	5.95 and 5.56
$INTV_{CC}$	5 and 4.75	5.95 and 5.56

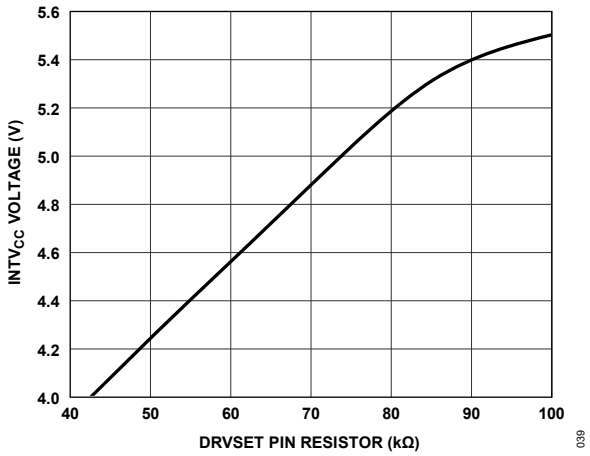


Figure 46. Relationship Between $INTV_{CC}$ Voltage and Resistor Value at the DRVSET Pin

High input voltage applications in which large FETs are driven at high frequencies can exceed the maximum junction temperature rating for the LTC7893. The $INTV_{CC}$ current, which is dominated by the gate charge current, can be supplied by either the V_{BIAS} LDO regulator or the $EXTV_{CC}$ LDO regulator. When the voltage on the $EXTV_{CC}$ pin is less than its switchover threshold (4.76V or 5.95V, as determined by the DRVUV pin), the V_{BIAS} LDO regulator is enabled. In this case Power dissipation for the IC is equal to V_{BIAS} × $INTV_{CC}$ current (I_{INTVCC}). The gate charge current is dependent on the operating frequency, as discussed in the *Efficiency Considerations* section. To estimate the junction temperature, use the equation detailed in *Table 2*. For example, the LTC7893 $INTV_{CC}$ current is limited to less than 36mA from a 36V supply when not using the $EXTV_{CC}$ supply at an ambient temperature of 70°C, as shown in Equation 19:

$$T_J = 70°C + (36mA)(36V)(43°C/W) = 125°C \quad (19)$$

To prevent the maximum junction temperature from exceeding, check the input supply current while operating in continuous conduction mode (MODE = $INTV_{CC}$) at maximum V_{BIAS}.

When the voltage applied to $EXTV_{CC}$ rises above its rising switchover threshold, the V_{BIAS} LDO regulator turns off and the $EXTV_{CC}$ LDO regulator enables. The $EXTV_{CC}$ LDO regulator remains on as long as the voltage applied to $EXTV_{CC}$ remains above its falling switchover threshold. The $EXTV_{CC}$ LDO regulator attempts to regulate the $INTV_{CC}$ voltage to the voltage as programmed by the DRVSET pin. Therefore, while $EXTV_{CC}$ is less than the programmed voltage set by the DRVSET pin, the LDO regulator is in dropout and the $INTV_{CC}$ voltage is approximately equal to $EXTV_{CC}$. When $EXTV_{CC}$ is greater than the programmed voltage (up to an absolute maximum of 30V), $INTV_{CC}$ is regulated to the programmed voltage. If more current is required through the $EXTV_{CC}$ LDO regulator than is specified, add an external Schottky diode between the $EXTV_{CC}$ and $INTV_{CC}$ pins. In this case, do not apply more than 6V to the $EXTV_{CC}$ pin.

Significant efficiency and thermal gains can be realized by powering $INTV_{CC}$ from an external supply. This is accomplished by tying the $EXTV_{CC}$ pin directly to an external supply that is greater than the $INTV_{CC}$ regulation point.

Tying the $EXTV_{CC}$ pin to an 8.5V supply reduces the junction temperature in Equation 19 from 125°C to the results given by Equation 20, as follows:

$$T_J = 70°C + (36mA)(8.5V)(43°C/W) = 83°C \quad (20)$$

The following list summarizes the three possible connections for $EXTV_{CC}$:

1. $EXTV_{CC}$ grounded. This connection causes the internal V_{BIAS} LDO regulator to power $INTV_{CC}$, resulting in an efficiency penalty of up to 10% or more at high V_{BIAS} voltages.
2. $EXTV_{CC}$ connected directly to V_{IN}. This connection is the normal connection for an application with V_{IN} in the 5V to 30V range and provides significant thermal gains if V_{BIAS} is tied to V_{OUT}.
3. $EXTV_{CC}$ connected directly to an external supply. If an external supply is available in the 5V to 30V range, it can be used to power $EXTV_{CC}$, provided that it is compatible with the FET gate drive requirements. This supply can be higher or lower than V_{BIAS}. However, a lower $EXTV_{CC}$ voltage results in higher efficiency.

Topside FET Driver Supply (C_B)

An external bootstrap capacitors C_B connected to the BOOST pins supply the gate drive voltages for the topside FETs. Capacitor C_B in *Figure 34* is charged through an internal switch from DRV_{CC} when the SW pin is low and the bottom FET is turned on. The on resistance of the internal switch is approximately 7Ω.

When the topside FET is to be turned on, the driver places the C_B voltage across the gate-source of the desired FET, which enhances the FET and turns on the topside switch. The switch node voltage, SW, rises to V_{OUT} and the BOOST pin follows. With the topside FET on, the boost voltage is more than the output voltage: $V_{BOOST} = V_{OUT} + V_{INTVCC}$. The value of the boost capacitor C_B needs to be 100 times that of the total input capacitance of the topside FETs. For a typical application, a value of $C_B = 0.1\mu F$ is generally sufficient.

Minimum On-Time Considerations

The minimum on-time ($t_{ON(MIN)}$) is the smallest time duration that the LTC7893 is capable of turning on the bottom FET. $t_{ON(MIN)}$ is determined by internal timing delays and the gate charge required to turn on the bottom FET. Low duty cycle applications can approach this minimum on-time limit. Take care to ensure the results in Equation 21, as follows:

$$t_{ON(MIN)} < \frac{V_{OUT} - V_{IN}}{V_{OUT} \cdot f} \quad (21)$$

If the duty cycle falls below what can be accommodated by the minimum on-time, the LTC7893 begins to skip cycles. The output voltage continues to be regulated, but the ripple voltage and current increases. The minimum on-time for the LTC7893 is approximately 100ns. If VIN increases thereby further decreasing the duty cycle, more cycles are skipped, and the LTC7893 can turn on the top FET continuously. If the bottom FET is not turned on frequently enough to recharge the bootstrap capacitor, the top FET will not fully enhance, or it can be completely off when the LTC7893 turns on the top FET. Thus, the LTC7893 cannot achieve 100% top FET on operation.

Fault Conditions: Overtemperature Protection

At higher temperatures, or in cases where the internal power dissipation causes excessive self-heating (such as a short from $INTV_{CC}$ to ground), internal overtemperature shutdown circuitry shuts down the LTC7893. When the internal die temperature exceeds 180°C, the $INTV_{CC}$ LDO regulator and gate drivers disable. When the die cools to 160°C, the LTC7893 enables the $INTV_{CC}$ LDO regulator and resumes operation, beginning with a soft-start startup. Avoid long-term overstress (T_J > 125°C) because it can degrade the performance or shorten the life of the device.

Phase-Locked Loop and Frequency Synchronization

The LTC7893 has an internal PLL that allows the turn on of the bottom FET to be synchronized to the rising edge of an external clock signal applied to the PLLIN/SPREAD pin.

Rapid phase locking can be achieved by using the FREQ pin to set a free-running frequency near the desired synchronization frequency. Before synchronization, the PLL is prebiased to the frequency set by the FREQ pin. Consequently, the PLL only needs to make minor adjustments to achieve phase-lock and synchronization. Although it is not required, placing the free-running frequency near the external clock frequency prevents the oscillator from passing through a large range of frequencies as the PLL locks.

When synchronized to an external clock, the LTC7893 operates in pulse-skipping mode if it is selected by the MODE pin, or in forced continuous mode otherwise. The LTC7893 is guaranteed to synchronize to an external clock applied to the PLLIN/SPREAD pin that swings up to at least 2.2V and down to 0.5V or less. Note that the LTC7893 can only be synchronized to an external clock frequency within the range of 100kHz to 3MHz.

Efficiency Considerations

The percent efficiency of a switching regulator is equal to the output power divided by the input power times 100%. Analyzing individual losses is useful for determining what is limiting the efficiency and which change produces the most improvement. The percent efficiency can be expressed by Equation 22, as follows:

$$\%\text{Efficiency} = 100\% - (L1 + L2 + L3 + ...) \quad (22)$$

where L1, L2, L3, and so on, are the individual losses as a percentage of input power.

Although all dissipative elements in the circuit produce losses, four main sources usually account for most of the losses in LTC7893 circuits: IC V_{BIAS} current, $INTV_{CC}$ regulator current, I^2R losses, and bottom side FET transition losses.

The V_{BIAS} current is the dc supply current given in *Table 1*, which excludes FET driver and control currents. Other than at light loads in Burst Mode operation, V_{BIAS} current typically results in a small (<0.1%) loss.

The $INTV_{CC}$ current is the sum of the FET driver and control currents. The FET driver current results from switching the gate capacitance of the power FETs. Each time a FET gate is switched from low to high to low again, a packet of charge (dQ) moves from $INTV_{CC}$ to GND. The resulting dQ/time duration (dt) is a current out of $INTV_{CC}$ that is typically much larger than the control circuit current. In continuous mode, gate charge current ($I_{GATECHG}$) = frequency (f) x (Q_T + Q_B), where Q_T and Q_B are the gate charges of the top and bottom FETs.

I^2R losses are predicted from the dc resistances of the input fuse (if used), FET, inductor, current sense resistor, and input and output capacitor ESR. In continuous mode, the average output current flows through L and R_{SENSE}, but is chopped between the top and bottom FETs. If the two FETs have approximately the same $R_{DS(ON)}$, the resistance of one FET can be summed with the resistances of L, R_{SENSE}, and ESR to obtain the I^2R losses.

Transition losses apply only to the bottom FETs and become significant only when operating at higher output voltages (typically 20V or greater) or at high frequency (MHz range). Transition losses can be estimated using Equation 23, as follows:

$$\text{TRANSITION LOSS} = (1.7)\frac{V_{OUT}^3}{V_{IN}} I_{L(MAX)} \times C_{MILLER} \times f \quad (23)$$

where:

$I_{L(MAX)}$ is the maximum average inductor current.
C_{MILLER} is the Miller capacitance.
f is the operating frequency.

Other hidden losses, such as copper trace and internal battery resistances, can account for an additional 5% to 10% efficiency degradation in portable systems. It is important to include these system level losses during the design phase. The internal battery and fuse resistance losses can be minimized by making sure that C_{IN} has adequate charge storage and low ESR at the switching frequency. A 25W supply typically requires a minimum of 20µF to 40µF of capacitance having a maximum of 20mΩ to 50mΩ of ESR. Other losses, including inductor core losses, generally account for less than 2% total additional loss.

Checking Transient Response

To check the regulator loop response, look at the load current transient response. Switching regulators take several cycles to respond to a step in dc (resistive) load current. When a load step occurs, V_{OUT} shifts by an amount equal to ΔI_{LOAD} × (ESR), where ESR is the effective series resistance of C_{OUT}. ΔI_{LOAD} also begins to charge or discharge C_{OUT}, generating the feedback error signal that forces the regulator to adapt to the current change and return V_{OUT} to its steady-state value. During this recovery time, V_{OUT} can be monitored for excessive overshoot or ringing, which indicates a stability problem.

OPTI-LOOP compensation allows the transient response to be optimized over a wide range of output capacitance and ESR values. The availability of the ITH pin not only allows optimization of control loop behavior, but it also provides a dc-coupled and ac filtered closed-loop response test point. The dc step, rise time, and settling at this test point reflects the closed-loop response. Assuming a predominantly second order system, the phase margin and/or damping factor can be estimated using the percentage of overshoot seen at the ITH pin. The bandwidth can also be estimated by examining the rise time at the ITH pin. The ITH external components shown in the *Typical Applications* section provide an adequate starting point for most applications.

The ITH series compensation resistor (R_C) and capacitor (C_C) filter sets the dominant pole zero loop compensation. The values can be modified slightly (from 0.5 to 2 times their initial values) to optimize transient response when the final PCB layout is done, and the particular output capacitor type and value are determined. The output capacitors must be selected because the various types and values determine the loop gain and phase. An output current pulse of 20% to 80% of full-load current, with a rise time of 1µs to 10µs, produces output voltage and ITH pin waveforms that give a sense of the overall loop stability without breaking the feedback loop.

Placing a power FET directly across the output capacitor and driving the gate with an appropriate signal generator is a practical way to produce a realistic load step condition. The initial output voltage step resulting from the step change in output current may not be within the bandwidth of the feedback loop. Therefore, this signal cannot be used to determine phase margin. For this reason, it is better to look at the ITH pin signal, which is in the feedback loop and is the filtered and compensated control loop response. The gain of the loop increases by increasing R_C, and the bandwidth of the loop increases by decreasing C_C. If R_C increases by the same factor that C_C is decreases, the zero frequency is kept the same, keeping the phase shift the same in the most critical frequency range of the feedback loop. The output voltage settling behavior is related to the stability of the closed-loop system and demonstrates the actual overall supply performance.

A second, more severe transient is caused by switching in loads with large (>1µF) supply bypass capacitors. The discharged bypass capacitors are effectively put in parallel with C_{OUT}, causing a rapid drop in V_{OUT}. No regulator can alter its delivery of current quickly enough to prevent this sudden step change in output voltage, if the load switch resistance is low and it is driven quickly. If the ratio of C_{LOAD} to C_{OUT} is greater than 1:50, the switch rise time must be controlled so that the load rise time is limited to approximately C_{LOAD} × 25µs/µF. Therefore, a 10µF capacitor requires a 250µs rise time, limiting the charging current to about 200mA.

Design Example

As a design example, assume the nominal input volage ($V_{IN(NOMINAL)}$) = 12V, $V_{IN(MAX)}$ = 20V, V_{OUT} = 24V, I_{OUT} = 4A, and f = 1MHz.

Take the following steps to design an application circuit:

1. Set the operating frequency. The frequency is not one of the internal preset values. Therefore, a resistor from the FREQ pin to GND is required, with a value given by Equation 24, as follows:

$$R_{FREQ}(\text{in k}\Omega) = \frac{37\text{MHz}}{1\text{MHz}} = 37\text{k}\Omega \quad (24)$$

2. Determine the inductor value. Initially, select a value based on an inductor ripple current of 30%. To calculate the inductor value, use Equation 25, as follows:

$$L = \frac{V_{IN}}{f \bullet \Delta I_L}\left(1 - \frac{V_{IN}}{V_{OUT}}\right) = 2.4\mu H \quad (25)$$

   The highest value of the ripple current occurs when $V_{IN} = (1/2) \bullet V_{OUT}$. In this case, the ripple at V_{IN} = 12V is 31%.

3. Verify that the minimum on-time of 100ns is not violated. The minimum on-time occurs at $V_{IN(MAX)}$, as shown in Equation 26:

$$t_{ON(MIN)} < \frac{V_{OUT} - V_{IN(MAX)}}{V_{OUT} \bullet f} = \frac{4V}{24V \bullet 1MHz} = 166\text{ns} \quad (26)$$

   This time is sufficient to satisfy the minimum on-time requirement. If the minimum on-time is violated, the LTC7893 skips pulses at high input voltage, resulting in lower frequency operation and higher inductor current ripple than desired. If undesirable, this behavior can be avoided by decreasing the frequency (with the inductor value accordingly adjusted) to avoid operation near the minimum on-time.

4. Select the R_{SENSE} resistor value. The peak inductor current is the maximum dc output current plus half the inductor ripple current, or 8A x (1 + 0.31/2) = 9.24A in this case. The R_{SENSE} resistor value is then calculated based on the minimum value for the maximum current sense threshold (45mV for ILIM = float) given by Equation 27, as follows:

$$R_{SENSE} \leq \frac{45\text{mV}}{9.24\text{A}} \approx 4\text{m}\Omega \quad (27)$$

   To allow for additional margin, a lower value R_{SENSE} can be used. However, be sure that the inductor saturation current has sufficient margin above $V_{SENSE(MAX)}/ R_{SENSE}$, where the maximum value of 55mV is used for $V_{SENSE(MAX)}$.

5. Select the feedback resistors. Choosing 1% resistors: R_A = 5kΩ and R_B = 95.3kΩ yields an output voltage of 24.07V. The resistance values selected give a feedback divider current of 24.07V/(5kΩ + 95.3kΩ) = 240µA.

6. Select the FETs. The best way to evaluate FET performance in a particular application is to build and test the circuit on the bench, facilitated by an LTC7893 evaluation board. However, an educated guess about the application is helpful to initially select FETs. Because this is a high current, low voltage application, I^2R losses will likely dominate over transition losses for the bottom FET. Therefore, choose a FET with lower $R_{DS(ON)}$ as opposed to lower gate charge to minimize the combined loss terms. The top FET does not experience transition losses, and its power loss is generally dominated by I^2R losses. For this reason, the top FET is typically chosen to be of lower $R_{DS(ON)}$ and subsequently higher gate charge than the bottom FET.

   When using silicon MOSFETs, be sure to select logic level threshold MOSFETs because the gate drive voltage is limited to 5.5V ($INTV_{CC}$).

7. Select the output capacitor. C_{OUT} is chosen to filter the square current in the output. The maximum output current peak is given by Equation 28, as follows:

$$I_{OUT(PEAK)} = I_{OUT(MAX)} \times \left(1 + \frac{RIPPLE\%}{2}\right) = 4 \times \left(1 + \frac{31\%}{2}\right) = 4.62A \quad (28)$$

   A low ESR (5mΩ) capacitor is suggested. This capacitor will limit output voltage ripple to 23.1mV (assuming ESR dominates the ripple).
8. Determine the bias supply components. If another supply is available that is above the $INTV_{CC}$ regulation voltage and below V_{IN}, for example an 8.5V supply, connect that supply to $EXTV_{CC}$ to improve the efficiency. For a 6.7ms soft start, select a 0.1µF capacitor for the SS pin. As a first pass estimate for the bias components, select the $INTV_{CC}$ capacitance (C_{INTVCC}) = 4.7µF and boost supply capacitor (C_B) = 0.1µF.
9. Determine and set application-specific parameters. Set the MODE pin based on the trade-off of light load efficiency and constant frequency operation. Set the PLLIN/SPREAD pin based on whether a fixed, spread spectrum, or phase-locked frequency is desired. The RUN pin can control the minimum input voltage for regulator operation, or can be tied to V_{IN} for always-on operation. Use ITH compensation components from the Typical Applications as a first guess, check the transient response for stability, and modify as necessary. Program the DTCA and DTCB pins for the desired dead time delays.

PCB Board Layout Checklist

Figure 47 shows the current waveforms present in the various branches of the synchronous boost converters operating in the continuous mode. 0

When laying out the printed circuit board, use the following checklist to ensure proper operation of the IC.

1. Place the top and bottom N-channel FETs (MTOP and MBOT) and the high frequency (ceramic) C_{OUT} capacitors as shown in the *Typical Applications* section within 1cm of each other.
2. Route the TGUP and TGDN traces together and connect them as close as possible to the top FET gate. Route the BGDN and BGUP traces together and connect them as close as possible to the bottom FET gate. If using gate resistors, connect the resistor connections to the FET gate as close as possible to the FET. Connecting TGUP and TGDN further away from the top FET gate as well as connecting BGUP and BGDN further away from the bottom FET gate can adversely affect the operation of the LTC7893's adaptive dead time control.
3. The combined IC GND pin and the GND return of C_{INTVCC} must return to the combined C_{OUT} negative terminals. The path formed by the bottom N-channel FET and the C_{IN} capacitor must have short leads and PCB trace lengths. Connect the output capacitor negative terminals as close as possible to the negative terminals of the input capacitor by placing the capacitors next to each other and away from the loop.
4. Connect the LTC7893 V_{FB} pin resistive dividers to the positive terminals of C_{OUT} and the signal GND. Place the divider close to the V_{FB} pin to minimize noise coupling into the sensitive V_{FB} node. The feedback resistor connections must not be along the high current input feeds from the input capacitors.
5. Route the $SENSE^-$ and $SENSE^+$ leads together with minimum PCB trace spacing. Route these traces away from the high frequency switching nodes on an inner layer, if possible. The filter capacitor between $SENSE^+$ and $SENSE^-$ must be as close as possible to the IC. Ensure accurate current sensing with Kelvin connections at the sense resistor.
6. Connect the $INTV_{CC}$ decoupling capacitor close to the IC, between the $INTV_{CC}$ and the power GND pin. This capacitor carries the current peaks of the FET drivers. Place an additional 1µF ceramic capacitor next to the DRV_{CC} and GND pins to help improve noise performance.

7. Keep the switching nodes (SW), top gate nodes (TGUP/TGDN), and boost nodes (BOOST) away from sensitive small signal nodes, especially from the voltage and current sensing feedback pins of the other channel. All of these nodes have large and fast-moving signals. Therefore, keep these nodes on the output side of the LTC7893 and ensure they occupy the minimum PCB trace area.
8. Use a modified star ground technique: a low impedance, large copper area central grounding point on the same side of the PCB as the input and output capacitors, with tie ins for the bottom of the $INTV_{CC}$ decoupling capacitor, the bottom of the voltage feedback resistive divider, and the GND pin of the IC.

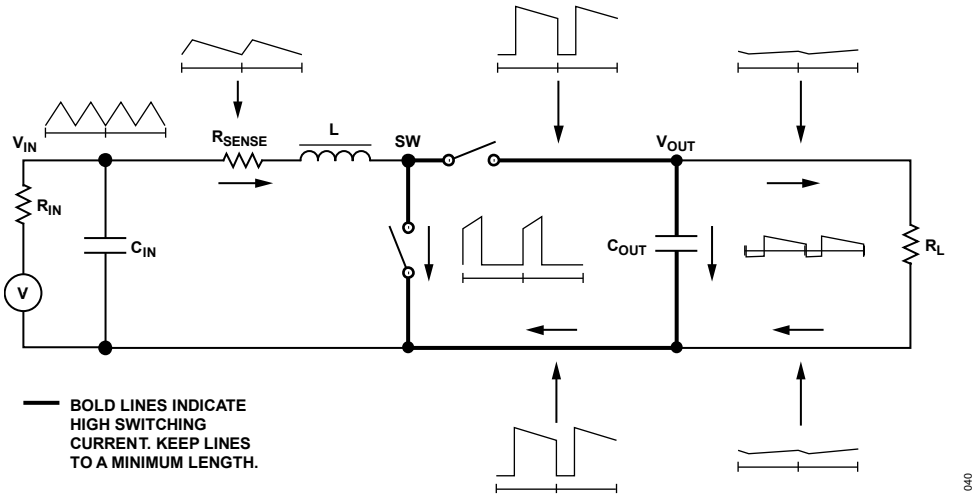


Figure 47. Branch Current Waveforms

PCB Layout Debugging

Start with one controller on at a time. Use a dc to 50MHz current probe to monitor the current in the inductor while testing the circuit. Monitor the output switching node (the SW pin) to synchronize the oscilloscope to the internal oscillator and probe the actual output voltage as well. Check for proper performance over the operating voltage and current range expected in the application. The frequency of operation is maintained over the input voltage range down to dropout and until the output load drops to less than the low current operation threshold, typically 25% of the maximum designed current level in Burst Mode operation.

The duty-cycle percentage is maintained from cycle to cycle in a well designed, low noise PCB implementation. Variation in the duty cycle at a subharmonic rate can suggest noise pickup at the current or voltage sensing inputs or inadequate loop compensation. Overcompensation of the loop can tame an improper PCB layout if regulator bandwidth optimization is not required. Turn on both controllers at the same time after each controller is checked for its individual performance. A particularly difficult region of operation is when one controller channel is nearing its current comparator trip point when the other channel is turning on its top FET, which occurs around 50% duty cycle on either channel due to the phasing of the internal clocks and may cause minor duty-cycle jitter.

Reduce V_{BIAS} from its nominal level to verify operation of the regulator at the maximum duty cycle. Check the operation of the undervoltage lockout circuit by further lowering V_{BIAS} while monitoring the outputs to verify operation.

Investigate whether any problems exist only at higher output currents or only at higher input voltages. If problems coincide with high input voltages and low output currents, look for capacitive coupling between the BOOST, SW, TGx, and possibly BGx connections and the sensitive voltage and current pins. Place a capacitor across the current sensing pins next to the pins of the IC. This capacitor helps to minimize the effects of differential noise injection due

to high frequency capacitive coupling. If problems are encountered with high current output loading at lower input voltages, look for inductive coupling between C_{IN}, the top FET, and the bottom FET components to the sensitive current and voltage sensing traces. In addition, investigate the common GND path voltage pickup between these components and the GND pin of the IC.

A problem that may be missed in an otherwise properly working switching regulator results when the current sensing leads are hooked up backwards. The output voltage under this improper hookup is maintained, but the advantages of current mode control are not realized. Compensation of the voltage loop is more sensitive to component selection. This behavior can be investigated by temporarily shorting out the current sensing resistor. The regulator maintains control of the output voltage even during this condition.

TYPICAL APPLICATIONS

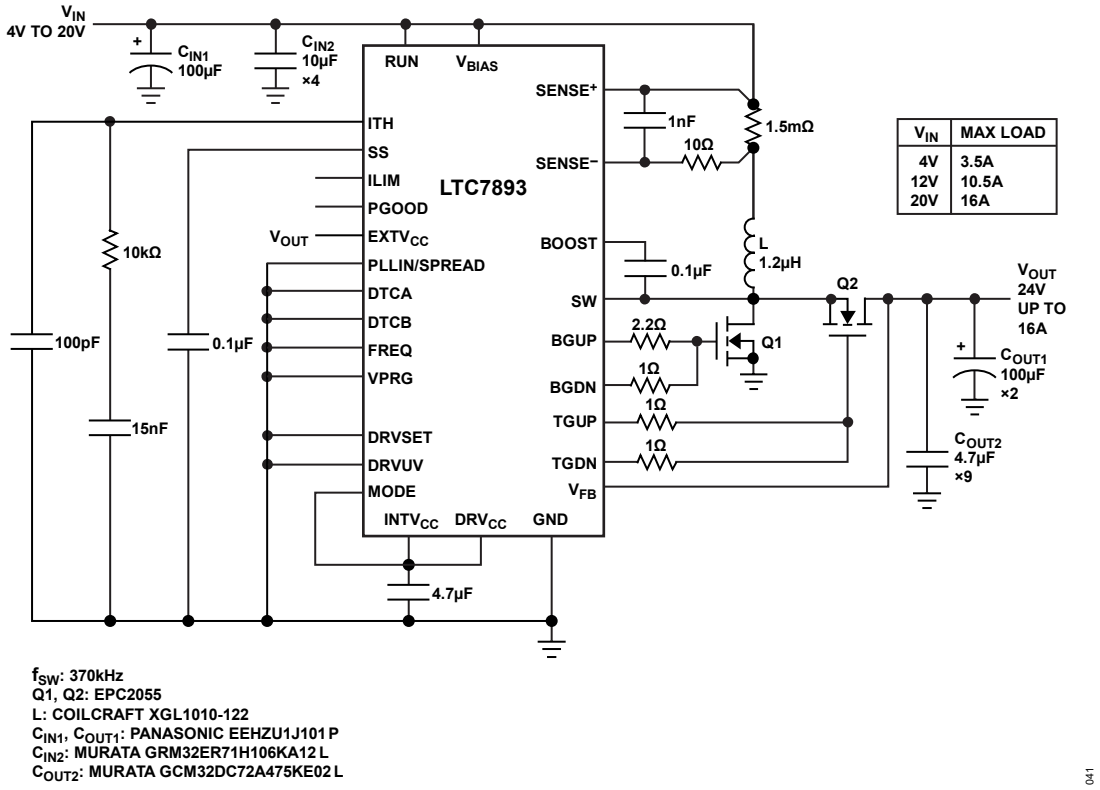


Figure 48. High Efficiency, 24V_{OUT}, Boost Regulator Using GaN FETs

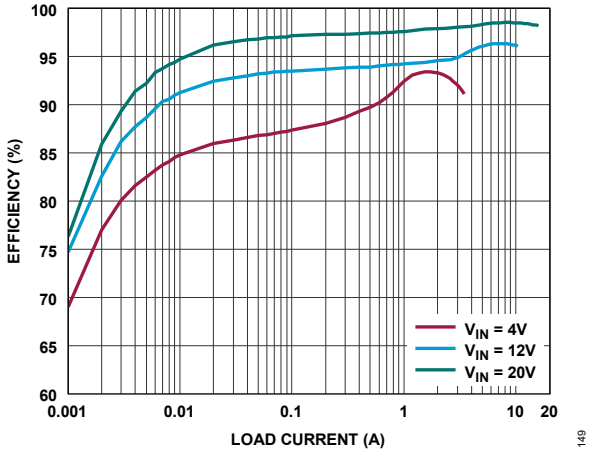


Figure 49. V_{OUT} Efficiency vs Load Current for Figure 48

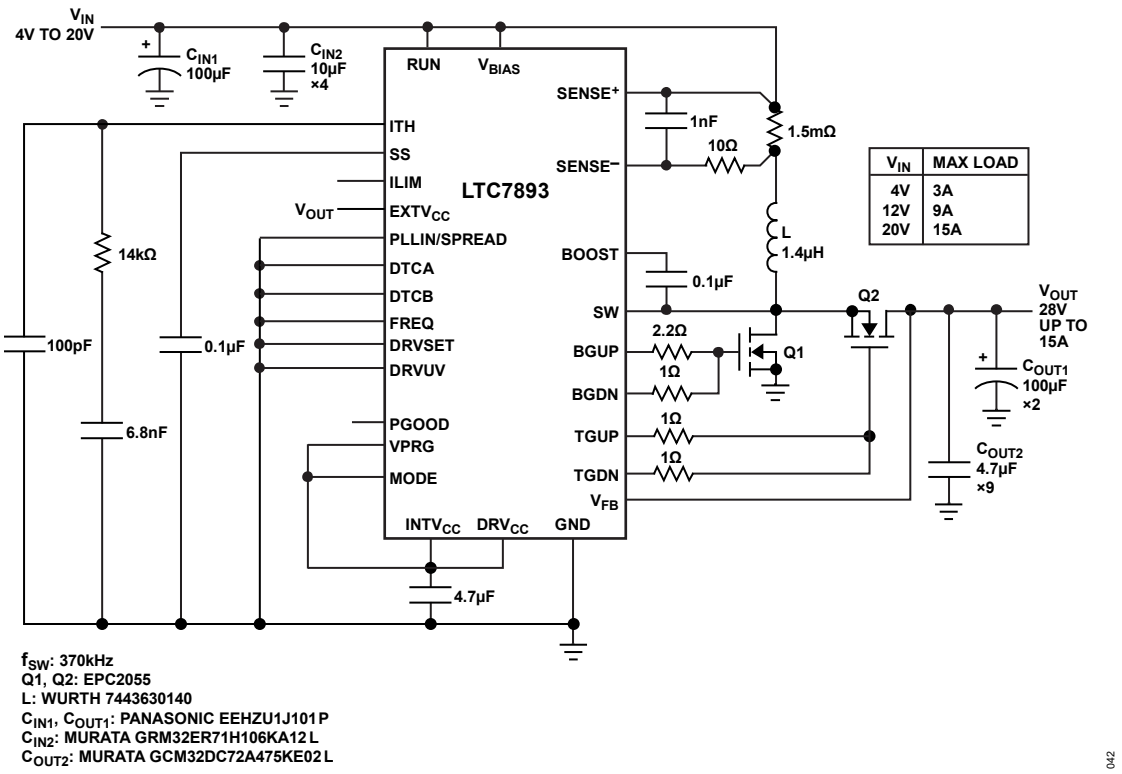


Figure 50. High Efficiency, 28V_{OUT}, Boost Regulator Using GaN FETs

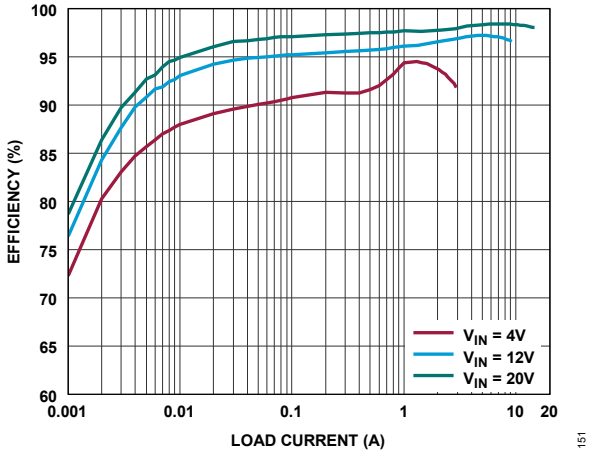


Figure 51. V_{OUT} Efficiency vs Load Current for Figure 50

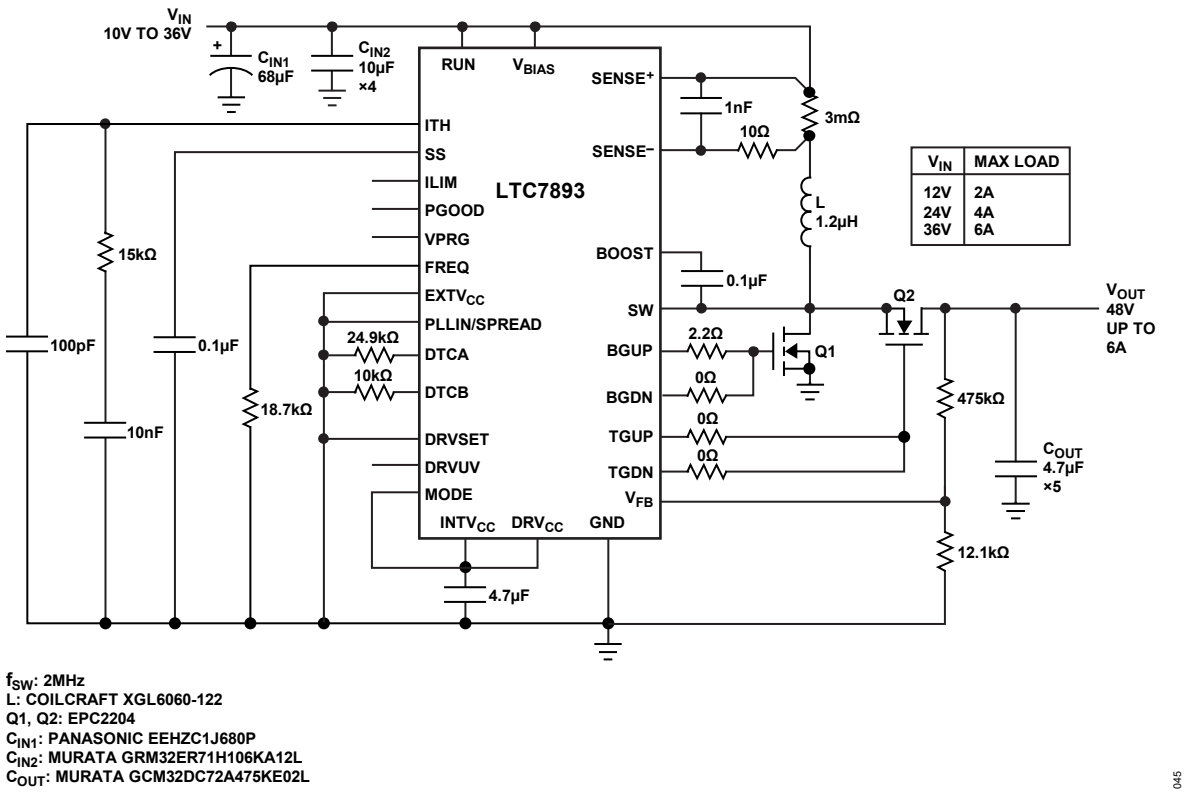


Figure 52. High Frequency (2MHz), 48V_{OUT}, Boost Regulator Using GaN FETs

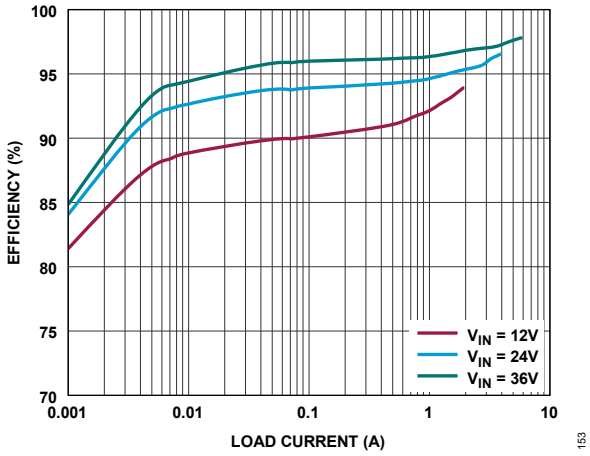


Figure 53. V_{OUT} Efficiency vs Load Current for Figure 52

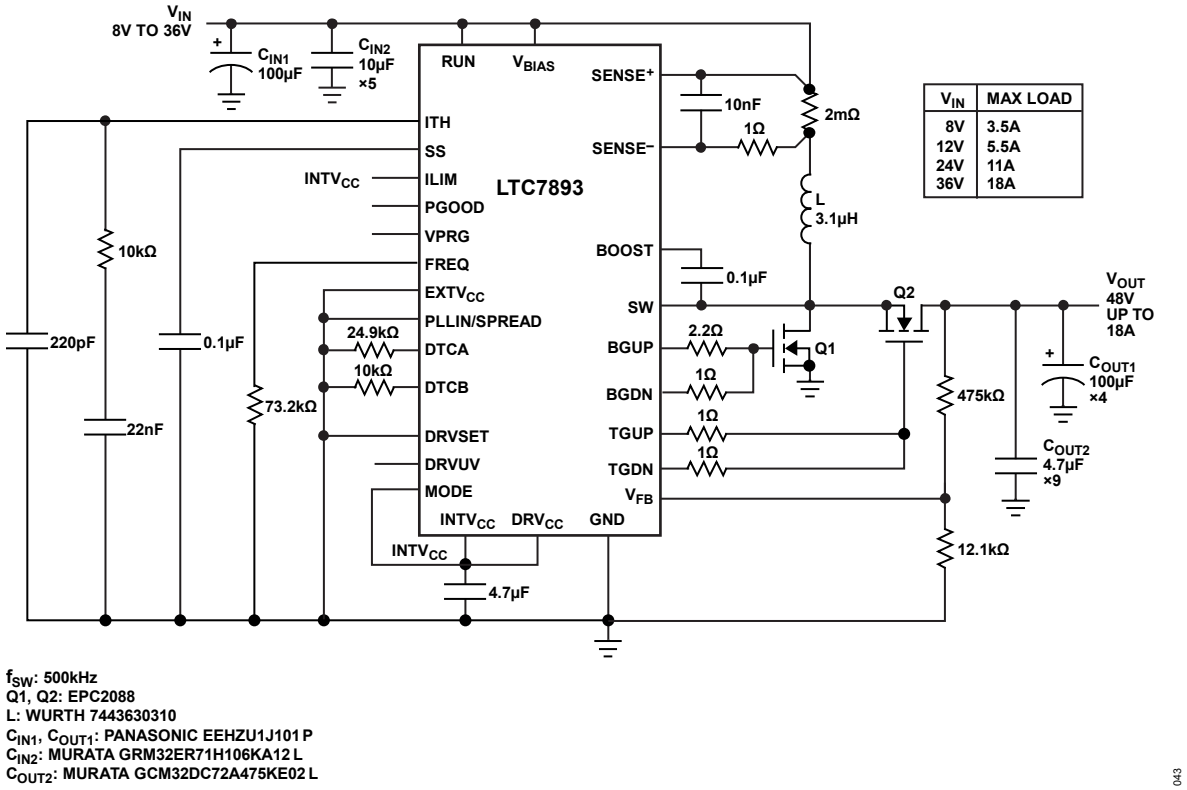


Figure 54. High Efficiency, 48V_{OUT}, Boost Regulator Using GaN FETs

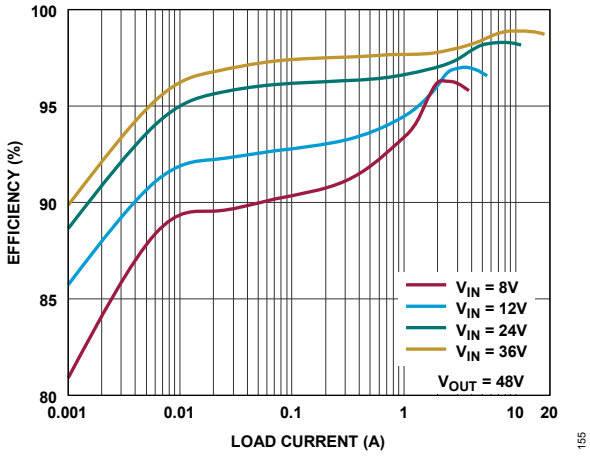


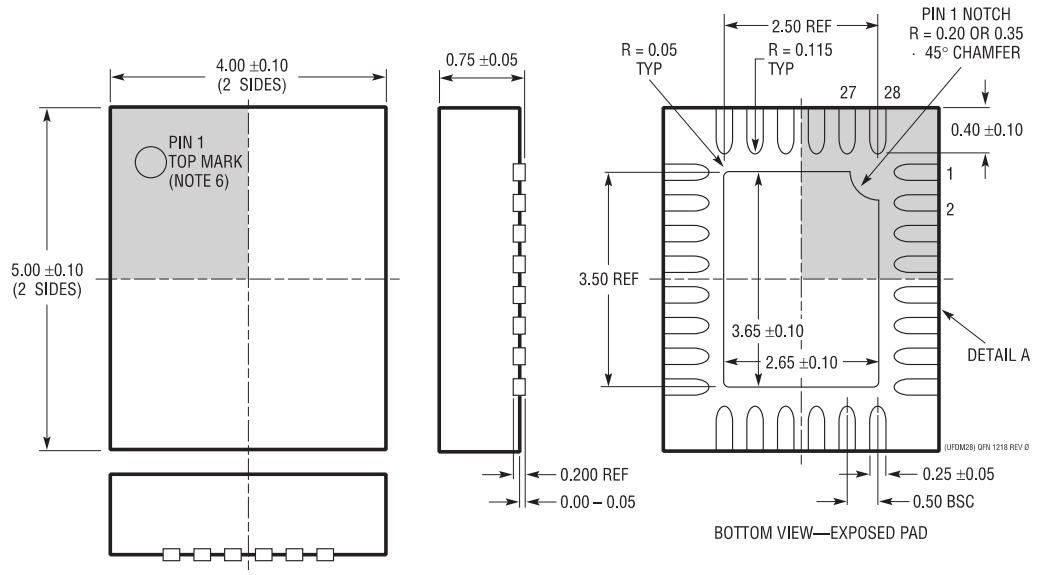
Figure 55. V_{OUT} Efficiency vs Load Current for Figure 54

RELATED PARTS

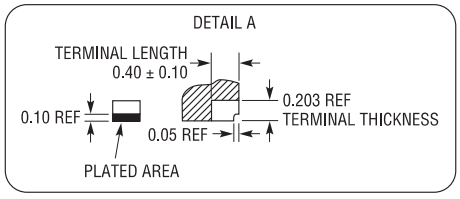
PART NUMBER	DESCRIPTION	COMMENTS
LTC3786	Low I_Q Synchronous Step-Up DC/DC Controller	4.5V (Down to 2.5V after Start-Up) ≤ V_{IN} ≤ 38V, V_{OUT} Up to 60V, 50kHz to 900kHz Fixed Operating Frequency, 3mm × 3mm QFN-16, MSOP-16E
LTC3769	Low I_Q Synchronous Step-Up DC/DC Controller	4.5V (Down to 2.3V after Start-Up) ≤ V_{IN} ≤ 60V, V_{OUT} Up to 60V, I_Q = 28µA, 50kHz to 900kHz Fixed Operating Frequency, 4mm × 4mm QFN-24, TSSOP-20
LTC3784	Single Output 2-Phase Low I_Q, Synchronous Step-Up DC/DC Controller	4.5V (Down to 2.5V after Start-Up) ≤ V_{IN} ≤ 60V, V_{OUT} Up to 60V, PLL Fixed Frequency 50kHz to 900kHz, I_Q = 28µA
LTC3788/LTC3788-1	Dual output synchronous Step-Up DC/DC Controller	4.5V (Down to 2.5V after Start-Up) ≤ V_{IN} ≤ 38V, V_{OUT} Up to 60V, 50kHz to 900kHz, Fixed Operating Frequency, 5mm × 5mm QFN-32, SSOP-28
LTC3787/LTC3787-1	Single output 2-Phase Low I_Q, Synchronous Step-Up DC/DC Controller	4.5V (Down to 2.5V after Start-Up) ≤ V_{IN} ≤ 38V, V_{OUT} Up to 60V, 50kHz to 900kHz Fixed Operating Frequency, 4mm × 5mm QFN-28, SSOP-28
LTC3897	Multiphase Synchronous Step-Up DC/DC Controller with Input/Output Protection	4.5V ≤ V_{IN} ≤ 65V, 75V Peak, V_{OUT} Up to 60V, PLL Fixed Frequency 75kHz to 550kHz, I_Q = 55µA, TSSOP-38, 5mm × 7mm QFN-38
LTC3862/LTC38621/ LTC3862-2	Multiphase, Single Output Dual Channel Step-Up DC/DC Controller	2.5V ≤ V_{IN} ≤ 36V, 5V or 10V Gate Drive, 75kHz to 500kHz, TSSOP-24, SSOP-24, 5mm × 5mm QFN-24
LTC7840	2-Phase Dual Output Non-Synchronous Step-Up DC/DC Controller	5.5V ≤ V_{IN} ≤ 60V, V_{OUT} Max Depends on External Components, PLL Fixed Frequency 50kHz to 425kHz, Flexible Topology for Boost, SEPIC and Flyback
LTC7804	40V Low I_Q, 3MHz Synchronous Boost Controller with PassThru	4.5V ≤ V_{IN} ≤ 40V, V_{OUT} Up to 40V, 100kHz to 3MHz Fixed Operating Frequency, 3mm × 3mm QFN-16
LTC7806	40V Low I_Q, 3MHz Multiphase Synchronous Boost Controller with Pass Thru	4.5V ≤ V_{IN} ≤ 40V, V_{OUT} Up to 40V, 100kHz to 3MHz Fixed Operating Frequency, 4mm × 5mm QFN-28
LTC7841	PolyPhase Synchronous Boost Controller with PMBus Interface	4.5V ≤ V_{IN} ≤ 60V, V_{OUT} Up to 60V, 75kHz to 850Hz Fixed Operating Frequency, 5mm × 6mm QFN-36

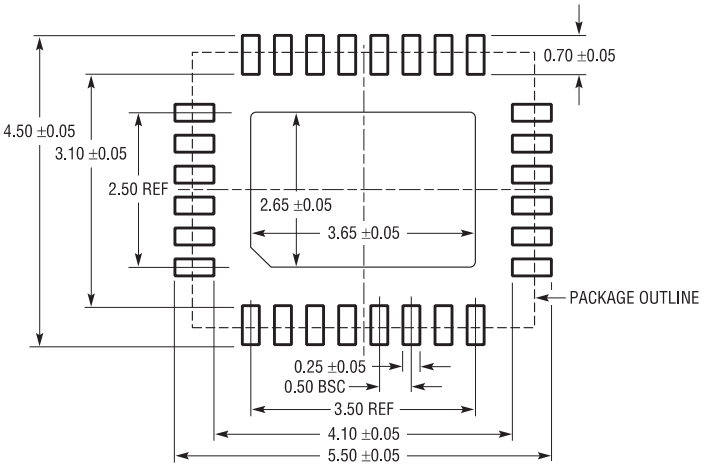
OUTLINE DIMENSIONS

UFDM Package
28-Lead Plastic Side Wettable QFN (4mm × 5mm)
(Reference DWG # 05-08-1682 Rev Ø)



NOTE:
1. DRAWING NOT TO SCALE
2. ALL DIMENSIONS ARE IN MILLIMETERS
3. DIMENSIONS OF EXPOSED PAD ON BOTTOM OF PACKAGE DO NOT INCLUDE MOLD FLASH. MOLD FLASH, IF PRESENT, SHALL NOT EXCEED 0.15mm ON ANY SIDE
4. SHADED AREA IS ONLY A REFERENCE FOR PIN 1 LOCATION ON THE TOP AND BOTTOM OF PACKAGE





RECOMMENDED SOLDER PAD PITCH AND DIMENSIONS
APPLY SOLDER MASK TO AREAS THAT ARE NOT SOLDERED

ORDERING GUIDE

Table 8. Ordering Guide

LEAD FREE FINISH	TAPE AND REEL	PART MARKING	PACKAGE DESCRIPTION	TEMPERATURE RANGE
LTC7893AUFDM#PBF	LTC7893AUFDM#TRPBF	LTC7893	28-Lead QFN (4mm x 5mm, Plastic Side Wettable)	−40°C to 125°C
AUTOMOTIVE PRODUCTS*				
LTC7893AUFDM#WPBF	LTC7893AUFDM#WTRPBF	LTC7893	28-Lead QFN (4mm × 5mm, Plastic Side Wettable)	−40°C to 125°C

Contact the factory for parts specified with wider operating temperature ranges.

Tape and reel specifications. Some packages are available in 500 unit reels through designated sales channels with #TRMPBF suffix.

*Versions of this part are available with controlled manufacturing to support the quality and reliability requirements of automotive applications. These models are designated with a #W suffix. Only the automotive grade products shown are available for use in automotive applications. Contact your local Analog Devices account representative for specific product ordering information and to obtain the specific Automotive Reliability reports for these models.

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