70V Parallelable 4-Switch Buck-Boost Controller with Inductor DCR Current Sensing

FEATURES

- **Single Inductor Architecture Allows V_{IN} Above, Below or Equal to the Regulated V_{OUT}**
- **Synchronous Rectification: Up to 98% Efficiency**
- **Wide V_{IN} Voltage Range: 5V to 70V**
- **±1% Output Voltage Accuracy: 1V ≤ V_{OUT} ≤ 70V**
- **DCR or R_{SENSE} Current Sensing**
- **Peak Current Mode Control in Buck/Boost/Buck-Boost Mode**
- **Programmable Input or Output Current Regulation**
- 7V NMOS Gate Drivers
- Phase-Lockable Frequency (100kHz to 600kHz)
- Multiphase/Multi-ICs Parallel Operation
- Selectable Continuous or Pulse-Skipping Mode Operation and Inductor Peak Current Limits
- Small 32-Lead 5mm × 5mm QFN Package
- 48-Lead 7mm x 7mm x 0.75mm LFCSP Package

APPLICATIONS

- Industrial and Telecom Systems
- Distributed DC Power or Battery Systems
- Battery Backup Units (BBU)

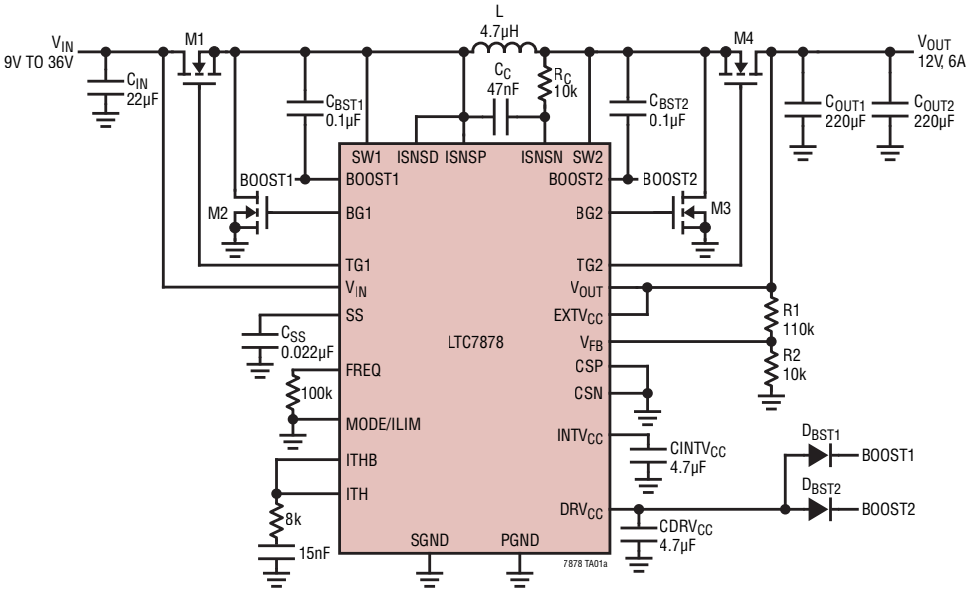
DESCRIPTION

The LTC®7878 is a high performance buck-boost switching regulator controller that operates from an input voltage above, below or equal to the output voltage. The constant-frequency, peak current mode architecture allows a phase-lockable switching frequency of up to 600kHz, while a programmable input or output current loop regulates the average input or output current accurately supporting battery charging applications. With a wide 5V to 70V input and output range and seamless, low noise transitions between operating regions, the LTC7878 is ideal for industrial and telecom systems.

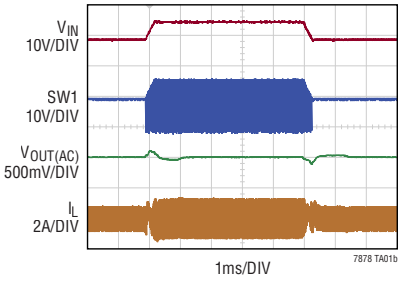
The LTC7878 features forced continuous mode (FCM)/pulse-skipping mode operation. It supports multiphase/multi-ICs parallel operation for high power applications. Additional features include 7V N-Channel gate drivers, smart $EXTV_{CC}$ auxiliary supply and programmable inductor peak current limit. A PGOOD pin indicates when the output is within 10% of its designed set point.

The LTC7878 is available in both a low-profile, 32-lead QFN and a 48-lead LFCSP packages.

TYPICAL APPLICATION



Input Voltage Line Transient
$9V_{IN}$ to $15V_{IN}$ to $9V_{IN}$

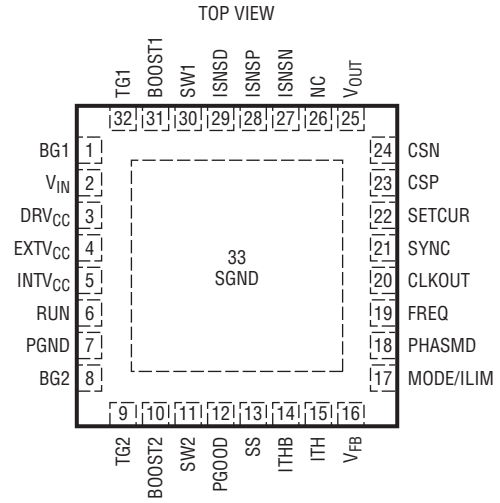


ABSOLUTE MAXIMUM RATINGS

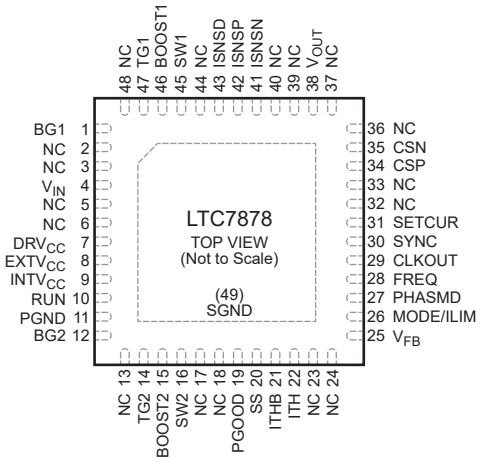
(Note 1)

Input and Output Voltage (V_{IN}, V_{OUT}) ..... –0.3V to 72V
Topside Driver Voltages
(BOOST1, BOOST2)..... –0.3V to 78V
Switch Voltages (SW1, SW2)..... –5V to 72V
(BOOST1 – SW1), (BOOST2 – SW2)..... –0.3V to 8V
Inductor Current Sense Voltages
(ISNSP, ISNSN, ISNSD)..... –5V to72V
Input/Output Current Sense Voltages
(CSP, CSN)..... –0.3V to 72V
$EXTV_{CC}$ Voltage ..... –0.3V to 72V
RUN Voltage..... –0.3V to 12V
PGOOD Voltage..... –0.3V to 6V
ITH, ITHB, V_{FB} Voltages ..... –0.3V to $INTV_{CC}$
PHASMD, SETCUR, SS Voltages..... –0.3V to $INTV_{CC}$
FREQ, SYNC, CLKOUT Voltages..... –0.3V to $INTV_{CC}$
MODE/ILIM Voltage ..... –0.3V to $INTV_{CC}$
DRV_{CC} Peak Current (Note 10)..... 100mA
TG1, BG1, TG2, BG2 ..... (Note 9)
Operating Junction Temperature Range (Notes 2, 3)
LTC7878A ..... –40°C to 125°C
Storage Temperature Range ..... –65°C to 150°C

PIN CONFIGURATION



UH PACKAGE
32-LEAD (5mm × 5mm) PLASTIC QFN
T_{JMAX} = 125°C, θ_{JA} = 44°C/W
EXPOSED PAD (PIN 33) IS SGND, MUST BE SOLDERED TO PCB



UK PACKAGE
48-LEAD (7mm × 7mm) LFCSP
T_{JMAX} = 125°C, θ_{JA} = 34°C/W
EXPOSED PAD (PIN 49) IS SGND, MUST BE SOLDERED TO PCB

ORDER INFORMATION

LEAD FREE FINISH	TAPE AND REEL	PART MARKING*	PACKAGE DESCRIPTION	TEMPERATURE RANGE
LTC7878AUH#PBF	LTC7878AUH#TRPBF	LTC7878	32-Lead (5mm × 5mm) Plastic QFN	–40°C to 125°C
LTC7878AUK#PBF	LTC7878AUK#TRPBF	LTC7878	48-Lead (7mm x 7mm) LFCSP	–40°C to 125°C

Contact the factory for parts specified with wider operating temperature ranges. *The temperature grade is identified by a label on the shipping container.

Tape and reel specifications. Some packages are available in 500 unit reels through designated sales channels with #TRMPBF suffix.

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the specified operating junction temperature range, otherwise specifications are at T_A = 25°C. , V_{IN} = 12V, RUN > 1.25V unless otherwise noted. (Note 2)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Bias Supply (V_{IN}, $EXTV_{CC}$)							
V_{IN}	Bias Input Supply Operating Voltage Range			5		70	V
EXTVcc	Auxiliary Bias Voltage Operating Range			5		70	V
I_Q	V_{IN} Supply Current (Shutdown Mode)	V_{IN} = 5V, RUN = 0V, $EXTV_{CC}$ = 0V			70	100	µA
	V_{IN} Supply Current (Standby Mode)	V_{IN} = 5V, RUN = 0.9V, $EXTV_{CC}$ = 0V			3		mA
Controller Operation							
V_{OUT}	Output Voltage Operating Range			1		70	V
V_{FB}	Regulated Feedback Voltage	(Note 4) ITH, ITHB Voltage = 1.2V	●	0.99	1.00	1.01	V
IV_{FB}	V_{FB} Pin Current	(Note 4)			–50	–100	nA
$V_{REFLNREG}$	Reference Voltage Line Regulation	(Note 4), V_{IN} = 12V to 72V			0.01	0.2	%
$V_{LOADREG}$	Output Voltage Load Regulation	Measure in Servo Loop, ITH = ITHB, ΔI_{TH} Voltage = 1.2V to 1.8V			0.05	0.2	%
		Measure in Servo Loop, ITH = ITHB, ΔI_{TH} Voltage = 1.2V to 0.6V			–0.05	–0.2	%
g_m	Error Amplifier Transconductance g_m	(Note 4) ITH = ITHB = 1.2V, Sink/Source = 10µA			2		mmho
g_{mb} (Buck)	Error Amplifier Transconductance g_{mb}	(Note 4) ITH = ITHB = 1.2V, Sink/Source = 10µA			1		mmho
$UVLO_DRV_{CC}$	DRV_{CC} Undervoltage Lockout	DRV_{CC} Ramping Down		3.9	4.3	4.5	V
UVLO_DRV_HYS	DRV_{CC} Undervoltage Hysteresis				0.35		V
$UVLO_INTV_{CC}$	$INTV_{CC}$ Undervoltage Lockout	$INTV_{CC}$ Ramping Down			3.95		V
UVLO_INTV_HYS	$INTV_{CC}$ Undervoltage Hysteresis				0.45		V
V_{RUN}	RUN Pin Threshold 1 (Shutdown to Standby) RUN Pin Threshold 2 (Standby to On)	V_{RUN} Rising V_{RUN} Rising		0.3 1.1	0.57 1.2	 1.3	V V
I_{RUN}	RUN Pin Source Current	V_{RUN} <0.57V 0.57V < V_{RUN} < 1.2V V_{RUN} > 1.2V			1 2 6		µA µA µA
I_{SS}	Soft-Start (SS Pin) Source Current				2.5		µA
DMAX_BG2	Maximum Duty Cycle of Boost Mode (BG2)				90		%
Inductor Current Sensing							
$V_{SENSE(ILMAX)}$	Maximum Inductor Peak Current Sense Threshold	MODE/ILIM < $INTV_{CC}$/2, ITH = ITHB = 2.1V, V_{ISNSP}– V_{ISNSD} = 25mV	●	18	25	32	mV
		MODE/ILIM > $INTV_{CC}$/2, ITH = ITHB = 2.1V, V_{ISNSP} – V_{ISNSD} = 50mV	●	40	50	60	mV
		MODE/ILIM < $INTV_{CC}$/2, ITH = ITHB = 2.1V, V_{ISNSP} = V_{ISNSD}	●	92	100	108	mV
		MODE/ILIM > $INTV_{CC}$/2, ITH = ITHB = 2.1V, V_{ISNSP} = V_{ISNSD}	●	190	200	210	mV
I_{ISNSD}	ISNSD Pin Leakage Current				0	±0.1	µA
I_{ISNSN}	ISNSN Pin Leakage Current				0	±0.1	µA
Input/Output Average Current Regulation							
I_{CSP}	CSP Pin Input Current	V_{CSP} = V_{CSN} > 5V, V_{CSP} – V_{CSN} = 50mV			14	20	µA
I_{CSN}	CSN Pin Input Current	V_{CSP} = V_{CSN} > 5V, V_{CSP} – V_{CSN} = 50mV			14	20	µA
ΔI_{CS}	CSP/CSN Pin Current Mismatch	V_{CSP} = 12V, V_{CSP} – V_{CSN} = 50mV			0.05	±1	µA
$V_{MAX(IAVG)}$	Maximum Average Current Limit	V_{CSP} = 12V	●	46.5	50	53	mV
I_{SETCUR}	SETCUR Pin Output Current			14	15	16	µA

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the specified operating junction temperature range, otherwise specifications are at T_A = 25°C. , V_{IN} = 12V, RUN > 1.25V unless otherwise noted. (Note 2)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
DRV_{CC} and $INTV_{CC}$ Linear Regulators							
$VDRV_{CC}$	DRV_{CC} Regulation Voltage	V_{IN} = 12V, $EXTV_{CC}$ = 0V V_{IN} = 5V, $EXTV_{CC}$ = 12V		6.8 6.8	7 7	7.2 7.2	V V
V_{DRVCC_LREG}	DRV_{CC} Voltage Load Regulation	$IDRV_{CC}$ = 0mA to 55mA, V_{IN} = 12V			1	2	%
V_{INTVCC}	$INTV_{CC}$ Regulation Voltage			4.8	5	5.2	V
Oscillator and Phase Locked Loop							
I_{FREQ}	FREQ Pin Output Current			9	10	11	µA
$f_{SW(MIN)}$	Low Fixed Switching Frequency	V_{FREQ} = 0V			50		kHz
$f_{SW(MAX)}$	High Fixed Switching Frequency	V_{FREQ} = 5V			800		kHz
f_{SW_SYNC}	Synchronizable Frequency	SYNC = External Clock		100		600	kHz
V_{TH_SYNC}	SYNC Pin Input Threshold	SYNC Pin Rising			1.2	2	V
		SYNC Pin Falling		0.5	0.9		V
R_{SYNC}	SYNC Pin Input Resistance to Ground				500		kΩ
	Clock Output High Voltage			4.8	5		V
	Clock Output Low Voltage				0	0.2	V
Power Good							
V_{PGOOD}	PGOOD Trip Level, V_{FB} Respect to Set Regulated Voltage	V_{FB} Ramping Negative			–10		%
		V_{FB} Ramping Positive			10		%
R_{PGOOD}	PGOOD Open Drain On-Resistance				55		Ω
I_{PGOOD}	PGOOD Leakage Current	V_{PGOOD} = 6V				±1	µA
Gate Drivers							
R_{TG1}, R_{TG2}	Top Driver Pull-Up On-Resistance	BOOST – SW = 7V			3		Ω
	Top Driver Pull-Down On-Resistance	BOOST – SW = 7V			1.5		Ω
R_{BG1}, R_{BG2}	Bottom Driver Pull-Up On-Resistance	DRV_{CC} = 7V			3.5		Ω
	Bottom Driver Pull-Down On-Resistance	DRV_{CC} = 7V			3		Ω

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: The LTC7878 is tested under pulsed load conditions such that $T_J \approx T_A$. The LTC7878A is guaranteed to meet specifications from –40°C to 125°C junction temperature. High junction temperatures degrade operating lifetimes; operating lifetime is derated for junction temperatures greater than 125°C. Note that the maximum ambient temperature consistent with these specifications is determined by specific operating conditions in conjunction with board layout, the rated package thermal impedance and other environmental factors. The junction temperature (T_J, in °C) is calculated from the ambient temperature (T_A, in °C) and power dissipation (P_D, in Watts) according to the formula: $T_J = T_A + (P_D \bullet J_A)$, where θ_{JA} (in °C/W) is the package thermal impedance.

Note 3: When V_{IN} > $EXTV_{CC}$ and $EXTV_{CC}$ > 8V, V_{BIAS} supply current is transferred to $EXTV_{CC}$ pin to reduce the total input supply quiescent current.

Note 4: The LTC7878 is tested in a feedback loop that servos V_{ITH} to a specified voltage and measures the resultant V_{FB}. The specifications at –40°C and 125°C are not tested in production and are assured by design, characterization and correlation to production testing at other temperatures.

Note 5: Dynamic supply current is higher due to the gate charge being delivered at the switching frequency. See Applications Information section.

Note 6: Rise and fall times are measured using 10% and 90% levels. Delay times are measured using 50% levels.

Note 7: The minimum on-time condition is specified for an inductor peak-to-peak ripple current > 40% of $I_{L(MAX)}$ (See Minimum On-Time Considerations in the Applications Information section).

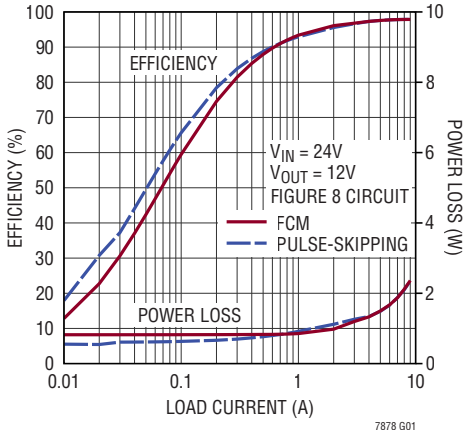
Note 8: This IC includes overtemperature protection that is intended to protect the device during momentary overload conditions. The maximum rated junction temperature will be exceeded when this protection is active. Continuous operation above the specified absolute maximum operating junction temperature may impair device reliability or permanently damage the device.

Note 9: Do not apply a voltage or current source to these pins. They must be connected to capacitive loads only, otherwise permanent damage may occur.

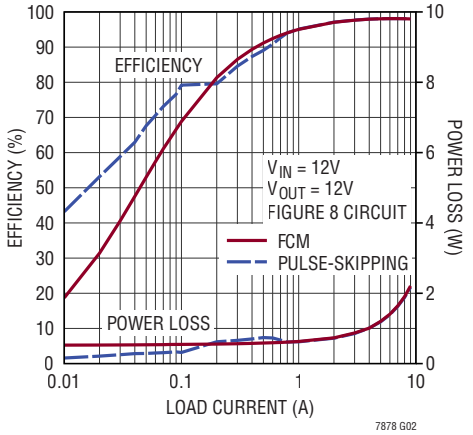
Note 10: Guaranteed by design.

TYPICAL PERFORMANCE CHARACTERISTICS T_A = 25°C, unless otherwise noted.

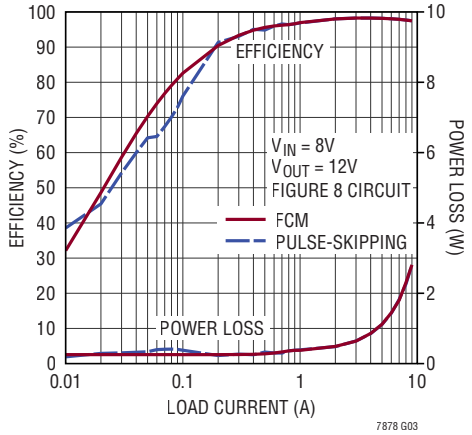
Efficiency and Power Loss vs Load Current (Buck Mode)



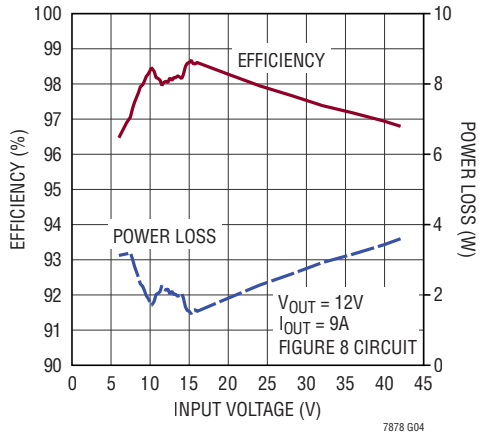
Efficiency and Power Loss vs Load Current (Buck-Boost Mode)



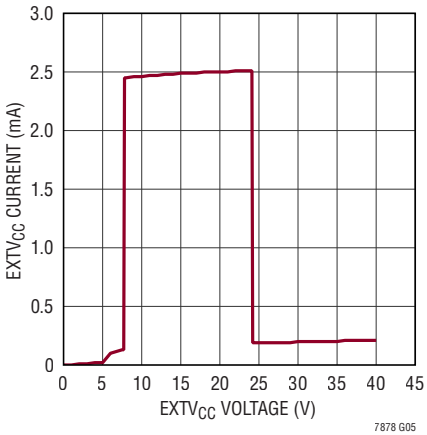
Efficiency and Power Loss vs Load Current (Boost Mode)



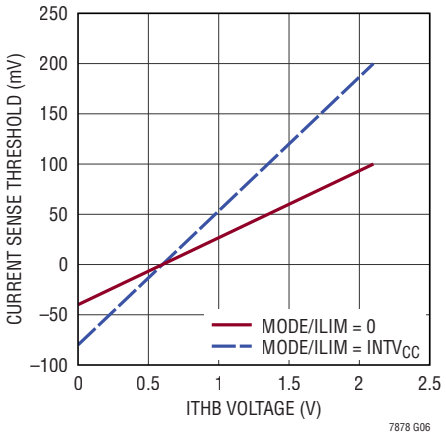
Efficiency and Power Loss vs V_{IN}



$EXTV_{CC}$ Bias Switch Over Voltage with V_{IN} = 24V, No Switching

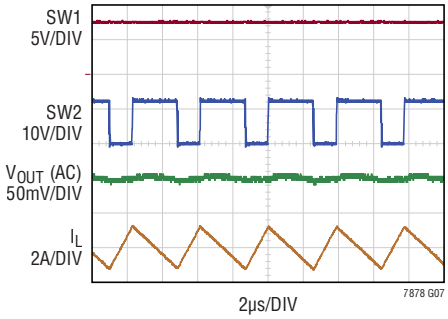


Current Sense Threshold vs ITHB Voltage



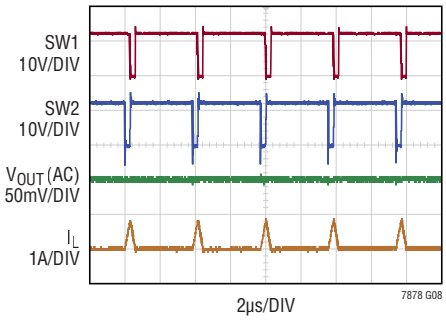
TYPICAL PERFORMANCE CHARACTERISTICS T_A = 25°C, unless otherwise noted.

Forced Continuous Mode Operation Boost Region

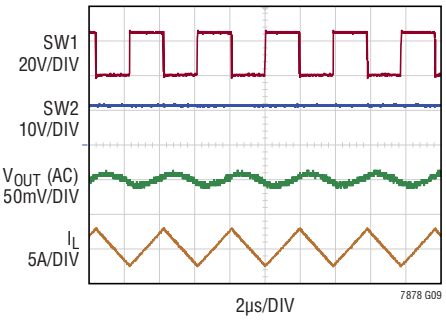


$8V_{IN}$, $12V_{OUT}$

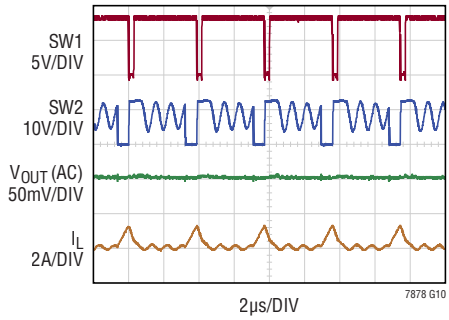
Forced Continuous Mode Operation Buck-Boost Region ($12V_{IN}$, $12V_{OUT}$)



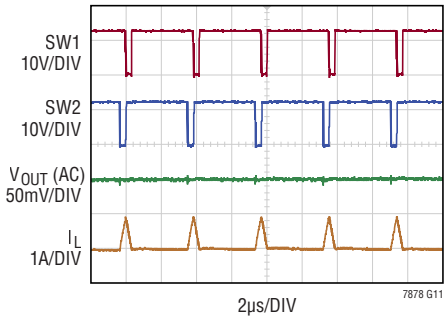
Forced Continuous Mode Operation Buck Region ($24V_{IN}$, $12V_{OUT}$)



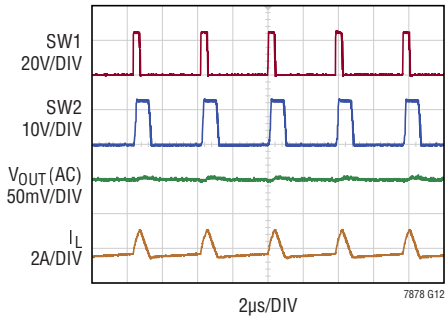
Pulse-Skipping Mode Waveforms with 100mA Load Boost Region ($8V_{IN}$, $12V_{OUT}$)



Pulse-Skipping Mode Waveforms with 100mA Load Buck-Boost Region ($12V_{IN}$, $12V_{OUT}$)

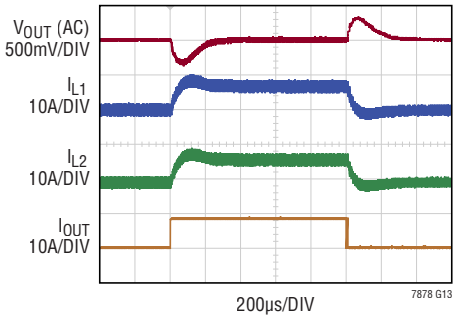


Pulse-Skipping Mode Waveforms with 100mA Load Buck Region ($24V_{IN}$, $12V_{OUT}$)

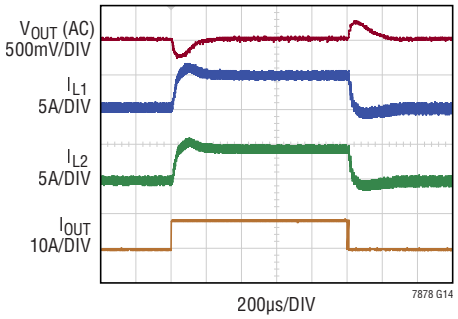


TYPICAL PERFORMANCE CHARACTERISTICS T_A = 25°C, unless otherwise noted.

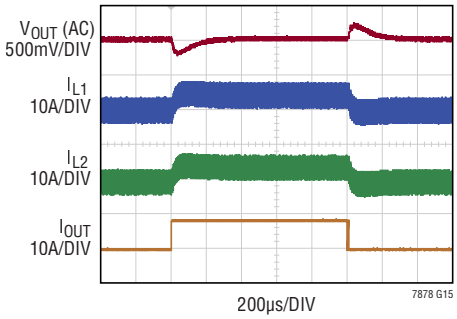
Two-Phase Parallel Operation Load Step ($8V_{IN}$, $12V_{OUT}$)



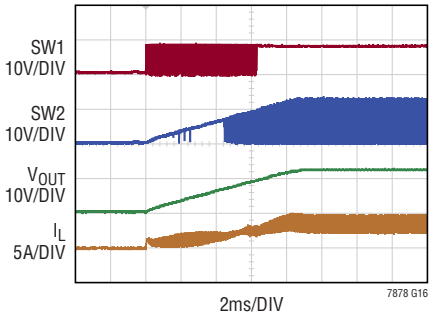
Two-Phase Parallel Operation Load Step ($12V_{IN}$, $12V_{OUT}$)



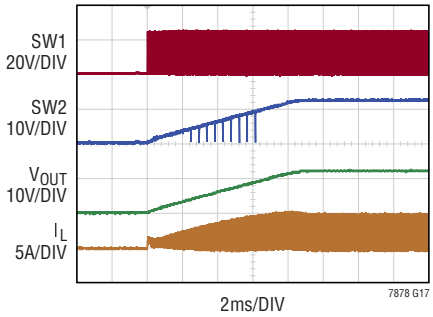
Two-Phase Parallel Operation Load Step ($24V_{IN}$, $12V_{OUT}$)



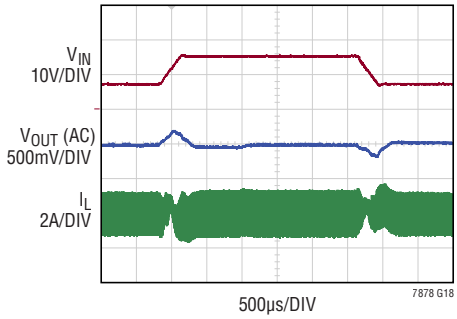
Boost Mode Start-Up with 5Ω Load ($8V_{IN}$ to $12V_{OUT}$)



Buck Mode Start-Up with 5Ω Load ($24V_{IN}$ to $12V_{OUT}$)



Input Voltage Line Transient $8V_{IN}$ to $16V_{IN}$ to $8V_{IN}$



PIN FUNCTIONS (QFN/LFCSP)

BG1, BG2 (Pins 1, 8/Pins 1, 12): Bottom Gate Driver Outputs. These pins drive the gates of the bottom N-Channel MOSFETs between PGND and DRV_{CC}.

V_{IN} (Pin 2/Pin 4): Main IC Supply. Power input to the internal LDO connect to DRV_{CC}. Bypass this pin to PGND with a capacitor (0.1µF to 1µF) close to the pin.

DRV_{CC} (Pin 3/Pin 7): Gate Driver Current Supply LDO Output. The voltage on this pin is regulated to 7V from either V_{IN} or $EXTV_{CC}$ during normal operation. Bypass this pin to PGND with a minimum of 4.7µF low ESR tantalum or ceramic capacitor.

$EXTV_{CC}$ (Pin 4/Pin 8): External Power Input to an Internal LDO Connected to DRV_{CC}. When the voltage on this pin is greater 8V and lower than the V_{IN} pin voltage, this LDO bypasses the internal LDO powered from V_{IN}. Bypass this pin to PGND with a capacitor (0.1µF to 1µF) close to the pin.

$INTV_{CC}$ (Pin 5/Pin 9): Internal 5V Regulator Output. The control circuits are powered from this voltage. Bypass this pin to SGND with a minimum of 4.7µF low ESR tantalum or ceramic capacitor.

RUN (Pin 6/Pin 10): Enable Control Input. A voltage above 1.22V turns on the IC. There is a 2µA pull-up current on this pin. Once the RUN pin rises above the 1.22V threshold, the pull-up increases to 6µA.

PGND (Pin 7/Pin 11): Power Ground Pin. Connect this pin closely to the sources of bottom N-channel MOSFETs and negative terminal of V_{IN}, DRV_{CC}, $EXTV_{CC}$ bypass capacitors.

TG2, TG1 (Pins 9, 32/Pins 14, 47): Top Gate Driver Outputs. These are the outputs of floating drivers with a voltage swing equal to DRV_{CC} superimposed on the switching nodes voltages.

BOOST2, BOOST1 (Pins 10, 31/Pins 15, 46): Bootstrapped Supplies to the Top Side Floating Drivers. Capacitors are connected between the BOOST and SW pins and Schottky diodes are tied between the BOOST and DRV_{CC} pins. Voltage swing at the BOOST1 pin is from DRV_{CC} to (V_{IN} + DRV_{CC}). Voltage swing at the BOOST2 pin is from DRV_{CC} to (V_{OUT} + DRV_{CC}).

SW2, SW1 (Pins 11, 30/Pins 16, 45): Switch Node Connections. Normally connect to the inductor terminals. SW1 swings from a Schottky diode voltage drop below ground up to V_{IN} and SW2 swings from a Schottky diode voltage drop below ground up to V_{OUT}. A bootstrap capacitor (0.1µF to 1µF) should be placed from each SW pin to the corresponding BOOST pin as close as possible.

PGOOD (Pin 12/Pin 19): Power Good Inductor Output for the Regulated Output Voltage. Open-drain logic out that is pulled down to ground when the regulated output voltage exceeds ±10% regulation window, after the internal 30µs power bad mask timer expires.

SS (Pin 13/Pin 20): Soft-Start Input. The voltage ramp rate at this pin sets the output voltage ramp rate of the regulated voltage. A capacitor to ground accomplishes soft-start. This pin has a 2.5µA pull-up current.

ITHB (Pin 14/Pin 21): Fast Transient Current Control Threshold. Optional transient response improvement configure pin based on the ITH pin voltage and operation mode. A resistor from ITHB pin to ITH pin may improve the transient response in buck mode. If no use, short ITHB pin and ITH pin together. See Applications Information section for details. Do not float this pin.

ITH (Pin 15/Pin 22): Current Control Threshold and Error Amplifier Compensation Point. The current comparator's threshold varies with the ITH control voltage. The Compensation network is from ITH pin to SGND.

V_{FB} (Pin 16/Pin 25): Output Voltage Sensing Error Amplifier Noninverting Input. This pin receives the remotely sensed feedback voltage from external resistor divider across the output voltage.

MODE/ILIM (Pin 17/Pin 26): FCM/Pulse-Skipping Mode and Inductor Current Limit Program Pin. Tying this pin to GND or $INTV_{CC}$ enables forced continuous mode operation, otherwise the controller works in the pulse-skipping mode. Tying this pin to a voltage lower than half of $INTV_{CC}$ enables the low current limit, higher than half of $INTV_{CC}$ enables the high current limit. See Applications Information section for details.

PIN FUNCTIONS (QFN/LFCSP)

PHASMD (Pin 18/Pin 27): Phase Mode Program Pin. This pin sets the phase relationship between the internal oscillator clock and the output clock on the CLKOUT pin. Tie this pin to SGND sets 180-degree phase-shift, float this pin sets 120-degree phase-shift and tie this pin to $INTV_{CC}$ sets 90-degree phase-shift. See Applications Information section for details.

FREQ (Pin 19/Pin 28): Frequency Set Pin. A resistor between this pin and SGND sets the switching frequency. This pin sources 10µA current.

CLKOUT (Pin 20/Pin 29): Clock Output Pin. Use this pin to synchronize the switching frequency of multiple LTC7878 ICs for parallel operations. Signal swings is from $INTV_{CC}$ to ground.

SYNC (Pin 21/Pin 30): Switching Frequency Synchronization Pin. Applying an external clock between 100kHz to 600kHz will cause the switching frequency to synchronize to the external clock. If SYNC is low, a resistor from the FREQ pin to SGND sets the default switching frequency. This pin has a 500k internal resistor to ground.

SETCUR (Pin 22/Pin 31): Average Current Regulation Pin. A resistor from this pin to SGND sets the maximum average input or output current sensed by the CSP and CSN pins. This pin sources 15µA current.

CSP, CSN (Pins 23, 24/Pins 34, 35): Average Current Sensing Pins. The positive/negative inputs of the internal rail-to-rail average current sense amplifier.

V_{OUT} (Pin 25/Pin 38): Floating Driver Bias Pin in Boost Mode. Supply the bias current for the BOOST1 to SW1 driver circuitry when V_{OUT} is much higher than V_{IN}.

NC (Pin 26/Pins 2, 3, 5, 6, 13, 17, 18, 23, 24, 32, 33, 36, 37, 39, 40, 44, 48): No Connect Pin.

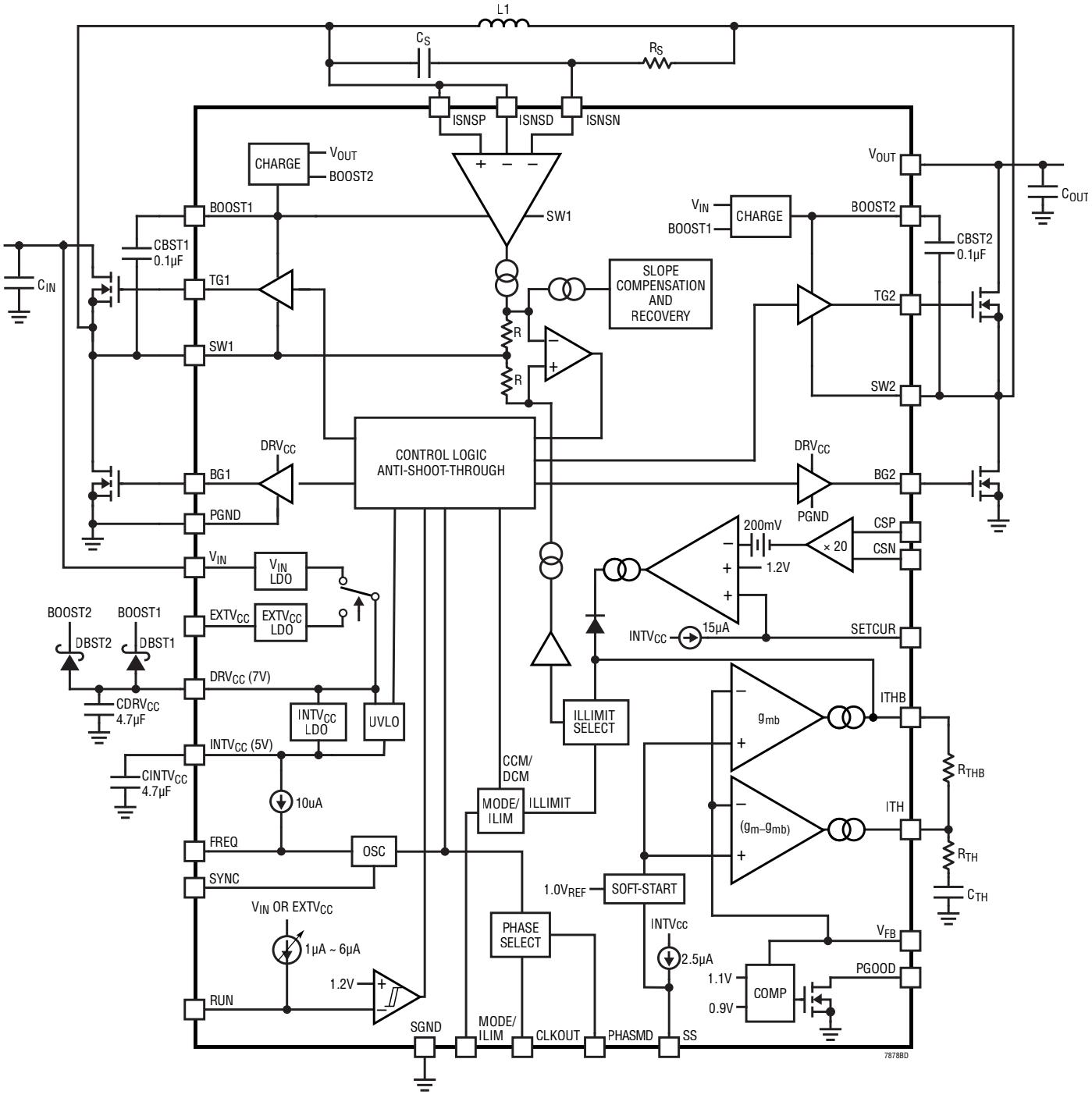
ISNSN (Pin 27/Pin 41): Negative Current Sense Comparator Inputs. The negative input of the current comparator is normally connected to the DCR sensing network.

ISNSP (Pin 28/Pin 42): Positive Current Sense Comparator Inputs. This pin must be Kelvin connected to the inductor on the switching node SW1.

ISNSD (Pin 29/Pin 43): DC Current Sense Comparator Inputs. These inputs amplify the DC portion of the sensed current signal to the IC's current comparator. If no use in large DCR applications, short ISNSD pin to ISNSP pin locally. See Applications Information section for details.

SGND (Exposed Pad Pin 33/Pin 49): Signal Ground Pin. Must be soldered to PCB ground for rated thermal performance. All small signal components e.g., $INTV_{CC}$, SS, ITH, V_{FB}, FREQ, etc. should be connected here.

BLOCK DIAGRAM



OPERATION

MAIN CONTROL LOOP

The LTC7878 is a constant-frequency, peak current mode controller for 4-switch buck-boost converters which can regulate an output voltage above, below or equal to the input voltage. The ADI proprietary current sensing and control architecture employs inductor DCR (DC Resistance) for current sensing and close loop regulation. The inductor peak current is controlled by the voltage on the ITH and ITHB pins, which is the output of the error amplifier EA. The V_{FB} pin receives the voltage feedback signal and compared with the internal 1.0V reference voltage by the EA. If the input or output average current regulation loop is implemented, the inductor current is controlled by either the output feedback voltage or the input/output average current.

DRV_{CC} POWER

Power for the top and bottom N-channel MOSFET drivers and most other internal circuitry is derived from the DRV_{CC} pin. When $EXTV_{CC}$ supply is not used, an internal 7V linear regulator supplies DRV_{CC} power from V_{IN}. If $EXTV_{CC}$ is connected to an external voltage source such as the output of the buck-boost converter, another 7V linear regulator under $EXTV_{CC}$ may be enabled and supply DRV_{CC} power. LTC7878 internally choose V_{IN} linear regulator or $EXTV_{CC}$ linear regulator to supply the DRV_{CC} based on the operation mode and supply voltages to minimize the IC power loss and reduce the IC temperature. Either V_{IN} or $EXTV_{CC}$ can supply the IC separately. If one of power supplies on V_{IN} or $EXTV_{CC}$ fails, LTC7878 can still operate normally with the other input supply on V_{IN} or $EXTV_{CC}$. Both V_{IN} and $EXTV_{CC}$ can take the voltage as high as 70V.

START-UP AND SHUTDOWN CONTROL (RUN)

The LTC7878 is in the shutdown mode when the RUN pin is pulled down and lower than 0.5V. In shutdown mode, most internal circuitry is turned off including the DRV_{CC}/$INTV_{CC}$ regulators and the LTC7878 consumes less than 100µA current. All the driver outputs are actively low to turn off the external N-channel MOSFETs. Releasing RUN allows an internal 1µA current to pull up this pin and enable the converter. When RUN pin voltage is higher than 0.5V and lower than 1.2V, the LTC7878 is in the standby mode, the DRV_{CC}/$INTV_{CC}$ regulators and all the internal circuitry are enabled but no switching. After RUN pin is higher than 1.2V, the LTC7878 is in the active mode and starts switching and regulating the output voltage. The RUN pin may be externally pulled up or driven directly by logic. Alternatively, the RUN pin can be controlled by a resistor divider from V_{IN} to SGND to achieve programmable V_{IN} UVLO (undervoltage lockout). Customers may design the converter to start-up at the pre-programmed V_{IN} voltage with different resistor divider values. Do not exceed the Absolute Maximum Ratings of 12V on the RUN pin.

The start-up of the converter's output, V_{OUT}, is controlled by the voltage on the SS pin. When the voltage on the SS pin is less than the 1.0V internal reference, the LTC7878 regulates the V_{FB} voltage to the SS voltage instead of the 1.0V reference. This allows the SS pin to be used to program soft-start by connecting an external capacitor from the SS pin to SGND. An internal 2.5µA pull-up current charges this capacitor, creating a voltage ramp on the SS pin. As the SS voltage rises linearly from 0V to 1.0V (and beyond), the output voltage V_{OUT} rises smoothly from zero to its final value. During the start-up, the LTC7878 operates in the pulse-skipping mode to avoid the negative inductor current and output voltage discharging. When RUN is pulled low to disable the controller, or when DRV_{CC} is below the undervoltage lockout threshold of 4.0V, the SS pin is pulled low by an internal MOSFET. In undervoltage lockout, the controller is disabled and the external MOSFETs are held off.

POWER SWITCH CONTROL

The simplified Block Diagram shows how the four power switches are connected to the inductor, V_{IN}, V_{OUT} and GND. LTC7878 operates in buck region ($V_{IN} >> V_{OUT}$), boost region ($V_{IN} << V_{OUT}$) and buck-boost region ($V_{IN} \approx V_{OUT}$) without sensing the V_{IN} and V_{OUT} voltage. The power switches are properly controlled so the transfer between regions is continuous and smooth.

OPERATION

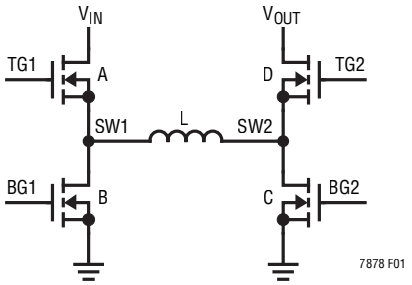


Figure 1. Simplified Diagram of the Output Switches

Buck Region (V_{IN} >> V_{OUT})

Switch D is always on and switch C is always off in this region. Switches A and B will alternate, behaving like a typical synchronous buck regulator. LTC7878 operates like a conventional buck controller with peak current mode control. The inductor peak current is regulated and proportional to the voltage on the ITH/ITHB pin. As the input voltage decreases and close to the output voltage, the duty cycle of the switch A in buck mode increases. Until the duty cycle reaches 83%, the LTC7878 will enter buck-boost region as the input voltage keeps decreasing.

Buck – Boost Region (V_{IN} ≈ V_{OUT})

When V_{IN} is close to V_{OUT}, the controller enters buck-boost region. To maintain peak current mode control, the current comparator needs to be tripped each cycle by the inductor peak current. However, at V_{IN} = V_{OUT}, the inductor current is flat and has no peak to trip the current comparator in buck or boost mode operation. To create an inductor peak current, when the duty cycle is larger than 83% in buck mode operation and the current comparator has not been tripped, switches A and C will be turned on to force inductor current ramping up quickly until the current comparator tripped. The peak inductor current is still controlled by the voltage on the ITH/ITHB pin with cycle by cycle peak current limit. As the input voltage keeps decreasing and the buck mode duty cycle reaches 100%, the LTC7878 enters boost mode naturally.

Boost Region (V_{IN} << V_{OUT})

Switch A is always on and synchronous switch B is always off in the boost region. Switches C and D will alternate, behaving like a typical synchronous boost regulator. LTC7878 operates like a conventional peak current mode control boost controller. In every cycle, switch C is turned on first, the inductor current is regulated and proportional to the voltage on the ITH/ITHB pin with same peak current limit as the buck mode. The maximum duty cycle of the switch C in boost mode operation is around 92%.

PULSE-SKIPPING MODE AND LIGHT LOAD CURRENT OPERATION (MODE/ILIM PIN)

LTC7878 can be set to enter pulse-skipping mode or FCM using MODE/ILIM pin. To select forced continuous operation, tie the MODE/ILIM pin to SGND or $INTV_{CC}$. To select pulse-skipping mode of operation, tie the MODE/ILIM pin to a voltage of 2/3 of $INTV_{CC}$ (e.g., a 10k/20k resistor divider from $INTV_{CC}$ to SGND) or leave it float. The MODE/ILIM pin is a multi-functional pin. It not only sets the operation mode but also programs the peak current limits. LTC7878 uses the inductor DCR for current sensing, the maximum voltage drop through the DCR is limited to 100mV/200mV if ISNSD is shorted to ISNSP. Refer to Table 1 for the MODE/ILIM pin setup.

Table 1.

MODE/ILIM PIN	MAXIM CURRENT SENSE THRESHOLD (ISNSD SHORT TO ISNSP)	OPERATION MODE
SGND	100mV	Forced Continuous Mode
Float	100mV	Pulse-Skipping Mode
2/3 $INTV_{CC}$	200mV	Pulse-Skipping Mode
$INTV_{CC}$	200mV	Forced Continuous Mode

When the LTC7878 is in the FCM, the light load operation is the same as the heavy load operation with a constant switching frequency and the output voltage ripple is minimized. When the LTC7878 enters pulse-skipping mode at light load conditions, the inductor current is not allowed to reverse, and the synchronous switch D is held off whenever reverse current on the inductor is detected. At very light loads, the current comparator may remain tripped for many cycles and force switch A and C to stay off for the same number of cycles (i.e., skipping pulses). In buck-boost region, the LTC7878 may switch several

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cycles and then keep skipping pulses for longer time at light loads until the control loop pull the ITH/ITHB high. The pulse-skipping mode decreases the switching frequency thus improves efficiency but may cause larger output voltage ripple at light loads.

OUTPUT OVERVOLTAGE OPERATION

If the output voltage is higher than the value commanded by the V_{FB} resistor divider, the LTC7878 will respond according to the mode and region of operation. In continuous conduction mode, the LTC7878 will sink current into the input. If the input supply is capable of sinking current, the LTC7878 will allow the reverse inductor current to be sunk into the input. The maximum valley current of the reverse inductor current is approximately 40% of the maximum peak inductor current in the positive direction. In pulse-skipping mode, switching will stop and the output will be allowed to remain high.

CONSTANT-CURRENT REGULATION (CSP/CSN/ SETCUR PINS)

The LTC7878 provides a constant-current regulation loop for either input or output average current. A sensing resistor close to the input or output capacitor can be used to sense the input or output current. Because the input or output current may be a pulse current in the different operation regions, A RC filter has to be applied on CSP and CSN pins for average current sensing. When the voltage on the current sensing resistor exceeds the programmed current limit, the voltage on the ITH/ITHB pin will be pulled low to decrease the inductor current and maintain the desired maximum input or output current. The current limit may be set by the voltage on the SETCUR pin from 0.2V to 1.2V corresponding to the linearly 0mV to 50mV current limit on the sensing resistor. There is a 15µA current out of the SETCUR pin and if the SETCUR pin is float or SETCUR pin voltage higher than 1.2V, the current limit is clamped at 50mV internally. The input current limit function prevents overloading the DC input source, while the output current limit provides a building block for battery charger or LED driver applications. It can also serve as an extra current limit protection for a constant-voltage regulation application. The input/output current limit function has an operating voltage range of GND to the absolute maximum V_{OUT}/V_{IN} (72V).

FREQUENCY SELECTION AND PHASE-LOCKED LOOP (FREQ, SYNC, PHASMD AND CLKOUT PINS)

The selection of switching frequency is a trade-off between efficiency and component size. Low frequency operation increases efficiency by reducing MOSFET switching losses but requires larger inductance and/or capacitance to maintain low output ripple voltage. The switching frequency of the LTC7878's controllers can be selected using the FREQ pin. If the SYNC pin is not being driven by an external clock source, the FREQ pin can be used to program the controller's operating frequency from 100kHz to 600kHz. Switching frequency is determined by the voltage on the FREQ pin. Since there is a precision 10µA current flowing out of the FREQ pin, the user can program the controller's switching frequency with a single resistor to SGND (e.g., the FREQ pin voltage is 1V with 100k resistor from the FREQ pin to SGND). A curve in Figure 2 is provided to show the relationship between the voltage on the FREQ pin and the switching frequency.

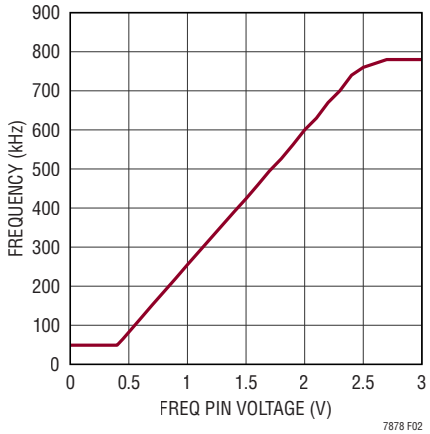


Figure 2. Relationship Between Switching Frequency and Voltage at FREQ Pin

A phase-locked loop (PLL) is integrated on the LTC7878 to synchronize the internal oscillator to an external clock source driving the SYNC pin. The PLL is capable of locking to any frequency within the range of 100kHz to 600kHz. The frequency setting resistor at FREQ pin should

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always be present to set the controller's initial switching frequency before locking to the external clock or in any cases the external clock is missing during the operation. The CLKOUT pin is a clock signal output with the same frequency as the internal oscillator with phase shift programmed by the PHASMD pin. It may be used in multi-IC parallel applications by passing the clock signal of the first IC to the SYNC pin of the second IC for frequency synchronization. The phase shift can be programmed based on Table 2.

Table 2.

PHASMD PIN	CLKOUT PHASE-SHIFT REFER TO THE INTERNAL OSCILLATOR
SGND	180°
Float	120°
$INTV_{CC}$	90°

POWER GOOD (PGOOD PIN)

The PGOOD pin is connected to the open-drain of an internal N-channel MOSFET. When V_{FB} is not within ±10% of the 1.0V reference voltage, the PGOOD pin is pulled low. The PGOOD pin is also pulled low when RUN is below 1.22V or when the LTC7878 is in the soft-start phase. There is an internal 30µs power good or bad mask when V_{FB} goes in or out of the ±10% window. The PGOOD pin can be pulled up by an external resistor to $INTV_{CC}$ or an external source of up to 6V.

SHORT-CIRCUIT PROTECTION, CURRENT LIMIT AND CURRENT LIMIT FOLDBACK

The maximum peak current threshold of the controller is limited by a voltage clamp on the ITH/ITHB pin. In normal operations, the ITH/ITHB voltage varies from 0.6V to 2.1V corresponding to the peak inductor current sensing voltage 0mV to 100mV (MODE/ILIM tied to SGND and ISNSD tied to ISNSP). The LTC7878 includes current foldback to help limit load current when the output is shorted to ground. If the output falls below 40% of its nominal output level, then the maximum sense voltage is progressively lowered from its maximum value to one-fifth of the maximum value. Foldback current limiting is disabled during the soft start-up. Under short-circuit conditions, the LTC7878 will limit the current by operating as a buck with very low duty cycles, and by skipping cycles. In this situation, synchronous switch B will dissipate most of the power (but less than in normal operation).

COMPENSATION LOOP AND FAST TRANSIENT RESPONSE (ITH, ITHB PINS)

The LTC7878 uses an internal transconductance error amplifier, the output of which, ITH, compensates the control loop. The external inductor, output capacitor, and the compensation resistor and capacitor determine the loop stability. The compensation design is similar to the traditional buck or boost converter with peak current mode control. For a typical voltage regulator application, a 5k resistor series with a 10nF compensation capacitor on the ITH pin to SGND is adequate and a good starting point.

The LTC7878 has a transient improvement function implemented with ITH and ITHB pins. In normal operation, short the ITHB and ITH pin together and place the RC compensation network from ITH/ITHB to SGND. This will disable the transient improvement circuit and LTC7878 behaves like a conventional peak current mode controller. The RC compensation decides the bandwidth of the close loop regulation and transient responses. To cover the wide input voltage range, the compensation has to be designed based on the minimum V_{IN} in the boost mode operation for stability. The transient response in the buck mode may be limited by the slow compensation designed for boost mode. To improve the transient response in buck mode, a single resistor may be connected from ITH to ITHB. Another g_m amplifier driving the ITHB pin in buck mode and further amplify the error between V_{FB} and internal reference voltage during transient, so the peak current threshold voltage moves faster. The resistance between ITH and ITHB need to be experimental verified and it is normally in the range of 1 to 5 times of the resistance used in the compensation network from ITH to SGND.

APPLICATIONS INFORMATION

The Typical Application on the first page is a basic LTC7878 application circuit. Detailed external components may be referred to the Figure 8. External component selection is driven by the load requirement and begins with the selection of the inductor value and DCR. Next, the power MOSFETs are selected. Finally, C_{IN} and C_{OUT} are selected. This circuit can be configured for operation up to an input voltage of 70V.

Inductor Selection and DCR Current Sensing

The inductor selection and operating frequency are interrelated in that higher operating frequencies allow the use of smaller inductor and capacitor values but with higher switching losses. The inductor value also has a direct effect on ripple current. Since LTC7878 is a constant-frequency peak current mode controller, the inductor peak current is regulated and limited cycle-by-cycle. The inductor should be selected with saturation current higher than the maximum peak current. The maximum output DC current in the buck mode is the peak inductor current minus half of the ripple current. In the boost mode, the maximum output DC current varies with duty cycle and ripple current. Too large ripple current will reduce the maximum output current and too small ripple may cause the small current sense signal and more sensitive to the switching noise. Typically, set the inductor current ripple ΔI_L to 30% to 60% of the maximum DC inductor current at the nominal input voltage is a good starting point. If the buck-boost converter only operates in buck mode and buck-boost mode, the maximum DC inductor current is about the maximum output load current. Otherwise, the maximum DC inductor current is the inductor current in the boost mode with minimum V_{IN} at the maximum load condition. And it can be calculated as:

$$I_L = I_{LOAD(MAX)} \frac{V_{OUT}}{V_{IN}}$$

LTC7878 uses the inductor DCR (DC Resistance) for current sensing and close loop regulation. After selecting the inductance and saturation current, the DCR of the inductor also need to be properly chosen to achieve the required output current and current limit. To sense the inductor current with a large DCR, ISNSD pin may be short to the ISNSP pin to achieve 100mV or 200mV current sense threshold limits. Choose the DCR of the inductor so that the peak current is less than the saturation current but higher than the maximum DC current plus the ripple current.

$$DCR \le \frac{V_{SENSE(MAX)}}{I_{LOAD(MAX)} + \frac{\Delta I_L}{2}}$$

Filter components, especially capacitors, must be placed close to the LTC7878, and the sense lines should run close together to a Kelvin connection underneath the current sense element (Figure 3). And in Figure 4, the external R1 • C1 time constant is chosen to be exactly equal to the L/DCR time constant, the voltage drop across the external capacitor is equal to the drop across the inductor DCR. C1 is usually selected to be in the range of 0.047µF to 0.47µF. For example, a 4.7µH/10mΩ inductor and C1= 0.047uF, the R1 should be L/(DCR • C1) = 10kΩ. The maximum peak inductor current is V_{SENSE}/DCR = (100mV or 200mV)/10mΩ = 10A or 20A depend on the MODE/ILIM pin setup. To further tune the current limit, another resistor may be paralleled with C1 to form a resistor divider with R1 and scale the sensed voltage. Refer to the standard DCR setup in buck controller data sheet (e.g. LTC3855) for details.

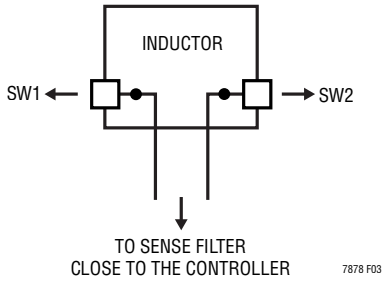


Figure 3. Sense Lines Placement with Inductor DCR

APPLICATIONS INFORMATION

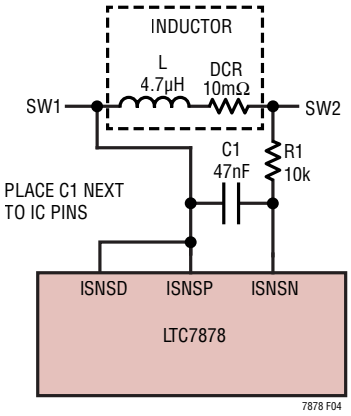


Figure 4. Inductor DCR Current Sensing

To properly dimension the external filter components, the DCR of the inductor must be known. It can be measured using a good RLC meter, but the DCR tolerance is not always the same and varies with temperature. To ensure that the application will deliver full load current over the full operating temperature range, use the manufacturer's maximum value, usually given at 20°C. Increase this value to account for the temperature coefficient of resistance, which is approximately 0.4%/°C. A conservative value for $T_{L(MAX)}$ is 100°C. Consult the manufacturers' data sheets for detailed information.

To maintain a good signal-to-noise ratio for the current sense signal, it suggested to have a minimum ΔV_{SENSE} larger than 10mV. For a DCR sensing application, the minimum sensed ripple voltage ΔV_{SENSE} may be estimated by the equation:

$$\Delta V_{SENSE} = DCR \bullet \Delta I_{L(MIN)}$$

In high current applications, a low DCR inductor is preferred for higher efficiency. LTC7878 is designed to sense the low DCR inductor current using ADI proprietary sensing method without sacrificing the signal-to-noise ratio. The low DCR current sensing requires another RC filter and ISNSD pin. As shown in the Figure 5.

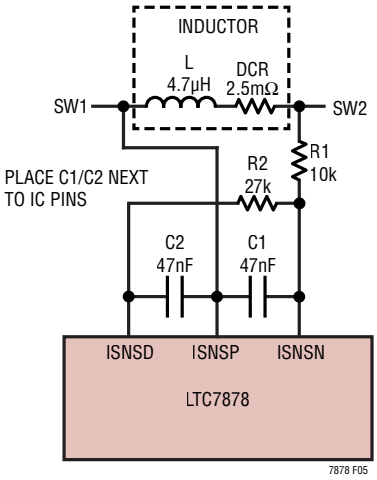


Figure 5. Small Inductor DCR Current Sensing

The external R1 • C1 time constant is chosen to be equal to the L/(4 • DCR) time constant. If the C1 = C2, the R2 = 3 • 0.9 • R1 = 2.7 • R1. For example, a 4.7µH/2.5m inductor and C1 = 0.047µF, the R1 should be L/(4 • DCR • C1) = 10kΩ, and R2 should be 2.7 • R1 = 27kΩ. With this setup, the voltage drop on the inductor DCR is sensed and amplified 4 times larger inside the IC to compared with 100mV or 200mV current threshold limits. Thus, the equivalent maximum current sense voltage V_{SENSE} is limited to 100mV/4 = 25mV or 200mV/4 = 50mV. And the maximum inductor current is V_{SENSE}/DCR = 25mV/2.5mΩ = 10A if MODE/ILIM = 0. Note, in this condition, the sensed ripple voltage is amplified 4 times larger and the ΔV_{SENSE} may be estimated by the equation:

$$\Delta V_{SENSE} = 4 \bullet DCR \bullet \Delta I_{L(MIN)}$$

LTC7878 can also work with the R_{SENSE} for precised current sensing. Both R_{SENSE} and DCR current sensing require ISNSP pin Kelvin connection to the inductor/R_{SENSE} left terminal and short to SW1. The ISNSP pin and SW1 pin must be electrically shorted together. Please contact factory or field application for supporting on detailed R_{SENSE} setup.

For high efficiency, choose an inductor with low core loss, such as ferrite. Also, the inductor should have as low

APPLICATIONS INFORMATION

DC resistance as possible to reduce the I^2R losses and must be able to handle the peak inductor current without saturating. To minimize radiated noise, use a toroid, pot core or shielded bobbin inductor.

Set Output Voltage

The LTC7878 output voltage is set by an external feedback resistive divider carefully placed across the output capacitor. The resultant feedback signal is compared with the internal precision 1.0V voltage reference by the error amplifier. The output voltage is given by the equation:

$$V_{OUT} = 1.0V \bullet \left(1 + \frac{R2}{R1}\right)$$

where R2 is connected to V_{OUT} and R1 is connected to SGND.

Program Average Input/Output Current Limit

As shown in Figure 6 and Figure 7, input/output average current sense resistor R_{SENSE} should be placed between the bulk capacitor for V_{IN}/V_{OUT} and the decoupling capacitor. A lowpass filter formed by R_F and C_F is recommended to reduce the switching noise and stabilize the current loop. Due to the same current on the SCP/CSN pins, the filter resistors R_F on CSP and CSN must be the same value. With the typical 100Ω resistors shown here, the value of capacitor CF should be 1µF to 2.2µF to filter the pulsed input/output current at the switching frequency. The current loop's transfer function should approximate that of the voltage loop. Crossover frequency should be one-tenth the switching frequency, and gain should decrease by 20dB/decade. Similar current and voltage loop transfer functions will ensure overall system stability.

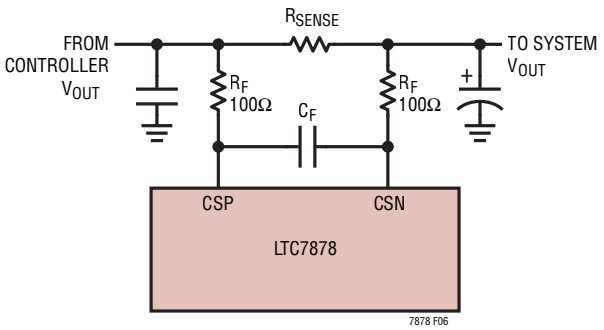


Figure 6. Programming Average Output Current Limit

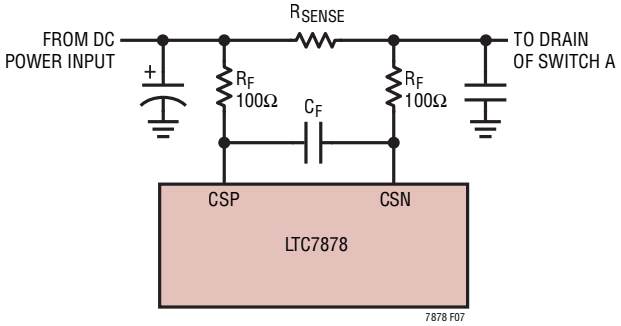


Figure 7. Programming Average Input Current Limit

The input/output current limit is set by the SETCUR pin linearly for 0.2V to 1.2V. The SETCUR pin voltage is internally clamped to 1.2V if SETCUR pin voltage is higher than 1.2V. The sensed voltage between CSP and CSN is amplified 20 times internally and plus 200mV offset to compare with the voltage on the SETCUR pin. When the sensed voltage is higher than the SETCUR voltage, the ITH/ITHB pin voltage is pulled low to decrease the inductor current and maintain the current loop regulation. Since the SETCUR pin voltage is internally clamped to 1.2V, the maximum sensed voltage between SCP and CSN is limited to (1.2V – 0.2V)/20 = 50mV.

If input/output average current limit is not desired, the CSP and CSN pins should be shorted together and tied to SGND, and the SETCUR pin should be tied to $INTV_{CC}$ or float.

C_{IN}/C_{OUT} Selection

In the boost region, input current is continuous. In the buck region, input current is discontinuous. In the buck region, the selection of input capacitor C_{IN} is driven by the need to filter the input square wave current. Use a low ESR capacitor sized to handle the maximum RMS current. For buck operation, the input RMS current is given by:

$$I_{RMS} \approx I_{OUT(MAX)}\ OUT \bullet \frac{V_{OUT}}{V_{IN}} \bullet \sqrt{\frac{V_{IN}}{V_{OUT}} - 1}$$

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This formula has a maximum at $V_{IN} = 2V_{OUT}$, where $I_{RMS} = I_{OUT(MAX)}/2$. This simple worst-case condition is commonly used for design because even significant deviations do not offer much relief. Note that ripple current ratings from capacitor manufacturers are often based on only2000 hours of life which makes it advisable to derate the capacitor.

In the boost region, the discontinuous current shifts from the input to the output, so C_{OUT} must be capable of reducing the output voltage ripple. The effects of ESR (equivalent series resistance) and the bulk capacitance must be considered when choosing the right capacitor for a given output ripple voltage. The steady ripple due to charging and discharging the bulk capacitance is given by:

$$RIPPLE_{(BOOST,CAP)} = I_{OUT(MAX)} \bullet \left(\frac{V_{OUT} - V_{IN(MIN)}}{C_{OUT} \bullet V_{OUT} \bullet f} \right)$$

where C_{OUT} is the output capacitor and f is the switching frequency.

The steady ripple due to the voltage drop across the ESR is given by:

$$\Delta V_{BOOST,ESR} = I_{OUT(MAX,BOOST)} \bullet ESR$$

In buck mode, V_{OUT} ripple is given by:

$$\Delta V_{OUT} \leq \Delta I_L \bullet \frac{ESR + 1}{8 \bullet f \bullet C_{OUT}} \quad (9)$$

Multiple capacitors placed in parallel may be needed to meet the ESR and RMS current handling requirements. Dry tantalum, special polymer, aluminum electrolytic and ceramic capacitors are all available in surface mount packages. Ceramic capacitors have excellent low ESR characteristics but can have a high voltage coefficient. Capacitors are now available with low ESR and high ripple current ratings, such as OS-CON and POSCAP.

Power MOSFET Selection

The LTC7878 requires four external N-channel power MOSFETs, two for the top switches (switches A and D, shown in Figure 1) and two for the bottom switches (switches B and C, shown in Figure 1). Important parameters for the power MOSFETs are the breakdown voltage VBR,DSS, threshold voltage VGS,TH, on-resistance $RDS_{(ON)}$, reverse transfer capacitance CRSS and maximum current $I_{DS(MAX)}$. For switches A and B on the input side, the breakdown voltage VBR,DSS must be higher than the input voltage. For switches C and D on the output side, the breakdown voltage must be higher than the output voltage. The LTC7878 MOSFETs driver voltage at DRV_{CC} pin is 7V which can drive either logic level (VGS,TH > 1.5V) or normal level (VGS,TH > 3V) threshold MOSFETs. **Do NOT** use super logic level and ultra logic level MOSFET where the threshold voltage is less than 1.5V ($V_{GS,TH}$ < 1.5V).

In order to select the power MOSFETs, the power dissipated by the device must be known. For switch A, the maximum power dissipation happens in the boost region, when it remains on all the time. Its maximum power dissipation at maximum output current is given by:

$$P_{A,BOOST} = \left(\frac{I_{OUT(MAX)} \bullet V_{OUT}}{V_{IN}} \right)^2 \bullet \rho_\tau \bullet R_{DS(ON)}$$

Where $\rho\tau$ is a normalization factor (unity at 25°C) accounting for the significant variation in on-resistance with temperature, typically about 0.4%/°C. For a maximum junction temperature of 125°C, using a value $\rho\tau$ = 1.5 is reasonable.

Switch B operates in the buck region as the synchronous rectifier. Its power dissipation at maximum output current is given by:

$$P_{B,BUCK} = I_{OUT(MAX)}{}^2 \bullet \rho\tau \bullet R_{DS(ON)} \bullet \frac{V_{IN} - V_{OUT}}{V_{IN}}$$

Switch C operates in the boost region as the control switch. Its power dissipation at maximum current is given by:

$$P_{C,BOOST} = I_{OUT(MAX)}{}^2 \bullet \rho\tau \bullet R_{DS(ON)} \bullet \frac{V_{OUT} - V_{IN}}{V_{IN}{}^2} + k \bullet I_{OUT(MAX)} \bullet C_{RSS} \bullet f \bullet \frac{V_{OUT}{}^3}{V_{IN}}$$

where C_{RSS} is usually specified by the MOSFET manufacturers. The constant k, which accounts for the loss caused

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by reverse recovery current, is inversely proportional to the gate drive current and has an empirical value of 1.7.

For switch D, the maximum power dissipation happens in the boost region, when its duty cycle is higher than 50%. Its maximum power dissipation at maximum output current is given by:

$$P_{D,BOOST} = \frac{I_{OUT(MAX)} \bullet V_{OUT}^{2}}{V_{IN}} \bullet \rho\tau \bullet R_{DS(ON)} \bullet \frac{V_{IN}}{V_{OUT}}$$

For the same output voltage and current, switch A has the highest power dissipation and switch B has the lowest power dissipation unless a short occurs at the output. From a known power dissipated in the power MOSFET, its junction temperature can be obtained using the following formula:

$$T_J = T_A + P \bullet R_{TH(JA)}$$

The $R_{TH(JA)}$ to be used in the equation normally includes the $R_{TH(JC)}$ for the device plus the thermal resistance from the case to the ambient temperature ($R_{TH(JC)}$). This value of T_J can then be compared to the original, assumed value used in the iterative calculation process.

Top MOSFET Driver Supply

Refer to the Block Diagram, the external bootstrap capacitors C_{BST1} and C_{BST2} connected to the BOOST1 and BOOST2 pins supply the gate drive voltage for the topside MOSFET. When the top switch A turns on, the switch node SW1 rises to V_{IN} and the BOOST1 pin rises to approximately V_{IN} + DRV_{CC}. When the bottom switch B turns on, the switch node SW1 drops to low and the boost capacitor C_{BST1} is charged through diode D_{BST1} from DRV_{CC}. When the top switch D turns on, the switch node SW2 rises to V_{OUT} and the BOOST2 pin rises to approximately V_{OUT} + DRV_{CC}. When the bottom switch C turns on, the switch node SW2 drops to low and the boost capacitor C_{BST2} is charged through diode DBST2 from DRV_{CC}. The boost capacitors C_{BST1} and C_{BST2} need to store about 100 times the gate charge required by the top switches A and D. In most applications, a 0.1µF to 0.47µF, X5R or X7R dielectric capacitor is adequate. The low leakage Schottky diodes D_{BST1} and D_{BST2} must be able to handle the top driver current. Due to the large duty cycle and short on-time of BG1/BG2 when V_{IN} is close to V_{OUT}, the pulse current on D_{BST1} and D_{BST2} could be higher than 100mA. It is suggested that the current capability of D_{BST1} and D_{BST2} higher than 100mA. The D_{BST1} reverse breakdown voltage must be greater than V_{IN} and D_{BST2} reverse breakdown voltage must be greater than V_{OUT}.

DRV_{CC} Regulators and $EXTV_{CC}$

The LTC7878 features a P-channel MOSFET LDO that supplies power to DRV_{CC} from the V_{IN} supply. DRV_{CC} powers the gate drivers and most of the LTC7878's internal circuitry. The linear regulator regulates the voltage at the DRV_{CC} pin to 7V when V_{IN} voltage is greater than 7V. $EXTV_{CC}$ connects to DRV_{CC} through another P-channel MOSFET LDO and can also regulate the DRV_{CC} to 7V. LTC7878 internally choose the efficient LDO between V_{IN} and $EXTV_{CC}$ to reduce the IC temperature. Both LDOs can supply the driver current and must be bypassed to ground with a minimum of 4.7µF ceramic capacitor or low ESR electrolytic capacitor. Good bypassing is needed to supply the high transient currents required by the MOSFET gate drivers.

High input voltage applications in which large MOSFETs are being driven at high frequencies may cause the maximum junction temperature rating for the LTC7878 to be exceeded. The DRV_{CC} current, which is dominated by the gate charge current, may be supplied by the linear regulator either from V_{IN} or from $EXTV_{CC}$. Power dissipation for the IC in this case is highest and is equal to (V_{IN} or $EXTV_{CC}$) • I_{DRVCC}. The gate charge current is dependent on operating frequency, as discussed in the Efficiency Considerations section. The junction temperature can be estimated by using the equations given in Note 3 of the Electrical Characteristics table. For example, the LTC7878 DRV_{CC} current is 40mA from a 12V~60V V_{IN} supply and no $EXTV_{CC}$ supply, the worst-case junction temperature at room temperature can be calculated by:

$$T_J = 25°C + (40mA)(60V)(34°C/W) = 106.6°C$$

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To prevent the maximum junction temperature from being exceeded, the input supply current must be checked while operating in continuous conduction mode at maximum V_{IN}. If the output voltage of the above example converter is 24V and it is connected to $EXTV_{CC}$ pin. When the voltage applied to $EXTV_{CC}$ rises above 7.5V, the DRV_{CC} linear regulator from V_{IN} is turned off and the linear regulator from $EXTV_{CC}$ is turned on. Using $EXTV_{CC}$ allows the MOSFET driver and control power to be derived from the LTC7878's switching regulator output during normal operation and from the V_{IN} when the output is out of regulation (e.g., start-up, short-circuit). Significant efficiency and thermal gains can be realized by powering $EXTV_{CC}$ from the 24V output, which reduces the junction temperature in the previous example from 106.6°C to 57.6°C:

$$T_J = 25°C + (40mA)(24V)(34°C/W) = 57.6°C$$

Powering $EXTV_{CC}$ from the output can also provide enough gate drive when V_{IN} drops below 7V. This allows a wider operating range for V_{IN} after the controller start into regulation. If both input and output voltages are high voltages such as 40V, an external low voltage (8V ~ 10V) bias supply is suggested to be used on the $EXTV_{CC}$ pin for better efficiency and thermal performance.

Undervoltage Lockout

The LTC7878 has two ways that help protect the controller in case of undervoltage conditions. A precision UVLO comparator constantly monitors the DRV_{CC} voltage to ensure that an adequate gate-drive voltage is present. It locks out the switching action when DRV_{CC} is below 4.3V. To prevent oscillation when there is a disturbance on the DRV_{CC}, the UVLO comparator has 350mV of precision hysteresis.

Another way to detect an undervoltage condition is to monitor the V_{IN} supply. Because the RUN pin has a precision turn-on reference of 1.2V, one can use a resistor divider from V_{IN} to turn on the IC when V_{IN} is high enough. An extra 4µA of current flows out of the RUN pin once its voltage passes 1.22V. One can program the hysteresis of the run comparator by adjusting the values of the resistive divider. To drive the non-logic level MOSFETs with higher threshold voltages, it is suggested to set the V_{IN} UVLO higher than 7V using RUN pin for enough gate drive voltage.

Soft Start-Up Function

When a capacitor is connected to the SS pin, a soft-start current of 2.5µA starts to charge the capacitor. A soft-start function is achieved by controlling the output ramp voltage according to the ramp rate on the SS pin. Current foldback is disabled during this phase to ensure smooth soft-start. When the chip is in the shutdown state with its RUN pin voltage below 1.22V, the SS pin is actively pulled to ground. The soft-start range is defined to be the voltage range from 0V to 1.0V on the SS pin. The total soft-start time can be calculated as:

$$t_{SOFT\text{-}START} = 1.0 \bullet \frac{C_{SS}}{2.5\mu A}$$

Regardless of the mode selected by the MODE/ILIM pin, the regulator will always start in pulse-skipping mode up to SS = 1.0V.

Fault Conditions: Current Limit and Current Foldback

The maximum inductor current is inherently limited in a current mode controller by the maximum sense voltage. With 100mV current limit setup (MODE/ILIM tie to ground and ISNSD short to ISNSP), maximum sense voltage and the inductor DCR determine the maximum allowed inductor peak current, which is:

$$I_{L(PEAK)} = \frac{100mV}{DCR}$$

To further limit current in the event of a short circuit to ground, the LTC7878 includes foldback current limiting. If the output falls by more than 40%, then the maximum sense voltage is progressively lowered to about one-fifth of its full value.

Efficiency Considerations

The percent efficiency of a switching regulator is equal to the output power divided by the input power times 100%. It is often useful to analyze individual losses to determine what is limiting the efficiency and which change would

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produce the most improvement. Although all dissipative elements in circuit produce losses, four main sources account for most of the losses in LTC7878 circuits.

1. DC I^2R Losses. These arise from the resistances of the MOSFETs, sensing resistor, inductor and PC board traces and cause the efficiency to drop at high output currents.
2. MOSFET Transition Loss. This loss arises from the brief amount of time switch A or switch C spends in the saturated region during switch node transitions. It depends upon the input voltage, load current, driver strength and MOSFET capacitance, among other factors.
3. DRV_{CC} Current. This is the sum of the MOSFET driver and control currents. This loss can be reduced by supplying DRV_{CC} current through the $EXTV_{CC}$ pin from a high efficiency source, such as the output (if $7V < V_{OUT} = < 20V$) or alternate low voltage supply if available.
4. C_{IN} and C_{OUT} Loss. The input capacitor has the difficult job of filtering the large RMS input current to the regulator in buck mode. The output capacitor has the more difficult job of filtering the large RMS output current in boost mode. Both C_{IN} and C_{OUT} are required to have low ESR to minimize the AC I^2R loss and sufficient capacitance to prevent the RMS current from causing additional upstream losses in fuses or batteries.
5. Other Losses. Optional Schottky diodes paralleled switch B and D are responsible for conduction losses during dead time. Inductor core loss should also be considered. Switch C causes reverse recovery current loss in boost mode.

When making adjustments to improve efficiency, the input current is the best indicator of changes in efficiency. If one makes a change and the input current decreases, then the efficiency has increased. If there is no change in input current, then there is no change in efficiency.

Maximum Step-Up Ratio

Due to BG2's maximum duty cycle limit, the maximum output voltage in Boost Mode is approximately 10 times the input voltage. A resistor divider from V_{IN} is recommended to turn off the RUN pin when the input voltage drops to below 1/10 of the output voltage, which prevents large reverse currents during transients.

Parallel Operations

For output loads that demand high current, multiple LTC7878s can be paralleled and daisy chained to run out of phase to provide more output current without increasing input and output voltage ripple. The SYNC pin allows the LTC7878 to synchronize to the CLKOUT signal of another LTC7878. The CLKOUT signal can be connected to the SYNC pin of the following LTC7878 stage to line up both the frequency and the phase of the entire system. Tying the PHASMD pin to GND, floating or $INTV_{CC}$ generates a phase difference (between SW1 and CLKOUT) of 180°, 120° or 90° respectively for 2, 3 or 4 ICs parallel operations.

Similar to other peak current mode controllers, LTC7878 may be paralleled with natural cycle-by-cycle current sharing and no extra current sharing loop and stability issues. When designing multiple ICs parallel operations, always start from the single LTC7878 design and check the output current capability and load current transient stability. Then the LTC7878s can be paralleled by making these connections.

- Tie All of the V_{FB} Pins Together
- Tie All of the ITH Pins Together (Assuming ITHB Short To ITH for Initial Debug)
- Tie All of the SS Pins Together
- Tie All of the RUN Pins Together
- Tie the Inputs of All Converters Together
- Tie the Outputs of All Converters Together
- Route One IC's CLKOUT to Another IC's SYNC Pin

Refer to the Typical Applications section for an example of a 2-phase parallel operation design.

The LTC7878 may also be paralleled from different input voltages for a redundancy design. Just do not tie SS and RUN pin of the LTC7878s together and each LTC7878 can start up with different input voltages to supply current to a single output. Any one input voltage failure won't

APPLICATIONS INFORMATION

affect the output voltage regulation as long as the other input sources can supply enough load current. The peak inductor currents are still shared among all the buck-boost converters by tying all the ITH pins together. In the redundancy design, it is suggested that each LTC7878 has its own compensation network and feedback resistor locally closed to the pin and then short the V_{FB} pins and ITH pins all together with PCB traces.

DESIGN EXAMPLE

As a design example for a buck-boost converter, assume $V_{IN(NOMINAL)}$ = 8V ~ 42V, V_{OUT} = 12V, I_{OUT} = 9A, and f_{SW} = 250kHz. Maximum ambient temperature = 60°C.

1. Set the frequency at 250kHz by applying 1V on the FREQ pin (See Figure 2), 10µA current flowing out of the FREQ pin will give 1.0V across a 100k resistor to GND.

$$R_{FREQ}\ (\text{in k}\Omega) = \frac{1.0V}{10\mu A} = 100k\Omega$$

2. Determine the inductor value. The nominal input voltage is 24V and set inductor ripple current to 60% of DC current (5.4A) at the nominal input voltage. This leads to an inductor value:

$$L = \left(V_{IN} - V_{OUT}\right) \bullet \frac{DT_S}{i_L} = (24V - 12V)\ \bullet$$

$$0.5 \bullet \frac{4\mu s}{5.4A} = 4.4\mu H$$

The peak inductor current at $24V_{IN}$ is 11.7A.

To achieve high efficiency, low DCR inductors are preferred. We choose Wurth 7443630420 inductor (4.2µH/3.04mΩ) with 24A rated current. With 2 RC filters and usage of ISNSD pin, we can set the peak sensed inductor current limit to 50mV. Then the peak inductor current is 50mV/3.04mΩ = 16.45A which is less than the saturation current of the selected inductor.

Next the inductor current at minimum and maximum input voltage should be examined. At V_{IN} = 8V and V_{OUT} = 12V, the converter is working as a boost converter. The peak inductor current with 9A load current is 14.7A. At V_{IN} = 42V and V_{OUT} = 12V, the converter is working as a buck converter. The peak inductor current with 9A load is 13.1A. Both are less than the peak current limit of 16.45A.

The DCR current sensing filter network should be designed based on the Figure 8. if C1 = C2 = 47nF, then R1 = L/(4 • DCR)/C1 = 7.35kΩ, R2 = R1 • 3 • 0.9 = 19.845kΩ. In real design, choose R1 = 7.32kΩ and R2 = 20kΩ. The worst case minimum sensed ripple signal for the internal current comparator happened at boost mode with 16.67% duty cycle. In this case, the inductor ripple current peak to peak value is 1.6A and sensed voltage is $\Delta V_{SENSE} = 4 \bullet DCR \bullet \Delta I_{L(MIN)}$ = 19mV. The sensed voltage is higher than 15mV so the signal to noise ratio is high enough and the jitter is minimized.

3. Set the output voltage. Select feedback resistors R1 and R2. If R1 is 10k, R2 is:

$$R2 = \frac{V_{OUT} \bullet R1}{1.0} - R1$$

Select R2 as 110k. Both R1 and R2 should have a tolerance of no more than 1%.

4. Select MOSFET based on the maximum input and output voltages. Switches A and B connected to SW1 operates under the max 42V input voltage, so the 60V rated MOSFETs are selected. Switches C and D connected to SW2 operates under the 12V output voltage, so the 25V rated MOSFETs are selected. Similar to buck or boost converter design, the low $R_{DS(ON)}$ MOSFETs are preferred for low conduction losses. However, the switching loss may be high for low $R_{DS(ON)}$ MOSFETs due to the large gate capacitance. LTC7878 can drive both logic level and non-logic level MOSFETs for users to select the MOSFET widely. In the design example, BSC034N06NS3 (non-logic level) and BSC014NE2LSI (logic level) are used. Bootstrap diodes should be able to handle the maximum V_{IN}/V_{OUT} voltage with higher than 100mA capability. PMEG6010 Schottky diodes are selected for the TG1/TG2 drivers.

Since the normal level MOSFETs are selected, an input voltage UVLO may be set up on the RUN pin. A 100k/20k resistor divider from V_{IN} to RUN pin will turn on the converter when V_{IN} is higher than 7.2V.

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PC BOARD LAYOUT CHECK LIST

The basic PC board layout requires a dedicated ground plane layer. Also, for high current, a multilayer board provides heat sinking for power components. Please refer to the evaluation kits, demo board layout and demo manual for detailed examples.

- The ground plane layer should not have any traces and should be as close as possible to the layer with power MOSFETs.
- Place C_{IN}, switch A, switch B in one compact area. Place C_{OUT}, switch C, switch D in one compact area.
- Use immediate vias to connect the components (including the LTC7878's SGND and PGND pins) to the ground plane. Use several large vias for each power component.
- Use planes for V_{IN} and V_{OUT} to maintain good voltage filtering and to keep power losses low.
- Flood all unused areas on all layers with copper. Flooding with copper will reduce the temperature rise of power components. Connect the copper areas to any DC net (V_{IN} or GND).
- Segregate the signal and power grounds. All small signal components should return to the SGND pin, which is then tied to the PGND pin at one point.
- Place switch B and switch C as close to the controller as possible, keeping the PGND, BG and SW traces short.
- Keep the high dv/dt SW1, SW2, BOOST1, BOOST2, TG1 and TG2 nodes away from sensitive small-signal nodes.
- The path formed by switch A, switch B and the C_{IN} capacitor should have short leads and PC trace lengths. The path formed by switch C, switch D and the C_{OUT} capacitor also should have short leads and PC trace lengths.
- The output capacitor (–) terminals should be connected as closely as possible to the (–) terminals of the input capacitor.
- Connect the top driver boost capacitor C_{BST1} closely to the BOOST1 and SW1 pins. Connect the top driver boost capacitor C_{BST2} closely to the BOOST2 and SW2 pins.
- Connect the input capacitors C_{IN} and output capacitors C_{OUT} closely to the power MOSFETs. These capacitors carry the MOSFET AC current in the boost and buck region.
- Connect V_{FB} pin resistive dividers to the (+) terminals of C_{OUT} and signal ground. A small V_{FB} bypass capacitor may be connected closely to the LTC7878 SGND pin. The R2 connection should not be along the high current or noise paths, such as the input capacitors.
- Route ISNSP and ISNSN leads together with minimum PC trace spacing. ISNSP has to be electrically connected to SW1 without any resistance. The filter capacitor between ISNSP and ISNSN should be as close as possible to the IC. Ensure accurate current sensing with Kelvin connections at the inductor. If ISNSD is used, the filter capacitor on the ISNSD should also be placed close to the IC.
- Connect the ITH/ITHB pin compensation network closely to the IC, between ITH and the signal ground pins. The capacitor helps to filter the effects of PCB noise and output voltage ripple voltage from the compensation loop.
- Connect the DRV_{CC} bypass capacitor, closely to the IC, between the DRV_{CC} and the PGND pin. This capacitor carries the MOSFET drivers' current peaks. An additional 1µF ceramic capacitor placed immediately next to the DRV_{CC} and PGND pins can help improve noise performance substantially.

TYPICAL APPLICATIONS

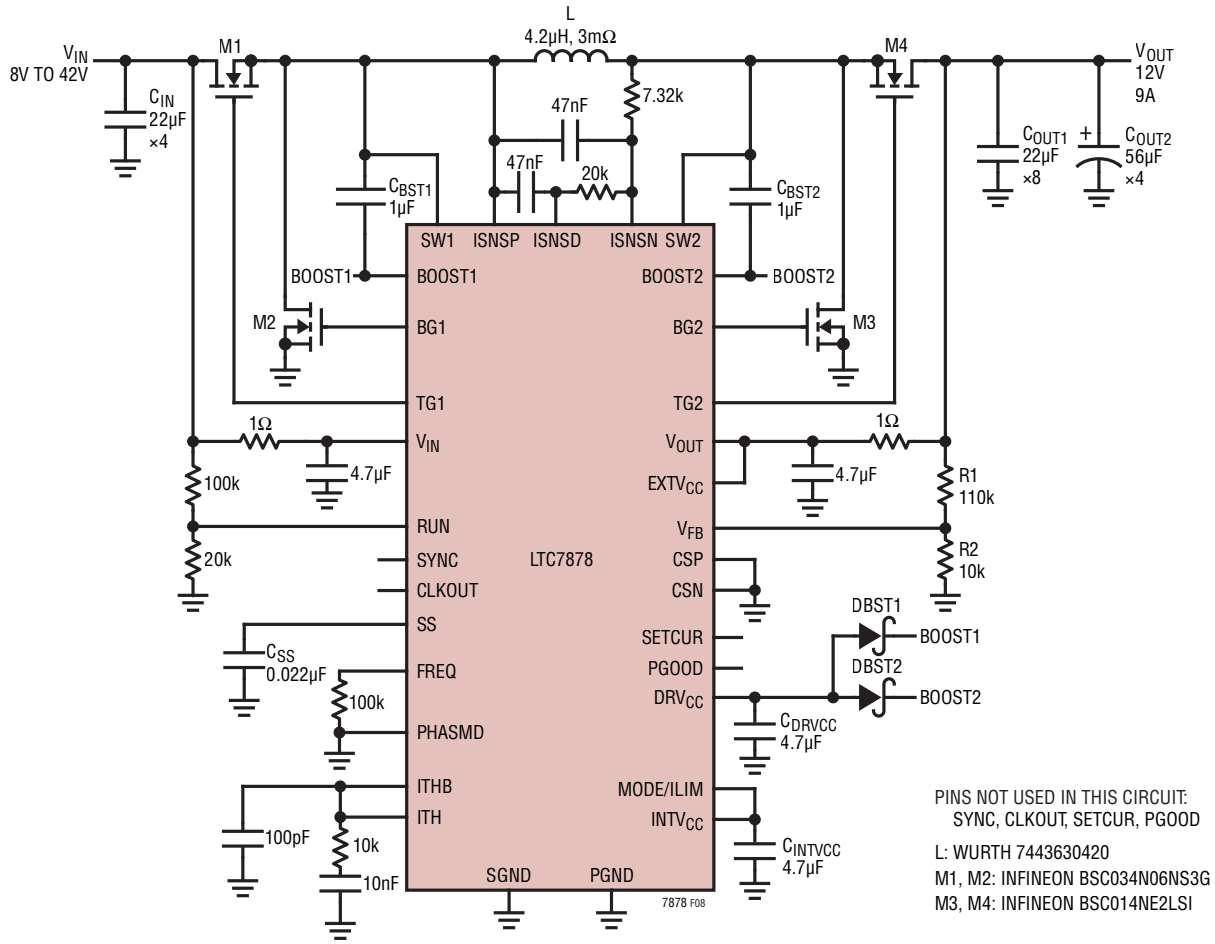


Figure 8. High Efficiency 8V to 42V Input, $12V_{OUT}$/9A Output Buck-Boost Converter

TYPICAL APPLICATIONS

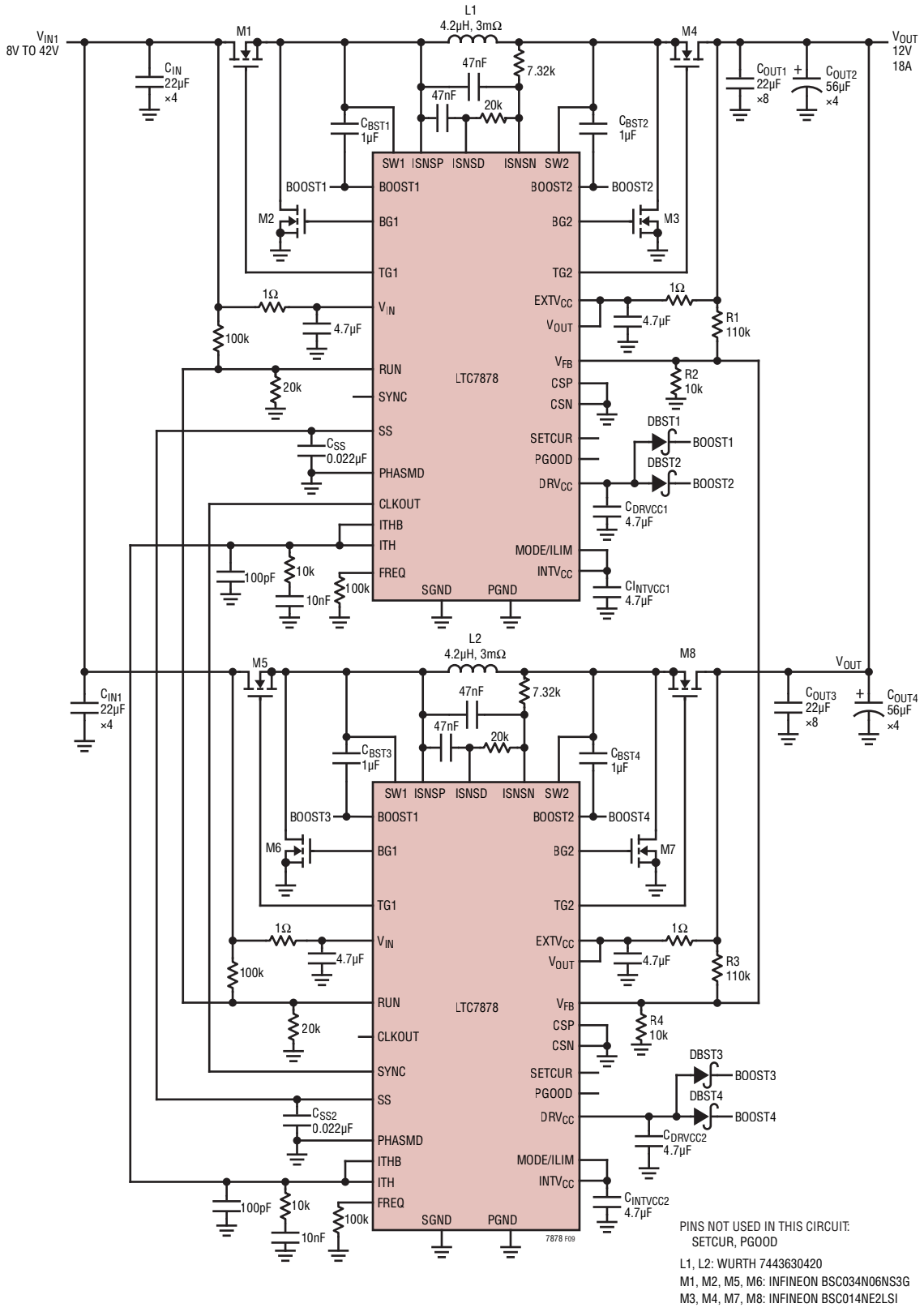


Figure 9. Two-Phase Parallel Operation 12V_{OUT}/18A Buck-Boost Converter

TYPICAL APPLICATIONS

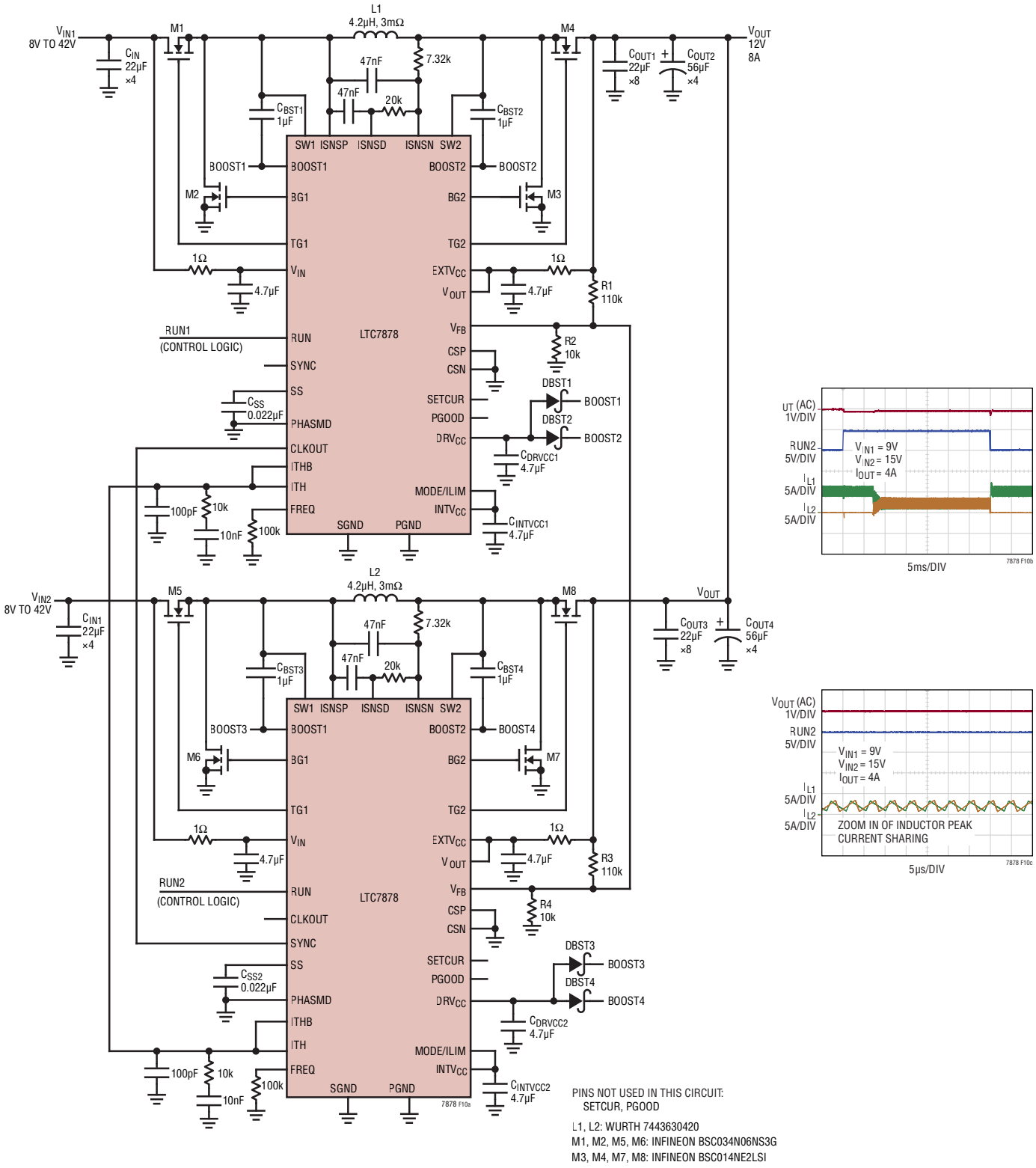
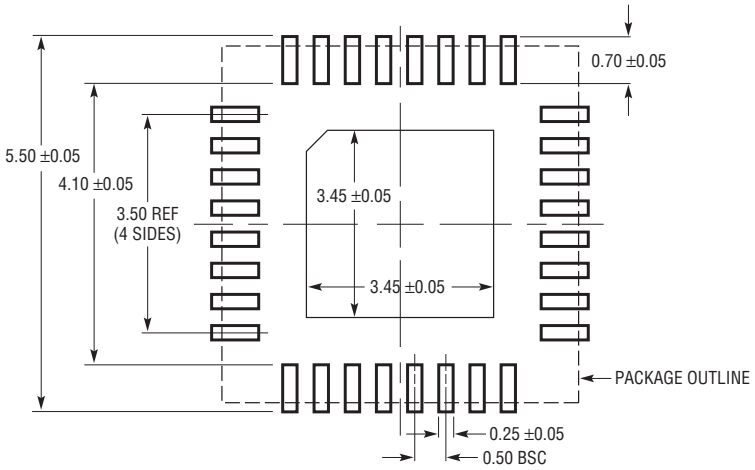


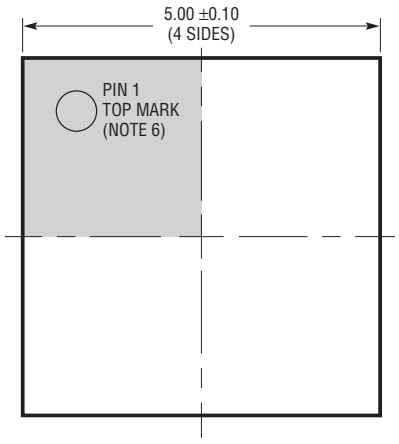
Figure 10. 12V_{OUT}/8A Two-Phase Parallel Buck-Boost Converter with Different Inputs for Redundancy Design

PACKAGE DESCRIPTION

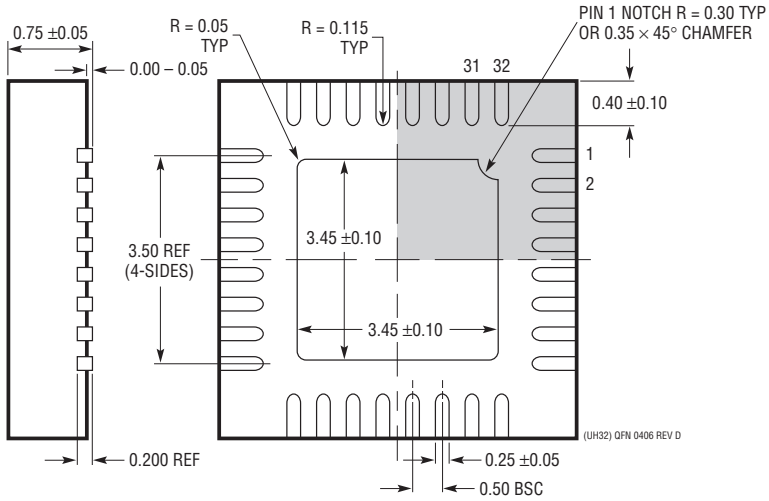
UH Package
32-Lead Plastic QFN (5mm × 5mm)
(Reference LTC DWG # 05-08-1693 Rev D)



RECOMMENDED SOLDER PAD LAYOUT
APPLY SOLDER MASK TO AREAS THAT ARE NOT SOLDERED



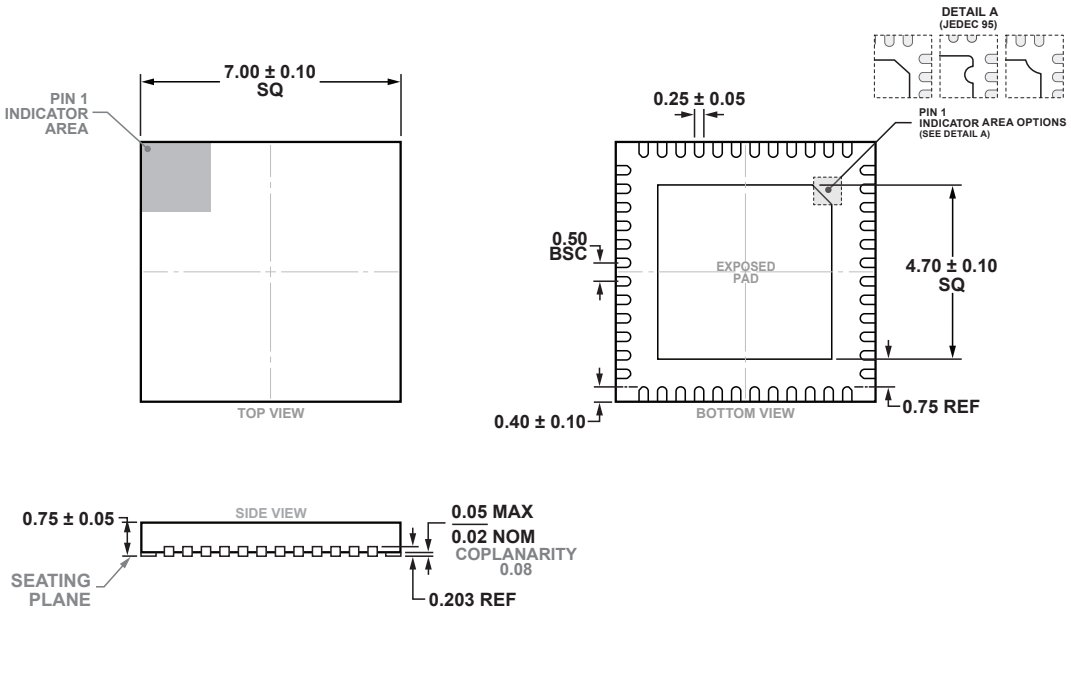
BOTTOM VIEW—EXPOSED PAD



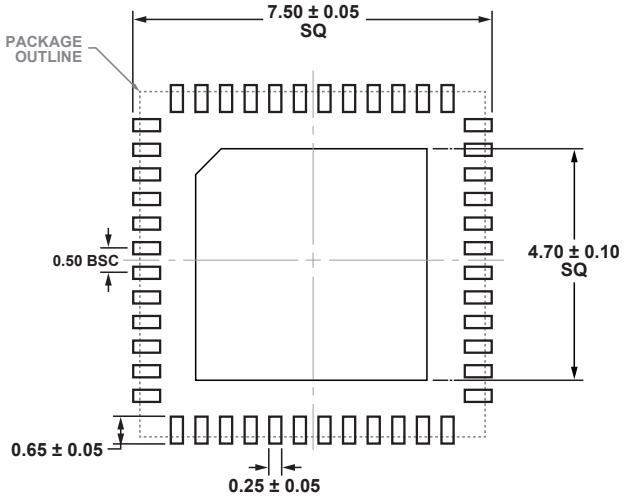
NOTE:
1. DRAWING PROPOSED TO BE A JEDEC PACKAGE OUTLINE
   M0-220 VARIATION WHHD-(X) (TO BE APPROVED)
2. DRAWING NOT TO SCALE
3. ALL DIMENSIONS ARE IN MILLIMETERS
4. DIMENSIONS OF EXPOSED PAD ON BOTTOM OF PACKAGE DO NOT INCLUDE
   MOLD FLASH. MOLD FLASH, IF PRESENT, SHALL NOT EXCEED 0.20mm ON ANY SIDE
5. EXPOSED PAD SHALL BE SOLDER PLATED
6. SHADED AREA IS ONLY A REFERENCE FOR PIN 1 LOCATION
   ON THE TOP AND BOTTOM OF PACKAGE

PACKAGE DESCRIPTION

48-Lead Lead Frame Chip Scale Package [LFCSP]
7 x 7 mm Body and 0.75 mm Package Height
(CP-48-30)
Dimensions shown in millimeters



RECOMMENDED SOLDER PAD LAYOUT
(TOP VIEW)



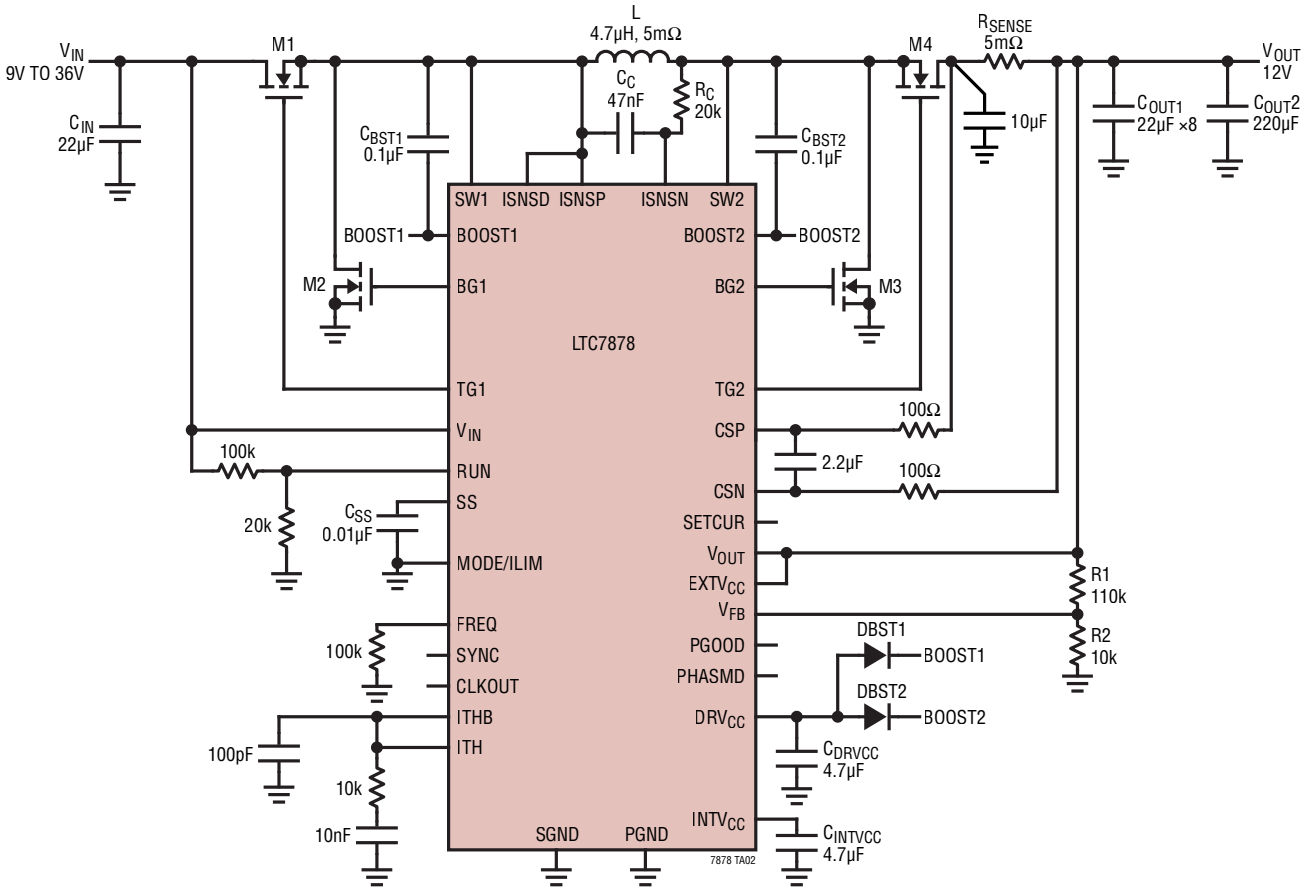
REVISION HISTORY

REV	DATE	DESCRIPTION	PAGE NUMBER
0	12/22	Initial Release	All
A	04/20	Updated Typical Application.	1
		Updated Block Diagram.	10
		Updated Inductor Selection and DCR Current Sensing Section.	15
		Updated Top MOSFET Driver Supply.	19
B	01/25	Updated Features, Applications, and Description for UK package.	1
		Updated Pin Configuration, Ordering Information for UK package.	2
		Updated Pin Functions for UK package.	8, 9
		Updated Package Description for UK package.	27, 28
C	10/25	Updated Thermal Resistance of UH Package.	2
		Updated Block Diagram.	10
		Updated Figure 4 and Figure 5.	16
		Added Maximum Step-Up Ratio section.	21
D	10/26	Corrected typographical errors in Typical Performance Characteristics graph references from Figure 5 to Figure 8.	5

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TYPICAL APPLICATION

9V to 36V Input, 12V Output Buck-Boost Converter with 10A Output Current Limit



RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LTC3789	38V V_{IN} and V_{OUT} High Efficiency, Synchronous, 4-Switch Buck-Boost Controller	4V ≤ V_{IN} ≤ 38V, 0.8V ≤ V_{OUT} ≤ 38V, Up to 99%, Current Mode Control
LTC3779	150V V_{IN} and V_{OUT} Synchronous 4-Switch Buck-Boost Controller	4.5V ≤ V_{IN} ≤ 150V, 1.2V ≤ V_{OUT} ≤ 150V, Up to 99% Efficiency Drives Logic Level or STD Threshold MOSFETs, TSSOP-38
LTC3777	150V V_{IN} and Vout Synchronous 4-Switch Buck-Boost Controller plus Switching Bias Supply	4.5V ≤ V_{IN} ≤ 150V, 1.2V ≤ V_{OUT} ≤ 150V, Up to 99% Efficiency Drives Logic Level or STD Threshold MOSFETs, TSSOP-38
LT®8705A	80V Synchronous 4-Switch Buck-Boost DC/DC Controller	2.8V ≤ V_{IN} ≤ 80V, Input and Output Current Monitor, 5mm × 7mm QFN-38 and TSSOP-38
LT8708	80V Bidirectional Synchronous 4-Switch Buck-Boost DC/DC Controller	2.8V (Need $EXTV_{CC}$ > 6.4V) ≤ V_{IN} ≤ 80V, 1.3V ≤ V_{OUT} ≤ 80V, 5mm × 8mm QFN-40.
LTM®8056	58V Buck-Boost µModule Regulator, Adjustable Input and Output Current Limiting	5V ≤ V_{IN} ≤ 58V, 1.2V ≤ V_{OUT} ≤ 48V, 15mm × 15mm × 4.92mm BGA Package
LT8392	60V Synchronous 4-Switch Buck-Boost Controller with Spread Spectrum	3V ≤ V_{IN} ≤ 60V, 1.2V ≤ V_{OUT} ≤ 60V, I_Q = 2uA, 4mm × 5mm QFN-28 and TSSOP-28
LTC7813	60V Low I_Q Synchronous Boost plus Buck Controller, Low EMI and Low Input/Output Ripple	4.5V (Down to 2.2V after Start-Up) ≤ V_{IN} ≤ 60V, Boost V_{OUT} Up to 60V, 0.8V ≤ Buck V_{OUT} ≤ 60V, I_Q = 29µA, 5mm × 5mm QFN-32

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