25A, Dual PolyPhase Regulator with Digital Power System Management

FEATURES

- **PMBus/I²C Compliant Serial Interface**
  - **Telemetry Read-Back Includes V_{IN}, I_{IN}, V_{OUT}, I_{OUT}, Temperature and Faults**
  - **Programmable Voltage, Current Limit, Digital Soft-Start/Stop, Sequencing, Margining, OV/UV/OC**
- **Sub-Milliohm DCR Current Sensing**
- **Digitally Adjustable Loop Compensation Parameters**
- **±0.5% Output Voltage Accuracy Over Temperature**
- **Integrated Input Current Sense Amplifier**
- **Internal EEPROM with ECC and Fault Logging**
- **Integrated N-Channel MOSFET Gate Drivers**

Power Conversion

- Wide V_{IN} Range: 4.5V to 20V
- V_{OUT} Range: 0.5V to 3.5V (with Ultralow DCR Setting); 0.5V to 5.5V (Typical DCR Setting)
- Accurate PolyPhase® Current Sharing for Up to 6 Phases
- Available in a 140-Lead (9mm × 11.25mm × 2.22mm) BGA Package

APPLICATIONS

- Telecom, Datacom and Storage Systems
- Industrial and Point-of-Load Applications

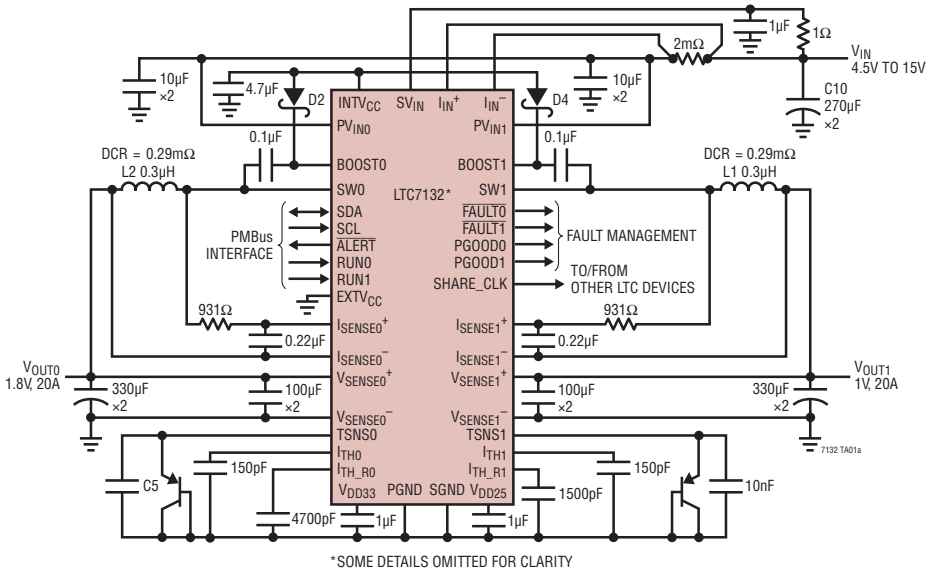
DESCRIPTION

The LTC®7132 is a dual output PolyPhase DC/DC synchronous step-down monolithic regulator with an I²C-based PMBus compliant serial interface. The regulator employs a constant-frequency current mode architecture, together with a unique scheme to provide excellent performance in sub-milliohm DCR applications. The LTC7132 is supported by the LTpowerPlay® software development tool with graphical user interface (GUI).

Programmable loop compensation allows the regulator to be compensated digitally. The switching frequency, channel phasing and device address can be programmed both by the digital interface as well as the external configuration resistors. Additionally, parameters can be set via the digital interface and stored in EEPROM. Both outputs have independent power good indicators and $\overline{\text{FAULT}}$ function.

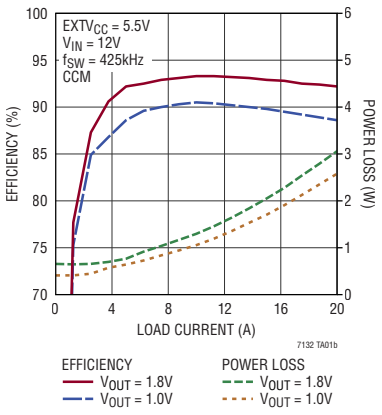
The LTC7132 can be configured to operate in discontinuous (pulse-skipping) mode or forced continuous conduction mode. Each channel can deliver up to 25A of load current; the total current capability will depend on the total power dissipations on both channels.

TYPICAL APPLICATION



*SOME DETAILS OMITTED FOR CLARITY

Efficiency and Power Loss vs Load Current



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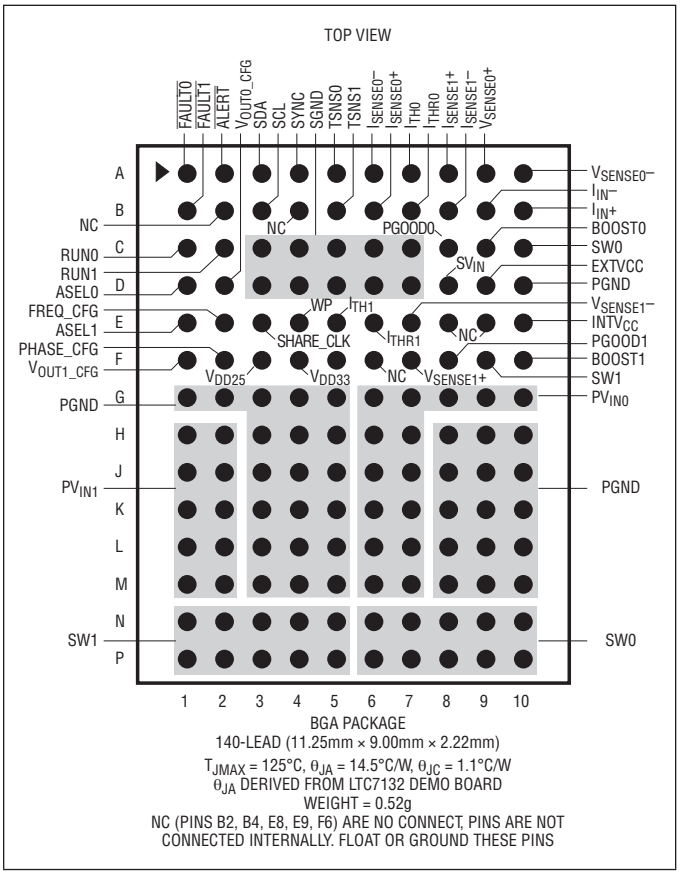
ABSOLUTE MAXIMUM RATINGS

(Note 1)

SV_{IN}, PV_{IN0}, PV_{IN1}, I_{IN}^+, I_{IN}^- ..... –0.3V to 20V
(V_{IN}–I_{IN}^+), (I_{IN}^+–I_{IN}^-) ..... –0.3V to 0.3V
BOOST0, BOOST1 ..... –0.3V to 26V
Switch Transient Voltage (SW0, SW1) ..... –5V to 26V
I_{SENSE0}^+, I_{SENSE0}^-, I_{SENSE1}^+, I_{SENSE1}^-,
V_{SENSE0}^+, V_{SENSE1}^+ ..... –0.3V to 6V
V_{SENSE0}^-, V_{SENSE1}^- ..... –0.3V to 0.3V
(BOOST0-SW0), (BOOST1-SW1) ..... –0.3V to 6V
$EXTV_{CC}$, $INTV_{CC}$ ..... –0.3V to 6V
PGOOD0, PGOOD1 ..... –0.3V to 3.6V
RUN0, RUN1, SDA, SCL, $\overline{ALERT}$ ..... –0.3V to 5.5V
ASEL0, ASEL1, V_{OUT0_CFG0}, V_{OUT1_CFG}, FREQ_CFG,
PHASE_CFG ..... –0.3V to 2.75V
$\overline{FAULT0}$, $\overline{FAULT1}$, SHARE_CLK, WP, SYNC –0.3V to 3.6V
TSNS0, TSNS1 ..... –0.3V to 2.2V
I_{TH0}, I_{TH1}, I_{THR0}, I_{THR1} ..... –0.3V to 2.7V
Operating Junction Temperature Range
(Notes 2, 17, 18) ..... –40°C to 125°C
Storage Temperature Range ..... –55°C to 125°C

*See Derating EEPROM Retention at Temperature in Applications Information section for junction temperatures in excess of 125°C.

PIN CONFIGURATION



BGA PACKAGE
140-LEAD (11.25mm × 9.00mm × 2.22mm)
T_{JMAX} = 125°C, θ_{JA} = 14.5°C/W, θ_{JC} = 1.1°C/W
θ_{JA} DERIVED FROM LTC7132 DEMO BOARD
WEIGHT = 0.52g
NC (PINS B2, B4, E8, E9, F6) ARE NO CONNECT, PINS ARE NOT CONNECTED INTERNALLY. FLOAT OR GROUND THESE PINS

ORDER INFORMATION

PART NUMBER	PAD OR BALL FINISH	PART MARKING*		PACKAGE TYPE	MSL RATING	TEMPERATURE RANGE (SEE NOTE 2)
		DEVICE	FINISH CODE			
LTC7132EY#PBF	SAC305 (RoHS)	LTC7132Y	e1	BGA	4	–40°C to 125°C
LTC7132IY#PBF						

- Contact the factory for parts specified with wider operating temperature ranges. *Pad or ball finish code is per IPC/JEDEC J-STD-609.
- Recommended LGA and BGA PCB Assembly and Manufacturing Procedures
- LGA and BGA Package and Tray Drawings

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the specified operating junction temperature range, otherwise specifications are at T_A = 25°C (Note 2). V_{IN} = 12V, $EXTV_{CC}$ = 0V, $V_{RUN0,1}$ = 3.3V, f_{SYNC} = 500kHz (externally driven) and all programmable parameters at factory default, unless otherwise specified.

SYMBOL	PARAMETER	CONDITION		MIN	TYP	MAX	UNITS
Input Voltage							
SV_{IN}, $PV_{IN0/1}$	Input Voltage Range	(Note 11)	●	4.5		20	V
I_Q	Input Voltage Supply Current	$V_{RUN0,1}$ = 3.3V (Note 16) $V_{RUN0,1}$ = 0V (Note 16)			25 23		mA mA
V_{UVLO}	Undervoltage Lockout Threshold When V_{IN} > 4.3V	V_{INTVCC} Falling V_{INTVCC} Rising			3.55 3.90		V V
t_{INIT}	Initialization Time	Time from V_{IN} Applied Until the TON_DELAY Timer Starts			35		ms
$t_{OFF(MIN)}$	Short Cycle Retry Time				120		ms
Control Loop							
V_{OUTRL}	Range 1 Maximum V_{OUT} Set Point Accuracy (0.6V ~ 2.5V) Resolution LSB Step Size	0.6V ≤ V_{OUT} ≤ 2.5V MFR_PWM_MODE[1] = 1 (Notes 9, 10, 13)	 ● 	 –0.5 	2.75 12 0.688	 0.5 	V % Bits mV
V_{OUTRH}	Range 0 Maximum V_{OUT} Set Point Accuracy (0.6V ~ 5.0V) Resolution LSB Step Size	1.2V ≤ V_{OUT} ≤ 5.5V MFR_PWM_MODE[1] = 0 (Notes 9, 10, 13)	● ● 	 –0.5 	5.5 12 1.375	 0.5 	V % Bits mV
$V_{LINEREG}$	Line Regulation	6V < V_{IN} < 20V	●			±0.02	%/V
$V_{LOADREG}$	Load Regulation	ΔV_{ITH} = 1.35V ~ 0.7V ΔV_{ITH} = 1.35V ~ 2V	● ●		0.01 –0.01	0.1 –0.1	% %
$I_{ISENSE0,1}$	Input Pin Bias Current	0V ≤ V_{PIN} ≤ 5.5V	●		±1	±3	µA
$V_{SENSERIN0,1}$	V_{SENSE} Input Resistance to GND	0V ≤ V_{PIN} ≤ 5.5V			50		kΩ
V_{ILIMIT}	V_{ILIM_HIGH} V_{ILIM_LOW} V_{REV}	MFR_PWM_MODE[7],[2]=0, 1, I_{LIM}[3:0]=1100, V_{OUT} ≤ 3.5V (Note 15) MFR_PWM_MODE[7],[2]=0, 1, I_{LIM}[3:0]=0001, V_{OUT} ≤ 3.5V MFR_PWM_MODE[7],[2]=0, 1, V_{OUT} ≥ V_{OV}	●	14.5	16.5 9.5 –7.5	18.5	mV mV mV
	V_{ILIM_HIGH} V_{ILIM_LOW} V_{REV}	MFR_PWM_MODE[7][2]=1, 1, I_{LIM}[3:0]=1100,V_{OUT} ≤ 3.5V MFR_PWM_MODE[7][2]=1, 1, I_{LIM}[3:0]=0001,V_{OUT} ≤ 3.5V MFR_PWM_MODE[7][2]=1, 1, V_{OUT} ≥ V_{OV}	●	27.0	29.5 17.0 –15	31.0	mV mV mV
	V_{ILIM_HIGH} V_{ILIM_LOW} V_{REV}	MFR_PWM_MODE[7][2]=0, 0, I_{LIM}[3:0]=1100 MFR_PWM_MODE[7][2]=0, 0, I_{LIM}[3:0]=0001 MFR_PWM_MODE[7][2]=0, 0, V_{OUT} ≥ V_{OV}	●	35	41.38 25 –18.8	49	mV mV mV
	V_{ILIM_HIGH} V_{ILIM_LOW} V_{REV}	MFR_PWM_MODE[7][2]=1, 0, I_{LIM}[3:0]=1100 MFR_PWM_MODE[7][2]=1, 0, I_{LIM}[3:0]=0001 MFR_PWM_MODE[7][2]=1, 0, V_{OUT} ≥ V_{OV}	●	67.5	74.5 43.5 –37.5	81.5	mV mV mV
$g_{m0,1}$	Resolution Error Amplifier $g_{m(MAX)}$ Error Amplifier $g_{m(MIN)}$ LSB Step Size	$I_{TH0,1}$ = 1.35V, MFR_PWM_CONFIG[7:5] = 0 to 7			3 4.6 0.8 0.54		Bits mmho mmho mmho
$R_{TH0,1}$	Resolution Compensation Resistor $R_{TH(MAX)}$ Compensation Resistor $R_{TH(MIN)}$	MFR_PWM_CONFIG[4:0] = 0 to 31 (See Figure 1)			5 62 0		Bits kΩ kΩ
$t_{ON(MIN)}$	Minimum On-Time				90		ns
$R_{DS(ON)}$							
R_{TOP}	Top Power NMOS On-Resistance				7.3		mΩ
R_{BOTTOM}	Bottom Power NMOS On-Resistance				2.1		mΩ

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the specified operating junction temperature range, otherwise specifications are at T_A = 25°C (Note 2). V_{IN} = 12V, $EXTV_{CC}$ = 0V, $V_{RUN0,1}$ = 3.3V, f_{SYNC} = 500kHz (externally driven) and all programmable parameters at factory default, unless otherwise specified.

SYMBOL	PARAMETER	CONDITION		MIN	TYP	MAX	UNITS
OV/UV Output Voltage Supervisor Channel 0/1							
N	Resolution				9		Bits
$V_{OUSTPSP\_RL}$	LSB Step Size	MFR_PWM_MODE[1] = 1 (Note 13)			5.6		mV
$V_{OUSTPSP\_RH}$	LSB Step Size	MFR_PWM_MODE[1] = 0 (Note 13)			11.2		mV
V_{RANGE_RL}	Range 0 Maximum Threshold	MFR_PWM_MODE[1] = 1			2.86		V
V_{RANGE_RH}	Range 1 Maximum Threshold	MFR_PWM_MODE[1] = 0			5.74		V
V_{THAC0_RL}	Threshold Accuracy 1V < V_{OUT} < 2.75V	MFR_PWM_MODE[1] = 1	●			±1.5	%
V_{THAC1_RH}	Threshold Accuracy 2V < V_{OUT} < 5.5V	MFR_PWM_MODE[1] = 0	●			±1.5	%
t_{PROPOV}	OV Comparator Response Time	V_{OD} = 10% of Threshold				100	µs
t_{PROPUV}	UV Comparator Response Time	V_{OD} = 10% of Threshold				100	µs
V_{IN} Voltage Supervisor							
N	Resolution				9		Bits
V_{INSTP}	LSB Step Size				76		mV
V_{IN}	Full-Scale Voltage				20		V
$V_{INTHACCM}$	Threshold Accuracy 9V < V_{IN} < 20V Threshold Accuracy 4.5V < V_{IN} ≤ 9V		● ●			±3 ±6.0	% %
$t_{PROPVIN}$	Comparator Response Time (VIN_ON and VIN_OFF)	V_{OD} = 10% of threshold				100	µs
Output Voltage Readback							
N	Resolution				16		Bits
V_{OUTSTP}	LSB Step Size				244		µV
$V_{F/S}$	Full-Scale Sense Voltage	V_{RUNn} = 0 (Note 8)			8		V
V_{OUT_TUE}	Total Unadjusted Error	V_{OUT} > 0.6V (Note 8)	●	–0.5		0.5	%
V_{OS}	Zero-Code Offset Voltage		●			±500	µV
$t_{CONVERT}$	Update Rate	(Note 6)			90		ms
V_{IN} Voltage Readback							
N	Resolution	(Note 5)			10		Bits
$V_{F/S}$	Full-Scale Input Voltage	(Note 11)			20		V
V_{INTUE}	Total Unadjusted Error	V_{VIN} > 4.5V (Note 8)	 ●			0.5 2	% %
$t_{CONVERT}$	Update Rate	(Note 6)			90		ms
Output Current Readback							
N	Resolution	(Note 5)			10		Bits
$V_{IOUTSTP}$	LSB Step Size	0V ≤ $\lvert V_{ISENSE}^+ - V_{ISENSE}^- \rvert$ < 16mV 16mV ≤ $\lvert V_{ISENSE}^+ - V_{ISENSE}^- \rvert$ < 32mV 32mV ≤ $\lvert V_{ISENSE}^+ - V_{ISENSE}^- \rvert$ < 64mV 64mV ≤ $\lvert V_{ISENSE}^+ - V_{ISENSE}^- \rvert$ < 100mV			15.63 31.25 62.5 125		µV µV µV µV
$I_{F/S}$	Full-Scale Input Current	(Note 7) DCR or R_{ISENSE} = 1mΩ			±100		A
I_{OUT_TUE}	Total Unadjusted Error	100mV > ($V_{ISENSE}^+ - V_{ISENSE}^-$) > 6mV (Note 8)	●			±1.25	%
V_{OS}	Zero-Code Offset Voltage					±50	µV
$t_{CONVERT}$	Update Rate	(Note 6)			90		ms

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the specified operating junction temperature range, otherwise specifications are at T_A = 25°C (Note 2). V_{IN} = 12V, $EXTV_{CC}$ = 0V, $V_{RUN0,1}$ = 3.3V, f_{SYNC} = 500kHz (externally driven) and all programmable parameters at factory default, unless otherwise specified.

SYMBOL	PARAMETER	CONDITION		MIN	TYP	MAX	UNITS
Input Current Readback							
N	Resolution	(Note 5)			10		Bits
V_{IINSTP}	LSB Step Size Full-Scale Range = 16mV LSB Step Size Full-Scale Range = 32mV LSB Step Size Full-Scale Range = 64mV	Gain = 8, 0V ≤ $\lvert V_{IIN}^+ - V_{IIN}^-\rvert$ ≤ 5mV Gain = 4, 0V ≤ $\lvert V_{IIN}^+ - V_{IIN}^-\rvert$ ≤ 20mV Gain = 2, 0V ≤ $\lvert V_{IIN}^+ - V_{IIN}^-\rvert$ ≤ 50mV			15.26 30.52 61		µV µV µV
I_{IN_TUE}	Total Unadjusted Error	Gain = 8, 2.5mV ≤ $\lvert V_{IIN}^+ - V_{IIN}^-\rvert$ ≤ 5mV (Note 8) Gain = 4, 4mV ≤ $\lvert V_{IIN}^+ - V_{IIN}^-\rvert$ ≤ 20mV (Note 8) Gain = 2, 6mV ≤ $\lvert V_{IIN}^+ - V_{IIN}^-\rvert$ ≤ 50mV (Note 8)				±2 ±1.3 ±1.2	% % %
V_{OS}	Zero-Code Offset Voltage					±50	µV
$t_{CONVERT}$	Update Rate	(Note 6)			90		ms
Supply Current Readback							
N	Resolution	(Note 5)			10		Bits
$V_{ICHIPSTP}$	LSB Step Size Full-Scale Range = 256mV				244		µV
$I_{CHIPTUE}$	Total Unadjusted Error	20mV ≤ $\lvert V_{IIN}^+ - V_{IN}\rvert$ ≤ 150mV (Note 19)	●			±3	%
$t_{CONVERT}$	Update Rate	(Note 6)			90		ms
Temperature Readback (T0, T1)							
T_{RES_T}	Resolution				0.25		°C
T0_TUE	External Temperature Total Unadjusted Readback Error	TSNS0, TSNS1 ≤ 1.85V (Note 8) MFR_PWM_MODE_[5] = 0 MFR_PWM_MODE_[5] = 1 (Note 14)	 ● ●	 –3 –10		 3 10	 °C °C
T1_TUE	Internal TSNS TUE	$V_{RUN0,1}$ = 0.0, f_{SYNC} = 0kHz (Note 8)			±1		°C
$t_{CONVERT}$	Update Rate	(Note 6)			100		ms
$INTV_{CC}$ Regulator/$EXTV_{CC}$							
V_{INTVCC}	Internal V_{CC} Voltage No Load	6V ≤ V_{IN} ≤ 20V	●	5.25	5.5	5.75	V
V_{LDO_INT}	$INTV_{CC}$ Load Regulation	I_{CC} = 0mA to 20mA, 6V ≤ V_{IN} ≤ 20V			0.5	±2	%
V_{EXTVCC}	$EXTV_{CC}$ Switchover Voltage	V_{IN} ≥ 7V, $EXTV_{CC}$ Rising	●	4.5	4.7	4.9	V
V_{LDO_HYS}	$EXTV_{CC}$ Hysteresis				290		mV
V_{LDO_EXT}	$EXTV_{CC}$ Voltage Drop	I_{CC} = 20mA, V_{EXTVCC} = 5.5V			50	100	mV
V_{IN_THR}	V_{IN} Threshold to Enable $EXTV_{CC}$ Switchover	V_{IN} Rising				7.4	V
V_{IN_HYS}	V_{IN} Hysteresis to Disable $EXTV_{CC}$ Switchover	V_{IN} Rising – V_{IN} Falling			600		mV
V_{DD33} Regulator							
V_{DD33}	Internal V_{DD33} Voltage	4.5V < V_{INTVCC} or 4.8V < V_{EXTVCC}		3.2	3.3	3.4	V
I_{LIM}	V_{DD33} Current Limit	V_{DD33} = GND, V_{IN} = $INTV_{CC}$ = 4.5V			100		mA
V_{DD33_OV}	V_{DD33} Overvoltage Threshold				3.5		V
V_{DD33_UV}	V_{DD33} Undervoltage Threshold				3.1		V
V_{DD25} Regulator							
V_{DD25}	Internal V_{DD25} Voltage				2.5		V
I_{LIM}	V_{DD25} Current Limit	V_{DD25} = GND, V_{IN} = $INTV_{CC}$ = 4.5V			80		mA

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the specified operating junction temperature range, otherwise specifications are at T_A = 25°C (Note 2). V_{IN} = 12V, $EXTV_{CC}$ = 0V, $V_{RUN0,1}$ = 3.3V, f_{SYNC} = 500kHz (externally driven) and all programmable parameters at factory default, unless otherwise specified.

SYMBOL	PARAMETER	CONDITION		MIN	TYP	MAX	UNITS
Oscillator and Phase-Locked Loop							
f_{RANGE}	PLL SYNC Range	Syncronized with Falling Edge of SYNC	●	200		1000	kHz
f_{OSC}	Oscillator Frequency Accuracy	Frequency Switch = 250kHz to 1000kHz	●			±7.5	%
$V_{TH(SYNC)}$	SYNC Input Threshold	V_{SYNC} Falling V_{SYNC} Rising			1 1.5		V V
$V_{OL(SYNC)}$	SYNC Low Output Voltage	I_{LOAD} = 3mA			0.2	0.4	V
$I_{LEAK(SYNC)}$	SYNC Leakage Current in Slave Mode	0V ≤ V_{PIN} ≤ 3.6V				±5	µA
θSYNC-θ0	SYNC to Ch0 Phase Relationship Based on the Falling Edge of Sync and Rising Edge of TG0	MFR_PWM_CONFIG[2:0] = 0,2,3 MFR_PWM_CONFIG[2:0] = 5 MFR_PWM_CONFIG[2:0] = 1 MFR_PWM_CONFIG[2:0]= 4,6			0 60 90 120		Deg Deg Deg Deg
θSYNC-θ1	SYNC to Ch1 Phase Relationship Based on the Falling Edge of Sync and Rising Edge of TG1	MFR_PWM_CONFIG[2:0] = 3 MFR_PWM_CONFIG[2:0] = 0 MFR_PWM_CONFIG[2:0] = 2,4,5 MFR_PWM_CONFIG[2:0] = 1 MFR_PWM_CONFIG[2:0] = 6			120 180 240 270 300		Deg Deg Deg Deg Deg
EEPROM Characteristics							
Endurance	(Note 12)	0°C < T_J < 85°C EEPROM Write Operations	●	10,000			Cycles
Retention	(Note 12)	T_J < 125°C	●	10			Years
Mass_Write	Mass Write Operation Time	STORE_USER_ALL, 0°C < T_J < 85°C During EEPROM Write Operation	●		440	4100	ms
Leakage Current SDA, SCL, $\overline{\text{ALERT}}$, RUN							
I_{OL}	Input Leakage Current	0V ≤ V_{PIN} ≤ 5.5V	●			±5	µA
Leakage Current $\overline{\text{FAULT}}$*n*, PGOOD*n*							
I_{GL}	Input Leakage Current	0V ≤ V_{PIN} ≤ 3.6V	●			±2	µA
Digital Inputs SCL, SDA, RUN*n*, $\overline{\text{FAULT}}$*n*							
V_{IH}	Input High Threshold Voltage		●			1.35	V
V_{IL}	Input Low Threshold Voltage		●	0.8			V
V_{HYST}	Input Hysteresis	SCL, SDA			0.08		V
C_{PIN}	Input Capacitance					10	pF
Digital Input WP							
I_{PUWP}	Input Pull-Up Current	WP			10		µA
Open-Drain Outputs SCL, SDA, $\overline{\text{FAULT}}$*n*, $\overline{\text{ALERT}}$, RUN*n*, SHARE_CLK, PGOOD*n*							
V_{OL}	Output Low Voltage	I_{SINK} = 3mA				0.4	V
Digital Inputs SHARE_CLK, WP							
V_{IH}	Input High Threshold Voltage		●		1.5	1.8	V
V_{IL}	Input Low Threshold Voltage		●	0.6	1		V
Digital Filtering of $\overline{\text{FAULT}}$*n*							
I_{FLTG}	Input Digital Filtering $\overline{\text{FAULT}}$*n*				3		µs

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the specified operating junction temperature range, otherwise specifications are at T_A = 25°C (Note 2). V_{IN} = 12V, $EXTV_{CC}$ = 0V, $V_{RUN0,1}$ = 3.3V, f_{SYNC} = 500kHz (externally driven) and all programmable parameters at factory default, unless otherwise specified.

SYMBOL	PARAMETER	CONDITION		MIN	TYP	MAX	UNITS
Digital Filtering of PGOOD*n*							
I_{FLTG}	Output Digital Filtering PGOOD*n*				60		µs
Digital Filtering of RUN*n*							
I_{FLTG}	Input Digital Filtering RUN				10		µs
PMBus Interface Timing Characteristics							
f_{SCL}	Serial Bus Operating Frequency		●	10		400	kHz
t_{BUF}	Bus Free Time Between Stop and Start		●	1.3			µs
$t_{HD(STA)}$	Hold Time After Repeated Start Condition After This Period, the First Clock is Generated		●	0.6			µs
$t_{SU(STA)}$	Repeated Start Condition Setup Time		●	0.6		10000	µs
$t_{SU(ST0)}$	Stop Condition Setup Time		●	0.6			µs
$t_{HD(DAT)}$	Data Hold Time Receiving Data Transmitting Data		 ● ●	 0 0.3		 0.9	 µs µs
$t_{SU(DAT)}$	Data Setup Time Receiving Data		 	 0.1		 	 µs
$t_{TIMEOUT\_SMB}$	Stuck PMBus Timer Non-Block Reads Stuck PMBus Timer Block Reads	Measured from the Last PMBus Start Event			32 255		ms
t_{LOW}	Serial Clock Low Period		●	1.3		10000	µs
t_{HIGH}	Serial Clock High Period		●	0.6			µs

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: The LTC7132 is tested under pulsed load conditions such that $T_J \approx T_A$. The LTC7132E is guaranteed to meet performance specifications from 0°C to 85°C. Specifications over the –40°C to 125°C operating junction temperature range are assured by design, characterization and correlation with statistical process controls. The LTC7132I is guaranteed over the full –40°C to 125°C operating junction temperature range. T_J is calculated from the ambient temperature T_A and power dissipation P_D according to the following formula:

$$T_J = T_A + (P_D \bullet \theta_{JA})$$

The maximum ambient temperature consistent with these specifications is determined by specific operating conditions in conjunction with board layout, the rated package thermal impedance and other environmental factors.

Note 3: All currents into device pins are positive; all currents out of device pins are negative. All voltages are referenced to ground unless otherwise specified

Note 4: Rise and fall times are measured using 10% and 90% levels. Delay times are measured using 50% levels. C_{LOAD} = 3500pF is guaranteed by design.

Note 5: The data format in PMBus is 5 bits exponent (signed) and 11 bits mantissa (signed). This limits the output resolution to 10 bits though the internal ADC is 16 bits and the calculations use 32-bit words.

Note 6: The data conversion is done by default in round robin fashion. All inputs signals are continuously converted for a typical latency of 90ms. Setting MFR_ADC_CONTRL value to be 0 to 12, LTC7132 can do fast data conversion with only 8ms to 10ms. See section PMBus Command for details.

Note 7: The IOUT_CAL_GAIN = 1.0mΩ and MFR_IOUT_TC = 0.0. Value as read from READ_IOUT in Amperes.

Note 8: Part tested with PWM disabled. Evaluation in application demonstrates capability. TUE(%) = ADC Gain Error (%) +100 • (Zero code Offset + ADC Linearity Error)/Actual Value.

Note 9: All V_{OUT} commands assume the ADC is used to auto zero the output to achieve the stated accuracy. LTC7132 is tested in a feedback loop that servos V_{OUT} to a specified value.

ELECTRICAL CHARACTERISTICS

Note 10: The maximum programmable V_{OUT} voltage is 5.5V when the output voltage range is High and 2.75V when the output voltage range is Low.

Note 11: The maximum V_{IN} voltage is 20V.

Note 12: EEPROM endurance and retention are guaranteed by design, characterization and correlation with statistical process controls. Data retention is production tested via a high temperature at wafer level. The minimum retention specification applies for devices whose EEPROM has been cycled less than the minimum endurance specification. The RESTORE_USER_ALL command (NVM read) is valid over the entire operating junction temperature range.

Note 13: MFR_PWM_MODE[1]=1 or 0 sets the output voltage range Low or High.

Note 14: MFR_PWM_MODE_[5] = 0 or 1 sets the temperature measurement method through ΔV_{BE}, or through $2V_{BE}$.

Note 15: MFR_PWM_MODE[2] = 1 or 0 sets device in ultralow DCR mode or typical DCR mode respectively. MFR_PWM_MODE[7]=1 or 0 sets device in high output current range or low current range. See "Output Current Sensing and Sub-Milliohm DCR Current Sensing" in Operation Section for details. Only V_{LIMIT} codes 1-9 are supported for DCR sensing.

Note 16: The LTC7132 quiescent current (I_Q) equals the I_Q of V_{IN} plus the I_Q of $EXTV_{CC}$.

Note 17: The LTC7132 includes overtemperature protection that is intended to protect the device during momentary overload conditions. Junction temperature will exceed 125°C when overtemperature protection is active. Continuous operation above the specified maximum operating junction temperature may impair device reliability.

Note 18: Write operations above T_J = 85°C or below 0°C are possible although the Electrical Characteristics are not guaranteed and the EEPROM will be degraded. Read operations performed at temperatures below 125°C will not degrade the EEPROM. Writing to the EEPROM above 85°C will result in a degradation of retention characteristics.

Note 19: Properly adjust the input current sensing resistor R_{VIN} to set the sensing voltage within the maximum voltage of 150mV.

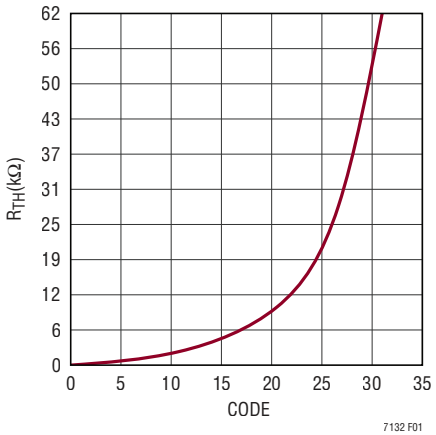
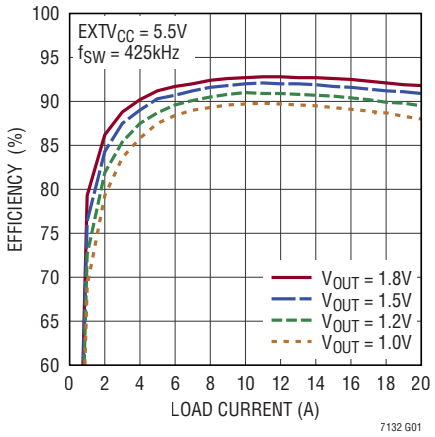


Figure 1. Programmable R_{TH}

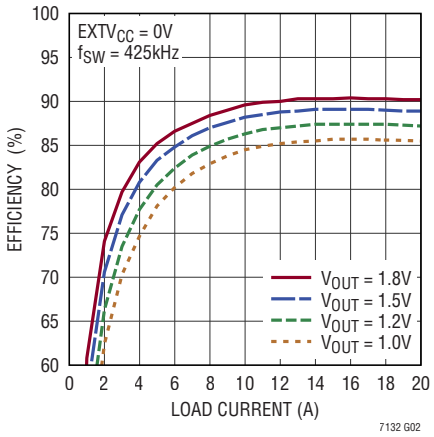
TYPICAL PERFORMANCE CHARACTERISTICS

T_A = 25°C, V_{IN} = 12V, L = 0.3µH, DCR = 0.29mΩ, $EXTV_{CC}$ = 0V unless otherwise noted.

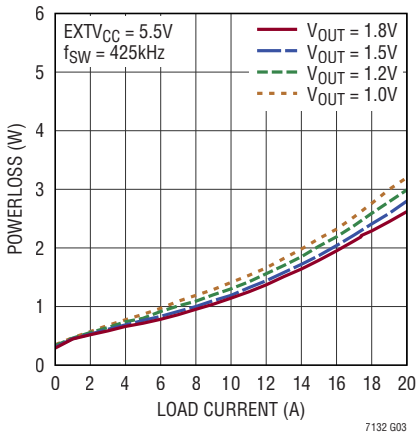
Efficiency vs Load Current



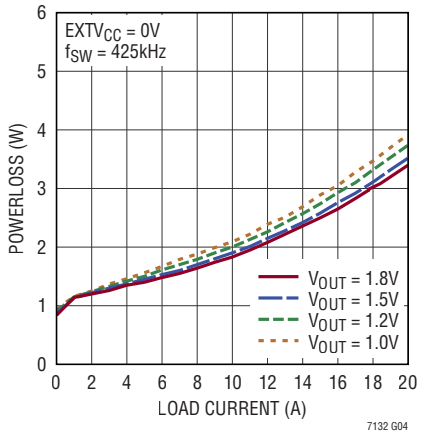
Efficiency vs Load Current



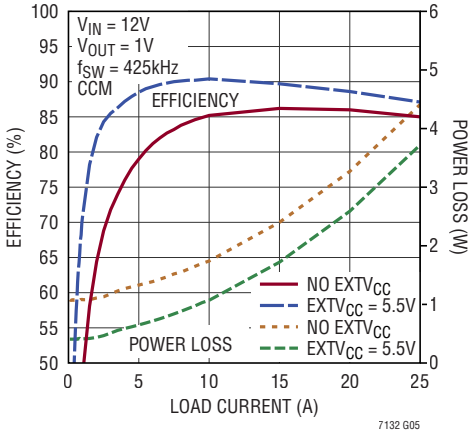
Power Loss vs Load Current



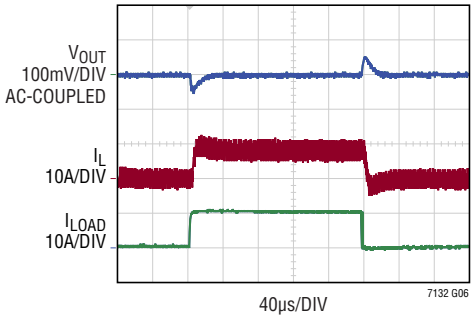
Power Loss vs Output Current



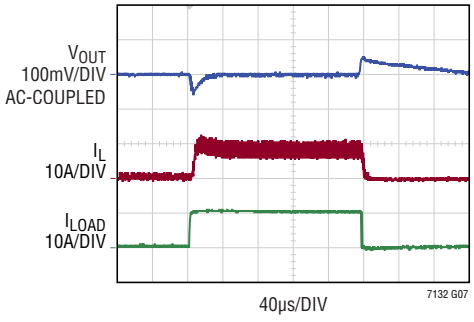
Efficiency and Power Loss vs Load Current



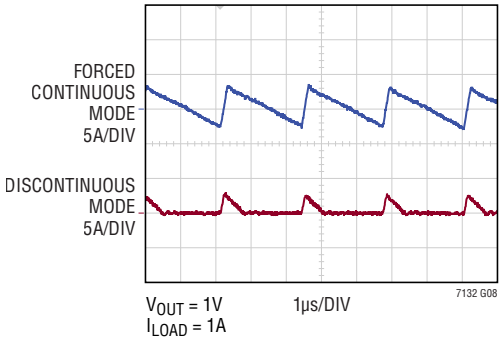
Load Step (Forced Continuous Mode)



Load Step (Discontinuous Mode)



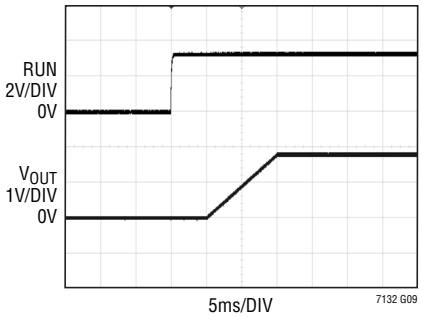
Inductor Current at Light Load



TYPICAL PERFORMANCE CHARACTERISTICS

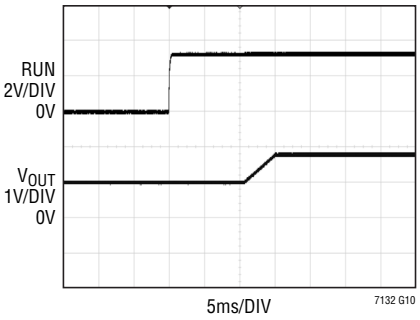
T_A = 25°C, V_{IN} = 12V, L = 0.3µH, DCR = 0.29mΩ, $EXTV_{CC}$ = 0V unless otherwise noted.

Soft-Start Ramp



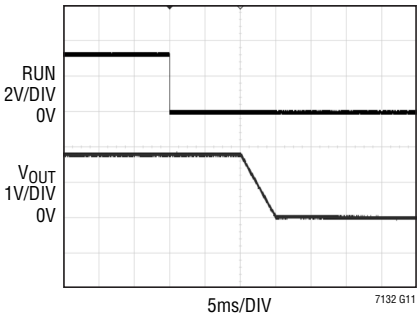
t_{ON_RISE} = 10ms
t_{ON_DELAY} = 5ms
V_{OUT} = 1.8V

Start-Up Into a Pre-Biased Output



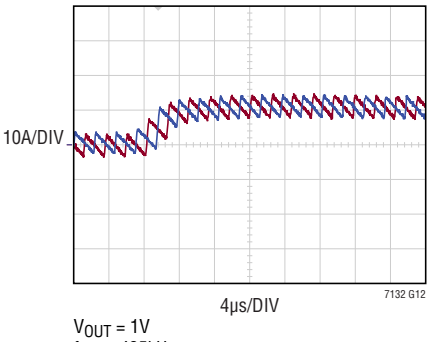
t_{ON_RISE} = 10ms
V_{OUT} = 1.8V

Soft-Off Ramp



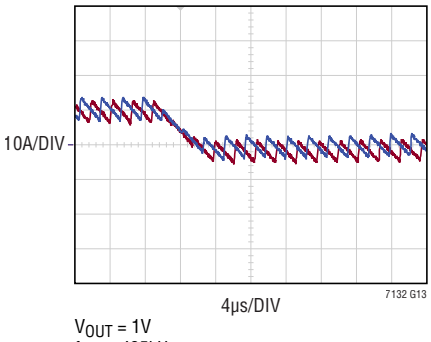
t_{OFF_FALL} = 5ms
t_{OFF_DELAY} = 10ms

Dynamic Current Sharing During a Load Transient in a 2-Phase System



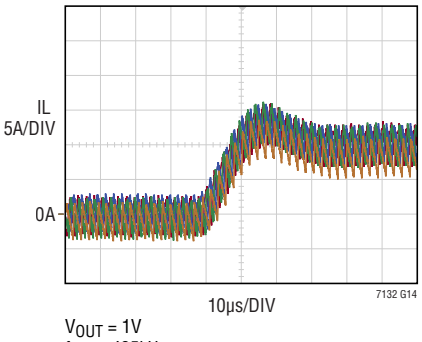
V_{OUT} = 1V
f_{SW} = 425kHz
0A TO 20A LOAD STEP

Dynamic Current Sharing During a Load Transient in a 2-Phase System



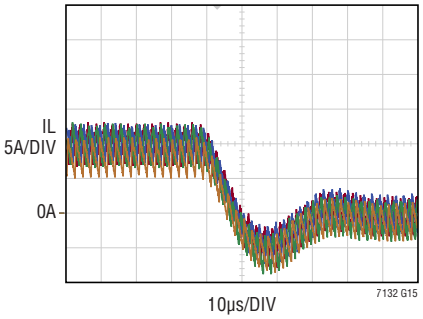
V_{OUT} = 1V
f_{SW} = 425kHz
0A TO 20A LOAD STEP

Dynamic Current Sharing During a Load Transient in a 4-Phase System



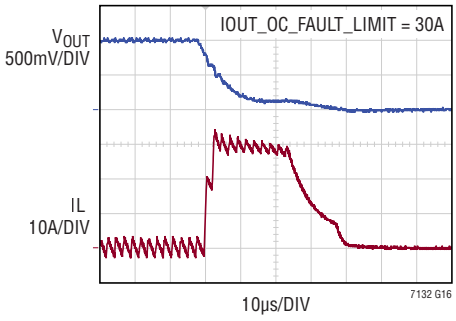
V_{OUT} = 1V
f_{SW} = 425kHz
0A TO 40A LOAD STEP

Dynamic Current Sharing During a Load Transient in a 4-Phase System

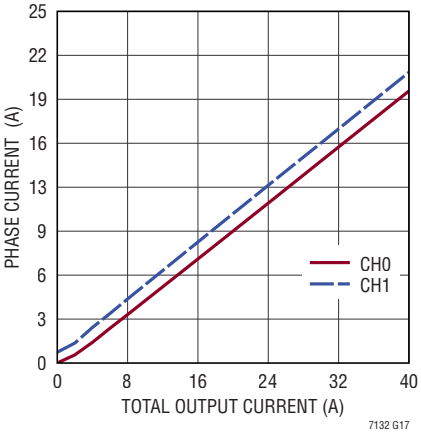


V_{OUT} = 1V
f_{SW} = 425kHz
0A TO 40A LOAD STEP

Current Limit During an Output Short Condition



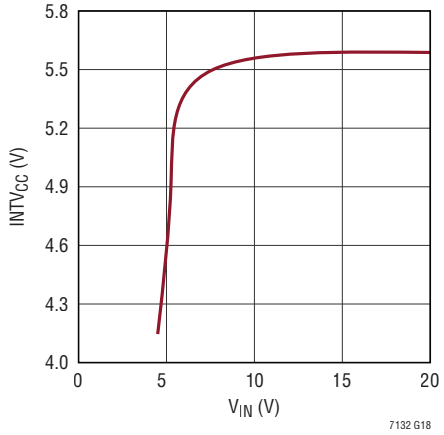
DC Output Current Matching in a 2-Phase System



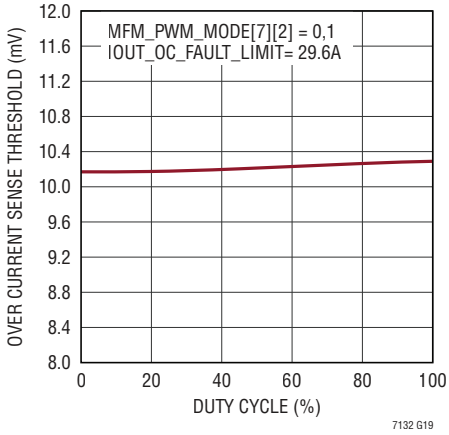
TYPICAL PERFORMANCE CHARACTERISTICS

T_A = 25°C, V_{IN} = 12V, L = 0.3µH, DCR = 0.29mΩ, $EXTV_{CC}$ = 0V unless otherwise noted.

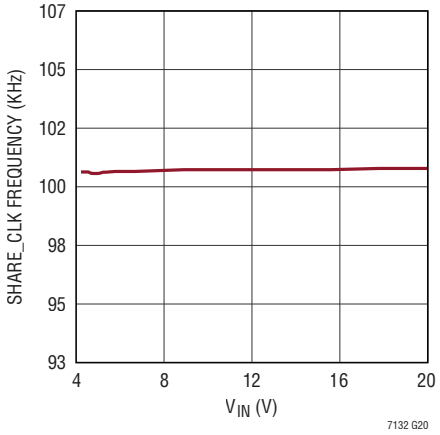
$INTV_{CC}$ Line Regulation



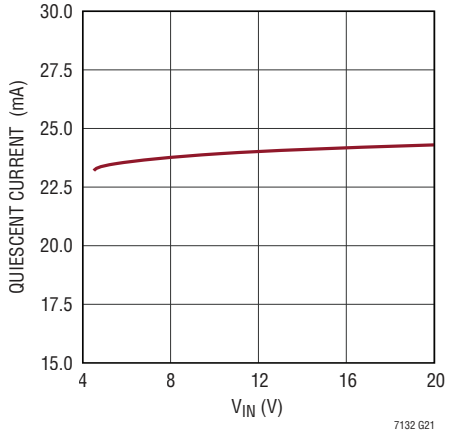
Current Sense Threshold vs Duty Cycle



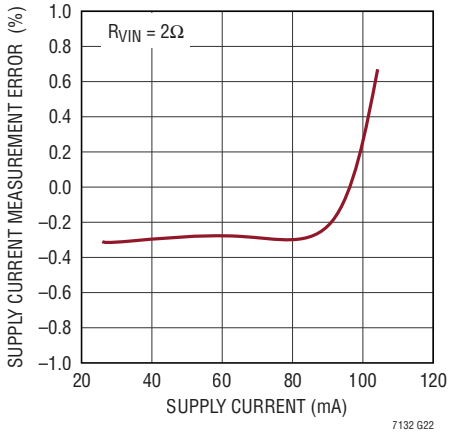
SHARE_CLK Frequency vs Input Voltage



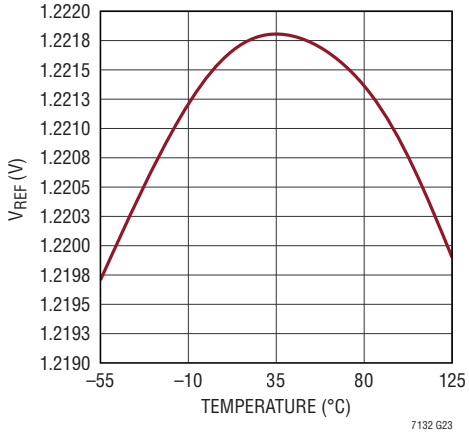
Quiescent Current vs Input Voltage



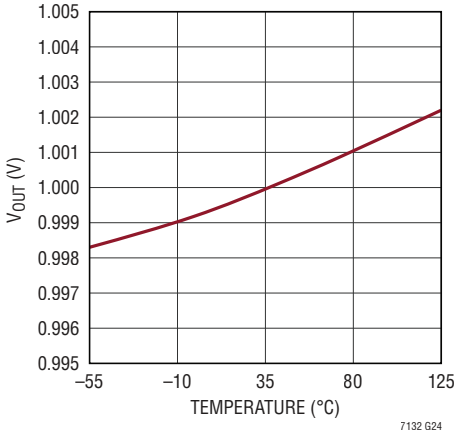
Supply Current Measurement Error vs Supply Current



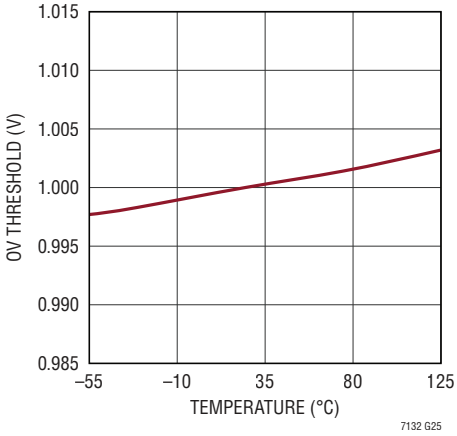
V_{REF} vs Temperature



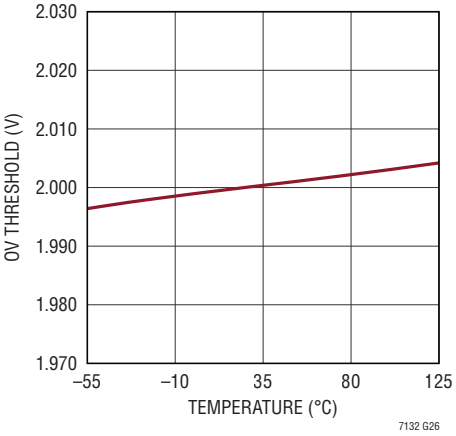
V_{OUT} vs Temperature



V_{OUT} Overvoltage Threshold vs Temperature (Target 1V)



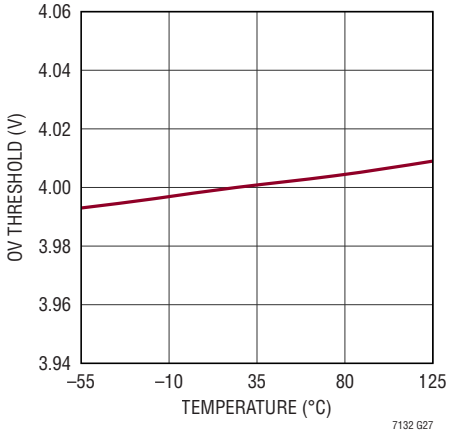
V_{OUT} Overvoltage Threshold vs Temperature (Target 2V)



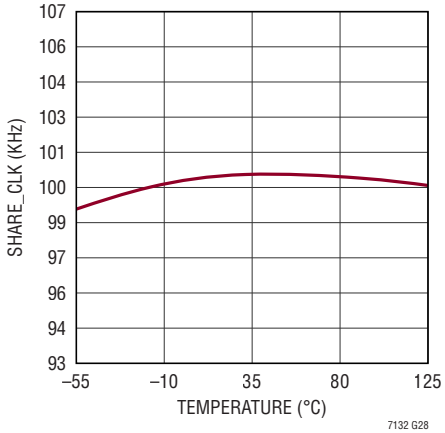
TYPICAL PERFORMANCE CHARACTERISTICS

T_A = 25°C, V_{IN} = 12V, L = 0.3µH, DCR = 0.29mΩ, $EXTV_{CC}$ = 0V unless otherwise noted.

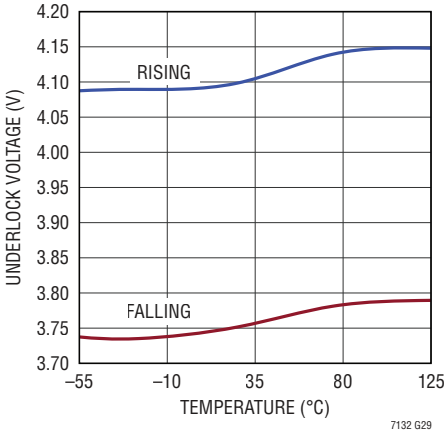
V_{OUT} Overvoltage Threshold vs Temperature (Target 4V)



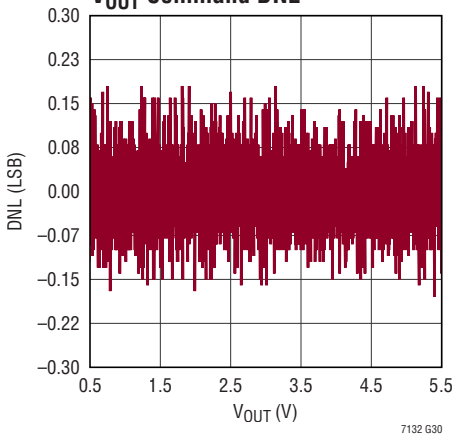
SHARE_CLK vs Temperature



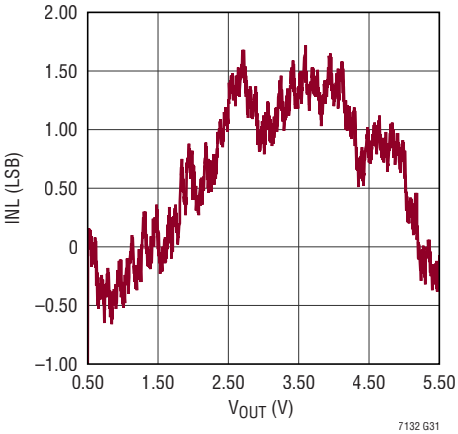
Underlock Voltage vs Temperature



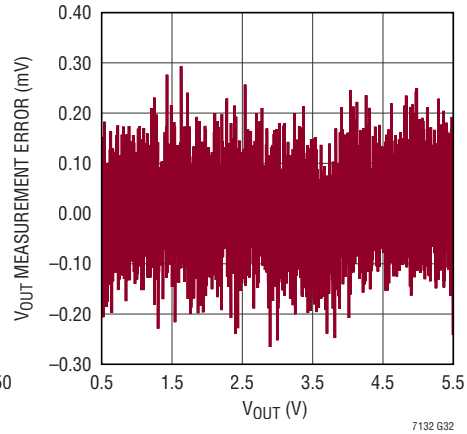
V_{OUT} Command DNL



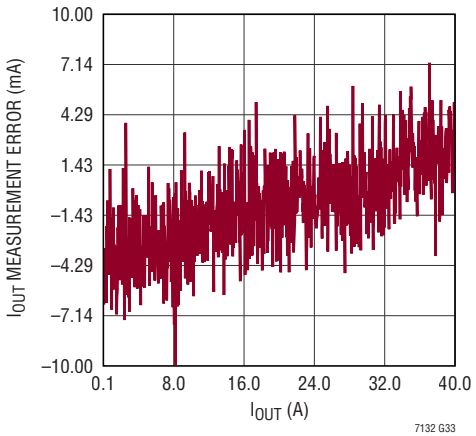
V_{OUT} Command INL



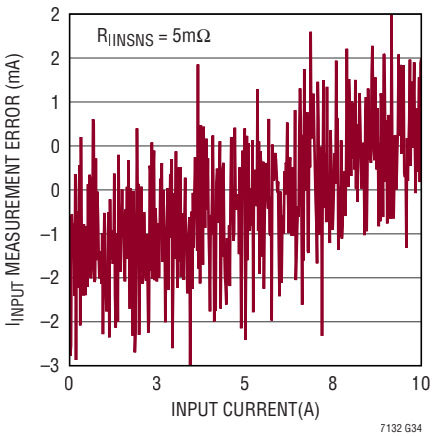
V_{OUT} Error vs V_{OUT}



I_{OUT} Error vs I_{OUT}



Input Current Error vs Input Current



Rev. B

PIN FUNCTIONS

$V_{SENSE0}^+/V_{SENSE1}^+$ (A9/F7): Positive Output Voltage Sense Inputs.

$V_{SENSE0}^-/V_{SENSE1}^-$ (A10/E7): Negative Output Voltage Sense Inputs.

I_{TH0}/I_{TH1} (A7/E5): Current Control Threshold and Error Amplifier Compensation Nodes. Each associated channel's current comparator tripping threshold increases with its I_{TH} voltage.

I_{THR0}/I_{THR1} (B7/E6): Loop Compensation Nodes.

$I_{SENSE0}^+/I_{SENSE1}^+$ (B6/A8): Current sense comparator positive inputs, normally connected to DCR sensing networks or current sensing resistors.

$I_{SENSE0}^-/I_{SENSE1}^-$ (A6/B8): Current sense comparator negative inputs, normally connected to outputs.

SYNC (A4): External Clock Synchronization Input and Open-Drain Output Pin. If an external clock is present at this pin, the switching frequency will be synchronized to the external clock. If clock master mode is enabled, this pin will pull low at the switching frequency with a 500ns pulse to ground. A resistor pull-up to 3.3V is required in the application if the LTC7132 is the master.

SCL (B3): Serial Bus Clock Input. Open-drain output can hold the output low if clock stretching is enabled. A pull-up resistor to 3.3V is required in the application.

SDA (A3): Serial Bus Data Input and Output. A pull-up resistor to 3.3V is required in the application.

$\overline{\text{ALERT}}$ (A2): Open-Drain Digital Output. Connect the $\overline{\text{SMBALERT}}$ signal to this pin. A pull-up resistor to 3.3V is required in the application.

$\overline{\text{FAULT0}}/\overline{\text{FAULT1}}$ (A1/B1): Digital Programmable FAULT Inputs and Outputs. Open-drain output. A pull-up resistor to 3.3V is required in the application.

RUN0/RUN1 (C1/C2): Enable Run Input and Output. Logic high on these pins enables the controller. An open-drain output holds the pin low until the LTC7132 is out of reset. A pull-up resistor to 3.3V is required in the application.

ASEL0/ASEL1 (D1/E1): Serial Bus Address Select Inputs. Connect optional ±1% resistor dividers between V_{DD25} and SGND to these pins to select the serial bus interface address. Refer to the Applications Information section for more details. Minimize capacitance when the pin is open to assure accurate detection of the pin state.

$V_{OUT0\_CFG}/V_{OUT1\_CFG}$ (D2/F1): Output Voltage Select Pins. Connect optional ±1% resistor divider between V_{DD25} VOUT_CFG and SGND in order to select output voltage for each channel. If the pin is left open, the IC will use the value programmed in EEPROM. Refer to the Applications Information section for more details. Minimize capacitance when the pin is open to assure accurate detection of the pin state.

FREQ_CFG (E2): Frequency Select Pin. Connect optional ±1% resistor divider between V_{DD25} and FREQ_CFG SGND in order to select PWM switching frequency. Refer to the Applications Information section for more details. Minimize capacitance when the pin is open to assure accurate detection of the pin state.

PHASE_CFG (F2): Phase Select Pin. Connect ±1% resistor divider between V_{DD25} PHASE_CFG SGND to this pin to configure the phase of each PWM channel relative to SYNC. If the pin is left open, the IC will use the value programmed in the NVM. Refer to the Applications Information section for more details. Minimize capacitance when the pin is open to assure accurate detection of the pin state.

V_{DD25} (F3): Internally Generated 2.5V Power Supply Output Pin. Bypass this pin to SGND with a low ESR 1µF capacitor. Do not load this pin with external current except for the ±1% resistor dividers required for the configuration pins.

WP (E4): Write Protect Pin Active High. An internal 10µA current source pulls the pin to V_{DD33}. If WP is high, the PMBus writes are restricted.

SHARE_CLK (E3): Share Clock, Bidirectional Open-Drain Clock Sharing Pin. Nominally 100kHz. Used to synchronize the timing between multiple LTC7132s. Tie all SHARE_CLK pins together. All LTC7132s will synchronize to the fastest clock. A pull-up resistor to 3.3V is required.

PIN FUNCTIONS

V_{DD33} (F4): Internally Generated 3.3V Power Supply Output Pin. Bypass this pin to SGND with a low ESR 1µF capacitor. Do not load this pin with external current except for the pull-up resistors required for $\overline{FAULT}n$, SHARE_CLK, SYNC and possibly RUN*n*, SDA and SCL, PGOOD*n*.

$INTV_{CC}$ (E10): Internal Regulator 5.5V Output. The control circuits are powered from this voltage. Decouple this pin to PGND with a minimum of 4.7µF low ESR tantalum or ceramic capacitor. This regulator is mainly designed for internal circuits, not to be used as supply for the other ICs.

$EXTV_{CC}$ (D9): External Power Input to an Internal Switch Connected to $INTV_{CC}$. This switch closes and supplies the IC power, bypassing the internal regulator whenever $EXTV_{CC}$ is higher than 4.7V and V_{IN} is higher than 7V. $EXTV_{CC}$ also powers up V_{DD33} when $EXTV_{CC}$ is higher than 4.7V and $INTV_{CC}$ is lower than 3.8V. Do not exceed 6V on this pin. Decouple this pin to PGND with a minimum of 4.7µF low ESR tantalum or ceramic capacitor. If the $EXTV_{CC}$ pin is not used to power $INTV_{CC}$, the $EXTV_{CC}$ pin must be tied to GND. The $EXTV_{CC}$ pin may be connected to a higher voltage than the V_{IN} pin.

SV_{IN} (D8): Signal V_{IN}. This pin is the input voltage to power the internal 5.5V $INTV_{CC}$ LDO. Tie this pin to V_{IN} with a 2.2Ω resistor in series between V_{IN} and SV_{IN}. Decouple this pin to PGND with a ceramic capacitor (1µF to 10µF typical).

BOOST0/BOOST1(C9/F10): Boosted Floating Driver Supplies. The (+) terminal of the booststrap capacitors connect to these pins. These pins swing from a diode voltage drop below $INTV_{CC}$ up to V_{IN} + $INTV_{CC}$.

SW0/SW1 (C10, N6, N7, N8, N9, N10, P6, P7, P8, P9, P10/F9, N1, N2, N3, N4, N5, P1, P2, P3, P4, P5): Switch Node Connections to the Output Inductors. Voltage swings at the pins are from a diode (internal body diode) voltage drop below ground to V_{IN}.

TSNS0/TSNS1 (A5/B5): External Diode Temperature Sense. Connect to the anode of a diode connected PNP transistor and star-connect the cathode to GND (Pin 49) in order to sense remote temperature. A bypass capacitor between the anode and cathode must be located in close proximity to the transistor. If external temperature sense elements are not installed, short pin to ground and set the UT_FAULT_LIMIT to –275°C and the UT_FAULT_RESPONSE to ignore.

I_{IN}^+ (B10): Positive Current Sense Comparator Input. If the input current sense amplifier is not used, this pin must be shorted to the I_{IN}^- and V_{IN} pins.

I_{IN}^- (B9): Negative Current Sense Comparator Input. If the input current sense amplifier is not used, this pin must be shorted to the I_{IN}^+ and V_{IN} pins.

PGOOD0/PGOOD1 (C8/F8): Power Good Indicator Outputs. Open-drain logic output that is pulled to ground when the output exceeds the UV and OV regulation window. The output is deglitched by an internal 60µs filter. A pull-up resistor to 3.3V is required in the application.

SGND (C3, C4, C5, C6, C7, D3, D4, D5, D6, D7): Internal Signal Ground. All small-signal and compensation components should connect to this ground, which in turn connects to PGND at a single point.

PV_{IN0}/PV_{IN1} (G6, G7, G8, G9, G10, H6, H7, J6, J7, K6, K7, L6, L7, M6, M7/H1, H2, J1, J2, K1, K2, L1, L2, M1, M2): Main Input Supply. These pins connect directly to the drain of the internal high side power MOSFETs. Decouple these pins to PGND with the input capacitance C_{IN}.

PGND (Pins D10, G1, G2, G3, G4, G5, H3, H4, H5, H8, H9, H10, J3, J4, J5, J8, J9, J10, K3, K4, K5, K8, K9, K10, L3, L4, L5, L8, L9, L10, M3, M4, M5, M8, M9, M10): Power Ground.

BLOCK DIAGRAM (UK PACKAGE)

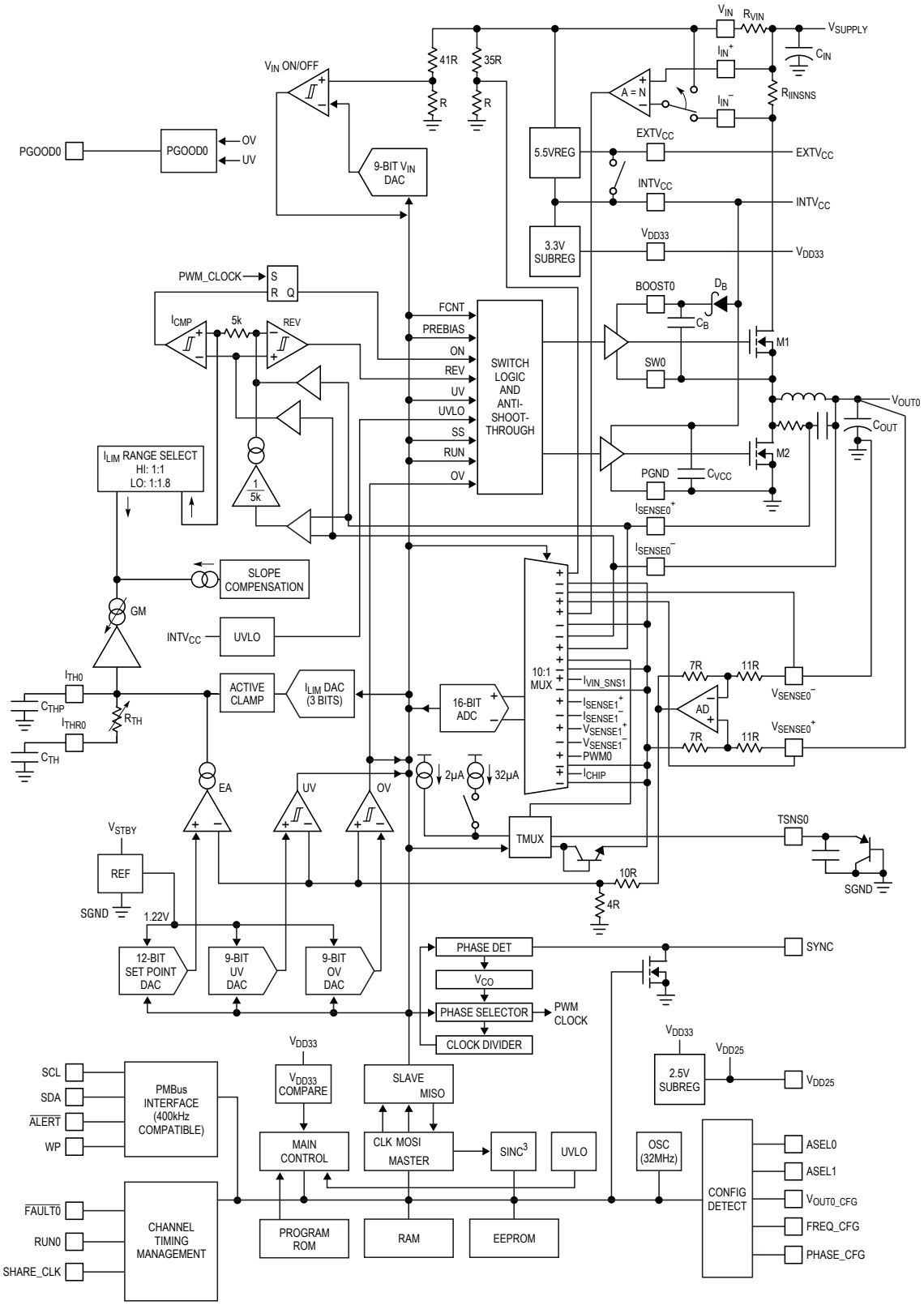


Figure 2. Block Diagram, One of Two Channels (Channel 0 Shown)

OPERATION

OVERVIEW

The LTC7132 is a dual channel/dual phase, constant-frequency, analog peak current mode controller for DC/DC step-down applications with a digital interface. The LTC7132 digital interface is compatible with PMBus which supports bus speeds of up to 400kHz. A Typical Application circuit is shown on the first page of this data sheet.

Major features include:

- **Sub-Milliohm DCR Sensing**
- **Dedicated Power Good Indicators**
- **Direct Input and Chip Current Sensing**
- **Programmable Loop Compensation Parameters**
- **T_{INIT} Start-Up Time: 35ms**
- **PWM Synchronization Circuit, (See Frequency and Phasing Section for Details)**
- **MFR_ADC_CONTROL for Fast ADC Sampling of One Parameter (as Fast as 8ms) (See PMBus Command for Details)**
- **Fully Differential Output Sensing for Both Channels; VOUT0/1 Both Programmable Up to 5.5V**
- **Power-Up and Program EEPROM with $EXTV_{CC}$**
- **Input Voltage Up to 20V**
- **Dual Diode Temperature Sensing**
- **SYNC Contention Circuit (Refer to Frequency and Phase Section for Details)**
- Fault Logging
- Programmable Output Voltage
- Programmable Input Voltage On and Off Threshold Voltage
- Programmable Current Limit
- Programmable Switching Frequency
- Programmable OV and UV Threshold voltage
- Programmable ON and Off Delay Times
- Programmable Output Rise/Fall Times
- Phase-Locked Loop for Synchronous PolyPhase Operation (2, 3, 4 or 6 Phases).
- Integrated Gate Drivers
- Nonvolatile Configuration Memory with ECC
- Optional External Configuration Resistors for Key Operating Parameters
- Optional Timebase Interconnect for Synchronization Between Multiple Controllers
- WP Pin to Protect Internal Configuration
- Stand Along Operation After User Factory Configuration
- PMBus, Version 1.2, 400kHz Compliant Interface

The PMBus interface provides access to important power management data during system operation including:

- Internal Controller Temperature
- External System Temperature via Optional Diode Sense Elements
- Average Output Current
- Average Output Voltage
- Average Input Voltage
- Average Input Current
- Average Chip Input Current from V_{IN}
- Configurable, Latched and Unlatched Individual Fault and Warning Status

Individual channels are accessed through the PMBus using the PAGE command, i.e., PAGE 0 or 1.

Fault reporting and shutdown behavior are fully configurable. Two individual $\overline{FAULT0}$, $\overline{FAULT1}$ outputs are provided, both of which can be masked independently. Three dedicated pins for $\overline{ALERT}$, PGOOD0/1 functions are provided. The shutdown operation also allows all faults to be individually masked and can be operated in either unlatched (hiccup) or latched modes.

Individual status commands enable fault reporting over the serial bus to identify the specific fault event. Fault or warning detection includes the following:

- Output Undervoltage/Overvoltage

OPERATION

- Input Undervoltage/Overvoltage
- Input and Output Overcurrent
- Internal Overtemperature
- External Overtemperature
- Communication, Memory or Logic (CML) Fault

MAIN CONTROL LOOP

The LTC7132 is a constant-frequency, current mode step-down controller containing two channels operating with user-defined relative phasing. During normal operation the top MOSFET is turned on when the clock for that channel sets the RS latch, and turned off when the main current comparator, I_{CMP}, resets the RS latch. The peak inductor current at which I_{CMP} resets the RS latch is controlled by the voltage on the I_{TH} pin which is the output of each error amplifier, EA. The EA negative terminal is equal to the differential voltage between V_{SENSE}^+ and V_{SENSE}^- divided by 5.5 (or 2.75 if MFR_PWM_MODE[1] = 1). The positive terminal of the EA is connected to the output of a 12-bit DAC with values ranging from 0V to 1.024V. The output voltage, through feedback of the EA, will be regulated to 5.5 times the DAC output (or 2.75 times). The DAC value is calculated by the part to synthesize the user's desired output voltage. The output voltage is programmed by the user either with the resistor configuration pins detailed in Table 3 or by the PMBus V_{OUT} command (either from EEPROM or by PMBus command). Refer to the PMBus command section of the data sheet or the PMBus specification for more details. The PMBus VOUT_COMMAND can be executed at any time while the device is running. This command will typically have a latency less than 10ms. The user is encouraged to refer to the PMBus Power System Management Protocol Specification to understand how to program the LTC7132.

Continuing the basic operation description, the current-mode controller will turn off the top gate when the peak current is reached. If the load current increases, sense voltage will slightly droop with respect to the DAC reference. This causes the I_{TH} voltage to increase until the average inductor current matches the new load current. After the top MOSFET has turned off, the bottom MOSFET is turned on. In continuous conduction mode, the bottom MOSFET stays on until the end of the switching cycle.

EEPROM

The LTC7132 contains internal EEPROM (nonvolatile memory) with error correction coding (ECC) to store user configuration settings and fault log information. EEPROM endurance retention and mass write operation time are specified in the Electrical Characteristics and Absolute Maximum Ratings sections. Write operations above T_J = 85°C are possible although the Electrical Characteristics are not guaranteed and the EEPROM will be degraded. Read operations performed at temperatures between –40°C and 125°C will not degrade the EEPROM. Writing to the EEPROM above 85°C will result in a degradation of retention characteristics. The fault logging function, which is useful in debugging system problems that may occur at high temperatures, only writes to fault log EEPROM locations. If occasional writes to these registers occur above 85°C, the slight degradation in the data retention characteristics of the fault log will not take away from the usefulness of the function.

It is recommended that the EEPROM not be written when the die temperature is greater than 85°C. If the die temperature exceeds 130°C, the LTC7132 will disable all EEPROM write operations. All EEPROM write operations will be re-enabled when the die temperature drops below 125°C. (The controller will also disable all the switching when the die temperature exceeds the internal overtemperature fault limit 160°C with a 10°C hysteresis)

The degradation in EEPROM retention for temperatures >125°C can be approximated by calculating the dimensionless acceleration factor using the following equation:

$$AF = e^{\left[\left(\frac{Ea}{k}\right)\bullet\left(\frac{1}{T_{USE}+273}-\frac{1}{T_{STRESS}+273}\right)\right]}$$

where:

AF = acceleration factor

Ea = activation energy = 1.4eV

K = $8.617 \bullet 10^{-5}$ eV/°K

T_{USE} = 125°C specified junction temperature

T_{STRESS} = actual junction temperature in °C

OPERATION

Example: Calculate the effect on retention when operating at a junction temperature of 135°C for 10 hours.

T_{STRESS} = 130°C

T_{USE} = 125°C,

$AF = e^{([(1.4/8.617 \bullet 10^{-5}) \bullet (1/398 - 1/403)])} = 16.6$

The equivalent operating time at 125°C = 16.6 hours.

Thus the overall retention of the EEPROM was degraded by 16.6 hours as a result of operating at a junction temperature of 130°C for 10 hours. The effect of the overstress is negligible when compared to the overall EEPROM retention rating of 87,600 hours at a maximum junction temperature of 125°C.

The integrity of the entire onboard EEPROM is checked with a CRC calculation each time its data is to be read, such as after a power-on reset or execution of a RESTORE_USER_ALL command. If a CRC error occurs, the CML bit is set in the STATUS_BYTE and STATUS_WORD commands, the EEPROM CRC Error bit in the STATUS_MFR_SPECIFIC command is set, and the $\overline{ALERT}$ and RUN pins pulled low (PWM channels off). At that point the device will only respond at special address 0x7C, which is activated only after an invalid CRC has been detected. The chip will also respond at the global addresses 0x5A and 0x5B, but use of these addresses when attempting to recover from a CRC issue is not recommended. All power supply rails associated with either PWM channel of a device reporting an invalid CRC should remain disabled until the issue is resolved. See the Applications Information section or contact the factory for details on efficient in-system EEPROM programming, including bulk EEPROM Programming, which the LTC7132 also supports.

POWER-UP AND INITIALIZATION

The LTC7132 is designed to provide standalone supply sequencing and controlled turn-on and turn-off operation. It operates from a single input supply (4.5V to 20V) while three on-chip linear regulators generate internal 2.5V, 3.3V and 5.5V. If V_{IN} does not exceed 6V, and the $EXTV_{CC}$ pin is not driven by an external supply, the $INTV_{CC}$ and SV_{IN} pins must be tied together. The controller configuration is initialized by an internal threshold based UVLO where SV_{IN} must be approximately 4V and the 5.5V, 3.3V and 2.5V linear regulators must be within approximately 20% of the regulated values. In addition to power supply,a PMBus RESTORE_USER_ALL or MFR_RESET command can initialize the part too.

The $EXTV_{CC}$ pin is driven by an external regulator to improve efficiency of the circuit and minimize power loss on the LTC7132 when V_{IN} is high. The $EXTV_{CC}$ pin must exceed approximately 4.8V, and SV_{IN} must exceed 7V before the $INTV_{CC}$ LDO operates from the $EXTV_{CC}$ pin. To minimize application power, the $EXTV_{CC}$ pin can be supplied by a switching regulator.

During initialization, the external configuration resistors are identified and/or contents of the NVM are read into the controller's commands. The RUN*n* and $\overline{FAULT}$*n* and PGOOD*n* are held low. The LTC7132 will use the contents of Tables 12 to 15 to determine the resistor defined parameters. See the Resistor Configuration section for more details. The resistor configuration pins only control some of the preset values of the controller. The remaining values are programmed in NVM either at the factory or by the user.

If the configuration resistors are not inserted or if the ignore RCONFIG bit is asserted (bit 6 of the MFR_CONFIG_ALL configuration command), the LTC7132 will use only the contents of NVM to determine the DC/DC characteristics. The ASEL0/1 value read at power-up or reset is always respected unless the pin is open. The ASEL0/1 will set the MSB and the LSB from the detected threshold. See the Applications Information section for more details.

After the part has initialized, an additional comparator monitors SV_{IN}. The SVIN_ON threshold must be exceeded before the output power sequencing can begin. After SV_{IN} is initially applied, the part will typically require 70ms to initialize and begin the TON_DELAY timer. The readback of voltages and currents may require an additional 0ms to 90ms.

SOFT-START

The method of start-up sequencing described below is time based. The part must enter the run state prior to soft-start. The run pins are released by the LTC7132 after

OPERATION

the part is initialized and SV_{IN} is greater than the SVIN_ON threshold. If multiple LTC7132s are used in an application, they all hold their respective run pins low until all devices are initialized and SV_{IN} exceeds the SVIN_ON threshold for every device. The SHARE_CLK pin assures all the devices connected to the signal use the same time base. The SHARE_CLK pin is held low until the part has been initialized after V_{IN} is applied. The LTC7132 can be set to turn-off (or remain off) if SHARE_CLK is low (set bit 2 of MFR_CHAN_CONFIG to 1). This allows the user to assure synchronization across numerous ADI ICs even if the RUN pins cannot be connected together due to board constraints. In general, if the user cares about synchronization between chips it is best not only to connect all the respective RUN pins together but also to connect all the respective SHARE_CLK pins together and pull up to V_{DD33} with a 10k resistor. This assures all chips begin sequencing at the same time and use the same time base.

After the RUN pins release and prior to entering a constant output voltage regulation state, the LTC7132 performs a monotonic initial ramp or "soft-start". Soft-start is performed by actively regulating the load voltage while digitally ramping the target voltage from 0V to the commanded voltage set-point. Once the LTC7132 is commanded to turn on (after power up and initialization), the controller waits for the user specified turn-on delay (TON_DELAY) prior to initiating this output voltage ramp. The rise time of the voltage ramp can be programmed using the TON_RISE command to minimize inrush currents associated with the start-up voltage ramp. The soft-start feature is disabled by setting the value of TON_RISE to any value less than 0.25ms. The LTC7132 PWM always uses discontinuous mode during the TON_RISE operation. In discontinuous mode, the bottom gate is turned off as soon as reverse current is detected in the inductor. This will allow the regulator to start up into a pre-biased load. When the TON_MAX_FAULT_LIMIT is reached, the part transitions to continuous mode, if so programmed. If TON_MAX_FAULT_LIMIT is set to zero, there is no time limit and the part transitions to the desired conduction mode after TON_RISE completes and V_{OUT} has exceeded the VOUT_UV_FAULT_LIMIT and IOUT_OC is not present. However setting TON_MAX_FAULT_LIMIT to a value of 0 is not recommended.

TIME-BASED SEQUENCING

The default mode for sequencing the outputs on and off is time based. Each output is enabled after waiting TON_ DELAY amount of time following either a RUN pin going high, a PMBus command to turn on or the V_{IN} rising above a pre-programmed voltage. Off sequencing is handled in a similar way. To assure proper sequencing, make sure all ICs connect the SHARE_CLK pin together and RUN pins together. If the RUN pins cannot be connected together for some reasons, set bit 2 of MFR_CHAN_ CONFIG to 1. This bit requires the SHARE_CLK pin to be clocking before the power supply output can start. When the RUN pin is pulled low, the LTC7132 will hold the pin low for the MFR_ RESTART_DELAY. The minimum MFR_RESTART_ DELAY is TOFF_DELAY + TOFF_FALL + 136ms. This delay assures proper sequencing of all rails. The LTC7132 calculates this delay internally and will not process a shorter delay. However, a longer commanded MFR_RESTART_DELAY will be used by the part. The maximum allowed value is 65.52 seconds.

VOLTAGE-BASED SEQUENCING

The sequence can also be voltage based. As shown in Figure 3, The PGOOD*n* pin is asserted when the UV threshold is exceeded for each output. It is possible to feed the PGOOD pin from one LTC7132 into the RUN pin of the next LTC7132 in the sequence, especially across multiple LTC7132s. The PGOOD*n* has a 60µs filter. If the V_{OUT} voltage bounces around the UV threshold for a long period of time it is possible for the PGOOD*n* output to toggle more than once. To minimize this problem, set the TON_RISE time under 100ms.

Voltage-Based Sequencing by Cascading PGs Into RUN Pins

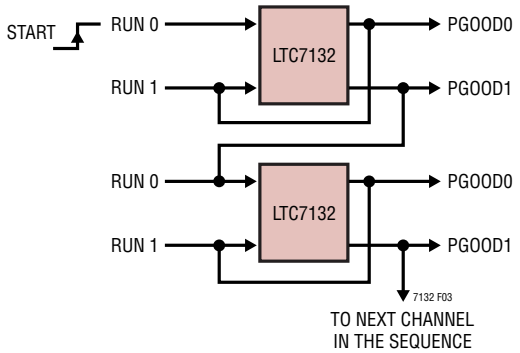


Figure 3. Event (Voltage) Based Sequencing

OPERATION

If a fault in the string of rails is detected, only the faulted rail and downstream rails will fault off. The rails in the string of devices in front of the faulted rail will remain on unless commanded off.

SHUTDOWN

The LTC7132 supports two shutdown modes. The first mode is closed-loop shutdown response, with user defined turn-off delay (TOFF_DELAY) and ramp down rate (TOFF_FALL). The controller will maintain the mode of operation for TOFF_FALL. The second mode is discontinuous conduction mode, the controller will not draw current from the load and the fall time will be set by the output capacitance and load current, instead of TOFF_FALL.

The shutdown occurs in response to a fault condition or loss of SHARE_CLK (if bit 2 of MFR_CHAN_ CONFIG is set to a 1) or SV_{IN} falling below the VIN_OFF threshold or $\overline{FAULT}$ pulled low externally (if the MFR_FAULT_ RESPONSE is set to inhibit). Under these conditions the power stage is disabled in order to stop the transfer of energy to the load as quickly as possible. The shutdown state can be entered from the soft-start or active regulation states or through user intervention.

There are two ways to respond to faults; which are retry mode and latched off mode. In retry mode, the controller responds to a fault by shutting down and entering the inactive state for a programmable delay time (MFR_RETRY_DELAY). This delay minimizes the duty cycle associated with autonomous retries if the fault that causes the shutdown disappears once the output is disabled. The retry delay time is determined by the longer of the MFR_RETRY_ DELAY command or the time required for the regulated output to decay below 12.5% of the programmed value. If multiple outputs are controlled by the same $\overline{FAULT}n$ pin, the decay time of the faulted output determines the retry delay. If the natural decay time of the output is too long, it is possible to remove the voltage requirement of the MFR_RETRY_DELAY command by asserting bit 0 of MFR_CHAN_CONFIG. Alternatively, latched off mode means the controller remains latched-off following a fault and clearing requires user intervention such as toggling RUN*n* or commanding the part OFF then ON.

LIGHT-LOAD CURRENT OPERATION

The LTC7132 has two modes of operation: high efficiency discontinuous conduction mode or forced continuous conduction mode. Mode selection is done using the MFR_PWM _MODE command (discontinuous conduction is always the start-up mode, forced continuous is the default running mode).

If a controller is enabled for discontinuous operation, the inductor current is not allowed to reverse. The reverse current comparator's output, I_{REV}, turns off the bottom gate of the external MOSFET just before the inductor current reaches zero, preventing it from reversing and going negative.

In forced continuous operation, the inductor current is allowed to reverse at light loads or under large transient conditions. The peak inductor current is determined solely by the voltage on the I_{TH} pin. In this mode, the efficiency at light loads is lower than in discontinuous mode operation. However, continuous mode exhibits lower output ripple and less interference with audio circuitry, but may result in reverse inductor current, which can cause the input supply to boost. The VIN_OV_FAULT_LIMIT can detect this and turn off the offending channel. However, this fault is based on an ADC read and can take up to $t_{CONVERT}$ to detect. If there is a concern about the input supply boosting, keep the part in discontinuous conduction mode.

If the part is set to discontinuous mode operation, as the inductor average current increases, the controller will automatically modify the operation from discontinuous mode to continuous mode.

SWITCHING FREQUENCY AND PHASE

The switching frequency of the PWM can be established with an internal oscillator or an external time base. The internal phase-locked loop (PLL) synchronizes PWM control to this timing reference with proper phase relation, whether the clock is provided internally or externally. The device can also be configured to provide the master clock to other ICs through PMBus command, NVM setting, or external configuration resistors as outlined in Table 4.

As clock master, the LTC7132 will drive its open-drain SYNC pin at the selected rate with a pulse width of 500ns.

OPERATION

An external pull-up resistor between SYNC and V_{DD33} is required in this case. Only one device connected to SYNC should be designated to drive the pin. But if multiple LTC7132s programmed as clock masters are wired to the same SYNC line with a pull-up resistor, just one of the devices is automatically elected to provide clocking, and the others disable their SYNC outputs.

The LTC7132 will automatically revert to an external SYNC input, disabling its own SYNC, as long as the external SYNC frequency is greater than 80% of the programmed SYNC frequency. The external SYNC input shall have a duty cycle between 20% and 80%.

Whether configured to drive SYNC or not, the LTC7132 can continue PWM operation using its own internal oscillator if an external clock signal is subsequently lost. The device can also be programmed to always require an external oscillator for PWM operation by setting bit 4 of MFR_CONFIG_ALL. The status of the SYNC driver circuit is indicated by bit 10 of MFR_PADS.

The MFR_PWM_CONFIG command can be used to configure the phase of each channel. Desired phase can also be set from EEPROM or external configuration resistors as outlined in Table 5. Designated phase is the relationship between the falling edge of SYNC and the internal clock edge that sets the PWM latch to turn on the top power switch. Additional small propagation delays to the PWM control pins will also apply. Both channels must be off before the FREQUENCY_SWITCH and MFR_PWM_CONFIG commands can be written to the LTC7132.

The phase relationships and frequency are independent of each other, providing numerous application options. Multiple LTC7132 ICs can be synchronized to realize a PolyPhase array. In this case the phases should be separated by 360/n degrees, where n is the number of phases driving the output voltage rail.

PWM LOOP COMPENSATION

The internal PWM loop compensation resistors R_{ITHn} of the LTC7132 can be adjusted using bit[4:0] of the MFR_PWM_COMP command.

The transconductance of the LTC7132 PWM error amplifier can be adjusted using bit[7:5] of the MFR_PWM_COMP command. These two loop compensation parameters can be programmed when device is in operation. Refer to the Programmable Loop Compensation subsection in the Applications Information section for further details.

OUTPUT VOLTAGE SENSING

Both channels in LTC7132 have differential amplifiers, which allow the remote sensing of the load voltage between V_{SENSEn}^+ and V_{SENSEn}^- pins. The telemetry ADC is also fully differential and makes measurements between V_{SENSEn}^+ and V_{SENSEn}^- pins respectively. The maximum allowed sense voltages for both channels is 5.5V.

$INTV_{CC}$/$EXTV_{CC}$ POWER

Power for the top and bottom MOSFET drivers and most of the internal circuitry is derived from the $INTV_{CC}$ pin. When the $EXTV_{CC}$ pin is shorted to GND or tied to a voltage less than 4.7V, an internal 5.5V linear regulator supplies $INTV_{CC}$ power from SV_{IN}. If $EXTV_{CC}$ is taken above 4.7V and SV_{IN} is higher than 7.0V, the 5.5V regulator is turned off and an internal switch is turned on, connecting $EXTV_{CC}$ to $INTV_{CC}$. Using the $EXTV_{CC}$ allows the $INTV_{CC}$ power to be derived from a high efficiency external source such as a switching regulator output.

$EXTV_{CC}$ can provide power to the internal 3.3V linear regulator even when V_{IN} is not present, which allows the LTC7132 to be initialized and programmed even without main power being applied.

Each top MOSFET driver is biased from the floating bootstrap capacitor, C_B, which normally recharges during each off cycle through an external diode when the bottom MOSFET turns on. If the input voltage V_{IN} decreases to a voltage close to V_{OUT}, the loop may enter dropout and attempt to turn on the top MOSFET continuously. The dropout detector detects this and forces the top MOSFET off for about one-twelfth of the clock period plus 100ns every three cycles to allow C_B to recharge. However, it is recommended that a load be present or the IC operates at low frequency during the drop-out transition to ensure C_B is recharged.

OPERATION

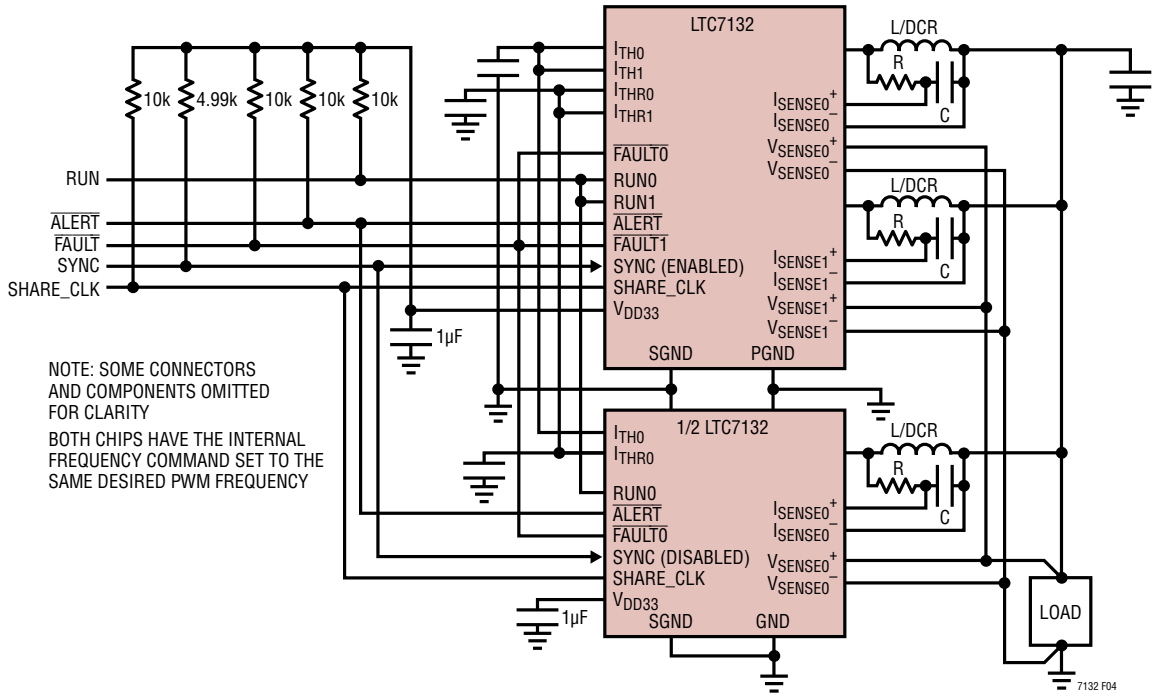


Figure 4. Load Sharing Connections for 3-Phase Operation

OUTPUT CURRENT SENSING AND SUB-MILLIOHM DCR CURRENT SENSING

For DCR current sense applications, a resistor in series with a capacitor is placed across the inductor. In this configuration, the resistor is tied to the SW side of the inductor while the capacitor is tied to the load side of the inductor as shown in Figure 4. If the RC values are chosen such that the RC time constant matches the inductor time constant (L/DCR, where DCR is the inductor series resistance), the resultant voltage appearing across the capacitor equals the voltage across the inductor series resistance (V_{DCR}) and thus represents the current flowing through the inductor. In addition to this regular current sensing, the LTC7132 employs a unique architecture to enhance the signal-to-noise ratio by 14dB, enabling it to operate with a small sense signal (as low as 2mV) via a sub-milliohm value of inductor DCR (such as 0.2mΩ) to improve the power efficiency for the heavy load applications while $V_{OUT} \leq 3.5V$. As shown in Figure 4, externally the new architecture only requires reducing R by 4/5, i.e., R_{LOWDCR} = 1/5Rnomdcr. Better signal-to-noise ratio helps to reduce jitter at the output with as low as 2mV sensing signal. Low DCR improves power efficiency in heavy system loads. So the new DCR sensing scheme provides a perfect solution for larger power, and noise sensitive systems. In the meantime, the current limit threshold is still a function of the inductor peak current and its DCR value, and can be accurately set with the MFR_PWM_MODE[2], MFR_PWM_MODE[7]. See Figure 26.

The RC calculations are based on the room temperature DCR of the inductor. The RC time constant should remain constant as a function of temperature. This assures the transient response of the circuit is the same regardless of the temperature. The DCR of the inductor has a large temperature coefficient, approximately 3900ppm/°C. The temperature coefficient of the inductor must be written to the MFR_IOUT_CAL_GAIN_TC register. The external temperature is sensed near the inductor and used to modify the internal current limit circuit to maintain an essentially constant current limit with temperature. In this application, the I_{SENSEn}^+ pin is connected to the FET side of the DCR sensing filter capacitor while the I_{SENSEn}^- pin is placed on the load side of the capacitor. The current sensed from the input is then given by the expression V_{DCR}/DCR. V_{DCR} is digitized by the LTC7132's telemetry ADC with an input range of ±128mV, a noise

OPERATION

floor of 7μV_{RMS}, and a peak-peak noise of approximately 46.5μV. The LTC7132 computes the inductor current using the DCR value stored in the IOUT_CAL_GAIN command and the temperature coefficient stored in command MFR_IOUT_CAL_GAIN_TC. The resulting current value is returned by the READ_IOUT command.

INPUT CURRENT SENSING

To sense the total input current consumed by the LTC7132 and the power stage, a resistor is placed between the input supply voltage and the PV_{IN} pins. The I_{IN}^+ and I_{IN}^- pins are connected to the sense resistor. The filtered voltage is amplified by the internal high side current sense amplifier and digitized by the LTC7132's telemetry ADC. The input current sense amplifier has three gain settings of 2x, 4x, and 8x set by the bit[6:5] of the MFR_PWM_CONFIG command. The maximum input sense voltage for the three gain settings is 50mV, 20mV, and 5mV respectively. The LTC7132 computes the input current using the R value stored in the IIN_CAL_GAIN command. The resulting measured power stage current is returned by the READ_IIN command.

The LTC7132 uses the RVIN resistor to measure the V_{IN} pin supply current being consumed by the LTC7132. This value is returned by the MFR_READ_ICHIP command. The chip current is calculated by using the R value stored in the MFR_RVIN command. Refer to the subsection titled Input Current Sense Amplifier in the Applications Information section for further details.

PolyPhase LOAD SHARING

Multiple LTC7132s can be arrayed in order to provide a balanced load-share solution by bussing the necessary pins. Figure 4 illustrates the shared connections required for load sharing.

If an external oscillator is not provided, the SYNC pin should only be enabled on one of the LTC7132s. The other(s) should be programmed to disable SYNC using bit 4 of MFR_CONFIG_ALL. If an external oscillator is present, the chip with the SYNC pin enabled will detect the presence of the external clock and disable its output.

Multiple chips need to tie all the V_{SENSE}^+ pins together, and all the V_{SENSE}^- pins together, and I_{THR} and I_{TH} together as well.

Do not assert bit[5] of MFR_PWM_CONFIG except in a PolyPhase application.

EXTERNAL/INTERNAL TEMPERATURE SENSE

External temperature can best be measured using a remote, diode-connected PNP transistor such as the MMBT3906.The emitter should be connected to a TSNS pin while the base and collector terminals of the PNP transistor should be returned directly to the LTC7132 SGND pin. Two different currents are applied to the diode

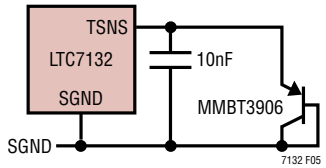


Figure 5. Temperature Sense Circuit

(nominally 2μA and 32μA) and the temperature is calculated from a ΔV_{BE} measurement made with the internal 16-bit monitor ADC (see Figure 5).

The LTC7132 also supports direct V_{BE} based external temperature measurements. In this case the diode or diode network is trimmed to a specific voltage at a specific current and temperature. In general this method does not yield as accurate result as the single PNP transistor ΔV_{BE} method, but may function better in a noisy application. Refer to MFR_PWM_MODE in the PMBus Command Details section for additional information on programming the LTC7132 for these two external temperature sense configurations. The calculated temperature is returned by the PMBus READ_TEMPERATURE_1 command. Refer to the Applications Information section for details on proper layout of external temperature sense elements and PMBus commands that can be used to improve the accuracy of calculated temperatures. The READ_TEMPERATURE_2 command returns the internal junction temperature of the LTC7132 using an on-chip diode with a ΔV_{BE} measurement and calculation.

OPERATION

The slope of the external temperature sensor can be modified with the temperature slope coefficient stored in MFR_TEMP_1_GAIN. Typical PNPs require temperature slope adjustments slightly less than 1. The MMBT3906 has a recommended value in this command of approximately MFR_TEMP_1_GAIN = 0.991 based on the ideality factor of 1.01. Simply invert the ideality factor to calculate the MFR_TEMP_1_GAIN. Different manufacturers and different lots may have different ideality factors. Consult with the manufacturer to set this value. The offset of the external temperature sense can be adjusted by MFR_TEMP_1_OFFSET. A value of 0 in this register sets the temperature offset to –273.15°C.

If the PNP cannot be placed in direct contact with the inductor, the slope or offset can be increased to account for temperature mismatches. If the user is adjusting the slope, the intercept point is at absolute zero, –273.15°C, so small adjustments in slope can change the apparent measured temperature significantly. Another way to artificially increase the slope of the temperature term is to increase the MFR_IOUT_CAL_GAIN_TC term. This will modify the temperature slope with respect to room temperature.

RCONFIG (RESISTOR CONFIGURATION) PINS

There are six input pins utilizing 1% resistor dividers between V_{DD25} and SGND to select key operating parameters. The pins are ASEL0, ASEL1, FREQ_CFG, V_{OUT0_CFG}, V_{OUT1_CFG}, PHASE_CFG. Refer to Tables 3, 4, 5 and 6 for more details of recommended values of these resistive dividers. If pins are floated, the value stored in the corresponding NVM command is used. If bit 6 of the MFR_CONFIG_ALL configuration command is asserted in NVM, the resistor inputs are ignored upon power-up except for ASEL0 and ASEL1 which are always respected. The resistor configuration pins are only measured during a power-up reset or after a MFR_RESET or after a RESTORE_USER_ALL command is executed.

The V_{OUTn_CFG} pin settings are described in Table 3. These pins select the output voltages for the LTC7132's analog PWM controllers. If the pin is open, the VOUT_COMMAND command is loaded from NVM to determine the output voltage. The default setting is to have the switcher off unless the voltage configuration pins are installed.

The following parameters are set as a percentage of the output voltage if the RCONFIG pins are used to determine the output voltage:

- VOUT_OV_FAULT_LIMIT ..... +10%
- VOUT_OV_WARN_LIMIT ..... +7.5%
- VOUT_MAX ..... +7.5%
- VOUT_MARGIN_HIGH 5%
- VOUT_MARGIN_LOW 5%
- VOUT_UV_WARN_LIMIT 6.5%
- VOUT_UV_FAULT_LIMIT 7%

The FREQ_CFG pin settings are described in Table 4. This pin selects the switching frequency. The phase relationships between the two channels and SYNC pin are determined by the PHASE_CFG pin described in Table 5. To synchronize to an external clock, the part should be put into external clock mode (SYNC output disabled but frequency set to the nominal value). If no external clock is supplied, the part will clock at the programmed frequency. If the application is multiphase and the SYNC signal between chips is lost, the parts will not operate at the designed phase even if they are programmed and trimmed to the same frequency. This may increase the ripple voltage on the output, possibly produce undesirable operation. If the external SYNC signal is being generated internally and external SYNC is not selected, bit 10 of MFR_PADS will be asserted. If no frequency is selected and the external SYNC frequency is not present, a PLL_FAULT will occur. If the user does not wish to see the $\overline{\text{ALERT}}$ from a PLL_FAULT even if there is not a valid synchronization signal at power-up, the $\overline{\text{ALERT}}$ mask for PLL_FAULT must be written. See the description on SMBALERT_MASK for more details. If the SYNC pin is connected between multiple ICs only one of the ICs should have the SYNC pin enabled, and all other ICs should be configured to have the SYNC pin disabled.

The ASEL0,1 pin settings are described in Table 6. ASEL1 selects the top 3 bits of the slave address for the LTC7132. ASEL0 selects the bottom 4 bits of the slave address for the LTC7132. If ASEL1 is floating, the 3 most significant bits are retrieved from the NVM MFR_ADDRESS command. If ASEL0 is floating, the 4 LSB bits stored in NVM MFR_ADDRESS command are used to determine the 4 LSB bits of the slave address. For more detail, refer to Table 6.

OPERATION

Note: Per the PMBus specification, pin programmed parameters can be overridden by commands from the digital interface with the exception of ASEL which is always honored. Do not set any part address to 0x5A or 0x5B because these are global addresses and all parts will respond to them.

FAULT DETECTION AND HANDLING

A variety of fault and warning reporting and handling mechanisms are available. Fault and warning detection capabilities include:

- Input OV FAULT Protection and UV Warning
- Average Input OC Warn
- Output OV/UV Fault and Warn Protection
- Output OC Fault and Warn Protection
- Internal and External Overtemperature Fault and Warn Protection
- External Undertemperature Fault and Warn Protection
- CML Fault (Communication, Memory or Logic)
- External Fault Detection via the Bidirectional $\overline{\text{FAULT}}n$ Pins.

In addition, the LTC7132 can map any combination of fault indicators to their respective $\overline{\text{FAULT}}n$ pin using the propagate $\overline{\text{FAULT}}n$ response commands, MFR_FAULT_PROPAGATE. Typical usage of a $\overline{\text{FAULT}}n$ pin is as a driver for an external crowbar device, overtemperature alert, overvoltage alert or as an interrupt to cause a microcontroller to poll the fault commands. Alternatively, the $\overline{\text{FAULT}}n$ pins can be used as inputs to detect external faults downstream of the controller that require an immediate response.

Any fault or warning event will always cause the $\overline{\text{ALERT}}$ pin to assert low unless the fault or warning is masked by the SMBALERT_MASK. The pin will remain asserted low until the CLEAR_FAULTS command is issued, the fault bit is written to a 1 or bias power is cycled or a MFR_RESET command is issued, or the RUN pins are toggled OFF/ON or the part is commanded OFF/ON via PMBus or an ARA command operation is performed. The MFR_FAULT_PROPAGATE command determines if the $\overline{\text{FAULT}}$ pins are pulled low when a fault is detected.

Output and input fault event handling is controlled by the corresponding fault response byte as specified in Tables 7 to 12. Shutdown recovery from these types of faults can either be autonomous or latched. For autonomous recovery, the faults are not latched, so if the fault conditions not present after the retry interval has elapsed, a new soft-start is attempted. If the fault persists, the controller will continue to retry. The retry interval is specified by the MFR_RETRY_DELAY command and prevents damage to the regulator components by repetitive power cycling, assuming the fault condition itself is not immediately destructive. The MFR_RETRY_DELAY must be greater than 120ms. It can not exceed 83.88 seconds.

Status Registers and $\overline{\text{ALERT}}$ Masking

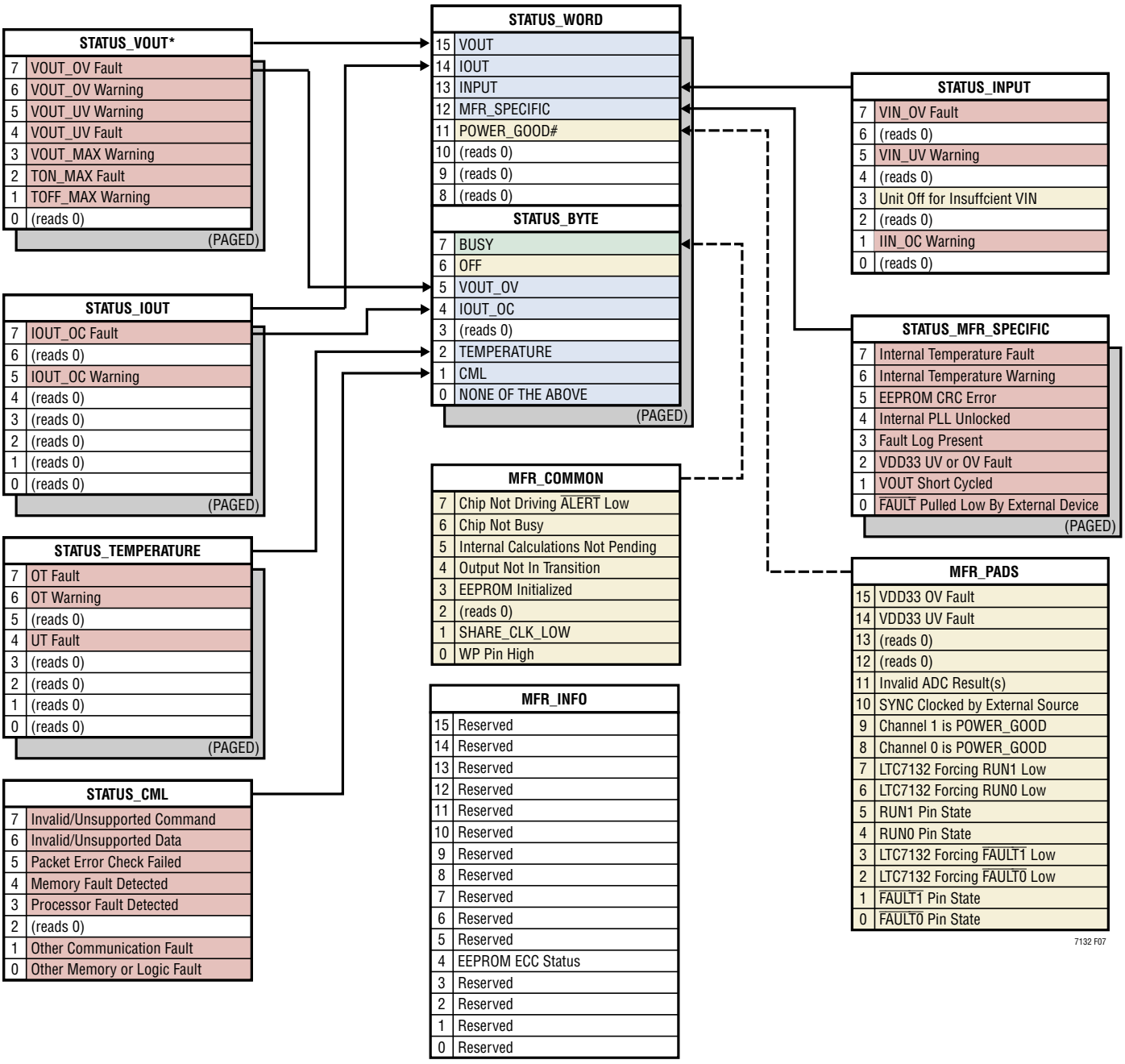
Figure 6 summarizes the internal LTC7132 status registers accessible by PMBus command. These contain indication of various faults, warnings and other important operating conditions. As shown, the STATUS_BYTE and STATUS_WORD commands also summarize contents of other status registers. Refer to PMBus Command Details for specific information.

NONE OF THE ABOVE in STATUS_BYTE indicates that one or more of the bits in the most-significant nibble of STATUS_WORD are also set.

In general, any asserted bit in a STATUS_x register also pulls the $\overline{\text{ALERT}}$ pin low. Once set, $\overline{\text{ALERT}}$ will remain low until one of the following occurs.

- A CLEAR_FAULTS or MFR_RESET Command Is Issued
- The Related Status Bit Is Written to a One
- The Faulted Channel Is Properly Commanded Off and Back On
- The LTC7132 Successfully Transmits Its Address During a PMBus ARA
- Bias Power Is Cycled

OPERATION



DESCRIPTION	MASKABLE	GENERATES ALERT	BIT CLEARABLE
General Fault or Warning Event	Yes	Yes	Yes
General Non-Maskable Event	No	Yes	Yes
Dynamic	No	No	No
Status Derived from Other Bits	No	Not Directly	No

Figure 6. LTC7132 Status Register Summary

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With some exceptions, the SMBALERT_MASK command can be used to prevent the LTC7132 from asserting $\overline{\text{ALERT}}$ for bits in these registers on a bit-by-bit basis. These mask settings are promoted to STATUS_WORD and STATUS_BYTE in the same fashion as the status bits themselves. For example, if $\overline{\text{ALERT}}$ is masked for all bits in Channel 0 STATUS_VOUT, then $\overline{\text{ALERT}}$ is effectively masked for the VOUT bit in STATUS_WORD for PAGE 0.

The BUSY bit in STATUS_BYTE also asserts $\overline{\text{ALERT}}$ low and cannot be masked. This bit can be set as a result of various internal interactions with PMBus communication. This fault occurs when a command is received that cannot be safely executed with one or both channels enabled. As discussed in Application Information, BUSY faults can be avoided by polling MFR_COMMON before executing some commands.

If masked faults occur immediately after power up, $\overline{\text{ALERT}}$ may still be pulled low because there has not been time to retrieve all of the programmed masking information from EEPROM.

Status information contained in MFR_COMMON and MFR_PADS can be used to further debug or clarify the contents of STATUS_BYTE or STATUS_WORD as shown, but the contents of these registers do not affect the state of the $\overline{\text{ALERT}}$ pin and may not directly influence bits in STATUS_BYTE or STATUS_WORD.

Mapping Faults to $\overline{\text{FAULT}}$ Pins

Channel-to-channel fault (including channels from multiple LTC7132s) dependencies can be created by connecting $\overline{\text{FAULT}}n$ pins together. In the event of an internal fault, one or more of the channels is configured to pull the bussed $\overline{\text{FAULT}}n$ pins low. The other channels are then configured to shut down when the $\overline{\text{FAULT}}n$ pins are pulled low. For autonomous group retry, the faulted channel is configured to let go of the $\overline{\text{FAULT}}n$ pin(s) after a retry interval, assuming the original fault has cleared. All the channels in the group then begin a soft-start sequence. If the fault response is LATCH_OFF, the $\overline{\text{FAULT}}n$ pin remains asserted low until either the RUN pin is toggled OFF/ON or the part is commanded OFF/ON. The toggling of the RUN either by the pin or OFF/ON command will clear faults associated with the channel. If it is desired to have all faults cleared when either RUN pin is toggled or, set bit 0 of MFR_CONFIG_ALL to a 1.

The status of all faults and warnings is summarized in the STATUS_WORD and STATUS_BYTE commands.

Additional fault detection and handling capabilities are:

Power Good Pins

The PGOOD*n* pins of the LTC7132 are connected to the open drains of internal MOSFETs. The MOSFETs turn on and pull the PGOOD*n* pins low when the channel output voltage is not within the channel's UV and OV voltage thresholds. During TON_DELAY and TON_RISE sequencing, the PGOOD*n* pin is held low. The PGOOD*n* pin is also pulled low when the respective RUN*n* pin is low. The PGOOD*n* pin response is deglitched by an internal 60µs digital filter. The PGOOD*n* pin and PGOOD status may be different at times due to communication latency of up to 10µs.

CRC Protection

The integrity of the NVM memory is checked after a power on reset. A CRC error will prevent the controller from leaving the inactive state. If a CRC error occurs, the CML bit is set in the STATUS_BYTE and STATUS_WORD commands, the appropriate bit is set in the STATUS_MFR_SPECIFIC command, and the $\overline{\text{ALERT}}$ pin will be pulled low. NVM repair can be attempted by writing the desired configuration to the controller and executing a STORE_USER_ALL command followed by a CLEAR_FAULTS command.

The LTC7132 manufacturing section of the NVM is mirrored. If both copies are corrupted, the "NVM CRC Fault" in the STATUS_MFR_SPECIFIC command is set. If this bit remains set after being cleared by issuing a CLEAR_FAULTS or writing a 1 to this bit, an irrecoverable internal fault has occurred. The user is cautioned to disable both output power supply rails associated with this specific part. There are no provisions for field repair of NVM faults in the manufacturing section.

SERIAL INTERFACE

The LTC7132 serial interface is a PMBus compliant slave device and can operate at any frequency between

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10kHz and 400kHz. The address is configurable using either the NVM or an external resistor divider. In addition the LTC7132 always responds to the global broadcast address of 0x5A (7 bit) or 0x5B (7 bit).

The serial interface supports the following protocols defined in the PMBus specifications: 1) send command, 2) write byte, 3) write word, 4) group, 5) read byte, 6) read word and 7) read block. 8) write block. All read operations will return a valid PEC if the PMBus master requests it. If the PEC_REQUIRED bit is set in the MFR_CONFIG_ALL command, the PMBus write operations will not be acted upon until a valid PEC has been received by the LTC7132.

Communication Protection

PEC write errors (if PEC_REQUIRED is active), attempts to access unsupported commands, or writing invalid data to supported commands will result in a CML fault. The CML bit is set in the STATUS_BYTE and STATUS_WORD commands, the appropriate bit is set in the STATUS_CML command, and the $\overline{\text{ALERT}}$ pin is pulled low.

DEVICE ADDRESSING

The LTC7132 offers five different types of addressing over the PMBus interface, specifically: 1) global, 2) device, 3) rail addressing and 4) alert response address (ARA).

Global addressing provides a means of the PMBus master to address all LTC7132 devices on the bus. The LTC7132 global address is fixed 0x5A (7 bit) or 0xB4 (8 bit) and cannot be disabled. Commands sent to the global address act the same as if PAGE is set to a value of 0xFF. Commands sent are written to both channels simultaneously. Global command 0x5B (7 bit) or 0xB6 (8 bit) is paged and allows channel specific command of all LTC7132 devices on the bus. Other ADI device types may respond at one or both of these global addresses. Reading from global addresses is strongly discouraged.

Device addressing provides the standard means of the PMBus master communicating with a single instance of an LTC7132. The value of the device address is set by a combination of the ASEL0 and ASEL1 configuration pins and the MFR_ ADDRESS command. When this addressing means is used, the PAGE command determines the channel being acted upon. Device addressing can be disabled by writing a value of 0x80 to the MFR_ADDRESS.

Rail addressing provides a means for the bus master to simultaneously communicate with all channels connected together to produce a single output voltage (PolyPhase). While similar to global addressing, the rail address can be dynamically assigned with the paged MFR_RAIL_ ADDRESS command, allowing for any logical grouping of channels that might be required for reliable system control. Reading from rail addresses is also strongly discouraged.

All four means of PMBus addressing require the user to employ disciplined planning to avoid addressing conflicts. Communication to LTC7132 devices at global and rail addresses should be limited to command write operations.

RESPONSES TO V_{OUT} and I_{IN}/I_{OUT} FAULTS

V_{OUT} OV and UV conditions are monitored by comparators. The OV and UV limits are set in three ways.

- As a Percentage of the V_{OUT} if Using the Resistor Configuration Pins
- In NVM if Either Programmed at the Factory or Through the GUI
- By PMBus Command

The I_{IN} and I_{OUT} overcurrent monitors are performed by ADC readings and calculations. Thus these values are based on average currents and can have a time latency of up to $t_{CONVERT}$. The I_{OUT} calculation accounts for the DCR or sense resistor and their temperature coefficient. The input current is equal to the voltage measured across the R_{IINSNS} resistor divided by the resistors value as set with the MFR_IIN_CAL_GAIN command. If this calculated input current exceeds the IN_OC_WARN_LIMIT the $\overline{\text{ALERT}}$ pin is pulled low and the IIN_OC_WARN bit is asserted in the STATUS_INPUT command.

The digital processor within the LTC7132 provides the ability to ignore the fault, shut down and latch off or shut down and retry indefinitely (hiccup). The retry interval is set in MFR_RETRY_ DELAY and can be from 120ms

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to 83.88 seconds in 1ms increments. The shutdown for OV/UV and OC can be done immediately or after a user selectable deglitch time.

Output Overvoltage Fault Response

A programmable overvoltage comparator (OV) guards against transient overshoots as well as long-term overvoltages at the output. In such cases, the top MOSFET is turned off and the bottom MOSFET is turned on. However, the reverse output current is monitored while device is in OV fault. When it reaches the limit, both top and bottom MOSFETs are turned off. The top and bottom MOSFETs will keep their state until the overvoltage condition is cleared regardless of the PMBus VOUT_OV_FAULT_RESPONSE command byte value. This hardware level fault response delay is typically 2µs from the overvoltage condition to BG asserted high. Using the VOUT_OV_FAULT_RESPONSE command, the user can select any of the following behaviors:

- OV Pull-Down Only (OV Cannot Be Ignored)
- Shut Down (Stop Switching) Immediately—Latch Off
- Shut Down Immediately—Retry Indefinitely at the Time Interval Specified in MFR_RETRY_DELAY

Either the Latch Off or Retry fault responses can be deglitched in increments of (0-7) • 10µs. See Table 7.

Output Undervoltage Response

The response to an undervoltage comparator output can be the following:

- Ignore
- Shut Down Immediately—Latch Off
- Shut Down Immediately—Retry Indefinitely at the Time Interval Specified in MFR_RETRY_DELAY.

The UV responses can be deglitched. See Table 8.

Peak Output Overcurrent Fault Response

Due to the current mode control algorithm, peak output current across the inductor is always limited on a cycle-by-cycle basis. The value of the peak current limit is specified in sense voltage in the EC table. The current limit circuit operates by limiting the I_{TH} maximum voltage. If DCR sensing is used, the I_{TH} maximum voltage has a temperature dependency directly proportional to the TC of the DCR of the inductor. The LTC7132 automatically monitors the external temperature sensors and modifies the maximum allowed I_{TH} to compensate for this term.

The overcurrent fault processing circuitry can execute the following behaviors:

- Current Limit Indefinitely
- Shut Down Immediately—Latch Off
- Shut Down Immediately—Retry Indefinitely at the Time Interval Specified in MFR_RETRY_DELAY.

The overcurrent responses can be deglitched in increments of (0-7) • 16ms. See Table 9.

RESPONSES TO TIMING FAULTS

TON_MAX_FAULT_LIMIT is the time allowed for V_{OUT} to rise and settle at start-up. The TON_MAX_FAULT_LIMIT condition is predicated upon detection of the VOUT_UV_FAULT_LIMIT as the output is undergoing a SOFT_START sequence. The TON_MAX_ FAULT_LIMIT time is started after TON_DELAY has been reached and a SOFT_START sequence is started. The resolution of the TON_MAX_FAULT_LIMIT is 10µs. If the VOUT_UV_FAULT _LIMIT is not reached within the TON_MAX_FAULT_LIMIT time, the response of this fault is determined by the value of the TON_MAX_FAULT_RESPONSE command value. This response may be one of the following:

- Ignore
- Shut Down (Stop Switching) Immediately—Latch Off
- Shut Down Immediately—Retry Indefinitely at the Time Interval Specified in MFR_RETRY_DELAY.

This fault response is not deglitched. A value of 0 in TON_MAX_FAULT_LIMIT means the fault is ignored. The TON_MAX_FAULT_LIMIT should be set longer than the TON_RISE time. It is recommended TON_MAX_FAULT_LIMIT always be set to a non-zero value, otherwise the output may never come up and no flag will be set to the user. See Table 11.

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RESPONSES TO V_{IN} OV FAULTS

V_{IN} overvoltage is measured with the ADC. The response is naturally deglitched by the 90ms typical response time of the ADC. The fault responses are:

- Ignore
- Shut Down Immediately—Latch Off
- Shut Down Immediately—Retry Indefinitely at the Time Interval Specified in MFR_RETRY_DELAY. See Table 11.

RESPONSES TO OT/UT FAULTS

Internal Overtemperature Fault Response

An internal temperature sensor protects against NVM damage. Above 85°C, no writes to NVM are recommended. Above 130°C, the internal overtemperature warn threshold is exceeded and the part disables the NVM and does not re-enable until the temperature has dropped to 125°C. When the die temperature exceed 160°C the internal temperature fault response is enabled and the PWM is disabled until the die temperature drops below 150°C. Temperature is measured by the ADC. Internal temperature faults cannot be ignored. Internal temperature limits cannot be adjusted by the user. See Table 10.

External Overtemperature and Undertemperature Fault Response

Two external temperature sensors can be used to sense the temperature of critical circuit elements like inductors and power MOSFETs. The OT_FAULT_ RESPONSE and UT_FAULT_ RESPOSE commands are used to determine the appropriate response to an overtemperature and under temperature condition, respectively. If no external sense elements are used (not recommended) set the UT_FAULT_RESPONSE to ignore and set the UT_FAULT_ LIMIT to –275°C. The fault responses are:

- Ignore
- Shut Down Immediately—Latch Off
- Shut Down Immediately—Retry Indefinitely at the Time Interval Specified in MFR_RETRY_DELAY. See Table 9.

RESPONSES TO INPUT OVERCURRENT AND OUTPUT UNDERCURRENT FAULTS

Input overcurrent and output undercurrent are measured with the ADC. The fault responses are:

- Ignore
- Shut Down Immediately—Latch Off
- Shut Down Immediately—Retry Indefinitely at the Time Interval Specified in MFR_RETRY_DELAY

See Table 11.

RESPONSES TO EXTERNAL FAULTS

When either $\overline{\text{FAULT}}n$ pin is pulled low, the OTHER bit is set in the STATUS_WORD command, the appropriate bit is set in the STATUS_MFR_SPECIFIC command, and the $\overline{\text{ALERT}}$ pin is pulled low. Responses are not deglitched. Each channel can be configured to ignore or shut down then retry in response to its $\overline{\text{FAULT}}n$ pin going low by modifying the MFR_FAULT_RESPONSE command. To avoid the $\overline{\text{ALERT}}$ pin asserting low when $\overline{\text{FAULT}}$ is pulled low, assert bit 1 of MFR_CHAN_CONFIG, or mask the $\overline{\text{ALERT}}$ using the SMBALERT_MASK command.

FAULT LOGGING

The LTC7132 has fault logging capability. Data is logged into memory in the order shown in Table 13. The data is stored in a continuously updated buffer in RAM. When a fault event occurs, the fault log buffer is copied from the RAM buffer into NVM. Fault logging is allowed at temperatures above 85°C; however, retention of 10 years is not guaranteed. When the die temperature exceeds 130°C the fault logging is delayed until the die temperature drops below 125°C. The fault log data remains in NVM until a MFR_FAULT _LOG_CLEAR command is issued. Issuing this command re-enables the fault log feature. Before re-enabling fault log, be sure no faults are present and a CLEAR_FAULTS command has been issued.

When the LTC7132 powers-up or exits its reset state, it checks the NVM for a valid fault log. If a valid fault log exists in NVM, the “Valid Fault Log” bit in the

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STATUS_MFR_SPECIFIC command will be set and an $\overline{\text{ALERT}}$ event will be generated. Also, fault logging will be blocked until the LTC7132 has received a MFR_FAULT_LOG_CLEAR command before fault logging will be re-enabled.

The information is stored in EEPROM in the event of any fault that disables the controller on either channel. A $\overline{\text{FAULT}}$*n* being externally pulled low will not trigger a fault logging event.

BUS TIMEOUT PROTECTION

The LTC7132 implements a timeout feature to avoid persistent faults on the serial interface. The data packet timer begins at the first START event before the device address write byte. Data packet information must be completed within 30ms or the LTC7132 will three-state the bus and ignore the given data packet. If more time is required, assert bit 3 of MFR_CONFIG_ALL to allow typical bus timeouts of 255ms. Data packet information includes the device address byte write, command byte, repeat start event (if a read operation), device address byte read (if a read operation), all data bytes and the PEC byte if applicable.

The LTC7132 allows longer PMBus timeouts for block read data packets. This timeout is proportional to the length of the block read. The additional block read timeout applies primarily to the MFR_FAULT_LOG command. The timeout period defaults to 32ms.

The user is encouraged to use as high a clock rate as possible to maintain efficient data packet transfer between all devices sharing the serial bus interface. The LTC7132 supports the full PMBus frequency range from 10kHz to 400kHz.

SIMILARITY BETWEEN PMBus, SMBus AND I²C 2-WIRE INTERFACE

The PMBus 2-wire interface is an incremental extension of the SMBus. SMBus is built upon I²C with some minor differences in timing, DC parameters and protocol. The PMBus/SMBus protocols are more robust than simple I²C byte commands because PMBus/SMBus provide timeouts to prevent persistent bus errors and optional packet error checking (PEC) to ensure data integrity. In general, a master device that can be configured for I²C communication can be used for PMBus communication with little or no change to hardware or firmware. Repeat start (restart) is not supported by all I²C controllers but is required for SMBus/PMBus reads. If a general purpose I²C controller is used, check that repeat start is supported.

The LTC7132 supports the maximum SMBus clock speed of 100kHz and is compatible with the higher speed PMBus specification (between 100kHz and 400kHz) if MFR_COMMON polling or clock stretching is enabled. For robust communication and operation refer to the Note section in the PMBus command summary. Clock stretching is enabled by asserting bit 1 of MFR_CONFIG_ALL.

For a description of the minor extensions and exceptions PMBus makes to SMBus, refer to PMBus Specification Part 1 Revision 1.2: Paragraph 5: Transport.

For a description of the differences between SMBus and I²C, refer to System Management Bus (SMBus) Specification Version 2.0: Appendix B—Differences Between SMBus and I²C.

PMBus SERIAL DIGITAL INTERFACE

The LTC7132 communicates with a host (master) using the standard PMBus serial bus interface. The Timing Diagram, Figure 7, shows the timing relationship of the signals on the bus. The two bus lines, SDA and SCL, must be high when the bus is not in use. External pull-up resistors or current sources are required on these lines. The LTC7132 is a slave device. The master can communicate with the LTC7132 using the following formats:

- Master Transmitter, Slave Receiver
- Master Receiver, Slave Transmitter

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The following PMBus protocols are supported:

- Write Byte, Write Word, Send Byte
- Read Byte, Read Word, Block Read, Block Write
- Alert Response Address

Figures 8-25 illustrate the aforementioned PMBus protocols. All transactions support PEC and GCP (group command protocol). The Block Read supports 255 bytes of returned data. For this reason, the PMBus timeout may be extended when reading the fault log.

Figure 8 is a key to the protocol diagrams in this section. PEC is optional.

A value shown below a field in the following figures is mandatory value for that field.

The data formats implemented by PMBus are:

- Master transmitter transmits to slave receiver. The transfer direction in this case is not changed.
- Master reads slave immediately after the first byte. At the moment of the first acknowledgment (provided by the slave receiver) the master transmitter becomes a master receiver and the slave receiver becomes a slave transmitter.
- Combined format. During a change of direction within a transfer, the master repeats both a start condition and the slave address but with the R/$\overline{W}$ bit reversed. In this case, the master receiver terminates the transfer by generating a NACK on the last byte of the transfer and a STOP condition.

Refer to Figure 8 for a legend.

Handshaking features are included to ensure robust system communication. Please refer to the PMBus Communication and Command Processing subsection of the Applications Information section for further details.

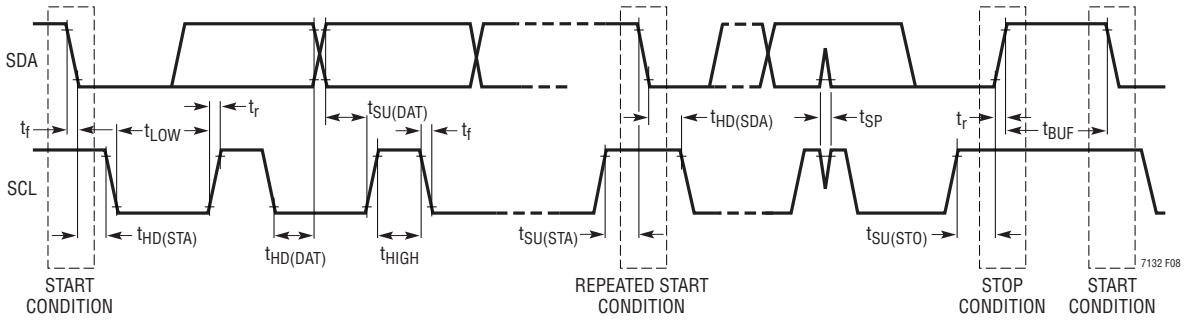

Figure 7. Timing Diagram

Table 1. Abbreviations of Supported Data Formats

	PMBus		ADI		
	TERMINOLOGY	SPECIFICATION REFERENCE	TERMINOLOGY	DEFINITION	EXAMPLE
L11	Linear	Part II ¶7.1	Linear_5s_1s	Floating point 16-bit data: value = Y • 2^N, where N = b[15:11] and Y = b[10:0], both two's compliment binary integers.	b[15:0] = 0x9807 = 10011_000_0000_0111 value = 7 • 2^{-13} = 854E-6
L16	Linear VOUT_MODE	Part II ¶8.2	Linear_16u	Floating point 16-bit data: value = Y • 2^{-12}, where Y = b[15:0], an unsigned integer.	b[15:0] = 0x4C00 = 0100_1100_0000_0000 value = 19456 • 2^{-12} = 4.75
CF	DIRECT	Part II ¶7.2	Varies	16-bit data with a custom format defined in the detailed PMBus command description.	Often an unsigned or two's compliment integer.
Reg	register bits	Part II ¶10.3	Reg	Per-bit meaning defined in detailed PMBus command description.	PMBus STATUS_BYTE command.
ASC	text characters	Part II ¶22.2.1	ASCII	ISO/IEC 8859-1 [A05]	LTC (0x4C5443)

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S	START CONDITION
Sr	REPEATED START CONDITION
Rd	READ (BIT VALUE OF 1)
Wr	WRITE (BIT VALUE OF 0)
A	ACKNOWLEDGE (THIS BIT POSITION MAY BE 0 FOR AN ACK OR 1 FOR A NACK)
P	STOP CONDITION
PEC	PACKET ERROR CODE
☐	MASTER TO SLAVE
▒	SLAVE TO MASTER
···	CONTINUATION OF PROTOCOL

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Figure 8. PMBus Packet Protocol Diagram Element Key

Figure 9. Quick Command Protocol

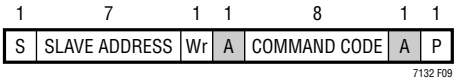

Figure 10. Send Byte Protocol

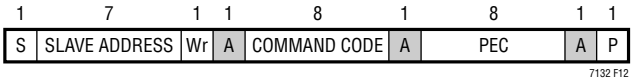

Figure 11. Send Byte Protocol with PEC

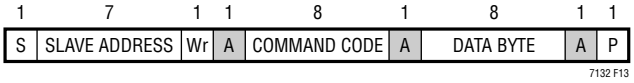

Figure 12. Write Byte Protocol

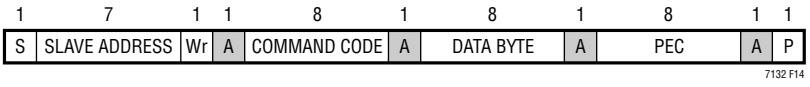

Figure 13. Write Byte Protocol with PEC

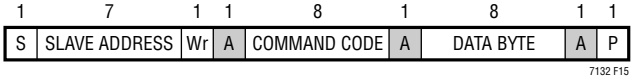

Figure 14. Write Word Protocol

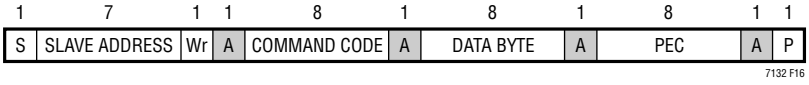

Figure 15. Write Word Protocol with PEC

OPERATION

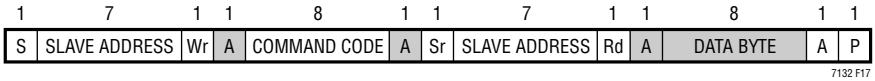

Figure 16. Read Byte Protocol

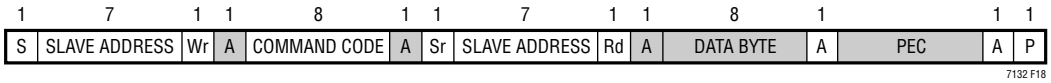

Figure 17. Read Byte Protocol with PEC

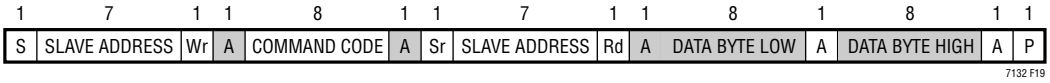

Figure 18. Read Word Protocol

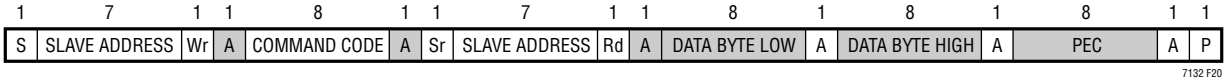

Figure 19. Read Word Protocol with PEC

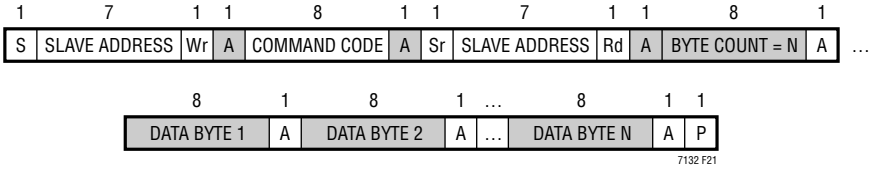

Figure 20. Block Read Protocol

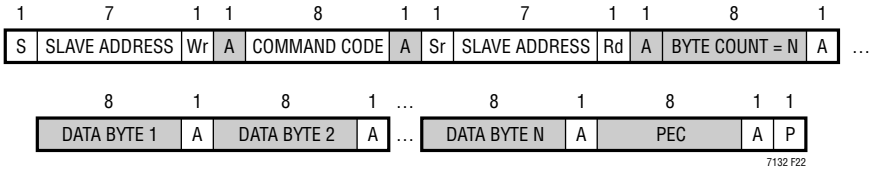

Figure 21. Block Read Protocol with PEC

OPERATION

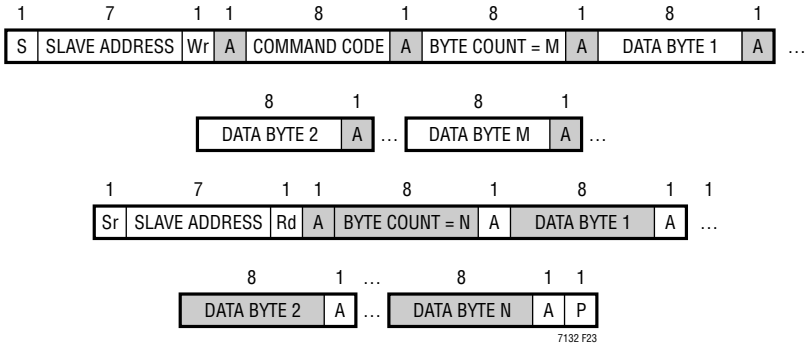

Figure 22. Block Write – Block Read Process Call

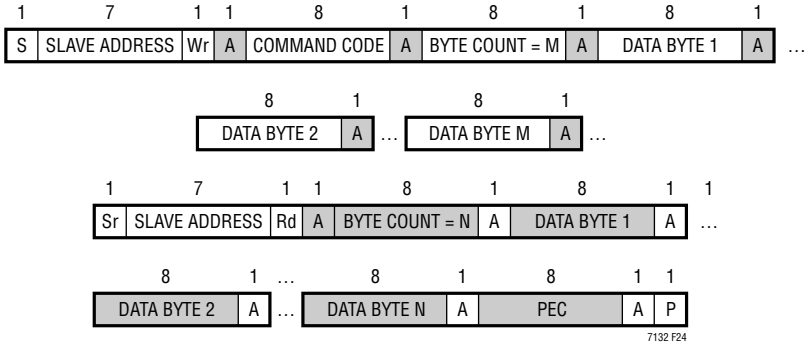

Figure 23. Block Write – Block Read Process Call with PEC

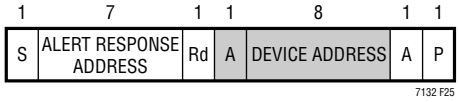

Figure 24. Alert Response Address Protocol

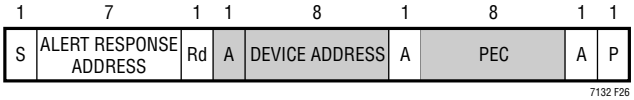

Figure 25. Alert Response Address Protocol with PEC

PMBus COMMAND SUMMARY

PMBus COMMANDS

The following tables list supported PMBus commands and manufacturer specific commands. A complete description of these commands can be found in the "PMBus Power System Mgt Protocol Specification – Part II – Revision 1.2". Users are encouraged to reference this specification. Exceptions or manufacturer specific implementations are listed below in Table 2. Floating point values listed in the "DEFAULT VALUE" column are either Linear 16-bit Signed (PMBus Section 8.3.1) or Linear_5s_11s (PMBus Section 7.1) format, whichever is appropriate for the command. All commands from 0xD0 through 0xFF not listed in this table are implicitly reserved by the manufacturer. Users should avoid blind writes within this range of commands to avoid undesired operation of the part. All commands from 0x00 through 0xCF not listed in this table are implicitly not supported by the manufacturer. Attempting to access non-supported or reserved commands may result in a CML command fault event. All output voltage settings and measurements are based on the VOUT_MODE setting of 0x14. This translates to an exponent of 2^{-12}.

If PMBus commands are received faster than they are being processed, the part may become too busy to handle new commands. In these circumstances the part follows the protocols defined in the PMBus Specification v1.2, Part II, Section 10.8.7, to communicate that it is busy. The part includes handshaking features to eliminate busy errors and simplify error handling software while ensuring robust communication and system behavior. Please refer to the subsection titled PMBus Communication and Command Processing in the Applications Information section for further details.

Table 2. Summary (Note: The Data Format abbreviations are detailed at the end of this table.)

COMMAND NAME	CMD CODE	DESCRIPTION	TYPE	PAGED	DATA FORMAT	UNITS	NVM	DEFAULT VALUE	PAGE
PAGE	0x00	Provides integration with multi-page PMBus devices.	R/W Byte	N	Reg			0x00	68
OPERATION	0x01	Operating mode control. On/off, margin high and margin low.	R/W Byte	Y	Reg		Y	0x80	72
ON_OFF_CONFIG	0x02	RUN pin and PMBus bus on/off command configuration.	R/W Byte	Y	Reg		Y	0x1E	72
CLEAR_FAULTS	0x03	Clear any fault bits that have been set.	Send Byte	N				NA	97
PAGE_PLUS_WRITE	0x05	Write a command directly to a specified page.	W Block	N					69
PAGE_PLUS_READ	0x06	Read a command directly from a specified page.	Block R/W	N					69
WRITE_PROTECT	0x10	Level of protection provided by the device against accidental changes.	R/W Byte	N	Reg		Y	0x00	69
STORE_USER_ALL	0x15	Store user operating memory to EEPROM.	Send Byte	N				NA	108
RESTORE_USER_ALL	0x16	Restore user operating memory from EEPROM.	Send Byte	N				NA	108
CAPABILITY	0x19	Summary of PMBus optional communication protocols supported by this device.	R Byte	N	Reg			0xB0	96
SMBALERT_MASK	0x1B	Mask $\overline{\text{ALERT}}$ activity	Block R/W	Y	Reg		Y	see CMD	97
VOUT_MODE	0x20	Output voltage format and exponent (2^{-12}).	R Byte	Y	Reg			2–12 0x14	77
VOUT_COMMAND	0x21	Nominal output voltage set point.	R/W Word	Y	L16	V	Y	1.0 0x1000	79
VOUT_MAX	0x24	Upper limit on the commanded output voltage including VOUT_MARGIN_HI.	R/W Word	Y	L16	V	Y	2.75 0x2C00	77
VOUT_MARGIN_HIGH	0x25	Margin high output voltage set point. Must be greater than VOUT_COMMAND.	R/W Word	Y	L16	V	Y	1.05 0x10CD	78
VOUT_MARGIN_LOW	0x26	Margin low output voltage set point. Must be less than VOUT_COMMAND.	R/W Word	Y	L16	V	Y	0.95 0x0F33	79

PMBus COMMAND SUMMARY

COMMAND NAME	CMD CODE	DESCRIPTION	TYPE	PAGED	DATA FORMAT	UNITS	NVM	DEFAULT VALUE	PAGE
VOUT_TRANSITION_ RATE	0X27	Rate the output changes when VOUT commanded to a new value.	R/W Word	Y	L11	V/ms	Y	0.25 0xAA00	85
FREQUENCY_SWITCH	0x33	Switching frequency of the controller.	R/W Word	N	L11	kHz	Y	425k 0xFB52	76
VIN_ON	0x35	Input voltage at which the unit should start power conversion.	R/W Word	N	L11	V	Y	6.5 0xCB40	76
VIN_OFF	0x36	Input voltage at which the unit should stop power conversion.	R/W Word	N	L11	V	Y	6.0 0xCB00	77
IOUT_CAL_GAIN	0x38	The ratio of the voltage at the current sense pins to the sensed current. For devices using a fixed current sense resistor, it is the resistance value in mΩ.	R/W Word	Y	L11	mΩ	Y	0.32 0xAA8F	80
VOUT_OV_FAULT_LIMIT	0x40	Output overvoltage fault limit.	R/W Word	Y	L16	V	Y	1.1 0x119A	78
VOUT_OV_FAULT_ RESPONSE	0x41	Action to be taken by the device when an output overvoltage fault is detected.	R/W Byte	Y	Reg		Y	0xB8	87
VOUT_OV_WARN_LIMIT	0x42	Output overvoltage warning limit.	R/W Word	Y	L16	V	Y	1.075 0x1133	78
VOUT_UV_WARN_LIMIT	0x43	Output undervoltage warning limit.	R/W Word	Y	L16	V	Y	0.925 0x0ECD	79
VOUT_UV_FAULT_LIMIT	0x44	Output undervoltage fault limit.	R/W Word	Y	L16	V	Y	0.9 0x0E66	79
VOUT_UV_FAULT_ RESPONSE	0x45	Action to be taken by the device when an output undervoltage fault is detected.	R/W Byte	Y	Reg		Y	0xB8	88
IOUT_OC_FAULT_LIMIT	0x46	Output overcurrent fault limit.	R/W Word	Y	L11	A	Y	45.0 0xE2D0	80
IOUT_OC_FAULT_ RESPONSE	0x47	Action to be taken by the device when an output overcurrent fault is detected.	R/W Byte	Y	Reg		Y	0x00	90
IOUT_OC_WARN_LIMIT	0x4A	Output overcurrent warning limit.	R/W Word	Y	L11	A	Y	35.0 0xE230	81
OT_FAULT_LIMIT	0x4F	External overtemperature fault limit.	R/W Word	Y	L11	C	Y	100.0 0xEB20	83
OT_FAULT_RESPONSE	0x50	Action to be taken by the device when an external overtemperature fault is detected,	R/W Byte	Y	Reg		Y	0xB8	92
OT_WARN_LIMIT	0x51	External overtemperature warning limit.	R/W Word	Y	L11	C	Y	85.0 0xEAA8	83
UT_FAULT_LIMIT	0x53	External undertemperature fault limit.	R/W Word	Y	L11	C	Y	–40.0 0xE580	84
UT_FAULT_RESPONSE	0x54	Action to be taken by the device when an external undertemperature fault is detected.	R/W Byte	Y	Reg		Y	0xB8	92
VIN_OV_FAULT_LIMIT	0x55	Input supply overvoltage fault limit.	R/W Word	N	L11	V	Y	15.5 0xD3E0	76
VIN_OV_FAULT_ RESPONSE	0x56	Action to be taken by the device when an input overvoltage fault is detected.	R/W Byte	Y	Reg		Y	0x80	87
VIN_UV_WARN_LIMIT	0x58	Input supply undervoltage warning limit.	R/W Word	N	L11	V	Y	6.3 0xCB26	76
IIN_OC_WARN_LIMIT	0x5D	Input supply overcurrent warning limit.	R/W Word	N	L11	A	Y	10.0 0xD280	82
TON_DELAY	0x60	Time from RUN and/or Operation on to output rail turn-on.	R/W Word	Y	L11	ms	Y	0.0 0x8000	84

PMBus COMMAND SUMMARY

COMMAND NAME	CMD CODE	DESCRIPTION	TYPE	PAGED	DATA FORMAT	UNITS	NVM	DEFAULT VALUE	PAGE
TON_RISE	0x61	Time from when the output starts to rise until the output voltage reaches the VOUT commanded value.	R/W Word	Y	L11	ms	Y	8.0 0xD200	84
TON_MAX_FAULT_LIMIT	0x62	Maximum time from the start of TON_RISE for VOUT to cross the VOUT_UV_FAULT_LIMIT.	R/W Word	Y	L11	ms	Y	10.00 0xD280	85
TON_MAX_FAULT_ RESPONSE	0x63	Action to be taken by the device when a TON_ MAX_FAULT event is detected.	R/W Byte	Y	Reg		Y	0xB8	90
TOFF_DELAY	0x64	Time from RUN and/or Operation off to the start of TOFF_FALL ramp.	R/W Word	Y	L11	ms	Y	0.0 0x8000	85
TOFF_FALL	0x65	Time from when the output starts to fall until the output reaches zero volts.	R/W Word	Y	L11	ms	Y	8.00 0xD200	85
TOFF_MAX_WARN_LIMIT	0x66	Maximum allowed time, after TOFF_FALL completed, for the unit to decay below 12.5%.	R/W Word	Y	L11	ms	Y	150.0 0xF258	86
STATUS_BYTE	0x78	One byte summary of the unit's fault condition.	R/W Byte	Y	Reg			NA	98
STATUS_WORD	0x79	Two byte summary of the unit's fault condition.	R/W Word	Y	Reg			NA	99
STATUS_VOUT	0x7A	Output voltage fault and warning status.	R/W Byte	Y	Reg			NA	99
STATUS_IOUT	0x7B	Output current fault and warning status.	R/W Byte	Y	Reg			NA	100
STATUS_INPUT	0x7C	Input supply fault and warning status.	R/W Byte	N	Reg			NA	100
STATUS_TEMPERATURE	0x7D	External temperature fault and warning status for READ_TEMPERATURE_1.	R/W Byte	Y	Reg			NA	101
STATUS_CML	0x7E	Communication and memory fault and warning status.	R/W Byte	N	Reg			NA	101
STATUS_MFR_SPECIFIC	0x80	Manufacturer specific fault and state information.	R/W Byte	Y	Reg			NA	102
READ_VIN	0x88	Measured input supply voltage.	R Word	N	L11	V		NA	104
READ_IIN	0x89	Measured input supply current.	R Word	N	L11	A		NA	104
READ_VOUT	0x8B	Measured output voltage.	R Word	Y	L16	V		NA	104
READ_IOUT	0x8C	Measured output current.	R Word	Y	L11	A		NA	105
READ_TEMPERATURE_1	0x8D	External temperature sensor temperature. This is the value used for all temperature related processing, including IOUT_CAL_GAIN.	R Word	Y	L11	C		NA	105
READ_TEMPERATURE_2	0x8E	Internal die junction temperature. Does not affect any other commands.	R Word	N	L11	C		NA	105
READ_FREQUENCY	0x95	Measured PWM switching frequency.	R Word	Y	L11	Hz		NA	105
READ_POUT	0x96	Measured output power	R Word	Y	L11	W		N/A	105
READ_PIN	0x97	Calculated input power	R Word	Y	L11	W		N/A	105
PMBus_REVISION	0x98	PMBus revision supported by this device. Current revision is 1.2.	R Byte	N	Reg			0x22	96
MFR_ID	0x99	The manufacturer ID of the LTC7132 in ASCII.	R String	N	ASC			LTC	96
MFR_MODEL	0x9A	Manufacturer part number in ASCII.	R String	N	ASC			LTC7132	96
MFR_VOUT_MAX	0xA5	Maximum allowed output voltage including VOUT_OV_FAULT_LIMIT.	R Word	Y	L16	V		5.7 0x5B33	79
MFR_PIN_ACCURACY	0xAC	Returns the accuracy of the READ_PIN command	R Byte	N		%		5.0%	105

PMBus COMMAND SUMMARY

COMMAND NAME	CMD CODE	DESCRIPTION	TYPE	PAGED	DATA FORMAT	UNITS	NVM	DEFAULT VALUE	PAGE
USER_DATA_00	0xB0	OEM RESERVED. Typically used for part serialization.	R/W Word	N	Reg		Y	NA	95
USER_DATA_01	0xB1	Manufacturer reserved for LTpowerPlay.	R/W Word	Y	Reg		Y	NA	95
USER_DATA_02	0xB2	OEM RESERVED. Typically used for part serialization	R/W Word	N	Reg		Y	NA	95
USER_DATA_03	0xB3	An NVM word available for the user.	R/W Word	Y	Reg		Y	0x0000	95
USER_DATA_04	0xB4	An NVM word available for the user.	R/W Word	N	Reg		Y	0x0000	95
MFR_INFO	0xB6	Manufacturer specific information	R/W Word	N	Reg			NA	103
MFR_EE_UNLOCK	0xBD	Contact factory.							112
MFR_EE_ERASE	0xBE	Contact factory.							112
MFR_EE_DATA	0xBF	Contact factory.							112
MFR_CHAN_CONFIG	0xD0	Configuration bits that are channel specific.	R/W Byte	Y	Reg		Y	0x1D	70
MFR_CONFIG_ALL	0xD1	General configuration bits.	R/W Byte	N	Reg		Y	0x21	71
MFR_FAULT_PROPAGATE	0xD2	Configuration that determines which faults are propagated to the FAULT pin.	R/W Word	Y	Reg		Y	0x6993	93
MFR_PWM_COMP	0xD3	PWM loop compensation configuration	R/W Byte	Y	Reg		Y	0xAE	74
MFR_PWM_MODE	0xD4	Configuration for the PWM engine.	R/W Byte	Y	Reg		Y	0xC7	73
MFR_FAULT_RESPONSE	0xD5	Action to be taken by the device when the FAULT pin is externally asserted low.	R/W Byte	Y	Reg		Y	0xC0	95
MFR_OT_FAULT_RESPONSE	0xD6	Action to be taken by the device when an internal overtemperature fault is detected.	R Byte	N	Reg			0xC0	91
MFR_IOUT_PEAK	0xD7	Report the maximum measured value of READ_IOUT since last MFR_CLEAR_PEAKS.	R Word	Y	L11	A		NA	105
MFR_ADC_CONTROL	0xD8	ADC telemetry parameter selected for repeated fast ADC read back	R/W Byte	N	Reg			0x00	106
MFR_RETRY_DELAY	0xDB	Retry interval during FAULT retry mode.	R/W Word	Y	L11	ms	Y	350.0 0xFABC	86
MFR_RESTART_DELAY	0xDC	Minimum time the RUN pin is held low by the LTC7132.	R/W Word	Y	L11	ms	Y	500.0 0xFBE8	86
MFR_VOUT_PEAK	0xDD	Maximum measured value of READ_VOUT since last MFR_CLEAR_PEAKS.	R Word	Y	L16	V		NA	106
MFR_VIN_PEAK	0xDE	Maximum measured value of READ_VIN since last MFR_CLEAR_PEAKS.	R Word	N	L11	V		NA	106
MFR_TEMPERATURE_1_PEAK	0xDF	Maximum measured value of external Temperature (READ_TEMPERATURE_1) since last MFR_CLEAR_PEAKS.	R Word	Y	L11	C		NA	106
MFR_READ_IIN_PEAK	0xE1	Maximum measured value of READ_IIN command since last MFR_CLEAR_PEAKS	R Word	N	L11	A		NA	106
MFR_CLEAR_PEAKS	0xE3	Clears all peak values.	Send Byte	N				NA	98
MFR_READ_ICHIP	0xE4	Measured supply current of the LTC7132	R Word	N	L11	A		NA	106
MFR_PADS	0xE5	Digital status of the I/O pads.	R Word	N	Reg			NA	102
MFR_ADDRESS	0xE6	Sets the 7-bit I^2C address byte.	R/W Byte	N	Reg		Y	0x4F	70
MFR_SPECIAL_ID	0xE7	Manufacturer code representing the LTC7132 and revision	R Word	N	Reg			0x4C0X 0x4CEX	96

PMBus COMMAND SUMMARY

COMMAND NAME	CMD CODE	DESCRIPTION	TYPE	PAGED	DATA FORMAT	UNITS	NVM	DEFAULT VALUE	PAGE
MFR_IIN_CAL_GAIN	0xE8	The resistance value of the input current sense element in mΩ.	R/W Word	N	L11	mΩ	Y	5.0 0xCA80	82
MFR_FAULT_LOG_STORE	0xEA	Command a transfer of the fault log from RAM to EEPROM.	Send Byte	N				NA	109
MFR_FAULT_LOG_CLEAR	0xEC	Initialize the EEPROM block reserved for fault logging.	Send Byte	N				NA	112
MFR_FAULT_LOG	0xEE	Fault log data bytes.	R Block	N	Reg		Y	NA	109
MFR_COMMON	0xEF	Manufacturer status bits that are common across multiple ADI chips.	R Byte	N	Reg			NA	103
MFR_COMPARE_USER_ALL	0xF0	Compares current command contents with NVM.	Send Byte	N				NA	108
MFR_TEMPERATURE_2_PEAK	0xF4	Peak internal die temperature since last MFR_CLEAR_PEAKS.	R Word	N	L11	C		NA	106
MFR_PWM_CONFIG	0xF5	Set numerous parameters for the DC/DC controller including phasing.	R/W Byte	N	Reg		Y	0x10	75
MFR_IOUT_CAL_GAIN_TC	0xF6	Temperature coefficient of the current sensing element.	R/W Word	Y	CF	ppm/°C	Y	3900 0x0F3C	80
MFR_RVIN	0xF7	The resistance value of the VIN pin filter element in mΩ.	R/W Word	N	L11	mΩ	Y	1000 0x03E8	77
MFR_TEMP_1_GAIN	0xF8	Sets the slope of the external temperature sensor.	R/W Word	Y	CF		Y	1.0 0x4000	83
MFR_TEMP_1_OFFSET	0xF9	Sets the offset of the external temperature sensor with respect to –273.1°C	R/W Word	Y	L11	C	Y	0.0 0x8000	83
MFR_RAIL_ADDRESS	0xFA	Common address for PolyPhase outputs to adjust common parameters.	R/W Byte	Y	Reg		Y	0x80	70
MFR_REAL_TIME	0xFB	48-bit share-clock counter value.	R Block	N	CF			NA	107
MFR_RESET	0xFD	Commanded reset without requiring a power down.	Send Byte	N				NA	72

Note 1: Commands indicated with Y in the NVM column indicate that these commands are stored and restored using the STORE_USER_ALL and RESTORE_USER_ALL commands, respectively.

Note 2: Commands with a default value of NA indicate “not applicable”. Commands with a default value of FS indicate “factory set on a per part basis”.

Note 3: The LTC7132 contains additional commands not listed in this table. Reading these commands is harmless to the operation of the IC; however, the contents and meaning of these commands can change without notice.

Note 4: Some of the unpublished commands are read-only and will generate a CML bit 6 fault if written.

Note 5: Writing to commands not published in this table is not permitted.

Note 6: The user should not assume compatibility of commands between different parts based upon command names. Always refer to the manufacturer’s data sheet for each part for a complete definition of a command’s function.

ADI strives to keep command functionality compatible between all ADI devices. Differences may occur to address specific product requirements.

PMBus COMMAND SUMMARY

*DATA FORMAT

L11	Linear_5s_11s	PMBus data field b[15:0] Value = $Y \cdot 2^N$ where N = b[15:11] is a 5-bit two's complement integer and Y = b[10:0] is an 11-bit two's complement integer Example: For b[15:0] = 0x9807 = 'b10011_000_0000_0111 Value = $7 \cdot 2^{-13} = 854 \cdot 10^{-6}$ From "PMBus Spec Part II: Paragraph 7.1"
L16	Linear_16u	PMBus data field b[15:0] Value = $Y \cdot 2^N$ where Y = b[15:0] is an unsigned integer and N = Vout_mode_parameter is a 5-bit two's complement exponent that is hardwired to –12 decimal Example: For b[15:0] = 0x9800 = 'b1001_1000_0000_0000 Value = $19456 \cdot 2^{-12} = 4.75$ From "PMBus Spec Part II: Paragraph 8.2"
Reg	Register	PMBus data field b[15:0] or b[7:0]. Bit field meaning is defined in detailed PMBus Command Description.
I16	Integer Word	PMBus data field b[15:0] Value = Y where Y = b[15:0] is a 16 bit unsigned integer Example: For b[15:0] = 0x9807 = 'b1001_1000_0000_0111 Value = 38919 (decimal)
CF	Custom Format	Value is defined in detailed PMBus Command Description. This is often an unsigned or two's complement integer scaled by an MFR specific constant.
ASC	ASCII Format	A variable length string of text characters conforming to ISO/IEC 8859-1 standard.

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The Typical Application on the back page is a common LTC7132 application circuit. The LTC7132 is mainly designed for low DCR application via PMBus command MFR_PWM_MODE[2] = 1 applicable when 0 ≤ V_{OUT} ≤ 3.5V, but it can be also configured to be regular DCR or regular resistor sensing by setting MFR_PWM_MODE[2] = 0 for 0≤ V_{OUT} ≤ 5.5V. The choice among them is largely a design trade-off between cost, power consumption and accuracy. DCR sensing is becoming popular because it saves expensive current sensing resistors and is more power efficient, especially in high current applications. Low DCR provides the most power efficient solution, and best signal-to-noise ratio of the input sensing voltage. The accuracy of the current reading and current limit are typically limited by the accuracy of the DCR resistor (accounted for in the IOUT_CAL_GAIN parameter of the LTC7132). Thus current sensing resistors provide the most accurate current sensing and limiting for the application. Other external component selection is driven by the load requirement, and begins with the selection of R_{SENSE} (if R_{SENSE} is used) and inductor value. Then the input and output capacitors are selected. To have a stable loop performance and reliability, the loop compensation parameters such as GM of error amplifier programmed by MFR_PWM_ COMP[7:5] and RTH by MFR_PWM_ COMP[4:0] together with current limit range, set by bit[7] of MFR_PWM_MODE and voltage range set by bit[1] of MFR_ PWM_MODE have to be properly selected. All other programmable parameters do not affect the loop gain, allowing parameters to be modified without impacting the transient response to load changes.

CURRENT LIMIT PROGRAMMING

The cycle-by-cycle current limit threshold voltage, V_{ILIMIT}, across the I_{SENSE}+/I_{SENSE}– pins is proportional to V_{ITH}. The V_{ITH} limit can be programmed from 1.45 to 2.2V using the PMBUS command IOUT_OC_FAULT_ LIMIT. See Figure 26. The LTC7132 has four ranges of current limit programming. Properly setting the value of MFR_PWM_MODE[2] and MFR_PWM_MODE[7], and IOUT_OC_FAULT_LIMIT, see the section of the PMBus commands, the device can regulate output voltage with the peak current under the value of IOUT_OC_FAULT_ LIMIT in normal operation. In case of output current exceeding that current limit, an OC fault will be issued. Each range in Figure 26 affects the loop gain, and subsequently effects the loop stability, so setting range of current limiting is a part of loop design.

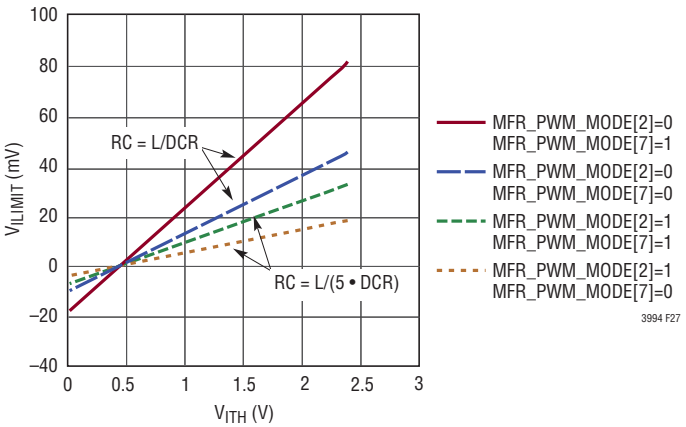

Figure 26. V_{ITH} vs V_{ILIMIT}

The LTC7132 will account for the DCR of the inductor if the device is configured for DCR sensing and automatically update the current limit as the inductor temperature changes. The temperature coefficient of the DCR is stored in the MFR_IOUT_CAL_GAIN_TC register. The setting MFR_PWM_MODE[2] = 1, MFR_PWM_MODE[7] = 0, allows for the use of very low DCR inductors or sense resistors, the peak output current is up to 16.5mV/DCR, the application LTC7132 is mainly designed for. Keep in mind this operation is based on a cycle-by-cycle basis and is only a function of the peak inductor current. The average inductor current is monitored by the ADC converter and can provide a warning if too much average output current is detected. The overcurrent fault is detected when the I_{TH} voltage hits the maximum value. The digital processor within the LTC7132 provides the ability to either ignore the fault, shut down and latch off or shut down and retry indefinitely (hiccup). Refer to the overcurrent portion of the Operation section for more detail.

$I_{SENSE0}^{\pm}$ AND $I_{SENSE1}^{\pm}$ PINS

The I_{SENSE}^{+} and I_{SENSE}^{-} pins are the inputs to the current comparator and the A/D. The common mode input voltage range of the current comparators is 0V to 5.5V. Both the SENSE pins are high impedance inputs with small input currents typically less than 1µA. The high impedance

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inputs to the current comparators enable accurate DCR sensing. Do not float these pins during normal operation.

Filter components connected to the $I_{SENSE}^{\pm}$ traces should be placed close to the IC. The positive and negative traces should be routed differentially and Kelvin connected to the current sense element; see Figure 27. A non-Kelvin connection or improper placement can add parasitic inductance and capacitance to the current sense element, degrading the signal at the sense terminals and making the programmed current limit perform poorly. In a PolyPhase system, poor placement of the sensing element will result in sub-optimal current sharing between power stages. If DCR sensing is used (Figure 28a), sense resistor R1 should be placed close to the inductor to prevent noise from coupling into sensitive small-signal nodes. The capacitor C1 should be placed close to the IC pins. Any impedance difference between the I_{SENSE}^{+} and I_{SENSE}^{-} signal paths can result in loss of accuracy in the current reading of the ADC. The current reading accuracy can be improved by matching the impedance of the two signal paths. To accomplish this add a series resistor R3 between V_{OUT} and I_{SENSE}^{-} equal to R1. A capacitor of 1µF or greater should be placed in parallel with this resistor.

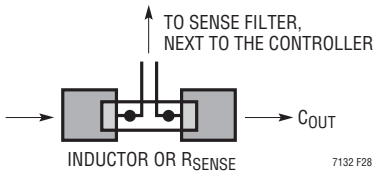

Figure 27. Sense Lines Placement with Inductor DCR

Inductor DCR Sensing

The DCR is the DC winding resistance of the inductor's copper, which is often less than 1mΩ for high current inductors. In high current and low output voltage applications, a conduction loss of a high DCR or a sense resistor will cause a significant reduction in power efficiency. For a specific output requirement, choose the inductor with the DCR that satisfies the maximum desirable sense voltage, and uses the relationship of the sense pin filters to output inductor characteristics as depicted in the following:

$$DCR = \frac{V_{SENSE(MAX)}}{I_{MAX} + \frac{\Delta I_L}{2}}$$

The RC sense filter time constant must be set by the following equations:

RC = L/(5 • DCR) at MFR_PWM_MODE[2] = 1 for low DCR

RC = L/DCR at MFR_PWM_MODE[2] = 0 for normal DCR

where:

$V_{SENSE(MAX)}$: Maximum sense voltage for a given I_{TH} voltage

I_{MAX}: Maximum load current

ΔI_L: Inductor ripple current

DCR: Inductor resistance

RC: Filter time constant

During normal DCR sensing, the voltage ripple across C1 is equal to the voltage ripple across the inductor DCR. During low DCR sensing, the voltage ripple across C1 is equal to the 5x the voltage ripple across the inductor DCR.

To ensure the load current will be delivered over the full operating temperature range, the temperature coefficient of DCR resistance, approximately 3900ppm/°C, should be taken into consideration.

Typically, C is selected in the range of 0.047µF to 0.47µF. This forces R1 to around 2kΩ at MFR_PWM_MODE[2]=0, 400Ω at MFR_PWM_MODE[2]=1 reducing error that might have been caused by the I_{SENSE} pins' ±1µA current (R3 and C2 are for reducing sensing error caused by input current through R1).

There will be some power loss in R1 that relates to the duty cycle, and will be the most in continuous mode at the maximum input voltage:

$$P_{LOSS}(R1) = \frac{\left(V_{IN(MAX)} - V_{OUT}\right) \bullet V_{OUT}}{R1}$$

Ensure that R1 has a power rating higher than this value. However, DCR sensing eliminates the conduction loss of sense resistor; it will provide better efficiency at heavy loads. To maintain a good signal-to-noise ratio for low current sense signals, it is best to enable the LOW DCR sensing network (MFR_PWM_MODE[2] = 1, RC = L/(5 • DCR).

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For a DCR sensing application, the peak-to-peak ripple voltage will be determined by the equation:

$$\Delta V_{SENSE} = \frac{V_{OUT}}{V_{IN}} \bullet \frac{V_{IN} - V_{OUT}}{RC \bullet f_{OSC}}$$

Low DCR sensing can be used at ΔV_{SENSE} signal as low as 2mV.

INDUCTOR VALUE CALCULATION

Given the desired input and output voltages, the inductor value and operating frequency, f_{OSC}, directly determine the inductor peak-to-peak ripple current:

$$\Delta I_L = \frac{V_{OUT}\left(V_{IN} - V_{OUT}\right)}{V_{IN} \bullet f_{OSC} \bullet L}$$

Lower ripple current reduces core losses in the inductor, ESR losses in the output capacitors, and output voltage ripple. Thus, at a given frequency, the highest efficiency operation is obtained with a small ripple current, which requires a large inductor.

A reasonable starting point is to choose a ripple current that is about 40% of $I_{OUT(MAX)}$. Note that the largest ripple current occurs at the highest input voltage. To guarantee that the ripple current does not exceed a specified maximum, the inductor should be chosen according to:

$$L \geq \frac{V_{OUT}\left(V_{IN} - V_{OUT}\right)}{V_{IN} \bullet f_{OSC} \bullet I_{RIPPLE}}$$

INDUCTOR CORE SELECTION

Once the inductor value is determined, the type of inductor must be selected. Core loss is independent of core size for a fixed inductor value, but it is very dependent on inductance. As the inductance increases, core losses go down. Unfortunately, increased inductance requires more turns of wire and therefore copper losses increase. Ferrite designs have very low core loss and are preferred at high switching frequencies, so design goals can concentrate on copper loss and preventing saturation. Ferrite core materials saturate hard, which means that the inductance collapses abruptly when the peak design current is exceeded. This results in an abrupt increase in inductor ripple current and consequent output voltage ripple. Do not allow the core to saturate!

LOW VALUE RESISTOR CURRENT SENSING

A typical sensing circuit using a discrete resistor is shown in Figure 28b. R_{SENSE} is chosen based on the required output current.

The current comparator has a maximum threshold $V_{SENSE(MAX)}$ determined by the I_{LIMIT} setting. The input common mode range of the current comparator is 0V to 5.5V. The current comparator threshold sets the peak of the inductor current, yielding a maximum average output current I_{MAX} equal to the peak value less half the peak-to-peak ripple current ΔI_L. To calculate the sense resistor value, use the equation:

$$R_{SENSE} = \frac{V_{SENSE(MAX)}}{I_{MAX} + \frac{\Delta I_L}{2}}$$

Due to possible PCB noise in the current sensing loop, the AC current sensing ripple of $\Delta V_{SENSE} = \Delta I_L \bullet R_{SENSE}$ also needs to be checked in the design to get a good signal-to-noise ratio. In general, for a reasonably good PCB layout, a 15mV minimum ΔV_{SENSE} voltage is recommended as a conservative number to start with for R_{SENSE} applications.

For previous generation current mode controllers, the maximum sense voltage was high enough (e.g., 75mV for the LTC1628/LTC3728 family) that the voltage drop across the parasitic inductance of the sense resistor represented a relatively small error. In the newer and higher current density solutions, the value of the sense resistor can be less than 1mΩ and the peak sense voltage can be less than 20mV. Also, inductor ripple currents greater than 50% with operation up to 750kHz are becoming more common. Under these conditions, the voltage drop across the sense resistor's parasitic inductance is no longer negligible. A typical sensing circuit using a discrete resistor is shown in Figure 28b. In previous generations of controllers, a small RC filter placed near the IC was commonly used to reduce the effects of the capacitive and inductive noise coupled in the sense traces on the PCB. A typical filter consists of two series 100Ω resistors connected to a parallel 1000pF capacitor, resulting in a time constant of 200ns.

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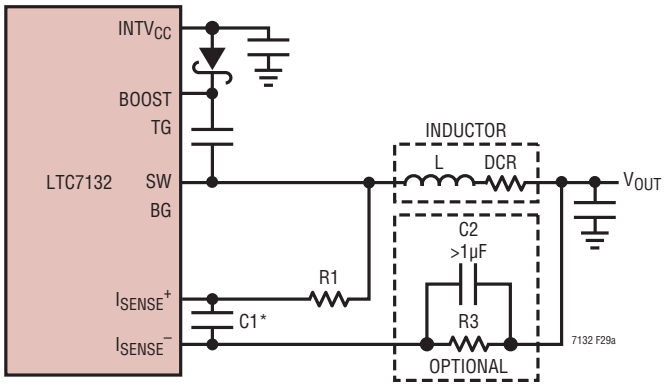

Figure 28a. Inductor DCR Current Sense Circuit

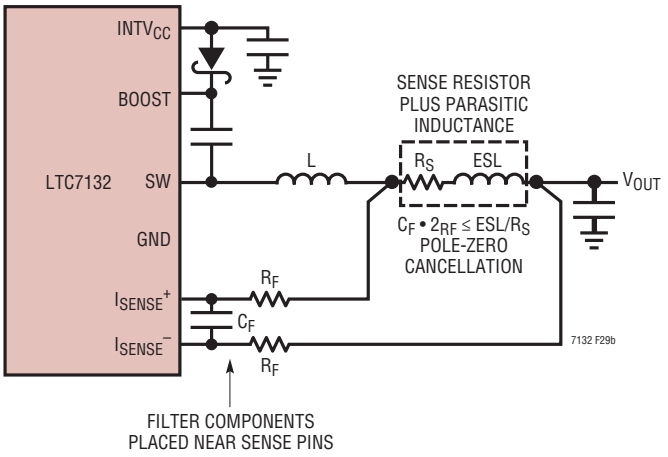

Figure 28b. Resistor Current Sense Circuit

This same RC filter, with minor modifications, can be used to extract the resistive component of the current sense signal in the presence of parasitic inductance. For example, Figure 29a illustrates the voltage waveform across a 2mΩ resistor with a PCB footprint of 2010. The waveform is the superposition of a purely resistive component and a purely inductive component. It was measured using two scope probes and waveform math to obtain a differential measurement. Based on additional measurements of the inductor ripple current and the on-time, t_{ON}, and off-time, t_{OFF}, of the top switch, the value of the parasitic inductance was determined to be 0.5nH using the equation:

$$ESL = \frac{V_{ESL}(STEP)}{\Delta I_L} \bullet \frac{t_{ON} \bullet t_{OFF}}{t_{ON} + t_{OFF}} \quad (1)$$

If the RC time constant is chosen to be close to the parasitic inductance divided by the sense resistor (L/R), the resultant waveform looks resistive, as shown in Figure 29b. For applications using low maximum sense voltages, check the sense resistor manufacturer's data sheet for information about parasitic inductance. In the absence of data, measure the voltage drop directly across the sense resistor to extract the magnitude of the ESL step and use Equation 1 to determine the ESL. However, do not overfilter the signal. Keep the RC time constant less than or equal to the inductor time constant to maintain a sufficient ripple voltage on V_{RSENSE} for optimal operation of the current loop controller.

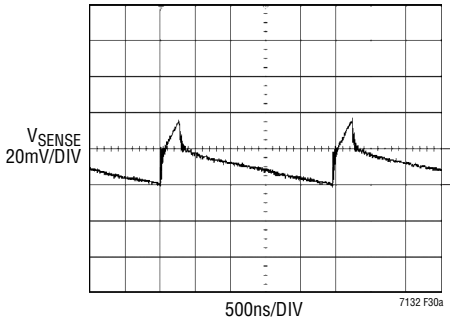

Figure 29a. Voltage Measured Directly Across R_{SENSE}

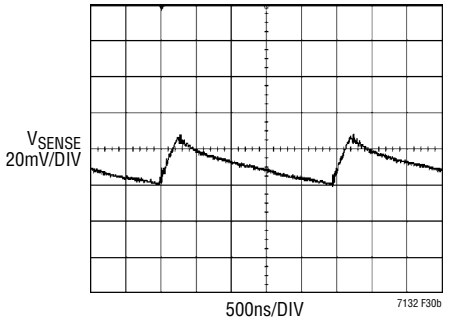

Figure 29b. Voltage Measured After the R_{SENSE} Filter

SLOPE COMPENSATION AND INDUCTOR PEAK CURRENT

Slope compensation provides stability in constant-frequency current-mode architectures by preventing subharmonic oscillations at high duty cycles. This is accomplished internally by adding a compensation ramp to the inductor current signal. The LTC7132 uses a patented

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current limit technique that counteracts the compensating ramp. This allows the maximum inductor peak current to remain unaffected throughout all duty cycles.

VARIABLE DELAY TIME, SOFT-START AND OUTPUT VOLTAGE RAMPING

The LTC7132 must enter the run state prior to soft-start. The RUN*n* pin is released after the part initializes and V_{IN} is greater than the VIN_ON threshold. If multiple LTC7132s are used in an application, they should be configured to share the same RUN*n* pins. They all hold their respective RUN*n* pins low until all devices initialize and V_{IN} exceeds the VIN_ON threshold for all devices. The SHARE_CLK pin assures all the devices connected to the signal use the same time base.

After the RUN*n* pin releases, the controller waits for the user-specified turn-on delay (TON_DELAY) prior to initiating an output voltage ramp. Multiple LTC7132s and other ADI parts can be configured to start with variable delay times. To work correctly, all devices use the same timing clock (SHARE_CLK) and all devices must share the RUN*n* pin. This allows the relative delay of all parts to be synchronized. The actual variation in the delay will be dependent on the highest clock rate of the devices connected to the SHARE_CLK pin (all Analog Devices ICs are configured to allow the fastest SHARE_CLK signal to control the timing of all devices). The SHARE_CLK signal can be ±10% in frequency, thus the actual time delays will have proportional variance.

Soft-start is performed by actively regulating the load voltage while digitally ramping the target voltage from 0.0V to the commanded voltage set point. The rise time of the voltage ramp can be programmed using the TON_RISE command to minimize inrush currents associated with the start-up voltage ramp. The soft-start feature is disabled by setting TON_RISE to any value less than 0.250ms. The LTC7132 will perform the necessary math internally to assure the voltage ramp is controlled to the desired slope. However, the voltage slope cannot be any faster than the fundamental limits of the power stage. The shorter TON_RISE time is set, the larger the discrete steps in the TON_RISE ramp will appear. The number of steps in the ramp is equal to TON_RISE/0.1ms.

The LTC7132 PWM will always use discontinuous mode during the TON_RISE operation. In discontinuous mode, the bottom gate is turned off as soon as reverse current is detected in the inductor. This will allow the regulator to start up into a pre-biased load.

There is no traditional tracking feature in the LTC7132. However, two outputs can be given the same TON_RISE and TON_DELAY times to effectively ramp up at the same time. If the RUN pin is released at the same time and both LTC7132s use the same time base, the outputs will track very closely. If the circuit is in a PolyPhase configuration, all timing parameters must be the same.

The method of start-up sequencing described above is time based. For concatenated events it is possible to control the RUN*n* pins based on the PGOOD*n* pin of a different controller. There is 60µs filtering to the PGOOD*n* inside the device. If unwanted transitions still occur on PGOOD*n*, place a capacitor to ground on the PGOOD*n* pin to filter the waveform. The RC time-constant of the filter should be set sufficiently fast to assure no appreciable delay is incurred. A value of 300µs to 500µs will provide some additional filtering without significantly delaying the trigger event.

DIGITAL SERVO MODE

For maximum accuracy in the regulated output voltage, enable the digital servo loop by asserting bit 6 of the MFR_PWM_MODE command. In digital servo mode, the LTC7132 will adjust the regulated output voltage based on the ADC voltage reading. Every 90ms the digital servo loop will step the LSB of the DAC (nominally 1.375mV or 0.688mV depending on the voltage range bit) until the output is at the correct ADC reading. At power-up this mode engages after TON_MAX_FAULT_LIMIT unless the limit is set to 0 (infinite). If the TON_MAX_FAULT_LIMIT is set to 0 (infinite), the servo begins after TON_RISE is complete and V_{OUT} has exceeded the VOUT_UV_FAULT_LIMIT. This same point in time is when the output changes from discontinuous to the programmed mode as indicated in MFR_PWM_MODE bit 0. Refer to Figure 30 for details on the V_{OUT} waveform under time-based sequencing. If the TON_MAX_FAULT_LIMIT is set to a value greater than 0

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and the TON_MAX_FAULT_RESPONSE is set to ignore 0x00, the servo begins:

1. After the TON_RISE sequence is complete
2. After the TON_MAX_FAULT_LIMIT time is reached; and
3. After the VOUT_UV_FAULT_LIMIT has been exceed or the IOUT_OC_FAULT_LIMIT is no longer active.

If the TON_MAX_FAULT_LIMIT is set to a value greater than 0 and the TON_MAX_FAULT_RESPONSE is not set to ignore 0X00, the servo begins:

1. After the TON_RISE sequence is complete;
2. After the TON_MAX_FAULT_LIMIT time has expired and both VOUT_UV_FAULT and IOUT_OC_FAULT are not present.

The maximum rise time is limited to 1.3 seconds.

In a PolyPhase configuration it is recommended only one of the control loops have the digital servo mode enabled. This will assure the various loops do not work against each other due to slight differences in the reference circuits.

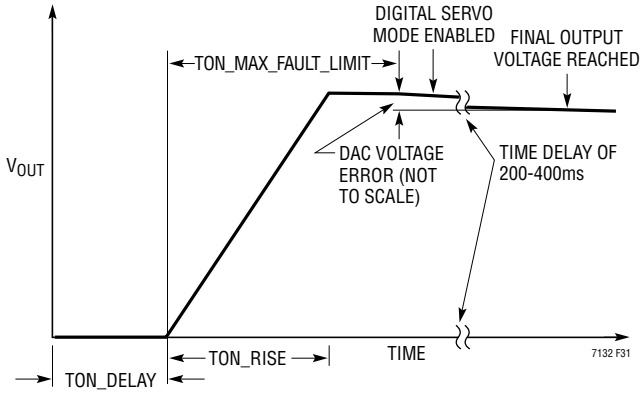

Figure 30. Timing Controlled V_{OUT} Rise

SOFT OFF (SEQUENCED OFF)

In addition to a controlled start-up, the LTC7132 also supports controlled turn-off. The TOFF_DELAY and TOFF_FALL functions are shown in Figure 31. TOFF_FALL is processed when the RUN pin goes low or if the part is commanded off. If the part faults off or $\overline{FAULT}n$ is pulled low externally and the part is programmed to respond to this, the output will three-state rather than exhibiting a controlled ramp. The output will decay as a function of the load. The output voltage will operate as shown in Figure 31 so long as the part is in forced continuous mode and the TOFF_FALL time is sufficiently slow that the power stage can achieve the desired slope. The TOFF_FALL time can only be met if the power stage and controller can sink sufficient current to assure the output is at zero volts by the end of the fall time interval. If the TOFF_FALL time is set shorter than the time required to discharge the load capacitance, the output will not reach the desired zero volt state. At the end of TOFF_FALL, the controller will cease to sink current and VOUT will decay at the natural rate determined by the load impedance. If the controller is in discontinuous mode, the controller will not pull negative current and the output will be pulled low by the load, not the power stage. The maximum fall time is limited to 1.3 seconds. The shorter TOFF_FALL time is set, the larger the discrete steps in the TOFF_FALL ramp will appear. The number of steps in the ramp is equal to TOFF_FALL/0.1ms.

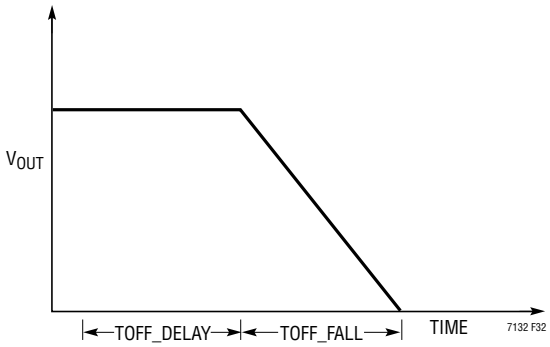

Figure 31. TOFF_DELAY and TOFF_FALL

$INTV_{CC}/EXTV_{CC}$ POWER

The internal MOSFET drivers and most other internal circuitry are derived from the $INTV_{CC}$ pin. When the $EXTV_{CC}$ pin is shorted to GND or tied to a voltage less than 4.7V, or SV_{IN} is lower than 7V, an internal 5.5V linear regulator supplies $INTV_{CC}$ power from V_{IN}. If $EXTV_{CC}$ is taken above 4.7V and SV_{IN} is higher than 7V, the internal 5.5V regulator is turned off and an internal switch is turned on connecting $EXTV_{CC}$ to $INTV_{CC}$. $EXTV_{CC}$ reduces power dissipation from the internal low dropout 5.5V regulator, thus improves the overall efficiency and thermal performance.

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$EXTV_{CC}$ can be applied before V_{IN}. The regulator can supply a peak current of 100mA. Both $INTV_{CC}$ and $EXTV_{CC}$ need to be bypassed to ground with a minimum of 1µF ceramic capacitor or low ESR electrolytic capacitor. No matter what type of bulk capacitor is used, an additional 0.1µF ceramic capacitor placed directly adjacent to the $INTV_{CC}$ and PGND pins is highly recommended. Good bypassing is needed to supply the high transient currents required by the MOSFET gate drivers.

Do not tie $INTV_{CC}$ on the LTC7132 to an external supply because $INTV_{CC}$ will attempt to pull the external supply high and hit current limit, significantly increasing the die temperature.

For applications where V_{IN} is less than 6V, tie the SV_{IN} and $INTV_{CC}$ pins together to the supply voltage through a 1Ω or 2.2Ω resistor as shown in Figure 32. To minimize the voltage drop caused by the gate charge current a low ESR capacitor must be connected to the $SV_{IN}/INTV_{CC}$ pins. This configuration will override the $INTV_{CC}$ linear regulator and will prevent $INTV_{CC}$ from dropping too low. The UVLO on $INTV_{CC}$ is set to approximately 4V.

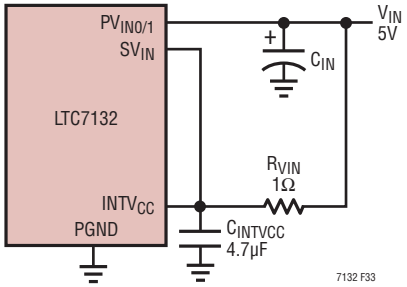

Figure 32. Setup for a 5V Input

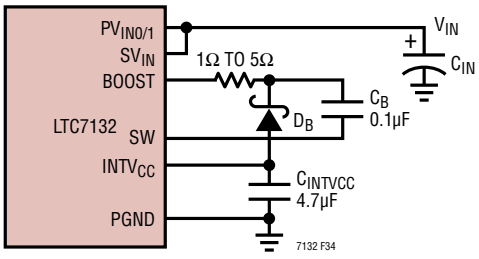

Figure 33. Boost Circuit to Minimize PWM Jitter

TOPSIDE MOSFET DRIVER SUPPLY (C_B, D_B)

External bootstrap capacitors, C_B, connected to the BOOST*n* pin supplies the gate drive voltages for the internal topside MOSFETs. Capacitor C_B in the Block Diagram is charged through external diode D_B from $INTV_{CC}$ when the SW*n* pin is low. When one of the topside MOSFETs is to be turned on, the driver places the C_B voltage across the gate source of the desired MOSFET. This enhances the MOSFET and turns on the topside switch. The switch node voltage, SW*n*, rises to V_{IN} and the BOOST*n* pin follows. With the internal topside MOSFET on, the boost voltage is above the input supply: $V_{BOOST} = V_{IN} + V_{INTVCC}$. The value of the boost capacitor, C_B, needs to be 100 times that of the total input capacitance of the topside MOSFET(s). The reverse breakdown of the external Schottky diode must be greater than $V_{IN(MAX)}$.

PWM jitter has been observed in some designs operating at higher V_{IN}/V_{OUT} ratios. This jitter does not substantially affect the circuit accuracy. Referring to Figure 33, PWM jitter can be removed by inserting a series resistor with a value of 1Ω to 5Ω between the cathode of the diode and the BOOSTn pin. A resistor case size of 0603 or larger is recommended to reduce ESL and achieve the best results.

UNDERVOLTAGE LOCKOUT

The LTC7132 is initialized by an internal threshold-based UVLO where V_{IN} must be approximately 4V and $INTV_{CC}$, V_{DD33}, and V_{DD25} must be within approximately 20% of their regulated values. In addition, V_{DD33} must be within approximately 7% of the targeted value before the RUN pin is released. After the part has initialized, an additional comparator monitors V_{IN}. The VIN_ON threshold must be exceeded before the power sequencing can begin. When V_{IN} drops below the VIN_OFF threshold, the SHARE_CLK pin will be pulled low and V_{IN} must increase above the VIN_ON threshold before the controller will restart. The normal start-up sequence will be allowed after the VIN_ON threshold is crossed. If $\overline{FAULTB}$ is held low when V_{IN} is applied, $\overline{ALERT}$ will be asserted low even if the part is programmed to not assert $\overline{ALERT}$ when $\overline{FAULTB}$ is held low. If I^2C communication occurs before the LTC7132 is out of reset and only a portion of the command is seen by

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the part, this can be interpreted as a CML fault. If a CML fault is detected, $\overline{ALERT}$ is asserted low.

It is possible to program the contents of the NVM in the application if the V_{DD33} supply is externally driven directly to V_{DD33} or through $EXTV_{CC}$. This will activate the digital portion of the LTC7132 without engaging the high voltage sections. PMBus communications are valid in this supply configuration. If V_{IN} has not been applied to the LTC7132, bit 3 (NVM Not Initialized) in MFR_COMMON will be asserted low. If this condition is detected, the part will only respond to addresses 5A and 5B. To initialize the part issue the following set of commands: global address 0x5B command 0xBD data 0x2B followed by global address 5B command 0xBD and data 0xC4. The part will now respond to the correct address. Configure the part as desired then issue a STORE_USER_ALL. When V_{IN} is applied a MFR_RESET command must be issued to allow the PWM to be enabled and valid ADC conversions to be read.

C_{IN} AND C_{OUT} SELECTION

In continuous mode, the source current of the internal top MOSFET is a square wave of duty cycle $(V_{OUT})/(V_{IN})$. To prevent large voltage transients, a low ESR capacitor sized for the maximum RMS current of one channel must be used. The maximum RMS capacitor current is given by:

$$C_{IN}\ \text{Required}\ I_{RMS} \approx \frac{I_{MAX}}{V_{IN}}\left[(V_{OUT})(V_{IN}-V_{OUT})\right]^{1/2}$$

This formula has a maximum at $V_{IN} = 2V_{OUT}$, where $I_{RMS} = I_{OUT}/2$. This simple worst-case condition is commonly used for design because even significant deviations do not offer much relief. Note that capacitor manufacturers' ripple current ratings are often based on only 2000 hours of life. This makes it advisable to further derate the capacitor, or to choose a capacitor rated at a higher temperature than required. Several capacitors may be paralleled to meet size or height requirements in the design. Due to the high operating frequency of the LTC7132, ceramic capacitors can also be used for C_{IN}. Always consult the manufacturer if there is any question.

The benefit of using a LTC7132 in 2-phase operation can be calculated by using the equation above for the higher power monolithic and then calculating the loss that would have resulted if both channels switched on at the same time. The total RMS power loss is lower when both channels are operating due to the reduced overlap of current pulses required through the input capacitor's ESR. This is why the input capacitor's requirement calculated above for the worst-case controller is adequate for the dual controller design. Also, the input protection fuse resistance, battery resistance, and PC board trace resistance losses are also reduced due to the reduced peak currents in a 2-phase system. The overall benefit of a multiphase design will only be fully realized when the source impedance of the power supply/battery is included in the efficiency testing.

A small (0.1µF to 1µF) bypass capacitor between the chip SV_{IN} pin and ground, placed close to the LTC7132, is also suggested. A 2.2Ω to 10Ω resistor placed between C_{IN} (C1) and the V_{IN} pin provides further isolation between the two LTC7132s.

The selection of C_{OUT} is driven by the effective series resistance (ESR). Typically, once the ESR requirement is satisfied, the capacitance is adequate for filtering. The output ripple (ΔV_{OUT}) is approximated by:

$$\Delta V_{OUT} \approx I_{RIPPLE}\left(ESR + \frac{1}{8 \bullet f \bullet C_{OUT}}\right)$$

where f is the operating frequency, C_{OUT} is the output capacitance and I_{RIPPLE} is the ripple current in the inductor. The output ripple is highest at maximum input voltage since I_{RIPPLE} increases with input voltage.

FAULT INDICATION

The LTC7132 $\overline{FAULT}$ pins are configurable to indicate a variety of faults including OV, UV, OC, OT, timing faults, and peak over current faults. In addition, the $\overline{FAULT}$ pins can be pulled low by external sources indicating a fault in

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some other portion of the system. The fault response is configurable and allows the following options:

- Ignore
- Shut Down Immediately—Latch Off
- Shut Down Immediately—Retry Indefinitely at the Time Interval Specified in MFR_RETRY_DELAY

Refer to the PMBus section of the data sheet and the PMBus specification for more details.

The OV response is automatic. If an OV condition is detected, SW*n* goes low.

Fault logging is available on the LTC7132. The fault logging is configurable to automatically store data when a fault occurs that causes the unit to fault off. The header portion of the fault logging table contains peak values. It is possible to read these values at any time. This data will be useful while troubleshooting the fault.

If the LTC7132 internal temperature is in excess of 85°C, writes into the NVM (other than fault logging) are not recommended. The data will still be held in RAM, unless the 3.3V supply UVLO threshold is reached. If the die temperature exceeds 130°C all NVM communication is disabled until the die temperature drops below 120°C.

OPEN-DRAIN PINS

The LTC7132 has the following open-drain pins:

3.3V Pins

1. $\overline{\text{FAULT}}$
2. SYNC
3. SHARE_CLK
4. PGOOD*n*

5V Pins (5V pins operate correctly when pulled to 3.3V.)

1. RUN*n*
2. $\overline{\text{ALERT}}$
3. SCL
4. SDA

All the above pins have on-chip pull-down transistors that can sink 3mA at 0.4V. The low threshold on the pins is 0.8V; thus, there is plenty of margin on the digital signals with 3mA of current. For 3.3V pins, 3mA of current is a 1.1k resistor. Unless there are transient speed issues associated with the RC time constant of the resistor pull-up and parasitic capacitance to ground, a 10k resistor or larger is generally recommended.

For high speed signals such as the SDA, SCL and SYNC, a lower value resistor may be required. The RC time constant should be set to 1/3 to 1/5 the required rise time to avoid timing issues. For a 100pF load and a 400kHz PMBus communication rate, the rise time must be less than 300ns. The resistor pull-up on the SDA and SCL pins with the time constant set to 1/3 the rise time is:

$$R_{PULLUP} = \frac{t_{RISE}}{3 \bullet 100pF} = 1k$$

The closest 1% resistor value is 1k. Be careful to minimize parasitic capacitance on the SDA and SCL pins to avoid communication problems. To estimate the loading capacitance, monitor the signal in question and measure how long it takes for the desired signal to reach approximately 63% of the output value. This is a one time constant. The SYNC pin has an on-chip pull-down transistor with the output held low for nominally 500ns. If the internal oscillator is set for 500kHz and the load is 100pF and a 3x time constant is required, the resistor calculation is as follows:

$$R_{PULLUP} = \frac{2\mu s - 500ns}{3 \bullet 100pF} = 5k$$

The closest 1% resistor is 4.99k.

If timing errors are occurring or if the SYNC frequency is not as fast as desired, monitor the waveform and determine if the RC time constant is too long for the application. If possible reduce the parasitic capacitance. If not reduce the pull-up resistor sufficiently to assure proper timing. The SHARE_CLK pull-up resistor has a similar equation with a period of 10µs and a pull-down time of 1µs. The RC time constant should be approximately 3µs or faster.

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PHASE-LOCKED LOOP AND FREQUENCY SYNCHRONIZATION

The LTC7132 has a phase-locked loop (PLL) comprised of an internal voltage-controlled oscillator (VCO) and a phase detector. The PLL is locked to the falling edge of the SYNC pin. The phase relationship between the PWM controller and the falling edge of SYNC is controlled by the lower 3 bits of the MFR_PWM_ CONFIG command. For PolyPhase applications, it is recommended that all the phases be spaced evenly. Thus for a 2-phase system the signals should be 180° out of phase and a 4-phase system should be spaced 90°.

The phase detector is an edge-sensitive digital type that provides a known phase shift between the external and internal oscillators. This type of phase detector does not exhibit false lock to harmonics of the external clock.

The output of the phase detector is a pair of complementary current sources that charge or discharge the internal filter network. The PLL lock range is guaranteed between 200kHz and 1MHz. Nominal parts will have a range beyond this; however, operation to a wider frequency range is not guaranteed.

The PLL has a lock detection circuit. If the PLL should lose lock during operation, bit 4 of the STATUS_MFR_SPECIFIC command is asserted and the $\overline{\text{ALERT}}$ pin is pulled low. The fault can be cleared by writing a 1 to the bit. If the user does not wish to see the $\overline{\text{ALERT}}$ pin assert if a PLL_FAULT occurs, the SMBALERT_MASK command can be used to prevent the alert.

If the SYNC signal is not clocking in the application, the nominal programmed frequency will control the PWM circuitry. However, if multiple parts share the SYNC pins and the signal is not clocking, the parts will not be synchronized and excess voltage ripple on the output may be present. Bit 10 of MFR_PADS will be asserted low if this condition exists.

If the PWM signal appears to be running at too high a frequency, monitor the SYNC pin. Extra transitions on the falling edge will result in the PLL trying to lock on to noise versus the intended signal. Review routing of digital control signals and minimize crosstalk to the SYNC signal to avoid this problem. Multiple LTC7132s are required to share one SYNC pin in PolyPhase configurations. For other configurations, connecting the SYNC pins to form a single SYNC signal is optional. If the SYNC pin is shared between LTC7132s, only one LTC7132 can be programmed with a frequency output. All the other LTC7132s should be programmed to disable the SYNC output. However their frequency should be programmed to the nominal desired value.

MINIMUM ON-TIME CONSIDERATIONS

Minimum on-time, $t_{ON(MIN)}$, is the smallest time duration that the LTC7132 is capable of turning on the top MOSFET. It is determined by internal timing delays and the gate charge required to turn on the top MOSFET. Low duty cycle applications may approach this minimum limit and care should be taken to ensure that:

$$t_{ON(MIN)} < \frac{V_{OUT}}{V_{IN} \bullet f_{OSC}}$$

If the duty cycle falls below what can be accommodated by the minimum on-time, the part will begin to skip cycles. The output voltage will continue to be regulated, but the ripple voltage and current will increase.

The minimum on-time for the LTC7132 is approximately 90ns. Reasonably good PCB layout, minimum 30% inductor current ripple and at least 2mV for LOW DCR structure or 10mV to 15mV for regular DCR ripple on the current sense signal are required to avoid increasing the minimum on-time. The minimum on-time can be affected by PCB switching noise in the voltage and current loop. As the peak current sense voltage decreases, the minimum on-time gradually increases to 130ns. This is of particular concern in forced continuous applications with low ripple current at light loads. If the duty cycle drops below the minimum on-time limit in this situation, a significant amount of cycle skipping can occur with correspondingly larger current and voltage ripple.

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EXTERNAL TEMPERATURE SENSE

The LTC7132 is capable of measuring the power stage temperature of each channel. Multiple methods using silicon junction type remote sensors are supported. The voltage produced by the remote sense circuit is digitized by the internal ADC, and the computed temperature value is returned by the paged READ_TEMPERATURE_1 telemetry command.

The most accurate external temperature measurement can be made using a diode-connected PNP transistor such as the MMBT3906 as shown in Figure 34 with bit 5 of MFR_PWM_MODE should be set to 0 (ΔV_{BE} method) when using this sensor configuration. The transistor should be placed in contact with or immediately adjacent to the power stage inductor. Its emitter should be connected to the TSNS*n* pin while the base and collector terminals of the PNP transistor should be returned to the LTC7132 GND paddle using a Kevin connection. For best noise immunity, the connections should be routed differentially and a 10nF capacitor should be placed in parallel with the diode-connected PNP. Parasitic PCB trace inductance between the capacitor and transistor should be minimized. Avoid placing PCB vias between the transistor and capacitor.

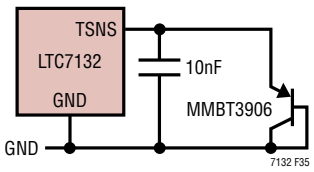

Figure 34. External ΔV_{BE} Temperature Sense

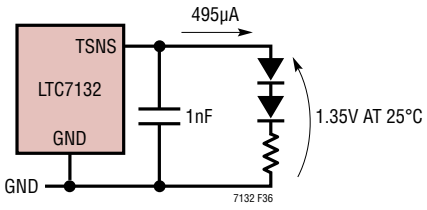

Figure 35. 2D+R Temperature Sense

The LTC7132 also supports direct junction voltage measurements when bit 5 of MFR_PWM_MODE_LTC7132 is set to 1. The factory defaults support a resistor trimmed dual diode network as shown in Figure 35. This second measurement method is not generally as accurate as the first, but it supports legacy power blocks or may prove necessary if high noise environments prevent use of the ΔV_{BE} approach with its lower signal levels.

For either method, the slope of the external temperature sensor can be modified with the coefficient stored in MFR_TEMP_1_GAIN. With the ΔV_{BE} approach, typical PNPs require temperature slope adjustments slightly less than 1. The MMBT3906 has a recommended value in this command of approximately MFR_TEMP_1_GAIN = 0.991 based on the ideality factor of 1.01. Simply invert the ideality factor to calculate the MFR_TEMP_1_GAIN. Different manufacturers and different lots may have different ideality factors. Consult with the manufacturer to set this value. Bench characterization over temperature is recommended when adjusting MFR_TEMP_1_GAIN for the direct p-n junction measurement method.

The offset of the external temperature sense can be adjusted by MFR_TEMP_1_OFFSET.

If an external temperature sense element is not used, the TSNS*n* pin must be shorted to GND. The UT_FAULT_LIMIT must be set to –275°C, and the UT_FAULT_RESPONSE must be set to ignore. The user also needs to set the IOUT_CAL_GAIN_TC to a value of 0.

To ensure proper use of these temperature adjustment parameters, refer to the specific formulas given for the two methods by the MFR_PWM_MODE command in the later section covering PMBus command details.

INPUT CURRENT SENSE AMPLIFIER

The LTC7132 input current sense amplifier can sense the supply current into the V_{IN} pin using an external resistor as well as the power stage current using an external current sense resistor shown in Figure 36. Unless care is taken to mitigate the frequency noise caused by the discontinuous input current, significant input current measurement error may occur. The noise will be the greatest in high current applications and at large step-down ratios. Careful layout and filtering at the SV_{IN} pin is recommended to minimize measurement error. The SV_{IN} pin should be filtered with a resistor and a ceramic capacitor. The filter should be

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located as close to the SV_{IN} pin as possible. The supply side of the SV_{IN} pin filter should be Kelvin connected to the supply side of the R_{IINSNS} resistor. A 2Ω resistor should be sufficient for most applications. The resistor will cause an IR voltage drop from the supply to the SV_{IN} pin due to the current flowing into the SV_{IN} pin. To compensate for this voltage drop, the MFR_RVIN command value should be set to the nominal resistor value. The LTC7132 will multiply the MFR_READ_ICHIP measurement value by the user defined MFR_RVIN value and add this voltage to the measured voltage at the SV_{IN} pin. Therefore

$$READ\_VIN = V_{SVIN\_PIN} + (MFR\_READ\_ICHIP \bullet MFR\_RVIN)$$

Therefore the READ_VIN command will return the value of the voltage at the supply side of the SV_{IN} pin filter. If no SV_{IN} filter element is used, set MFR_RVIN = 0.

The capacitor C1 should be a low ESR ceramic capacitor. It should be placed as close as possible to $PV_{IN0/1}$ to supply high frequency transient input current. This will help prevent noise from the top gate MOSFET from feeding into the input current sense amplifier inputs and supply.

If the input current sense amplifier is not used, short the SV_{IN}, I_{IN}^+, and I_{IN}^- pins together.

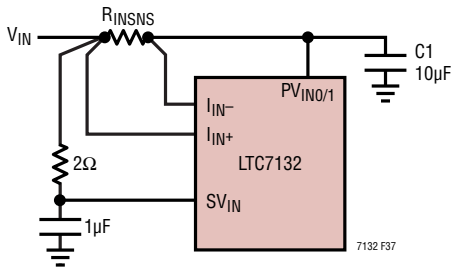

Figure 36. Low Noise Input Current Sense Circuit

EXTERNAL RESISTOR CONFIGURATION PINS (RCONFIG)

The LTC7132 is factory programmed to use the external resistor configuration. This allows output voltage, PWM frequency, PWM phasing, and the PMBus address to be set by the user without programming the part through the PMBus interface or purchasing custom programmed parts. To use resistor programming, the RCONFIG pins require a resistor divider between V_{DD25} and GND. The RCONFIG pins are only interrogated at initial power up and during a reset, so modifying their values on the fly while the part is powered will have no effect. However, this does mean that RCONFIG pins on the same IC can be shared with a single resistor divider if they require identical programming. Resistors with a tolerance of 1% or better must be used to assure proper operation. In the following tables, R_{TOP} is connected between V_{DD25} and the RCONFIG pin while R_{BOT} is connected between the pin and GND. Noisy clock signals should not be routed near these pins.

Voltage Selection

When an output voltage is set using the VOUT_CFG*n* pins (by Table 3) the following parameters are set as a percentage of the output voltage:

- VOUT_OV_FAULT_LIMIT..... +10%
- VOUT_OV_WARN_LIMIT..... +7.5%
- VOUT_MAX..... +7.5%
- VOUT_MARGIN_HIGH.....+5%
- VOUT_MARGIN_LOW.....–5%
- VOUT_UV_WARN_LIMIT..... –6.5%
- VOUT_UV_FAULT_LIMIT..... –7%

Table 3. VOUT_CFG*n* Resistor Programming

R_{TOP} (kΩ)	R_{BOTTOM} (kΩ)	V_{OUT} (V)	ON/OFF
0 or Open	Open	NVM	NVM
10	23.2	5.000	ON
10	15.8	3.300	ON
16.2	20.5	2.500	ON
16.2	17.4	1.800	ON
20	17.8	1.500	ON
20	15	1.350	ON
20	12.7	1.250	ON
20	11	1.200	ON
24.9	11.3	1.150	ON
24.9	9.09	1.100	ON
24.9	7.32	1.050	ON
24.9	5.76	0.900	ON
24.9	4.32	0.750	ON
30.1	3.57	0.650	ON
30.1	1.96	0.600	ON
Open	0	NVM	OFF

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Frequency Selection

The PWM switching frequency is set according to Table 4. The SYNC pins must be shared in PolyPhase configurations where multiple LTC7132s are used to produce the output. If the configuration is not PolyPhase, the SYNC pins do not have to be shared. If the SYNC pins are shared between LTC7132s only one SYNC pin should be enabled; all other SYNC pins should be disabled. A pull-up resistor to V_{DD33} is required on the SYNC pin.

Table 4. FREQ_CFG Resistor Programming

R_{TOP} (kΩ)	R_{BOTTOM} (kΩ)	FREQUENCY (kHz)
0 or Open	Open	NVM
10	23.2	NVM
10	15.8	NVM
16.2	20.5	NVM
16.2	17.4	NVM
20	17.8	NVM
20	15	NVM
20	12.7	NVM
20	11	1000
24.9	11.3	750
24.9	9.09	650
24.9	7.32	575
24.9	5.76	500
24.9	4.32	425
30.1	3.57	350
30.1	1.96	250
Open	0	External Clock

Phase Selection

The phase of the channels with respect to the falling edge of SYNC is set using the values in Table 5.

Table 5. PHASE_CFG Resistor Programming

R_{TOP} (kΩ)	R_{BOTTOM} (kΩ)	SYNC TO CH0 (DEGREES)	SYNC TO CH1 (DEGREES)	SYNC OUTPUT
0 or Open	Open	NVM	NVM	NVM
10	23.2	NVM	NVM	NVM
10	15.8	NVM	NVM	NVM
16.2	20.5	120	300	DISABLED
16.2	17.4	60	240	
20	17.8	120	240	
20	15	0	120	
20	12.7	0	240	
20	11	90	270	
24.9	11.3	0	180	
24.9	9.09	120	300	ENABLED
24.9	7.32	60	240	
24.9	5.76	120	240	
24.9	4.32	0	120	
30.1	3.57	0	240	
30.1	1.96	90	270	
Open	0	0	180	

For example in a 4-phase configuration clocked at 500kHz, all of the LTC7132s must be set to the desired frequency and phase and only one LTC7132 should be set to the desired frequency with the SYNC pin enabled. All phasing is with respect to the falling edge of SYNC.

For LTC7132 Chip 1, set the frequency to 500kHz with 90° and 270° phase shift with the SYNC pin enabled:

Frequency: R_{TOP} = 24.9kΩ and R_{BOT} = 5.76kΩ

Phase: R_{TOP} = 30.1kΩ and R_{BOT} = 1.96kΩ

For LTC7132 Chip 2, set the frequency to 500kHz with 0°and 180° phase shift and the SYNC pin disabled:

Frequency: 24.9kΩ and R_{BOT} = 5.76kΩ

Phase: R_{TOP} = 24.9kΩ and R_{BOT} = 11.3kΩ

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Address Selection Using RCONFIG

The LTC7132 address is selected based on the programming of the two configuration pins ASEL0 and ASEL1 according to Table 6. ASEL0 programs the bottom four bits of the device address for the LTC7132, and ASEL1 programs the three most significant bits. Either portion of the address can also be retrieved from the MFR_ADDRESS value in EEPROM. If both pins are left open, the full 7-bit MFR_ADDRESS value stored in EEPROM is used to determine the device address. The LTC7132 always responds to 7-bit global addresses 0x5A and 0x5B. MFR_ADDRESS should not be set to either of these values because these are global addresses and all parts will respond to them.

Table 6. ASEL*n* Resistor Programming

		ASEL1		ASEL0	
		LTC7132 DEVICE ADDRESS BITS[6:4]		LTC7132 DEVICE ADDRESS BITS[3:0]	
R_{TOP} (kΩ)	R_{BOTTOM} (kΩ)	BINARY	HEX	BINARY	HEX
0 or Open	Open	EEPROM		EEPROM	
10	23.2			1111	F
10	15.8			1110	E
16.2	20.5			1101	D
16.2	17.4			1100	C
20	17.8			1011	B
20	15			1010	A
20	12.7			1001	9
20	11			1000	8
24.9	11.3	111	7	0111	7
24.9	9.09	110	6	0110	6
24.9	7.32	101	5	0101	5
24.9	5.76	100	4	0100	4
24.9	4.32	011	3	0011	3
30.1	3.57	010	2	0010	2
30.1	1.96	001	1	0001	1
Open	0	000	0	0000	0

Table 6b[1]. LTC7132 MFR_ADDRESS Command Examples Expressing Both 7- or 8-Bit Addressing

DESCRIPTION	HEX DEVICE ADDRESS 7 BIT	8 BIT	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0	R/W
Rail[4]	0x5A	0xB4	0	1	0	1	1	0	1	0	0
Global[4]	0x5B	0xB6	0	1	0	1	1	0	1	1	0
Default	0x4F	0x9E	0	1	0	0	1	1	1	1	0
Example 1	0x60	0xC0	0	1	1	0	0	0	0	0	0
Example 2	0x61	0xC2	0	1	1	0	0	0	0	1	0
Disabled[2,3,5]			1	0	0	0	0	0	0	0	0

Note 1: This table can be applied to the MFR_RAIL_ADDRESS command as well as the MFR_ADDRESS command.

Note 2: A disabled value in one command does not disable the device, nor does it disable the Global address.

Note 3: A disabled value in one command does not inhibit the device from responding to device addresses specified in other commands.

Note 4: It is not recommended to write the value 0x00, 0x0C (7 bit), or 0x5A or 0x5B(7 bit) to the MFR_ADDRESS, or the MFR_RAIL_ADDRESS commands.

Note 5: To disable the address enter 0x80 in the MFR_ADDRESS command. The 0x80 is greater than the 7-bit address field, disabling the address.

EFFICIENCY CONSIDERATIONS

The percent efficiency of a switching regulator is equal to the output power divided by the input power times 100%. It is often useful to analyze individual losses to determine what is limiting the efficiency and which change would produce the most improvement. Percent efficiency can be expressed as: %Efficiency = 100% – (L1 + L2 + L3 + ...) where L1, L2, etc. are the individual losses as a percentage of input power.

Although all dissipative elements in the circuit produce losses, four main sources usually account for most of the losses in LTC7132 circuits: 1) IC V_{IN} current, 2) $INTV_{CC}$ regulator current, 3) I^2R losses, 4) Topside MOSFET transition losses.

1. The V_{IN} current is the DC supply current given in the Electrical Characteristics table, which excludes internal MOSFET driver and control currents. V_{IN} current typically results in a small (<0.1%) loss.

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2. $INTV_{CC}$ current is the sum of the internal MOSFET driver and control currents. The internal MOSFET driver current results from switching the gate capacitance of the power MOSFETs. Each time a MOSFET gate is switched from low to high to low again, a packet of charge dQ moves from $INTV_{CC}$ to ground. The resulting dQ/dt is a current out of $INTV_{CC}$ that is typically much larger than the control circuit current.

3. I^2R losses are predicted from the DC resistances of the fuse (if used), internal MOSFETs, inductor, and current sense resistor. In continuous mode, the average output current flows through the inductor and R_{SENSE}, but is "chopped" between the topside MOSFET and the synchronous (bottom) MOSFET.

4. Transition losses apply only to the topside internal MOSFET(s), and become significant only when operating at high input voltages (typically 15V or greater). Transition losses can be estimated from:

   $$\text{Transition Loss} = (1.7) \bullet V_{IN}^2 \bullet I_{O(MAX)} \bullet C_{RSS} \bullet f$$

Other "hidden" losses such as copper trace and internal battery resistances can account for an additional 5% to 10% efficiency degradation in portable systems. It is very important to include these "system" level losses during the design phase. The internal battery and fuse resistance losses can be minimized by making sure that C_{IN} has adequate charge storage and very low ESR at the switching frequency. A 25W supply will typically require a minimum of 20µF to 40µF of capacitance having a maximum of 20mΩ to 50mΩ of ESR. The LTC7132 two-phase architecture typically halves this input capacitance requirement over competing solutions. Other losses including Schottky conduction losses during dead time and inductor core losses generally account for less than 2% total additional loss.

THERMAL CONSIDERATIONS

In LTC7132, the READ_TEMPERATURE_2 command returns the internal die junction temperature of the part using an on-chip diode with a delta VBE measurement and calculation. For applications where the LTC7132 is operated at high ambient temperature, high V_{IN}, high switching frequency and maximum load current, the hot spot may migrate to the power MOSFETs which are located farther away from the internal on-chip diode. Therefore, the maximum output load current rating shall be derated to prevent the internal MOSFETs from overheating.

The junction to ambient thermal resistance of the part will vary depending on the copper area and thickness of the PCB board where the part is mounted, the heat sink mounted on top of the part, as well as the amount of forced air flow used to cool down the device. Figures 38–41 below show the output current derating with both heat sink and airflow on the existing standard demo board.

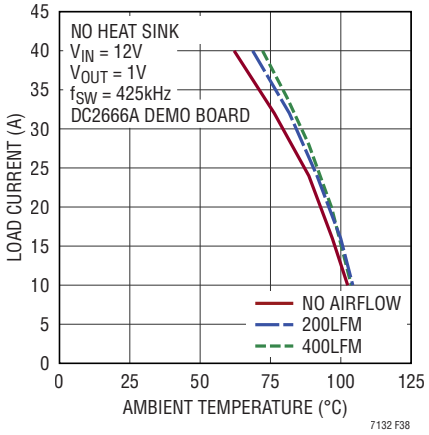

Figure 37. Temperature Derating Curve Based on the DC2666A Demo Board

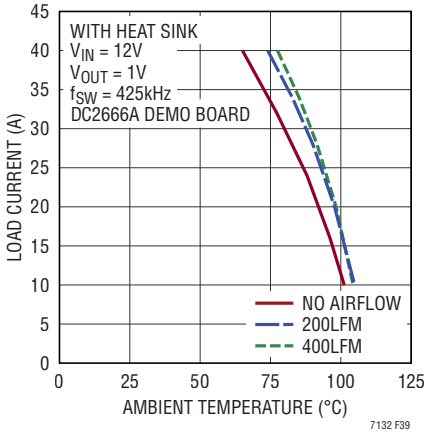

Figure 38. Temperature Derating Curve Based on the DC2666A Demo Board

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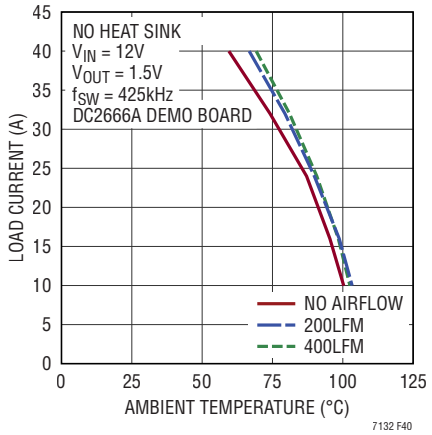

Figure 39. Temperature Derating Curve Based on the DC2666A Demo Board

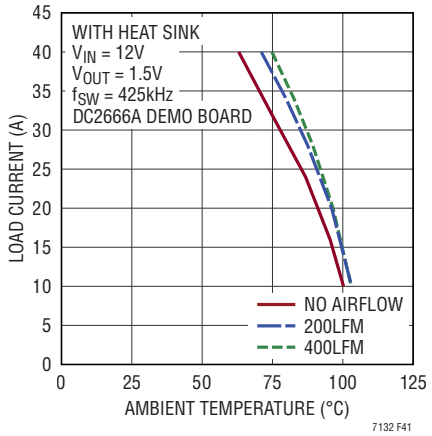

Figure 40. Temperature Derating Curve Based on the DC2666A Demo Board

PROGRAMMABLE LOOP COMPENSATION

The LTC7132 offers programmable loop compensation to optimize the transient response without any hardware change. The error amplifier gain g_m varies from 0.8mmho to 4.6mmho, and the compensation resistor R_{TH} varies from 0kΩ to 62kΩ inside the controller. Two compensation capacitors, C_{TH} and C_{THP}, are required in the design and the typical ratio between C_{TH} and C_{THP} is 10 in Figure 41.

By adjusting the g_m and R_{TH} only, the LTC7132 can provide a flexible type II compensation network to optimize the loop over a wide range of output capacitors. Adjusting the g_m will change the gain of the compensation over the whole frequency range without moving the pole and zero location, as shown in Figure 42.

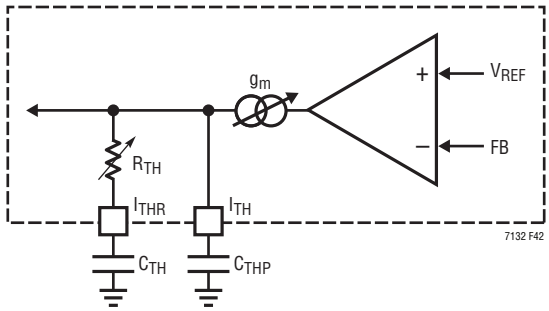

Figure 41. Programmable Loop Compensation

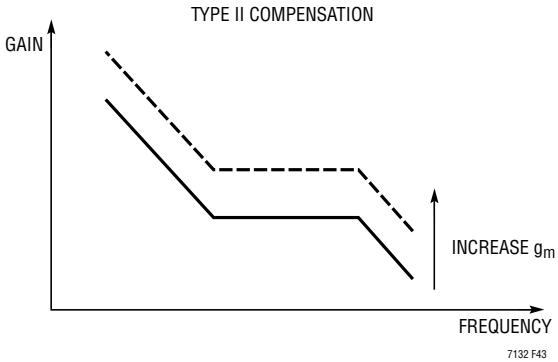

Figure 42. Error Amp g_m Adjust

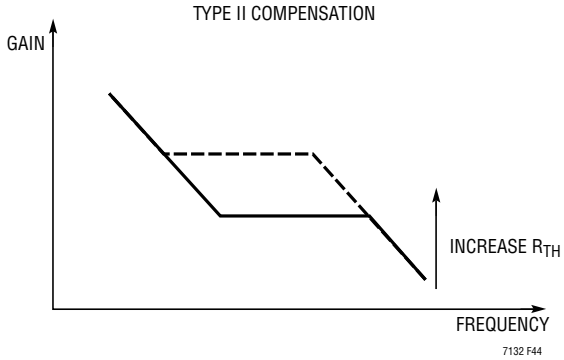

Figure 43. R_{TH} Adjust

Adjusting the R_{TH} will change the pole and zero location, as shown in Figure 43. It is recommended that the user determines the appropriate value for the g_m and R_{TH} using the LTPowerCAD tool.

CHECKING TRANSIENT RESPONSE

The regulator loop response can be checked by looking at the load current transient response. Switching regulators take several cycles to respond to a step in DC (resistive) load current. When a load step occurs, V_{OUT} shifts by an amount equal to ΔI_{LOAD} • (ESR), where ESR is the effective

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series resistance of C_{OUT}. ΔI_{LOAD} also begins to charge or discharge C_{OUT} generating the feedback error signal that forces the regulator to adapt to the current change and return V_{OUT} to its steady-state value. During this recovery time V_{OUT} can be monitored for excessive overshoot or ringing, which would indicate a stability problem. The availability of the I_{TH} pin not only allows optimization of control loop behavior but also provides a DC-coupled and AC-filtered closed-loop response test point. The DC step, rise time and settling at this test point truly reflects the closed-loop response. Assuming a predominantly second order system, phase margin and/or damping factor can be estimated using the percentage of overshoot seen at this pin. The bandwidth can also be estimated by examining the rise time at the pin. The I_{THR} external capacitor shown in the Typical Application circuit will provide an adequate starting point for most applications. The programmable parameters that affect loop gain are the voltage range, bit[1] of the MFR_PWM_MODE command, the current range, bit[2] and bit[7] of the MFR_PWM_MODE command, the g_m of the PWM channel amplifier bits [7:5] of MFR_PWM_COMP, and the internal R_{TH} compensation resistor, bits[4:0] of MFR_PWM_COMP. Be sure to establish these settings prior to compensation calculation.

The I_{TH} series internal R_{TH} external C_{TH} filter sets the dominant pole-zero loop compensation. The internal R_{TH} value can be modified (from 0Ω to 62kΩ) using bits[4:0] of the MFR_PWM_ COMP command. Adjust the value of R_{TH} to optimize transient response once the final PCB layout is done and the particular C_{TH} filter capacitor and output capacitor type and value have been determined. The output capacitors need to be selected because the various types and values determine the loop gain and phase. An output current pulse of 20% to 80% of full-load current having a rise time of 1µs to 10µs will produce output voltage and I_{TH} pin waveforms that will give a sense of the overall loop stability without breaking the feedback loop. Placing a power MOSFET in series with a current sense resistor to ground directly across the output capacitor and driving the gate with an appropriate signal generator is a practical way to produce to a load step. The MOSFET + R_{SERIES} will produce output currents approximately equal to V_{OUT}/R_{SERIES}. R_{SERIES} values from 0.1Ω to 2Ω are valid depending on the current limit settings and the programmed output voltage. The initial output voltage step resulting from the step change in output current may not be within the bandwidth of the feedback loop, so this signal cannot be used to determine phase margin. This is why it is better to look at the I_{TH} pin signal which is in the feedback loop and is the filtered and compensated control loop response. The gain of the loop will be increased by increasing R_{TH} and the bandwidth of the loop will be increased by decreasing C_{TH}. If R_{TH} is increased by the same factor that C_{TH} is decreased, the zero frequency will be kept the same, thereby keeping the phase shift the same in the most critical frequency range of the feedback loop. The gain of the loop will be proportional to the transconductance of the error amplifier which is set using bits[7:5] of the MFR_PWM_COMP command. The output voltage settling behavior is related to the stability of the closed-loop system and will demonstrate the actual overall supply performance. A second, more severe transient is caused by switching in loads with large (>1µF) supply bypass capacitors. The discharged bypass capacitors are effectively put in parallel with C_{OUT}, causing a rapid drop in V_{OUT}. No regulator can alter its delivery of current quickly enough to prevent this sudden step change in output voltage if the load switch resistance is low and it is driven quickly. If the ratio of C_{LOAD} to C_{OUT} is greater than 1:50, the switch rise time should be controlled so that the load rise time is limited to approximately 25 • C_{LOAD}. Thus a 10µF capacitor would require a 250µs rise time, limiting the charging current to about 200mA.

PolyPhase Configuration

When configuring a PolyPhase rail with multiple LTC7132s, the user must share the SYNC, I_{TH}, SHARE_CLK, $\overline{\text{FAULT}}$, and $\overline{\text{ALERT}}$ pins of these parts. Be sure to use pull-up resistors on $\overline{\text{FAULT}}$, SHARE_CLK and $\overline{\text{ALERT}}$. One of the part's SYNC pins must be set to the desired switching frequency, and all other FREQUENCY_SWITCH commands must be set to External Clock. If an external oscillator is provided, set the FREQUENCY_SWITCH command to External Clock for all parts. The relative phasing of all the channels should be spaced equally. The MFR_RAIL_ADDRESS of all the devices should be set to the same value.

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When connecting a PolyPhase rail with LTC7132s, connect the V_{IN} pins of the LTC7132s directly back to the supply voltage through the V_{IN} pin filter networks.

PC BOARD LAYOUT CHECKLIST

When laying out the printed circuit board, the following checklist should be used to ensure proper operation of the IC. These items are also illustrated graphically in the layout diagram of Figure 44. Figure 45 illustrates the current waveforms present in the various branches of a synchronous regulator operating in continuous mode. Check the following in your layout:

1. Are signal ground and power ground kept separate? The ground return of C_{INTVCC} must return to the combined C_{OUT} (–) terminals.
2. The I_{TH} trace should be as short as possible.
3. The loop formed by the top N-channel MOSFET, Schottky diode and the C_{IN} capacitor should have short leads and PC trace lengths.
4. The output capacitor (–) terminals should be connected as close as possible to the (–) terminals of the input capacitor by placing the capacitors next to each other and away from the Schottky loop described in item 4.
5. Are the I_{SENSE}^+ and I_{SENSE}^- leads routed together with minimum PC trace spacing? The filter capacitor between I_{SENSE}^+ and I_{SENSE}^- should be as close as possible to the IC. Ensure accurate current sensing with Kelvin connections at the sense resistor or inductor, whichever is used for current sensing.
6. Is the $INTV_{CC}$ decoupling capacitor connected close to the IC, between the $INTV_{CC}$ and the power ground pins? This capacitor carries the MOSFET driver current peaks. An additional 1µF ceramic capacitor placed immediately next to the $INTV_{CC}$ and GND pins can help improve noise performance substantially.
7. Keep the switching nodes (SW*n*) and boost nodes (BOOST*n*) away from sensitive small-signal nodes, especially from the voltage and current sensing feedback pins. All of these nodes have very large and fast moving signals and therefore should be kept on the "output side" of the LTC7132 and occupy minimum PC trace area. If DCR sensing is used, place the top resistor (Figure 25a, R1) close to the switching node.

PC BOARD LAYOUT DEBUGGING

It is helpful to use a DC-50MHz current probe to monitor the current in the inductor while testing the circuit. Monitor the output switching node (SW*n* pin) to synchronize the oscilloscope to the internal oscillator and probe the actual output voltage as well. Check for proper performance over the operating voltage and current range expected in the application. The frequency of operation should be maintained over the input voltage range down to dropout and until the output load drops below the low current operation threshold.

The duty cycle percentage should be maintained from cycle to cycle in a well-designed, low noise PCB implementation. Variation in the duty cycle at a subharmonic rate can suggest noise pickup at the current or voltage sensing inputs or inadequate loop compensation. Overcompensation of the loop can be used to tame a poor PC layout if regulator bandwidth optimization is not required.

Reduce V_{IN} from its nominal level to verify operation of the regulator in dropout. Check the operation of the undervoltage lockout circuit by further lowering V_{IN} while monitoring the outputs to verify operation.

Investigate whether any problems exist only at higher output currents or only at higher input voltages. If problems coincide with high input voltages and low output currents, look for capacitive coupling between the BOOST*n* and SW*n* connections and the sensitive voltage and current pins. The capacitor placed across the current sensing pins needs to be placed immediately adjacent to the pins of the IC. This capacitor helps to minimize the effects of differential noise injection due to high frequency capacitive coupling. If problems are encountered with high current output loading at lower input voltages, look for inductive coupling between C_{IN}, Schottky components to the sensitive current and voltage sensing traces. In addition, investigate common ground path voltage pickup between these components and the GND pin of the IC.

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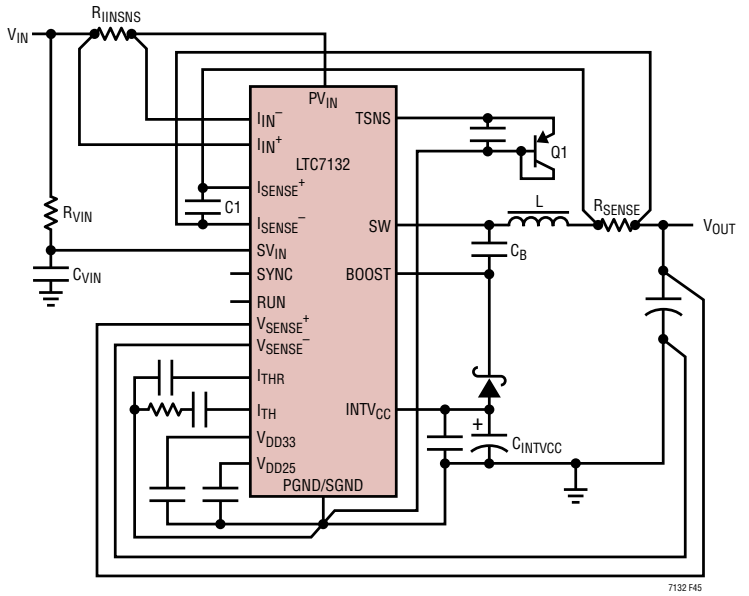

Figure 44. Recommended Printed Circuit Layout Diagram, Single Phase Shown

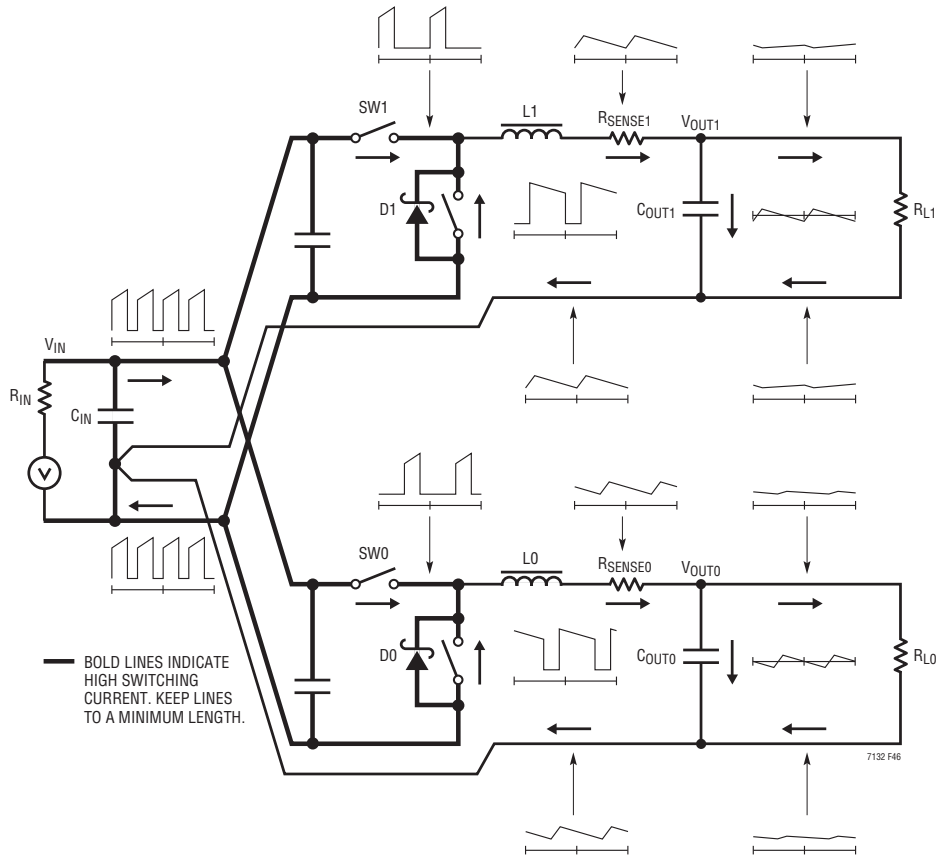

Figure 45. Branch Current Waveforms

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DESIGN EXAMPLE

As a design example for a 2-channel medium current regulator, assume V_{IN} = 12V nominal, V_{IN} = 20V maximum, V_{OUT0} =1.5V, V_{OUT1} = 1.05V, $I_{MAX0,1}$ = 20A and f = 425kHz.

The regulated output is established by the VOUT_COMMAND stored in NVM or placing the following resistor divider between V_{DD25}, the RCONFIG pin and SGND:

1. V_{OUT0_CFG}, R_{TOP} = 20k, R_{BOTTOM} = 17.8k
2. V_{OUT1_CFG}, R_{TOP} = 24.9k, R_{BOTTOM} = 7.32k

The frequency and phase are set by NVM or by setting the resistor divider between V_{DD25}, FREQ_CFG and SGND and V_{DD25}, PHASE_CFG and SGND.

Frequency, R_{TOP} = 24.9kΩ and R_{BOTTOM} = 4.32kΩ

Phase, R_{TOP} = open and R_{BOTTOM} = 0Ω

The address is set to XF where X is the MSB stored in the NVM.

The following parameters are set as a percentage of the output voltage if the resistor configuration pins are used to determined output voltage:

- VOUT_OV_FAULT_LIMIT..... +10%
- VOUT_OV_WARN_LIMIT..... +7.5%
- VOUT_MAX..... +7.5%
- VOUT_MARGIN_HIGH.....5%
- VOUT_MARGIN_LOW.....5%
- VOUT_UV_WARN_LIMIT.....6.5%
- VOUT_UV_FAULT_LIMIT.....7%

All other user defined parameters must be programmed into the NVM. The GUI can be utilized to quickly set up the part with the desired operating parameters.

The inductance values are based on a 40% maximum ripple current assumption (8A). The highest value of ripple current occurs at the maximum input voltage:

$$L = \frac{V_{OUT}}{f \bullet \Delta I_{L(MAX)}}\left[1 - \frac{V_{OUT}}{V_{IN(MAX)}}\right]$$

Channel 0 will require 0.41µH and channel 1 will require 0.28µH. Use a standard value of L = 0.4µH for channel 0 and L = 0.3µH for channel 1. At the nominal V_{IN} = 12V, the peak to peak inductor current ripple will be 7.72A (38.6%) for channel 0 and 7.2A (35.9%) for channel 1.

$$\Delta I_{L(NOM)} = \frac{V_{OUT}}{f \bullet L}\left[1 - \frac{V_{OUT}}{V_{IN(NOM)}}\right]$$

The peak inductor current will be the maximum DC value plus one-half the ripple current or 23.9A for channel 0 and 23.6A for channel 1. The minimum on time occurs on channel 1 at the maximum V_{IN}, and should not be less than 90ns:

$$t_{ON(MIN)} = \frac{V_{OUT}}{V_{IN(MAX)} \bullet f} = \frac{1.5V}{20V \bullet 425kHz} = 118ns$$

The next design focuses on Channel1 only.

The Coiltronics/Eaton FP1007R3-R30-R 0.3µH (0.29mΩ DCR at 20°C) is used for channel 1. So IOUT_CAL_GAIN = 0.29mΩ.

Based on the output current and inductor value, it is considered to be a perfect example of low DCR application.

Set: MFR_PWM_MODE[2] = 1 (Ultralow DCR)

then choose C = 220nF,

$$R1 = \frac{L}{DCR \bullet C \bullet 5} = \frac{0.30\mu H}{0.29m\Omega \bullet 220nF \bullet 5} = 940.4\Omega$$

Choose R1 = 931Ω (standard value, 1% tolerance resistor).

The maximum power loss in R1 is related to the duty cycle, and will occur in continuous conduction mode at the maximum input voltage:

$$P_{LOSSR1} = \frac{\left(V_{IN(MAX)} - V_{OUT}\right) \bullet V_{OUT}}{R1} = \frac{(20-1) \bullet 1.5}{931} = 20.4mW$$

The current limit will be set 30% higher than the peak value to assure variation in components and noise in the system do not limit the average current.

V_{ILIMIT} = (1 + 30%) • I_{PEAK} • $R_{DCR(MAX)}$

= (1 + 30%) • 23.6A • 0.29mΩ = 8.9mV

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Based on Figure 26, set MFR_PWM_MODE[1] = 1(low V_{OUT} range), MFR_PWM_MODE[2] = 1, (ultralow DCR) and MFR_PWM_MODE[7] = 0 (low current range) and IOUT_CAL_GAIN = 0.29mΩ in GUI.

Enter IOUT_OC_FAULT_LIMIT = 30.69A, the LTC7132 will automatically set the current limit to 29.62A, based on the IOUT_FAULT_LIMIT table, (see PMBus command for details).

ADDITIONAL DESIGN CHECKS

Tie $\overline{FAULT0}$ and $\overline{FAULT1}$ together and pull up to V_{DD33} with a 10k resistor. Tie RUN0 and RUN1 together and pull up to V_{DD33} with a 10k resistor.

If there are other ADI PSM parts, connect the RUN pins between chips and connect the $\overline{FAULT}$ pins between chips. Be sure all PMBus pins have resistor pull-up to V_{DD33} and connect these inputs across all ADI PSM parts in the application.

Tie SHARE_CLK high with a 4.99k resistor to V_{DD33} and share between all ADI PSM parts in the application. Be sure a unique address for each chip can be decoded with the ASEL0 and ASEL1 pins. Refer to Table 6. For maximum flexibility, allow board space for R_{TOP} and R_{BOTTOM} for any parameter that is set with resistors such as ASEL0 and ASEL1.

CONNECTING THE USB TO I²C/SMBus/PMBus CONTROLLER TO THE LTC7132 IN SYSTEM

The ADI USB-to-I²C/SMBus/PMBus adapter (DC1613A or equivalent) can be interfaced to the LTC7132 on the user's board for programming, telemetry and system debug. The adapter, when used in conjunction with LTpowerPlay, provides a powerful way to debug an entire power system. Faults are quickly diagnosed using telemetry, fault status commands and the fault log. The final configuration can be quickly developed and stored to the LTC7132 EEPROM. Figure 46 illustrates the application schematic for powering, programming and communication with one or more LTC7132s via the ADI I²C/SMBus/PMBus adapter regardless of whether or not system power is present. If system power is not present the dongle will power the

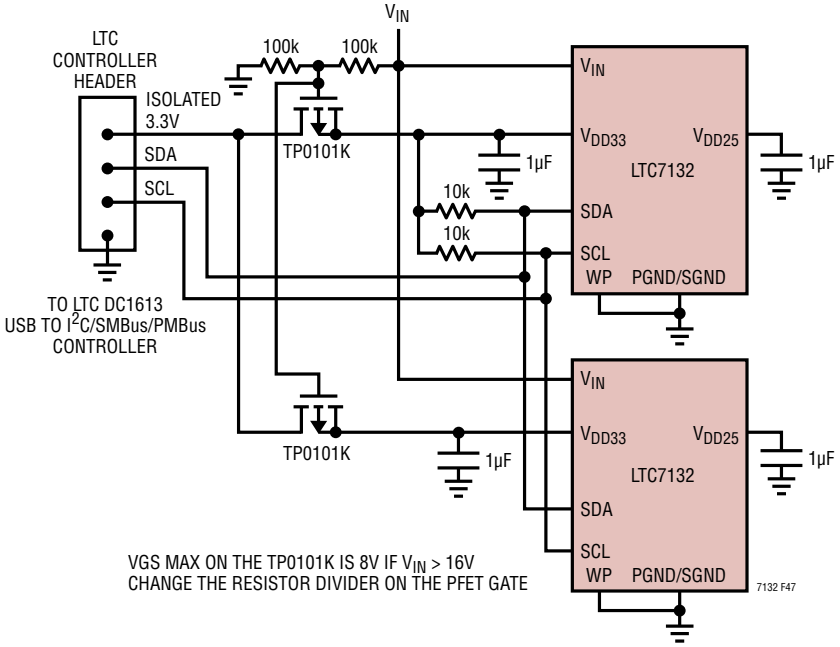

Figure 46. Controller Connection

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LTC7132 through the V_{DD33} supply pin. To initialize the part when V_{IN} is not applied and the V_{DD33} pin is powered use global address 0x5B command 0xBD data 0x2B followed by address 0x5B command 0xBD data 0xC4.The LTC7132 can now communicate with, and the project file can be updated. To write the updated project file to the NVM issue a STORE_USER _ALL command. When V_{IN} is applied, a MFR_RESET must be issued to allow the PWM to be enabled and valid ADCs to be read.

Because of the adapter's limited current sourcing capability, only the LTC7132s, their associated pull-up resistors and the I^2C pull-up resistors should be powered from the ORed 3.3V supply. In addition any device sharing the I^2C bus connections with the LTC7132 should not have body diodes between the SDA/SCL pins and their respective V_{DD} node because this will interfere with bus communication in the absence of system power. If V_{IN} is applied, the DC1613A will not supply the power to the LTC7132s on the board. It is recommended the RUN*n* pins be held low or no voltage configuration resistors inserted to avoid providing power to the load until the part is fully configured.

The LTC7132 is fully isolated from the host PC's ground by the DC1613A.The 3.3V from the adapter and the LTC7132 V_{DD33} pin must be driven to each LTC7132 with a separate PFET. If both V_{IN} and $EXTV_{CC}$ are not applied, the V_{DD33} pins can be in parallel because the on-chip LDO is off. The controller 3.3V current limit is 100mA but typical V_{DD33} currents are under 15mA. The V_{DD33} does back drive the $INTV_{CC}/EXTV_{CC}$ pin. Normally this is not an issue if V_{IN} is open.

LTpowerPlay: AN INTERACTIVE GUI FOR DIGITAL POWER

LTpowerPlay (Figure 47) is a powerful Windows-based development environment that supports Analog Devices digital power system management ICs including the LTC7132. The software supports a variety of different tasks. LTpowerPlay can be used to evaluate Analog Devices ICs by connecting to a demo board or the user application. LTpowerPlay can also be used in an offline mode (with no hardware present) in order to build multiple IC configuration files that can be saved and reloaded at a later time. LTpowerPlay provides unprecedented diagnostic and debug features. It becomes a valuable diagnostic tool during board bring-up to program or tweak the power system or to diagnose power issues when bring up rails. LTpowerPlay utilizes Analog Devices' USB-to-I^2C/SMBus/PMBus adapter to communication with one of the many potential targets including the DC2165A demo board, the DC2666A socketed programming board, or a customer target system. The software also provides an automatic update feature to keep the revisions current with the latest set of device drivers and documentation.

A great deal of context sensitive help is available with LTpower Play along with several tutorial demos. Complete information is available at:

www.analog.com/en/design-center/ltpower-play

PMBus COMMUNICATION AND COMMAND PROCESSING

The LTC7132 has a one deep buffer to hold the last data written for each supported command prior to processing as shown in Figure 48, Write Command Data Processing. When the part receives a new command from the bus, it copies the data into the Write Command Data Buffer, indicates to the internal processor that this command data needs to be fetched, and converts the command to its internal format so that it can be executed. Two distinct parallel blocks manage command buffering and command processing (fetch, convert, and execute) to ensure the last data written to any command is never lost. Command data buffering handles incoming PMBus writes by storing the command data to the Write Command Data Buffer and marking these commands for future processing. The internal processor runs in parallel and handles the sometimes slower task of fetching, converting and executing commands marked for processing. Some computationally intensive commands (e.g., timing parameters, temperatures, voltages and currents) have internal processor execution times that may be long relative to PMBus timing. If the part is busy processing a command, and new command(s) arrive, execution may be delayed or processed in a different order than received. The part

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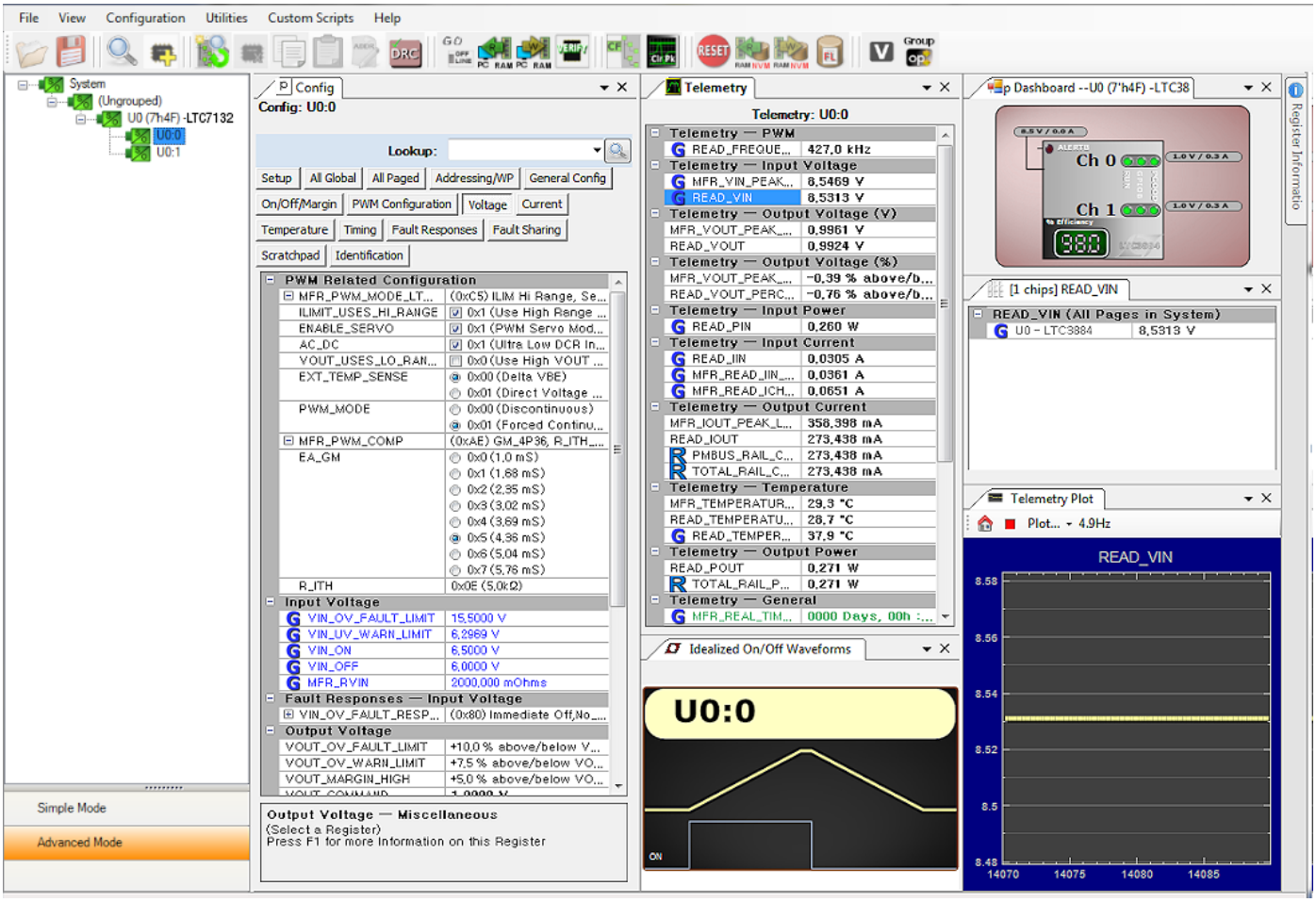

Figure 47. LTpowerPlay Screen Shot

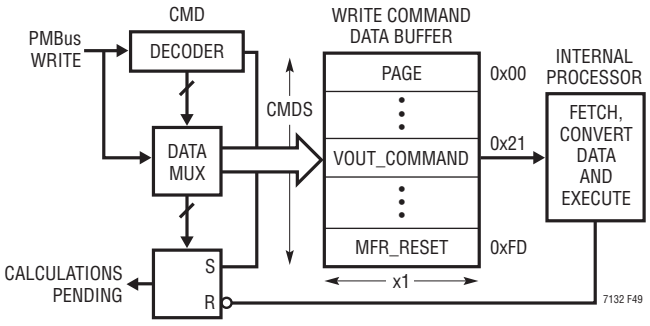

Figure 48. Write Command Data Processing

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```
// wait until chip is not busy
do
{
mfrCommonValue = PMBUS_READ_BYTE(0xEF);
partReady = (mfrCommonValue & 0x68) == 0x68;
}while(!partReady)
// now the part is ready to receive the next command
PMBUS_WRITE_WORD(0x21, 0x2000); //write VOUT_COMMAND to 2V
```

Figure 50. Example of a Command Write of VOUT_COMMAND

indicates when internal calculations are in process via bit 5 of MFR_COMMON ('calculations not pending'). When the part is busy calculating, bit 5 is cleared. When this bit is set, the part is ready for another command. An example polling loop is provided in Figure 50 which ensures that commands are processed in order while simplifying error handling routines.

When the part receives a new command while it is busy, it will communicate this condition using standard PMBus protocol. Depending on part configuration it may either NACK the command or return all ones (0xFF) for reads. It may also generate a BUSY fault and $\overline{\text{ALERT}}$ notification, or stretch the SCL clock low. For more information refer to PMBus Specification v1.1, Part II, Section 10.8.7 and SMBus v2.0 section 4.3.3. Clock stretching can be enabled by asserting bit 1 of MFR_CONFIG_ ALL. Clock stretching will only occur if enabled and the bus communication speed exceeds 100kHz.

PMBus busy protocols are well accepted standards, but can make writing system level software somewhat complex. The part provides three 'hand shaking' status bits which reduce complexity while enabling robust system level communication.

The three hand shaking status bits are in the MFR_COMMON register. When the part is busy executing an internal operation, it will clear bit 6 of MFR_COMMON ('chip not busy'). When the part is busy specifically because it is in a transitional V_{OUT} state (margining hi/lo, power off/on, moving to a new output voltage set point, etc.) it will clear bit 4 of MFR_COMMON ('output not in transition'). When internal calculations are in process, the part will clear bit 5 of MFR_COMMON ('calculations not pending'). These three status bits can be polled with a PMBus read byte of the MFR_COMMON register until all three bits are set. A command immediately following the status bits being set will be accepted without NACKing or generating a BUSY fault/$\overline{\text{ALERT}}$ notification. The part can NACK commands for other reasons, however, as required by the PMBus spec (for instance, an invalid command or data). An example of a robust command write algorithm for the VOUT_COMMAND register is provided in Figure 50.

It is recommended that all command writes (write byte, write word, etc.) be preceded with a polling loop to avoid the extra complexity of dealing with busy behavior and unwanted ALERT notification. A simple way to achieve this is to create a SAFE_WRITE_BYTE() and SAFE_WRITE_WORD() subroutine. The above polling mechanism allows your software to remain clean and simple while robustly communicating with the part. For a detailed discussion of these topics and other special cases please refer to the application note section located at:

www.analog.com/en/education.html

When communicating using bus speeds at or below 100kHz, the polling mechanism shown here provides a simple solution that ensures robust communication without clock stretching. At bus speeds in excess of 100kHz, it is strongly recommended that the part be configured to enable clock stretching. This requires a PMBus master that supports clock stretching. System software that detects and properly recovers from the standard PMBus NACK/BUSY faults as described in the PMBus Specification v1.1, Part II, Section 10.8.7 is required to communicate: the LTC7132 is not recommended in applications with bus speeds in excess of 400kHz.

PMBus COMMAND DETAILS

ADDRESSING AND WRITE PROTECT

COMMAND NAME	CMD CODE	DESCRIPTION	TYPE	PAGED	DATA FORMAT	UNITS	NVM	DEFAULT VALUE
PAGE	0x00	Provides integration with multi-page PMBus devices.	R/W Byte	N	Reg			0x00
PAGE_PLUS_WRITE	0x05	Write a supported command directly to a PWM channel.	W Block	N				
PAGE_PLUS_READ	0x06	Read a supported command directly from a PWM channel.	Block R/W	N				
WRITE_PROTECT	0x10	Level of protection provided by the device against accidental changes.	R/W Byte	N	Reg		Y	0x00
MFR_ADDRESS	0xE6	Sets the 7-bit I^2C address byte.	R/W Byte	N	Reg		Y	0x4F
MFR_RAIL_ADDRESS	0xFA	Common address for PolyPhase outputs to adjust common parameters.	R/W Byte	Y	Reg		Y	0x80

PAGE

The PAGE command provides the ability to configure, control and monitor both PWM channels through only one physical address, either the MFR_ADDRESS or GLOBAL device address. Each PAGE contains the operating commands for one PWM channel.

Pages 0x00 and 0x01 correspond to Channel 0 and Channel 1, respectively, in this device.

Setting PAGE to 0xFF applies any following paged commands to both outputs. With PAGE set to 0xFF the LTC7132 will respond to read commands as if PAGE were set to 0x00 (Channel 0 results).

This command has one data byte.

PAGE_PLUS_WRITE

The PAGE_PLUS_WRITE command provides a way to set the page within a device, send a command, and then send the data for the command, all in one communication packet. Commands allowed by the present write protection level may be sent with PAGE_PLUS_WRITE.

The value stored in the PAGE command is not affected by PAGE_PLUS_WRITE. If PAGE_PLUS_WRITE is used to send a non-paged command, the Page Number byte is ignored.

This command uses Write Block protocol. An example of the PAGE_PLUS_WRITE command with PEC sending a command that has two data bytes is shown in Figure 50.

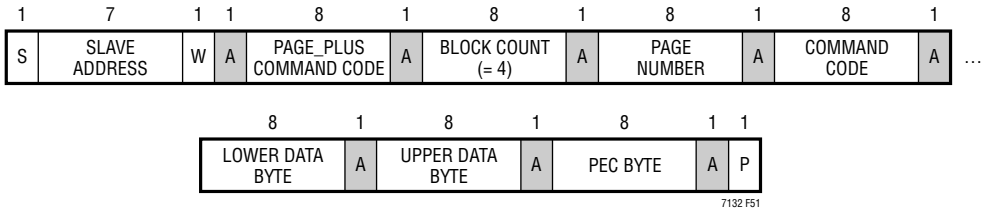

Figure 50. Example of PAGE_PLUS_WRITE

PMBus COMMAND DETAILS

PAGE_PLUS_READ

The PAGE_PLUS_READ command provides the ability to set the page within a device, send a command, and then read the data returned by the command, all in one communication packet .

The value stored in the PAGE command is not affected by PAGE_PLUS_READ. If PAGE_PLUS_READ is used to access data from a non-paged command, the Page Number byte is ignored.

This command uses the Process Call protocol. An example of the PAGE_PLUS_READ command with PEC is shown in Figure 51.

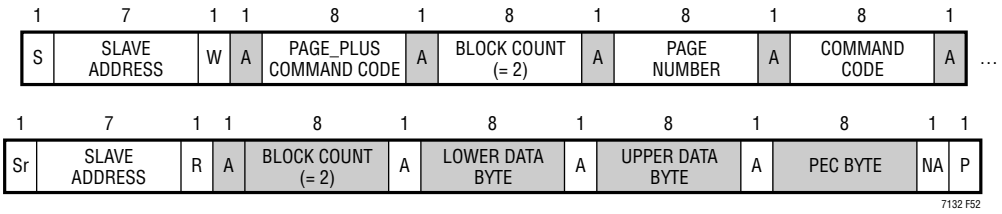

Figure 51. Example of PAGE_PLUS_READ

Note: PAGE_PLUS commands cannot be nested. A PAGE_PLUS command cannot be used to read or write another PAGE_PLUS command. If this is attempted, the LTC7132 will NACK the entire PAGE_PLUS packet and issue a CML fault for Invalid/Unsupported Data.

WRITE_PROTECT

The WRITE_PROTECT command is used to control writing to the LTC7132 device. This command does not indicate the status of the WP pin which is defined in the MFR_COMMON command. The WP pin takes precedence over the value of this command.

BYTE	MEANING
0x80	Disable all writes except to the WRITE_PROTECT, PAGE, MFR_EE_UNLOCK, and STORE_USER_ALL commands.
0x40	Disable all writes except to the WRITE_PROTECT, PAGE, MFR_EE_UNLOCK, MFR_CLEAR_PEAKS, STORE_USER_ALL, OPERATION and CLEAR_FAULTS command. Individual fault bits can be cleared by writing a 1 to the respective bits in the STATUS commands.
0x20	Disable all writes except to the WRITE_PROTECT, OPERATION, MFR_EE_UNLOCK, MFR_CLEAR_PEAKS, CLEAR_FAULTS, PAGE, ON_OFF_CONFIG, VOUT_COMMAND and STORE_USER_ALL. Individual fault bits can be cleared by writing a 1 to the respective bits in the STATUS commands.
0x10	Reserved, must be 0
0x08	Reserved, must be 0
0x04	Reserved, must be 0
0x02	Reserved, must be 0
0x01	Reserved, must be 0

Enable writes to all commands when WRITE_PROTECT is set to 0x00.

If WP pin is high, PAGE, OPERATION, MFR_CLEAR_PEAKS, MFR_EE_UNLOCK, WRITE_PROTECT and CLEAR_FAULTS commands are supported. Individual fault bits can be cleared by writing a 1 to the respective bits in the STATUS commands.

PMBus COMMAND DETAILS

MFR_ADDRESS

The MFR_ADDRESS command byte sets the 7 bits of the PMBus slave address for this device.

Setting this command to a value of 0x80 disables device addressing. The GLOBAL device address, 0x5A and 0x5B, cannot be deactivated. If RCONFIG is set to ignore, the ASEL0 and ASEL1 pins are still used to determine the LSB and MSB, respectively, of the channel address. If the ASEL0 and ASEL1 pins are both open, the LTC7132 will use the address value stored in NVM. If the ASEL0 pin is open, the LTC7132 will use the lower 4 bits of the MFR_ADDRESS value stored in NVM to construct the effective address of the part. If the ASEL1 pin is open, the LTC7132 will use the upper 4 bits of the MFR_ADDRESS value stored in NVM to construct the effective address of the part.

This command has one data byte.

MFR_RAIL_ADDRESS

The MFR_RAIL_ADDRESS command enables direct device address access to the PAGE activated channel. The value of this command should be common to all devices attached to a single power supply rail.

The user should only perform command writes to this address. If a read is performed from this address and the rail devices do not respond with EXACTLY the same value, the LTC7132 will detect bus contention and may set a CML communications fault.

Setting this command to a value of 0x80 disables rail device addressing for the channel.

This command has one data byte.

GENERAL CONFIGURATION COMMANDS

COMMAND NAME	CMD CODE	DESCRIPTION	TYPE	PAGED	DATA FORMAT	UNITS	NVM	DEFAULT VALUE
MFR_CHAN_CONFIG	0xD0	Configuration bits that are channel specific.	R/W Byte	Y	Reg		Y	0x10
MFR_CONFIG_ALL	0xD1	General configuration bits.	R/W Byte	N	Reg		Y	0x21

MFR_CHAN_CONFIG

General purpose configuration command common to multiple ADI products.

BIT	MEANING
7	Reserved
6	Reserved
5	Reserved
4	Disable RUN Low. When asserted the RUN pin is not pulsed low if commanded OFF.
3	Enable Short Cycle recognition if this bit is set to a 1.
2	SHARE_CLOCK control. If SHARE_CLOCK is held low, the output is disabled.
1	No $\overline{\text{FAULT}}$ $\overline{\text{ALERT}}$, $\overline{\text{ALERT}}$ is not pulled low if $\overline{\text{FAULT}}$ is pulled low externally. Assert this bit if either POWER_GOOD or VOUT_UVUF are propagated on $\overline{\text{FAULT}}$.
0	Disables the V_{OUT} decay value requirement for MFR_RETRY_TIME and $t_{OFF(MIN)}$ processing. When this bit is set to a 0, the output must decay to less than 12.5% of the programmed value for any action that turns off the rail including a fault, an OFF/ON command, or a toggle of RUN from high to low to high.

This command has one data byte.

PMBus COMMAND DETAILS

A ShortCycle event occurs whenever the PWM channel is commanded back ON, or reactivated, after the part has been commanded OFF and is processing either the TOFF_DELAY or the TOFF_FALL states. The PWM channel can be turned ON and OFF through either the RUN pin and or the PMBus OPERATION command.

If the PWM channel is reactivated during the TOFF_DELAY, the part will perform the following:

1. Immediately tri-state the PWM channel output;
2. Start the retry delay timer as specified by the $t_{OFF(MIN)}$.
3. After the $t_{OFF(MIN)}$ value has expired, the PWM channel will proceed to the TON_DELAY state and the STATUS_MFR_SPECIFIC bit #1 will assert.

If the PWM channel is reactivated during the TOFF_FALL, the part will perform the following:

1. Stop ramping down the PWM channel output;
2. Immediately tri-state the PWM channel output;
3. Start the retry delay timer as specified by the $t_{OFF(MIN)}$.
4. After the $t_{OFF(MIN)}$ value has expired, the PWM channel will proceed to the TON_DELAY state and the STATUS_MFR_SPEFIFIC bit #1 will assert.

If the ShortCycle event occurs and the ShortCycle MFR_CHAN_CONFIG bit is not set, the PWM channel state machine will complete its TOFF_DELAY and TOFF_FALL operations as previously commanded by the user.

MFR_CONFIG_ALL

General purpose configuration command common to multiple ADI products.

BIT	MEANING
7	Enable Fault Logging
6	Ignore Resistor Configuration Pins
5	Mask PMBus, Part II, Section 10.9.1 Violations
4	Disable SYNC output
3	Enable 255ms PMBus timeout
2	PMBus command writes require a valid Packet Error Checking, PEC to be accepted.*
1	Enable the use of PMBus clock stretching
0	Execute CLEAR_FAULTS on rising edge of either RUN pin.

*PMBus command writes that have a valid PEC byte are always processed. PMBus command writes that have an invalid PEC byte are not processed and set a CML status fault.

This command has one data byte.

ON/OFF/MARGIN

COMMAND NAME	CMD CODE	DESCRIPTION	TYPE	PAGED	DATA FORMAT	UNITS	NVM	DEFAULT VALUE
ON_OFF_CONFIG	0x02	RUN pin and PMBus bus on/off command configuration.	R/W Byte	Y	Reg		Y	0x1E
OPERATION	0x01	Operating mode control. On/off, margin high and margin low.	R/W Byte	Y	Reg		Y	0x80
MFR_RESET	0xFD	Commanded reset without requiring a power-down.	Send Byte	N				NA

PMBus COMMAND DETAILS

ON_OFF_CONFIG

The ON_OFF_CONFIG command specifies the combination of RUN*n* pin input state and PMBus commands needed to turn the PWM channel on and off.

Supported Values:

VALUE	MEANING
0x1F	OPERATION value and RUN*n* pin must both command the device to start/run. Device executes immediate off when commanded off.
0x1E	OPERATION value and RUN*n* pin must both command the device to start/run. Device uses TOFF_ command values when commanded off.
0x17	RUN*n* pin control with immediate off when commanded off. OPERATION on/off control ignored.
0x16	RUN*n* pin control using TOFF_ command values when commanded off. OPERATION on/off control ignored.

Programming an unsupported ON_OFF_CONFIG value will generate a CML fault and the command will be ignored.

This command has one data byte.

OPERATION

The OPERATION command is used to turn the unit on and off in conjunction with the input from the RUN*n* pins. It is also used to cause the unit to set the output voltage to the upper or lower MARGIN VOLTAGEs. The unit stays in the commanded operating mode until a subsequent OPERATION command or change in the state of the RUN*n* pin instructs the device to change to another mode. If the part is stored in the MARGIN_LOW/HIGH state, the next RESET or POWER_ON cycle will ramp to that state. If the OPERATION command is modified, for example ON is changed to MARGIN_LOW, the output will move at a fixed slope set by the VOUT_TRANSITION_RATE. The default operation command is sequence off. If V_{IN} is applied to a part with factory default programming and the VOUT_CONFIG resistor configuration pins are not installed, the outputs will be commanded off.

The part defaults to the Sequence Off state.

This command has one data byte.

Supported Values:

VALUE	MEANING
0xA8	Margin high.
0x98	Margin low.
0x80	On (V_{OUT} back to nominal even if bit 3 of ON_OFF_CONFIG is not set).
0x40*	Soft off (with sequencing).
0x00*	Immediate off (no sequencing).

*Device does not respond to these commands if bit 3 of ON_OFF_CONFIG is not set.

Programming an unsupported OPERATION value will generate a CML fault and the command will be ignored.

This command has one data byte.

MFR_RESET

This command provides a means to reset the LTC7132 from the serial bus. This forces the LTC7132 to turn off both PWM channels, load the operating memory from internal EEPROM, clear all faults and then perform a soft-start of both PWM channels, if enabled.

This write-only command has no data bytes.

PMBus COMMAND DETAILS

PWM CONFIGURATION

COMMAND NAME	CMD CODE	DESCRIPTION	TYPE	PAGED	DATA FORMAT	UNITS	NVM	DEFAULT VALUE
MFR_PWM_COMP	0xD3	PWM loop compensation configuration	R/W Byte	Y	Reg		Y	0xAE
MFR_PWM_MODE	0xD4	Configuration for the PWM engine.	R/W Byte	Y	Reg		Y	0xC7
MFR_PWM_CONFIG	0xF5	Set numerous parameters for the DC/DC controller including phasing.	R/W Byte	N	Reg		Y	0x10
FREQUENCY_SWITCH	0x33	Switching frequency of the controller.	R/W Word	N	L11	kHz	Y	425 0xFB52

MFR_PWM_MODE

The MFR_PWM_MODE command sets important PWM controls for each channel.

The MFR_PWM_MODE command allows the user to program the PWM controller to use discontinuous (pulse-skipping mode), or forced continuous conduction mode.

BIT	MEANING
7	Use High Range of I_{LIMIT}
0b	Low Current Range
1b	High Current Range
6	Enable Servo Mode
5	External temperature sense:
	0: ΔV_{BE} measurement.
	1: Direct voltage measurement.
[4:3]	Reserved
2	Enable ultra-low DCR current sense
1	V_{OUT} Range
1b	The maximum output voltage is 2.75V
0b	The maximum output voltage is 5.5V
Bit[0]	Mode
0b	Discontinuous
1b	Forced Continuous

Bit [7] of this command determines if the part is in high range or low range of the IOUT_OC_FAULT_LIMIT command. Changing this bit value changes the PWM loop gain and compensation. This bit value should not be changed when the channel output is active. Writing this bit when the channel is active will generate a CML fault.

Bit [6] The LTC7132 will not servo while the part is OFF, ramping on or ramping off. When set to a one, the output servo is enabled. The output set point DAC will be slowly adjusted to minimize the difference between the READ_VOUT_ADC and the VOUT_COMMAND (or the appropriate margined value).

When Bit[5] is cleared, the LTC7132 computes temperature in °C from ΔV_{BE} measured by the ADC at the TSNS*n* pin as

$$T = (G \bullet \Delta V_{BE} \bullet q/(K \bullet \ln(16))) - 273.15 + O$$

When Bit[5] is set, the LTC7132 computes temperature in °C from TSNS*n* voltage measured by the ADC as

$$T = (G \bullet (1.35 - V_{TSNSn} + O)/4.3e\text{-}3) + 25$$

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For both equations,

G = MFR_TEMP_1_GAIN • 2^{-14}, and

O = MFR_TEMP_1_OFFSET

K = 1.381 • 10^{-23}J/K

q = 1.602 • 10^{-19}C

Bit[2] determines if the part uses ultralow DCR for sensing the output current. This is a very critical selection in terms of overcurrent limit. It is highly recommend that Bit[2] should not be changed when device is in operation.

Bit[1] of this command determines if the part is in high range or low voltage range. Changing this bit value changes the PWM loop gain and compensation. This bit value should not be changed when the channel output is active. Writing this bit when the channel is active will generate a CML fault.

Bit[0] determines if the PWM mode of operation is discontinuous (pulse-skipping mode), or forced continuous conduction mode. Whenever the channel is ramping on, the PWM mode will be discontinuous, regardless of the value of this bit. This command has one data byte.

MFR_PWM_COMP

The MFR_PWM_COMP command sets the g_m of the PWM channel error amplifiers and the value of the internal R_{ITHn} compensation resistors. This command affects the loop gain of the PWM output which may require modifications to the external compensation network.

BIT	MEANING
BIT [7:5]	**Error Amplifier GM Adjust (mS)**
000b	0.8
001b	1.3
010b	1.9
011b	2.4
100b	2.9
101b	3.5
110b	4.0
111b	4.6
BIT [4:0]	**R_{ITH} (kΩ)**
00000b	0
00001b	0.25
00010b	0.5
00011b	0.75
00100b	1
00101b	1.25
00110b	1.5
00111b	1.75
01000b	2
01001b	2.5
01010b	3
01011b	3.5
01100b	4
01101b	4.5

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01110b	5
01111b	5.5
10000b	6
10001b	7
10010b	8
10011b	9
10100b	11
10101b	13
10110b	15
10111b	17
11000b	20
11001b	24
11010b	28
11011b	32
11100b	38
11101b	46
11110b	54
11111b	62

This command has one data byte.

MFR_PWM_CONFIG

The MFR_PWM_CONFIG command sets the switching frequency phase offset with respect to the falling edge of the SYNC signal. The part must be in the OFF state to process this command. Either the RUN pins must be low or the channels must be commanded off. If either channel is in the RUN state and this command is written, the command will be NACK'd and a BUSY fault will be asserted.

BIT	MEANING	
7	Reserved	
[6:5]	Input current sense gain.	
00b	2x gain. 0mV to 50mV range.	
01b	4x gain. 0mV to 20mV range.	
10b	8x gain. 0mV to 5mV range.	
11b	Reserved	
4	Share Clock Enable : If this bit is 1, the SHARE_CLK pin will not be released until V_{IN} > VIN_ON. The SHARE_CLK pin will be pulled low when V_{IN} < VIN_OFF. If this bit is 0, the SHARE_CLK pin will not be pulled low when VIN < VIN_OFF except for the initial application of VIN.	
BIT [2:0]	**CHANNEL 0 (DEGREES)**	**CHANNEL 1 (DEGREES)**
000b	0	180
001b	90	270
010b	0	240
011b	0	120
100b	120	240
101b	60	240
110b	120	300

PMBus COMMAND DETAILS

FREQUENCY_SWITCH

The FREQUENCY_SWITCH command sets all switching frequencies between 250kHz to 1MHz.

The part must be in the OFF state to process this command. The RUN pin must be low or both channels must be commanded off. If the part is in the RUN state and this command is written, the command will be NACK'd and a BUSY fault will be asserted. When the part is commanded off and the frequency is changed, a PLL_UNLOCK status may be detected as the PLL locks onto the new frequency.

This command has two data bytes and is formatted in Linear_5s_11s format.

VOLTAGE

Input Voltage and Limits

COMMAND NAME	CMD CODE	DESCRIPTION	TYPE	PAGED	DATA FORMAT	UNITS	NVM	DEFAULT VALUE
VIN_OV_FAULT_LIMIT	0x55	Input supply overvoltage fault limit.	R/W Word	N	L11	V	Y	15.5 0xD3E0
VIN_UV_WARN_LIMIT	0x58	Input supply undervoltage warning limit.	R/W Word	N	L11	V	Y	6.3 0xCB26
VIN_ON	0x35	Input voltage at which the unit should start power conversion.	R/W Word	N	L11	V	Y	6.5 0xCB40
VIN_OFF	0x36	Input voltage at which the unit should stop power conversion.	R/W Word	N	L11	V	Y	6.0 0xCB00
MFR_RVIN	0xF7	The resistance value of the V_{IN} pin filter element in milliohms	R/W Word	N	L11	mΩ	Y	1000 0x03E8

VIN_OV_FAULT_LIMIT

The VIN_OV_FAULT_LIMIT command sets the value of the input voltage measured by the ADC, in volts, that causes an input overvoltage fault.

This command has two data bytes in Linear_5s_11s format.

VIN_UV_WARN_LIMIT

The VIN_UV_WARN_LIMIT command sets the value of input voltage measured by the ADC that causes an input under-voltage warning. This warning is disabled until the input exceeds the input startup threshold value set by the VIN_ON command and the unit has been enabled. If the V_{IN} Voltage drops below the VIN_OV_WARN_LIMIT the device:

- Sets the INPUT Bit Is the STATUS_WORD
- Sets the V_{IN} Undervoltage Warning Bit in the STATUS_INPUT Command
- Notifies the Host by Asserting $\overline{\text{ALERT}}$, unless Masked

VIN_ON

The VIN_ON command sets the input voltage, in Volts, at which the unit starts power conversion.

This command has two data bytes and is formatted in Linear_5s_11s format.

PMBus COMMAND DETAILS

VIN_OFF

The VIN_OFF command sets the input voltage, in Volts, at which the unit stops power conversion.

This command has two data bytes and is formatted in Linear_5s_11s format.

MFR_RVIN

The MFR_RVIN command is used to set the resistance value of the V_{IN} pin filter element in milliohms. (See also READ_VIN). Set MFR_RVIN equal to 0 if no filter element is used.

This command has two data bytes and is formatted in Linear_5s_11s format.

Output Voltage and Limits

COMMAND NAME	CMD CODE	DESCRIPTION	TYPE	PAGED	DATA FORMAT	UNITS	NVM	DEFAULT VALUE
VOUT_MODE	0x20	Output voltage format and exponent (2^{-12}).	R Byte	Y	Reg			2^{-12} 0x14
VOUT_MAX	0x24	Upper limit on the output voltage the unit can command regardless of any other commands.	R/W Word	Y	L16	V	Y	2.75 0x2C00
VOUT_OV_FAULT_ LIMIT	0x40	Output overvoltage fault limit.	R/W Word	Y	L16	V	Y	1.1 0x119A
VOUT_OV_WARN_ LIMIT	0x42	Output overvoltage warning limit.	R/W Word	Y	L16	V	Y	1.075 0x1133
VOUT_MARGIN_HIGH	0x25	Margin high output voltage set point. Must be greater than VOUT_COMMAND.	R/W Word	Y	L16	V	Y	1.05 0x10CD
VOUT_COMMAND	0x21	Nominal output voltage set point.	R/W Word	Y	L16	V	Y	1.0 0x1000
VOUT_MARGIN_LOW	0x26	Margin low output voltage set point. Must be less than VOUT_COMMAND.	R/W Word	Y	L16	V	Y	0.95 0x0F33
VOUT_UV_WARN_ LIMIT	0x43	Output undervoltage warning limit.	R/W Word	Y	L16	V	Y	0.925 0x0ECD
VOUT_UV_FAULT_ LIMIT	0x44	Output undervoltage fault limit.	R/W Word	Y	L16	V	Y	0.9 0x0E66
MFR_VOUT_MAX	0xA5	Maximum allowed output voltage.	R Word	Y	L16	V		5.7 0x5B33

VOUT_MODE

The data byte for VOUT_MODE command, used for commanding and reading output voltage, consists of a 3-bit mode (only linear format is supported) and a 5-bit parameter representing the exponent used in output voltage Read/Write commands.

This read-only command has one data byte.

VOUT_MAX

The VOUT_MAX command sets an upper limit on any voltage, including VOUT_MARGIN_HIGH, the unit can command regardless of any other commands or combinations. The maximum allowed value of this command is 5.8V. The maximum output voltage the LTC7132 can produce is 5.5V including VOUT_MARGIN_HIGH. However, the VOUT_OV_FAULT_LIMIT can be commanded as high as 5.7V.

This command has two data bytes and is formatted in Linear_16u format.

PMBus COMMAND DETAILS

VOUT_OV_FAULT_LIMIT

The VOUT_OV_FAULT_LIMIT command sets the value of the output voltage measured by the OV supervisor comparator at the sense pins, in volts, which causes an output overvoltage fault.

If the VOUT_OV_FAULT_LIMIT is modified and the part is in the RUN state, allow 10ms after the command is modified to assure the new value is being honored. The part indicates if it is busy making a calculation. Monitor bits 5 and 6 of MFR_COMMON. Either bit is low if the part is busy. If this wait time is not honored and the VOUT_COMMAND is modified above the old overvoltage limit, an OV condition might temporarily be detected resulting in undesirable behavior and possible damage to the switcher.

If VOUT_OV_FAULT_RESPONSE is set to OV_PULLDOWN or 0x00, the $\overline{\text{FAULT}}$ pin will not assert if VOUT_OV_FAULT is propagated. The LTC7132 will pull the TG low and assert the BG bit as soon as the overvoltage condition is detected.

This command has two data bytes and is formatted in Linear_16u format.

VOUT_OV_WARN_LIMIT

The VOUT_OV_WARN_LIMIT command sets the value of the output voltage measured by the ADC at the sense pins, in volts, which causes an output voltage high warning. The MFR_VOUT_PEAK value can be used to determine if this limit has been exceeded.

In response to the VOUT_OV_WARN_LIMIT being exceeded, the device:

- Sets the NONE_OF_THE_ABOVE bit in the STATUS_BYTE
- Sets the VOUT bit in the STATUS_WORD
- Sets the VOUT Overvoltage Warning bit in the STATUS_VOUT command
- Notifies the host by asserting $\overline{\text{ALERT}}$ pin, unless masked

This condition is detected by the ADC so the response time may be up to $t_{CONVERT}$.

This command has two data bytes and is formatted in Linear_16u format.

VOUT_MARGIN_HIGH

The VOUT_MARGIN_HIGH command loads the unit with the voltage to which the output is to be changed, in Volts, when the OPERATION command is set to “Margin High”. The value should be greater than VOUT_COMMAND. The maximum guaranteed value on VOUT_MARGIN_HIGH is 5.5V.

This command will not be acted on during TON_RISE and TOFF_FALL output sequencing. The VOUT_TRANSITION_RATE will be used if this command is modified while the output is active and in a steady-state condition.

This command has two data bytes and is formatted in Linear_16u format.

PMBus COMMAND DETAILS

VOUT_COMMAND

The VOUT_COMMAND consists of two bytes and is used to set the output voltage, in volts. The maximum guaranteed value on VOUT is 5.5V.

This command will not be acted on during TON_RISE and TOFF_FALL output sequencing. The VOUT_TRANSITION_RATE will be used if this command is modified while the output is active and in a steady-state condition.

This command has two data bytes and is formatted in Linear_16u format.

VOUT_MARGIN_LOW

The VOUT_MARGIN_LOW command loads the unit with the voltage to which the output is to be changed, in volts, when the OPERATION command is set to “Margin Low”. The value must be less than VOUT_COMMAND.

This command will not be acted on during TON_RISE and TOFF_FALL output sequencing. The VOUT_TRANSITION_RATE will be used if this command is modified while the output is active and in a steady-state condition.

This command has two data bytes and is formatted in Linear_16u format.

VOUT_UV_WARN_LIMIT

The VOUT_UV_ WARN_LIMIT command reads the value of the output voltage measured by the ADC at the sense pins, in volts, which causes an output voltage low warning.

In response to the VOUT_UV_WARN_LIMIT being exceeded, the device:

- Sets the NONE_OF_THE_ABOVE bit in the STATUS_BYTE
- Sets the VOUT bit in the STATUS_WORD
- Sets the VOUT Undervoltage Warning bit in the STATUS_VOUT command
- Notifies the host by asserting $\overline{\text{ALERT}}$ pin, unless masked

This command has two data bytes and is formatted in Linear_16u format.

VOUT_UV_FAULT_LIMIT

The VOUT_UV_FAULT_LIMIT command reads the value of the output voltage measured by the UV supervisor comparator at the sense pins, in volts, which causes an output undervoltage fault.

This command has two data bytes and is formatted in Linear_16u format.

MFR_VOUT_MAX

The MFR_VOUT_MAX command is the maximum output voltage in volts for each channel, including VOUT_OV_FAULT_LIMIT. If the output voltages are set to high range (Bit 1 of MFR_PWM_MODE set to a 0) MFR_VOUT_MAX is 5.5V. If the output voltage is set to low range (Bit 1 of MFR_PWM_MODE set to a 1) the MFR_VOUT_MAX is 2.75V. Entering a VOUT_COMMAND value greater than this will result in a CML fault and the output voltage setting will be clamped to the maximum level. This will also result in Bit 3 VOUT_MAX_Warning in the STATUS_VOUT command being set.

This read only command has 2 data bytes and is formatted in Linear_16u format.

PMBus COMMAND DETAILS

OUTPUT CURRENT AND LIMITS

COMMAND NAME	CMD CODE	DESCRIPTION	TYPE	PAGED	DATA FORMAT	UNITS	NVM	DEFAULT VALUE
IOUT_CAL_GAIN	0x38	The ratio of the voltage at the current sense pins to the sensed current. For devices using a fixed current sense resistor, it is the resistance value in mΩ.	R/W Word	Y	L11	mΩ	Y	0.32 0xAA8F
MFR_IOUT_CAL_GAIN_TC	0xF6	Temperature coefficient of the current sensing element.	R/W Word	Y	CF		Y	3900 0x0F3C
IOUT_OC_FAULT_LIMIT	0x46	Output overcurrent fault limit.	R/W Word	Y	L11	A	Y	45.0 0xE2D0
IOUT_OC_WARN_LIMIT	0x4A	Output overcurrent warning limit.	R/W Word	Y	L11	A	Y	34.0 0xE230

IOUT_CAL_GAIN

The IOUT_CAL_GAIN command is used to set the resistance value of the current sense resistor in milliohms. (see also MFR_IOUT_CAL_GAIN_TC).

This command has two data bytes and is formatted in Linear_5s_11s format.

MFR_IOUT_CAL_GAIN_TC

The MFR_IOUT_CAL_GAIN_TC command allows the user to program the temperature coefficient of the IOUT_CAL_GAIN sense resistor or inductor DCR in ppm/°C.

This command has two data bytes and is formatted in 16-bit 2's complement integer ppm. N = –32768 to 32767 • 10^{-6}. Nominal temperature is 27°C. The IOUT_CAL_GAIN is multiplied by:

[1.0 + MFR_IOUT_CAL_GAIN_TC • (READ_TEMPERATURE_1-27)].

DCR sensing will have a typical value of 3900.

The IOUT_CAL_GAIN and MFR_IOUT_CAL_GAIN_TC impact all current parameters including: READ_IOUT, MFR_IOUT_PEAK, IOUT_OC_FAULT_LIMIT and IOUT_OC_WARN_LIMIT.

IOUT_OC_FAULT_LIMIT

The IOUT_OC_FAULT_LIMIT command sets the value of the peak output current limit, in Amperes. When the controller is in current limit, the overcurrent detector will indicate an overcurrent fault condition. The following table lists the progammable peak output current limit value in mV between I_{SENSE}^+ and I_{SENSE}^-. The actual value of current limit is ($I_{SENSE}^+ – I_{SENSE}^-$)/IOUT_CAL_GAIN in Amperes.

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CODE	MFR_PWM_MODE[2] = 1 (Sub-milli Ω DCR) RC = L/(5 • DCR)		MFR_PWM_MODE[2] = 0 (Normal Value of DCR) RC = L/(DCR)	
	MFR_PWM_MODE[7]=1 High Current Range V_{ILIMIT} (mV)	MFR_PWM_MODE[7]=0 Low Current Range V_{ILIMIT} (mV)	MFR_PWM_MODE[7]=1 High Current Range V_{ILIMIT} (mV)	MFR_PWM_MODE[7]=0 Low Current Range V_{ILIMIT} (mV)
0000	15.45	8.59	38.64	21.46
0001	16.59	9.22	41.48	23.04
0010	17.73	9.85	44.32	24.62
0011	18.86	10.48	47.16	26.20
0100	20.42	11.34	51.04	28.36
0101	21.14	11.74	52.84	29.36
0110	22.27	12.37	55.68	30.93
0111	23.41	13.01	58.52	32.51
1000	24.55	13.64	61.36	34.09
1001	25.68	14.27	64.20	35.67
1010	26.82	14.90	67.05	37.25
1011	27.95	15.53	69.89	38.83
1100	29.5	16.5	74.5	41.38
1101	30.23	16.79	75.57	41.98
1110	31.36	17.42	78.41	43.56
1111	32.50	18.06	81.25	45.14

Note: V_{ILIMIT} values used to calculate IOUT_OC_FAULT_LIMIT.

Note: This is the peak of the current waveform. The READ_IOUT command returns the average current. The peak output current limits are adjusted with temperature based on the MFR_IOUT_CAL_GAIN_TC using the equation:

Peak Current Limit = IOUT_CAL_GAIN • (1 + MFR_IOUT_CAL_GAIN_TC • (READ_TEMPERTURE_1-27.0)).

The LTC7132 automatically converts currents to the appropriate internal bit value.

The IOUT range is set with bit 7 of the MFR_PWM_MODE command.

The IOUT_OC_FAULT_LIMIT is ignored during TON_RISE and TOFF_FALL.

If the IOUT_OC_FAULT_LIMIT is exceeded, the device:

- Sets the IOUT bit in the STATUS word
- Sets the IOUT Overcurrent fault bit in the STATUS_IOUT
- Notifies the host by asserting $\overline{\text{ALERT}}$, unless masked

This command has two data bytes and is formatted in Linear_5s_11s format.

IOUT_OC_WARN_LIMIT

This command sets the value of the output current measured by the ADC that causes an output overcurrent warning in Amperes. The READ_IOUT value will be used to determine if this limit has been exceeded.

In response to the IOUT_OC_WARN_LIMIT being exceeded, the device:

- Sets the NONE_OF_THE_ABOVE bit in the STATUS_BYTE
- Sets the IOUT bit in the STATUS_WORD
- Sets the IOUT Overcurrent Warning bit in the STATUS_IOUT command, and

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• Notifies the host by asserting $\overline{\text{ALERT}}$ pin, unless masked

The IOUT_OC_FAULT_LIMIT is ignored during TON_RISE and TOFF_FALL.

This command has two data bytes and is formatted in Linear_5s_11s format

Input Current and Limits

COMMAND NAME	CMD CODE	DESCRIPTION	TYPE	DATA FORMAT	UNITS	NVM	DEFAULT VALUE
MFR_IIN_CAL_GAIN	0xE8	The resistance value of the input current sense element in mΩ.	R/W Word	L11	mΩ	Y	5.000 0xCA80

MFR_IIN_CAL_GAIN

The MFR_IIN_CAL_GAIN command is used to set the resistance value of the input current sense resistor in milliohms. (see also READ_IIN).

This command has two data bytes and is formatted in Linear_5s_11s format.

COMMAND NAME	CMD CODE	DESCRIPTION	TYPE	PAGED	DATA FORMAT	UNITS	NVM	DEFAULT VALUE
IIN_OC_WARN_LIMIT	0x5D	Input overcurrent warning limit.	R/W Word	N	L11	A	Y	10.0 0xD280

IIN_OC_WARN_LIMIT

The IIN_OC_WARN_LIMIT command sets the value of the input current measured by the ADC, in amperes, that causes a warning indicating the input current is high. The READ_IIN value will be used to determine if this limit has been exceeded.

In response to the IIN_OC_WARN_LIMIT being exceeded, the device:

• Sets the OTHER bit in the STATUS_BYTE

• Sets the INPUT bit in the upper byte of the STATUS_WORD

• Sets the IIN Overcurrent Warning bit[1] in the STATUS_INPUT command, and

• Notifies the host by asserting $\overline{\text{ALERT}}$ pin

This command has two data bytes and is formatted in Linear_5s_11s format.

TEMPERATURE

External Temperature Calibration

COMMAND NAME	CMD CODE	DESCRIPTION	TYPE	PAGED	DATA FORMAT	UNITS	NVM	DEFAULT VALUE
MFR_TEMP_1_GAIN	0xF8	Sets the slope of the external temperature sensor.	R/W Word	Y	CF		Y	1.0 0x4000
MFR_TEMP_1_OFFSET	0xF9	Sets the offset of the external temperature sensor.	R/W Word	Y	L11	C	Y	0.0 0x8000

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MFR_TEMP_1_GAIN

The MFR_TEMP_1_GAIN command will modify the slope of the external temperature sensor to account for non-idealities in the element and errors associated with the remote sensing of the temperature in the inductor.

This command has two data bytes and is formatted in 16-bit 2's complement integer. The effective gain adjustment is $N \cdot 2^{-14}$. The nominal value is 1.

MFR_TEMP_1_OFFSET

The MFR_TEMP_1_OFFSET command will modify the offset of the external temperature sensor to account for non-idealities in the element and errors associated with the remote sensing of the temperature in the inductor.

This command has two data bytes and is formatted in Linear_5s_11s format.

External Temperature Limits

COMMAND NAME	CMD CODE	DESCRIPTION	TYPE	PAGED	DATA FORMAT	UNITS	NVM	DEFAULT VALUE
OT_FAULT_LIMIT	0x4F	External overtemperature fault limit.	R/W Word	Y	L11	C	Y	100.0 0xEB20
OT_WARN_LIMIT	0x51	External overtemperature warning limit.	R/W Word	Y	L11	C	Y	85.0 0xEAA8
UT_FAULT_LIMIT	0x53	External undertemperature fault limit.	R/W Word	Y	L11	C	Y	–40.0 0xE580

OT_FAULT_LIMIT

The OT_FAULT_LIMIT command sets the value of the external sense temperature measured by the ADC, in degrees Celsius, which causes an overtemperature fault. The READ_TEMPERATURE_1 value will be used to determine if this limit has been exceeded.

This command has two data bytes and is formatted in Linear_5s_11s format.

OT_WARN_LIMIT

The OT_WARN_LIMIT command sets the value of the external sense temperature measured by the ADC, in degrees Celsius, which causes an overtemperature warning. The READ_TEMPERATURE_1 value will be used to determine if this limit has been exceeded.

In response to the OT_WARN_LIMIT being exceeded, the device:

- Sets the TEMPERATURE bit in the STATUS_BYTE
- Sets the Overtemperature Warning bit in the STATUS_TEMPERATURE command, and
- Notifies the host by asserting $\overline{\text{ALERT}}$ pin, unless masked

This command has two data bytes and is formatted in Linear_5s_11s format.

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UT_FAULT_LIMIT

The UT_FAULT_LIMIT command sets the value of the external sense temperature measured by the ADC, in degrees Celsius, which causes an undertemperature fault. The READ_TEMPERATURE_1 value will be used to determine if this limit has been exceeded.

Note: If the temp sensors are not installed, the UT_FAULT_LIMIT can be set to –275°C and UT_FAULT_LIMIT response set to ignore to avoid $\overline{\text{ALERT}}$ being asserted.

This command has two data bytes and is formatted in Linear_5s_11s format.

TIMING

Timing—On Sequence/Ramp

COMMAND NAME	CMD CODE	DESCRIPTION	TYPE	PAGED	DATA FORMAT	UNITS	NVM	DEFAULT VALUE
TON_DELAY	0x60	Time from RUN and/or Operation on to output rail turn-on.	R/W Word	Y	L11	ms	Y	0.0 0x8000
TON_RISE	0x61	Time from when the output starts to rise until the output voltage reaches the VOUT commanded value.	R/W Word	Y	L11	ms	Y	8.0 0xD200
TON_MAX_FAULT_LIMIT	0x62	Maximum time from the start of TON_RISE for VOUT to cross the VOUT_UV_FAULT_LIMIT.	R/W Word	Y	L11	ms	Y	10.0 0xD280
VOUT_TRANSITION_RATE	0x27	Rate the output changes when VOUT commanded to a new value.	R/W Word	Y	L11	V/ms	Y	0.25 0xAA00

TON_DELAY

The TON_DELAY command sets the time, in milliseconds, from when a start condition is received until the output voltage starts to rise. Values from 0ms to 83 seconds are valid. The resulting turn-on delay will have a typical delay of 270µs for TON_DELAY = 0 and an uncertainty of ±50µs for all values of TON_DELAY.

This command has two data bytes and is formatted in Linear_5s_11s format.

TON_RISE

The TON_RISE command sets the time, in milliseconds, from the time the output starts to rise to the time the output enters the regulation band. Values from 0 to 1.3 seconds are valid. The part will be in discontinuous mode during TON_RISE events. If TON_RISE is less than 0.25ms, the LTC7132 digital slope will be bypassed and the output voltage transition will only be controlled by the analog performance of the PWM switcher. The number of steps in TON_RISE is equal to TON_RISE (in ms)/0.1ms with an uncertainty of ±0.1ms.

This command has two data bytes and is formatted in Linear_5s_11s format.

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TON_MAX_FAULT_LIMIT

The TON_MAX_FAULT_LIMIT command sets the value, in milliseconds, on how long the unit can attempt to power up the output without reaching the output undervoltage fault limit.

A data value of 0ms means that there is no limit and that the unit can attempt to bring up the output voltage indefinitely. The maximum limit is 83 seconds.

This command has two data bytes and is formatted in Linear_5s_11s format.

VOUT_TRANSITION_RATE

When a PMBus device receives either a VOUT_COMMAND or OPERATION (Margin High, Margin Low) that causes the output voltage to change, this command set the rate in V/ms at which the output voltage changes. The commanded rate of change does not apply when the unit is commanded on or off. The maximum allowed slope is 4V/ms.

This command has two data bytes and is formatted in Linear_5s_11s format.

Timing—Off Sequence/Ramp

COMMAND NAME	CMD CODE	DESCRIPTION	TYPE	PAGED	DATA FORMAT	UNITS	NVM	DEFAULT VALUE
TOFF_DELAY	0x64	Time from RUN and/or Operation off to the start of TOFF_FALL ramp.	R/W Word	Y	L11	ms	Y	0.0 0x8000
TOFF_FALL	0x65	Time from when the output starts to fall until the output reaches zero volts.	R/W Word	Y	L11	ms	Y	8.0 0xD200
TOFF_MAX_WARN_LIMIT	0x66	Maximum allowed time, after TOFF_FALL completed, for the unit to decay below 12.5%.	R/W Word	Y	L11	ms	Y	150 0xF258

TOFF_DELAY

The TOFF_DELAY command sets the time, in milliseconds, from when a stop condition is received until the output voltage starts to fall. Values from 0 to 83 seconds are valid. The resulting turn off delay will have a typical delay of 270µs for TOFF_DELAY = 0 and an uncertainty of ±50µs for all values of TOFF_DELAY. TOFF_DELAY is not applied when a fault event occurs

This command has two data bytes and is formatted in Linear_5s_11s format.

TOFF_FALL

The TOFF_FALL command sets the time, in milliseconds, from the end of the turn-off delay time until the output voltage is commanded to zero. It is the ramp time of the V_{OUT} DAC. When the V_{OUT} DAC is zero, the PWM output will be set to high impedance state.

The part will maintain the mode of operation programmed. For defined TOFF_FALL times, the user should set the part to continuous conduction mode. Loading the max value indicates the part will ramp down at the slowest possible rate. The minimum supported fall time is 0.25ms. A value less than 0.25ms will result in a 0.25ms ramp. The maximum fall time is 1.3 seconds. The number of steps in TOFF_FALL is equal to TOFF_FALL (in ms)/0.1ms with an uncertainty of ±0.1ms.

In discontinuous conduction mode, the controller will not draw current from the load and the fall time will be set by the output capacitance and load current.

This command has two data bytes and is formatted in Linear_5s_11s format.

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TOFF_MAX_WARN_LIMIT

The TOFF_MAX_WARN_LIMIT command sets the value, in milliseconds, on how long the output voltage exceeds 12.5% of the programmed voltage before a warning is asserted. The output is considered off when the V_{OUT} voltage is less than 12.5% of the programmed VOUT_COMMAND value. The calculation begins after TOFF_FALL is complete.

A data value of 0ms means that there is no limit and that the output voltage exceeds 12.5% of the programmed voltage indefinitely. Other than 0, values from 120ms to 524 seconds are valid.

This command has two data bytes and is formatted in Linear_5s_11s format.

Precondition for Restart

COMMAND NAME	CMD CODE	DESCRIPTION	TYPE	PAGED	DATA FORMAT	UNITS	NVM	DEFAULT VALUE
MFR_RESTART_ DELAY	0xDC	Minimum time the RUN pin is held low by the LTC7132.	R/W Word	Y	L11	ms	Y	500 0xFBE8

MFR_RESTART_DELAY

This command specifies the minimum RUN off time in milliseconds. This device will pull the RUN pin low for this length of time once a falling edge of RUN has been detected. The minimum recommended value is 136ms.

Note: The restart delay is different than the retry delay. The restart delay pulls RUN low for the specified time, after which a standard start-up sequence is initiated. The minimum restart delay should be equal to TOFF_DELAY + TOFF_FALL + 136ms. Valid values are from 136ms to 65.52 seconds in 16ms increments. To assure a minimum off time, set the MFR_RESTART_DELAY 16ms longer than the desired time. The output rail can be off longer than the MFR_RESTART_DELAY after the RUN pin is pulled high if the output decay bit 0 is enabled in MFR_CHAN_CONFIG and the output takes a long time to decay below 12.5% of the programmed value.

This command has two data bytes and is formatted in Linear_5s_11s format.

FAULT RESPONSE

Fault Responses All Faults

COMMAND NAME	CMD CODE	DESCRIPTION	TYPE	PAGED	DATA FORMAT	UNITS	NVM	DEFAULT VALUE
MFR_RETRY_ DELAY	0xDB	Retry interval during FAULT retry mode.	R/W Word	Y	L11	ms	Y	350 0xFABC

MFR_RETRY_DELAY

This command sets the time in milliseconds between retries if the fault response is to retry the controller at specified intervals. This command value is used for all fault responses that require retry. The retry time starts once the fault has been detected by the offending channel. Valid values are from 120ms to 83.88 seconds in 10µs increments.

Note: The retry delay time is determined by the longer of the MFR_RETRY_DELAY command or the time required for the regulated output to decay below 12.5% of the programmed value. If the natural decay time of the output is too long, it is possible to remove the voltage requirement of the MFR_RETRY_DELAY command by asserting bit 0 of MFR_CHAN_CONFIG.

This command has two data bytes and is formatted in Linear_5s_11s format.

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Fault Responses Input Voltage

COMMAND NAME	CMD CODE	DESCRIPTION	TYPE	PAGED	DATA FORMAT	UNITS	NVM	DEFAULT VALUE
VIN_OV_FAULT_RESPONSE	0x56	Action to be taken by the device when an input supply overvoltage fault is detected.	R/W Byte	Y	Reg		Y	0x80

VIN_OV_FAULT_RESPONSE

The VIN_OV_FAULT_RESPONSE command instructs the device on what action to take in response to an input overvoltage fault. The data byte is in the format given in Table 11.

The device also:

- Sets the NONE_OF_THE_ABOVE bit in the STATUS_BYTE
- Set the INPUT bit in the upper byte of the STATUS_WORD
- Sets the VIN Overvoltage Fault bit in the STATUS_INPUT command, and
- Notifies the host by asserting $\overline{\text{ALERT}}$ pin, unless masked

This command has one data byte.

Fault Responses Output Voltage

COMMAND NAME	CMD CODE	DESCRIPTION	TYPE	PAGED	DATA FORMAT	UNITS	NVM	DEFAULT VALUE
VOUT_OV_FAULT_RESPONSE	0x41	Action to be taken by the device when an output overvoltage fault is detected.	R/W Byte	Y	Reg		Y	0xB8
VOUT_UV_FAULT_RESPONSE	0x45	Action to be taken by the device when an output undervoltage fault is detected.	R/W Byte	Y	Reg		Y	0xB8
TON_MAX_FAULT_ RESPONSE	0x63	Action to be taken by the device when a TON_MAX_FAULT event is detected.	R/W Byte	Y	Reg		Y	0xB8

VOUT_OV_FAULT_RESPONSE

The VOUT_OV_FAULT_RESPONSE command instructs the device on what action to take in response to an output overvoltage fault. The data byte is in the format given in Table 7.

The device also:

- Sets the VOUT_OV bit in the STATUS_BYTE
- Sets the VOUT bit in the STATUS_WORD
- Sets the VOUT Overvoltage Fault bit in the STATUS_VOUT command
- Notifies the host by asserting $\overline{\text{ALERT}}$ pin, unless masked

The only values recognized for this command are:

0x00–Part performs OV pull down only, or OV_PULLDOWN.

0x80–The device shuts down (disables the output) and the unit does not attempt to retry. (PMBus, Part II, Section 10.7).

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0xB8–The device shuts down (disables the output) and device attempts to retry continuously, without limitation, until it is commanded OFF (by the RUN pin or OPERATION command or both), bias power is removed, or another fault condition causes the unit to shut down.

0x4n The device shuts down and the unit does not attempt to retry. The output remains disabled until the part is commanded OFF then ON or the RUN pin is asserted low then high or RESET through the command or removal of VIN. The OV fault must remain active for a period of n • 10µs, where n is a value from 0 to 7.

0x78+n The device shuts down and the unit attempts to retry continuously until either the fault condition is cleared or the part is commanded OFF then ON or the RUN pin is asserted low then high or RESET through the command or removal of VIN. The OV fault must remain active for a period of n • 10µs, where n is a value from 0 to 7.

Any other value will result in a CML fault and the write will be ignored.

This command has one data byte.

Table 7. VOUT_OV_FAULT_RESPONSE Data Byte Contents

BITS	DESCRIPTION	VALUE	MEANING
7:6	Response For all values of bits [7:6], the LTC7132: • Sets the corresponding fault bit in the status commands and • Notifies the host by asserting $\overline{\text{ALERT}}$ pin, unless masked. The fault bit, once set, is cleared only when one or more of the following events occurs: • The device receives a CLEAR_FAULTS command. • The output is commanded through the RUN pin, the OPERATION command, or the combined action of the RUN pin and OPERATION command, to turn off and then to turn back on, or • Bias power is removed and reapplied to the LTC7132.	00	Part performs OV pull down only or OV_PULLDOWN (i.e., turns off the top MOSFET and turns on lower MOSFET while V_{OUT} is > VOUT_OV_FAULT).
		01	The PMBus device continues operation for the delay time specified by bits [2:0] and the delay time unit specified for that particular fault. If the fault condition is still present at the end of the delay time, the unit responds as programmed in the Retry Setting (bits [5:3]).
		10	The device shuts down immediately (disables the output) and responds according to the retry setting in bits [5:3].
		11	Not supported. Writing this value will generate a CML fault.
5:3	Retry Setting	000	The unit does not attempt to restart. The output remains disabled until the fault is cleared until the device is commanded OFF bias power is removed.
		111	The PMBus device attempts to restart continuously, without limitation, until it is commanded OFF (by the RUN pin or OPERATION command or both), bias power is removed, or another fault condition causes the unit to shut down without retry. Note: The retry interval is set by the MFR_RETRY_DELAY command.
2:0	Delay Time	000-111	The delay time in 10µs increments. This delay time determines how long the controller continues operating after a fault is detected. Only valid for deglitched off state.

VOUT_UV_FAULT_RESPONSE

The VOUT_UV_FAULT_RESPONSE command instructs the device on what action to take in response to an output undervoltage fault. The data byte is in the format given in Table 8.

The device also:

- Sets the NONE_OF_THE_ABOVE bit in the STATUS_BYTE
- Sets the VOUT bit in the STATUS_WORD
- Sets the VOUT undervoltage fault bit in the STATUS_VOUT command
- Notifies the host by asserting $\overline{\text{ALERT}}$ pin, unless masked

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The UV fault and warn are masked until the following criteria are achieved:

1) The TON_MAX_FAULT_LIMIT has been reached
2) The TON_DELAY sequence has completed
3) The TON_RISE sequence has completed
4) The VOUT_UV_FAULT_LIMIT threshold has been reached
5) The IOUT_OC_FAULT_LIMIT is not present

The UV fault and warn are masked whenever the channel is not active.

The UV fault and warn are masked during TON_RISE and TOFF_FALL sequencing.

This command has one data byte.

Table 8. VOUT_UV_FAULT_RESPONSE Data Byte Contents

BITS	DESCRIPTION	VALUE	MEANING
7:6	Response For all values of bits [7:6], the LTC7132: • Sets the corresponding fault bit in the status commands and • Notifies the host by asserting $\overline{\text{ALERT}}$ pin, unless masked. The fault bit, once set, is cleared only when one or more of the following events occurs: • The device receives a CLEAR_FAULTS command. • The output is commanded through the RUN pin, the OPERATION command, or the combined action of the RUN pin and OPERATION command, to turn off and then to turn back on, or • The device receives a RESTORE_USER_ALL command. • The device receives a MFR_RESET command. • The device supply power is cycled.	00	The PMBus device continues operation without interruption. (Ignores the fault functionally)
		01	The PMBus device continues operation for the delay time specified by bits [2:0] and the delay time unit specified for that particular fault. If the fault condition is still present at the end of the delay time, the unit responds as programmed in the Retry Setting (bits [5:3]).
		10	The device shuts down (disables the output) and responds according to the retry setting in bits [5:3].
		11	Not supported. Writing this value will generate a CML fault.
5:3	Retry Setting	000	The unit does not attempt to restart. The output remains disabled until the fault is cleared until the device is commanded OFF bias power is removed.
		111	The PMBus device attempts to restart continuously, without limitation, until it is commanded OFF (by the RUN pin or OPERATION command or both), bias power is removed, or another fault condition causes the unit to shut down without retry. Note: The retry interval is set by the MFR_RETRY_DELAY command.
2:0	Delay Time	000-111	The delay time in 10µs increments. This delay time determines how long the controller continues operating after a fault is detected. Only valid for deglitched off state.

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TON_MAX_FAULT_RESPONSE

The TON_MAX_FAULT_RESPONSE command instructs the device on what action to take in response to a TON_MAX fault. The data byte is in the format given in Table 11.

The device also:

- Sets the NONE_OF_THE_ABOVE bit in the STATUS_BYTE
- Sets the VOUT bit in the STATUS_WORD
- Sets the TON_MAX_FAULT bit in the STATUS_VOUT command, and
- Notifies the host by asserting $\overline{\text{ALERT}}$ pin, unless masked

A value of 0 disables the TON_MAX_FAULT_RESPONSE. It is not recommended to use 0.

Note: The PWM channel remains in discontinues mode until the TON_MAX_FAULT_LIMIT has been exceeded.

This command has one data byte.

Fault Responses Output Current

COMMAND NAME	CMD CODE	DESCRIPTION	TYPE	PAGED	DATA FORMAT	UNITS	NVM	DEFAULT VALUE
IOUT_OC_FAULT_RESPONSE	0x47	Action to be taken by the device when an output overcurrent fault is detected.	R/W Byte	Y	Reg		Y	0x00

IOUT_OC_FAULT_RESPONSE

The IOUT_OC_FAULT_RESPONSE command instructs the device on what action to take in response to an output overcurrent fault. The data byte is in the format given in Table 9.

The device also:

- Sets the NONE_OF_THE_ABOVE bit in the STATUS_BYTE
- Sets the IOUT_OC bit in the STATUS_BYTE
- Sets the IOUT bit in the STATUS_WORD
- Sets the IOUT Overcurrent Fault bit in the STATUS_IOUT command, and
- Notifies the host by asserting $\overline{\text{ALERT}}$ pin, unless masked

This command has one data byte.

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Table 9. IOUT_OC_FAULT_RESPONSE Data Byte Contents

BITS	DESCRIPTION	VALUE	MEANING
7:6	Response For all values of bits [7:6], the LTC7132: • Sets the corresponding fault bit in the status commands and • Notifies the host by asserting $\overline{\text{ALERT}}$ pin, unless masked. The fault bit, once set, is cleared only when one or more of the following events occurs: • The device receives a CLEAR_FAULTS command. • The output is commanded through the RUN pin, the OPERATION command, or the combined action of the RUN pin and OPERATION command, to turn off and then to turn back on, or • The device receives a RESTORE_USER_ALL command. • The device receives a MFR_RESET command. • The device supply power is cycled.	00	The LTC7132 continues to operate indefinitely while maintaining the output current at the value set by IOUT_OC_FAULT_LIMIT without regard to the output voltage (known as constant-current or brick-wall limiting).
		01	Not supported.
		10	The LTC7132 continues to operate, maintaining the output current at the value set by IOUT_OC_FAULT_LIMIT without regard to the output voltage, for the delay time set by bits [2:0]. If the device is still operating in current limit at the end of the delay time, the device responds as programmed by the Retry Setting in bits [5:3].
		11	The LTC7132 shuts down immediately and responds as programmed by the Retry Setting in bits [5:3].
5:3	Retry Setting	000	The unit does not attempt to restart. The output remains disabled until the fault is cleared by cycling the RUN pin or removing bias power.
		111	The device attempts to restart continuously, without limitation, until it is commanded OFF (by the RUN pin or OPERATION command or both), bias power is removed, or another fault condition causes the unit to shut down. Note: The retry interval is set by the MFR_RETRY_DELAY command.
2:0	Delay Time	000-111	The number of delay time units in 16ms increments. This delay time is used to determine the amount of time a unit is to continue operating after a fault is detected before shutting down. Only valid for deglitched off response.

Fault Responses IC Temperature

COMMAND NAME	CMD CODE	DESCRIPTION	TYPE	PAGED	DATA FORMAT	UNITS	NVM	DEFAULT VALUE
MFR_OT_FAULT_RESPONSE	0xD6	Action to be taken by the device when an internal overtemperature fault is detected.	R Byte	N	Reg			0xC0

MFR_OT_FAULT_RESPONSE

The MFR_OT_FAULT_RESPONSE command byte instructs the device on what action to take in response to an internal overtemperature fault. The data byte is in the format given in Table 10.

The LTC7132 also:

- Sets the NONE_OF_THE_ABOVE bit in the STATUS_BYTE
- Sets the MFR bit in the STATUS_WORD, and
- Sets the Overtemperature Fault bit in the STATUS_MFR_SPECIFIC command
- Notifies the host by asserting $\overline{\text{ALERT}}$ pin, unless masked

This command has one data byte.

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Table 10. Data Byte Contents MFR_OT_FAULT_RESPONSE

BITS	DESCRIPTION	VALUE	MEANING
7:6	Response For all values of bits [7:6], the LTC7132: • Sets the corresponding fault bit in the status commands and • Notifies the host by asserting $\overline{\text{ALERT}}$ pin, unless masked. The fault bit, once set, is cleared only when one or more of the following events occurs: • The device receives a CLEAR_FAULTS command. • The output is commanded through the RUN pin, the OPERATION command, or the combined action of the RUN pin and OPERATION command, to turn off and then to turn back on, or • Bias power is removed and reapplied to the LTC7132.	00	Not supported. Writing this value will generate a CML fault.
		01	Not supported. Writing this value will generate a CML fault
		10	The device shuts down immediately (disables the output) and responds according to the retry setting in bits [5:3].
		11	The device's output is disabled while the fault is present. Operation resumes and the output is enabled when the fault condition no longer exists.
5:3	Retry Setting	000	The unit does not attempt to restart. The output remains disabled until the fault is cleared.
		001-111	Not supported. Writing this value will generate CML fault.
2:0	Delay Time	XXX	Not supported. Value ignored

Fault Responses External Temperature

COMMAND NAME	CMD CODE	DESCRIPTION	TYPE	PAGED	DATA FORMAT	UNITS	NVM	DEFAULT VALUE
OT_FAULT_ RESPONSE	0x50	Action to be taken by the device when an external overtemperature fault is detected,	R/W Byte	Y	Reg		Y	0xB8
UT_FAULT_ RESPONSE	0x54	Action to be taken by the device when an external undertemperature fault is detected.	R/W Byte	Y	Reg		Y	0xB8

OT_FAULT_RESPONSE

The OT_FAULT_RESPONSE command instructs the device on what action to take in response to an external overtemperature fault on the external temp sensors. The data byte is in the format given in Table 11.

The device also:

• Sets the TEMPERATURE bit in the STATUS_BYTE

• Sets the Overtemperature Fault bit in the STATUS_TEMPERATURE command, and

• Notifies the host by asserting $\overline{\text{ALERT}}$ pin, unless masked

This command has one data byte.

UT_FAULT_RESPONSE

The UT_FAULT_RESPONSE command instructs the device on what action to take in response to an external undertemperature fault on the external temp sensors. The data byte is in the format given in Table 11.

The device also:

• Sets the TEMPERATURE bit in the STATUS_BYTE

• Sets the Undertemperature Fault bit in the STATUS_TEMPERATURE command, and

• Notifies the host by asserting $\overline{\text{ALERT}}$ pin, unless masked

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This condition is detected by the ADC so the response time may be up to $t_{CONVERT}$.

This command has one data byte.

Table 11. Data Byte Contents: TON_MAX_FAULT_RESPONSE, VIN_OV_FAULT_RESPONSE, OT_FAULT_RESPONSE, UT_FAULT_RESPONSE

BITS	DESCRIPTION	VALUE	MEANING
7:6	Response	00	The PMBus device continues operation without interruption.
	For all values of bits [7:6], the LTC7132: • Sets the corresponding fault bit in the status commands, and • Notifies the host by asserting $\overline{ALERT}$ pin, unless masked.	01	Not supported. Writing this value will generate a CML fault.
		10	The device shuts down immediately (disables the output) and responds according to the retry setting in bits [5:3].
	The fault bit, once set, is cleared only when one or more of the following events occurs: • The device receives a CLEAR_FAULTS command. • The output is commanded through the RUN pin, the OPERATION command, or the combined action of the RUN pin and OPERATION command, to turn off and then to turn back on, or • The device receives a RESTORE_USER_ALL command. • The device receives a MFR_RESET command. • The device supply power is cycled.	11	Not supported. Writing this value will generate a CML fault.
5:3	Retry Setting	000	The unit does not attempt to restart. The output remains disabled until the fault is cleared until the device is commanded OFF bias power is removed.
		111	The PMBus device attempts to restart continuously, without limitation, until it is commanded OFF (by the RUN pin or OPERATION command or both), bias power is removed, or another fault condition causes the unit to shut down without retry. Note: The retry interval is set by the MFR_RETRY_DELAY command.
2:0	Delay Time	XXX	Not supported. Values ignored

FAULT SHARING

Fault Sharing Propagation

COMMAND NAME	CMD CODE	DESCRIPTION	TYPE	PAGED	DATA FORMAT	UNITS	NVM	DEFAULT VALUE
MFR_FAULT_PROPAGATE	0xD2	Configuration that determines which faults are propagated to the FAULT pins.	R/W Word	Y	Reg		Y	0x6993

MFR_FAULT_PROPAGATE

The MFR_FAULT_PROPAGATE command enables the faults that can cause the $\overline{FAULT}n$ pin to assert low. The command is formatted as shown in Table 12. Faults can only be propagated to the $\overline{FAULT}n$ pin if they are programmed to respond to faults.

This command has two data bytes.

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Table 12. $\overline{\text{FAULT}}n$ Propagate Fault Configuration

The $\overline{\text{FAULT0}}$ and $\overline{\text{FAULT1}}$ pins are designed to provide electrical notification of selected events to the user. Some of these events are common to both output channels. Others are specific to an output channel. They can also be used to share faults between channels.

BIT(S)	SYMBOL	OPERATION
B[15]	VOUT disabled while not decayed.	This is used in a PolyPhase configuration when bit 0 of the MFR_CHAN_CONFIG_LTC7132 is a zero. If the channel is turned off, by toggling the RUN pin or commanding the part OFF, and then the RUN is reasserted or the part is commanded back on before the output has decayed, VOUT will not restart until the 12.5% decay is honored. The $\overline{\text{FAULT}}$ pin is asserted during this condition if bit 15 is asserted.
B[14]	Mfr_fault_propagate_short_CMD_cycle	0: No action 1: Asserts low if commanded off then on before the output has sequenced off. Re-asserts high $t_{OFF(MIN)}$ after sequence off.
b[13]	Mfr_fault_propagate_ton_max_fault	0: No action if a TON_MAX_FAULT fault is asserted 1: Associated output will be asserted low if a TON_MAX_FAULT fault is asserted $\overline{\text{FAULT0}}$ is associated with page 0 TON_MAX_FAULT faults $\overline{\text{FAULT1}}$ is associated with page 1 TON_MAX_FAULT faults
b[12]	Reserved	
b[11]	Mfr_fault0_propagate_int_ot, Mfr_fault1_propagate_int_ot	0: No action if the MFR_OT_FAULT_LIMIT fault is asserted 1: Associated output will be asserted low if the MFR_OT_FAULT_LIMIT fault is asserted
b[10]	Reserved	
b[9]	Reserved	
b[8]	Mfr_fault0_propagate_ut, Mfr_fault1_propagate_ut	0: No action if the UT_FAULT_LIMIT fault is asserted 1: Associated output will be asserted low if the UT_FAULT_LIMIT fault is asserted $\overline{\text{FAULT0}}$ is associated with page 0 UT faults $\overline{\text{FAULT1}}$ is associated with page 1 UT faults
b[7]	Mfr_fault0_propagate_ot, Mfr_fault1_propagate_ot	0: No action if the OT_FAULT_LIMIT fault is asserted 1: Associated output will be asserted low if the OT_FAULT_LIMIT fault is asserted $\overline{\text{FAULT0}}$ is associated with page 0 OT faults $\overline{\text{FAULT1}}$ is associated with page 1 OT faults
b[6]	Reserved	
b[5]	Reserved	
b[4]	Mfr_fault0_propagate_input_ov, Mfr_fault1_propagate_input_ov	0: No action if the VIN_OV_FAULT_LIMIT fault is asserted 1: Associated output will be asserted low if the VIN_OV_FAULT_LIMIT fault is asserted
b[3]	Reserved	
b[2]	Mfr_fault0_propagate_iout_oc, Mfr_fault1_propagate_iout_oc	0: No action if the IOUT_OC_FAULT_LIMIT fault is asserted 1: Associated output will be asserted low if the IOUT_OC_FAULT_LIMIT fault is asserted $\overline{\text{FAULT0}}$ is associated with page 0 OC faults $\overline{\text{FAULT1}}$ is associated with page 1 OC faults
b[1]	Mfr_fault0_propagate_vout_uv, Mfr_fault1_propagate_vout_uv	0: No action if the VOUT_UV_FAULT_LIMIT fault is asserted 1: Associated output will be asserted low if the VOUT_UV_FAULT_LIMIT fault is asserted $\overline{\text{FAULT0}}$ is associated with page 0 UV faults $\overline{\text{FAULT1}}$ is associated with page 1 UV faults
b[0]	Mfr_fault0_propagate_vout_ov, Mfr_fault1_propagate_vout_ov	0: No action if the VOUT_OV_FAULT_LIMIT fault is asserted 1: Associated output will be asserted low if the VOUT_OV_FAULT_LIMIT fault is asserted $\overline{\text{FAULT0}}$ is associated with page 0 OV faults $\overline{\text{FAULT1}}$ is associated with page 1 OV faults

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Fault Sharing Response

COMMAND NAME	CMD CODE	DESCRIPTION	TYPE	PAGED	DATA FORMAT	UNITS	NVM	DEFAULT VALUE
MFR_FAULT_RESPONSE	0xD5	Action to be taken by the device when the FAULT pin is asserted low.	R/W Byte	Y	Reg		Y	0xC0

MFR_FAULT_RESPONSE

The MFR_FAULT_RESPONSE command instructs the device on what action to take in response to the $\overline{\text{FAULT}}n$ pin being pulled low by an external source.

Supported Values:

VALUE	MEANING
0xC0	FAULT_INHIBIT The LTC7132 will three-state the output in response to the $\overline{\text{FAULT}}$ pin pulled low.
0x00	FAULT_IGNORE The LTC7132 continues operation without interruption.

The device also:

- Sets the MFR Bit in the STATUS_WORD.
- Sets Bit 0 in the STATUS_MFR_SPECIFIC Command to Indicate $\overline{\text{FAULT}}n$ Is Being Pulled Low
- Notifies the Host by Asserting $\overline{\text{ALERT}}$, Unless Masked

This command has one data byte.

SCRATCHPAD

COMMAND NAME	CMD CODE	DESCRIPTION	TYPE	PAGED	DATA FORMAT	UNITS	NVM	DEFAULT VALUE
USER_DATA_00	0xB0	OEM reserved. Typically used for part serialization.	R/W Word	N	Reg		Y	NA
USER_DATA_01	0xB1	Manufacturer reserved for LTpowerPlay.	R/W Word	Y	Reg		Y	NA
USER_DATA_02	0xB2	OEM reserved. Typically used for part serialization.	R/W Word	N	Reg		Y	NA
USER_DATA_03	0xB3	A NVM word available for the user.	R/W Word	Y	Reg		Y	0x0000
USER_DATA_04	0xB4	A NVM word available for the user.	R/W Word	N	Reg		Y	0x0000

USER_DATA_00 through USER_DATA_04

These commands are non-volatile memory locations for customer storage. The customer has the option to write any value to the USER_DATA_nn at any time. However, the LTpowerPlay software and contract manufacturers use some of these commands for inventory control. Modifying the reserved USER_DATA_nn commands may lead to undesirable inventory control and incompatibility with these products.

These commands have 2 data bytes and are in register format.

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IDENTIFICATION

COMMAND NAME	CMD CODE	DESCRIPTION	TYPE	PAGED	DATA FORMAT	UNITS	NVM	DEFAULT VALUE
PMBus_REVISION	0x98	PMBus revision supported by this device. Current revision is 1.2.	R Byte	N	Reg		FS	0x22
CAPABILITY	0x19	Summary of PMBus optional communication protocols supported by this device.	R Byte	N	Reg			0xB0
MFR_ID	0x99	The manufacturer ID of the LTC7132 in ASCII.	R String	N	ASC			LTC
MFR_MODEL	0x9A	Manufacturer part number in ASCII.	R String	N	ASC			LTC7132
MFR_SPECIAL_ID	0xE7	Manufacturer code representing the LTC7132.	R Word	N	Reg			0x4C0X

PMBus_REVISION

The PMBUS_REVISION command indicates the revision of the PMBus to which the device is compliant. The LTC7132 is PMBus Version 1.2 compliant in both Part I and Part II.

This read-only command has one data byte.

CAPABILITY

This command provides a way for a host system to determine some key capabilities of a PMBus device.

The LTC7132 supports packet error checking, 400kHz bus speeds, and $\overline{\text{ALERT}}$ pin.

This read-only command has one data byte.

MFR_ID

The MFR_ID command indicates the manufacturer ID of the LTC7132 using ASCII characters.

This read-only command is in block format.

MFR_MODEL

The MFR_MODEL command indicates the manufacturer's part number of the LTC7132 using ASCII characters.

This read-only command is in block format.

MFR_SPECIAL_ID

The 16-bit word representing the part name and revision. 0x4C denotes the part is an LTC7132, XX is adjustable by the manufacturer.

This read-only command has two data bytes.

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FAULT WARNING AND STATUS

COMMAND NAME	CMD CODE	DESCRIPTION	TYPE	PAGED	FORMAT	UNITS	NVM	DEFAULT VALUE
CLEAR_FAULTS	0x03	Clear any fault bits that have been set.	Send Byte	N				NA
SMBALERT_MASK	0x1B	Mask activity.	Block R/W	Y	Reg		Y	See CMD Details
MFR_CLEAR_PEAKS	0xE3	Clears all peak values.	Send Byte	Y				NA
STATUS_BYTE	0x78	One byte summary of the unit's fault condition.	R/W Byte	Y	Reg			NA
STATUS_WORD	0x79	Two byte summary of the unit's fault condition.	R/W Word	Y	Reg			NA
STATUS_VOUT	0x7A	Output voltage fault and warning status.	R/W Byte	Y	Reg			NA
STATUS_IOUT	0x7B	Output current fault and warning status.	R/W Byte	Y	Reg			NA
STATUS_INPUT	0x7C	Input supply fault and warning status.	R/W Byte	N	Reg			NA
STATUS_ TEMPERATURE	0x7D	External temperature fault and warning status for READ_TEMPERATURE_1.	R/W Byte	Y	Reg			NA
STATUS_CML	0x7E	Communication and memory fault and warning status.	R/W Byte	N	Reg			NA
STATUS_MFR_ SPECIFIC	0x80	Manufacturer specific fault and state information.	R/W Byte	Y	Reg			NA
MFR_PADS	0xE5	Digital status of the I/O pads.	R Word	N	Reg			NA
MFR_COMMON	0xEF	Manufacturer status bits that are common across multiple ADI chips.	R Byte	N	Reg			NA

CLEAR_FAULTS

The CLEAR_FAULTS command is used to clear any fault bits that have been set. This command clears all bits in all status commands simultaneously. At the same time, the device negates (clears, releases) its $\overline{\text{ALERT}}$ pin signal output if the device is asserting the $\overline{\text{ALERT}}$ pin signal. If the fault is still present when the bit is cleared, the fault bit will remain set and the host notified by asserting the $\overline{\text{ALERT}}$ pin low. CLEAR_FAULTS can take up to 10µs to process. If a fault occurs within that time frame it may be cleared before the status register is set.

This write-only command has no data bytes.

The CLEAR_FAULTS does not cause a unit that has latched off for a fault condition to restart. Units that have shut down for a fault condition are restarted when:

- The output is commanded through the RUN pin, the OPERATION command, or the combined action of the RUN pin and OPERATION command, to turn off and then to turn back on, or
- MFR_RESET command is issued.
- Bias power is removed and reapplied to the integrated circuit

SMBALERT_MASK

The SMBALERT_MASK command can be used to prevent a particular status bit or bits from asserting $\overline{\text{ALERT}}$ as they are asserted.

Figure 52 shows an example of the Write Word format used to set an $\overline{\text{ALERT}}$ mask, in this case without PEC. The bits in the mask byte align with bits in the specified status register. For example, if the STATUS_TEMPERATURE command code is sent in the first data byte, and the mask byte contains 0x40, then a subsequent External Overtemperature Warning

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would still set bit 6 of STATUS_TEMPERATURE but not assert $\overline{\text{ALERT}}$. All other supported STATUS_TEMPERATURE bits would continue to assert $\overline{\text{ALERT}}$ if set.

Figure 53 shows an example of the Block Write – Block Read Process Call protocol used to read back the present state of any supported status register, again without PEC.

SMBALERT_MASK cannot be applied to STATUS_BYTE, STATUS_WORD, MFR_COMMON or MFR_PADS_LTC7132. Factory default masking for applicable status registers is shown below. Providing an unsupported command code to SMBALERT_MASK will generate a CML for Invalid/Unsupported Data.

SMBALERT_MASK Default Setting: (Refer Also to Figure 2)

STATUS RESISTER	ALERT Mask Value	MASKED BITS
STATUS_VOUT	0x00	None
STATUS_IOUT	0x00	None
STATUS_TEMPERATURE	0x00	None
STATUS_CML	0x00	None
STATUS_INPUT	0x00	None
STATUS_MFR_SPECIFIC	0x11	Bit 4 (internal PLL unlocked), bit 0 ($\overline{\text{FAULT}}$ pulled low by external device)

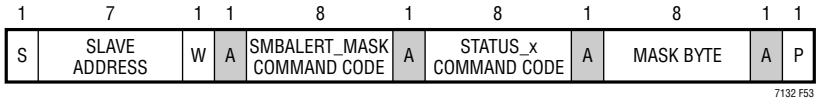

Figure 52. Example of Writing SMBALERT_MASK

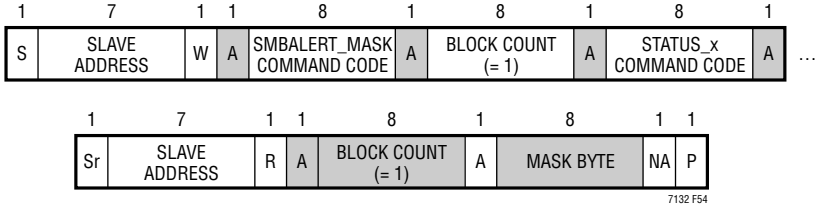

Figure 53. Example of Reading SMBALERT_MASK

MFR_CLEAR_PEAKS

The MFR_CLEAR_PEAKS command clears the MFR_*_PEAK data values. A MFR_RESET command will also clear the MFR_*_PEAK data values.

This write-only command has no data bytes.

STATUS_BYTE

The STATUS_BYTE command returns one byte of information with a summary of the most critical faults. This is the lower byte of the status word.

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STATUS_BYTE Message Contents:

BIT	STATUS BIT NAME	MEANING
7*	BUSY	A fault was declared because the LTC7132 was unable to respond.
6	OFF	This bit is set if the channel is not providing power to its output, regardless of the reason, including simply not being enabled.
5	VOUT_OV	An output overvoltage fault has occurred.
4	IOUT_OC	An output overcurrent fault has occurred.
3	VIN_UV	Not supported (LTC7132 returns 0).
2	TEMPERATURE	A temperature fault or warning has occurred.
1	CML	A communications, memory or logic fault has occurred.
0*	NONE OF THE ABOVE	A fault Not listed in bits[7:1] has occurred.

*$\overline{\text{ALERT}}$ can be asserted if either of these bits is set. They may be cleared by writing a 1 to their bit position in the STATUS_BYTE, in lieu of a CLEAR_FAULTS command.

This command has one data byte.

STATUS_WORD

The STATUS_WORD command returns a two-byte summary of the channel's fault condition. The low byte of the STATUS_WORD is the same as the STATUS_BYTE command.

STATUS_WORD High Byte Message Contents:

BIT	STATUS BIT NAME	MEANING
15	V_{OUT}	An output voltage fault or warning has occurred.
14	I_{OUT}	An output current fault or warning has occurred.
13	INPUT	An input voltage fault or warning has occurred.
12	MFR_SPECIFIC	A fault or warning specific to the LTC7132 has occurred.
11	POWER_GOOD#	The POWER_GOOD state is false if this bit is set.
10	FANS	Not supported (LTC7132 returns 0).
9	OTHER	Not supported (LTC7132 returns 0).
8	UNKNOWN	Not supported (LTC7132 returns 0).

If any of the bits in the upper byte are set, NONE_OF_THE_ABOVE is asserted.

This command has two data bytes.

STATUS_VOUT

The STATUS_VOUT command returns one byte of V_{OUT} status information.

STATUS_VOUT Message Contents:

BIT	MEANING
7	V_{OUT} overvoltage fault.
6	V_{OUT} overvoltage warning.
5	V_{OUT} undervoltage warning.
4	V_{OUT} undervoltage fault.
3	V_{OUT} max warning.
2	TON max fault.
1	TOFF max fault.
0	Not supported (LTC7132 returns 0).

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The user is permitted to write a 1 to any bit in this command to clear a specific fault. This permits the user to clear status by means other than using the CLEAR_FAULTS command.

Any supported fault bit in this command will initiate an $\overline{\text{ALERT}}$ event.

This command has one data byte.

STATUS_IOUT

The STATUS_IOUT command returns one byte of I_{OUT} status information.

STATUS_IOUT Message Contents:

BIT	MEANING
7	I_{OUT} overcurrent fault.
6	Not supported (LTC7132 returns 0).
5	I_{OUT} overcurrent warning.
4:0	Not supported (LTC7132 returns 0).

The user is permitted to write a 1 to any bit in this command to clear a specific fault. This permits the user to clear status by means other than using the CLEAR_FAULTS command.

Any supported fault bit in this command will initiate an $\overline{\text{ALERT}}$ event. This command has one data byte.

STATUS_INPUT

The STATUS_INPUT command returns one byte of V_{IN} (VINSNS) status information.

STATUS_INPUT Message Contents:

BIT	MEANING
7	V_{IN} overvoltage fault.
6	Not supported (LTC7132 returns 0).
5	V_{IN} undervoltage warning.
4	Not supported (LTC7132 returns 0).
3	Unit off for insufficient V_{IN}.
2	Not supported (LTC7132 returns 0).
1	I_{IN} overcurrent warning.
0	Not supported (LTC7132 returns 0).

The user is permitted to write a 1 to any bit in this command to clear a specific fault. This permits the user to clear status by means other than using the CLEAR_FAULTS command.

Any supported fault bit in this command will initiate an $\overline{\text{ALERT}}$ event. Bit 3 of this command is not latched and will not generate an $\overline{\text{ALERT}}$ even if it is set. This command has one data byte.

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STATUS_TEMPERATURE

The STATUS_TEMPERATURE commands returns one byte with status information on temperature. This is a paged command and is related to the respective READ_TEMPERATURE_1 value.

STATUS_TEMPERATURE Message Contents:

BIT	MEANING
7	External overtemperature fault.
6	External overtemperature warning.
5	Not supported (LTC7132 returns 0).
4	External undertemperature fault.
3:0	Not supported (LTC7132 returns 0).

.

The user is permitted to write a 1 to any bit in this command to clear a specific fault. This permits the user to clear status by means other than using the CLEAR_FAULTS command.

This command has one data byte.

STATUS_CML

The STATUS_CML command returns one byte of status information on received commands, internal memory and logic.

STATUS_CML Message Contents:

BIT	MEANING
7	Invalid or unsupported command received.
6	Invalid or unsupported data received.
5	Packet error check failed.
4	Memory fault detected.
3	Processor fault detected.
2	Reserved (LTC7132 returns 0).
1	Other communication fault.
0	Other memory or logic fault.

If either bit 3 or bit 4 of this command is set, a serious and significant internal error has been detected. Continued operation of the part is not recommended if these bits are continuously set.

The user is permitted to write a 1 to any bit in this command to clear a specific fault. This permits the user to clear status by means other than using the CLEAR_FAULTS command.

Any supported fault bit in this command will initiate an $\overline{\text{ALERT}}$ event.

This command has one data byte.

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STATUS_MFR_SPECIFIC

The STATUS_MFR_SPECIFIC commands returns one byte with the manufacturer specific status information.

The format for this byte is:

BIT	MEANING
7	Internal Temperature Fault Limit Exceeded.
6	Internal Temperature Warn Limit Exceeded.
5	Factory Trim Area NVM CRC Fault.
4	PLL is Unlocked
3	Fault Log Present
2	V_{DD33} UV or OV Fault
1	ShortCycle Event Detected
0	$\overline{FAULT}$ Pin Asserted Low by External Device

If any of these bits are set, the MFR bit in the STATUS_WORD will be set, and $\overline{ALERT}$ may be asserted.

The user is permitted to write a 1 to any bit in this command to clear a specific fault. This permits the user to clear status by means other than using the CLEAR_FAULTS command. However, the fault log present bit can only be cleared by issuing the MFR_FAULT_LOG_CLEAR command.

Any supported fault bit in this command will initiate an $\overline{ALERT}$ event.

This command has one data byte.

MFR_PADS

This command provides the user a means of directly reading the digital status of the I/O pins of the device. The bit assignments of this command are as follows:

BIT	ASSIGNED DIGITAL PIN
15	V_{DD33} OV Fault
14	V_{DD33} UV Fault
13	Reserved
12	Reserved
11	ADC Values Invalid, Occurs During Start-Up. May Occur Briefly on Current Measurement Channels During Normal Operation
10	SYNC clocked by external device (when LTC7132 configured to drive SYNC pin)
9	Channel 1 Power Good
8	Channel 0 Power Good
7	LTC7132 Driving RUN1 Low
6	LTC7132 Driving RUN0 Low
5	RUN1 Pin State
4	RUN0 Pin State
3	LTC7132 Driving $\overline{FAULT1}$ Low
2	LTC7132 Driving $\overline{FAULT0}$ Low
1	$\overline{FAULT1}$ Pin State
0	$\overline{FAULT0}$ Pin State

A 1 indicates the condition is true.

This read-only command has two data bytes.

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MFR_COMMON

The MFR_COMMON command contains bits that are common to all ADI digital power and telemetry products.

BIT	MEANING
7	Chip Not Driving $\overline{\text{ALERT}}$ Low
6	LTC7132 Not Busy
5	Calculations Not Pending
4	LTC7132 Outputs Not in Transition
3	NVM Initialized
2	Reserved
1	SHARE_CLK Timeout
0	WP Pin Status

This read-only command has one data byte.

MFR_INFO

The MFR_INFO command contains additional status bits that are LTC7132-specific and may be common to multiple ADI PSM products.

MFR_INFO Data Contents:

BIT	MEANING
15:5	Reserved.
4	EEPROM ECC status. 0: Corrections made in the EEPROM user space. 1: No corrections made in the EEPROM user space.
3:0	Reserved

EEPROM ECC status is updated after each RESTORE_USER_ALL or RESET command, a power-on reset or an EEPROM bulk read operation. This read-only command has two data bytes.

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TELEMETRY

COMMAND NAME	CMD CODE	DESCRIPTION	TYPE	PAGED	FORMAT	UNITS	NVM	DEFAULT VALUE
READ_VIN	0x88	Measured input supply voltage.	R Word	N	L11	V		NA
READ_IIN	0x89	Measured input supply current.	R Word	N	L11	A		NA
READ_VOUT	0x8B	Measured output voltage.	R Word	Y	L16	V		NA
READ_IOUT	0x8C	Measured output current.	R Word	Y	L11	A		NA
READ_TEMPERATURE_1	0x8D	External diode junction temperature. This is the value used for all temperature related processing, including IOUT_CAL_GAIN.	R Word	Y	L11	C		NA
READ_TEMPERATURE_2	0x8E	Internal junction temperature. Does not affect any other commands.	R Word	N	L11	C		NA
READ_FREQUENCY	0x95	Measured PWM switching frequency.	R Word	Y	L11	Hz		NA
READ_POUT	0x96	Calculated output power.	R Word	Y	L11	W		NA
READ_PIN	0x97	Calculated input power.	R Word	N	L11	W		NA
MFR_PIN_ACCURACY	0xAC	Returns the accuracy of the READ_PIN command	R Byte	N		%		5.0%
MFR_IOUT_PEAK	0xD7	Report the maximum measured value of READ_IOUT since last MFR_CLEAR_PEAKS.	R Word	Y	L11	A		NA
MFR_VOUT_PEAK	0xDD	Maximum measured value of READ_VOUT since last MFR_CLEAR_PEAKS.	R Word	Y	L16	V		NA
MFR_VIN_PEAK	0xDE	Maximum measured value of READ_VIN since last MFR_CLEAR_PEAKS.	R Word	N	L11	V		NA
MFR_TEMPERATURE_1_PEAK	0xDF	Maximum measured value of external Temperature (READ_TEMPERATURE_1) since last MFR_CLEAR_PEAKS.	R Word	Y	L11	C		NA
MFR_READ_IIN_PEAK	0xE1	Maximum measured value of READ_IIN command since last MFR_CLEAR_PEAKS.	R Word	N	L11	A		NA
MFR_READ_ICHIP	0xE4	Measured current used by the LTC7132.	R Word	N	L11	A		NA
MFR_TEMPERATURE_2_PEAK	0xF4	Peak internal die temperature since last MFR_CLEAR_PEAKS.	R Word	N	L11	C		NA
MFR_ADC_CONTROL	0xD8	ADC telemetry parameter selected for repeated fast ADC read back.	R/W Byte	N	N	Reg		NA
MFR_REAL_TIME	0xFB	48-bit share-clock counter value	R Block	N	CF			NA

READ_VIN

The READ_VIN command returns the measured V_{IN} pin voltage, in volts added to READ_ICHIP • MFR_RVIN. This compensates for the IR voltage drop across the V_{IN} filter element due to the supply current of the LTC7132.

This read-only command has two data bytes and is formatted in Linear_5s_11s format.

READ_VOUT

The READ_VOUT command returns the measured output voltage by the VOUT_MODE command.

This read-only command has two data bytes and is formatted in Linear_16u format.

READ_IIN

The READ_IIN command returns the input current, in Amperes, as measured across the input current sense resistor (see also MFR_IIN_CAL_GAIN).

This read-only command has two data bytes and is formatted in Linear_5s_11s format.

PMBus COMMAND DETAILS

READ_IOUT

The READ_IOUT command returns the average output current in amperes. The IOUT value is a function of:

a) the differential voltage measured across the I_{SENSE} pins

b) the IOUT_CAL_GAIN value

c) the MFR_IOUT_CAL_GAIN_TC value, and

d) READ_TEMPERATURE_1 value

e) The MFR_TEMP_1_GAIN and the MFR_TEMP_1_OFFSET

This read-only command has two data bytes and is formatted in Linear_5s_11s format.

READ_TEMPERATURE_1

The READ_TEMPERATURE_1 command returns the temperature, in degrees Celsius, of the external sense element.

This read-only command has two data bytes and is formatted in Linear_5s_11s format.

READ_TEMPERATURE_2

The READ_TEMPERATURE_2 command returns the LTC7132's die temperature, in degrees Celsius, of the internal sense element.

This read-only command has two data bytes and is formatted in Linear_5s_11s format.

READ_FREQUENCY

The READ_FREQUENCY command is a reading of the PWM switching frequency in kHz.

This read-only command has 2 data bytes and is formatted in Linear_5s_11s format.

READ_POUT

The READ_POUT command is a reading of the DC/DC converter output power in Watts. POUT is calculated based on the most recent correlated output voltage and current reading.

This read-only command has 2 data bytes and is formatted in Linear_5s_11s format.

READ_PIN

The READ_PIN command is a reading of the DC/DC converter input power in Watts. PIN is calculated based on the most recent input voltage and current reading.

This read-only command has 2 data bytes and is formatted in Linear_5s_11s format.

MFR_PIN_ACCURACY

The MFR_PIN_ACCURACY command returns the accuracy, in percent, of the value returned by the READ_PIN command.

There is one data byte. The value is 0.1% per bit which gives a range of ±0.0% to ±25.5%.

This read-only command has one data byte and is formatted as an unsigned integer.

PMBus COMMAND DETAILS

MFR_IOUT_PEAK

The MFR_IOUT_PEAK command reports the highest current, in amperes, reported by the READ_IOUT measurement.

This command is cleared using the MFR_CLEAR_PEAKS command.

This read-only command has two data bytes and is formatted in Linear_5s_11s format.

MFR_VOUT_PEAK

The MFR_VOUT_PEAK command reports the highest voltage, in volts, reported by the READ_VOUT measurement.

This command is cleared using the MFR_CLEAR_PEAKS command.

This read-only command has two data bytes and is formatted in Linear_16u format.

MFR_VIN_PEAK

The MFR_VIN_PEAK command reports the highest voltage, in volts, reported by the READ_VIN measurement.

This command is cleared using the MFR_CLEAR_PEAKS command.

This read-only command has two data bytes and is formatted in Linear_5s_11s format.

MFR_TEMPERATURE_1_PEAK

The MFR_TEMPERATURE_1_PEAK command reports the highest temperature, in degrees Celsius, reported by the READ_TEMPERATURE_1 measurement.

This command is cleared using the MFR_CLEAR_PEAKS command.

This read-only command has two data bytes and is formatted in Linear_5s_11s format.

MFR_READ_IIN_PEAK

The MFR_READ_IIN_PEAK command reports the highest current, in Amperes, reported by the READ_IIN measurement.

This command is cleared using the MFR_CLEAR_PEAKS command.

This command has two data bytes and is formatted in Linear_5s_11s format.

MFR_READ_ICHIP

The MFR_READ_ICHIP command returns the measured input current, in Amperes, used by the LTC7132.

This command has two data bytes and is formatted in Linear_5s_11s format.

MFR_TEMPERATURE_2_PEAK

The MFR_TEMPERATURE_2_PEAK command reports the highest temperature, in degrees Celsius, reported by the READ_TEMPERATURE_2 measurement.

This command is cleared using the MFR_CLEAR_PEAKS command.

This read-only command has two data bytes and is formatted in Linear_5s_11s format.

MFR_ADC_CONTROL

The MFR_ADC_CONTROL command determines the ADC read back selection. A default value of 0 in the command runs the standard telemetry loop with all parameters updated in a round robin fashion with a typical latency of $t_{CONVERT}$. The user can command a non-zero value to monitored a single parameter with an approximate update rate of 8ms.

PMBus COMMAND DETAILS

This command has a latency of up to 2 ADC conversions or approximately 16ms (external temperature conversions may have a latency of up to 3 ADC conversion or approximately 24ms). It is recommended the part remain in standard telemetry mode except for special cases where fast ADC updates of a single parameter is required. The part should be commanded to monitor the desired parameter for a limited period of time (less then 1 second) then set the command back to standard round robin mode. If this command is set to any value except standard round robin telemetry (0) all warnings and faults associated with telemetry other than the selected parameter are effectively disabled and voltage servoing is disabled. When round robin is reasserted, all warnings and faults and servo mode are re-enabled.

COMMANDED VALUE	TELEMETRY COMMAND NAME	DESCRIPTION
0x0F		Reserved
0x0E		Reserved
0x0D		Reserved
0x0C	READ_TEMPERATURE_1	Channel 1 external temperature
0x0B		Reserved
0x0A	READ_IOUT	Channel 1 measured output current
0x09	READ_VOUT	Channel 1 measured output voltage
0x08	READ_TEMPERATURE_1	Channel 0 external temperature
0x07		Reserved
0x06	READ_IOUT	Channel 0 measured output current
0x05	READ_VOUT	Channel 0 measured output voltage
0x04	READ_TEMPERATURE_2	Internal junction temperature
0x03	READ_IIN	Measured input supply current
0x02	MFR_READ_ICHIP	Measured supply current of the LTC7132
0x01	READ_VIN	Measured input supply voltage
0x00		Standard ADC Round Robin Telemetry

If a reserved command value is entered, the telemetry will default to Internal IC Temperature and issue a CML fault. CML faults will continue to be issued by the LTC7132 until a valid command value is entered. The accuracy of the measured input supply voltage is only guaranteed if the MFR_ADC_CONTROL command is set to standard round robin telemetry.

This write-only command has 1 data byte and is formatted in register format.

MFR_REAL_TIME

The MFR_REAL_TIME command is the real-time clock value of the device with a resolution of 200µs. The value is synchronous to the share-clock. The format of the PMBus block read is as follows:

Format of the MFR_REAL_TIME

BYTE	BIT	DESCRIPTION
0		Length of the block read (fixed at 6)
1	[7:0]	LSB of the 48-bit real-time clock value
2	[15:8]	
3	[23:16]	
4	[31:24]	
5	[39:32]	
6	[47:40]	MSB of the 48-bit real-time clock value

This read-only command is in block format. The length will be 6. The value of this command is typically updated every 25ms.

PMBus COMMAND DETAILS

NVM MEMORY COMMANDS

Store/Restore

COMMAND NAME	CMD CODE	DESCRIPTION	TYPE	PAGED	FORMAT	UNITS	NVM	DEFAULT VALUE
STORE_USER_ALL	0x15	Store user operating memory to EEPROM.	Send Byte	N				NA
RESTORE_USER_ALL	0x16	Restore user operating memory from EEPROM.	Send Byte	N				NA
MFR_COMPARE_USER_ALL	0xF0	Compares current command contents with NVM.	Send Byte	N				NA

STORE_USER_ALL

The STORE_USER_ALL command instructs the PMBus device to copy the non-volatile user contents of the Operating Memory to the matching locations in the non-volatile User NVM memory.

Executing this command if the die temperature exceeds 85°C or is below 0°C is not recommended and the data retention of 10 years cannot be guaranteed. If the die temperature exceeds 130°C, the STORE_USER_ALL command is disabled. The command is re-enabled when the IC temperature drops below 125°C.

Communication with the LTC7132 and programming of the NVM can be initiated when $EXTV_{CC}$ or VDD33 is available and VIN is not applied. To enable the part in this state, using global address 0x5B write MFR_EE_UNLOCK to 0x2B followed by 0xC4. The LTC7132 will now communicate normally, and the project file can be updated. To write the updated project file to the NVM issue a STORE_USER_ALL command. When VIN is applied, a MFR_RESET must be issued to allow the PWM to be enabled and valid ADCs to be read.

This write-only command has no data bytes.

RESTORE_USER_ALL

The RESTORE_USER_ALL command instructs the LTC7132 to copy the contents of the non-volatile User memory to the matching locations in the Operating Memory. The values in the Operating Memory are overwritten by the value retrieved from the User commands. The LTC7132 ensures both channels are off, loads the operating memory from the internal EEPROM, clears all faults, reads the resistor configuration pins, and then performs a soft-start of both PWM channels if applicable.

STORE_USER_ALL, MFR_COMPARE_USER_ALL and RESTORE_USER_ALL commands are disabled if the die exceeds 130°C and are not re-enabled until the die temperature drops below 125°C.

This write-only command has no data bytes.

MFR_COMPARE_USER_ALL

The MFR_COMPARE_USER_ALL command instructs the PMBus device to compare current command contents with what is stored in non-volatile memory. If the compare operation detects differences, a CML bit 0 fault will be generated.

This write-only command has no data bytes.

PMBus COMMAND DETAILS

Fault Logging

COMMAND NAME	CMD CODE	DESCRIPTION	TYPE	PAGED	DATA FORMAT	UNITS	NVM	DEFAULT VALUE
MFR_FAULT_LOG	0xEE	Fault log data bytes.	R Block	N	CF		Y	NA
MFR_FAULT_LOG_ STORE	0xEA	Command a transfer of the fault log from RAM to EEPROM.	Send Byte	N				NA
MFR_FAULT_LOG_CLEAR	0xEC	Initialize the EEPROM block reserved for fault logging.	Send Byte	N				NA

MFR_FAULT_LOG

The MFR_FAULT_LOG command allows the user to read the contents of the FAULT_LOG after the first fault occurrence since the last MFR_FAULT_LOG_CLEAR command was written. The contents of this command are stored in non-volatile memory, and are cleared by the MFR_FAULT_LOG_CLEAR command. The length and content of this command are listed in Table 13. If the user accesses the MFR_FAULT_LOG command and no fault log is present, the command will return a data length of 0. If a fault log is present, the MFR_FAULT_LOG will return a block of data 147 bytes long. If a fault occurs within the first second of applying power, some of the earlier pages in the fault log may not contain valid data.

NOTE: The approximate transfer time for this command is 3.4ms using a 400kHz clock.

This read-only command is in block format.

MFR_FAULT_LOG_STORE

The MFR_FAULT_LOG_STORE command forces the fault log operation to be written to NVM just as if a fault event occurred. This command will set bit 3 of the STATUS_MFR_SPECIFIC fault if bit 7 “Enable Fault Logging” is set in the MFR_CONFIG_ALL command.

If the die temperature exceeds 130°C, the MFR_FAULT_LOG_STORE command is disabled until the IC temperature drops below 125°C.

This write-only command has no data bytes.

Table 13. Fault Logging

This table outlines the format of the block data from a read block data of the MFR_FAULT_LOG command.

Data Format Definitions				LIN 11 = PMBus = Rev 1.2, Part 2, section 7.1
				LIN 16 = PMBus Rev 1.2, Part 2, section 8. Mantissa portion only
				BYTE = 8 bits interpreted per definition of this command
DATA	**BITS**	**DATA FORMAT**	**BYTE NUM**	**BLOCK READ COMMAND**
Block Length		BYTE	147	The MFR_FAULT_LOG command is a fixed length of 147 bytes The block length will be zero if a data log event has not been captured
HEADER INFORMATION				
Fault Log Preface	[7:0]	ASC	0	Returns LTxx beginning at byte 0 if a partial or complete fault log exists. Word xx is a factory identifier that may vary part to part.
	[7:0]		1	
	[15:8]	Reg	2	
	[7:0]		3	
Fault Source	[7:0]	Reg	4	Refer to Table 13a.

PMBus COMMAND DETAILS

MFR_REAL_TIME	[7:0]	Reg	5	48 bit share-clock counter value when fault occurred (200µs resolution).
	[15:8]		6	
	[23:16]		7	
	[31:24]		8	
	[39:32]		9	
	[47:40]		10	
MFR_VOUT_PEAK (PAGE 0)	[15:8]	L16	11	Peak READ_VOUT on Channel 0 since last power-on or CLEAR_PEAKS command.
	[7:0]		12	
MFR_VOUT_PEAK (PAGE 1)	[15:8]	L16	13	Peak READ_VOUT on Channel 1 since last power-on or CLEAR_PEAKS command.
	[7:0]		14	
MFR_IOUT_PEAK (PAGE 0)	[15:8]	L11	15	Peak READ_IOUT on Channel 0 since last power-on or CLEAR_PEAKS command.
	[7:0]		16	
MFR_IOUT_PEAK (PAGE 1)	[15:8]	L11	17	Peak READ_IOUT on Channel 1 since last power-on or CLEAR_PEAKS command.
	[7:0]		18	
MFR_VIN_PEAK	[15:8]	L11	19	Peak READ_VIN since last power-on or CLEAR_PEAKS command.
	[7:0]		20	
READ_TEMPERATURE1 (PAGE 0)	[15:8]	L11	21	External temperature sensor 0 during last event.
	[7:0]		22	
READ_TEMPERATURE1 (PAGE 1)	[15:8]	L11	23	External temperature sensor 1 during last event.
	[7:0]		24	
READ_TEMPERATURE2	[15:8]	L11	25	LTC7132 die temperature sensor during last event.
	[7:0]		26	
CYCLICAL DATA				
EVENT n **(Data at Which Fault Occurred; Most Recent Data)**				Event “n” represents one complete cycle of ADC reads through the MUX at time of fault. Example: If the fault occurs when the ADC is processing step 15, it will continue to take readings through step 25 and then store the header and all 6 event pages to EEPROM
READ_VOUT (PAGE 0)	[15:8]	LIN 16	27	
	[7:0]	LIN 16	28	
READ_VOUT (PAGE 1)	[15:8]	LIN 16	29	
	[7:0]	LIN 16	30	
READ_IOUT (PAGE 0)	[15:8]	LIN 11	31	
	[7:0]	LIN 11	32	
READ_IOUT (PAGE 1)	[15:8]	LIN 11	33	
	[7:0]	LIN 11	34	
READ_VIN	[15:8]	LIN 11	35	
	[7:0]	LIN 11	36	
READ_IIN	[15:8]	LIN 11	37	
	[7:0]	LIN 11	38	
STATUS_VOUT (PAGE 0)		BYTE	39	
STATUS_VOUT (PAGE 1)		BYTE	40	
STATUS_WORD (PAGE 0)	[15:8]	WORD	41	
	[7:0]	WORD	42	
STATUS_WORD (PAGE 1)	[15:8]	WORD	43	
	[7:0]	WORD	44	
STATUS_MFR_SPECIFIC (PAGE 0)		BYTE	45	
STATUS_MFR_SPECIFIC (PAGE 1)		BYTE	46	

PMBus COMMAND DETAILS

EVENT n-1 (data measured before fault was detected)				
READ_VOUT (PAGE 0)	[15:8]	LIN 16	47	
	[7:0]	LIN 16	48	
READ_VOUT (PAGE 1)	[15:8]	LIN 16	49	
	[7:0]	LIN 16	50	
READ_IOUT (PAGE 0)	[15:8]	LIN 11	51	
	[7:0]	LIN 11	52	
READ_IOUT (PAGE 1)	[15:8]	LIN 11	53	
	[7:0]	LIN 11	54	
READ_VIN	[15:8]	LIN 11	55	
	[7:0]	LIN 11	56	
READ_IIN	[15:8]	LIN 11	57	
	[7:0]	LIN 11	58	
STATUS_VOUT (PAGE 0)		BYTE	59	
STATUS_VOUT (PAGE 1)		BYTE	60	
STATUS_WORD (PAGE 0)	[15:8]	WORD	61	
	[7:0]	WORD	62	
STATUS_WORD (PAGE 1)	[15:8]	WORD	63	
	[7:0]	WORD	64	
STATUS_MFR_SPECIFIC (PAGE 0)		BYTE	65	
STATUS_MFR_SPECIFIC (PAGE 1)		BYTE	66	
*				
*				
*				
EVENT n-5 (Oldest Recorded Data)				
READ_VOUT (PAGE 0)	[15:8]	LIN 16	127	
	[7:0]	LIN 16	128	
READ_VOUT (PAGE 1)	[15:8]	LIN 16	129	
	[7:0]	LIN 16	130	
READ_IOUT (PAGE 0)	[15:8]	LIN 11	131	
	[7:0]	LIN 11	132	
READ_IOUT (PAGE 1)	[15:8]	LIN 11	133	
	[7:0]	LIN 11	134	
READ_VIN	[15:8]	LIN 11	135	
	[7:0]	LIN 11	136	
READ_IIN	[15:8]	LIN 11	137	
	[7:0]	LIN 11	138	
STATUS_VOUT (PAGE 0)		BYTE	139	
STATUS_VOUT (PAGE 1)		BYTE	140	
STATUS_WORD (PAGE 0)	[15:8]	WORD	141	
	[7:0]	WORD	142	
STATUS_WORD (PAGE 1)	[15:8]	WORD	143	
	[7:0]	WORD	144	
STATUS_MFR_SPECIFIC (PAGE 0)		BYTE	145	
STATUS_MFR_SPECIFIC (PAGE 1)		BYTE	146	

PMBus COMMAND DETAILS

Table 13a. Explanation of Position_Fault Values

POSITION_FAULT VALUE	SOURCE OF FAULT LOG
0xFF	MFR_FAULT_LOG_STORE
0x00	TON_MAX_FAULT
0x01	VOUT_OV_FAULT
0x02	VOUT_UV_FAULT
0x03	IOUT_OC_FAULT
0x05	TEMP_OT_FAULT
0x06	TEMP_UT_FAULT
0x07	VIN_OV_FAULT
0x0A	MFR_TEMP_2_OT_FAULT

MFR_FAULT_LOG_CLEAR

The MFR_FAULT_LOG_CLEAR command will erase the fault log file stored values. It will also clear bit 3 in the STATUS_MFR_SPECIFIC command. After a clear is issued, the status can take up to 8ms to clear.

This write-only command is send bytes.

Block Memory Write/Read

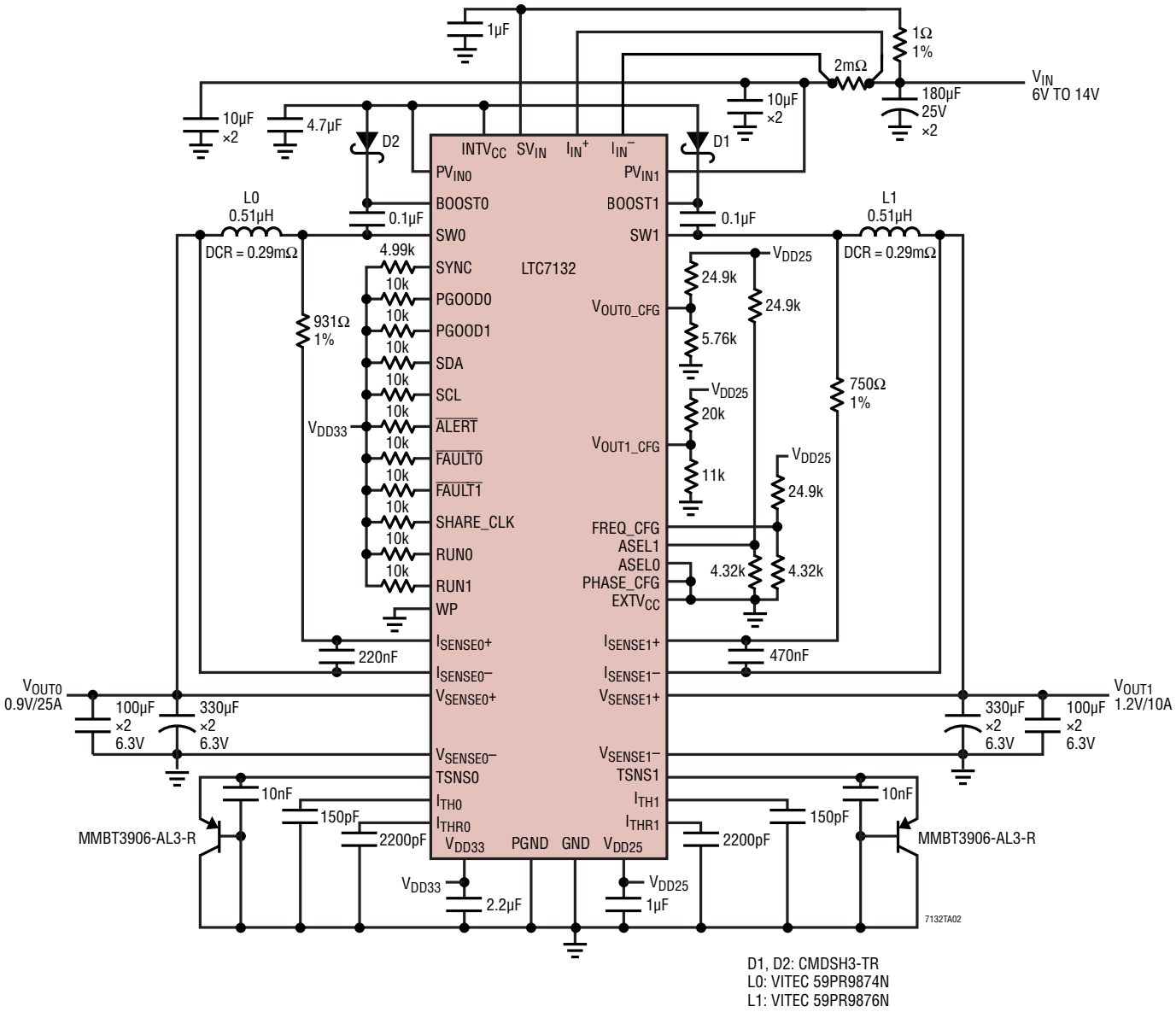
COMMAND NAME	CMD CODE	DESCRIPTION	TYPE	PAGED	DATA FORMAT	UNITS	NVM	DEFAULT VALUE
MFR_EE_UNLOCK	0xBD	Unlock user EEPROM for access by MFR_EE_ERASE and MFR_EE_DATA commands.	R/W Byte	N	Reg			NA
MFR_EE_ERASE	0xBE	Initialize user EEPROM for bulk programming by MFR_EE_DATA.	R/W Byte	N	Reg			NA
MFR_EE_DATA	0xBF	Data transferred to and from EEPROM using sequential PMBus word reads or writes. Supports bulk programming.	R/W Word	N	Reg			NA

All the NVM commands are disabled if the die temperature exceeds 130°C. NVM commands are re-enabled when the die temperature drops below 125°C.

MFR_EE_xxxx

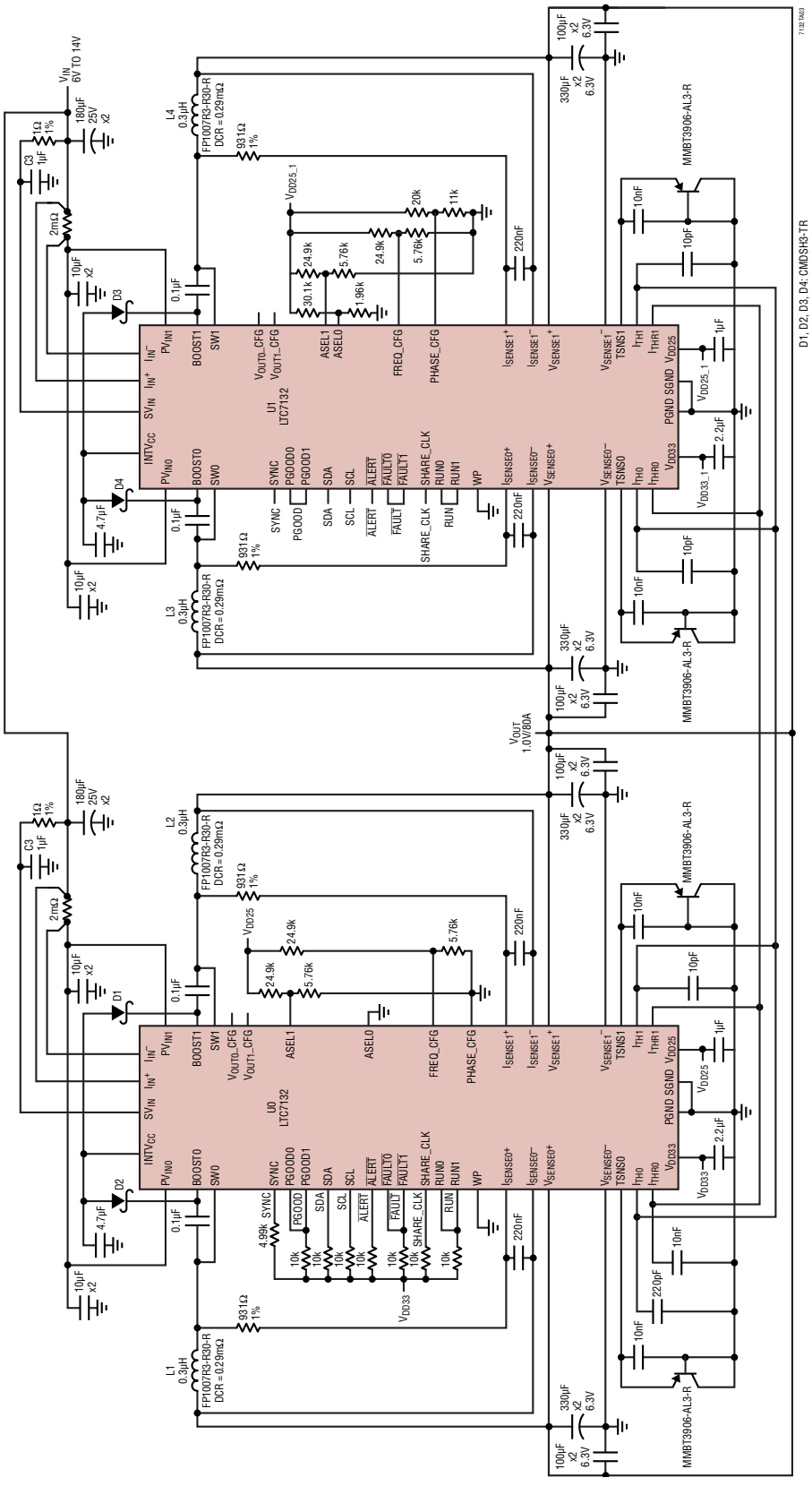
The MFR_EE_xxxx commands facilitate bulk programming of the LTC7132 internal EEPROM. Contact the factory for details.

TYPICAL APPLICATIONS

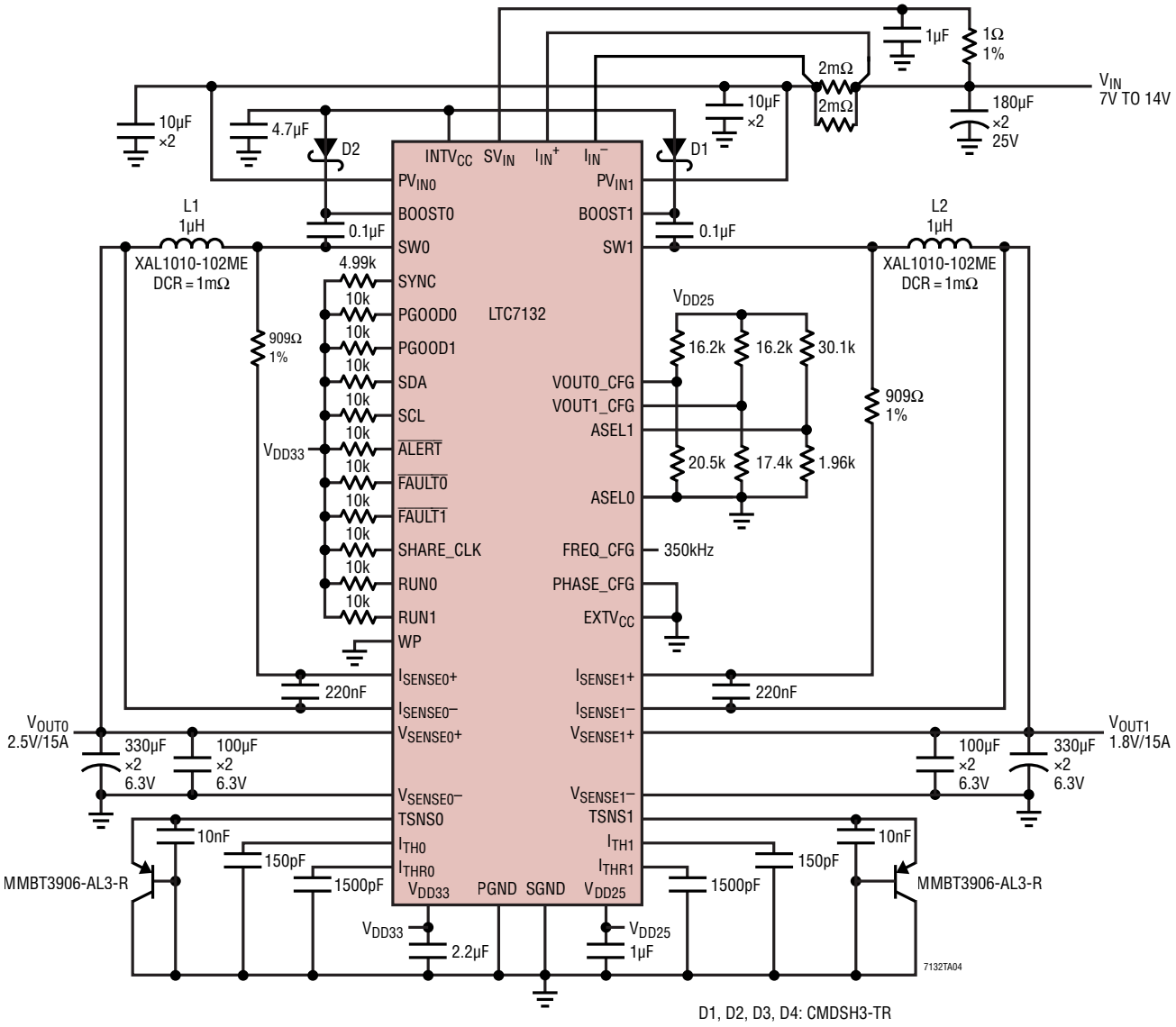


High Efficiency, Ultralow DCR Sense Dual-Output 0.9V/25A and 1.2V/10A, 425 kHz Buck Converter

TYPICAL APPLICATIONS

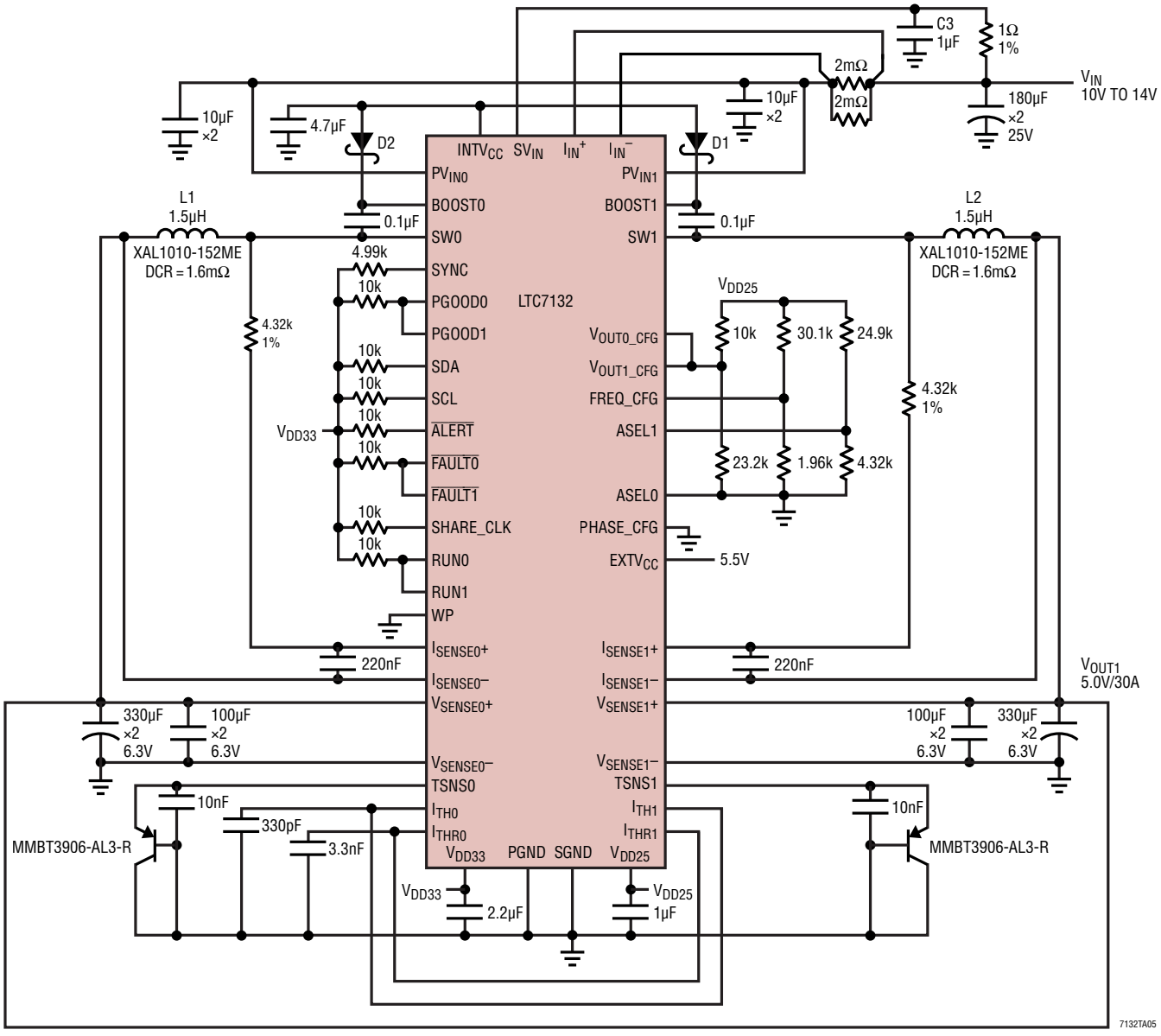


TYPICAL APPLICATIONS



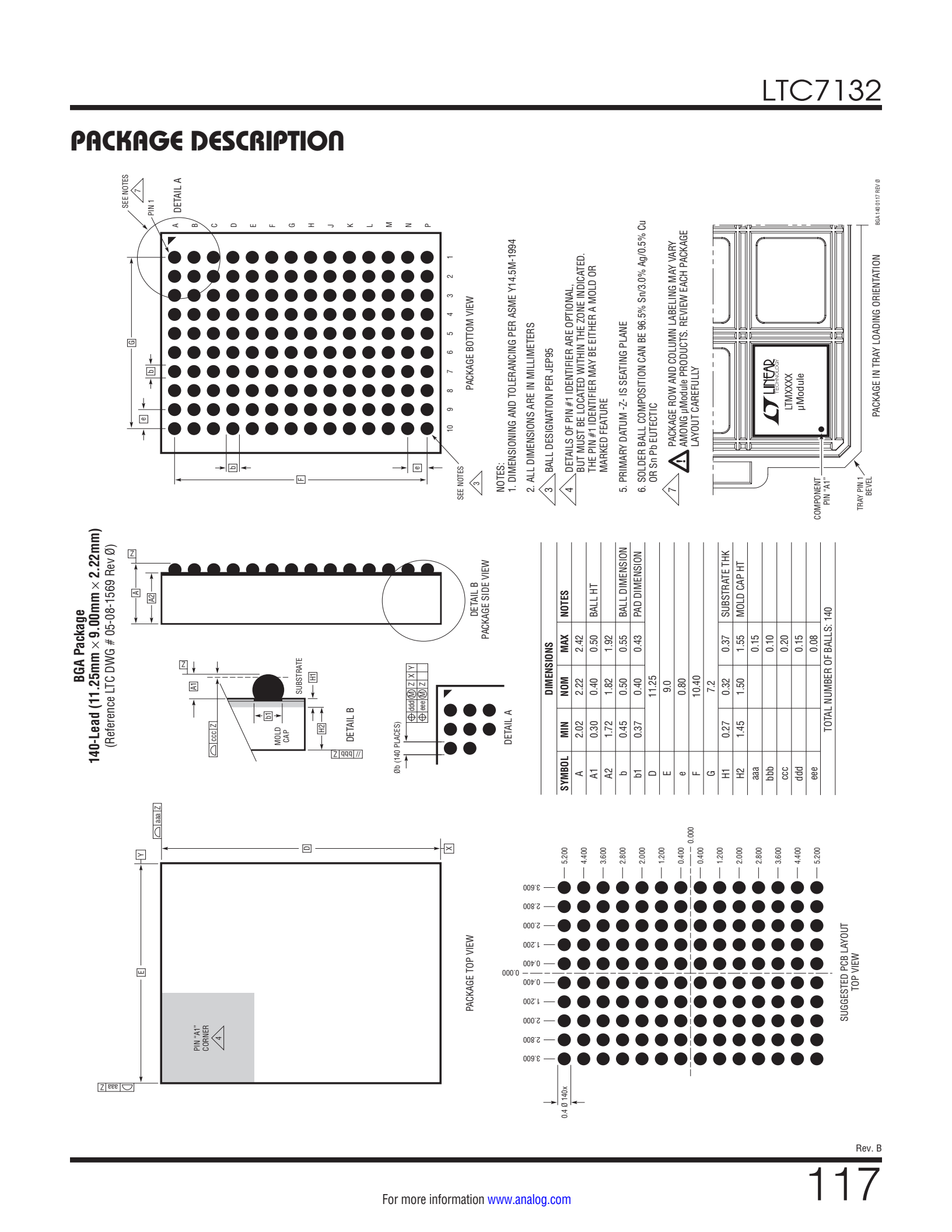
High Efficiency, 350kHz, Dual-Output, 2.5V/15A and 1.8V/15A Buck Converter

TYPICAL APPLICATIONS



High Efficiency, Typical DCR Current Sense, 250kHz, Dual Phase Single-Output, 5V/30A Buck Converter

PACKAGE DESCRIPTION



DIMENSIONS				
SYMBOL	MIN	NOM	MAX	NOTES
A	2.02	2.22	2.42	
A1	0.30	0.40	0.50	BALL HT
A2	1.72	1.82	1.92	
b	0.45	0.50	0.55	BALL DIMENSION
b1	0.37	0.40	0.43	PAD DIMENSION
D		11.25		
E		9.0		
e		0.80		
F		10.40		
G		7.2		
H1	0.27	0.32	0.37	SUBSTRATE THK
H2	1.45	1.50	1.55	MOLD CAP HT
aaa			0.15	
bbb			0.10	
ccc			0.20	
ddd			0.15	
eee			0.08	
TOTAL NUMBER OF BALLS: 140				

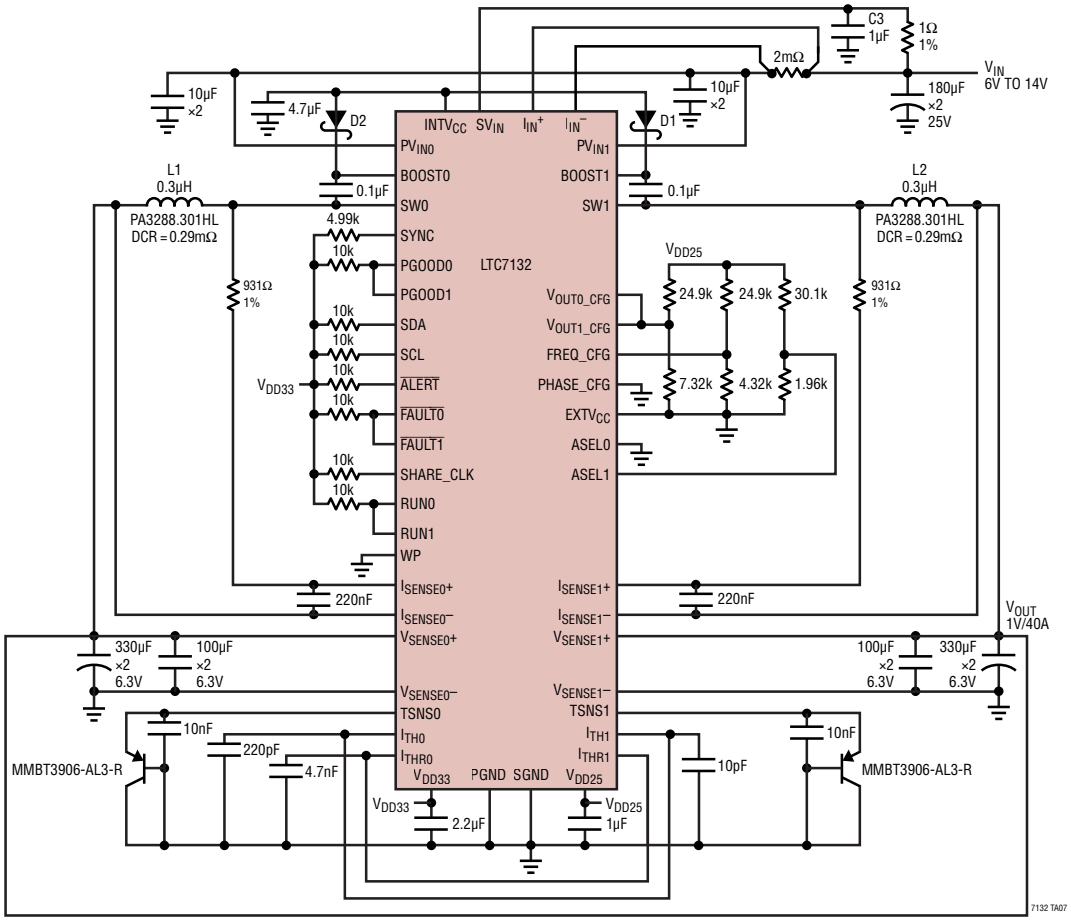
Rev. B

REVISION HISTORY

REV	DATE	DESCRIPTION	PAGE NUMBER
A	4/24	Updated Absolute Maximum Ratings	4
B	11/25	Updated Figure 2	17

TYPICAL APPLICATION

Low DCR Sensing, 425kHz, Dual Phase Single-Output, 1V/40A Buck Converter



RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LTM4676A	Dual 13A or Single 26A Step-Down DC/DC µModule Regulator with Digital Power System Management	4.5V ≤ V_{IN} ≤17V; 0.5V ≤ V_{OUT} (±0.5%) ≤ 5.5V, I^2C/PMBus Interface, 16mm × 16mm × 5mm, BGA Package
LTM4675	Dual 9A or Single 18A µModule Regulator with Digital Power System Management	4.5V ≤ V_{IN} ≤17V; 0.5V ≤ V_{OUT} (±0.5%) ≤ 5.5V, I^2C/PMBus Interface, 11.9mm × 16mm × 5mm, BGA Package
LTM4677	Dual 18A or Single 36A µModule Regulator with Digital Power System Management	4.5V ≤ V_{IN} ≤ 16V; 0.5V ≤ V_{OUT} (±0.5%) ≤ 1.8V, I^2C/PMBus Interface, 16mm × 16mm × 5.01mm, BGA Package
LTC3874	Multiphase Step-Down Synchronous Slave Controller with Sub MilliOhm DCR Sensing	4.5V ≤ V_{IN} ≤ 38V, V_{OUT} up to 5.5V, Very High Output Current, Accurate Current Sharing, Current Mode Applications
LTC3887/ LTC3887-1	Dual Output Multiphase Step-Down DC/DC Controller with Digital Power System Management, 70mS Start-Up	4.5V ≤ V_{IN} ≤ 24V, 0.5V ≤ $V_{OUT0,1}$ (±0.5%) ≤ 5.5V, 70mS Start-Up, I^2C/ PMBus Interface, –1 Version uses DrMOS or Power Blocks
LTC3882/ LTC3882-1	Dual Output Multiphase Step-Down DC/DC Voltage Mode Controller with Digital Power System Management	3V ≤ V_{IN} ≤ 38V, 0.5V ≤ $V_{OUT1,2}$ ≤ 5.25V, (±0.5%) V_{OUT} Accuracy I^2C/ PMBus Interface, uses DrMOS or Power Blocks
LTC3886	60V Dual Output Step-Down Controller with Digital Power System Management	4.5V ≤ V_{IN} ≤ 60V, 0.5V ≤ $V_{OUT0,1}$ (±0.5%) ≤ 13.8V, 70mS Start-Up, I^2C/ PMBus Interface, Input Current Sense
LTC3815	6A Monolithic Synchronous DC/DC Step-Down Converter with Digital Power System Management	2.25V ≤ V_{IN} ≤ 5.5V, 0.4V ≤ V_{OUT} ≤ 0.72V_{IN}, Programmable V_{OUT} Range ±25% with 0.1% Resolution, Up to 3MHz Operation with 13-Bit ADC