15V, ±5A Rail-to-Rail Synchronous Buck Regulator

FEATURES

- Resistor Programmable Voltage:
  V_{OUT}: 0V to V_{IN} – 0.5V
  V_{OUT} Pin: 0 to ISET
- Silent Switcher® Architecture
- I_{SET} Accuracy: ±1%
- Tight V_{OUT} Regulation Across V_{OUT} Range
- Output Current Monitor Accuracy: ±5%
- Programmable Wire Drop Compensation
- Easy to Parallel for Higher Current and Heat Spreading
- Input Supply Voltage Regulation Loop
- High Efficiency: Up to 96%
- Output Current: ±5A
- Integrated N-MOSFETs (60mΩ Top & 30mΩ Bottom)
- Adjustable Switching Frequency: 400kHz to 4MHz
- V_{IN} Range: 4V to 15V
- Current Mode Operation for Excellent Line and Load Transient Response
- Shutdown Mode Draws Less Than 1µA Supply Current
- Low Profile 24-Lead 3mm × 5mm QFN Package

APPLICATIONS

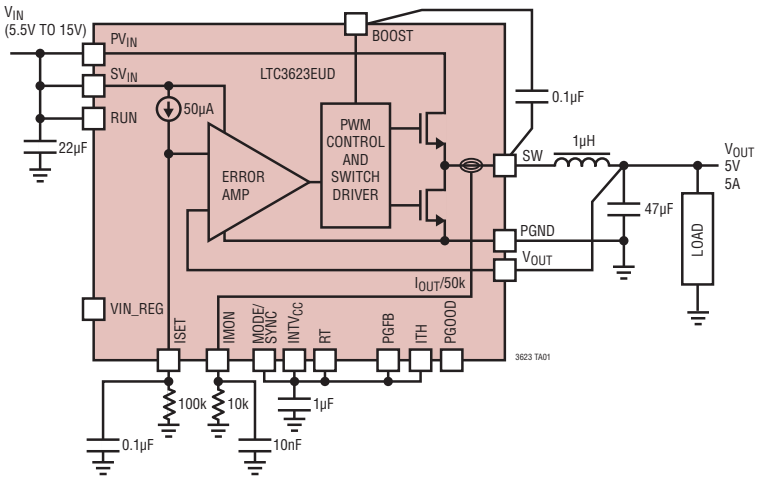
- Tracking Supply or DDR Memory Supply
- ASIC Substrate Biasing
- Point-of-Load (POL) Power Supply
- Portable Instruments, Battery-Powered Equipment
- Thermo Electric Cooler (TEC) Systems

DESCRIPTION

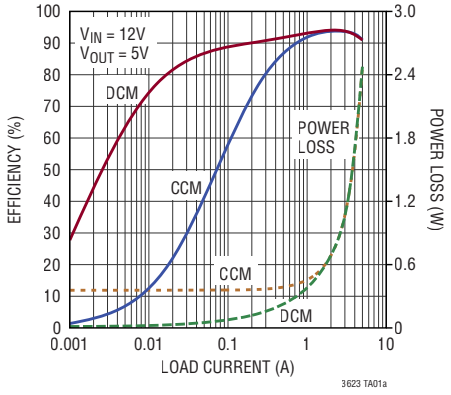
The LTC®3623 is a high efficiency, monolithic synchronous buck regulator in which the output voltage is programmed with a single external resistor. The accurate internally generated 50µA current source on the ISET pin allows the user to program an output voltage through an external R_{ISET} resistor or directly drive the ISET pin with an external voltage supply up to 9V to program the converter's V_{OUT}. The V_{OUT} voltage is fed directly back to the error amplifier to be regulated to the ISET voltage. The operating supply voltage range for the SV_{IN} pin is from 15V down to 4V, while the PV_{IN} pin's voltage range is 15V down to 1.5V, making it suitable for dual Li-Ion batteries and for taking power from a 12V or 5V rail.

The operating frequency is programmable from 400kHz to 4MHz with an external R_T resistor. Higher switching frequency allows the use of smaller surface mount inductors while lower frequency allows for higher power efficiency. The unique constant-frequency/controlled on-time architecture is ideal for high step-down ratio applications that are operating at high frequency while demanding fast transient response.

TYPICAL APPLICATION



Efficiency and Power Loss vs Load Current



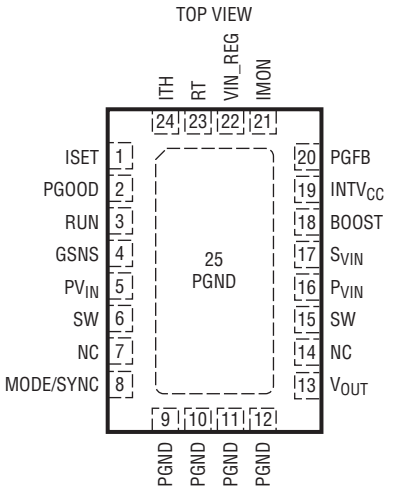
Rev. B

ABSOLUTE MAXIMUM RATINGS

(Note 1)

PV_{IN}, SV_{IN} Voltage ..... –0.3V to 17V
V_{OUT}, ISET Voltage.....–0.3 to V_{IN}
BOOST Voltage ..... SW –0.3V to SW+6V
RUN Voltage..... –0.3V to SV_{IN}
MODE/SYNC Voltage ..... –0.3V to 6V
ITH, RT, VIN_REG Voltage .....–0.3V to $INTV_{CC}$
IMON, PGOOD, PGFB Voltage .....–0.3V to $INTV_{CC}$
GSNS Voltage .....–0.3V to 12V
Operating Junction Temperature Range
(Notes 4, 5)..... –40°C to 125°C

PIN CONFIGURATION



UDD PACKAGE
24-LEAD (3mm × 5mm) PLASTIC QFN

T_{JMAX} = 125°C, θ_{JA} = 36°C/W
EXPOSED PAD (PIN 25) IS GND, MUST BE SOLDERED TO PCB

ORDER INFORMATION

LEAD FREE FINISH	TAPE AND REEL	PART MARKING	PACKAGE DESCRIPTION	TEMPERATURE RANGE
LTC3623EUDD#PBF	LTC3623EUDD#TRPBF	LGMW	24-Lead (3mm × 5mm) Plastic QFN	–40°C to 125°C
LTC3623IUDD#PBF	LTC3623IUDD#TRPBF	LGMW	24-Lead (3mm × 5mm) Plastic QFN	–40°C to 125°C

Contact the factory for specified parts with wider operating temperature ranges.

*The temperature grade is identified by a label on the shipping container.

For more information on lead free part marking, refer to: https://www.analog.com/en/support/quality-and-reliability/product-stewardship/material-declarations.html
For more information on tape and reel specifications, refer to: https://www.analog.com/media/en/package-pcb-resources/package/tape-reel-rev-o.pdf.
Some packages are available in 500 unit reels through designated sales channels with #TRMPBF suffix.

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the specified operating junction temperature range, otherwise specifications are at T_A = 25°C. (Note 4) V_{IN} = 12V, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
SV_{IN}	Signal V_{IN} Supply Range			4		15	V
PV_{IN}	Power V_{IN} Supply Range			1.5		15	V
V_{OUT}	V_{OUT} Range (Note 6)	V_{IN} = 15V		0		14.5	V
V_{OUT} Pin	V_{OUT} Pin Voltage Range (Note 6)	V_{IN} = 15V		0		ISET	V
I_{ISET}	Reference Current	25°C 25°C to 130°C –45°C to 25°C	 ● ●	49.5 49 49.5	50 50 50	50.5 50.5 51.5	µA µA µA
ISET	ISET Dropout Voltage	V_{IN} – ISET			360		mV
	ISET Line Regulation	V_{IN} = 5V to 15V	●	–10		10	nA/V
	ISET Load Regulation (Note 6)	I_{LOAD} = 0 to 5A			0.5		%
	V_{OUT} Load Regulation	I_{TH} = 0.9V to 1.6V			0.05		%
	EA's Input Offset	ISET = 3V		–4.5		4.5	mV
g_m (EA)	Error Amplifier Transconductance	ITH = 1.2V		0.21	0.28	0.35	mS
I_Q	Input DC Supply Current (Note 2) Shutdown Discontinuous	 RUN = 0 Mode = 0, R_T = 33.2k			 0 1.45	 5 1.75	 µA mA
$t_{on(min)}$	Minimum On Time (Note 6)				30		ns
$t_{off(min)}$	Minimum Off Time (Note 6)				100		ns
I_{LIM}	Current Limit		●	5.2	6.2	7.4	A
	Negative Current Limit			–5	–6.5	–9	
R_{TOP}	Top Switch ON Resistance				60		mΩ
R_{BOTTOM}	Bottom Switch On Resistance				30		mΩ
V_{INTVCC}	Internal V_{CC} Voltage	5.5V < V_{IN} < 15V			5		V
V_{UVLO}	$INTV_{CC}$ Undervoltage Lockout Threshold	$INTV_{CC}$ Rising		3.6	3.8	4	V
	UVLO Hysteresis				0.36		V
V_{RUN}	Run Threshold Run Hysteresis	RUN Rising	●	1.2	1.45 0.34	1.67	V V
	Run Leakage	RUN = 15V			0	1	µA
	$INTV_{CC}$ Load Regulation	I_{LOAD} = 0 to 20mA			0.5		%
OV	Output Overvoltage PGFB Upper Threshold	PGFB Rising		0.585	0.63	0.67	V
	PGFB OV Hysteresis				15		mV
UV	Output Undervoltage PGFB Lower Threshold	PGFB Falling		0.5	0.54	0.575	V
	PGFB UV Hysteresis				15		mV
R_{PGOOD}	PGOOD Pull-Down Resistance	5mA Load			100		Ω
	PGOOD Leakage					1	µA
f_{OSC}	Frequency	R_T = 33.2k R_T = $INTV_{CC}$	●	0.94 0.75	1 1	1.07 1.22	MHz MHz

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the specified operating junction temperature range, otherwise specifications are at T_A = 25°C. (Note 4) V_{IN} = 12V, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
	MODE/SYNC Threshold	MODE $V_{IL(MAX)}$				0.4	V
		MODE $V_{IH(MIN)}$		4.5			V
		SYNC $V_{IH(MIN)}$		2.5			V
		SYNC $V_{IL(MAX)}$				0.4	V
	MODE/SYNC Pin Current	MODE/SYNC = 5V			10		µA
VIN_REG	Input Voltage Regulation Reference (Note 6)				1.45		V
	V_{OUT} Resistance to GND				600		kΩ
VINOV	V_{IN} Overvoltage Lockout	V_{IN} Rising		15.5	16.8		V
	V_{IN} 0V Hystersis				1.4		V
I_{IMON}	I_{MON} Current Limit Threshold			2.15	2.35	2.55	V
	IMON Gain	I_{LOAD} = 5A, Not Switching		20	21	22	µA/A

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime. Absolute Maximum Ratings are those values beyond which the life of a device may be impaired.

Note 2: Dynamic supply current is higher due to the internal gate charge being delivered at the switching frequency.

Note 3: The LTC3623 is tested in a feedback loop that adjusts V_{OUT} to achieve a specified error amplifier output voltage (I_{TH}).

Note 4: The LTC3623 is tested under pulsed load conditions such that $T_J \approx T_A$. The LTC3623E is guaranteed to meet performance specifications from 0°C to 85°C junction temperature. Specifications over the –40°C to 125°C operating junction temperature range are assured by design, characterization and correlation with statistical process controls. The LTC3623I is guaranteed over the full –40°C to 125°C operating junction temperature range. Note that the maximum ambient temperature consistent with these specifications is determined by specific operating conditions in conjunction with board layout, the rated package thermal impedance and other environmental factors. The junction temperature (T_J, in °C) is calculated from the ambient temperature (T_A, in °C) and power dissipation (P_D, in watts) according to the formula:

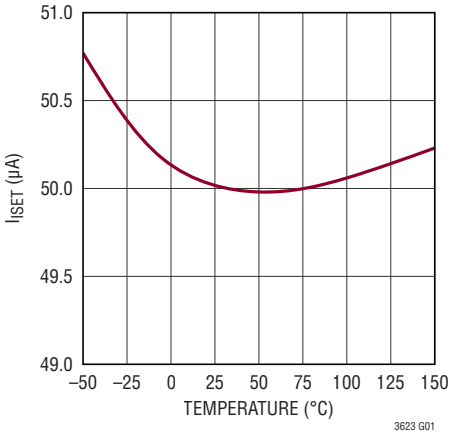
$T_J = T_A + (P_D \bullet \theta_{JA})$, where θ_{JA} (in °C/W) is the package thermal impedance.

Note 5: This IC includes overtemperature protection that is intended protect the device during momentary overload conditions. Junction temperature will exceed 125°C when overtemperature protection is active. Continuous operation above the specified maximum operating junction temperature may impair device reliability.

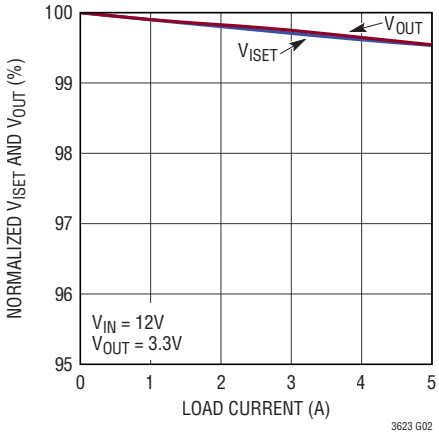
Note 6: Guaranteed by design.

TYPICAL PERFORMANCE CHARACTERISTICS T_A = 25°C, unless otherwise noted.

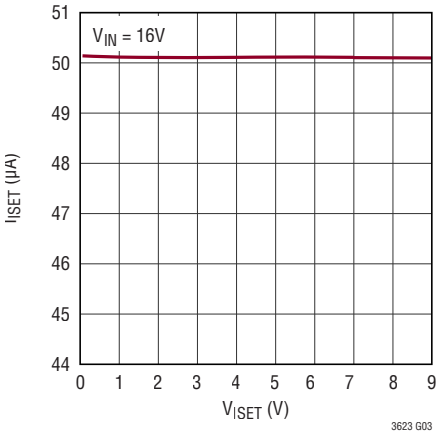
ISET Current vs. Temperature



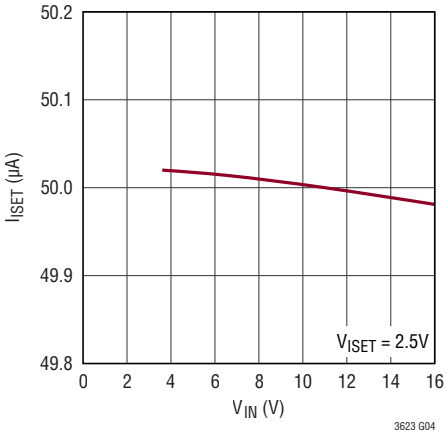
Load Regulation



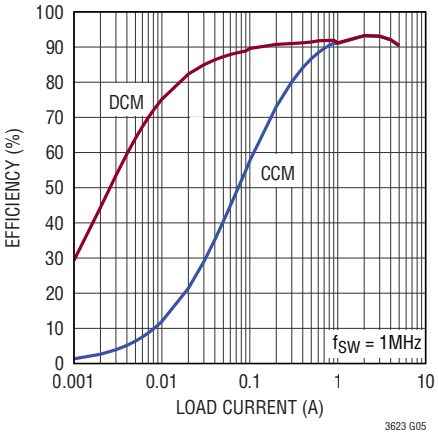
ISET Current vs V_{ISET}



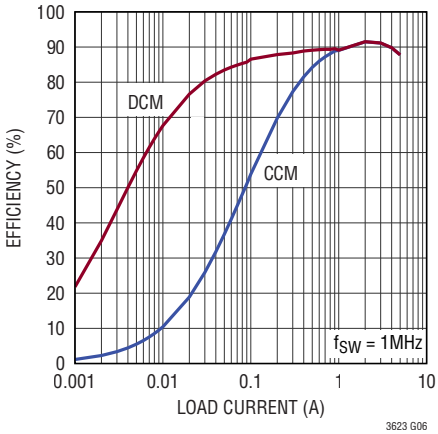
ISET Current Line Regulation



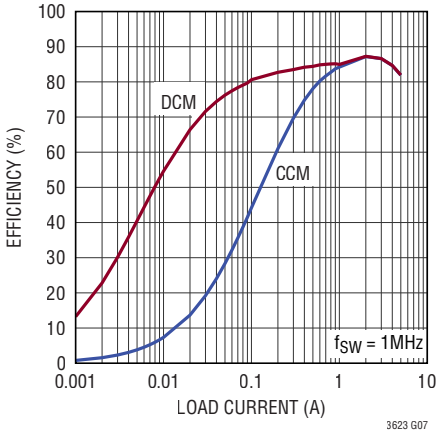
Efficiency vs Load Current V_{OUT} = 5V, V_{IN} = 12V



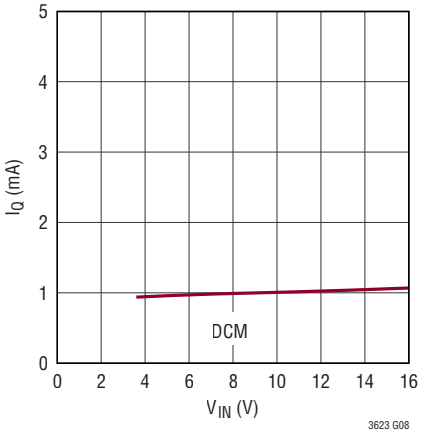
Efficiency vs Load Current V_{OUT} = 3.3V, V_{IN} = 12V



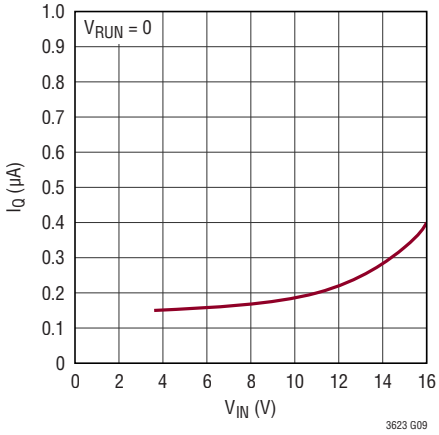
Efficiency vs Load Current V_{OUT} = 1.8V, V_{IN} = 12V



Quiescent Current vs V_{IN}

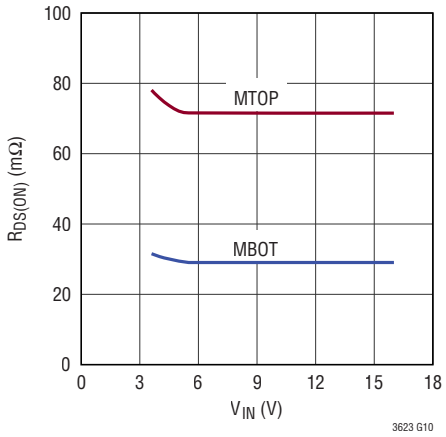


Shutdown Current vs V_{IN}

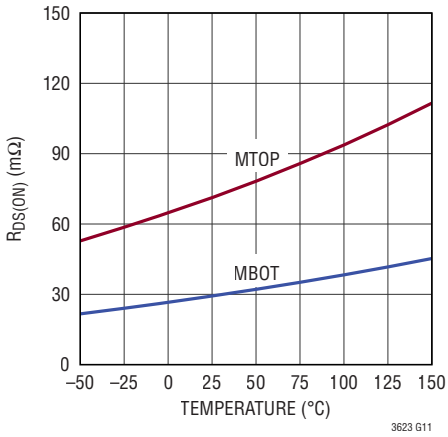


TYPICAL PERFORMANCE CHARACTERISTICS T_A = 25°C, unless otherwise noted.

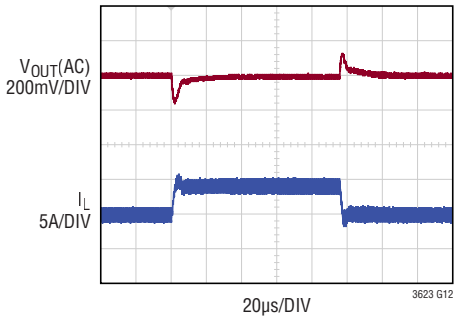
$R_{DS(ON)}$ vs V_{IN}



$R_{DS(ON)}$ vs Temperature

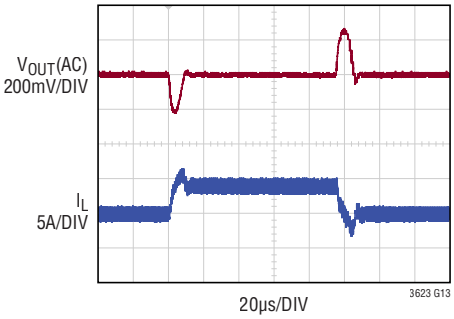


Transient Response CCM Operation, External Compensation



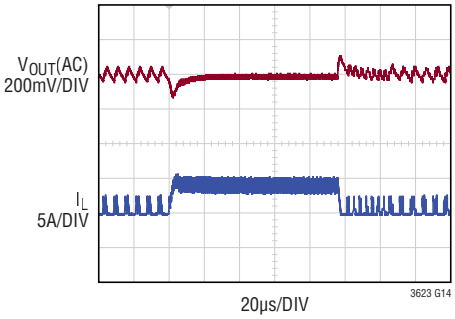
V_{IN} = 12V
V_{OUT} = 3.3V
I_{OUT} = 0A TO 4A
L = 1.2µH
f_{SW} = 1MHz
R_{ITH} = 20kΩ, C_{ITH} = 470pF
MODE = $INTV_{CC}$
C_{OUT} = 47µF

Transient Response CCM Operation, Internal Compensation



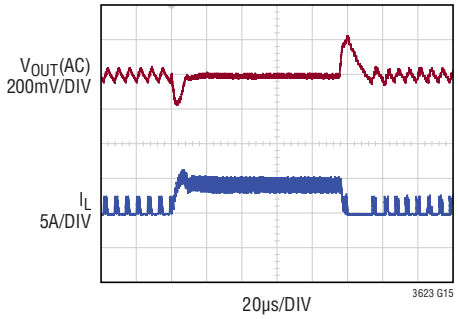
V_{IN} = 12V
V_{OUT} = 3.3V
I_{OUT} = 0A TO 4A
L = 1.2µH
f_{SW} = 1MHz
ITH = $INTV_{CC}$
MODE = $INTV_{CC}$
C_{OUT} = 47µF

Transient Response DCM Operation, External Compensation



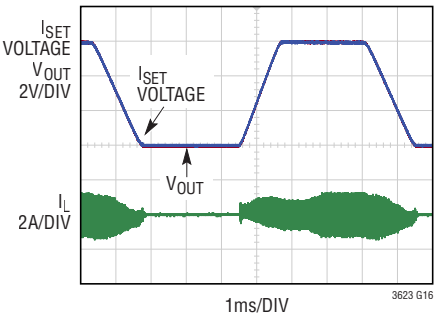
V_{IN} = 12V
V_{OUT} = 3.3V
I_{OUT} = 0.5A TO 4A
L = 1.2µH
f_{SW} = 1MHz
R_{ITH} = 20kΩ, C_{ITH} = 470pF
MODE = 0V
C_{OUT} = 47µF

Transient Response DCM Operation, Internal Compensation

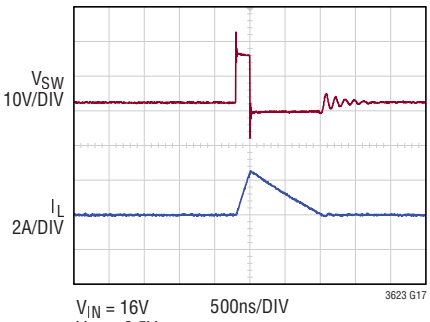


V_{IN} = 12V
V_{OUT} = 3.3V
I_{OUT} = 0.5A TO 4A
L = 1.2µH
f_{SW} = 1MHz
ITH = $INTV_{CC}$
MODE = 0V
C_{OUT} = 47µF

Output Tracking

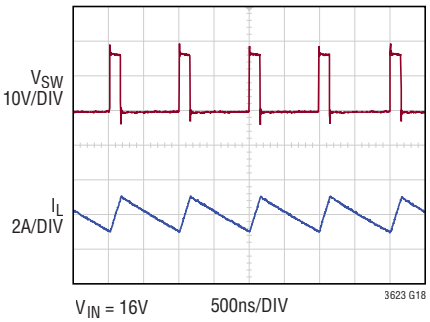


Discontinuous Conduction Mode (DCM) Operation



V_{IN} = 16V
V_{OUT}=2.5V
MODE=0V
L=1.0µH

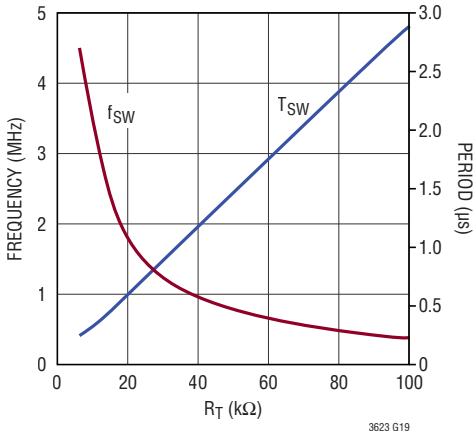
Continuous Conduction Mode (CCM) Operation



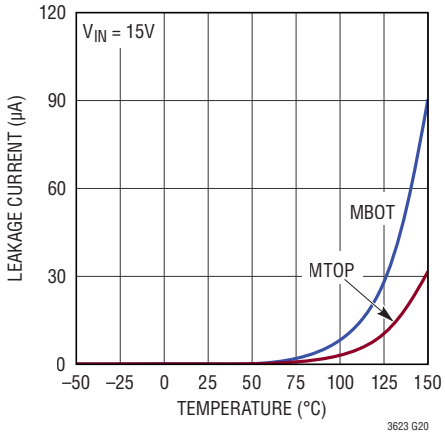
V_{IN} = 16V
V_{OUT}=2.5V
MODE=$INTV_{CC}$
L=1.0µH

TYPICAL PERFORMANCE CHARACTERISTICS T_A = 25°C, unless otherwise noted.

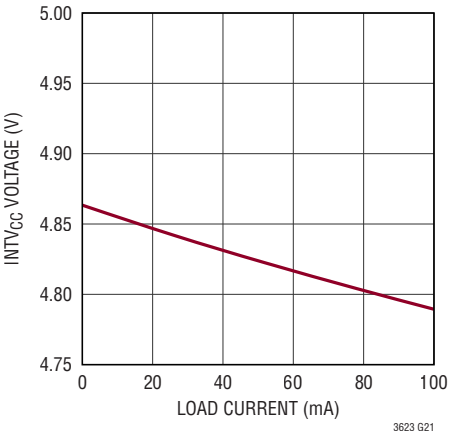
Switching Frequency/Period vs R_T



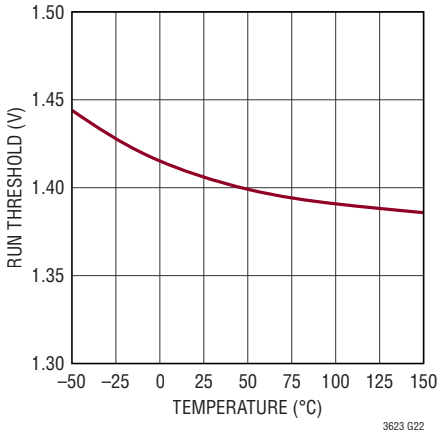
Switch Leakage Current



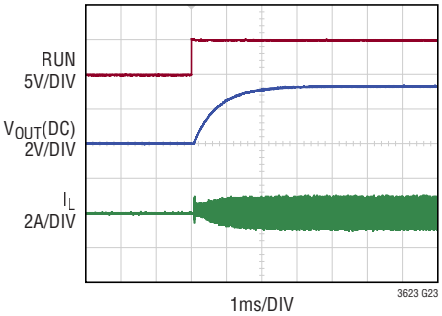
$INTV_{CC}$ Load Regulation



Rising RUN Threshold vs Temperature

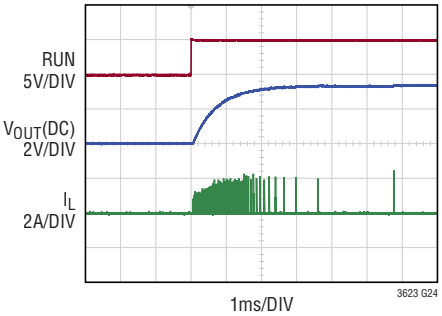


Start-up Waveform in CCM



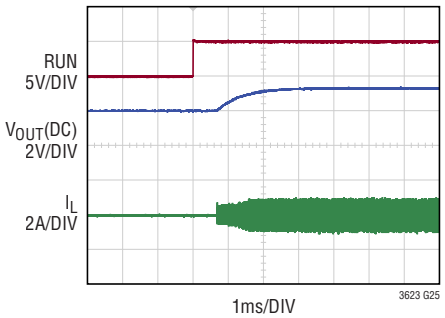
MODE = $INTV_{CC}$
NO PREBIASED V_{OUT}
V_{IN} = 12V
V_{OUT} = 3.3V

Start-up Waveform in DCM



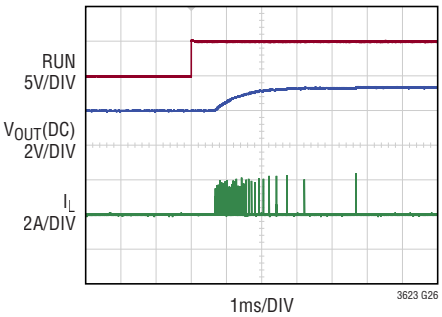
MODE = OV
NO PREBIASED V_{OUT}
V_{IN} = 12V
V_{OUT} = 3.3V

Prebiased Start-up Waveform in CCM



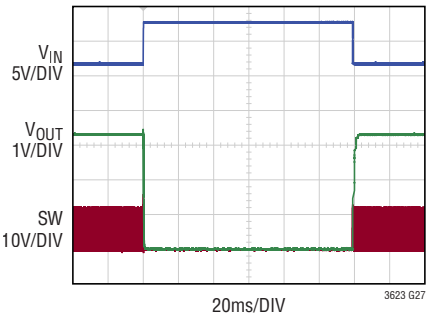
MODE = $INTV_{CC}$
V_{OUT} IS PREBIASED TO 2V
V_{IN} = 12V
V_{OUT} = 3.3V

Prebiased Start-up Waveform in DCM



MODE = OV
V_{OUT} IS PREBIASED TO 2V
V_{IN} = 12V
V_{OUT} = 3.3V

V_{IN} Overvoltage



V_{IN} = 12V TO 18V TO 12V
V_{OUT} = 3.3V
I_{OUT} = 1A
MODE = CCM

PIN FUNCTIONS

ISET (Pin 1): Accurate 50µA Current Source. Positive input to the error amplifier. Connect an external resistor from this pin to signal GND to program the V_{OUT} voltage. Connecting an external capacitor from ISET to ground will soft start the output voltage and reduce current inrush at the input cap when turning on. V_{OUT} can also be programmed by driving ISET directly with an accurate external voltage supply from 0 to 9V, in which case the external supply would be sinking this 50µA. Do not drive ISET above V_{IN} or below GND.

PGOOD (Pin 2): Output Power Good with Open-Drain Logic. PGOOD is pulled to ground when the PGFB pin is more than 0.63V or less than 0.54V. If PGFB is tied to $INTV_{CC}$, the open drain logic on PGOOD is disabled. PGOOD voltage is referred to GSNS.

RUN (Pin 3): Run Control Input. Enables chip operation by tying RUN above 1.45V. Tying RUN below 1V shuts down switching regulator. Tying RUN below 0.4V shuts off the entire chip. RUN voltage is referred to GSNS.

GSNS (Pin 4): System Ground SENSE. Ground reference for the RUN, PGOOD and MODE/SYNC pins. For positive V_{OUT} applications, connect GSNS to PGND. For negative V_{OUT} applications, connect GSNS to ground return of the system board.

PV_{IN} (Pins 5, 16): Power V_{IN}. Input voltage connected to the drain of the top power NMOS. Must be decoupled to PGND with capacitor close to PV_{IN} pin. PV_{IN} operates down to 1.5V as long as SV_{IN} > 4V.

SW (Pins 6, 15): Switch Node Connection to External Inductor. Voltage swing of SW is from a diode voltage drop below ground to PV_{IN}.

MODE/SYNC (Pin 8): Operation Mode Select. Tie this pin to $INTV_{CC}$ to force continuous synchronous operation at all output loads. Tying it to GSNS enables discontinuous mode operation at light loads. Applying an external clock signal to this pin will synchronize switching frequency to the external clock. MODE/SYNC voltage is referred to GSNS. During external clock synchronization, R_T value should be set up such that the free running frequency is within ±30% of the external clock frequency.

PGND (Pins 9, 10, 11, 12, Exposed Pad Pin 25): Power Ground. Return path of Internal Power MOSFETs. Connect these pins to the negative terminals of the input and output capacitors. The exposed pad must be soldered to the PCB ground for electrical contact and rated thermal performance.

V_{OUT} (Pin 13): Output Voltage Pin. Negative input of the error amplifier which is driven to be the same voltage as ISET.

SV_{IN} (Pin 17): Signal V_{IN}. Input voltage to power internal bias circuitry. SV_{IN} must be above 4V.

BOOST (Pin 18): Boosted Floating Driver Supply for Internal Top Power MOSFET. The (+) terminal of the bootstrap capacitor connects here. This pin swings from a diode voltage drop below $INTV_{CC}$ up to PV_{IN} + $INTV_{CC}$.

$INTV_{CC}$ (Pin 19): Internal 5V Regulator Output. The internal power drivers and control circuits are powered from this voltage. Decouple this pin to PGND with a minimum of 1µF low ESR ceramic capacitor.

PGFB (Pin 20): Power Good Feedback. Place a resistor divider on V_{OUT} to detect power good level. If PGFB is more than 0.63V or less than 0.54V, PGOOD will be pulled down. Tie PGFB to $INTV_{CC}$ to disable PGOOD function. Tying PGFB to a voltage between 0.67V and 4V will force continuous synchronous operation regardless of the MODE/SYNC state.

IMON (Pin 21): Current Monitor Pin. There will be a current equal to 21µA • I_{OUT} coming out of the IMON pin. Place a resistor in parallel with a filtering capacitor (10nF) from IMON to GND to report I_{OUT}. When the voltage on IMON is above 2.35V, I_{OUT} will be limited. IMON can also be used to program V_{OUT} to compensate for output voltage drop at the load due to wire resistance by injecting the IMON current into a portion of the ISET resistor.

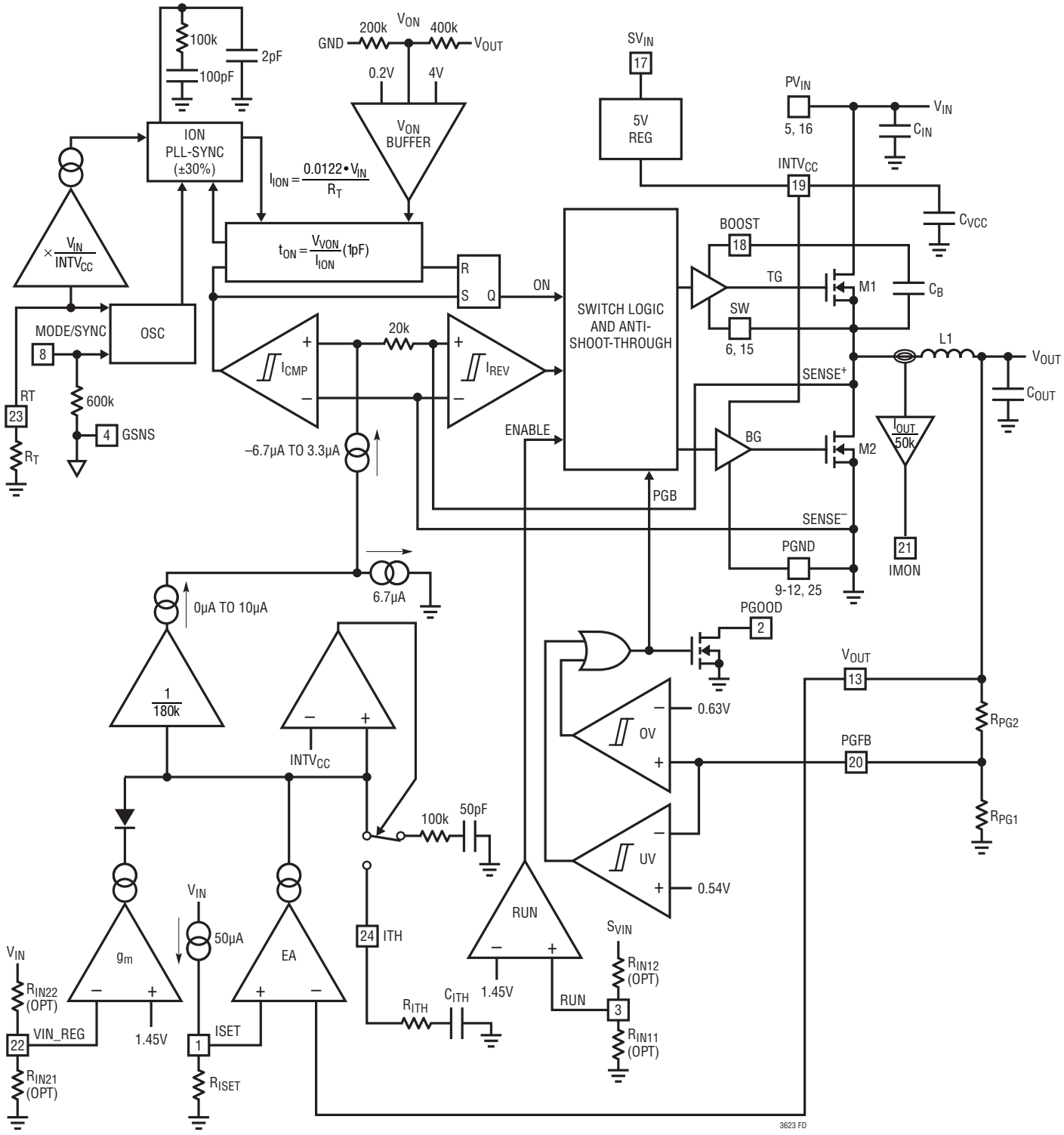
VIN_REG (Pin 22): Control Pin for V_{IN} regulation. Tie this pin to $INTV_{CC}$ for buck converter operation where V_{OUT} is regulated to ISET. Tie this pin to a resistor divider from V_{IN} to GND to enable input voltage regulation. When VIN_REG drops below 1.45V, the system will reduce the inductor current to keep V_{IN} from dropping.

PIN FUNCTIONS

RT (Pin 23): Switching Frequency Programming Pin. Connect an external resistor (between 100k to 10k) from RT to GND to program the frequency from 400kHz to 4MHz. Tying the RT pin to $INTV_{CC}$ programs 1MHz operation. Floating the RT pin shuts off the power switches.

ITH (Pin 24): Error Amplifier Output and Switching Regulator Compensation Point. The internal current comparator's trip threshold is linearly proportional to this voltage, whose normal range is from 0.55V to 1.85V. For external compensation, tie a resistor (R_{ITH}) in series with a capacitor (C_{ITH}) to signal GND. A separate 10pF high frequency filtering cap can also be placed from ITH to signal GND. Tying ITH to $INTV_{CC}$ enables the default internal compensation and removes the need for external compensation components.

FUNCTIONAL DIAGRAM



OPERATION

Main Control Loop

The LTC3623 is a current mode monolithic step down regulator. The accurate 50µA current source on the ISET pin allows the user to use just one external resistor to program the output voltage in a unity gain buffer fashion. In normal operation, the internal top power MOSFET is turned on for a fixed interval determined by a fixed one-shot timer OST. When the top power MOSFET turns off, the bottom power MOSFET turns on until the current comparator I_{CMP} trips, restarting the one shot timer and initiating the next cycle. Inductor current is determined by sensing the voltage drop across the SW and PGND nodes of the bottom power MOSFET. The voltage on the ITH pin sets the comparator threshold corresponding to inductor valley current. The error amplifier EA adjusts this I_{TH} voltage by comparing the V_{OUT} voltage with the voltage on ISET. If the load current increases, it causes a drop in the V_{OUT} voltage relative to V_{ISET}. The I_{TH} voltage then rises until the average inductor current matches that of the load current.

At low load current, the inductor current can drop to zero and become negative. This is detected by current reversal comparator I_{REV}, which then shuts off the bottom power MOSFET, resulting in discontinuous operation. Both power MOSFETs will remain off with the output capacitor supplying the load current until the I_{TH} voltage rises above the zero current level to initiate another cycle. Discontinuous mode operation is disabled by tying the MODE pin to $INTV_{CC}$, which forces continuous synchronous operation regardless of output load.

The operating frequency is determined by the value of the R_T resistor, which programs the current for the internal oscillator as well as the current for the internal one-shot timer. An internal phase-lock loop servos the switching regulator on-time to track the internal oscillator to force constant switching frequency. If an external synchronization clock is present on the MODE/SYNC pin, the regulator on-time and switching frequency would then track the external clock.

Overvoltage and under-voltage comparators OV and UV pull the PGOOD output low if the output power-good feedback voltage V_{PGFB} exits a ±7.5% window around the regulation point. Continuous operation is forced during an OV condition. To defeat the PGOOD function, simply tie PGFB to $INTV_{CC}$.

Pulling the RUN pin to ground forces the LTC3623 into its shutdown state, turning off both power MOSFETs as well as all of its internal control circuitry. Bringing the RUN pin above 0.7V turns on the internal reference only, while still keeping the power MOSFETs off. Further increasing the RUN voltage above 1.45V turns on the entire chip.

$INTV_{CC}$ Regulator

An internal low drop out (LDO) regulator produces the 5V supply that powers the drivers and the internal bias circuitry. The $INTV_{CC}$ can supply up to 50mA RMS and must be bypassed to ground with a minimum of 1µF ceramic capacitor. Good bypassing is necessary to supply the high transient currents required by the power MOSFET gate drivers. Applications with high input voltage and high switching frequency will increase die temperature because of the higher power dissipation across the LDO. Connecting a load to the $INTV_{CC}$ pin is not recommended since it will further push the LDO into its RMS current rating while increasing power dissipation and die temperature.

V_{IN} Overvoltage Protection

In order to protect the internal power MOSFET devices against transient voltage spikes, the LTC3623 constantly monitors the V_{IN} pin for an overvoltage condition. When V_{IN} rises above 16.8V, the regulator suspends operation by shutting off both power MOSFETs and discharges the ISET pin voltage to ground. Once V_{IN} drops below 15.4V, the regulator immediately resumes normal switching operation by first charging up the ISET pin to its programmed voltage.

Programming Switching Frequency

Connecting a resistor from the RT pin to GND programs the switching frequency from 400kHz to 4MHz according to the following formula:

$$\text{Frequency(Hz)} = \frac{3.32 \bullet 10^{10}}{R_T}$$

For ease of use, the RT pin can be connected directly to the $INTV_{CC}$ pin for 1MHz operation. The internal on-time phase lock loop has a synchronization range of ±30% around its programmed frequency. Therefore, during external clock synchronization, the proper R_T value should

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be selected such that the external clock frequency is within this ±30% range of the RT programmed frequency.

MODE/SYNC Operation

The MODE/SYNC pin is a multipurpose pin allowing both mode selection and operating frequency synchronization. Connecting it to ground enables Discontinuous Mode operation for superior efficiency at low load currents at the expense of slightly higher output voltage ripple. When the MODE/SYNC pin is tied to $INTV_{CC}$, forced continuous mode operation is selected, creating the lowest fixed output ripple at the expense of lower light load efficiency. The LTC3623 will detect the presence of an external clock signal on the MODE/SYNC pin and synchronize the switching frequency to that of the incoming clock. The presence of an external clock will place the part into forced continuous mode operation.

Current Monitor and Programmable Output Current Limit

The LTC3623 provides a 21µA scaled replica of the average output current at the IMON pin. Placing an external resistor at the IMON pin will generate a corresponding IMON voltage reflecting that of the output current. An internal current limit amplifier with a threshold of 2.35V is placed on the IMON pin, allowing the user to use an appropriately valued resistor to program the output current limit:

$$R_{LIM} = \frac{2.35V}{21\mu A \bullet I_{LIM}}$$

where I_{LIM} is the programmable output current limit.

For instance, placing a 50k resistor between IMON and ground would program an approximate 2.2A output current limit.

When the programmable current limit feature is used, a compensation capacitor (10nF typical) should be placed in parallel with the chosen resistor. To disable output current monitor or remove output current programmability, connect IMON to ground.

Output Cable Drop Compensation

For applications where the actual load is far away from the output of the LTC3623 converter and the resistance of the connecting cable is affecting the output regulation voltage at the load, the user can compensate for such cable drop voltage by placing an additional resistor between IMON and ISET. This resistor's value should be (1/21µ) times that of the measured cable resistance.

$$R_{ISET2} = 2 \bullet R_{CABLE} / 21\mu A$$

$$V_{OUT} = I_{SET} \bullet (R_{ISET1} + R_{ISET2})$$

$$V_{OUT,COMP} = I_{SET} \bullet R_{ISET1} + (I_{SET} + I_{IMON}) \bullet R_{ISET2}$$

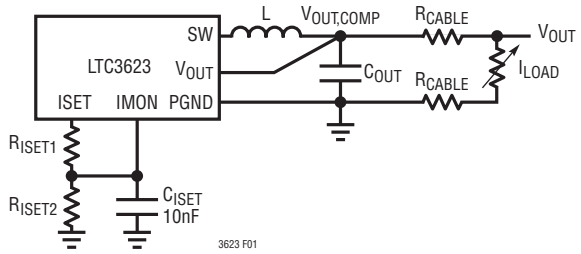

Figure 1. Output Cable Drop Compensation

If there's an equivalent cable resistance for the ground return between the load and the converter, then the resistor's value should be doubled. As a result, the ISET programming reference voltage would increase as the load current increase, compensating for the V_{OUT} cable drop at the load.

Output Voltage Tracking and Soft Start

The LTC3623 allows the user to program its output voltage ramp rate by means of the ISET pin. Since V_{OUT} servos its voltage to that of the ISET pin, placing an external capacitor C_{ISET} on the ISET pin will program the ramp-up rate of the ISET pin and thus the V_{OUT} voltage:

$$V_{OUT}(t) = I_{SET} \bullet R_{ISET} \left[1 - e^{\frac{-t}{(R_{ISET} \bullet C_{ISET})}} \right]$$

From 0 to 90% of V_{OUT}

$$t_{SS} = -R_{ISET} \bullet C_{ISET} \bullet \ln(1-0.9)$$

$$t_{SS} = 2.3 \bullet R_{ISET} \bullet C_{ISET}$$

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The soft-start time tss (from 0% to 90% V_{OUT}) is 2.3 times of time constant (R_{ISET} • C_{ISET}). The ISET pin can also be driven by an external Voltage supply capable of sinking the provided 50µA.

When starting up into a pre-biased V_{OUT}, the LTC3623 will stay in discontinuous mode and keep the power switches off until the voltage on ISET has ramped up to be equal to V_{OUT}, at which point the switcher will begin switching and V_{OUT} will ramp up with ISET.

Input Voltage Regulation Loop for Backup Power Supply

The input voltage regulation loop circuit is used to hold up and regulate the input voltage for backup power supply applications when the input supply is removed or is very resistive. An external resistor divider from V_{IN} can be used to sense the V_{IN} voltage and feeds into the VIN_REG pin of the LTC3623. When the voltage on the VIN_REG pin is less than 1.45V, the part will dynamically reduce the inductor current to prevent the input voltage from drooping below the 1.45V threshold. If the V_{IN} voltage and the VIN_REG pin voltage continues to fall, charge will be transferred from the V_{OUT} capacitor to the V_{IN} capacitor in order to hold up the V_{IN} voltage. Duration of the holdup will depend on the amount of charge stored in the output capacitor. Activation and termination of the input voltage regulation loop can also be set using a separate resistor divider from V_{IN} to drive the RUN pin, which has a rising threshold of 1.45V to enable the chip, and a falling threshold of 1.1V to disable the chip. If the V_{IN} voltage regulation feature is not used, connect the VIN_REG pin to $INTV_{CC}$.

$$VIN_{holdup} = \left(\frac{R_{DIR1}+R_{DIR2}}{R_{DIR1}}\right) \bullet 1.45V$$

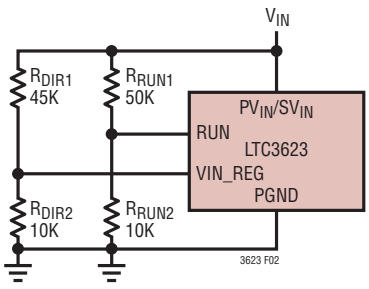

Figure 2. Input Voltage Regulation

Output Power Good

When the LTC3623's output voltage is within the ±7.5% window of the regulation point, which is reflected back as a V_{PGFB} voltage in the range of 0.54V to 0.63V, the output voltage is in regulation and the PGOOD pin is pulled high with an external resistor. Otherwise, an internal open-drain pull down device (100Ω) will pull the PGOOD pin low. To prevent unwanted PGOOD glitches during transients or dynamic V_{OUT} changes, the LTC3623's PGOOD falling edge includes a blanking delay of approximately 20µsec.

Internal/External ITH Compensation

For ease of use, the user can simplify the loop compensation by tying the ITH pin to $INTV_{CC}$ to enable internal compensation. This connects an internal 100k resistor in series with a 50pF cap to the output of the error amplifier (internal I_{TH} compensation point). This is a trade-off for simplicity instead of OPTI-LOOP® optimization, where I_{TH} components are external and are selected to optimize the loop transient response with minimum output capacitance.

Minimum Off-Time Considerations

The minimum off-time $t_{OFF(min)}$ is the smallest amount of time that the LTC3623 is capable of turning on the bottom power MOSFET, tripping the current comparator and turning the power MOSFET back off. This time is generally about 100ns. The minimum off-time limit imposes a maximum duty cycle of $t_{on}/(t_{ON}+t_{OFF(min)})$. If the maximum duty cycle is reached, due to the input voltage dropping, for example, then the output will drop out of regulation. The minimum input voltage to avoid dropout is:

$$V_{IN(MIN)} = V_{OUT} \bullet \left(\frac{\left(t_{ON}+t_{OFF(MIN)}\right)}{t_{ON}}\right)$$

Conversely, the minimum on-time is the smallest duration of time in which the top power MOSFET can be in its "on" state. This time is typically 30ns. In continuous mode operation, the minimum on-time limit imposes a minimum duty cycle of:

$$DC_{MIN} = f \bullet t_{ON(MIN)}$$

Where $t_{ON(MIN)}$ is the minimum on-time. As the equation shows, reducing the operating frequency will alleviate the minimum duty cycle constraint.

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In the rare cases where the minimum duty cycle is surpassed, the output voltage will still remain in regulation, but the switching frequency will decrease from its programmed value. This is an acceptable result in many applications, so this constraint may not be of critical importance in most cases. High switching frequencies may be used in the design without any fear of severe consequences. As the sections on inductor and capacitor selection show, high switching frequencies allow the use of smaller board components, thus reducing the size of the application circuit.

C_{IN} and C_{OUT} Selection

The input capacitance, C_{IN}, is needed to filter the trapezoidal wave current at the drain of the top power MOSFET. To prevent large voltage transients from occurring, a low ESR input capacitor sized for the maximum RMS current should be used. The maximum RMS current is given by:

$$I_{RMS} = I_{OUT(MAX)} \left(\frac{V_{OUT}}{V_{IN}} \right) \left(\frac{V_{IN}}{V_{OUT}} - 1 \right)^{1/2}$$

This formula has a maximum at $V_{IN} = 2V_{OUT}$, where $I_{RMS} = I_{OUT}/2$. This simple worst case condition is commonly used for design because even significant deviations do not offer much relief. Note that ripple current ratings from capacitor manufacturers are often based on only 2000 hours of life which makes it advisable to further de-rate the capacitor, or choose a capacitor rated at a higher temperature than required.

Several capacitors may also be paralleled to meet size or height requirements in the design. For low input voltage applications, sufficient bulk input capacitance is needed to minimize transient effects during output load changes.

The selection of C_{OUT} is determined by the effective series resistance (ESR) that is required to minimize voltage ripple and load step transients as well as the amount of bulk capacitance that is necessary to ensure that the control loop is stable. Loop stability can be checked by viewing the load transient response. The output ripple, ΔV_{OUT}, is determined by:

$$\Delta V_{OUT} < \Delta I_L \left(\frac{1}{8 \bullet f_{SW} \bullet C_{OUT}} + R_{ESR} \right)$$

The output ripple is highest at maximum input voltage since ΔI_L increases with input voltage. Multiple capacitors placed in parallel may be needed to meet the ESR and RMS current handling requirements. Dry tantalum, special polymer, aluminum electrolytic, and ceramic capacitors are all available in surface mount packages. Special polymer capacitors are very low ESR but have lower capacitance density than other types. Tantalum capacitors have the highest capacitance density but it is important to only use types that have been surge tested for use in switching power supplies. Aluminum electrolytic capacitors have significantly higher ESR, but can be used in cost-sensitive applications provided that consideration is given to ripple current ratings and long term reliability. Ceramic capacitors have excellent low ESR characteristics and small footprints. Their relatively low value of bulk capacitance may require multiples in parallel.

Using Ceramic Input and Output Capacitors

Higher values, lower cost ceramic capacitors are now becoming available in smaller case sizes. Their high ripple current, high voltage rating and low ESR make them ideal for switching regulator applications. However, care must be taken when these capacitors are used at the input and output. When a ceramic capacitor is used at the input and the power is supplied by a wall adapter through long wires, a load step at the output can induce ringing at the V_{IN} input. At best, this ringing can couple to the output and be mistaken as loop instability. At worst, a sudden inrush of current through the long wires can potentially cause a voltage spike at V_{IN} large enough to damage the part.

When choosing the input and output ceramic capacitors, choose the X5R and X7R dielectric formulations. These dielectrics have the best temperature and voltage characteristics of all the ceramics for a given value and size.

Since the ESR of a ceramic capacitor is so low, the input and output capacitor must instead fulfill a charge storage requirement. During a load step, the output capacitor must instantaneously supply the current to support the load until the feedback loop raises the switch current enough to support the load. The time required for the feedback loop to respond is dependent on the compensation and the output capacitor size. Typically, 3 to 4 cycles

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are required to respond to a load step, but only in the first cycle does the output drop linearly. The output droop, V_{DROOP}, is usually about 2 to 3 times the linear drop of the first cycle. Thus, a good place to start with the output capacitor value is approximately:

$$C_{OUT} \sim 2.5 \bullet \left(\frac{\Delta I_{OUT}}{f_{SW} \bullet V_{DROOP}} \right)$$

More capacitance may be required depending on the duty cycle and load step requirements.

In most applications, the input capacitor is merely required to supply high frequency bypassing, since the impedance to the supply is very low. A 22µF ceramic capacitor is usually enough for these conditions. Place this input capacitor as close to V_{IN} pin as possible.

Inductor Selection

Given the desired input and output voltages, the inductor value and operating frequency determine the ripple current:

$$\Delta I_L = \left(\frac{V_{OUT}}{f_{SW} \bullet L} \right) \left(1 - \frac{V_{OUT}}{V_{IN}} \right)$$

Lower ripple current reduces core losses in the inductor, ESR losses in the output capacitors, and output voltage ripple. Highest efficiency operation is obtained at low frequency with small ripple current. However, achieving this requires a large inductor. There is a trade-off between component size, efficiency, and operating frequency.

A reasonable starting point is to choose a ripple current that is about 40% of $I_{OUT(MAX)}$. Note that the largest ripple current occurs at the highest V_{IN}. To guarantee that ripple current does not exceed a specified maximum, the inductance should be chosen according to:

$$L = \left(\frac{V_{OUT}}{f_{SW} \bullet \Delta I_{L(MAX)}} \right) \left(1 - \frac{V_{OUT}}{V_{IN(MAX)}} \right)$$

Once the value for L is known, the type of inductor must be selected. Actual core loss is independent of core size for a fixed inductor value, but is very dependent on the inductance selected. As the inductance increases, core losses decrease. Unfortunately, increased inductance requires more turns of wire and therefore copper losses will increase.

Ferrite designs have very low core losses and are preferred at high switching frequencies, so design goals can concentrate on copper loss and preventing saturation. Ferrite core material saturates “hard”, which means that inductance collapses abruptly when the peak design current is exceeded. This results in an abrupt increase in inductor ripple current and consequent output voltage ripple. Do not allow the core to saturate!

Different core materials and shapes will change the size/current and price/current relationship of an inductor. Toroid or shielded pot cores in ferrite or permalloy materials are small and don’t radiate much energy, but generally cost more than powdered iron core inductors with similar characteristics. The choice of which style inductor to use mainly depends on the price versus size requirements and any radiated field/EMI requirements. New designs for surface mount inductors are available from Toko, Vishay, NEC/Tokin, Cooper, TDK, and Würth Elektronik. Refer to Table 1 for more details

Checking Transient Response

The OPTI-LOOP compensation allows the transient response to be optimized for a wide range of loads and output capacitors. The availability of the ITH pin not only allows optimization of the control loop behavior but also provides a DC-coupled and AC-filtered closed-loop response test point. The DC step, rise time and settling at this test point truly reflects the closed-loop response. Assuming a predominantly second order system, phase margin and/or damping factor can be estimated using the percentage of overshoot seen at this pin.

The I_{TH} external components shown in Figure 6 circuit will provide an adequate starting point for most applications. The series R-C filter sets the dominant pole-zero loop compensation. The values can be modified slightly (from 0.5 to 2 times their suggested values) to optimize transient response once the final PC layout is done and the particular output capacitor type and value have been determined. The output capacitors need to be selected because their

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Table 1. Inductor Selection Table

INDUCTANCE	DCR	MAX CURRENT	DIMENSIONS	HEIGHT
Vishay IHLP-2525CZ-01 Series				
0.33µH	4.1mΩ	18A	6.7mm × 7mm	3mm
0.47µH	6.5mΩ	13.5A		
0.68µH	9.4mΩ	11A		
0.82µH	11.8mΩ	10A		
1.0µH	14.2mΩ	9A		
Vishay IHLP-1616BZ-11 Series				
0.22µH	4.1mΩ	12A	4.3mm × 4.7mm	2.0mm
0.47µH	15mΩ	7A		
Toko FDV0620 Series				
0.20µH	4.5mΩ	12.4A	7mm × 7.7mm	2.0mm
0.47µH	8.3mΩ	9A		
1µH	18.3mΩ	5.7A		
NEC/Tokin MLC0730L Series				
0.47µH	4.5mΩ	16.6A	6.9mm × 7.7mm	3.0mm
0.75µH	7.5mΩ	12.2A		
1µH	9mΩ	10.6A		
Cooper HCP0703 Series				
0.22µH	2.8mΩ	23A	7mm × 7.3mm	3.0mm
0.47µH	4.2mΩ	17A		
0.68µH	5.5mΩ	15A		
0.82µH	8mΩ	13A		
1µH	10mΩ	11A		
1.5µH	14mΩ	9A		
TDK RLF7030 Series				
1µH	8.8mΩ	6.4A	6.9mm × 7.3mm	3.2mm
1.5µH	9.6mΩ	6.1A		
2.2µH	12mΩ	5.4A		
Würth Elektronik WE-HC 744312 Series				
0.25µH	2.5mΩ	18A	7mm × 7.7mm	3.8mm
0.47µH	3.4mΩ	16A		
0.72µH	7.5mΩ	12A		
1µH	9.5mΩ	11A		
1.5µH	10.5mΩ	9A		

various types and values determine the loop feedback factor gain and phase. An output current pulse of 20% to 100% of full load current having a rise time of 1µs to 10µs will produce output voltage and ITH pin waveforms that will give a sense of the overall loop stability without breaking the feedback loop.

Switching regulators take several cycles to respond to a step in load current. When a load step occurs, V_{OUT} immediately shifts by an amount equal to $\Delta I_{LOAD} \bullet ESR$, where ESR is the effective series resistance of C_{OUT}. ΔI_{LOAD} also begins to charge or discharge C_{OUT} generating a feedback error signal used by the regulator to return V_{OUT} to its steady-state value. During this recovery time, V_{OUT} can be monitored for overshoot or ringing that would indicate a stability problem.

The initial output voltage step may not be within the bandwidth of the feedback loop, so the standard second order overshoot/DC ratio cannot be used to determine phase margin. The gain of the loop increases with the R and the bandwidth of the loop increases with decreasing C. If R is increased by the same factor that C is decreased, the zero frequency will be kept the same, thereby keeping the phase the same in the most critical frequency range of the feedback loop. In addition, a feed forward capacitor C_{FF} can be added to improve the high frequency response, as shown in Figure 1. Capacitor C_{FF} provides phase lead by creating a high frequency zero with R2 which improves the phase margin.

The output voltage settling behavior is related to the stability of the closed-loop system and will demonstrate the actual overall supply performance. For a detailed explanation of optimizing the compensation components, including a review of control loop theory, refer to AN76 - OPTI-LOOP Architecture Reduces Output Capacitance and Improves Transient Response.

In some applications, a more severe transient can be caused by switching in loads with large (>10µF) input capacitors. The discharged input capacitors are effectively put in parallel with C_{OUT}, causing a rapid drop in V_{OUT}. No regulator can deliver enough current to prevent this problem, if the switch connecting the load has low resistance and is driven quickly. The solution is to limit the turn-on speed of the load

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switch driver. A Hot Swap controller is designed specifically for this purpose and usually incorporates current limit, short-circuit protection, and soft-start.

Efficiency Considerations

The percent efficiency of a switching regulator is equal to the output power divided by the input power times 100%. It is often useful to analyze individual losses to determine what is limiting the efficiency and which change would produce the most improvement. Percent efficiency can be expressed as:

$$\% \text{ Efficiency} = 100\% - (L1 + L2 + L3 + \ldots)$$

where L1, L2, etc. are the individual losses as a percentage of input power.

Although all dissipative elements in the circuit produce losses, four main sources usually account for most of the losses in LTC3623 circuits: 1) I^2R losses, 2) Transition losses, 3) switching losses, 4) other losses.

1. I^2R losses are calculated from the DC resistances of the internal switches, R_{SW}, the external inductor, R_L, and board trace resistance, Rb. In continuous mode, the average output current flows through inductor L but is "chopped" between the internal top and bottom power MOSFETs. Thus, the series resistance looking into the SW pin is a function of both top and bottom MOSFET $R_{DS(ON)}$ and the duty cycle (DC) as follows:

   $$R_{SW} = R_{DS(ON)(TOP)}(DC) + R_{DS(ON)(BOT)}(1\text{-}DC)$$

   The $R_{DS(ON)}$ for both the top and bottom MOSFETs can be obtained from the Typical Performance Characteristics curves. Thus to obtain I^2R losses:

   $$I^2R \text{ losses} = I_{OUT}^2(R_{SW} + R_L + Rb)$$

2. Transition loss arises from the brief amount of time the top power MOSFET spends in the saturated region during switch node transitions. It depends upon the input voltage, load current, internal power MOSFET gate capacitance, internal driver strength, and switching frequency.

3. The $INTV_{CC}$ current is the sum of the power MOSFET driver and control currents. The power MOSFET driver current results from switching the gate capacitance of the power MOSFETs, Each time a power MOSFET gate is switched from low to high to low again, a packet of charge dQ moves from V_{IN} to ground. The resulting dQ/dt is a current out of $INTV_{CC}$ that is typically much larger than the DC control bias current. In continuous mode, $I_{GATECHG} = f_{SW}(Q_T + Q_B)$, where Q_T and Q_B are the gate charges of the internal top and bottom power MOSFETs and f_{SW} is the switching frequency. Since $INTV_{CC}$ is a low drop out regulator output powered by V_{IN}, the $INTV_{CC}$ current also shows up as V_{IN} current, unless a separate voltage supply (>5V and <6V) is used to drive $INTV_{CC}$.

4. Other "hidden" losses such as copper trace and internal load resistances can account for additional efficiency degradations in the overall power system. It is very important to include these "system" level losses in the design of a system. Other losses including diode conduction losses during dead-time and inductor core losses generally account for less than 2% total additional loss.

Thermal Considerations

In a majority of applications, the LTC3623 does not dissipate much heat due to its high efficiency and low thermal resistance of its exposed-back DFN or MSOP package. However, in applications where the LTC3623 is running at high ambient temperature, high V_{IN}, high switching frequency, and maximum output current load, the heat dissipated may exceed the maximum junction temperature of the part. If the junction temperature reaches approximately 160°C, both power switches will be turned off until temperature is about 15°C cooler.

To avoid the LTC3623 from exceeding the maximum junction temperature, the user will need to do some thermal analysis. The goal of the thermal analysis is to determine whether the power dissipated exceeds the maximum junction temperature of the part. The temperature rise is given by:

$$T_{RISE} = P_D \bullet \theta_{JA}$$

OPERATION

As an example, consider the case when the LTC3623 is used in application where V_{IN} = 12V, I_{OUT} = 5A, f = 1MHz, V_{OUT} = 1.8V. The equivalent power MOSFET resistance R_{SW} is

$$R_{SW} = R_{DS(ON)TOP} \bullet \frac{1.8}{12} + R_{DS(ON)BOT} \bullet \frac{10.2}{12}$$

$$= 0.06 \bullet \left(\frac{1.8}{12}\right) + 0.03\left(\frac{10.2}{12}\right)$$

$$= 0.0345\Omega$$

The V_{IN} current during 1MHz force continuous operation with no load is about 6mA, which includes switching and internal biasing current loss, transition loss, inductor core loss, and other losses in the application. Therefore, the total power dissipated by the part is:

$$P_D = I_{OUT}^2 \bullet R_{SW} + V_{IN} \bullet I_{VIN(No\ Load)}$$

$$= 25A^2 \bullet 0.0345 + 12V \bullet 6mA$$

$$= 0.93W$$

The QFN 5mm × 3mm package junction-to-ambient thermal resistance, θ_{JA}, is around 36°C/W. Therefore, the junction temperature of the regulator operating in a 25°C ambient temperature is approximately:

$$T_J = 0.93 \bullet 36 + 25 = 59°C$$

Remembering that the above junction temperature is obtained from an $R_{DS(ON)}$ at 25°C, we might recalculate the junction temperature based on a higher $R_{DS(ON)}$ since it increases with temperature. Redoing the calculation assuming that R_{SW} increased 25% at 59°C yields a new junction temperature of 70°C, which is still very far away from thermal shutdown or maximum allowed junction temperature rating.

Board Layout Considerations

When laying out the printed circuit board, the following checklist should be used to ensure proper operation of the LTC3623. Check the following in your layout:

1. Do the capacitors C_{IN} connect to the power V_{IN} and power GND as close as possible? These capacitors provide the AC current to the internal power MOSFETs and their drivers.
2. Are C_{OUT} and L1 closely connected? The (–) plate of C_{OUT} returns current to PGND and the (–) plate of C_{IN}.
3. The ground terminal of ISET resistor must be connected to other quiet signal GND and together connects to the power GND at only one point. The ISET resistor should be placed and routed away from noisy components and traces, such as the SW line, and its trace should be minimized.
4. Keep sensitive components away from the SW pin. The ISET resistor, R_T resistor, the compensation capacitor C_C and C_{ITH} and all the resistors R1, R3, and R_C, and the $INTV_{CC}$ bypass capacitor, should be routed away from the SW trace and the inductor L1.
5. A ground plane is preferred, but if not available, keep the signal and power grounds segregated with small signal components returning to the signal GND at one point which is then connected to the power GND at the exposed back with minimal resistance.

Flood all unused areas on all layers with copper, which reduces the temperature rise of power components. These copper areas should be connected to one of the input supplies: V_{IN} or GND.

Design Example

As a design example, consider using the LTC3623 in an application with the following specifications:

V_{IN} = 10.8V to 13.2V, V_{OUT} = 1.8V, $I_{OUT(MAX)}$ = 5A, $I_{OUT(MIN)}$ = 500mA, f_{SW} = 2MHz

Because efficiency is important at both high and low load currents, discontinuous mode operation will be utilized. First select from the characteristic curves the correct R_T resistor value for 2MHz switching frequency. Based on that R_T should be 16.5k. Then calculate the inductor value for about 40% ripple current at maximum V_{IN}:

$$L = \left(\frac{1.8V}{2MHz \bullet 2A}\right)\left(1 - \frac{1.8V}{13.2V}\right) = 0.39\mu H$$

The nearest standard value inductor would be 0.33µH.

OPERATION

C_{OUT} will be selected based on the ESR that is required to satisfy the output voltage ripple requirement and the bulk capacitance needed for loop stability. For this design, one 47µF ceramic capacitor will be used.

C_{IN} should be sized for a maximum current rating of:

$$I_{RMS} = 5A\left(\frac{1.8V}{13.2V}\right)\left(\frac{13.2V}{1.8V}-1\right)^{1/2} = 1.7A$$

Decoupling the V_{IN} pin with one 22µF ceramic capacitor is adequate for most applications.

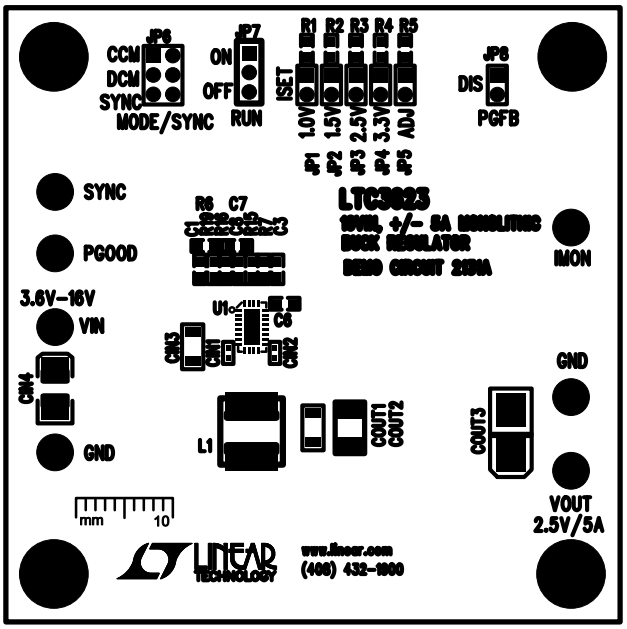


Figure 3. PCB Layout – Top Side

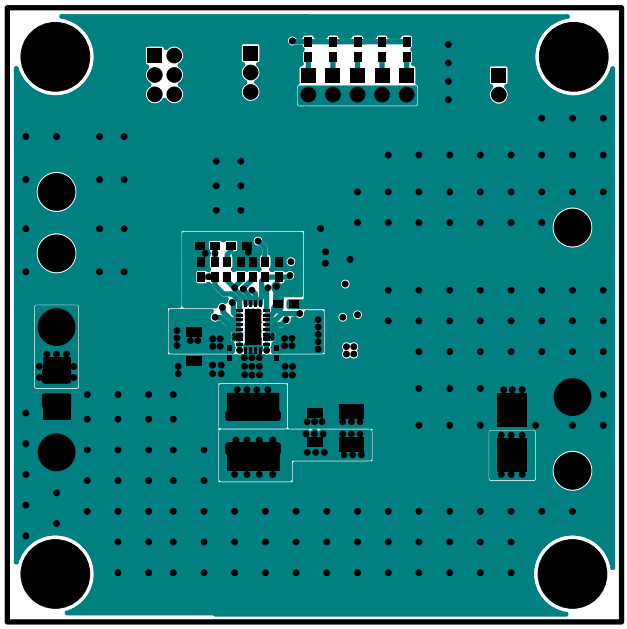


Figure 4. PCB Layout

TYPICAL APPLICATIONS

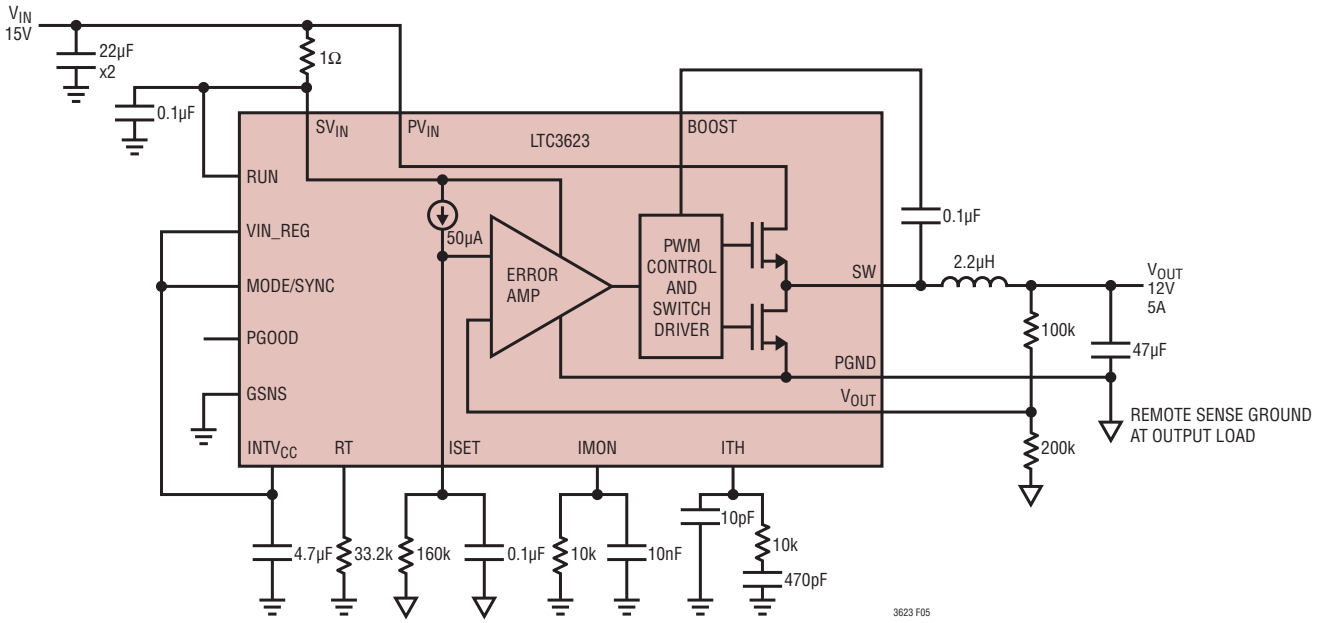


Figure 5. 15V to 12V 1MHz Buck Converter with Output Resistor Dividers

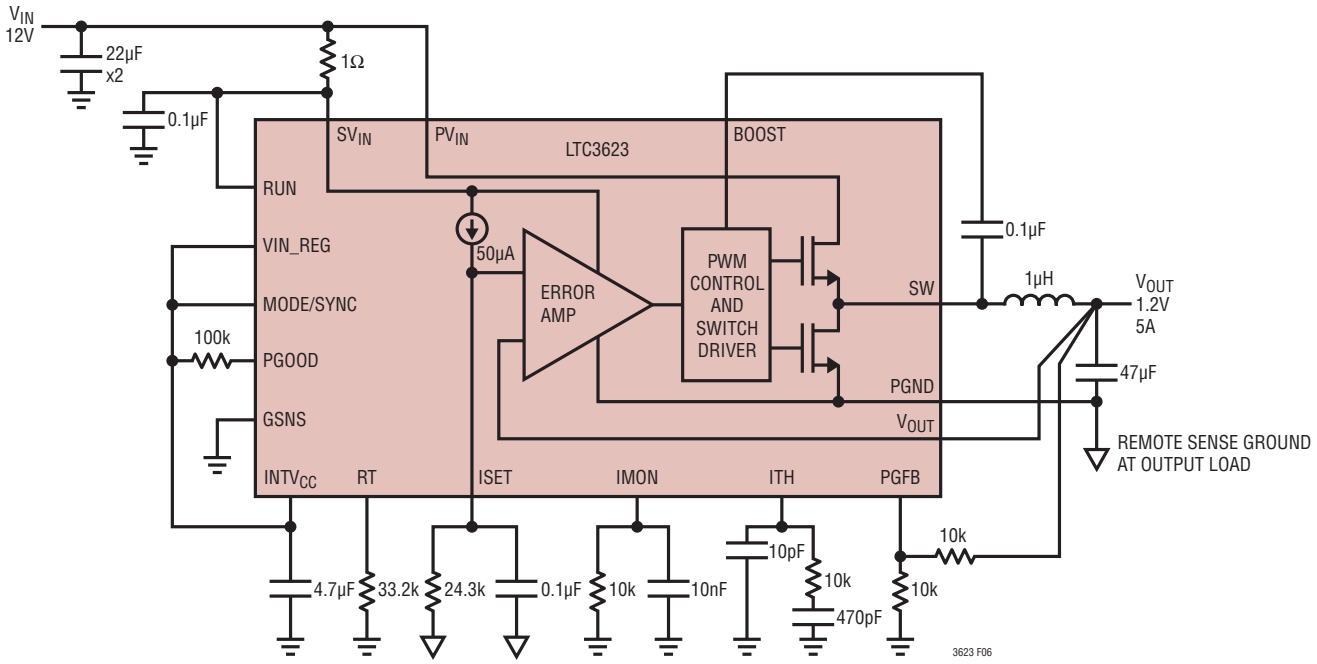


Figure 6. 12V to 1.2V 1MHz Buck Regulator with Differential Remote Sense

TYPICAL APPLICATIONS

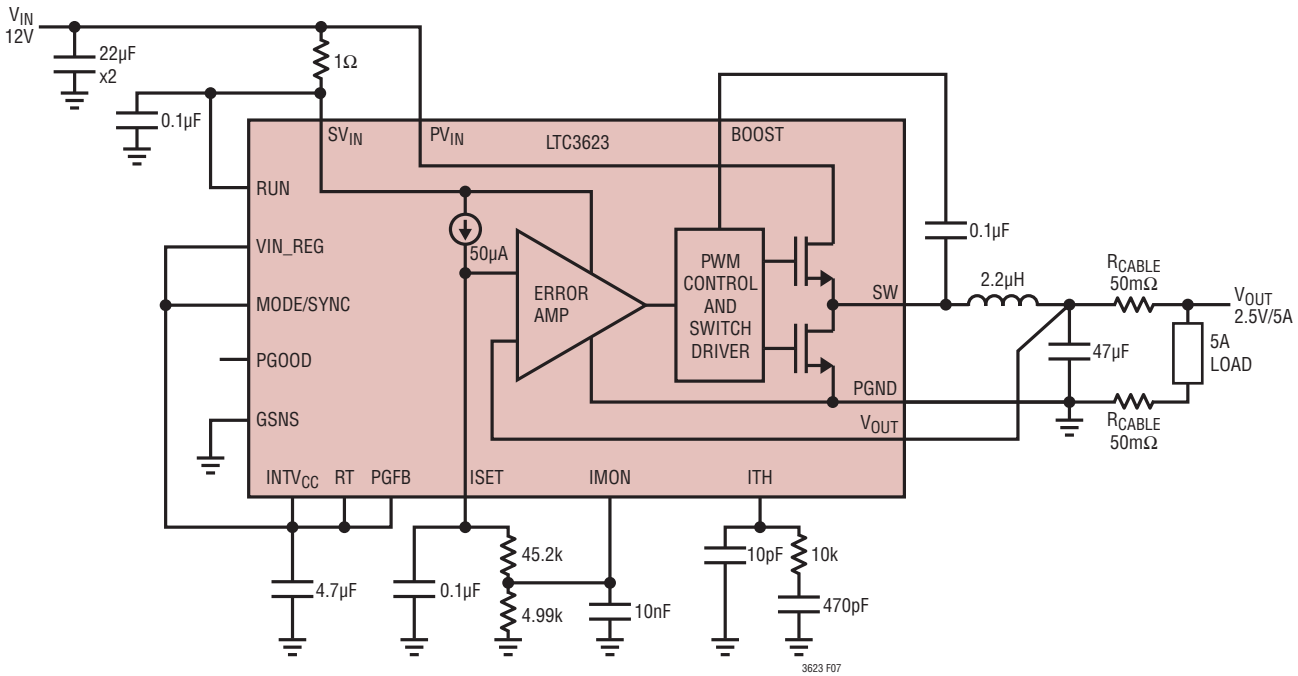
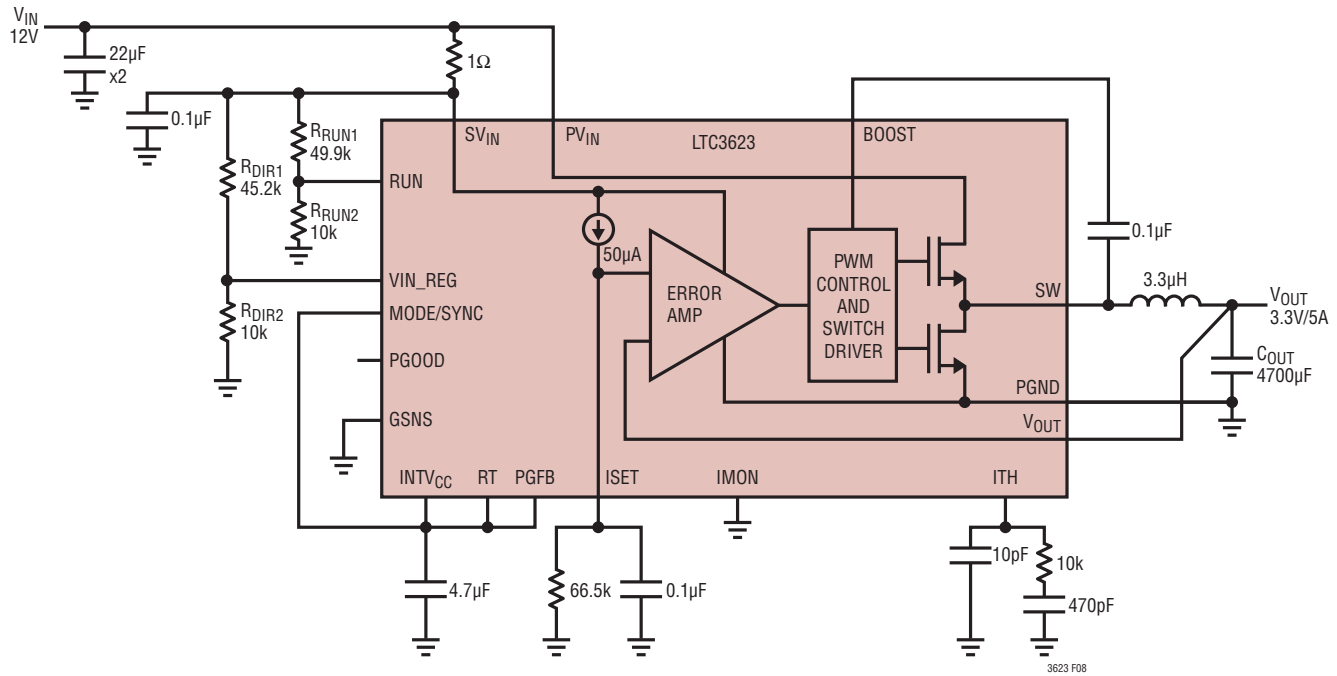


Figure 7. 12V to 2.5V 1MHz Buck Regulator with Cable Drop Compensation

TYPICAL APPLICATIONS



Input Voltage Hold Up

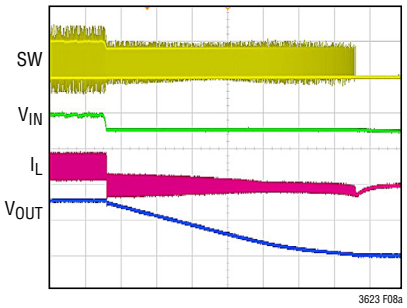
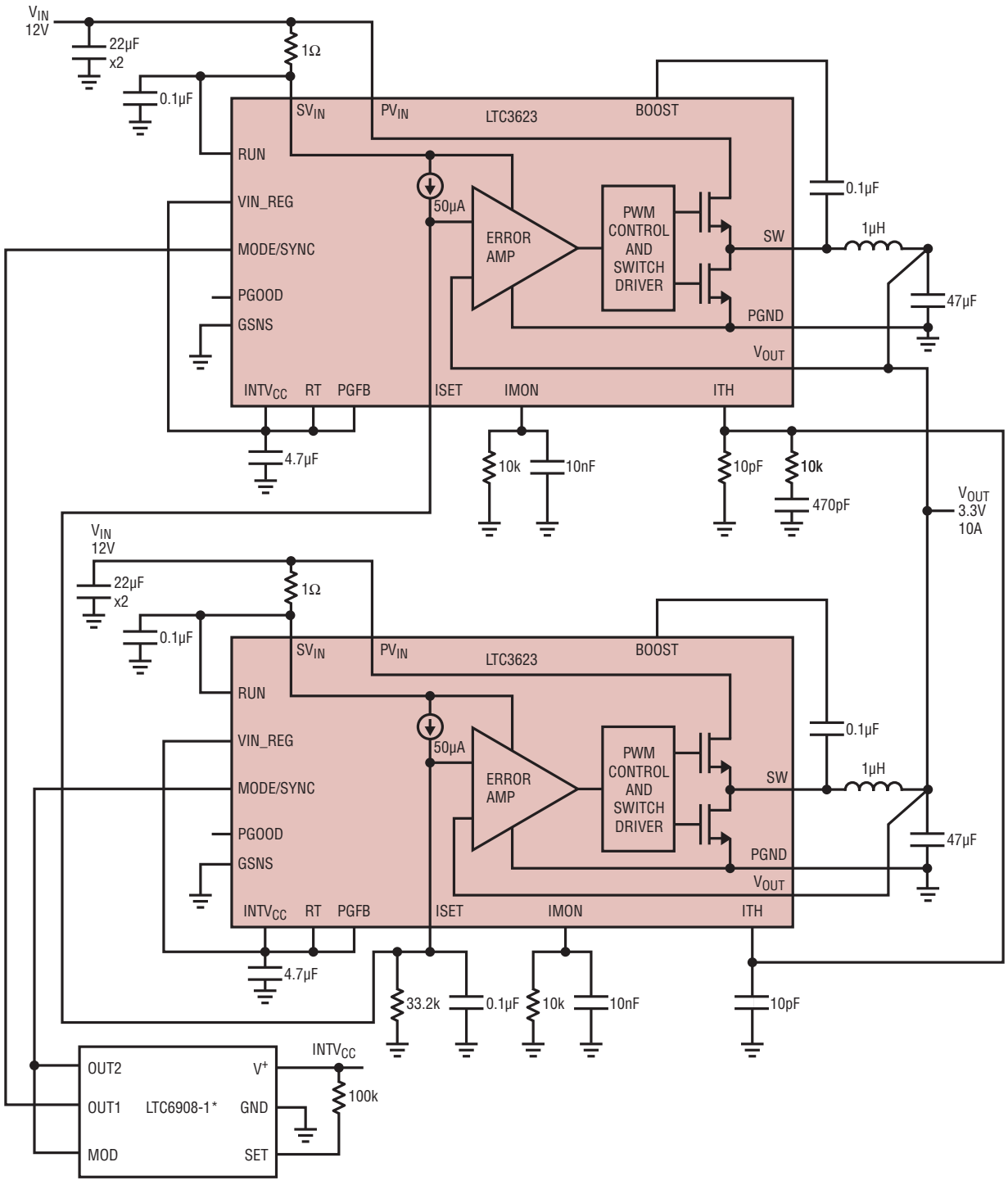


Figure 8. 12V to 3.3V 1MHz Buck Regulator with Input Supply Regulation Loop

TYPICAL APPLICATIONS



*EXTERNAL CLOCK FOR FREQUENCY SYNCHRONIZATION IS RECOMMENDED

3623 F09

Figure 9. 12V to 10A 2-Phase Single Output Regulator

TYPICAL APPLICATIONS

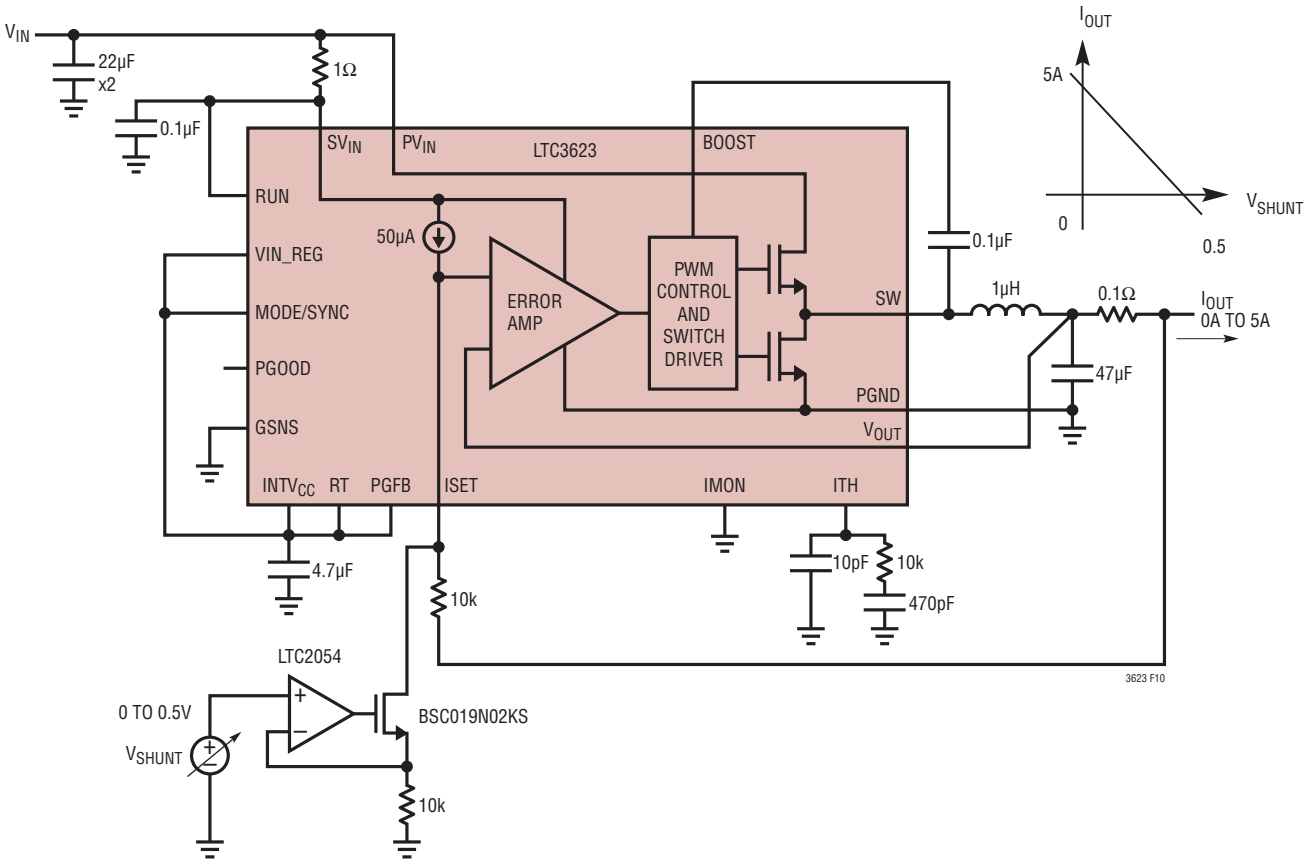


Figure 10. Programmable 5A Current Source

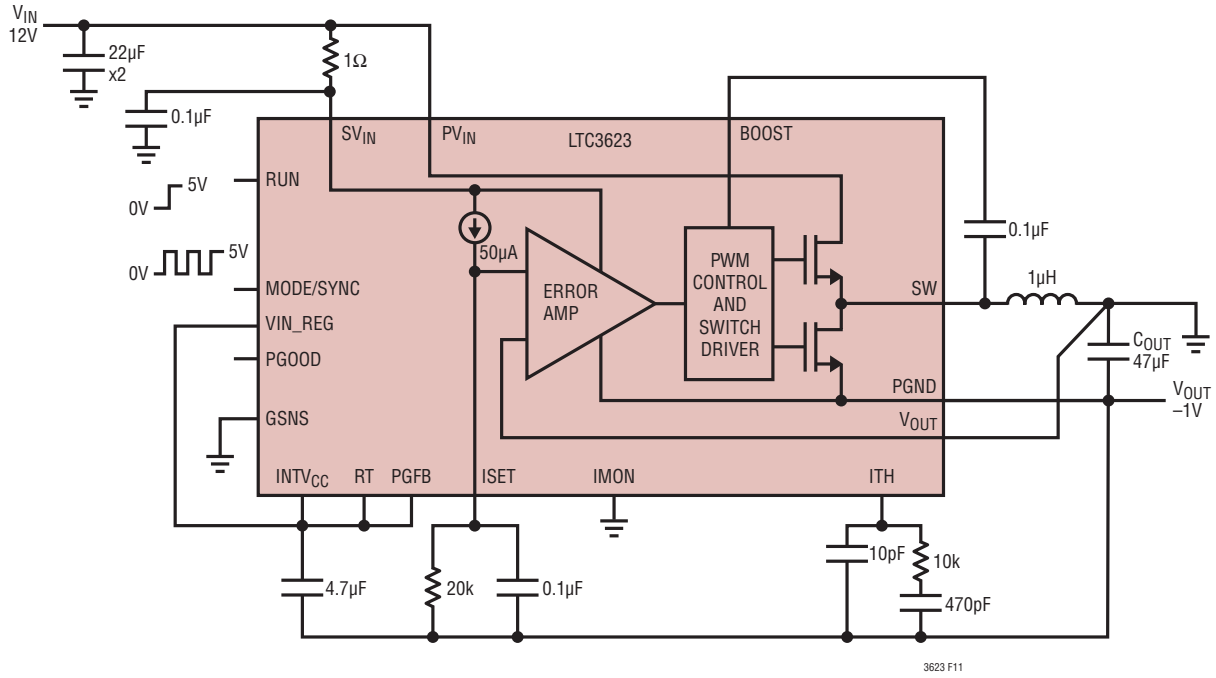


Figure 11. 12V to –1V, 1MHz Buck Regulator

TYPICAL APPLICATIONS

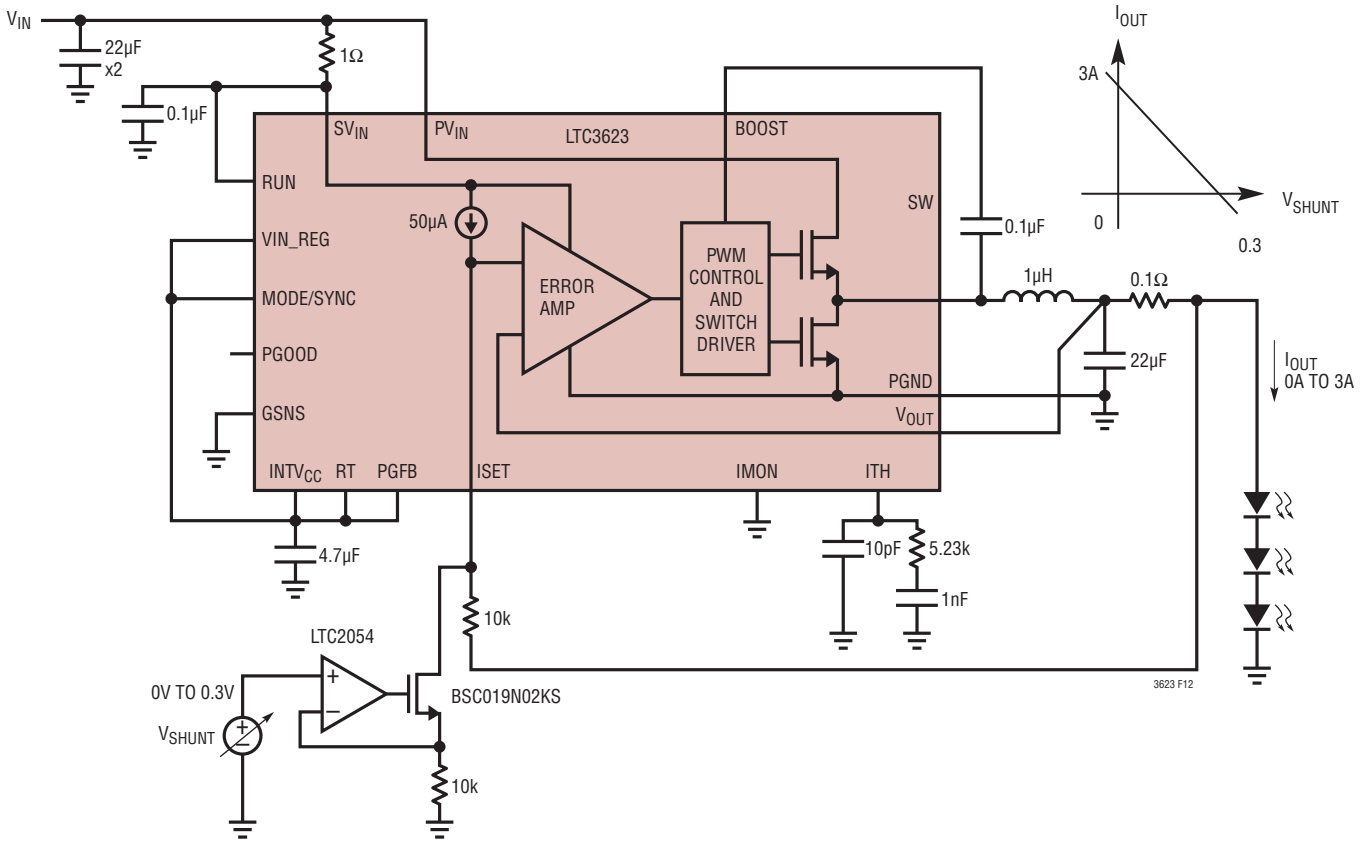


Figure 12. LED Driver with Programmable Control

TYPICAL APPLICATIONS

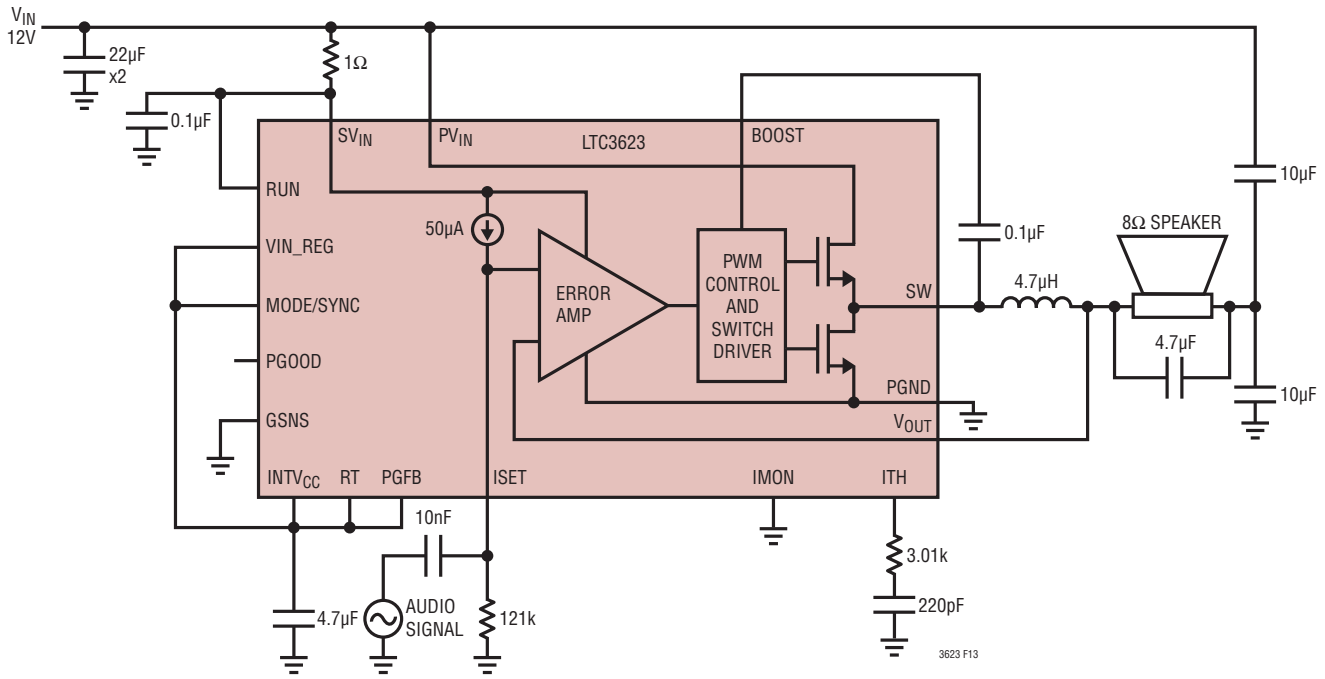


Figure 13. High Efficiency 12V Audio Driver

TYPICAL APPLICATIONS

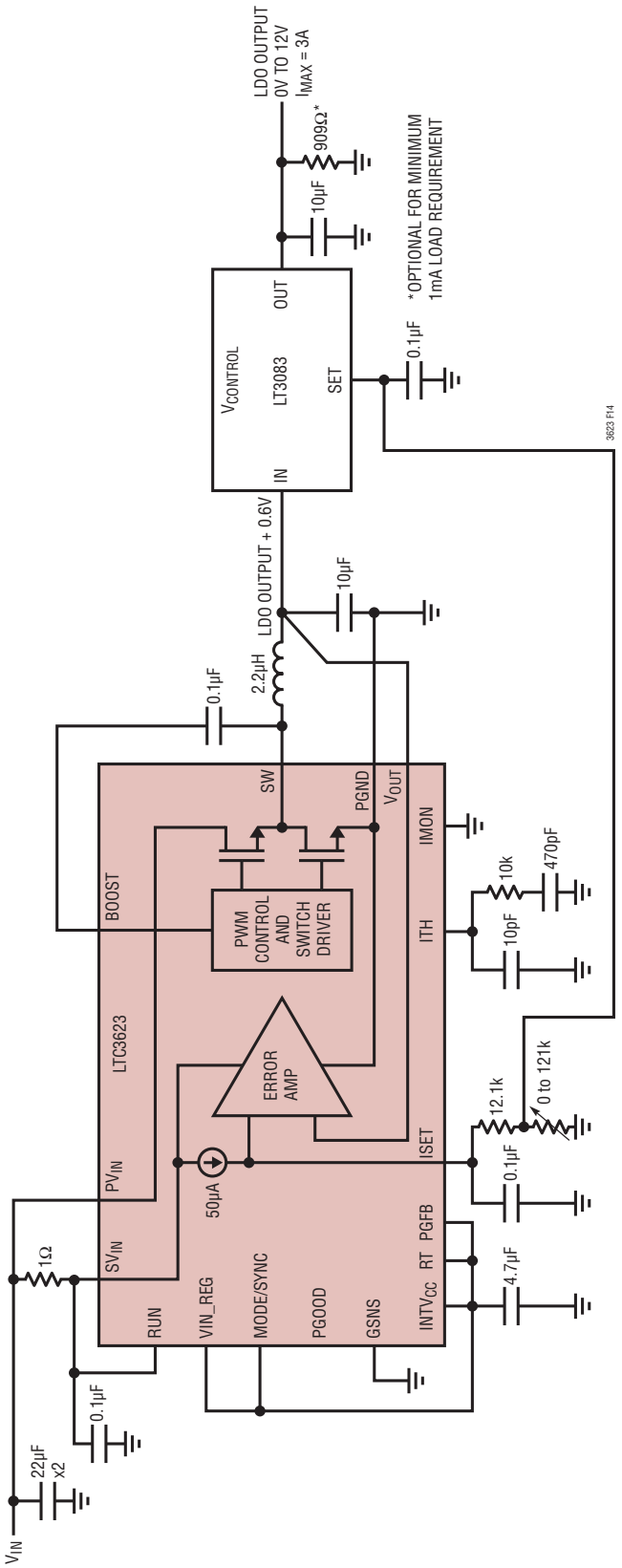


Figure 14. Low Noise Step Down Regulator

TYPICAL APPLICATIONS

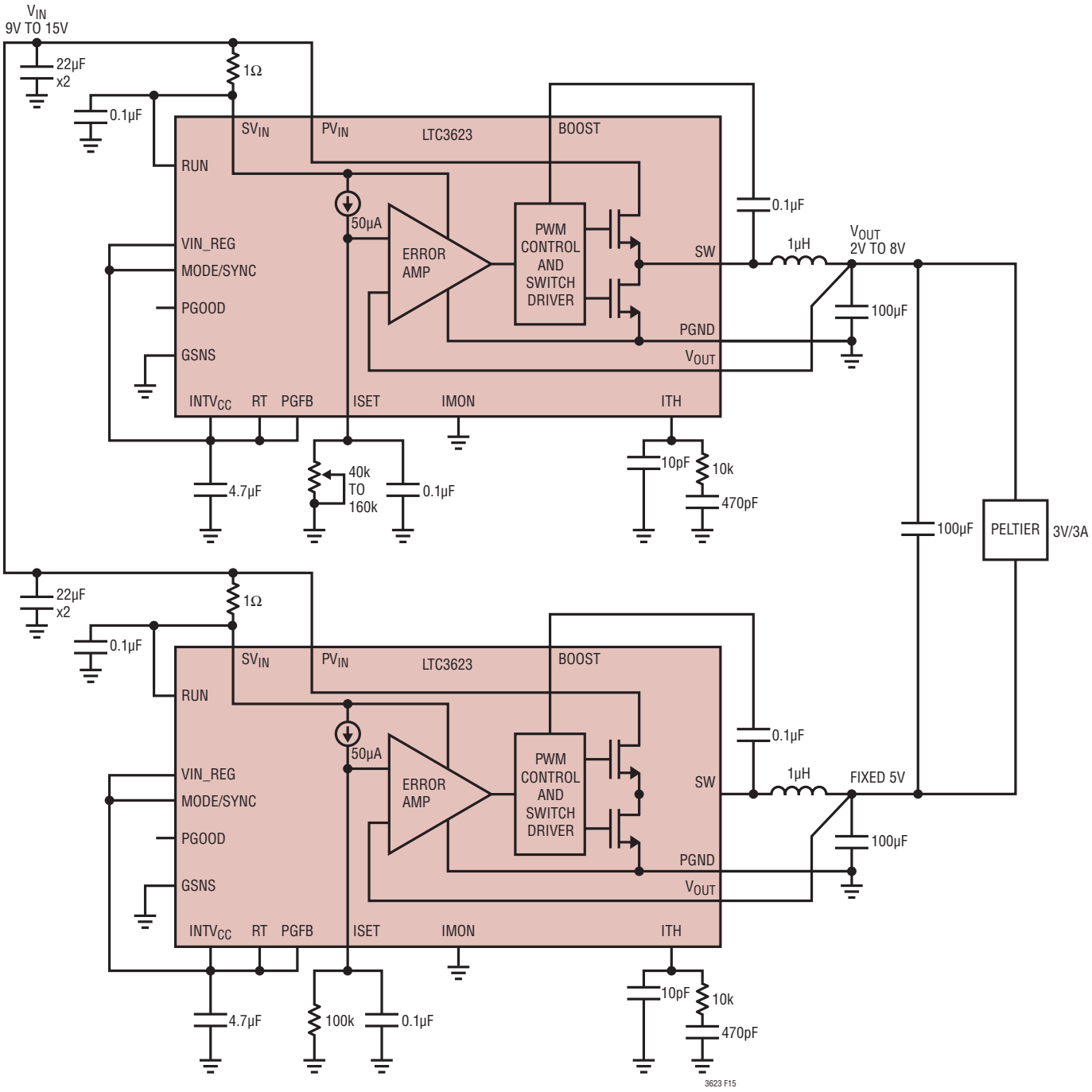
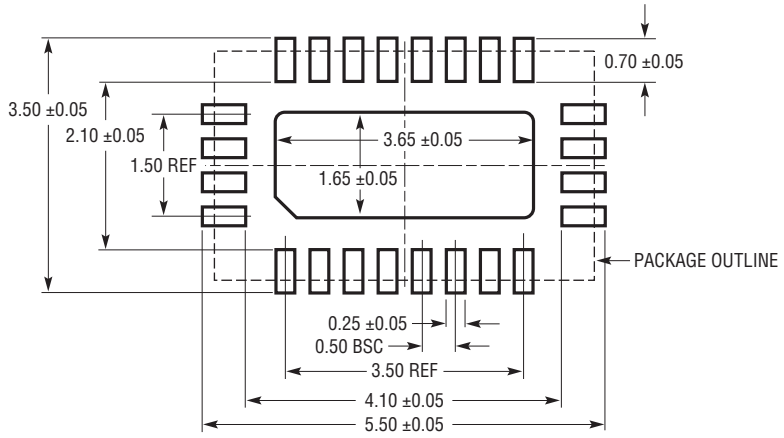


Figure 15. Regulate Positive or Negative Current Across a Peltier Device

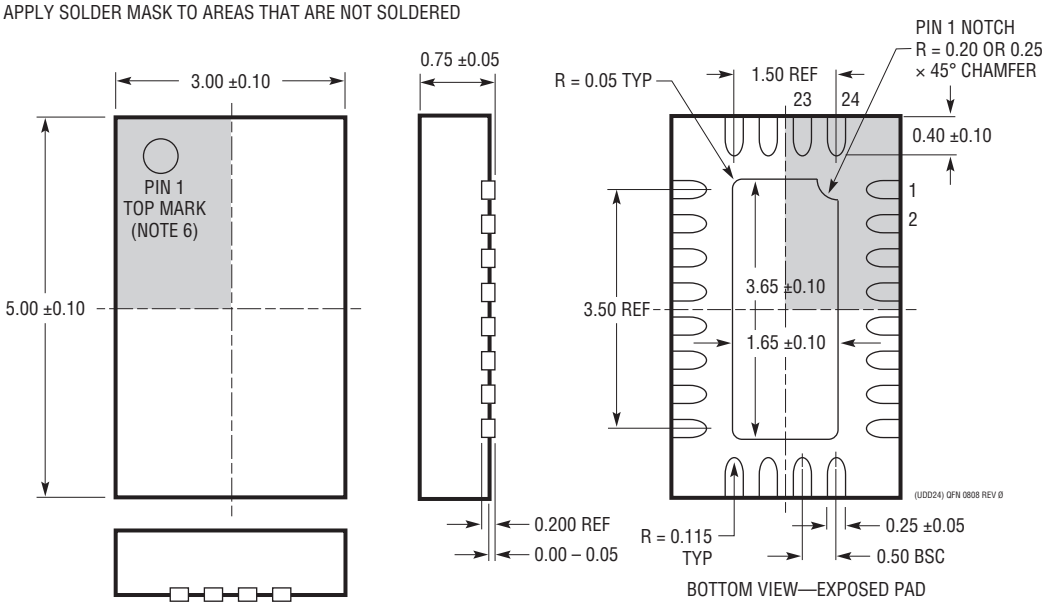
PACKAGE DESCRIPTION

Refer to https://www.analog.com/en/products/ltc3623.html#packaging for the most recent package drawings.

UDD Package
24-Lead Plastic QFN (3mm × 5mm)
(Reference LTC DWG # 05-08-1833 Rev Ø)



RECOMMENDED SOLDER PAD PITCH AND DIMENSIONS
APPLY SOLDER MASK TO AREAS THAT ARE NOT SOLDERED



BOTTOM VIEW—EXPOSED PAD

NOTE:
1. DRAWING IS NOT A JEDEC PACKAGE OUTLINE
2. DRAWING NOT TO SCALE
3. ALL DIMENSIONS ARE IN MILLIMETERS
4. DIMENSIONS OF EXPOSED PAD ON BOTTOM OF PACKAGE DO NOT INCLUDE MOLD FLASH. MOLD FLASH, IF PRESENT, SHALL NOT EXCEED 0.15mm ON ANY SIDE
5. EXPOSED PAD SHALL BE SOLDER PLATED
6. SHADED AREA IS ONLY A REFERENCE FOR PIN 1 LOCATION ON THE TOP AND BOTTOM OF PACKAGE

REVISION HISTORY

REV	DATE	DESCRIPTION	PAGE NUMBER
A	07/17	Modified Typical Application Circuit.	1
		Changed I_{SET} to I_{ISET}.	3, 5
		Changed MODE/SYNC GND to GNDS.	8
		Added Figure 14.	27
B	06/26	Updated the document using the Analog template.	1–31
		Updated Features.	1
		Updated Description.	1
		Updated Electrical Characteristics.	3
		Updated Typical Performance Characteristics.	5
		Updated Pin Functions	8
		Updated Checking Transient Response.	16
		Added Figure 5 and figure numbering has been updated.	20–27

TYPICAL APPLICATION

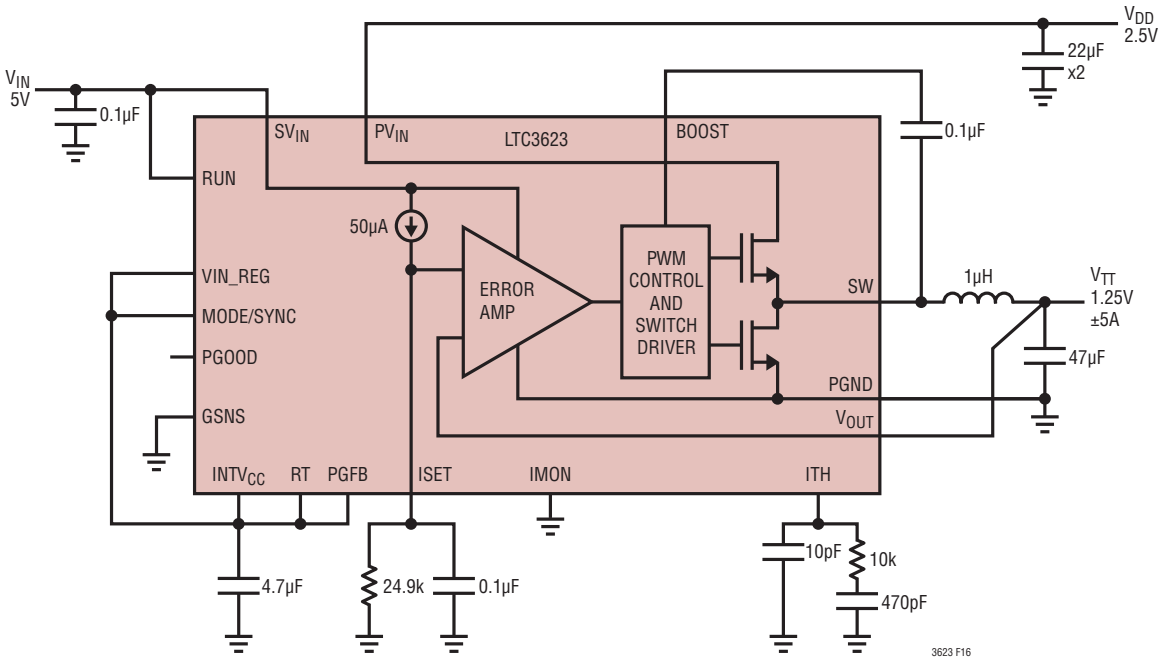


Figure 16. High Efficiency ±5A V_{TT} Supply for DDR Termination

RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LTC3600	15V, 1.5A (I_{OUT}), Synchronized Rail-to-Rail Step-Down DC/DC Converter	96% Efficiency, V_{IN}: 4V to 15V, $V_{OUT(MIN)}$ = 0V, I_Q = 700µA, 3mm × 3mm DFN-12 and MSOP-12E Packages
LTC3601	15V, 1.5A (I_{OUT}), 4MHz, Synchronous Step-Down DC/DC Converter	95% Efficiency, V_{IN}: 4.5V to 15V, $V_{OUT(MIN)}$ = 0.6V, I_Q = 300µA, I_{SD} < 1µA, 4mm × 4mm QFN-20 and MSOP-16E Packages
LTC3603	15V, 2.5A (I_{OUT}), 3MHz, Synchronous Step-Down DC/DC Converter	95% Efficiency, V_{IN}: 4.5V to 15V, $V_{OUT(MIN)}$ = 0.6V, I_Q = 75µA, I_{SD} < 1µA, 4mm × 4mm QFN-20 and MSOP-16E Packages
LTC3633/ LTC3633A	15V/20V, Dual 3A (I_{OUT}), 4MHz, Synchronous Step-Down DC/DC Converter	95% Efficiency, V_{IN}: 3.6V to 15V/20V, $V_{OUT(MIN)}$ = 0.6V, I_Q = 500µA, I_{SD} < 15µA, 4mm × 5mm QFN-28 and TSSOP-28E Packages
LTC3605/ LTC3605A	15V/20V, 5A (I_{OUT}), 4MHz, Synchronous Step-Down DC/DC Converter	95% Efficiency, V_{IN}: 4V to 15V/20V, $V_{OUT(MIN)}$ = 0.6V, I_Q = 2mA, I_{SD} < 15µA, 4mm × 4mm QFN-24 and MSOP-16E Packages
LTC3604	15V, 2.5A (I_{OUT}), 4MHz, Synchronous Step-Down DC/DC Converter	95% Efficiency, V_{IN}: 3.6V to 15V, $V_{OUT(MIN)}$ = 0.6V, I_Q = 300µA, I_{SD} < 14µA, 3mm × 3mm QFN-16 and MSOP-16E Packages
LT3080	1.1A, Parallelable, Low Noise, Low Dropout Linear Regulator	300mV Dropout Voltage (2 Supply Operation), Low Noise = 40µV_{RMS} V_{IN}: 1.2V to 36V, V_{OUT}: 0V to 35.7V, MSOP-8, 3mm × 3mm DFN Packages
LT3083	Adjustable 3A Single Resistor Low Dropout Regulator	310mV Dropout Voltage, Low Noise 40µV_{RMS} V_{IN}: 1.2V to 23V, V_{OUT}: 0V to 22.7V, 4mm × 4mm DFN, TSSOP-16E Packages
LTC7149	60V, 4A Synchronous Step-Down Regulator for Inverting Inputs	Wide V_{IN} Range: 3.4V to 60V; Wide V_{OUT} Range: 0V to 28V; Single Resistor V_{OUT} Programming; 92% Efficiency with 12V_{IN} and –5V_{OUT}; Regulated I_Q: 440µA, Shutdown I_Q: 15µA; 28-Lead (4mm × 5mm) QFN and TSSOP Packages
LTC3649	60V, 4A Synchronous Step-Down Regulator with Rail-to-Rail Programmable Output	Wide V_{IN} Range: 3.1V to 60V; Wide V_{OUT} Range: 0V to (V_{IN} – 0.5V); Single Resistor V_{OUT} Programming; 95% Efficiency with 12V_{IN} and 5V_{OUT}; Regulated I_Q: 440µA, Shutdown I_Q: 15µA; 28-Lead (4mm × 5mm) QFN and TSSOP Packages