5V, Dual 6A/Dual-Phase 12A Step-Down DC/DC Regulator

FEATURES

- **Dual 6A Outputs**
- **Configurable as Single Output, 2-Phase 12A Buck**
- **High Efficiency: 12mΩ High-Side and 8mΩ Low-Side**
- **±1% Maximum Total DC Output Error**
- **Wide Bandwidth, Fast Transient Response**
- **Internal Input Capacitors Reduce EMI**
- V_{IN} Range: 2.25V to 5.5V
- V_{OUT} Range: 0.5V to V_{IN}
- Programmable Frequency to 3MHz
- Low Ripple Burst Mode® Operation with Low I_Q
- Shutdown Current: 1.4µA
- 35ns Minimum On-Time
- Internal Compensation
- Precision Enable, Power Good for Power Sequencing
- Tracking, Programmable Soft-Start, Temp Monitor Output
- Thermally Enhanced, 22-Lead 4mm × 3mm × 0.95mm LQFN package
- AEC-Q100 Qualified for Automotive Applications

APPLICATIONS

- Servers, Telecom Power Supplies, Optical Networking
- Distributed DC Power Systems (POL)
- FPGA, ASIC, µP Core Supplies
- Industrial/Automotive/Communications

DESCRIPTION

The LTC®3312SA features dual monolithic synchronous 6A step-down converters in a 4mm × 3mm package for space saving applications with demanding performance requirements. Using a constant frequency, peak current mode architecture at switching frequencies up to 3MHz, both bucks achieve high efficiency and fast transient response with small external components. The LTC3312SA can also be configured as a single output, 2-phase 12A step-down converter.

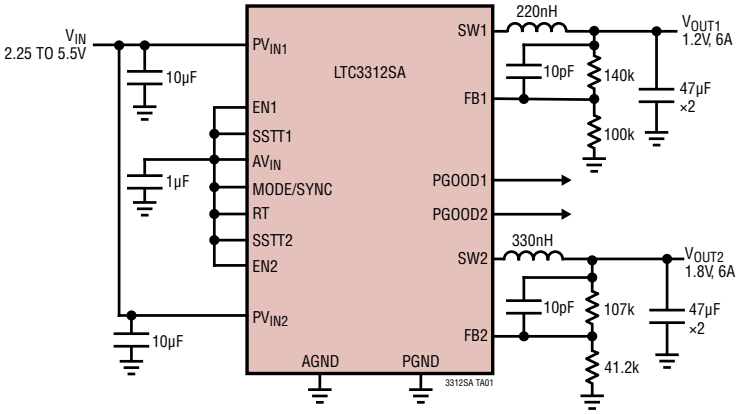
The LTC3312SA operates in forced continuous or pulse-skipping mode for low noise, or in Burst Mode operation for high efficiency at light loads. The common switching frequency is set to a default 2MHz, programmed with an external resistor, or synchronized to an external oscillator via the MODE/SYNC pin. To reduce input ripple current, the dual converters switch 180 degrees out of phase.

With an input range of 2.25V to 5.5V the LTC3312SA regulates to outputs as low as 500mV. Other features include precision enable thresholds, PGOOD signals, output overvoltage protection, thermal shutdown, and output short circuit protection. Programmable soft-start and a temperature monitor output are also included. The device is available in a low profile 22-lead 4mm × 3mm × 0.95mm LQFN package with exposed pad for low thermal resistance.

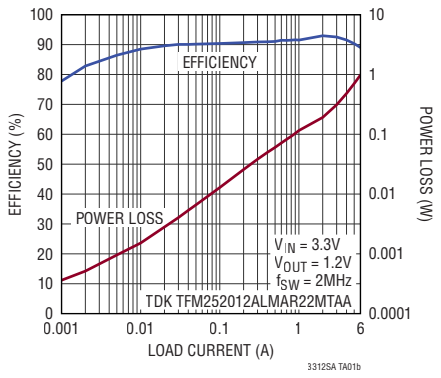
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TYPICAL APPLICATION

Dual 2MHz 6A Buck Regulators



Efficiency and Power Loss in Burst Mode Operation



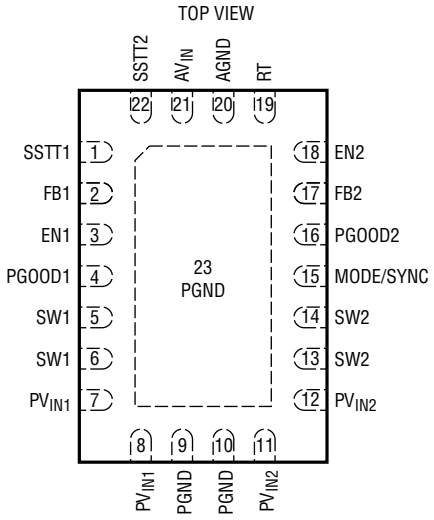
Rev. B

ABSOLUTE MAXIMUM RATINGS

(Note 1)

PV_{IN1}, PV_{IN2}, AV_{IN} ..... –0.3V to 6V
EN1, EN2 ..... –0.3V to Lesser of (AV_{IN} + 0.3V) or 6V
FB1, FB2 ..... –0.3V to Lesser of (AV_{IN} + 0.3V) or 6V
MODE/SYNC ..... –0.3V to Lesser of (AV_{IN} + 0.3V) or 6V
RT ..... –0.3V to Lesser of (AV_{IN} + 0.3V) or 6V
SSTT1, SSTT2 .... –0.3V to Lesser of (AV_{IN} + 0.3V) or 6V
AGND to PGND ..... –0.3V to +0.3V
PGOOD1, PGOOD2 ..... –0.3V to 6V
I_{PGOOD1}, I_{PGOOD2} 5mA
Operating Junction Temperature Range (Note 2):
LTC3312SAA ..... –40°C to 125°C
LTC3312SAJ ..... –40°C to 125°C
Storage Temperature Range ..... –65°C to 150°C
Maximum Reflow (Package Body)Temperature .... 260°C

PIN CONFIGURATION



LQFN PACKAGE
22-LEAD (4mm × 3mm)
$^{2}\theta_{JA}$ = 36.5°C/W, θ_{JCTOP} = 50.3°C/W,
$\theta_{JCBOTTOM}$ = 4.4°C/W

NOTES:
1. θ_{JA} VALUE IS OBTAINED WITH DEMO BOARD.
2. θ VALUES ARE DETERMINED BY SIMULATION PER JESD-51 CONDITIONS.

ORDER INFORMATION

PART NUMBER	PART MARKING*	FINISH CODE	PAD FINISH	PACKAGE TYPE	MSL RATING	TEMPERATURE RANGE
LTC3312SAAV#PBF	312SA	e4	Au (RoHS)	LQFN (Laminate Package with QFN Footprint)	3	–40°C to 125°C
LTC3312SAAV#TRPBF	312SA	e4	Au (RoHS)	LQFN (Laminate Package with QFN Footprint)	3	–40°C to 125°C
AUTOMOTIVE PRODUCTS**						
LTC3312SAJV#WPBF	312SA	e4	Au (RoHS)	LQFN (Laminate Package with QFN Footprint)	3	–40°C to 125°C
LTC3312SAJV#WTRPBF	312SA	e4	Au (RoHS)	LQFN (Laminate Package with QFN Footprint)	3	–40°C to 125°C

Contact the factory for parts specified with wider operating temperature ranges. *The temperature grade is identified by a label on the shipping container.

**Versions of this part are available with controlled manufacturing to support the quality and reliability requirements of automotive applications. These models are designated with a #W suffix. Only the automotive grade products shown are available for use in automotive applications. Contact your local Analog Devices account representative for specific product ordering information and to obtain the specific Automotive Reliability reports for these models.

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V_{IN} = 3.3V, unless otherwise noted. PV_{IN} = PV_{IN1} = PV_{IN2}

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Operating Supply Voltage (PV_{IN})		●	2.25		5.5	V
PV_{IN} Undervoltage Lockout PV_{IN} Undervoltage Lockout Hysteresis	PV_{IN} Rising	●	2.05	2.15 150	2.25	V mV
PV_{IN} Quiescent Current in Shutdown				1.4	3	µA
PV_{IN} Quiescent Current with One Buck Enabled	Burst Mode Operation, Sleeping All Modes, Not Sleeping, (Note 3)			50 1.5	80 2.3	µA mA
PV_{IN} Quiescent Current with Both Bucks Enabled	Burst Mode Operation, Sleeping All Modes, Not Sleeping, (Note 3)			90 2.8	130 4.2	µA mA
Enable Threshold Enable Threshold Hysteresis	V_{EN} Rising	●	0.375	0.4 50	0.425	V mV
EN Pin Leakage					±20	nA
Voltage Regulation, Buck 1 and Buck 2						
Regulated Feedback Voltage (V_{FB})		●	495	500	505	mV
Feedback Voltage Line Regulation	2.25V ≤ PV_{IN} ≤ 5.5V			0.02	0.1	%/V
Feedback Pin Input Current	V_{FB} = 500mV				±20	nA
Top Switch Current Limit ($I_{PEAKMAX}$)	Current Out of SW, V_{OUT}/V_{IN} ≤ 0.2V		9.1	9.6	10.1	A
Bottom Switch Current Limit ($I_{VALLEYMAX}$)	Current Out of SW			7.8		A
Bottom Switch Reverse Current Limit (I_{LIMR})	Current into SW, Forced Continuous Mode		2.5	4.0	5.5	A
Top Switch ON-Resistance				12		mΩ
Bottom Switch ON-Resistance				8		mΩ
SW Leakage Current	Shutdown, V_{IN} = 5.5V				±1	µA
Minimum On-Time	V_{IN} = 5.5V	●		35	50	ns
Maximum Duty-Cycle		●	98			%
Overtemperature Shutdown (OT) Overtemperature Shutdown Hysteresis	Temperature Rising (Note 4)			165 5		°C °C
Power Good/Soft-Start/Temp Monitor						
PGOOD Rising Threshold PGOOD Hysteresis	As a % of the Regulated V_{OUT}	● ●	97 0.6	98 1.1	99 1.6	% %
Overvoltage Rising Threshold Overvoltage Hysteresis	As a % of the Regulated V_{OUT}	● ●	107 1	110 2.2	114 3.5	% %
PGOOD Delay				100		µs
PGOOD Pull-Down Resistance	V_{PGOOD} = 0.1V			10	20	Ω
PGOOD Leakage Current	V_{PGOOD} = 5.5V				20	nA
Default Soft-Start Duration	V_{SSTT} = AV_{IN}, V_{OUT} Rising from 0V to PGOOD Threshold			1		ms
Soft-Start Charge Current	V_{SSTT} = 0.5V	●	3	4	5	µA

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V_{IN} = 3.3V, unless otherwise noted. PV_{IN} = PV_{IN1} = PV_{IN2}

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Temp Monitor Slope				4		mV/°C
Oscillator and MODE/SYNC						
Default Oscillator Frequency	R_T = AV_{IN}	●	1.85	2	2.15	MHz
Oscillator Frequency	R_T = 34.8kΩ to AGND	●	1.9	2	2.1	MHz
Frequency Range	R_T-Programming and Synchronization	●	1		3	MHz
Minimum SYNC High or Low Pulse Width		●	40			ns
SYNC Level High on MODE/SYNC SYNC Level Low on MODE/SYNC		● ●	1.2		 0.4	V V
MODE/SYNC No Clock Detect Time		●		10		µs
MODE/SYNC Pin Threshold	For Programming Pulse-Skipping Mode For Programming Burst Mode Operation	●	 V_{IN} – 0.1		0.1	V V

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect the device reliability and lifetime.

Note 2: The LTC3312SA is tested under pulsed load conditions such that T_J = T_A. The LTC3312SA is guaranteed to meet performance specifications from –40°C to 125°C junction temperature. High junction temperatures degrade operating lifetimes; operating lifetime is derated for junction temperatures above 125°C. Note that the maximum ambient temperature consistent with these specifications is determined by specific operating conditions in conjunction with board layout, the rated package thermal impedance, and other environmental factors. The junction temperature (T_J in °C) is calculated from ambient temperature (T_A in °C) and power dissipation (P_D in Watts) according to the formula: $T_J = T_A + (P_D \bullet \theta_{JA})$, where θ_{JA} (in °C/W) is the package thermal impedance. See the High Temperature Considerations section for more details.

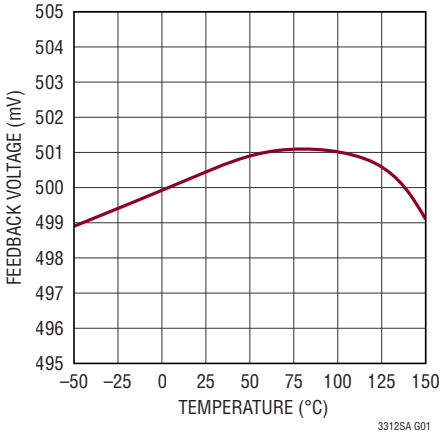
The LTC3312SA includes overtemperature protection that protects the device during momentary overload conditions. Junction temperatures will exceed 150°C when overtemperature protection is engaged. Continuous operation above the specified maximum operating junction temperature may impair device reliability.

Note 3: Supply current specification does not include switching currents. Actual supply currents will be higher.

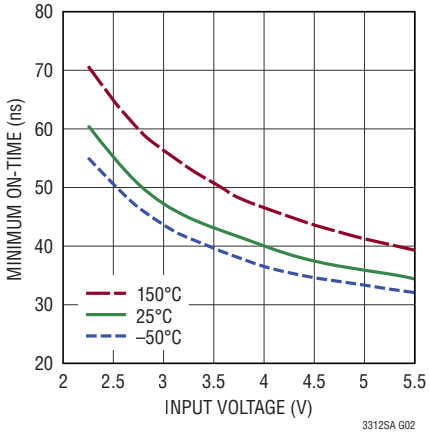
Note 4: Overtemperature shutdown in not tested in production.

TYPICAL PERFORMANCE CHARACTERISTICS T_A = 25°C, unless otherwise noted.

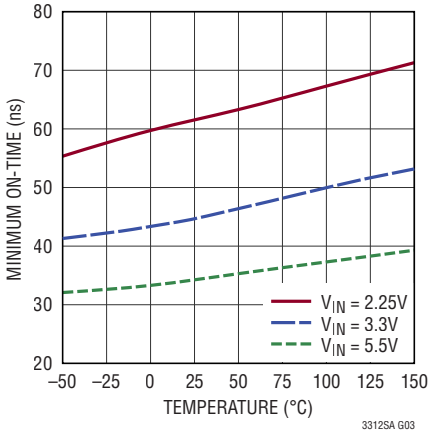
Feedback Voltage



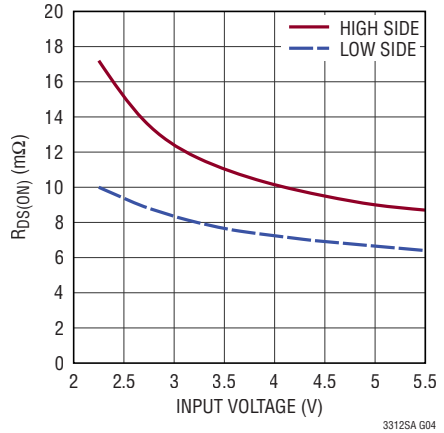
Minimum On-Time vs V_{IN}



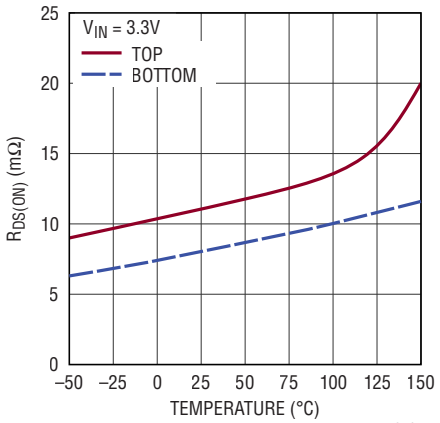
Minimum On-Time



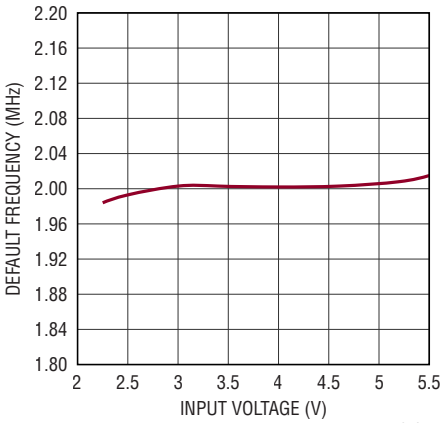
Switch On-Resistance vs V_{IN}



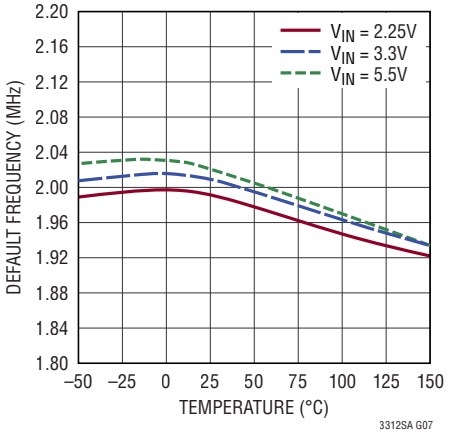
Switch On-Resistance



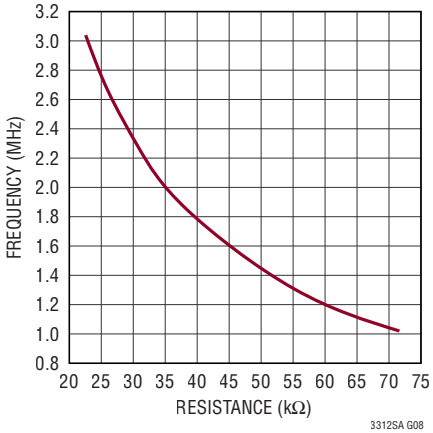
Default Switching Frequency vs V_{IN}



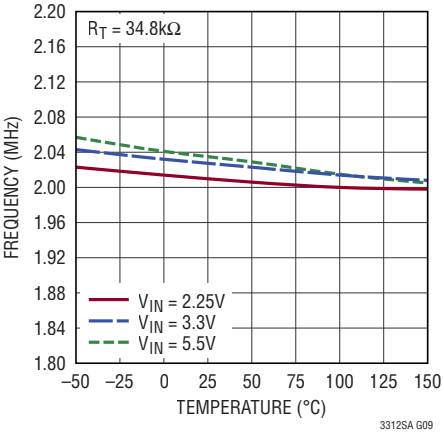
Default Switching Frequency



Switching Frequency vs R_T

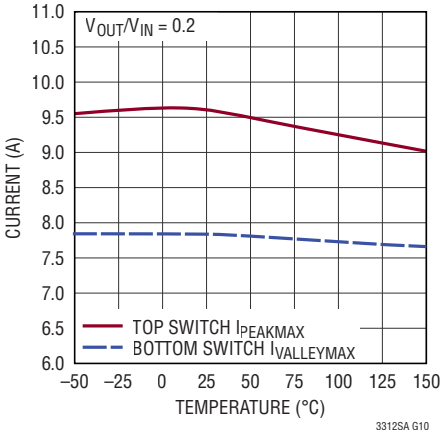


Switching Frequency

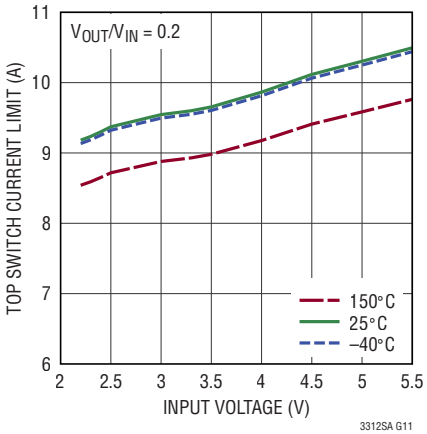


TYPICAL PERFORMANCE CHARACTERISTICS T_A = 25°C, unless otherwise noted.

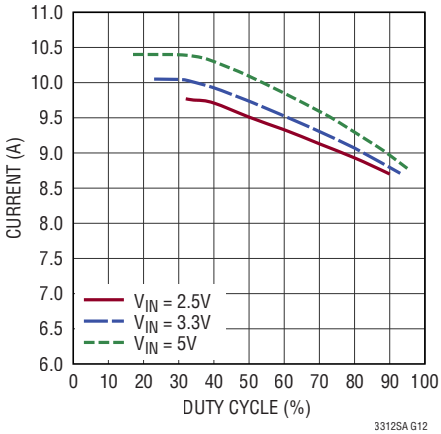
Switch Current Limits



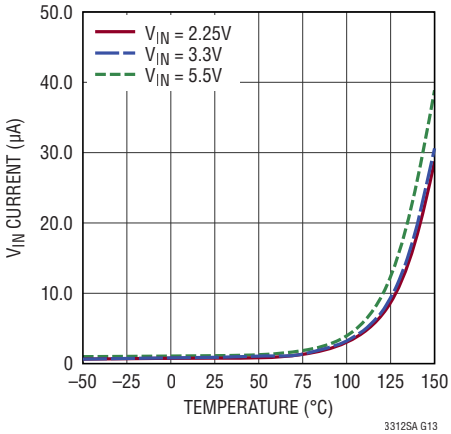
Top Switch Current Limit vs V_{IN}



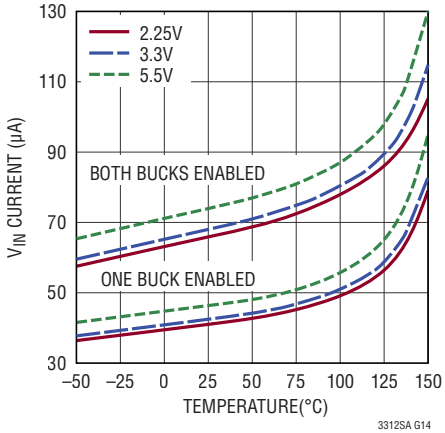
Top Switch Current Limit



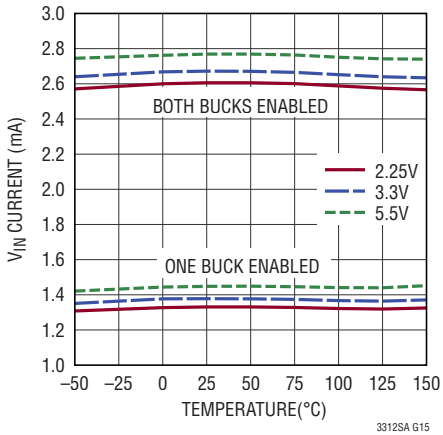
PV_{IN} Shutdown Current



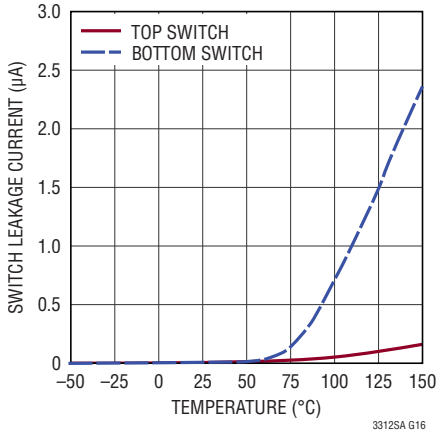
PV_{IN} Quiescent Current, Burst Mode Operation, Sleeping



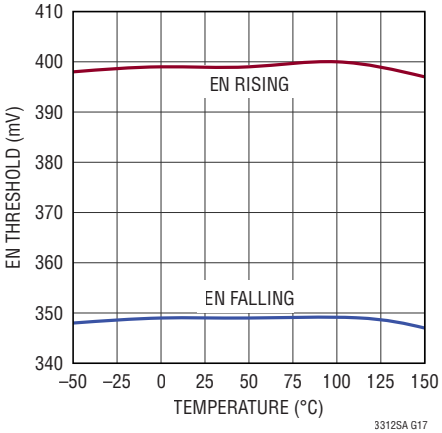
PV_{IN} Shutdown Quiescent Current, All Modes, Not Sleeping



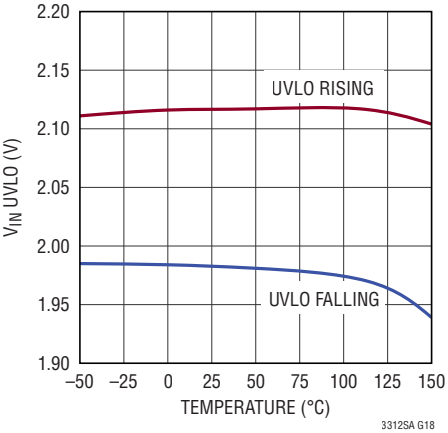
Switch Leakage



EN Threshold

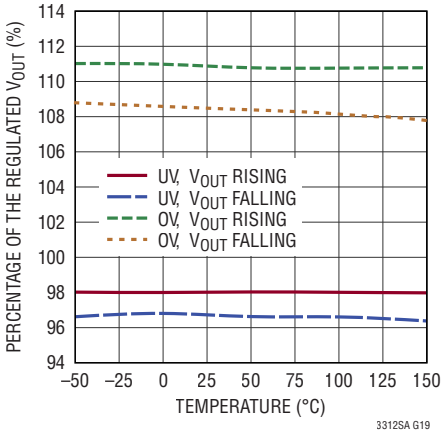


PV_{IN} UVLO Threshold

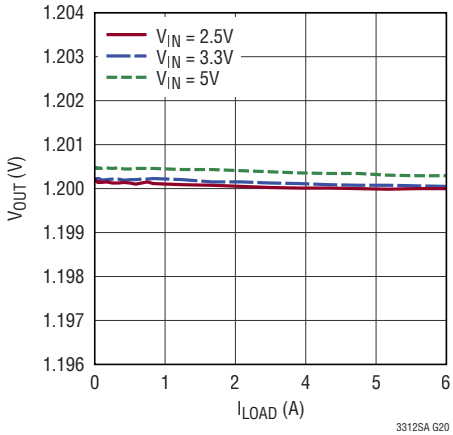


TYPICAL PERFORMANCE CHARACTERISTICS T_A = 25°C, unless otherwise noted.

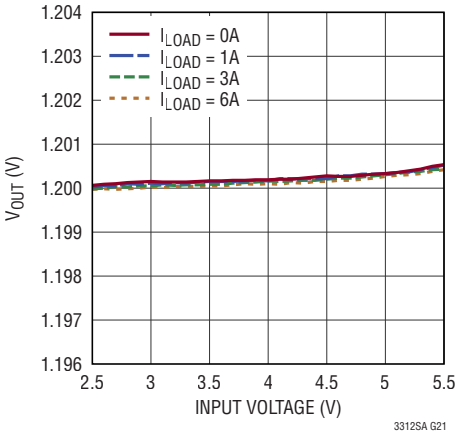
UV, OV PGOOD Thresholds



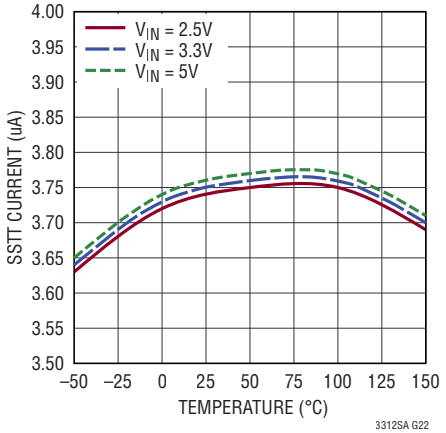
VOUT Load Regulation for the VOUT = 1.2V Application Forced Continuous Mode



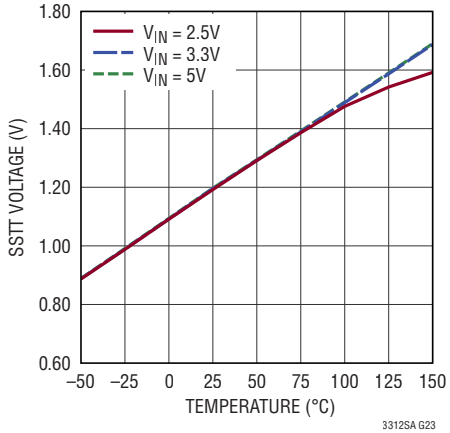
VOUT Line Regulation for the VOUT = 1.2V Application Forced Continuous Mode



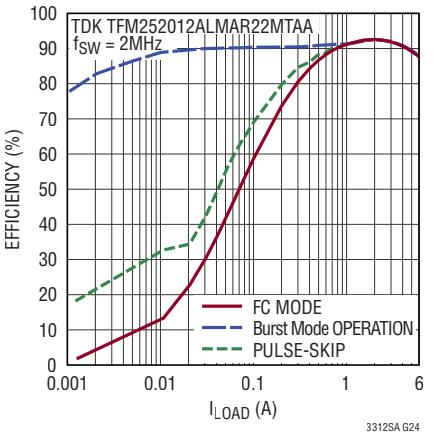
SSTT Current vs Temperature



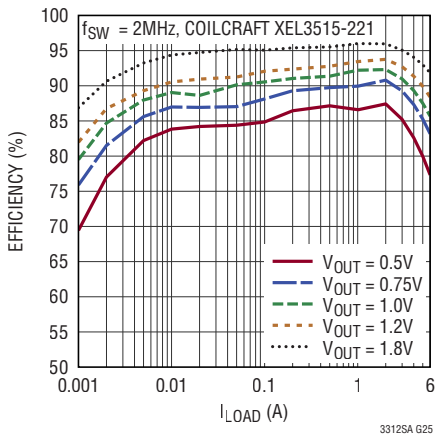
SSTT Voltage vs Temperature



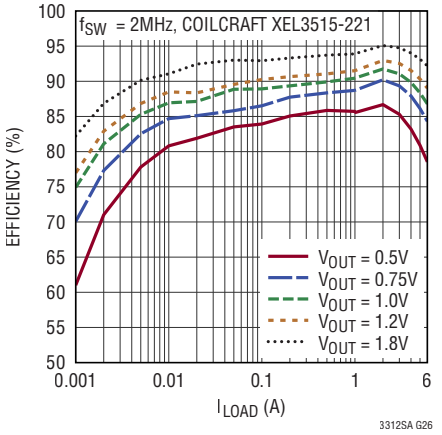
Efficiency, VIN = 3.3V, VOUT = 1.2V, All Modes



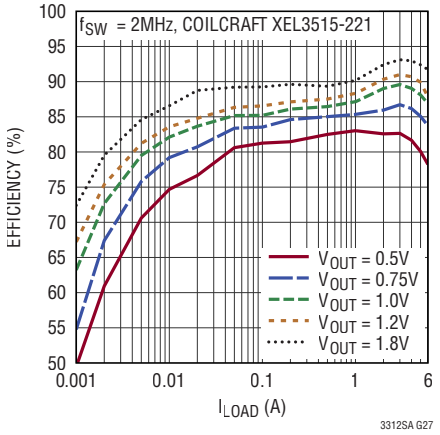
Efficiency, VIN = 2.5V, Burst Mode Operation



Efficiency, VIN = 3.3V, Burst Mode Operation

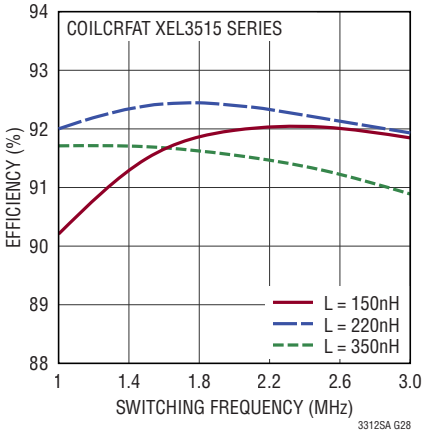


Efficiency, VIN = 5.0V, Burst Mode Operation

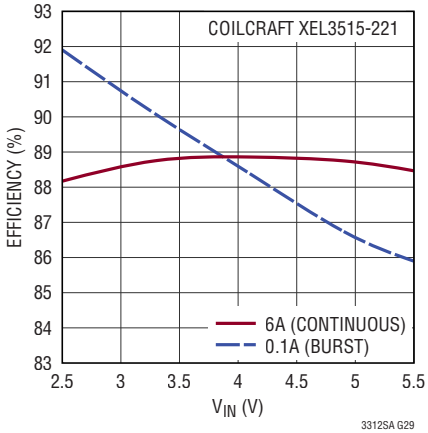


TYPICAL PERFORMANCE CHARACTERISTICS T_A = 25°C, unless otherwise noted.

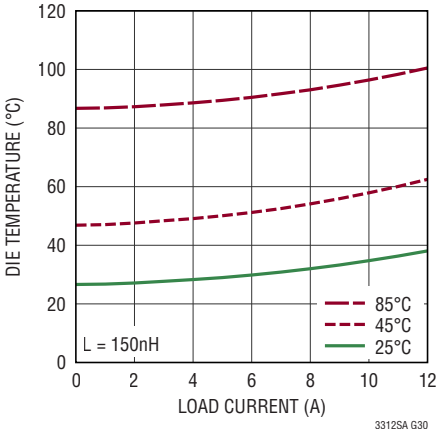
Efficiency vs f_{SW}
3.3V to 1.2V, I_{LOAD} = 3A



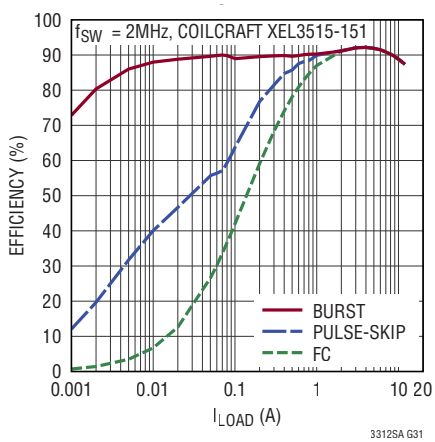
Efficiency vs V_{IN}
V_{OUT} = 1.2V, f_{SW} = 2MHz



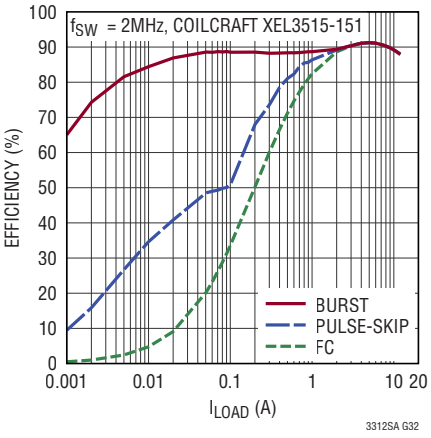
2-Phase Die Temperature vs Load
3.3V_{IN} to 1.0V_{OUT}, f_{SW} = 2MHz,
Forced Continuous Mode



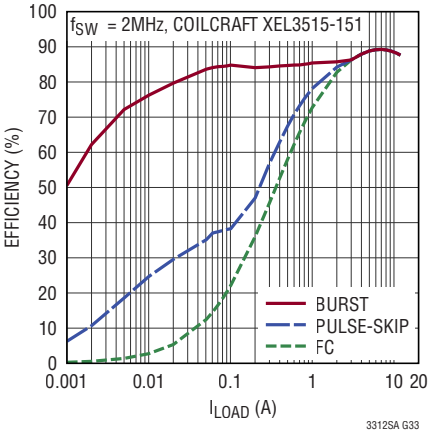
2-Phase Efficiency vs Load,
2.5V to 1.0V, f_{SW} = 2MHz



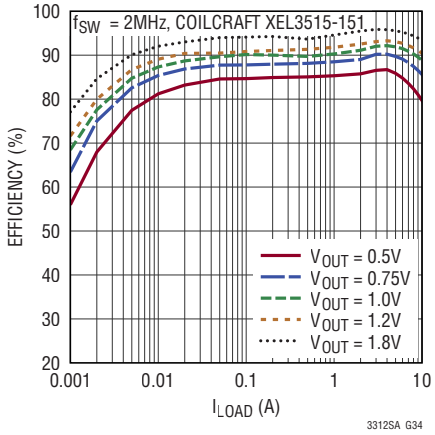
2-Phase Efficiency vs Load,
3.3V to 1.0V, f_{SW} = 2MHz



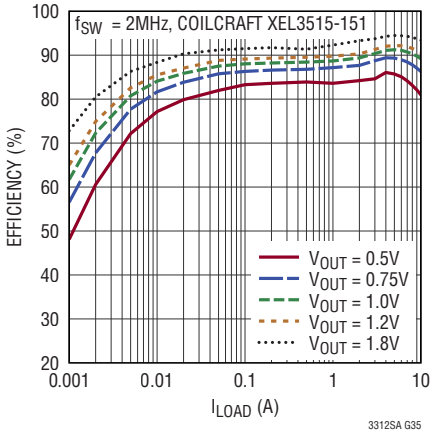
2-Phase Efficiency vs Load,
5.0V to 1.0V, f_{SW} = 2MHz



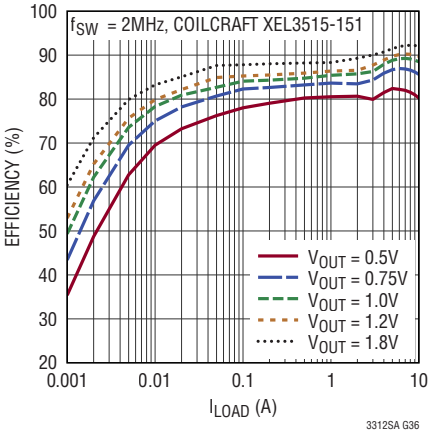
2-Phase Efficiency, V_{IN} = 2.5V
Burst Mode Operation



2-Phase Efficiency, V_{IN} = 3.3V
Burst Mode Operation

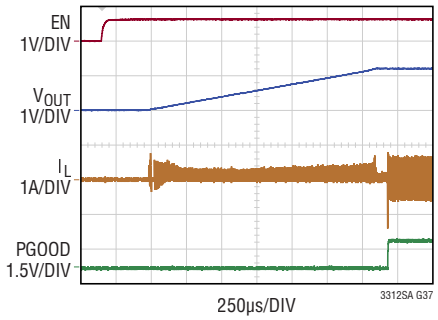


2-Phase Efficiency, V_{IN} = 5.0V
Burst Mode Operation



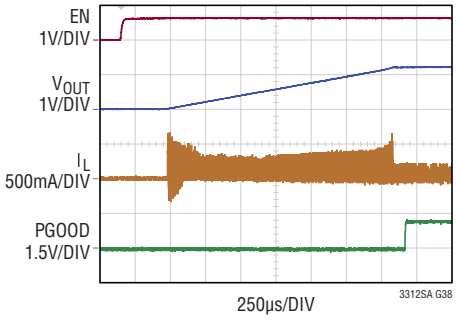
TYPICAL PERFORMANCE CHARACTERISTICS T_A = 25°C, unless otherwise noted.

Start-Up Waveforms Forced Continuous Mode



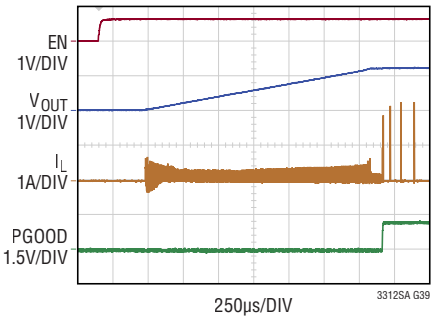
3.3V TO 1.2V, 2MHz TYPICAL APPLICATION
R_{LOAD} = 120Ω

Start-Up Waveforms Pulse-Skipping Mode



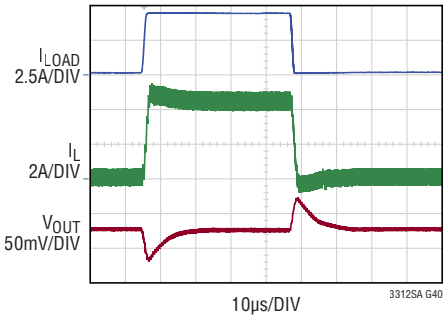
3.3V TO 1.2V, 2MHz TYPICAL APPLICATION
R_{LOAD} = 120Ω

Start-Up Waveforms Burst Mode Operation



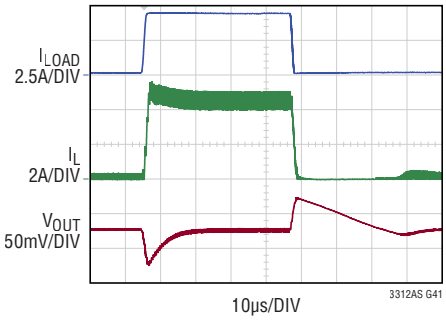
3.3V TO 1.2V, 2MHz TYPICAL APPLICATION
R_{LOAD} = 120Ω

Load Transient Response, Forced Continuous Mode



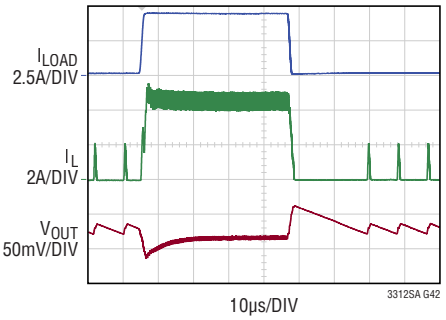
3.3V TO 1.2V, 2MHz TYPICAL APPLICATION
C_{OUT} = 66µF, L = 220nH
LOAD STEP: 0.1A TO 4.5A IN 1µs

Load Transient Response, Pulse-Skipping Mode



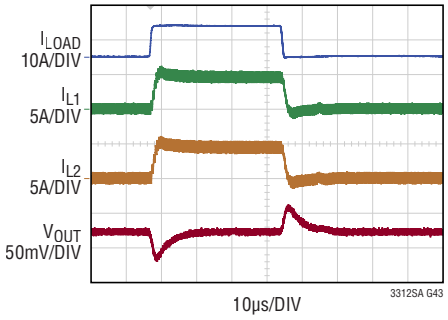
3.3V TO 1.2V, 2MHz TYPICAL APPLICATION
C_{OUT} = 66µF, L = 220nH
LOAD STEP: 0.1A TO 4.5A IN 1µs

Load Transient Response, Burst Mode Operation



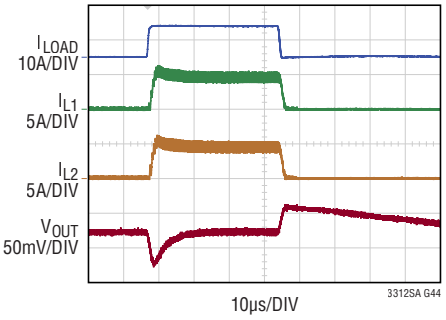
3.3V TO 1.2V, 2MHz TYPICAL APPLICATION
C_{OUT} = 66µF, L = 220nH
LOAD STEP: 0.1A TO 4.5A IN 1µs

2-Phase Configuration Load Transient Response, Forced Continuous Mode



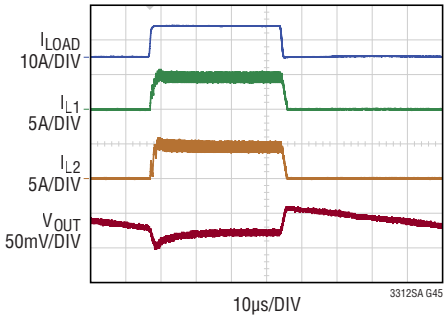
3.3V TO 1.0V, 2MHz 2-PHASE APPLICATION
C_{OUT} = 47µF ×6, L = 150nH
LOAD STEP: 0.1A TO 9A IN 1µs

2-Phase Configuration Load Transient Response, Pulse-Skipping Mode



3.3V TO 1.0V, 2MHz 2-PHASE APPLICATION
C_{OUT} = 47µF ×6, L = 150nH
LOAD STEP: 0.1A TO 9A IN 1µs

2-Phase Configuration Load Transient Response, Burst Mode Operation



3.3V TO 1.0V, 2MHz 2-PHASE APPLICATION
C_{OUT} = 47µF ×6, L = 150nH
LOAD STEP: 0.1A TO 9A IN 1µs

PIN FUNCTIONS

SSTT1 (Pin 1) : Soft-Start, Tracking, Temperature Monitor Input for Buck Regulator 1. An internal 4µA current into an external capacitor on the soft-start pin programs the output voltage ramp rate during start-up. When SSTT1 is below 0.5V, the FB1 pin voltage will track the SSTT1 pin voltage. When SSTT1 is above 0.5V, the tracking function is disabled, the internal reference resumes control of the error amplifier and the SSTT1 pin servos to a voltage proportional to junction temperature. For a clean recovery from an output short circuit condition, the SSTT1 pin is pulled down to approximately 100mV above the V_{FB} voltage and a new soft-start cycle is initiated. During shutdown and fault conditions, the SSTT1 pin is pulled to ground. Short the SSTT1 pin to AV_{IN} to use an internally set default soft-start time of 1ms (typical).

FB1 (Pin 2): Feedback Input for Buck Regulator 1. Program the output voltage of Buck 1 by connecting this pin to the middle node of a resistor divider between the output and ground. The FB1 pin is regulated to 500mV. A phase lead capacitor connected between V_{OUT1} and FB1 may be used to optimize transient response.

EN1 (Pin 3): Active High Enable Input for Buck Regulator 1. The EN1 pin has a precision threshold. An external resistor divider from V_{IN}, or from another supply, can be used to program when Buck Regulator 1 is enabled. If the enable function is not required, tie EN1 directly to AV_{IN}. The EN1 pin should not be floated.

PGOOD1 (Pin 4): Power Good (Open-Drain) Output for Buck Regulator 1. When the regulated output voltage is outside the power-good voltage window, and PV_{IN} is above 2.25V, this pin is driven LOW. The PGOOD1 output is also pulled low when PV_{IN} is above 2.25V and Buck Regulator 1 is in shutdown.

SW1 (Pins 5, 6): Switch Node for Buck Regulator 1. Connect an external inductor to this pin.

PV_{IN1} (Pins 7, 8): Input Supply for Buck Regulator 1. Supplies gate drive circuits and inductor current when the high side turns on. Bypass PV_{IN1} to PGND with a separate low ESR capacitor close to the pins. PV_{IN1} and PV_{IN2} should be shorted externally. Use separate capacitors to PGND for PV_{IN1} and PV_{IN2} to prevent interaction between the buck regulators. There is an internal 20Ω resistor from PV_{IN1} to AV_{IN} to help create a filtered supply for the internal control circuits.

PGND (Pins 9,10, 23): The PGND pins are the return path of the internal bottom side power switches. Connect the PGND pins together and to the exposed pad. Connect the negative terminal of the input capacitors as close to the PGND pins as possible. The PGND node is the main thermal highway and should be connected to a large PCB ground plane with many large vias.

PV_{IN2} (Pins 11, 12): Input Supply for Buck Regulator 2. Supplies gate drive circuits and inductor current when the high side turns on. Bypass PV_{IN2} to PGND with a separate low ESR capacitor close to the pins. PV_{IN1} and PV_{IN2} should be shorted externally. Use separate capacitors to PGND for PV_{IN1} and PV_{IN2} to prevent interaction between the buck regulators. There is an internal 20Ω resistor from PV_{IN2} to AV_{IN} to help create a filtered supply for the internal control circuits.

SW2 (Pins 13,14): Switch Node for Buck Regulator 2. Connect an external inductor to this pin.

MODE/SYNC (Pin 15): Mode Selection and External Clock Synchronization Input. Ground this pin to enable pulse-skipping mode. Tie this pin to AV_{IN} to enable Burst Mode operation for higher efficiency at light loads. Float this pin to enable forced continuous mode for fast transient response and full frequency operation over a wide load range. Drive MODE/SYNC with an external clock to synchronize both switchers to the applied frequency. The slope compensation is automatically adapted to the external clock frequency. In the absence of an external clock, the RT pin controls the switching frequency.

PIN FUNCTIONS

PGOOD2 (Pin 16): Power Good (Open-Drain) Output for Buck Regulator 2. When the regulated output voltage is outside the power-good voltage window, and PV_{IN} is above 2.25V, this pin is driven LOW. The PGOOD2 output is also pulled low when V_{IN} is above 2.25V and Buck Regulator 2 is in shutdown.

FB2 (Pin 17): Feedback Input for Buck Regulator 2. Program the output voltage of Buck 2 by connecting this pin to the middle node of a resistor divider between the output and ground. The FB2 pin is regulated to 500mV. A phase lead capacitor connected between V_{OUT2} and FB2 may be used to optimize transient response.

EN2 (Pin 18): Active high Enable Input for Buck Regulator 2. The EN2 pin has a precision threshold. An external resistor divider from V_{IN}, or from another supply, can be used to program when Buck Regulator 2 is enabled. If the enable function is not required, tie EN2 directly to AV_{IN}. The EN2 pin should not be floated.

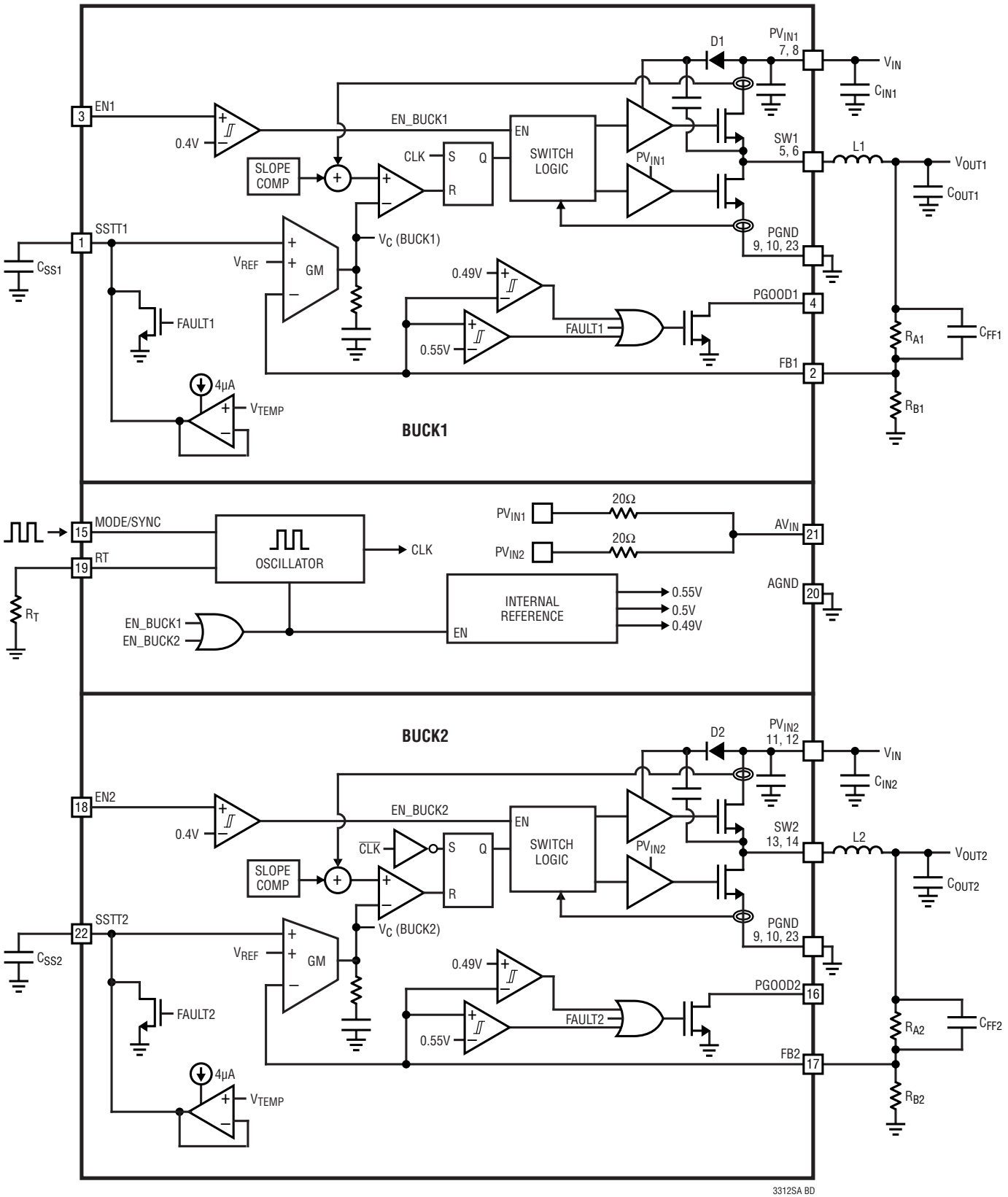
RT (Pin 19): The RT pin sets the switching frequency with an external resistor to AGND. If this pin is tied to AV_{IN}, the buck will switch at the default oscillator frequency. If the external clock is driving the MODE/SYNC pin, the RT pin is ignored.

AGND (Pin 20): The AGND pin is the ground pin for the internal bias circuits, including the bandgap reference. Connect the bottom resistor of the FB1 and FB2 resistor dividers to the AGND pin for accurate output voltage regulation.

AV_{IN} (Pin 21): Filtered Input Supply used to bias the internal bandgap reference and buck control circuits. There are internal 20Ω resistors from PV_{IN1} to AV_{IN}, and from PV_{IN2} to AV_{IN}. Connect a 1µF ceramic capacitor from AV_{IN} to AGND to provide a filtered supply for the internal control circuits. Do not externally load this pin.

SSTT2 (Pin 22): Soft-Start, Tracking, Temperature Monitor Input for Buck Regulator 2. An internal 4µA current into an external capacitor on the soft-start pin programs the output voltage ramp rate for during start-up. When SSTT2 is below 0.5V, the FB2 pin voltage will track the SSTT2 pin voltage. When SSTT2 is above 0.5V, the tracking function is disabled, the internal reference resumes control of the error amplifier and the SSTT2 pin servos to a voltage proportional to junction temperature. For a clean recovery from an output short circuit condition, the SSTT2 pin is pulled down to approximately 100mV above the V_{FB} voltage and a new soft-start cycle is initiated. During shutdown and fault conditions, the SSTT2 pin is pulled to ground. Short the SSTT2 pin to AV_{IN} to use an internally set default soft-start time of 1ms (typical).

BLOCK DIAGRAM



OPERATION

Dual Buck Switching Regulators

The LTC3312SA is a 5V dual 6A monolithic, constant frequency, peak current mode step-down DC/DC converter. The synchronous buck switching regulators are internally compensated and require only external feedback resistors to set the output voltage.

An internal oscillator, with frequency set using a resistor on the RT pin or synchronized to an external clock, turns on the internal top power switch at the start of each clock cycle, (the clock's rising edge for Buck 1). Current in the inductor then increases until the top switch current comparator trips and turns off the top power switch. The peak inductor current at which the top switch turns off is controlled by an internal V_C voltage. The error amplifier regulates V_C by comparing the voltage on the FB pin with an internal 500mV reference. When the load current increases it causes a reduction in the feedback voltage relative to the reference leading the error amplifier to raise the V_C voltage until the average inductor current matches the new load current. When the top power switch turns off, the synchronous power switch turns on and ramps down the inductor current for the remainder of the clock cycle or, if in pulse-skipping or Burst Mode operation, until the inductor current falls to zero. If overload conditions result in excessive current flowing through the bottom switch, the next clock cycle will be skipped until the switch current returns to a safe level. The top switches of the two buck regulators are turned on 180 degrees out of phase to reduce input current ripple.

Each buck switching regulator has its own SW, FB, SSTT, PGOOD, and EN pins. The enable pins have precision 400mV thresholds which may be used to provide event-based power-up sequencing by connecting the enable pin to the output of another buck through a resistor divider. If the EN pin of a buck is low, that buck is in shutdown and in a low quiescent current state. If both EN pins are low, both bucks are in shutdown, the SW pins are high impedance, and the quiescent current of the LTC3312SA is 1.4µA (typical). If either EN pin is above the enable threshold of 400mV, its respective buck is enabled.

Both buck regulators have forward and reverse current limiting, short-circuit protection, output overvoltage protection, and soft-start to limit inrush current during start-up or recovery from a short-circuit.

2-Phase, Single Output Operation

The LTC3312SA is easily configured as a single output, 2-phase, 12A buck regulator by connecting the FB2 and SSTT2 pins to AV_{IN}, and connecting the EN2 pin to AGND. The PGOOD2 pin can be floated or shorted to ground. The EN1 pin will control the enable for both power stages, and the PGOOD1 pin functions as the power good indicator.

The part detects that FB2 is connected high and uses the output of the error amplifier (V_C) for Buck 1 to control the peak inductor current for both buck power stages. The top switches of the two phases are turned on 180 degrees out of phase to reduce input current ripple. The difference between peak inductor currents of the two phases are determined by internal matching and will typically be within 10% of each other at high currents.

The equations used to determine the inductor value for a single-phase 6A buck are also used to select the inductors for the dual-phase 12A circuit (see Applications Information section for inductor selection). The total capacitance on the 2-phase output should be double what is calculated for a single phase 6A buck (see Applications Information section for output capacitor selection).

When waking up from sleep in Burst Mode operation, the top switches of the two phases are turned on initially without a delay, to improve the transient response coming out of sleep. The 180-degree phase difference will start on the subsequent turn-on after exiting sleep.

Input Supply

The AV_{IN} pin is a noise-filtered version of PV_{IN} used to bias the internal bandgap reference and buck control circuits. A 1µF external filter capacitor should be connected from AV_{IN} to AGND, and no current should be drawn by external circuits. AV_{IN} connects to the PV_{IN1} and PV_{IN2} pins through internal 20Ω filter resistors.

OPERATION

PV_{IN1} and PV_{IN2} are not connected internally and should be externally shorted to a single input supply. Each PV_{IN} pin should have its own input bypass capacitor to PGND.

Mode Selection

The buck switching regulators operate in three different modes set by the MODE/SYNC pin: pulse-skipping mode (when the MODE/SYNC pin is set low), forced continuous mode (when the MODE/SYNC pin is floating), and Burst Mode (when the MODE/SYNC pin is set high). The MODE/SYNC pin sets the operating mode for both buck switching regulators.

In pulse-skipping mode, the oscillator operates continuously, and positive SW transitions are aligned to the clock. Negative inductor current is disallowed, and switch pulses are skipped for light loads to regulate the output voltage.

In forced continuous mode, the oscillator operates continuously. The top switch turns on every cycle and regulation is maintained by allowing the inductor current to reverse at light load. This mode allows the buck to run at a fixed frequency with minimal output ripple. In forced continuous mode, if the inductor current reaches 4A (typical) into the SW pin, the bottom switch will turn off for the remainder of the cycle to limit the current.

In Burst Mode operation at light loads, the output capacitor is charged to a voltage slightly higher than its regulation point. The regulator then goes into a sleep state, during which time the output capacitor provides the load current. In sleep, most of the regulator's circuitry is powered down, helping conserve input power. When the output voltage drops below its programmed value, the circuitry is powered on and another burst cycle begins. The sleep time decreases as load current increases. In Burst Mode operation, the regulator will burst at light loads whereas at higher loads it will operate in constant frequency PWM mode.

Synchronizing the Oscillator to an External Clock

The LTC3312SA's internal oscillator is synchronized through an internal PLL circuit to an external frequency by applying a square wave clock signal to the MODE/SYNC pin. During synchronization, the Buck 1 top power switch turn-on is locked to the rising edge of the external frequency source. The Buck 2 top switch turn-on will be 180 degrees out of phase with respect to Buck 1. While synchronizing, the buck switching regulators operate in forced continuous mode. The slope compensation is automatically adapted to the external clock frequency. The synchronization frequency range is 1MHz to 3MHz.

After detecting an external clock on the first rising edge of the MODE/SYNC pin, the internal PLL gradually adjusts its operating frequency to match the frequency and phase of the signal on the MODE/SYNC pin. When the external clock is removed, the LTC3312SA will detect the absence of the external clock within approximately 10µs. During this time, the PLL will continue to provide clock cycles. Once the external clock removal has been detected, the oscillator will gradually adjust its operating frequency to the one programmed by the RT pin.

Output Power Good

Both buck switching regulators have an external open-drain PGOOD pin, that operates independently of the other. When a buck output voltage is within the –2/+10% (typical) window of the nominal regulation voltage, the output is considered good. The corresponding open-drain PGOOD pin goes high impedance and is typically pulled high with an external resistor. Otherwise, an internal pull-down device will pull the corresponding PGOOD pin low. Each PGOOD pin is also pulled low during the following fault conditions: the corresponding buck EN pin is low, V_{IN} is too low, or thermal shutdown. To filter noise and short duration output voltage transients, the lower thresholds have a hysteresis of 1.1% (typical), the upper thresholds have a hysteresis of 2.2% (typical), and transitions of the PGOOD pins have a built-in time delay, typically 100µs.

Output Overvoltage Protection

If there is an output overvoltage event, which occurs when the FB pin voltage is greater than 110% of nominal, the buck regulator top power switch will be turned off. If the output remains out of regulation for more than 100µs, the PGOOD pin will be pulled low.

OPERATION

An output overvoltage event should not happen under normal operating conditions.

Overtemperature Protection

To prevent thermal damage to the LTC3312SA, the device incorporates an overtemperature (OT) function. If the die temperature reaches 165°C (typical, not tested), both buck switching regulators will be shut down and remain in shutdown until the die temperature falls to 160°C (typical, not tested).

Soft-Start/Tracking/Temperature Monitor

The soft-start tracking function facilitates supply sequencing, limits V_{IN} inrush current, and reduces start-up output overshoot. Each buck regulator has an SSTT pin, which sources a 4µA current when that buck is enabled. When the SSTT pin voltage is low, it replaces the 500mV reference normally used for regulating the FB voltage. A capacitor on the SSTT pin to ground can be used to set the soft-start ramp time for each buck regulator. When soft-starting is completed, each SSTT pin parks itself at a voltage representative of the LTC3312SA die junction temperature.

An alternative is to connect an SSTT pin to AV_{IN}, which selects an internally-set 1ms default soft-start time for that buck regulator.

An active pull-down circuit is connected to either the SSTT pin, or to the internal soft-start node if SSTT is connected high. This is used to discharge it in the case of fault conditions. The soft-start ramp will restart when the fault is cleared. Fault conditions that clear the soft-start voltage ramp are the EN pin transitioning low, V_{IN} voltage falling too low, or thermal shutdown.

Dropout Operation

As the input supply voltage approaches the output voltage, the duty-cycle increases until SW is low for a minimum time of 30ns (typical). Further reduction of the supply voltage forces the main switch to remain on for more than one cycle, allowing the duty-cycle to increase despite the internally set minimum SW low-time. As the input drops further, the main switch stays on for more cycles, until it reaches the maximum allowed 16 cycles. At least one minimum low-time is forced every 16 cycles in dropout, limiting the maximum duty-cycle to 99% (typical).

Deep in dropout, the output voltage will be approximately determined by 0.99 times the input voltage, minus the voltage drops across the internal high-side MOSFET and the inductor.

Low Supply Operation

The LTC3312SA is designed to operate down to an input supply voltage of 2.25V. One important consideration at low input supply voltages is that the $R_{DS(ON)}$ of the internal power switches increases. Calculate the worst case LTC3312SA power dissipation and die junction temperature at the lowest input voltages.

Output Short-Circuit Protection and Recovery

The peak inductor current level, at which the current comparator shuts off the top power switch, is controlled by the internal V_C voltage. If the output current increases, the error amplifier raises V_C until the average inductor current matches the load current. The LTC3312SA clamps the maximum V_C voltage, thereby limiting the peak inductor current.

When the output is shorted to ground, the inductor current decays very slowly when the bottom power switch is on, because the voltage across the inductor is low. To keep the inductor current in control, a secondary limit is imposed on the valley of the inductor current. If the inductor current measured through the bottom power switch is greater than I_{LIMN} at the end of a cycle, the top power switch will be held off. Subsequent switching cycles will be skipped until the inductor current is reduced below I_{LIMN}.

Recovery from an output short circuit may involve a soft-start cycle if V_{FB} falls more than approximately 100mV below regulation. During such a recovery, V_{FB} will quickly charge up by that ~100mV and then follow the soft-start ramp until regulation is reached.

APPLICATIONS INFORMATION

Output Voltage and Feedback Network

The output voltage of the buck switching regulators is programmed by a resistor divider between the output and the FB pin. Choose the resistor values according to Equation 1.

$$R_A = R_B\left(\frac{V_{OUT}}{500mV} - 1\right) \quad (1)$$

as shown in Figure 1:

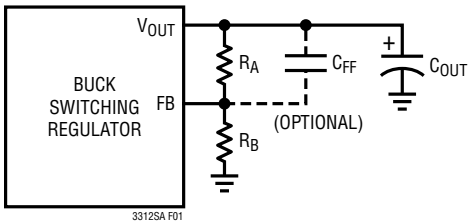


Figure 1. Feedback Components

Typical values for R_B range from 40k to 400k. 0.1% resistors are recommended to maintain output voltage accuracy. The buck regulator transient response may improve with an optional phase lead capacitor C_{FF} that helps cancel the pole created by the feedback resistors and the input capacitance of the FB pin. Experimentation with capacitor values between 2pF and 40pF may improve transient response. The values used in the typical application circuits are a good starting point.

Operating Frequency Selection and Trade-Offs

Selection of the operating frequency is a trade-off between efficiency, component size, transient response and input voltage range.

The advantage of high frequency operation is that smaller inductor and capacitor values may be used. Higher switching frequencies allow for higher control loop bandwidth and, therefore, faster transient response. The disadvantages of higher switching frequencies are lower efficiency, because of increased switching losses, and a smaller input voltage range, because of minimum switch on-time limitations.

The minimum on-time of the buck regulators imposes a minimum operating duty-cycle. The highest switching frequency ($f_{SW(MAX)}$) for a given application can be calculated with Equation 2.

$$f_{SW(MAX)} = \frac{V_{OUT}}{t_{ON(MIN)} \bullet PV_{IN(MAX)}} \quad (2)$$

where $PV_{IN(MAX)}$ is the maximum input voltage, V_{OUT} is the output voltage, and $t_{ON(MIN)}$ is the minimum top switch on-time. This equation shows that a slower switching frequency might be necessary to accommodate a high V_{IN}/V_{OUT} ratio.

The LTC3312SA is capable of a maximum duty-cycle of 98%. Therefore, the V_{IN}-to-V_{OUT} dropout is limited by 0.98 times the input supply, the $R_{DS(ON)}$ of the top switch, the inductor DCR, and the load current.

Setting the Switching Frequency

The LTC3312SA uses a constant frequency peak current mode control architecture. There are three methods to set the switching frequency.

The first method, connecting the RT pin to V_{IN}, sets the switching frequency to the internal default with a nominal value of 2MHz.

The second method is with a resistor (R_T) tied from the RT pin to ground. The frequency can be programmed from 1MHz to 3MHz. Table 1 and Equation 3 show the necessary R_T value for a desired switching frequency:

$$R_T = \frac{73.4}{f_{SW}} - 1.9 \quad (3)$$

where R_T is in kΩ and f_{SW} is the desired switching frequency in MHz, ranging from 1MHz to 3MHz.

APPLICATIONS INFORMATION

Table 1. R_T Value vs Switching Frequency

f_{SW} (MHz)	R_T (kΩ)
1.0	71.5
1.2	59.0
1.4	51.1
1.6	44.2
1.8	39.2
2.0	34.8
2.2	31.6
2.4	28.7
2.6	26.1
2.8	24.3
3.0	22.6

The third method to set the switching frequency is by synchronizing the internal PLL circuit to an external square wave clock applied to the MODE/SYNC pin. The synchronization frequency range is 1MHz to 3MHz. The square wave amplitude should have valleys that are below 0.4V and peaks above 1.2V. High and low pulse widths should both be at least 40ns.

Inductor Selection and Maximum Output Current

Considerations in choosing an inductor are inductance, RMS current rating, saturation current rating, DCR, and core loss.

Select the inductor value based on Equation 4 and Equation 5.

$$L \approx \frac{V_{OUT}}{1.8A \bullet f_{SW}} \bullet \left(1 - \frac{V_{OUT}}{PV_{IN(MAX)}}\right) \text{ for } \frac{V_{OUT}}{PV_{IN(MAX)}} \leq 0.5 \quad (4)$$

$$L \approx \frac{0.25 \bullet PV_{IN(MAX)}}{1.8A \bullet f_{SW}} \text{ for } \frac{V_{OUT}}{PV_{IN(MAX)}} > 0.5 \quad (5)$$

where f_{SW} is the switching frequency and $PV_{IN(MAX)}$ is the maximum input voltage.

To avoid overheating of the inductor choose an inductor with an RMS current rating that is greater than the maximum expected output load of the application. Overload and short circuit conditions may need to be taken into consideration.

In addition, ensure that the saturation current rating (typically labeled I_{SAT}) of the inductor is higher than the maximum expected load current plus half the inductor ripple current (Equation 6).

$$I_{SAT} > I_{LOAD(MAX)} + \frac{1}{2}\Delta I_L \quad (6)$$

where $I_{LOAD(MAX)}$ is the maximum output load current for a given application and ΔI_L is the inductor ripple current calculated by Equation 7.

$$\Delta I_L = \frac{V_{OUT}}{L \bullet f_{SW}} \bullet \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \quad (7)$$

A more conservative choice would be to use an inductor with an I_{SAT} rating higher than the maximum current limit of the LTC3312SA.

To keep the efficiency high, choose an inductor with the lowest series resistance (DCR). The core material should be intended for high frequency applications. Table 2 shows recommended inductors from several manufacturers.

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Table 2. Recommended Inductors with Typical Specifications

INDUCTANCE (nH)	I_{TEMP} (A)*	I_{SAT} (A)	DCR (mΩ)	W × L × H (mm)	MANUFACTURER	MANUFACTURER'S PART NUMBER
220 to 560	9.3 to 5.1	9.3 to 6.7	9.5 to 18.7	3.0 × 3.0 × 1.2	Vishay	IHLP-1212AB-11
330	5.2	6.8	16	2.7 × 2.2 × 1.0	Sumida	252010CDMCCDS-R33MC
330, 470	5.1, 4.9	7.6, 6.7	19, 23 (Max)	2.5 × 2.0 × 1.2	Murata	DFE252012F
330	4.8	6.8	16	2.5 × 2.0 × 1.0	Murata	DFE252010F-R33M
330	5.5	7.3	16	2.5 × 2.0 × 1.0	Cyntec	HMLQ25201T-R33MSR
330	5.5	8.3	14	3.0 × 3.0 × 2.0	Wurth Elektronik	744383360033
250	5.5	12	10	3.2 × 2.5 × 1.5	Wurth Elektronik	74479290125
240	6	9.5	18	2.5 × 2.0 × 1.0	NIC	NPIM20LP
240	6.5	7.5	15	2.0 × 1.6 × 1.0	NIC	NPIM26LP
240	5.2	6.5	19	2.2 ×1.8×1.0	Sumida	201610CDMCCDS-R24MC
240	5	6.6	19 (Max)	2.0 × 1.6 × 1.2	Murata	DFE201612E-R24M
240	4.7	6.3	20 (Max)	2.0 × 1.6 × 1.0	Murata	DFE201610E-R24M
220	5.9	7.0	9.4	2.5 × 2.0 × 1.0	Cyntec	HMLB25201T-R22MSR-01
220	7.4	7.1	8.4	2.5 × 2.0 × 1.2	Vishay	IHHP1008ABERR22M01
220	8.0	7.0	13 (Max)	2.5 × 2.0 × 1.2	XFRMS	XFHCL43LT-R22M
72 to 560	23.6 to 8.1	16.0 to 6.5	2.85 to 21.5	3.2 × 3.5 × 1.5	Coilcraft	XEL3515
110	5.5	8.8	12 (Max)	2.0 × 1.2 × 1.0	Murata	DFE201210S-R11M
100	11.13	7.38	7.31	3.3 × 3.3 × 1.0	Vishay	IHLP1212AZEER10M5A
100 to 470	5.6 to 12	5.8 to 10	4 to 19	2.5 × 2.0 × 1.2	TDK	TFM252012ALMA

*Strongly depends on the PCB thermal properties

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Input Capacitors

Bypass the input of the LTC3312SA with at least two ceramic capacitors close to the part, one near each PV_{IN} pin. Connect the ground of each capacitor to a wide PCB trace on the top layer of the PCB that connects pins 9 and 10 with the exposed pad. These capacitors should be 0603 or 0805 in size. Smaller 0201 capacitors can also be placed as close as possible from PV_{IN1} to PGND, and from PV_{IN2} to PGND to reduce input noise with minimal increase in application footprint. See the PCB Layout Considerations section for more detail. X7R or X5R capacitors are recommended for best performance across temperature and input voltage variations (see Table 3). Note that larger input capacitance is required when a lower switching frequency is used. If the input power source has high impedance, or there is significant inductance due to long wires or cables, additional bulk capacitance may be necessary. This can be provided with an electrolytic capacitor.

A ceramic input capacitor combined with trace or cable inductance forms a high quality (underdamped) tank circuit. If the LTC3312SA circuit is plugged into a live supply, the input voltage can ring to twice its nominal value, possibly exceeding the LTC3312SA's voltage rating. This situation is easily avoided (see Application Note AN88).

Table 3. Ceramic Capacitor Manufacturers

VENDOR	URL
AVX	www.avxcorp.com
Murata	www.murata.com
TDK	www.tdk.com
Taiyo Yuden	www.t-yuden.com
Samsung	www.samsungsem.com
Wurth Elektronik	www.we-online.com

Output Capacitor, Output Ripple and Transient Response

The output capacitor has two essential functions. Along with the inductor, it filters the square wave generated by the LTC3312SA to produce the DC output. In this role it determines the output ripple; thus, low impedance at the switching frequency is important. The second function is to store energy in order to satisfy transient loads and stabilize the LTC3312SA's control loop.

The LTC3312SA is internally compensated and has been designed to operate at a high bandwidth for fast transient response capability. The selection of C_{OUT} will affect the bandwidth of the system, but the transient response is also affected by V_{OUT}, V_{IN}, f_{SW}, and other factors. A good place to start is with the output capacitor value given by Equation 8.

$$C_{OUT} = 20 \bullet \frac{I_{MAX}}{f_{SW}} \sqrt{\frac{0.5}{V_{OUT}}} \quad (8)$$

where C_{OUT} is the recommended output capacitor value in µF, f_{SW} is the switching frequency in MHz, I_{MAX} = 6A per phase is the rated output current in Amps, and V_{OUT} is in volts.

A lower value of output capacitor can be used to save space and cost, but transient performance will suffer and loop stability must be verified.

Ceramic capacitors have very low equivalent series resistance (ESR) and provide the best output ripple and transient performance. Use X5R or X7R ceramic capacitors (see Table 3). Even better output ripple and transient performance can be achieved by using low-ESL reverse geometry or three-terminal ceramic capacitors.

During a load step, the output capacitor must instantaneously supply the current to support the load until the feedback loop increases the switch current enough to support the load. The time required for the feedback loop to respond is dependent on the compensation components and the output capacitor size. Typically, 3 to 4 cycles are required to respond to a load step, but only in the first cycle does the output drop linearly. Although affected by V_{OUT}, V_{IN}, f_{SW}, $t_{ON(MIN)}$, the equivalent series inductance (ESL) of the output capacitor, and other factors, the output droop, V_{DROOP}, is usually about 3 times the linear drop of the first cycle (Equation 9).

$$V_{DROOP} = \frac{3 \bullet \Delta I_{OUT}}{C_{OUT} \bullet f_{SW}} \quad (9)$$

Transient performance and control loop stability can be improved with a higher C_{OUT} and/or the addition of a

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feedforward capacitor C_{FF} placed between V_{OUT} and FB. Capacitor C_{FF} provides phase lead compensation by creating a high frequency zero which improves the phase margin and the high frequency response. The values used in the typical application circuits are good starting points. LTpowerCAD® is a useful tool to help optimize C_{FF} and C_{OUT} for a desired transient performance.

Applying a load transient and monitoring the response of the system or using a network analyzer to measure the actual loop response are two ways to experimentally verify transient performance and control loop stability, and to optimize C_{FF} and C_{OUT}.

When using the load transient response method to stabilize the control loop, apply an output current pulse of 20% to 100% of full load current having a very fast rise time. This will produce a transient on the output voltage. Monitor V_{OUT} for overshoot or ringing that would indicate a stability problem (see Application Note AN149).

Output Voltage Sensing

The LTC3312SA's AGND pin is the ground reference for the internal analog circuitry, including the bandgap voltage reference. For the single output, 2-phase application, load regulation can be improved by connecting the AGND pin to the negative terminal of the output capacitor (C_{OUT}) at the load. Any drop in the high current power ground return path will be compensated. All of the signal components, such as the FB resistor dividers and the R_T resistor, should be referenced to the AGND node. AGND carries very little current and, therefore, can be a minimal size trace.

For dual-buck applications, connect the FB resistor dividers, the R_T resistor ground, and the AV_{IN} capacitor ground to the AGND pin close to the part. Connect AGND, using a via, to a low resistance ground plane that minimizes any voltage drops between AGND and the negative terminals of the buck output capacitors.

Enable Threshold Programming

The LTC3312SA has precision threshold enable pins for each buck regulator to enable or disable each buck. When both are forced low, the device enters into a low current shutdown mode.

The rising threshold of both EN comparators is 400mV, with 50mV of hysteresis. The EN pins can be tied to AV_{IN} if the shutdown feature is not used. Adding a resistor divider from PV_{IN} to an EN pin programs the LTC3312SA to regulate that output only when PV_{IN} is above a desired voltage. Typically, this threshold, $V_{IN(EN)}$, is used in situations where the input supply is current limited or has a relatively high source resistance. A switching regulator draws near constant power from its input source, so source current increases as source voltage drops. This looks like a negative resistance load to the source and can cause the source to current limit or latch low under low source voltage conditions. The $V_{IN(EN)}$ threshold prevents the regulator from operating at source voltages where problems may occur. Referring to Figure 2, this threshold can be adjusted by setting the values R1 and R2 such that they satisfy Equation 10.

$$PV_{IN(EN)} = \left(\frac{R1}{R2} + 1\right) \bullet 400mV \quad (10)$$

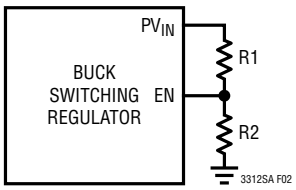


Figure 2. EN Divider

The buck regulator will remain off until PV_{IN} is above $PV_{IN(EN)}$. The buck regulator will remain enabled until PV_{IN} falls to 0.875 • $PV_{IN(EN)}$ and EN is 350mV.

Alternatively, a resistor divider from the output of one buck to the EN pin of the second buck provides event-based power-up sequencing, as the first buck reaching regulation enables the second buck. Replace $PV_{IN(EN)}$ in Equation 10 with the desired output voltage of the first buck, (e.g., 90% of the regulated value), at which the second buck is enabled.

Output Voltage Tracking and Soft-Start

Each buck regulator has an independent SSTT pin. An internal 4µA current pulls up each SSTT pin when that buck is enabled, allowing an external capacitor from

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SSTT to AGND to set the soft-start time, calculated using Equation 11.

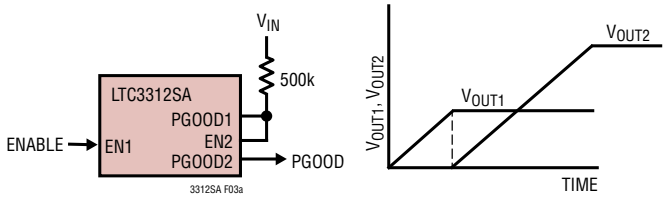
$$t_{SS} = C_{SS} \bullet 500mV/4\mu A \quad (11)$$

From 0V to 0.5V, the SSTT voltage will override the internal 0.5V reference input to the error amplifier, thus regulating the FB pin voltage to that of the SSTT pin. When SSTT is above 0.5V, tracking is disabled, and the feedback voltage will regulate to the internal reference voltage.

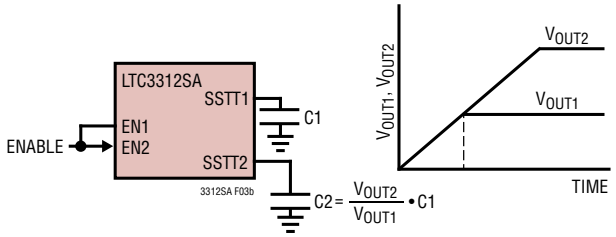
An alternative is to connect an SSTT pin to AV_{IN}, which selects an internally-set 1ms default soft-start time for that buck regulator.

An active pull-down circuit is connected to either the SSTT pin, or to the internal soft-start node if SSTT is connected high. This is used to discharge it in the case of fault conditions. The soft-start ramp will restart when the fault is cleared. Fault conditions that clear the soft-start voltage ramp are the EN pin transitioning low, V_{IN} voltage falling too low, or thermal shutdown.

Figure 2 (above) and Figure 3 (below) show examples for some of the ways to control power-up sequencing using the EN, SSTT and PGOOD pins.



(a) Sequential Voltage Power-Up



(b) Tracking Voltage Power-Up

Figure 3. Power-Up Sequencing

Temperature Monitor

After the soft-start cycle has completed and the output power good flag is high, the SSTT pin voltages are set to a PTAT (proportional to absolute temperature) voltage. The following procedure can be used to accurately measure the die junction temperature:

1. Measure the ambient temperature (T_A), and one of the SSTT pin voltages (V_{SSTT}), when both buck regulators are unloaded. Calculate an accurate slope for the temperature sensing circuit using Equation 12.

$$\text{Slope (V/°K)} = \frac{V_{SSTT}}{T_A + 273} \quad (12)$$

2. The calibrated slope can then be used to accurately determine the die temperature for any load or ambient conditions using Equation 13.

$$T_{JDIE}(°C) = \frac{V_{SSTT}}{\text{Slope}} - 273 \quad (13)$$

When an output voltage goes out of regulation or is disabled, and the PGOOD pin is pulled low, the corresponding SSTT pin no longer reports the temperature.

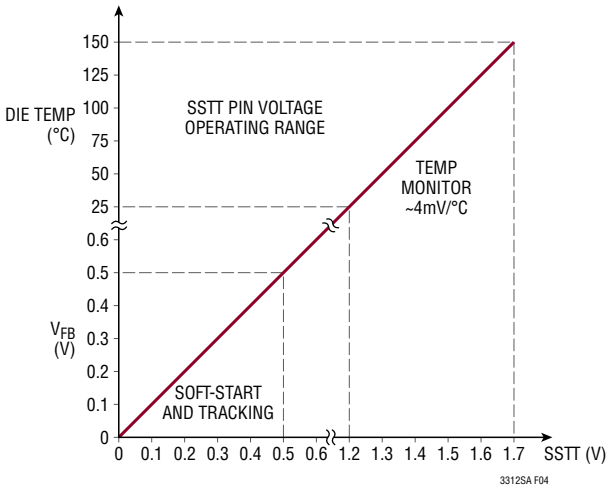


Figure 4. Soft-Start and Temperature Monitor Operation

PCB Layout Considerations

The LTC3312SA is a high performance IC designed for high efficiency and fast transient response. For optimal results carefully consider the layout of the PCB board

APPLICATIONS INFORMATION

and follow the recommendations below to ensure proper operation. See Figure 5 for a recommended PCB layout.

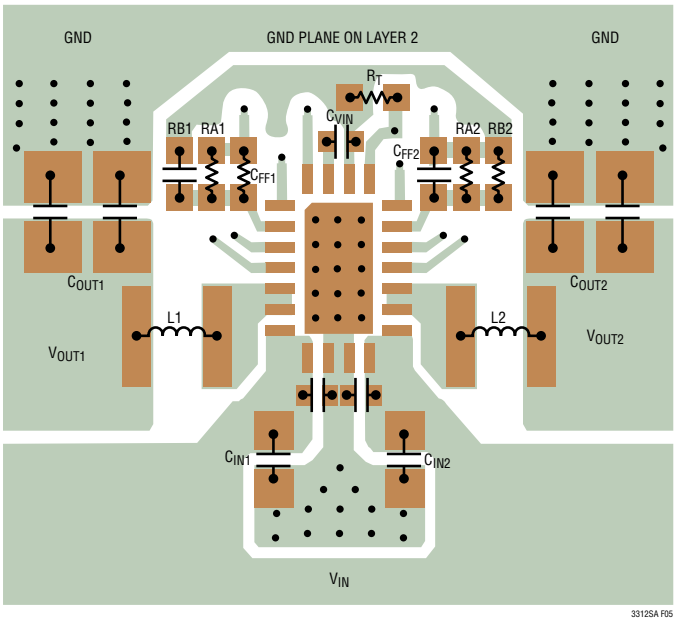


Figure 5. Recommended PCB Layout

1. Connect the exposed pad of the package (Pin 23) directly to a large, unbroken ground plane under the application circuit on the layer closest to the surface layer to minimize thermal and electrical impedance. Additionally, short the exposed pad to pins 9 and 10 on the top layer. See the Analog Devices Application Note, Application Notes for Thermally Enhanced Leaded Plastic Packages for the proper size and layout of the thermal vias and solder stencils.

2. The PV_{IN1} (Pins 7, 8) and PV_{IN2} (Pins 11, 12) input supply pins should have local decoupling capacitors with the ground side of the capacitors connected on the top layer to the ground plane close to pin 9 and pin 10. These capacitors provide the AC current to the internal power MOSFETs and their drivers. Large, switched currents flow in these capacitors and it is important to minimize inductance from these capacitors by choosing a small case size, such as 0603, and placing them close to the pins on the top side of the board. To further minimize inductance and input noise, smaller 0201 capacitors can be placed in parallel, also as close as possible to the pins, from PV_{IN1} to PGND and from PV_{IN2} to PGND.

3. Place both regulator inductors on the same side of the board as the LTC3312SA. The switching power traces connecting SW1 and SW2 to their inductors should be minimized to reduce radiated EMI and parasitic coupling. Due to the large voltage swing on the switching nodes, high impedance sensitive nodes, such as the feedback nodes, should be kept far away or shielded from SW1 (Pins 5, 6) and SW2 (Pins 13, 14). Minimize the trace lengths from the inductors to their output capacitors.

4. Connect the ground side of any FB, R_T, and SSTT components to AGND (Pin 20). Connect a 1µF decoupling capacitor from AV_{IN} (Pin 21) to AGND, close to the pins. For all layouts, only connect AGND to the rest of the PCB ground plane in one location, to prevent transient currents in the ground plane from also flowing through the AGND trace, which would cause voltage noise between AGND referenced circuits.

   For dual-buck applications, connect the AGND pin to the ground plane with a single via, close to the AGND pin. Use an unbroken low resistance ground plane to minimize any voltage drops between AGND and the negative terminals of the output capacitors.

   For 2-phase, single output designs, optionally connect the AGND pin to the negative terminal of the output capacitor (C_{OUT}) at the load. This will reduce any load regulation caused by voltage drops between the ground at the load and the LTC3312SA voltage reference ground. The AGND node carries very little current and, therefore, can be a minimal size trace. The ground side of any FB, R_T, and SSTT components, and the AV_{IN} capacitor ground should connect to the AGND node.

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High Temperature Considerations

Care should be taken in the layout of the PCB to ensure good heat sinking of the LTC3312SA. Connect the exposed pad on the bottom of the package to a large unbroken ground plane under the application circuit on the layer closest to the surface layer. Place many vias to minimize thermal and electrical impedance. Solder the PGND pins directly to a ground plane on the top layer. Connect the top layer ground plane to ground plane(s) on lower levels with many thermal vias. These layers will spread heat dissipated by the LTC3312SA. Figure 6 is a simplified thermal representation of a thermally enhanced LQFN package with exposed pad, with the silicon die and thermal metrics identified. The current source represents power loss P_D on the die; node voltages represent temperatures; electrical impedances represent conductive thermal impedances $\theta_{JCBOTTOM}$, θ_{JCTOP}, θ_{VIA}, θ_{CB}, and convective thermal impedances θ_{BA} and θ_{CA}. The junction temperature, T_J, is calculated from the ambient temperature, T_A, as given by Equation 14.

$$T_J = T_A + P_D \bullet \theta_{JA} \quad (14)$$

where, neglecting the $\theta_{JCTOP} + \theta_{CA}$ path.

$$\theta_{JA} \approx \theta_{JCBOTTOM} + \left(\frac{\theta_{CB}+\theta_{BA}}{2}\right) \| \left(\frac{\theta_{CB}+\theta_{BA}}{2}+\theta_{VIA}\right) \quad (15)$$

where $\theta_{JCBOTTOM}$ = 4.0°C/W. The value of θ_{JA} = 23°C/W reported in the Pin Configuration section corresponds to the demo board.

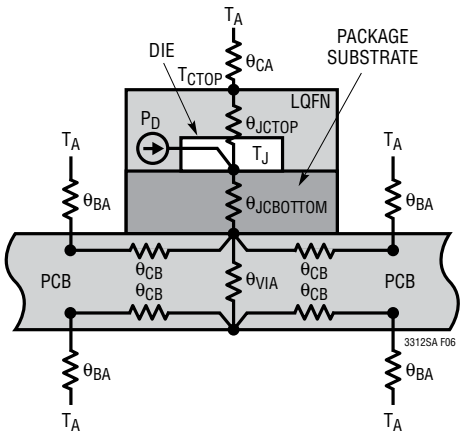
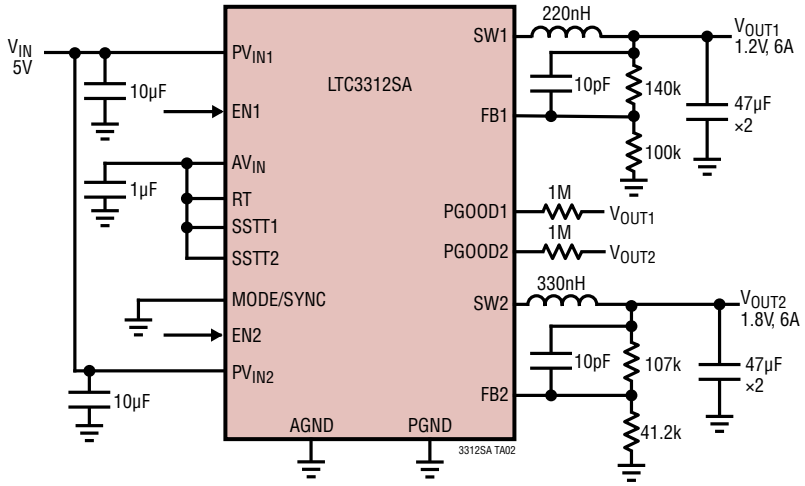


Figure 6. Multi-Layer PCB with Thermal Vias Acts as a Heat Sink

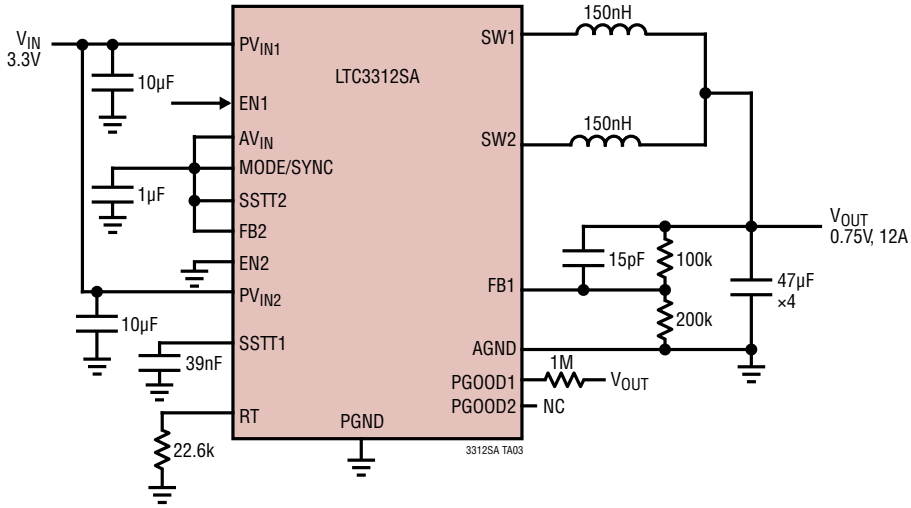
The low value of $\theta_{JCBOTTOM}$ means that θ_{JA} will be dominated by (θ_{CB} + θ_{BA}) and θ_{VIA}. Minimize θ_{VIA} by including a large number of low thermal resistance vias from the top layer ground plane to ground plane(s) on lower levels, close to the exposed paddle of the part. Minimize (θ_{CB} + θ_{BA}) by having more ground planes that are larger, uninterrupted, and higher copper-weight. See the Application Note, Application Notes for Thermally Enhanced Leaded Plastic Packages, for the proper size and layout of the thermal vias and solder stencils. The maximum load current should be derated as the ambient temperature approaches the maximum junction rating. Power dissipation within the LTC3312SA is estimated by calculating the total power loss from an efficiency measurement and subtracting the inductor loss.

TYPICAL APPLICATIONS

Dual 1.2V and 1.8V, 2MHz, 6A, V_{IN} = 5V, Pulse-Skipping Mode

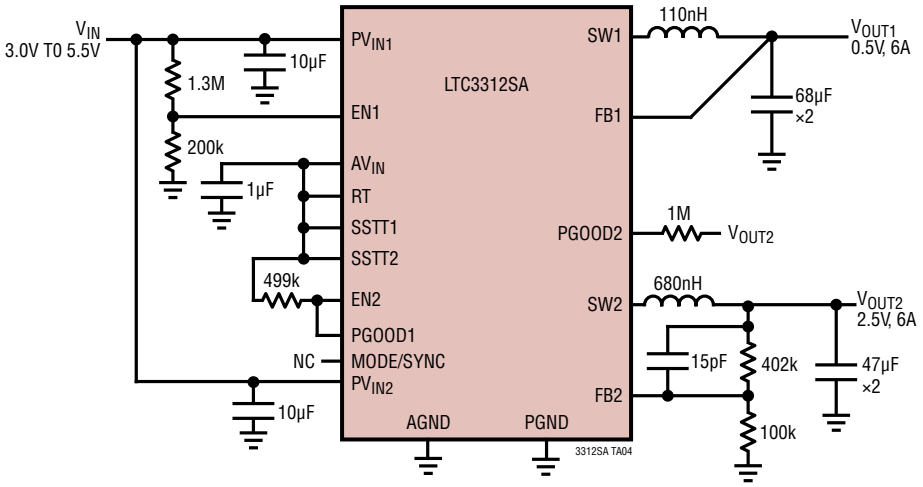


Single Output 2-Phase, 0.75V, 3MHz, 12A, V_{IN} = 3.3V, t_{SS} = 4.9ms, Burst Mode Operation

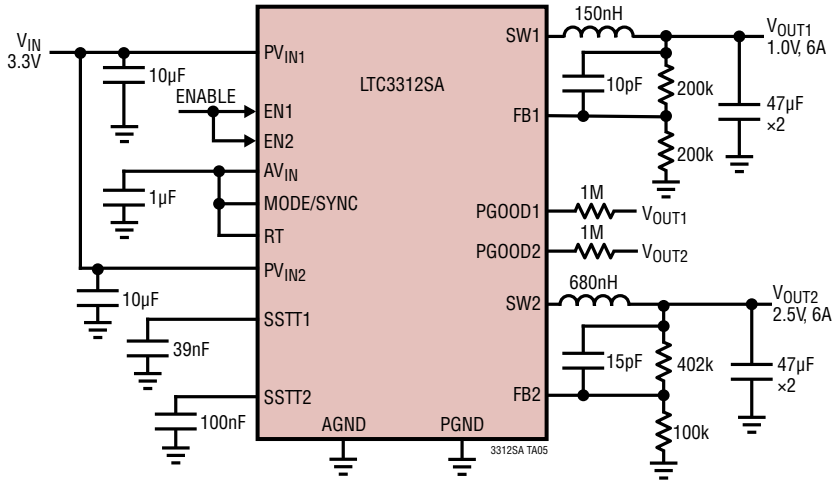


TYPICAL APPLICATIONS

Dual 0.5V and 2.5V, 2MHz, 6A, UVLO = 3.0V, Sequential Power-Up Sequencing (V_{OUT1} powers first), Forced Continuous Mode

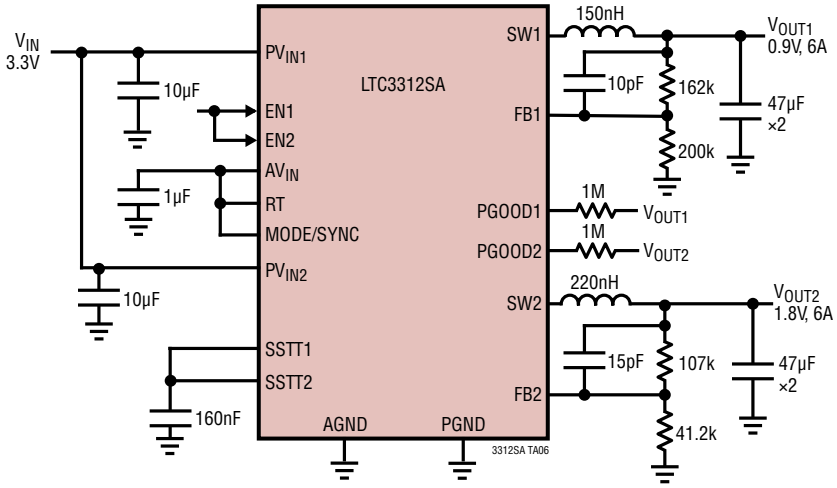


Dual 1.0V and 2.5V, 2MHz, 6A, V_{IN} = 3.3V, Voltage Tracking Power-Up Sequencing (with t_{SS1} = 4.9ms, t_{SS2} = 12.5ms), Burst Mode Operation

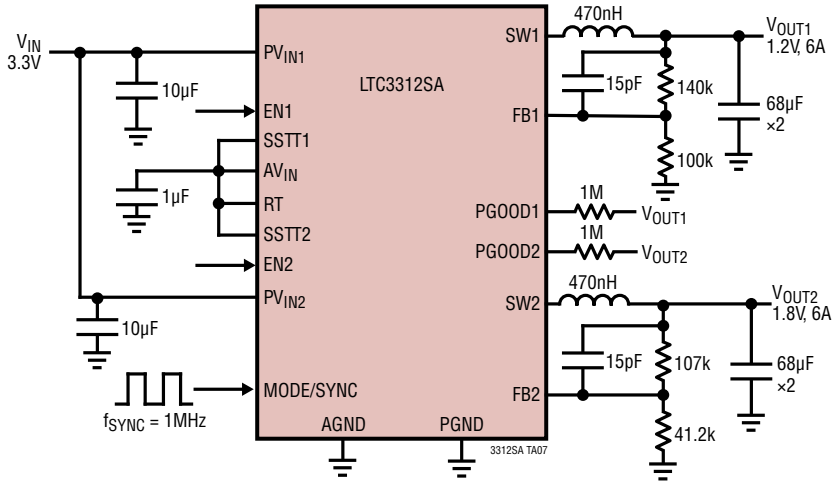


TYPICAL APPLICATIONS

Dual 0.9V and 1.8V, 2MHz, 6A, V_{IN} = 3.3V, Burst Mode Operation
Ratiometric Power-Up with t_{SS} = 10ms

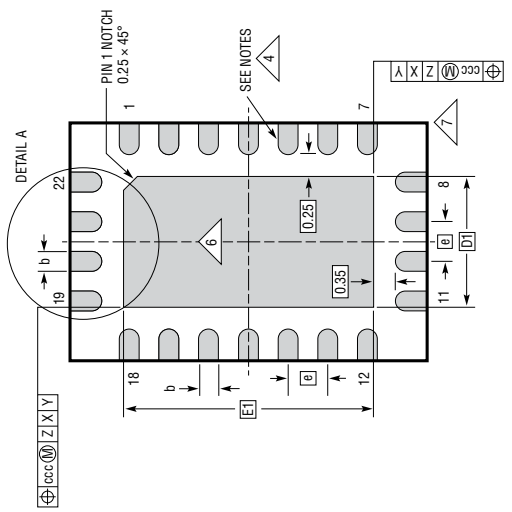


Dual 1.2V and 1.8V, 1MHz, 6A, V_{IN} = 3.3V, Syncing to 1MHz

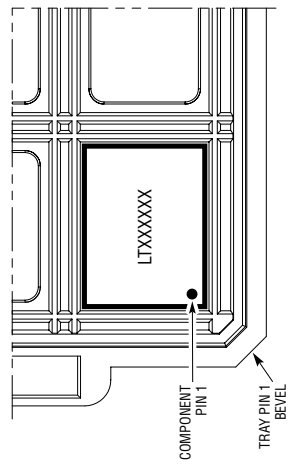


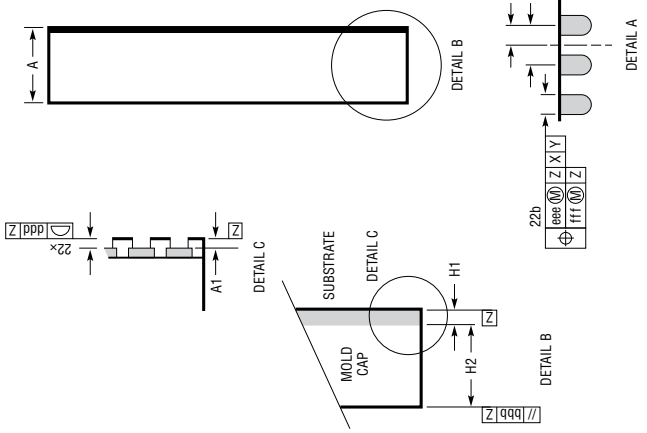
PACKAGE DESCRIPTION

LQFN Package
22-Lead (4mm × 3mm × 0.95mm)
(Reference LTC DWG # 05-08-7012 Rev Ø)

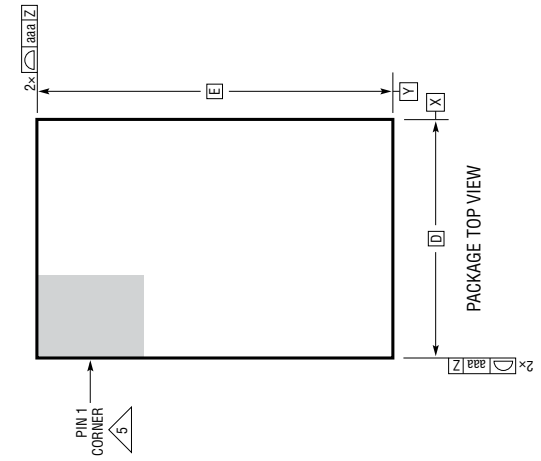


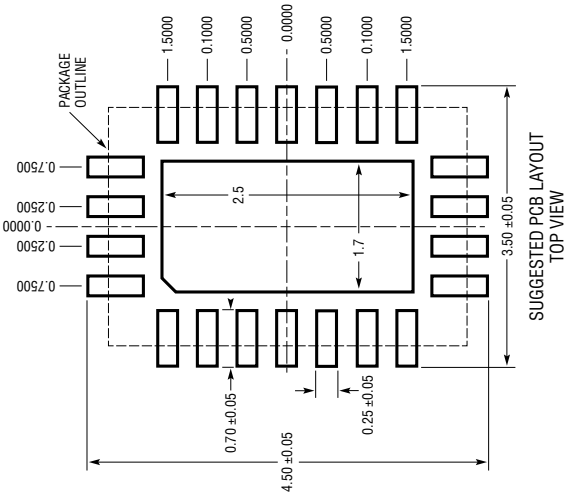
NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994
2. ALL DIMENSIONS ARE IN MILLIMETERS
3. PRIMARY DATUM -Z- IS SEATING PLANE
4. METAL FEATURES UNDER THE SOLDER MASK OPENING NOT SHOWN SO AS NOT TO OBSCURE THESE TERMINALS AND HEAT FEATURES
5. DETAILS OF PIN 1 IDENTIFIER ARE OPTIONAL, BUT MUST BE LOCATED WITHIN THE ZONE INDICATED. THE PIN 1 IDENTIFIER MAY BE EITHER A MOLD OR MARKED FEATURE
6. THE EXPOSED HEAT FEATURE MAY HAVE OPTIONAL CORNER RADII
7. CORNER SUPPORT PAD CHAMFER IS OPTIONAL





DIMENSIONS				
SYMBOL	MIN	NOM	MAX	NOTES
A	0.85	0.95	1.05	
A1			0.03	
L	0.30	0.40	0.50	
b	0.22	0.25	0.28	
D		3.00		
E		4.00		
D1		1.70		
E1		2.5		
e		0.50		
H1		0.25 REF		SUBSTRATE THK
H2		0.70 REF		MOLD CAP HT
aaa			0.10	
bbb			0.10	
ccc			0.10	
ddd			0.10	
eee			0.15	
fff			0.08	





Rev. B

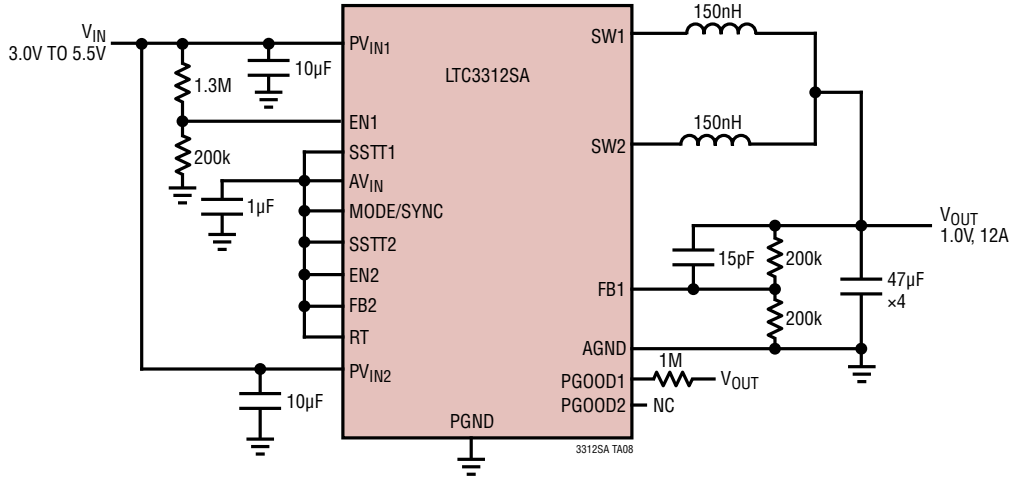
REVISION HISTORY

REV	DATE	DESCRIPTION	PAGE NUMBER
A	09/25	Updated Thermal Number	1
B	11/25	Added LTC3312SAAV#TRPBF and LTC3312SAJV#WTRPBF to Order Information	2

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TYPICAL APPLICATION

Single Output 2-Phase, 1.0V, 2MHz, 12A, UVLO = 3.0V, Burst Mode Operation



RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LTC3309A/ LTC3309B	5V, 6A Synchronous Step-Down Silent Switcher	Monolithic Synchronous Step-Down DC/DC Capable of Supplying 6A at Switching Frequencies Up to 3MHz/10MHz, Silent Switcher Architecture for Ultralow EMI Emissions, 2.25V to 5.5V Input Operating Range, 0.5V to V_{IN} Output Voltage Range with ±1% Accuracy, PGOOD Indication, R_T Programming, SYNC Input, 2mm × 2mm LQFN
LTC3315A/ LTC3315B	Dual 5V, 2A Synchronous Step-Down DC/DCs	Dual Monolithic Synchronous Step-Down Voltage Regulators Each Capable of Supplying 2A at Switching Frequencies Up to 3MHz/10MHz, 2.25V to 5.5V Input Operating Range, 0.5V to V_{IN} Output Voltage Range with ±1% Accuracy, PGOOD Indication, SYNC Input, 2mm × 2mm LQFN
LTC3310/ LTC3310S LTC3311/ LTC3311S	5V, 10A/12.5A Synchronous Step-Down Silent Switcher/Silent Switcher	Monolithic Synchronous Step-Down DC/DC Capable of Supplying 10A/12.5A at Switching Frequencies Up to 5MHz, Silent Switcher Architecture for Ultralow EMI Emissions, 2.25V to 5.5V Input Operating Range, 0.5V to V_{IN} Output Voltage Range with ±1% Accuracy, PGOOD Indication, R_T Programming, SYNC Input, Configurable for Paralleling Power Stages, 3mm × 3mm LQFN
LTC3308A/ LTC3308B	5V, 4A Synchronous Step-Down Silent Switcher	Monolithic Synchronous Step-Down DC/DC Capable of Supplying 4A at Switching Frequencies Up to 3MHz/10MHz, Silent Switcher Architecture for Ultralow EMI Emissions, 2.25V to 5.5V Input Operating Range, 0.5V to V_{IN} Output Voltage Range with ±1% Accuracy, PGOOD Indication, R_T Programming, SYNC Input, 2mm × 2mm LQFN
LTC3307A/ LTC3307B	5V, 3A Synchronous Step-Down Silent Switcher	Monolithic Synchronous Step-Down DC/DC Capable of Supplying 3A at Switching Frequencies Up to 3MHz/10MHz, Silent Switcher Architecture for Ultralow EMI Emissions, 2.25V to 5.5V Input Operating Range, 0.5V to V_{IN} Output Voltage Range with ±1% Accuracy, PGOOD Indication, R_T Programming, SYNC Input, 2mm × 2mm LQFN
LTC3616	5.5V, 6A, 4MHz, Synchronous Step-Down Regulator	95% Efficiency, V_{IN}: 2.25 to 5.5V, $V_{OUT(MIN)}$ = 0.8V, I_Q = 64µA, ISD < 1µA, 4mm × 4mm QFN-16 Package

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