Power Conditioner for APL Field Devices

FEATURES

- **650mW Power Limit for Intrinsic Safety Thermal Rating when Line Voltage ≤ 18.5V**
- **35mA Current Limit if Line Voltage > 18.5V**
- **55mA Current Limit for APL Class A Devices**
- **Shunt Regulator for Mitigating Load Changes**
- **Guaranteed 20mA Rectifier Current for Signal Integrity**
- **Guaranteed to deliver full 500mW APL power to the load**
- **6V to 36V Input Voltage**
- **Integrated Current Sense Resistor**
- **Polarity Insensitive Line Voltage Detection**
- **8-Lead SOIC Package with Exposed Pad**

APPLICATIONS

- **Industrial Ethernet**
- **Advanced Physical Layer**
- **Current Limiting**

GENERAL DESCRIPTION

The LT8440 is a power conditioner for intrinsically safe, industrial ethernet ports in hazardous or explosive environments. The internal pass transistor is normally fully enhanced to deliver power to the load efficiently. In case of load circuit failures, the FET is modulated to limit the power to less than 650mW if line voltage ≤ 18.5V or less than 35mA if line voltage > 18.5V. The internal shunt transistor draws current parallel with the load up to the 500mW minimum guaranteed for Class A load power ports in compliance with Advanced Physical Layer (APL) standard or to 20mA minimum guaranteed if line voltage > 18.5V. The line voltage is sensed with two input pins that are insensitive to polarity, which can be connected in front of the port rectifier and incorporate the rectifier power consumption in the limitation of total power. The line current is measured as a voltage across the internal sense resistor, and the shunt current and the current limit are automatically adjusted for line voltage.

The LT8440 is packaged in an 8-lead SOIC with pin spacing that satisfies the device under coating specification so that shorts from pin to pin are countable faults when the circuit is examined for intrinsic safety at the highest levels of protection.

TYPICAL APPLICATION

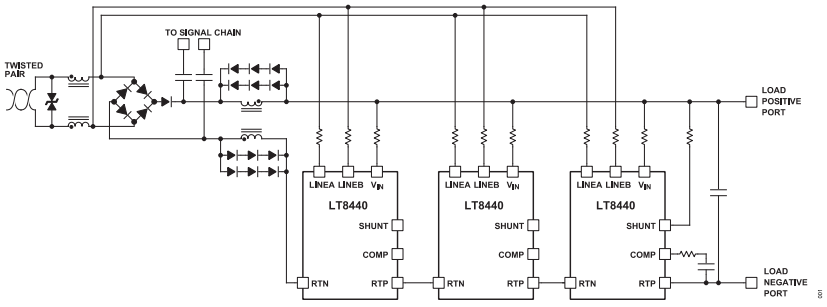

Figure 1. APL Field Device Port Power Conditioner

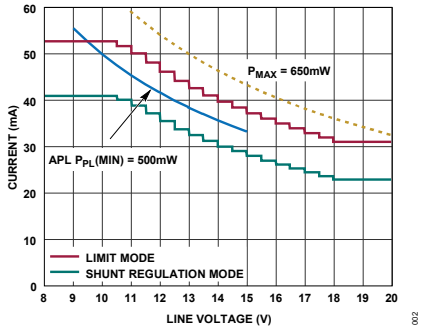

Figure 2. Regulation and Limit Current

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REVISION HISTORY

REVISION NUMBER	REVISION DATE	DESCRIPTION	DESCRIPTION
0	7/24	Initial release	—

SPECIFICATIONS

Table 1. Electrical Characteristics

(T_A = 25°C, V_{IN} = 9V, and V_{RTN} = 0V, unless otherwise noted[1].)

PARAMETER	CONDITIONS	COMMENTS	MIN	TYP	MAX	UNITS
Operating Input Voltage Range			6		36	V
V_{IN} Quiescent Current	V_{LINEA} = 20V, V_{LINEB} = 0V	-55°C ≤ T_A ≤ 150°C		120	200	µA
LINEA Pin Current	V_{LINEA} = 15V, V_{LINEB} = 0V			30	40	µA
LINEB Pin Current	V_{LINEB} = 15V, V_{LINEA} = 0V			30	40	µA
RTP to RTN Pass-Through Resistance	V_{LINEA} = 0V, V_{LINEB} = 8V, I_{RTP} = 30mA			4		Ω
Current Limit	$\lvert V_{LINEA}–V_{LINEB}\rvert$ = 0.5V			0		
	$\lvert V_{LINEA}–V_{LINEB}\rvert$ = 9V	-55°C ≤ T_A ≤ 150°C	49.5	52.1	55	mA
	Level 1		49.5	52.1	55	mA
	Level 2		48.3	51.1	54.2	mA
	Level 3		46.8	49.6	52.7	mA
	Level 4		44.9	47.6	50.7	mA
	Level 5		43.0	45.6	48.7	mA
	Level 6		41.0	43.6	46.7	mA
	Level 7		39.6	42.1	45.2	mA
	Level 8		38.1	40.6	43.7	mA
	Level 9		36.7	39.2	42.3	mA
	Level 10		35.6	37.9	41.1	mA
	Level 11		34.4	36.7	39.9	mA
	Level 12		33.2	35.5	38.7	mA
	Level 13		32.3	34.5	37.7	mA
	Level 14		31.3	33.5	36.7	mA
	Level 15		30.3	32.5	35.7	mA
	Level 16		29.3	31.5	34.7	mA
	Level 17		28.5	30.6	33.8	mA
Shunt Regulated Current	$\lvert V_{LINEA}–V_{LINEB}\rvert$ = 0.5V			0		
	$\lvert V_{LINEA}–V_{LINEB}\rvert$ = 9V		37.7	40.5	43.3	mA
	Level 1		37.7	40.5	43.3	mA
	Level 2		36.9	39.7	42.4	mA
	Level 3		35.7	38.4	41.1	mA

(T_A = 25°C, V_{IN} = 9V, and V_{RTN} = 0V, unless otherwise noted[1].)

PARAMETER	CONDITIONS	COMMENTS	MIN	TYP	MAX	UNITS
	Level 4		34.1	36.8	39.4	mA
	Level 5		32.5	35.1	37.7	mA
	Level 6		30.9	33.4	36.1	mA
	Level 7		29.7	32.1	34.8	mA
	Level 8		28.4	30.9	33.4	mA
	Level 9		27.3	29.7	32.3	mA
	Level 10		26.3	28.7	31.3	mA
	Level 11		25.3	27.7	30.3	mA
	Level 12		24.3	26.7	29.3	mA
	Level 13		23.4	25.9	28.4	mA
	Level 14		22.6	25.0	27.6	mA
	Level 15		21.7	24.2	26.7	mA
	Level 16		20.9	23.4	25.9	mA
	Level 17	–55°C ≤ T_A ≤ 150°C	20.2	22.7	25.2	mA
LINE Voltage Threshold (Rising)	Levels 1–2		10.14	10.5	10.82	V
	Levels 2–3		10.62	11	11.41	V
	Levels 3–4		11.12	11.5	11.91	V
	Levels 4–5		11.65	12	12.36	V
	Levels 5–6		12.16	12.5	12.84	V
	Levels 6–7		12.59	13	13.42	V
	Levels 7–8		13.12	13.5	13.88	V
	Levels 8–9		13.62	14	14.37	V
	Levels 9–10		14.07	14.5	14.92	V
	Levels 10–11		14.57	15	15.43	V
	Levels 11–12		15.05	15.5	15.93	V
	Levels 12–13		15.5	16	16.48	V
	Levels 13–14		16.02	16.5	16.96	V
	Levels 14–15		16.52	17	17.45	V
	Levels 15–16		17.02	17.5	17.95	V
	Levels 16–17		17.51	18	18.45	V
LINE Voltage Threshold Hysteresis				80		mV

(T_A = 25°C, V_{IN} = 9V, and V_{RTN} = 0V, unless otherwise noted[1].)

PARAMETER	CONDITIONS	COMMENTS	MIN	TYP	MAX	UNITS
Shunt and Limit Current Step Transition Rate	$\lvert V_{LINEA}–V_{LINEB}\rvert$ step from 12.2V to 12.8V				8	mA/ms

ABSOLUTE MAXIMUM RATINGS

T_A = 25°C unless otherwise specified. All pin voltages are relative to RTN[2].

Table 2. Absolute Maximum Ratings

PARAMETER	RATING
V_{IN}, RTP, COMP, and SHUNT	–0.3V to 42V
LINEA and LINEB	–42V to 42V
Operating Junction Temperature Range LT8440R[1, 3]	–55°C to 150°C
Storage Temperature Range	–65°C to 150°C

1 The LT8440R is specified over the −55°C to 150°C junction temperature range. High junction temperatures degrade operating lifetimes; operating lifetime is derated for junction temperatures greater than 150°C. Note that the maximum ambient temperature consistent with these specifications is determined by specific operating conditions in conjunction with board layout, the rated package thermal impedance and other environmental factors.

2 Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

3 This IC includes overtemperature protection, which is intended to protect the device during momentary overload conditions. The maximum rated junction temperature will be exceeded when this protection is active. Continuous operation above the specified absolute maximum operating junction temperature may impair device reliability or permanently damage the device.

BLOCK DIAGRAM

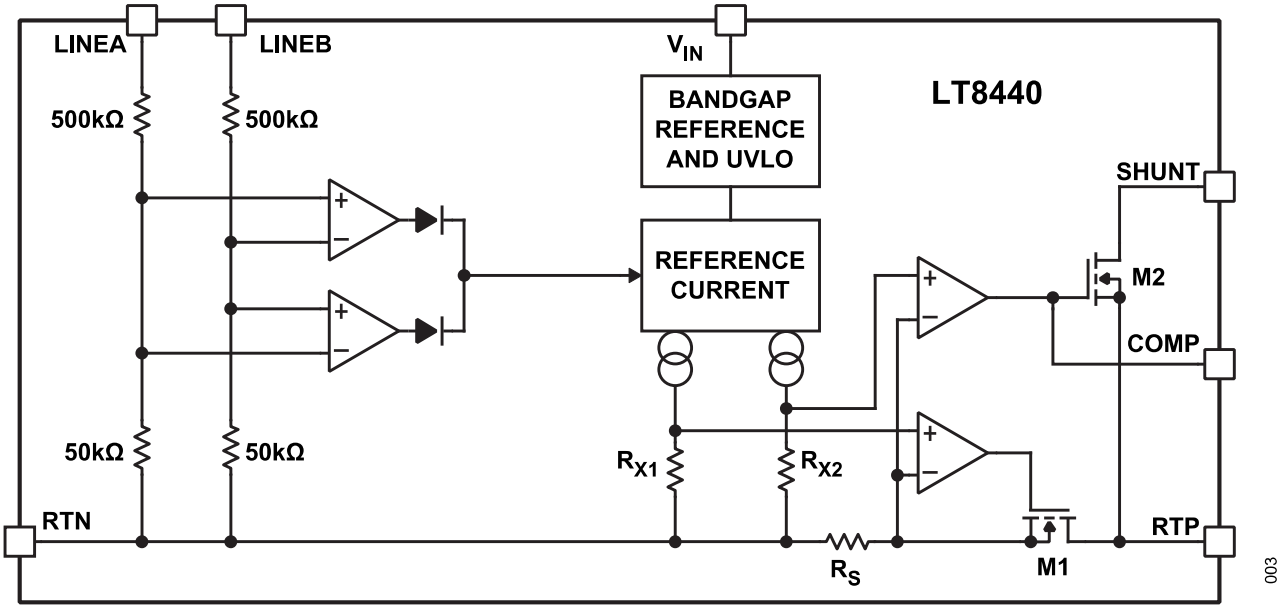
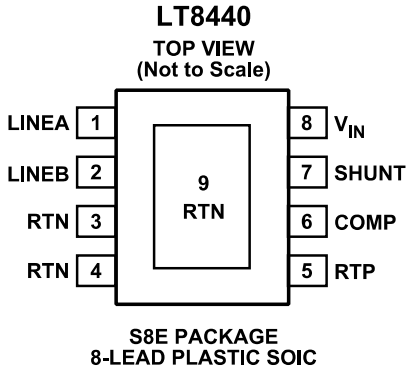


Figure 3. Block Diagram

PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS



θ_{JA} = 39.3°C/W, θ_{JCTOP} = 80.9°C/W, θ_{JCBOT} = 5.8°C/W

THE EXPOSED PAD (PIN 9) IS RTN AND MUST BE SOLDERED TO PCB.

Figure 4. Pin Configuration

Table 3. Pin Descriptions

PIN	NAME	DESCRIPTION
1, 2	LINEA, LINEB	Connect each of these pins through their own resistors to the terminals of the twisted pair to sense the line voltage. The resistors should be around 20kΩ. A smaller resistance is insufficient for intrinsic safety if the LT8440 is damaged, and a larger resistor negatively impacts the accuracy of the voltage measurement. The polarity of the connection to the twisted pair does not matter. The LT8440 will adjust the limit for the current it allows through the internal pass device according to the absolute voltage between these pins.
3, 4, 9 (EP)	RTN	Connect these pins to the RTP pins of another instance of the LT8440 or to the return terminal of the rectifier for the twisted pair. The current for the load circuits will exit from these pins after passing through the LT8440.
5	RTP	Connect these pins to the RTN pins of another instance of the LT8440 or to the common return path for all the field device load circuits.
6	COMP	Optional pin for additional compensation of the shunt regulation loop. If unused, leave it floating. See the *Applications Information* section for more details.
7	SHUNT	Connect this pin to load positive. The internal shunt transistor will draw current as necessary to maintain about 500mW through the rectifier for the twisted pair. Optional resistors can reduce the power dissipation of LT8440. If unused, leave it floating.
8	V_{IN}	The quiescent current for the LT8440 is drawn through this pin, where the input voltage is applied. Connect it to the output of the rectifier of the twisted pair through a resistor. The resistor should be around 15kΩ. A smaller resistor is insufficient for intrinsic safety if the LT8440 is damaged, and a larger resistor limits the LT8440's operating range unnecessarily. See the *Applications Information* for more details on how to select this resistor.

TYPICAL PERFORMANCE CHARACTERISTICS

(T_A = 25°C, unless otherwise noted.)

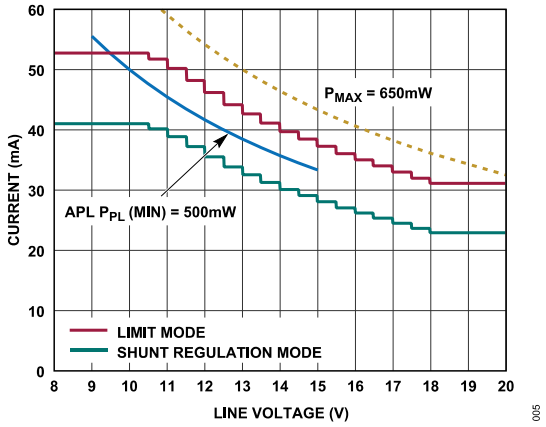


Figure 5. Current Regulation and Limit

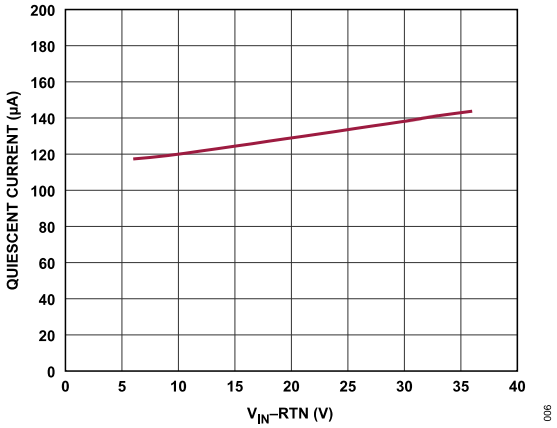


Figure 6. V_{IN} Pin Quiescent Current vs Pin Voltage

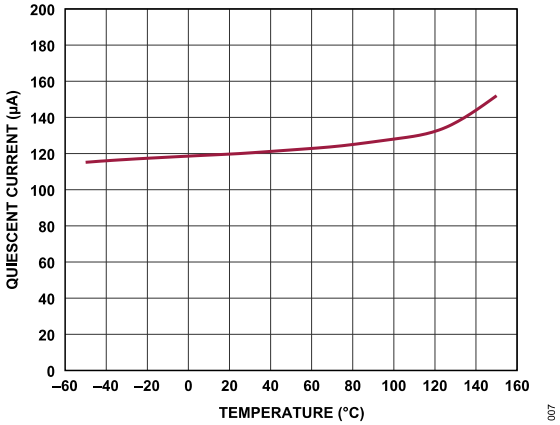


Figure 7. V_{IN} Pin Quiescent Current vs Temperature at V_{IN}-V_{RTN} = 9V

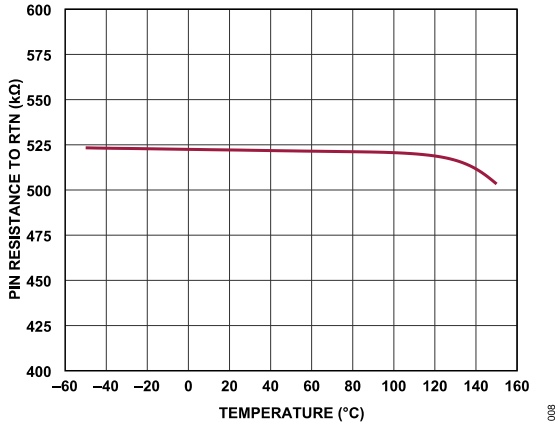


Figure 8. LINEA/LINEB Pin Resistance vs Temperature

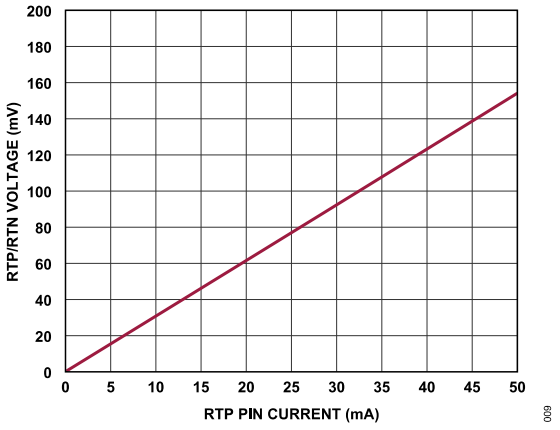


Figure 9. RTP/RTN Voltage Drop vs Current at $V_{LINEA-LINEB}$ = 9V

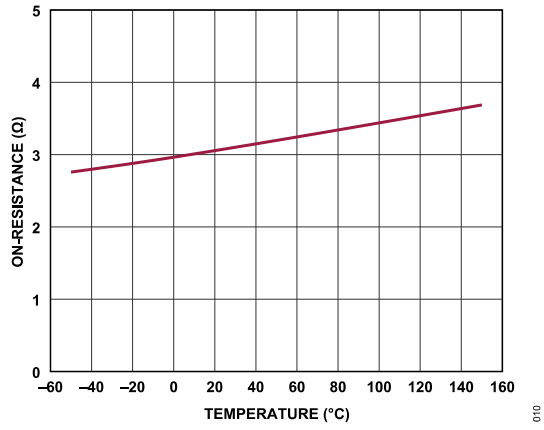


Figure 10. RTP/RTN On-Resistance vs Temperature

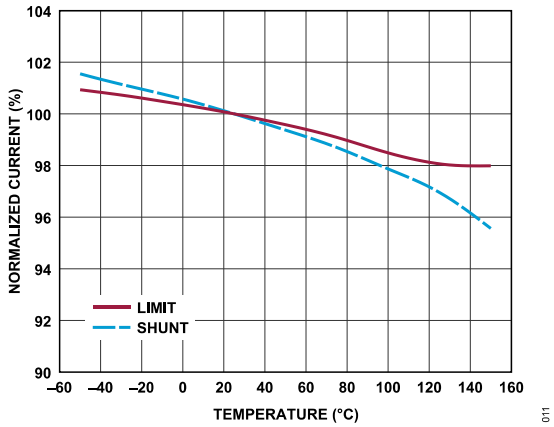


Figure 11. Normalized Current Regulation vs Temperature

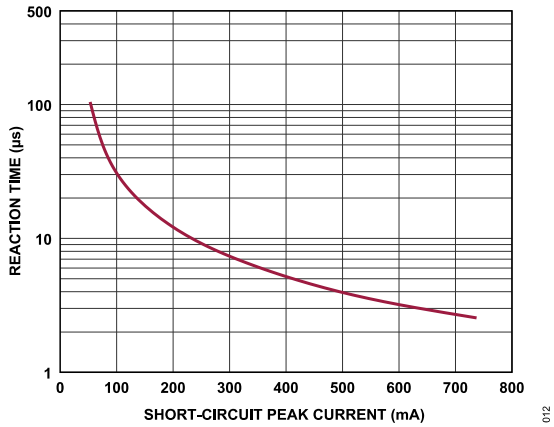


Figure 12. Current Limit Reaction Time in Short-Circuit Event

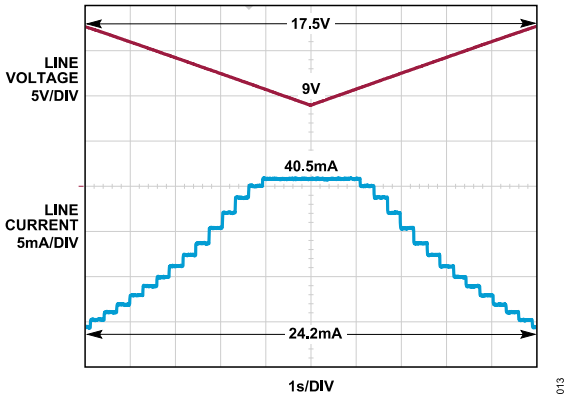


Figure 13. Line Voltage Sweep with Open Load (See Typical Application, Figure 32)

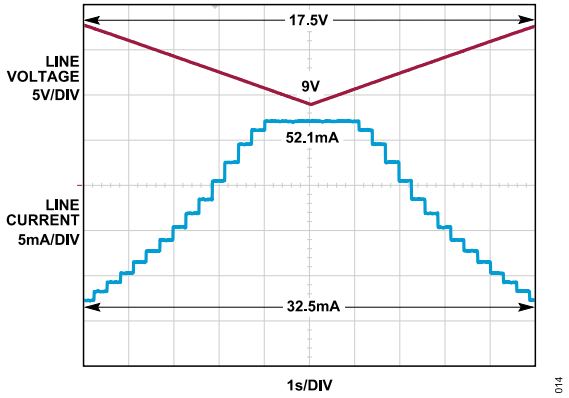


Figure 14. Line Voltage Sweep with Shorted Load (See Typical Application, Figure 32)

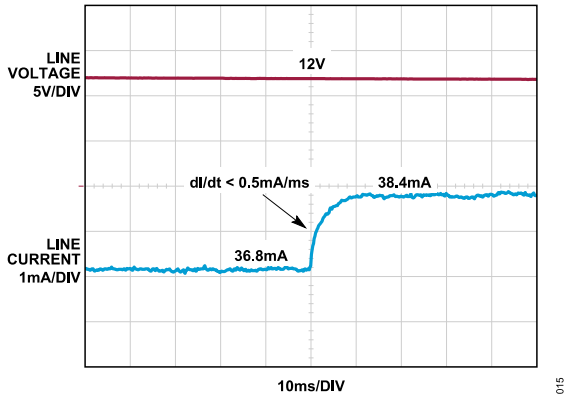


Figure 15. Zoom-In of Current Step-Up with Open Load (See Typical Application, Figure 32)

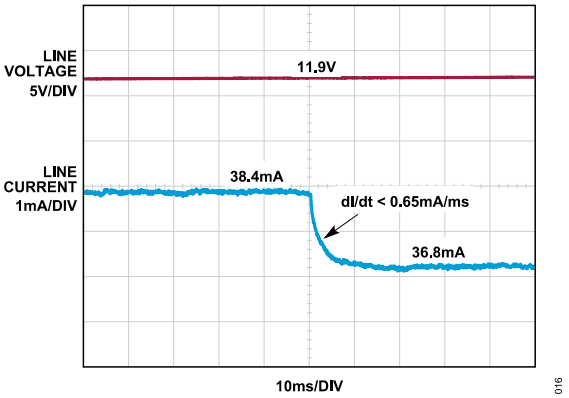


Figure 16. Zoom-In of Current Step-Down with Open Load (See Typical Application, Figure 32)

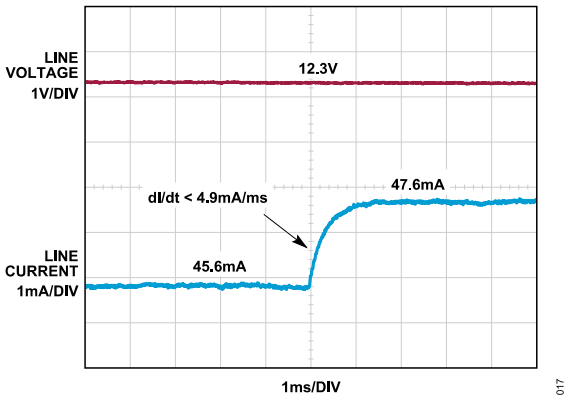


Figure 17. Zoom-In of Current Step-Up with Shorted Load (See Typical Application, Figure 32)

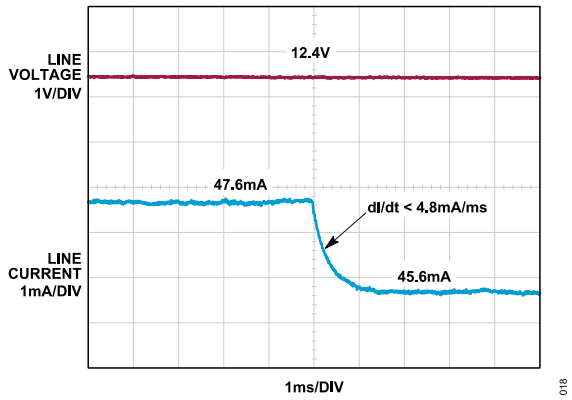


Figure 18. Zoom-In of Current Step-Down with Shorted Load (See Typical Application, Figure 32)

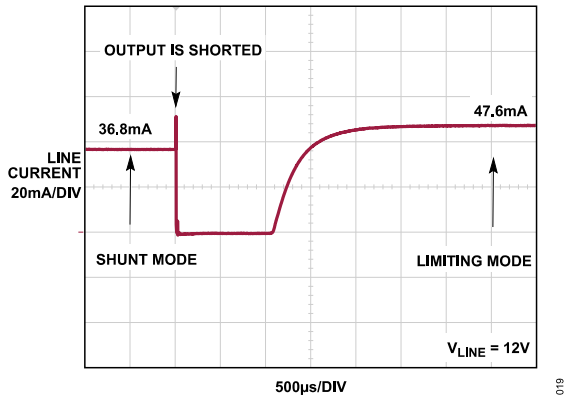


Figure 19. Short-Circuit Protection (See Typical Application, Figure 32)

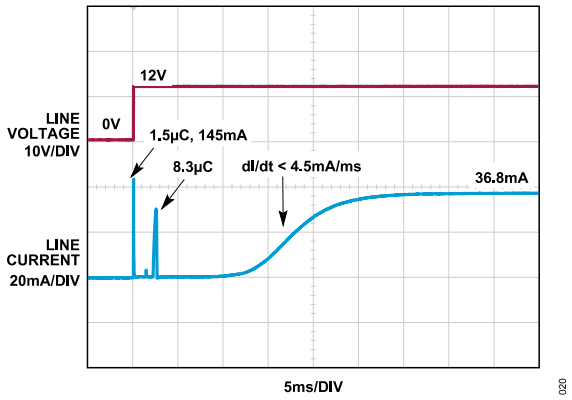


Figure 20. Hot-Input Connection (See Typical Application, Figure 32)

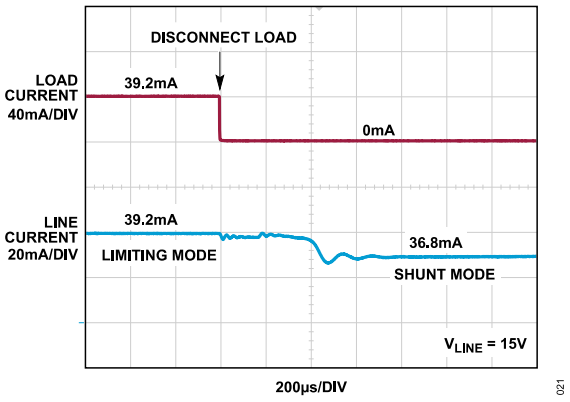


Figure 21. Transition From Current Limiting Mode to Current Shunt Mode (See Typical Application, Figure 32)

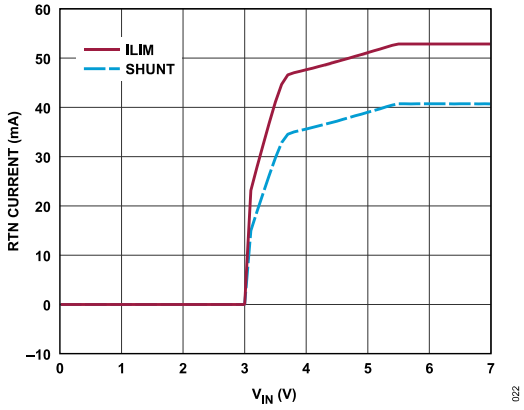


Figure 22. Current Shunt and Limit Behavior at Input Undervoltage

OPERATION

Overview

Ethernet-APL (Advanced Physical Layer) is a standardized 2-Wire Ethernet physical layer based on 10BASE-T1L (IEEE802.3cg). It can transmit both signal and power over long distances in hazardous or explosive environments. APL enables direct and high-speed connection of field devices to Ethernet infrastructure for the process industry. *Figure 23* shows an exemplary APL topology. The field devices connect to field switches through the spur connections up to the 200m distance, and field switches connect to the power switch or other field switches through the trunk connection up to the 1000m distance.

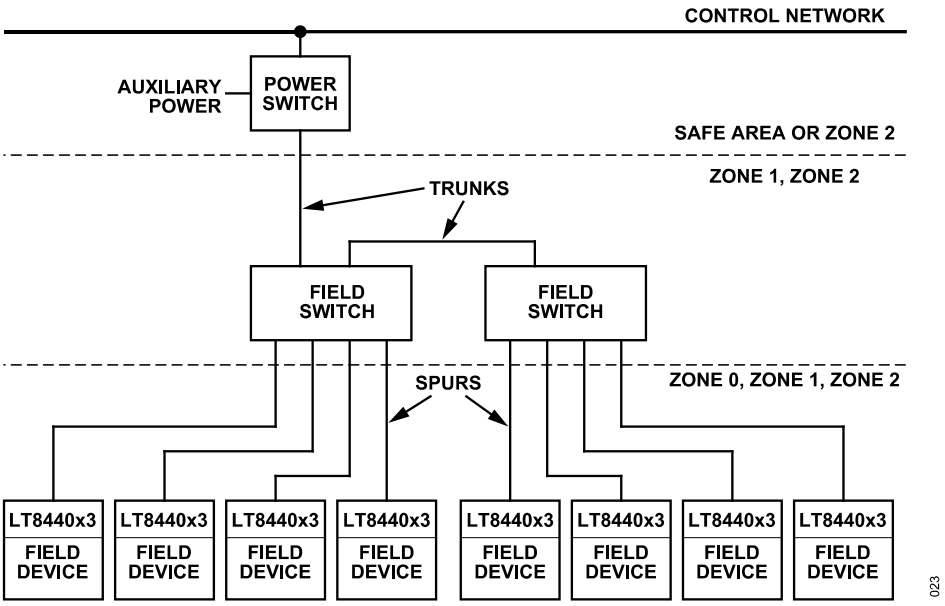


Figure 23.Exemplary APL Topology

LT8440 power conditioner is designed for Class A field devices with intrinsic safety Ex ia (APL port class SLAA), which should be used in Zone 0/Div 1 hazardous area. With three LT8440s in series, it protects the field device from two countable faults, and optimizes the power delivery while maintaining compliance with APL and Intrinsic Safety. Across the voltage range, it maintains ≥500mW power available to the load but also limits <650mW from the port at fault.

Theory of Operation

The LT8440 should be positioned in the return path of the load current for a power port in an ethernet field device such that the current enters the RTP pins and exits through the RTN pins. The part includes a resistor for measuring the current drawn through the port and a pass transistor for regulating that current. The pass transistor will be driven to full enhancement to minimize the voltage across its source and drain until the current rises to a limit that varies with the line voltage sensed by LINEA and LINEB pins. The limitation of current and, ultimately, power by means of the pass device facilitates certification for intrinsic safety because failing components would otherwise have to dissipate the full power available from the power-sourcing equipment.

The collection of APL and Intrinsic Safety requirements limit the permitted current in the field device to between 55mA and 20mA, and the permitted power to between 500mW and 5.32W. Under all these conditions, including fault scenarios, the field device must not exceed allowed self-heating temperatures. The optimal way to meet all the

requirements is to implement a V-times-I power limit in the field device that gives the load maximum operating power and still limits fault-related heating. As shown in *Figure 3* (Block Diagram), this is achieved by adjusting the current limit as the voltage changes. At any given line voltage, a selected reference current flows through the internal resistor R_{X1}. The voltage across the resistor R_{X1} is compared to the voltage across the sense resistor R_S by the error amplifier. When the R_{X1} voltage exceeds the R_S voltage, the amplifier will drive the gate of the internal pass transistor M1 high. When the voltages are equal, the internal amplifier will reduce the gate voltage of M1 such that the current through M1 is reduced and the load current is limited. The current limit is, therefore, steady through each narrow division of the operating voltage range but changes as the voltage changes to maintain a power limit between 500mW and 650mW. This guarantees that the load can receive at least 500mW but not more than 650mW under any conditions.

By a similar process, a separate amplifier compares the voltage across R_{X2} to the voltage across R_S. In this case, the transistor M2 increases the shunt current whenever the voltage on R_{X2} exceeds the voltage on R_S. The voltage across R_{X2} is similar to that of R_{X1}, but lower, so that the total power drawn by the port is maintained just under 500mW. The shunt current guarantees at least 20mA port current even at zero load, which is required by APL specification for signal integrity. The shunt current dynamically balances the changes to the load current, so that the current in the twisted pair does not change abruptly. The APL standard limits the rate of change of the line current for signal integrity.

The line voltage is sensed through the LINEA and LINEB pins. These pins are loaded internally with a resistor network that divides the sensed line voltage to a lower level suitable for the comparators. This means that the line voltage is sensitive to the value of the external resistors, which are connected in series with the lines to limit current in the case of pin short, to satisfy the assessment for intrinsic safety. See the *Applications Information* section for more details on how to select this resistor.

APPLICATIONS INFORMATION

Very few components are required to configure the LT8440 for use in a load power port of an intrinsically safe field device and limit the power drawn by the port according to the Advanced Physical Layer standard. The following sections are intended to guide the selection of those components.

Input Frontend Design

Figure 24 shows a typical field device frontend design. The cable shield is directly connected to the field device's chassis. A TVS diode D1 protects any surge or ESD event on a twisted pair. The trip voltage of D1 should be higher than 17.5V to not interfere with normal operation, while it should be low enough to still protect the circuits following. A common-mode choke L1 suppresses the common-mode noise.

After L1, a diode bridge is used to eliminate polarity sensitivity at the module input. An additional diode, D6, is used to block the spark energy when faults happen in the diode bridge. The LINEA/LINEB pins of LT8440 can be connected either before or after the diode bridge. Connecting them before the diode bridge improves the accuracy of voltage sensing. However, in this configuration, a two-point failure scenario where LINEA/LINEB shorts to SHUNT and RTP, respectively, can form a leakage path from the input port to the load capacitor through LINEA/LINEB resistors. If the total capacitance on the load side is large, LINEA/LINEB pins should be connected after the diode bridge, as shown in *Figure 25*. Note that if a fault happens after the diode bridge, according to IEC60079, D2~D6 should be able to withstand 1.5x of the worst-case stress. The worst-case voltage/current is 17.5V/380mA. Therefore, the diodes should be rated to at least 26.25V/570mA. Also be aware that the diode drops reduce the total available power to the load, as well as the minimum input voltage of LT8440. Schottky diodes can be used instead, to have less voltage drop. However, Schottky diodes usually have a significantly higher leakage current at hot temperatures, and these leakages cannot be sensed by LT8440.

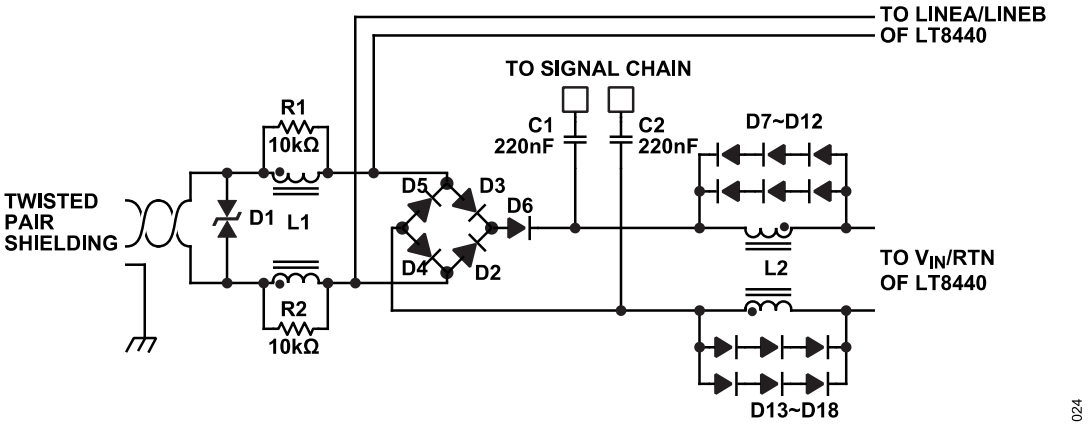


Figure 24.Typical Field Device Frontend Design

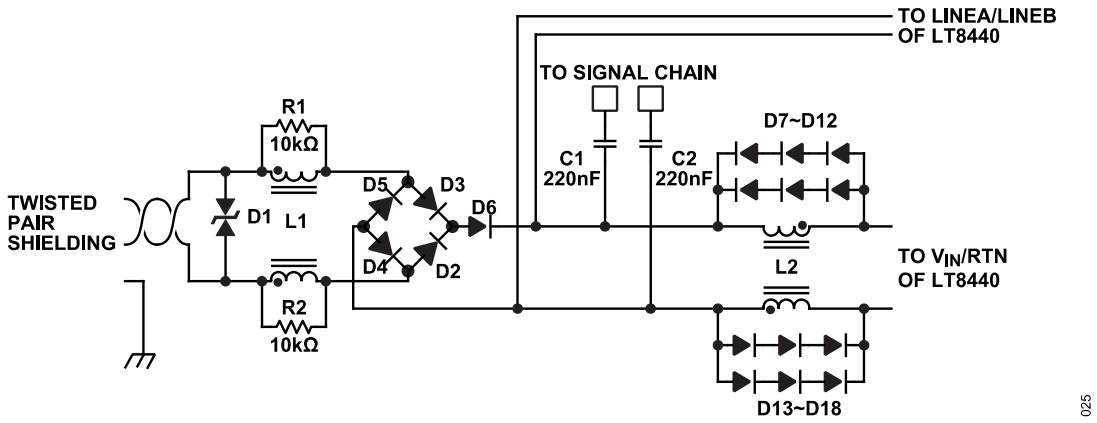


Figure 25. Alternative Frontend Design with Large Capacitance on the Load Side

After the diode bridge, a differential choke L2 is necessary to separate the DC path from the AC signal, and LT8440 is connected after L2 to condition and limit the input power. See the *Differential Choke* section on the design of the differential choke.

If the application requires input decoupling capacitors in the power path, these capacitors should be placed after LT8440 (between load positive/negative ports, as shown in *Figure 1*) not before LT8440, so that the LT8440 can protect any capacitor failures. LT8440 will also limit the inrush current to these capacitors during a line hot-connect to comply with the APL standard.

Differential Choke

The differential choke L2 is required to isolate the signal from the large capacitive load on the power path. The signal attenuation is measured by transmitter output signal droop as well as medium-dependent interface (MDI) return loss. APL requires ≤ 10% droop and return loss to meet or exceed limits, as shown *Table 4* (with 100Ω ±0.1% reference impedance).

Table 4. MDI Return Loss Specifications Based on IEEE 802.3cg-2019 Standards

Frequency Range	Limit in dB
$0.1\text{MHz} \leq f \leq 0.2\text{MHz}$	$20 - 18 \times \log_{10}\left(\frac{0.2}{f}\right)$
$0.2\text{MHz} \leq f \leq 1\text{MHz}$	20
$1\text{MHz} \leq f \leq 10\text{MHz}$	$20 - 16.7 \times \log_{10}(f)$
$10\text{MHz} \leq f \leq 20\text{MHz}$	$3.3 - 7.6 \times \log_{10}\left(\frac{f}{10}\right)$

To meet these requirements, it is recommended to use 220nF±20% for C1/C2, and L2 to have 220µH±20% inductance per winding (equivalently 220µH × 4 = 880µH in total). *Figure 26* shows the measured signal droop and return loss from the LT8440 demo board. For a detailed measurement setup, refer to the *LT8440 demo manual*.

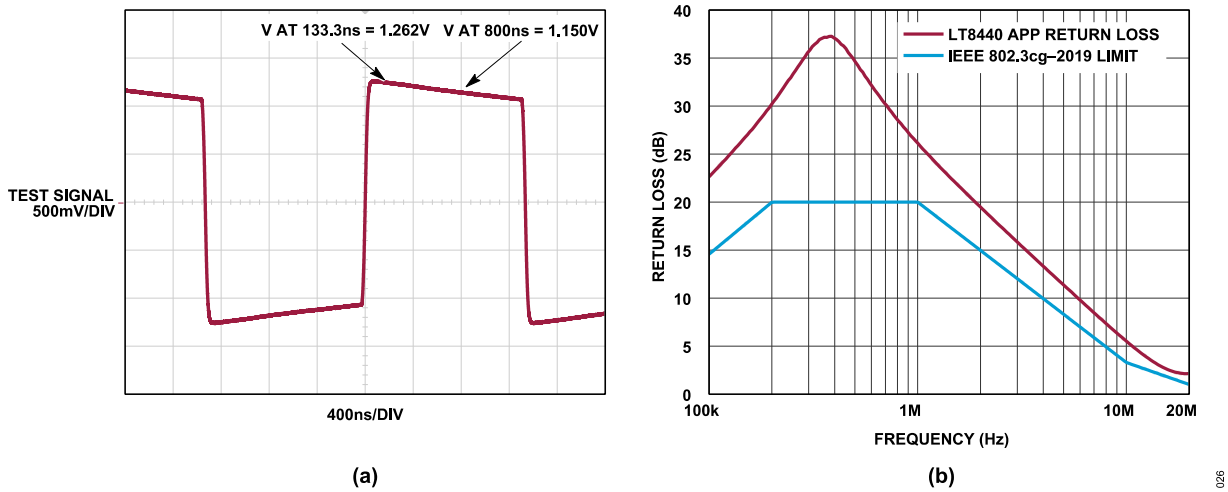


Figure 26. Measured (a) Signal Droop and (b) Return Loss on the Typical Application Circuit (See Figure 32). C1 = C2 = 220nF, L2 = 220µH.

In the event of a fault, for example, a sudden open circuit, a large dI/dt in L2 can cause a significant voltage surge across L2, which must be clamped. Since the ethernet signal level is about $1.0V_{PP}$, the clamp should trigger at a higher voltage so that normal communication is not interfered with. It is recommended to use two or three silicon diodes in series, to have sufficient voltage drop across the full temperature range. Also, two diode strings are used in parallel as safety redundancy.

Redundant Use of LT8440

The highest level of Intrinsic safety allows the system to withstand two countable faults. (Countable faults refer to arbitrary faults imposed by the examiner to analyze the efficacy of protection against thermal and spark ignition faults.) Therefore, three independent power-limiting devices are required in series, and the LT8440 has been designed so that three instances of the part can operate in series. The RTN and RTP pins are positioned on opposite sides of the package so that the current exiting from the RTN pins of one instance can enter the RTP pins of the following instance by a short and direct path.

The LT8440 can operate in single, double, or triple redundant circuits to provide Ex ic, ib, or ia level of circuit protection.

V_{IN}/LINEA/LINEB External Resistors

Three pins, LINEA, LINEB, and V_{IN}, each require an external resistor to limit the current drawn by the port in the event of either damage to the LT8440 or LT8440 pin-shorts, resulting in a short-circuit that would bypass the pass transistor. In this case, the power dissipated in the resistor would be unavailable to the load but would prevent a spark or excessive heat. Film resistors in 1206 or larger packages have sufficient size and construction to be considered infallible to short-circuit faults. Therefore, a single resistor to each pin is sufficient. In a scenario where this assumption does not hold, two resistors in series are required on each pin for two countable failures.

The resistance of the current-limiting resistor on each pin should be large enough so that at a fault event, the surface temperature rise in the worst-case scenario still complies with IEC60079. However, larger resistors increase the voltage drop. *Figure 27* is a simplified circuit diagram regarding components on LINEA, LINEB, and V_{IN} pins (assuming a frontend design as shown in *Figure 24*). For LINEA and LINEB pins, the equivalent internal resistance is about 550kΩ typical, and the resistance change over temperature is shown in *Figure 8*. The additional voltage drop on the pin resistors R_A and R_B will reduce the sensed line voltage and, therefore, a small error in power. It is recommended to use around 20kΩ current limiting resistors on LINEA and LINEB pins. At 9V, the V_{IN} pin has a

quiescent current of about 120µA at 25°C or about 150µA at 150°C. It varies across c voltage and temperature, as shown in *Figure 6* and *Figure 7*. On top of the voltage drop across the input resistor R_{IN}, there are three additional diode drops. Therefore, the input resistor, R_{IN}, value should be small enough that at the minimum line voltage (9V), the V_{IN}–RTN voltage is still above the minimum 6V operating voltage. It is recommended to use a 15kΩ current-limiting resistor on the V_{IN} pin.

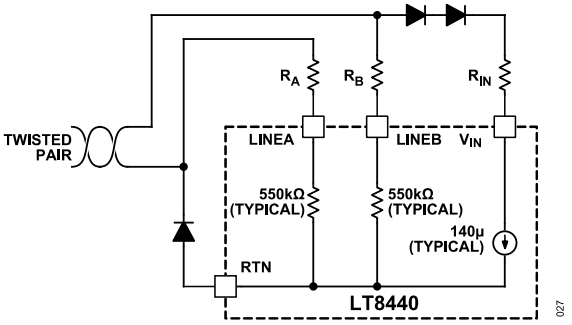


Figure 27. Simplified Circuit on LINEA, LINEB, and V_{IN} Pins

Loop Stability

Current Limit Loop

The current limit loop is internally compensated. *Figure 28* shows a simplified equivalent circuit of the current limit loop while the load is short-circuited. V_{LINE} is the input port voltage, and L is the total input inductance.

$$L \approx L_{SOURCE} + 4 \times L_{DIFF}$$

where L_{SOURCE} is the total inductance from the source side, including the cable inductance, and L_{DIFF} is the inductance of each winding of the differential choke. Since the load side has a low-impedance short, it is assumed that the load impedance (including the output capacitors) has a negligible effect on the loop stability.

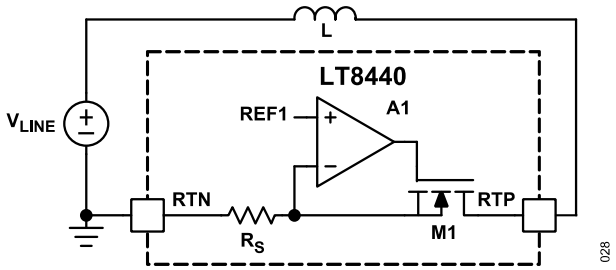


Figure 28.Simplified Equivalent Circuit of Current Limit Loop at Load Short

The current limit loop has two poles. The dominant pole is at the gate of M1, which is internally compensated. LT8440 guarantees stable operation across process and temperature variations when L ≤ 5mH.

Current Shunt Loop

The current shunt loop is more complicated than a current limit loop. *Figure 29* shows the equivalent circuit of the shunt loop. R_{ON1} is the on-resistance of M1. C_{LOAD} is the output capacitance, and I_{LOAD} is the load current.

Similar to the current limit loop, in the shunt loop, the dominant pole is at the gate of M2 (or COMP pin). The load capacitors C_{LOAD} and L create non-dominant complex poles. A fourth pole is due to the capacitor current. Therefore, if a large load capacitor is needed (≥ 10µF), it is advised to increase the ESR of C_{LOAD} to about 1Ω to 5Ω to insert a zero to compensate for the effect of these non-dominant poles.

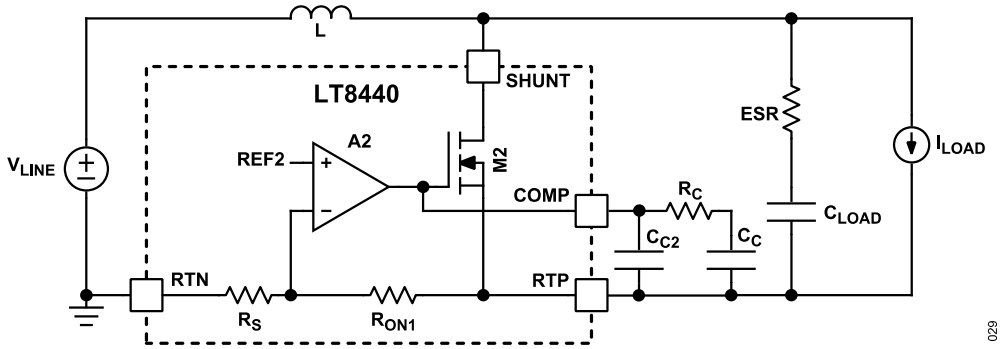


Figure 29. Simplified Equivalent Circuit of Current Shunt Loop

Regarding the current shunt loop compensation, theoretically, an external capacitor C_C can be sufficiently lower than the frequency of the dominant pole to stabilize the loop. However, if the shunt loop bandwidth is too slow, it can impact the ability of the shunt loop to compensate for the fast-changing current from the load. Resistor R_C adds another zero, which can help increase the bandwidth while maintaining the loop stability. Sometimes, an additional small cap C_{C2} can be added between COMP and RTP to improve the gain margin and, therefore, the high-frequency noise immunity.

Table 5 shows the choice of compensation for certain C_{LOAD} values. For different application requirements, a practical approach is to start from a similar condition in the table and tune the compensation to optimize the performance. LTspice® simulations can help in this process. Stability should then be checked across all operating conditions, including load current, input voltage, and temperature.

Table 5. Recommended Compensation Values

C_{LOAD}	ESR	L_{SOURCE}	L_{DIFF}	R_C	C_C	C_{C2}
660nF	1Ω	0mH~4mH	220µH	20kΩ	47nF	Open
6.6µF	1Ω			62kΩ	22nF	Open
	10Ω			470kΩ	2.2nF	Open
100µF	1Ω			470kΩ	4.7nF	Open

Short-Circuit Event

When a fault occurs at the load side that causes a short-circuit, the current limit loop in LT8440 will activate to eventually limit the total input current to 55mA or lower, depending on the line voltage. However, due to the finite bandwidth of the current limit loop, the short-circuit current cannot be limited immediately. Before the current limit loop functions, the peak current spike is limited by the total loop impedance from the power source to the short location. The simplified test setup in *Figure 30* emulates the worst-case scenario where the loop impedance is minimized. With this setup, the measured reaction to a hard short event is shown in *Figure 31* at 17.5V input voltage. *Figure 12* shows the typical reaction time of LT8440 at different peak current spike, where the reaction time and short-circuit peak current are shown in *Figure 31*. LT8440 is guaranteed to survive at least a 600mA fault current spike flowing through either RTP, RTN, or SHUNT pins within its own reaction time. The downstream circuits must also survive the surge for the corresponding reaction time.

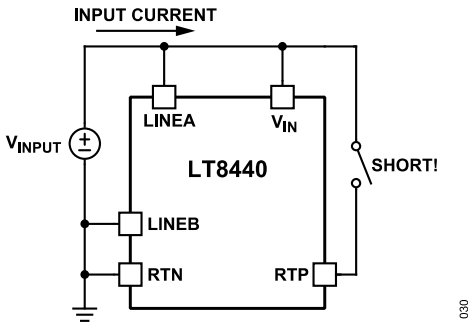


Figure 30. Simplified Short-Circuit Reaction Test Setup

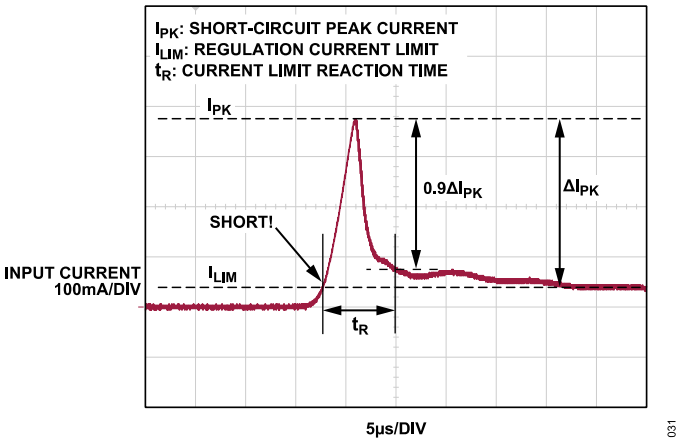


Figure 31. Measured Fast Short-Circuit Reaction at 17.5V input.

Printed Circuit Board (PCB) Layout, Coating, and Thermal Considerations

Care should be taken in the PCB layout to ensure good heat sinking of the LT8440. The power ground plane should consist of large copper layers with thermal vias; these layers spread heat dissipated by the IC. Placing additional vias can reduce thermal resistance further. Extra attention is also needed to guarantee that the designed circuit board is intrinsically safe. For example, the trace separations should comply with the clearance and creepage requirements documented in IEC60079-11. The distance between conductor planes in the z-axis should be carefully examined as well. For more details and PCB design files, refer to the *LT8440 demo manual*.

According to IEC60079-11 Ed. 7.0 Table 7, with peak voltage of 10V~ 30V, level ia/ib protection requires ≥ 2mm conductor separation without coating, or ≥ 0.7mm clearance with coating. Due to the limit of SOIC pin spacing, the LT8440 needs to be at least coated (or potted) on the application circuit board to be able to treat the pin shorts as countable faults.

The maximum load current should be derated as the junction temperature approaches its maximum temperature rating. Power dissipation within the IC can be estimated by calculating the total power loss. The junction temperature can be calculated by multiplying the total IC power dissipation by the thermal resistance from the junction to the ambient and adding the ambient temperature. The LT8440 includes internal overtemperature protection intended to protect the device during momentary overload conditions. The overtemperature protection shuts down the IC when the junction temperature exceeds 175°C (typ). The maximum rated junction temperature is exceeded when this protection is active. Continuous operation above the specified absolute maximum operating junction temperature (see *Absolute Maximum Ratings* section) may impair device reliability or permanently damage the device.

TYPICAL APPLICATIONS

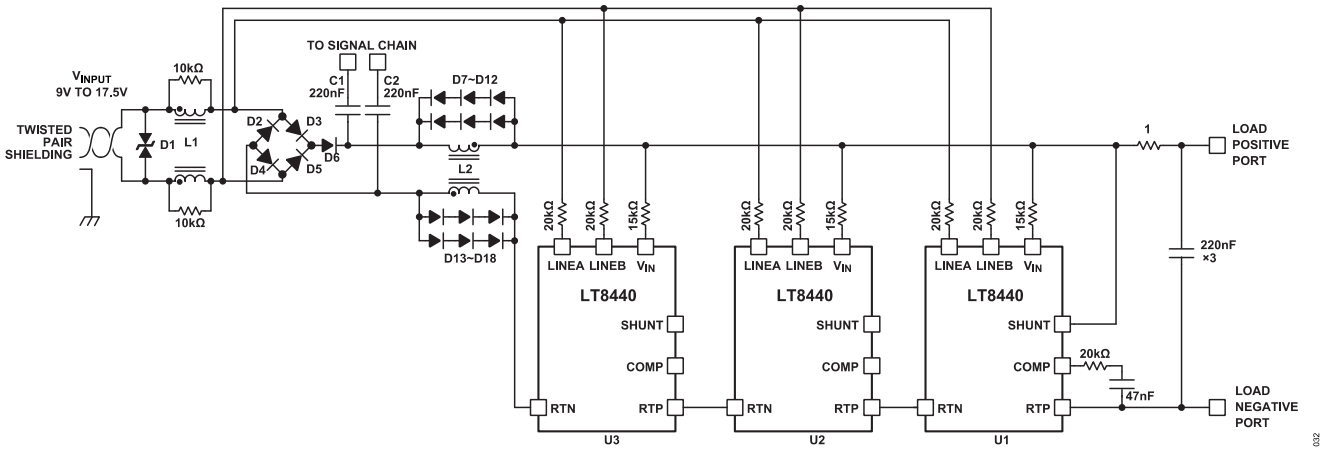


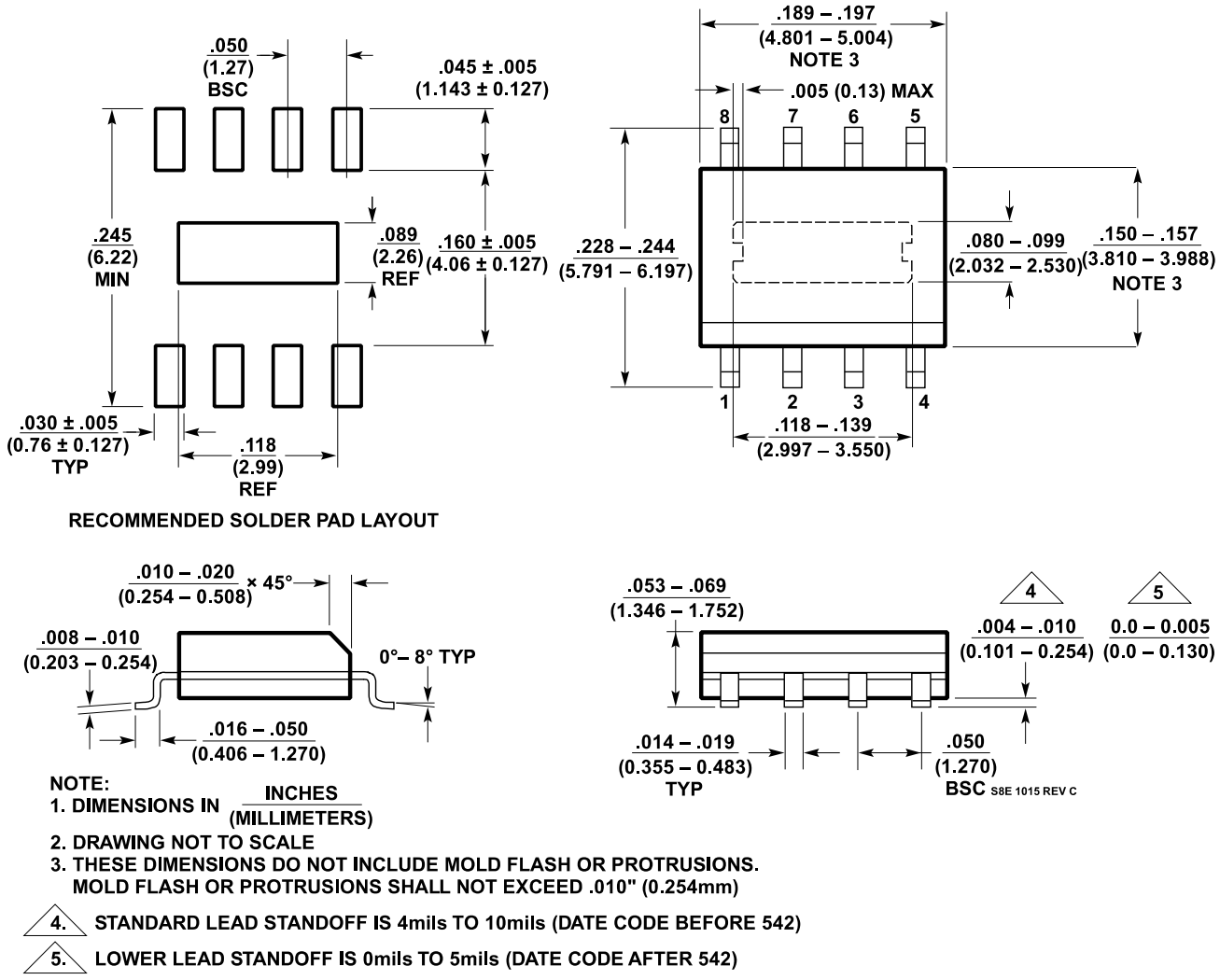
Figure 32. APL Class A Field Device Port Power Conditioner

Table 6. Recommended Components for Typical Application[1]

	L1	L2	D1	D2–D6	D7–D18
PART NUMBER	744223	MSD1260-224KLD	SM4T30CAY	BAT165E632HTSA1	S1AFL
MANUFACTURER	Wurth	Coilcraft	STMicroelectronics	Infineon	OnSemi
VALUE	500µH	220µH	V_{RM} = 26V, V_{CL} = 39.4V at 25A 8/20µs	40V/750mA	50V/1A

1. The recommendation is subject to further assessment for usage in specific intrinsically safe applications.

OUTLINE DIMENSIONS



NOTE:
1. DIMENSIONS IN INCHES (MILLIMETERS)
2. DRAWING NOT TO SCALE
3. THESE DIMENSIONS DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS.
   MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED .010" (0.254mm)
4. STANDARD LEAD STANDOFF IS 4mils TO 10mils (DATE CODE BEFORE 542)
5. LOWER LEAD STANDOFF IS 0mils TO 5mils (DATE CODE AFTER 542)

Figure 33. Package Drawing

ORDERING GUIDE

Table 7. Ordering Guide

PART NUMBER	TAPE AND REEL[1]	PART MARKING	PACKAGE DESCRIPTION	MSL RATING	TEMPERATURE RANGE[2]
LT8440RS8E#PBF	LT8440RS8E#TRPBF	8440	8-Lead Narrow SOIC	3	–55°C to 150°C

1. *Tape and reel specifications*. This package is available in 500-unit reels through designated sales channels with the #TRMPBF suffix.

2. The LT8440R is specified over the −55°C to 150°C junction temperature range. High junction temperatures degrade operating lifetimes; operating lifetime is derated for junction temperatures greater than 150°C. Note that the maximum ambient temperature consistent with these specifications is determined by specific operating conditions in conjunction with board layout, the rated package thermal impedance and other environmental factors.

RELATED PARTS

Table 8. Related Parts

PART NUMBER	DESCRIPTION	COMMENTS
ADIN1100	Robust, Industrial, 10BASE-T1L Ethernet PHY	IEEE 802.3cg-2019 compliant, low power, 40-lead 6mm × 6mm LFCSP
ADIN1110	Robust, Industrial, 10BASE-T1L Ethernet MAC-PHY	IEEE 802.3cg-2019 compliant, ultralow power, 40-lead 6mm × 6mm LFCSP
LTC9111	Industrial SPoE PD Controller	IEEE 802.3cg compliant, 2.3V to 60V input, support SCCP, 12-Pin MSOP or 4mm × 3mm DFN
LT8606/ LT8606B	42V, 350mA Synchronous Step-Regulator with 2.5µA Quiescent Current	V_{IN} = 3V to 42V, I_Q = 2.5µA, $V_{OUT(MIN)}$ = 0.8V, MSOP-10 or 2mm × 2mm DFN
LTC3315B	Dual 5V, 2A Synchronous Step-Down DC/DCs	V_{IN} = 2.25V to 5.5V, $V_{OUT(MIN)}$ = 0.5V, 2mm × 2mm LQFN
ADP2140	3 MHz, 600mA, Low Quiescent Current Buck with 300mA LDO Regulator	Buck output 1.5V to 3.3V, LDO output 0.8V to 3.3V, 3mm × 3mm LFCSP
MAX25210	Automotive Ultra Low Quiescent Current Linear Regulator Family	V_{IN} = 3.5V to 36V, fixed (3.3V or 5V) or adjustable output, up to 300mA, 3mm × 3mm TQFN