Data Sheet

LT8349

8V, 12A, 2-Phase Low IQ Synchronous Boost Converter

FEATURES

- Input Voltage Range: 2.5V to 5.5V
- Output Voltage Programmable Up to 8V
- 2-Phase Operation Reduces Required Input and Output Capacitance and Power Supply Induced Noise
- Synchronous Operation for High Efficiency and Reduced Heat Dissipation
- Stage Shedding™ and Optional Burst Mode® Operation for High Efficiency at Light Load
- Low V_{IN} Pin Quiescent Current:
  - 0.5µA in Shutdown
  - 15µA in Burst Mode Operation
- Integrated 8V/6A Synchronous Power Switches
- Adjustable and Synchronizable: 300kHz to 4MHz
- Burst Mode or Forced Continuous Operation at Light Load
- Accurate 1V Enable Pin Threshold
- Small 1.9mm x 2.6mm WLCSP Package

APPLICATIONS

- Handheld and Industrial Power Supplies

GENERAL DESCRIPTION

The LT8349 is a 2-phase single output synchronous boost converter that drives two internal N-Channel power MOSFET stages out-of-phase. Multiphase operation reduces input and output capacitor requirements and allows the use of smaller inductors than the single-phase equivalent. Synchronous rectification increases efficiency, reduces power losses, and eases thermal requirements, enabling high power boost applications.

The LT8349 features Stage Shedding and selectable Burst Mode operation at light load conditions allowing high efficiency over a wide range of load. It features optional spread spectrum frequency modulation (SSFM) to minimize EMI emissions.

The LT8349 integrates 8V/6A power switches, operating at a fixed switching frequency programmable between 300kHz and 4MHz and synchronizable to an external clock. The LT8349 features output soft-start and output overvoltage lockout.

TYPICAL APPLICATION

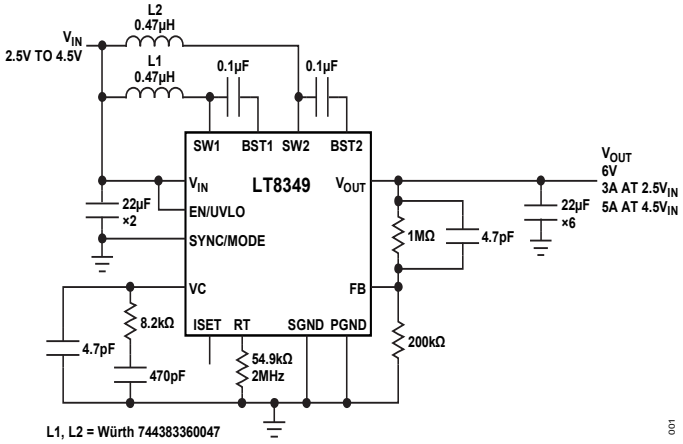

Figure 1. 2.5V to 4.5V Input, 6V Output Boost Converter

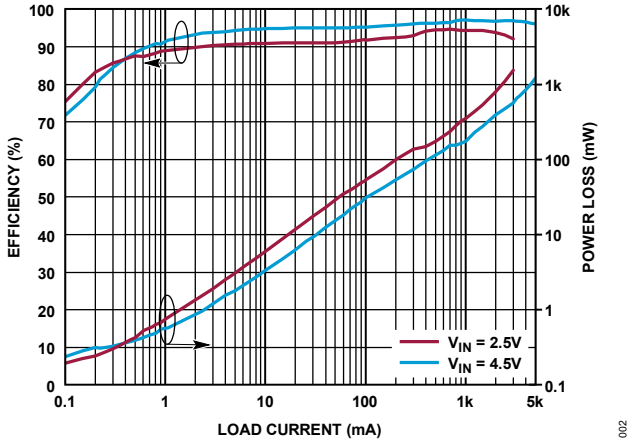

Figure 2. Efficiency and Power Loss (Burst Mode)

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REVISION HISTORY

Nature of Chnage	Page Number
10/2023 - Rev Sp0	—
1/2024 – Rev A, open-market release	—
2/2024 – Updated Electrical Characteristics table, V_{IN} Quiescent Current Units	4

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SPECIFICATIONS

Table 1. Electrical Characteristics

(Specifications are for T_A = 25°C, V_{IN} = 3.6V, $V_{EN/UVLO}$ = 1.5V unless otherwise noted[1].)

PARAMETER	SYMBOL	CONDITIONS/COMMENTS		MIN	TYP	MAX	UNITS
V_{IN} Operating Voltage Range	V_{IN}	–40°C ≤ T_J ≤ 125°C		2.5		5.5	V
V_{IN} Undervoltage Lockout Threshold	$V_{IN\_UVLO\_R}$	Rising			2.36	2.5	V
	$V_{IN\_UVLO\_F}$	Falling		2.1	2.3		
V_{IN} Quiescent Current in Shutdown	I_{Q-SD}	$V_{EN/UVLO}$ ≤ 0.3V			0.5	3	µA
			–40°C ≤ T_J ≤ 125°C		0.5	10	
V_{IN} Quiescent Current	I_Q	SYNC/MODE = 0V, Not Switching			15	30	µA
		SYNC/MODE = Open, FB = 1.5V, RT = 54.9kΩ			11.2	15	mA
V_{OUT} Operating Voltage	V_{OUT}	–40°C ≤ T_J ≤ 125°C				8	V
V_{OUT} Quiescent Current	I_{Q-OUT}	SYNC/MODE = 0V, V_{OUT} = 5.5V, Not Switching			1	2	µA
		SYNC/MODE = Open, VOUT = 2.5V, FB = 1.5V, RT = 54.9kΩ			7.6	12	mA
V_{OUT} Over Voltage Protection Threshold	$V_{OUT\_OV\_R}$	Rising		8.12	9	9.8	V
	$V_{OUT\_OV\_HYS}$	Hysteresis			0.1		
FB Regulation Voltage[3]	V_{FB_REG}	VC=1.25V	–40°C ≤ T_J ≤ 125°C	0.985	1.00	1.015	V
FB Line Regulation[3]		2.5V < V_{IN} < 5.5V			0.2	0.35	%/V
FB Pin Input Current	I_{FB}	FB = 1.0V		-20		20	nA
Error Amp Transconductance[3]	g_m	VC = 1.25V			0.4		mS
Error Amp Gain[3]	G_v				400		V/V
VC Source Current	I_{VC}	FB = 0.8V, VC = 1.25V			-80		µA
VC Sink Current	I_{VC}	FB = 1.2V, VC = 1.25V			73		µA
VC to Switch Current Gain, per phase, no shedding					6.0		A/V
Switching Frequency	f_{SW}	R_T = 464kΩ		0.25	0.3	0.36	MHz
		R_T = 127kΩ		0.82	1	1.2	
		R_T = 54.9kΩ		1.83	2	2.2	
		R_T = 18.7kΩ		3.6	4	4.67	

(Specifications are for T_A = 25°C, V_{IN} = 3.6V, $V_{EN/UVLO}$ = 1.5V unless otherwise noted[1].)

PARAMETER	SYMBOL	CONDITIONS/COMMENTS		MIN	TYP	MAX	UNITS
Spread Spectrum Modulation Frequency as Percentage of f_{SW}		R_T = 54.9kΩ			0.45		%
Spread Spectrum Modulation Frequency Range as Percentage of f_{SW}		R_T = 54.9kΩ			25		%
Synchronizable Frequency	f_{SYNC}	SYNC/MODE = External Clock		0.3		4	MHz
SYNC/MODE Pin Input Logic Level for Frequency Synchronization	V_{SYNC_HIGH}	SYNC Logic Low				0.4	V
	V_{SYNC_LOW}	SYNC Logic High		1.8			
Soft-Start Time	SS	R_T = 54.9kΩ			1.2		ms
EN/UVLO Threshold Voltage	V_{EN_F}	Falling	–40°C ≤ T_J ≤ 125°C	0.94	1.0	1.06	V
	V_{EN_HYS}	Hysteresis			35		mV
EN/UVLO Input Bias Current	I_{EN}	EN/UVLO = 2V		-40		40	nA
Bottom Switch On-Resistance per Phase	$R_{DS\_ON\_BOT}$	I_{SW} = 1A			12		mΩ
Top Switch On-Resistance per Phase	$R_{DS\_ON\_TOP}$	I_{SW} = 1A			13		mΩ
Bottom Switch Current Limit per Phase	I_{SW_LIM}	–40°C ≤ T_J ≤ 125°C		6	7	8	A
Channel 1 Burst Mode Bottom Switch Minimum Peak Current	I_{PK_BURST}	ISET = V_{IN}			1.7		A
		ISET = Open			1.47		
		ISET = 0V			1.23		
Bottom Switch Minimum Off-time	$t_{OFF-MIN}$			20	36	60	ns
Bottom Switch Minimum On-time	t_{ON-MIN}			20	61	90	ns
SW Leakage Current per Phase	I_{SW_LKG}	V_{OUT} = 6.1V, SW = 0V, 6.1V		-1.5		1.5	µA

ABSOLUTE MAXIMUM RATINGS

Table 2. Absolute Maximum Ratings

PARAMETER	RATING
V_{IN}, EN/UVLO, SYNC/MODE, FB, ISET	−0.3V to 6V
V_{OUT}	−0.3V to 10V
VC	−0.3V to 3V
Operating Junction Temperature Range [1, 2]	−40°C to 125°C
Storage Temperature Range	−65°C to 150°C

[1] LT8349 is specified over the −40°C to 125°C operating junction temperature range. High Junction temperatures degrade operating lifetimes. Note the maximum ambient temperature consistent with these specifications is determined by specific operating conditions in conjunction with board layout, the rated package thermal impedance and other environmental factors.

[2] The LT8349 includes overtemperature protection that is intended to protect the device during momentary overload conditions. Junction temperature will exceed 150°C when overtemperature protection is active. Continuous operation above the specified absolute maximum operating junction temperature may impair device reliability.

[3] The LT8349 is tested in a feedback loop which servos VC pin voltage to a specified voltage and measures the resultant FB pin voltage.

Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS

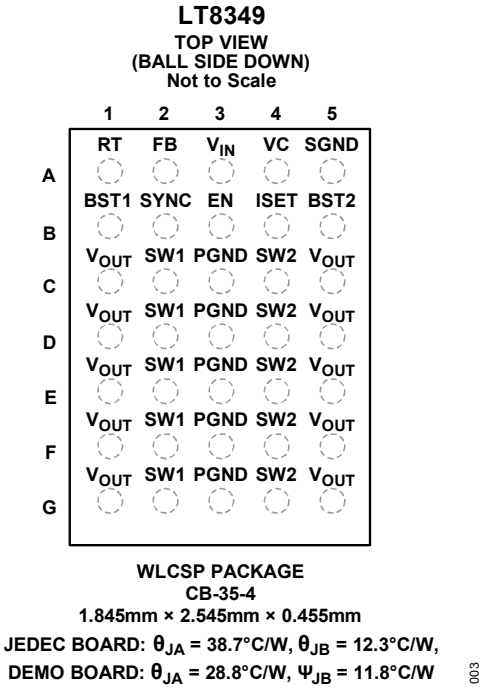


Figure 3. Pin Configuration

Table 3. Pin Descriptions

PIN	NAME	DESCRIPTION
A1	RT	A resistor is tied between RT and SGND to set the switching frequency.
A2	FB	Feedback Input Pin. This pin receives the feedback voltage from the external resistor divider between V_{OUT} and SGND. FB pin is one input to the error amplifier of the output voltage control loop.
A3	V_{IN}	Input Supply Pin. This pin provides supply for internal drivers and control circuits. This pin must be decoupled with a 1µF minimum low ESR ceramic capacitor to the ground plane. Place the V_{IN} bypass capacitor close to the V_{IN} pin.
A4	VC	Error Amplifier Output and Switching Regulator Compensation Pin. Connect this pin to appropriate external components to compensate the regulator loop frequency response.
A5	SGND	Signal Ground. Connect SGND to PGND on the PCB with low impedance.
B1	BST1	This pin is used to provide a gate drive voltage to the top side power switch of channel 1. Place a 0.1µF bootstrap capacitor between BST1 and SW1 pins and close to the IC.
B2	SYNC/MODE	External Synchronization Input and Mode Selection Pin. This pin allows five selectable modes for optimization of performance. Where the selectable modes of operation are: Burst = low I_Q, low output ripple operation at light loads

<table>
<tr><td></td><td></td><td>Forced Continuous = allowing negative inductor current. Not skipping pulse(s) (aligned to clock), fixed switching frequency.
Sync = switching frequency synchronized to half of the SYNC clock frequency.
SSFM = Spread Spectrum Frequency Modulation for low EMI
<table>
<tr><th>SYNC/MODE Pin Input</th><th>Capable Mode(s) of Operations</th></tr>
<tr><td>SGND or <0.1V</td><td>Burst</td></tr>
<tr><td>50kΩ Resistor to SGND</td><td>Burst + SSFM</td></tr>
<tr><td>Float (Pin Open)</td><td>Forced Continuous</td></tr>
<tr><td>V_{IN}</td><td>Forced Continuous + SSFM</td></tr>
<tr><td>External Clock</td><td>Forced Continuous + Sync Clock</td></tr>
</table></td></tr>
<tr><td>B3</td><td>EN/UVLO</td><td>Enable and Input Undervoltage Lockout Pin. The IC is shut down when this pin is below 1V (typical). The IC draws a low V_{IN} current of 0.5µA (typical) when this pin is below 0.15V. The IC is enabled when this pin is above 1.035V (typical). A resistor divider from V_{IN} to SGND can be used to program a V_{IN} threshold below which the IC is shut down. Tie EN/UVLO to V_{IN} if the shutdown and UVLO features are not used.</td></tr>
<tr><td>B4</td><td>ISET</td><td>Channel 1 Burst Mode Bottom Switch Minimum Peak Current Adjust Input. This pin allows three selectable burst mode peak current (I_{PK_BURST}) levels for optimization of performance.
<table>
<tr><th>ISET Pin Setting</th><th>Burst Mode Peak Current (I_{PK_BURST}) (typ)</th></tr>
<tr><td>V_{IN}</td><td>1.7A</td></tr>
<tr><td>Float (Pin Open)</td><td>1.47A</td></tr>
<tr><td>SGND or < 0.4V</td><td>1.23A</td></tr>
</table></td></tr>
<tr><td>B5</td><td>BST2</td><td>This pin is used to provide a gate drive voltage to the top side power switch of channel 2. Place a 0.1µF bootstrap capacitor between BST2 and SW2 pins and close to the IC.</td></tr>
<tr><td>C1, D1, E1, F1, G1, C5, D5, E5, F5, G5</td><td>V_{OUT}</td><td>Boost Converter Output Pins. Connect both rows of V_{OUT} pins together on the PCB. Bypass this pin to ground plane with low ESR ceramic capacitors. Place the capacitors as close to the pins as possible. See the Applications Information section for a sample layout.</td></tr>
<tr><td>C2, D2, E2, F2, G2</td><td>SW1</td><td>The SW1 pins are the switching nodes of phase 1 internal power switches. Tie these pins together and connect them to the phase 1 inductor and bootstrap capacitor. These nodes should be kept small on the PCB for good EMI performance.</td></tr>
<tr><td>C3, D3, E3, F3, G3</td><td>PGND</td><td>Power Ground.</td></tr>
<tr><td>C4, D4, E4, F4, G4</td><td>SW2</td><td>The SW2 pins are the switching nodes of the phase 2 internal power switches. Tie these pins together and connect them to the phase 2 inductor and bootstrap capacitor. These nodes should be kept small on the PCB for good EMI performance.</td></tr>
</table>

TYPICAL PERFORMANCE CHARACTERISTICS

T_A = 25°C, unless otherwise noted.

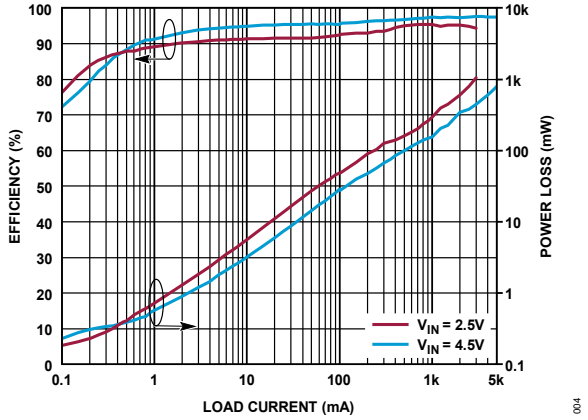


Figure 4. Efficiency and Power Loss vs Output Current (Burst Mode) (Reference to Page 26 Circuit)

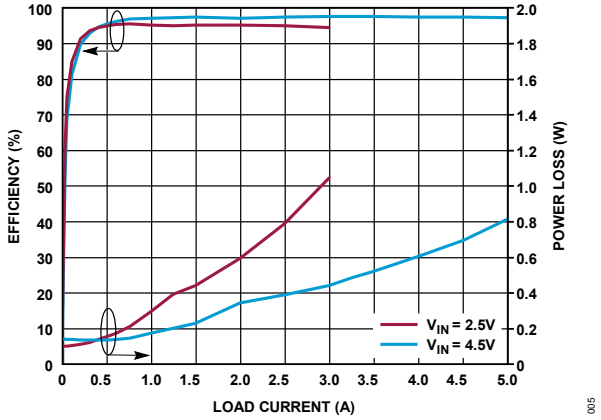


Figure 5. Efficiency and Power Loss vs Output Current (FCM Mode) (Reference to Page 26 Circuit)

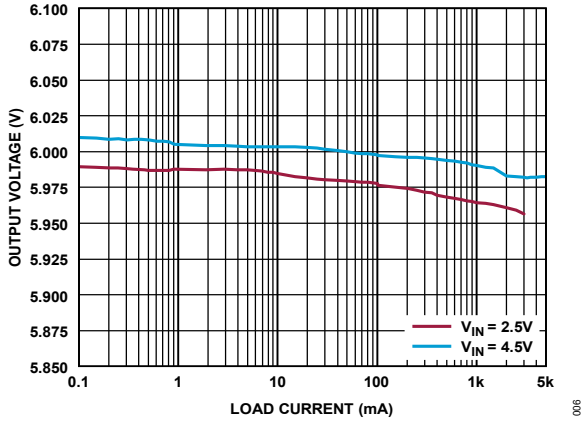


Figure 6. Output Voltage vs Output Current (Burst Mode) (Reference to Page 26 Circuit)

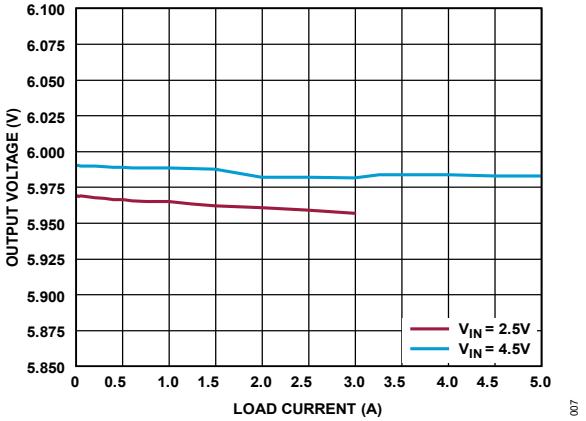


Figure 7. Output Voltage vs Output Current (FCM Mode) (Reference to Page 26 Circuit)

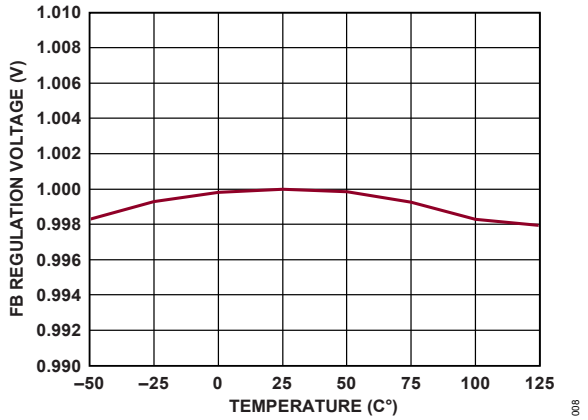


Figure 8. FB Regulation Voltage vs Temperature

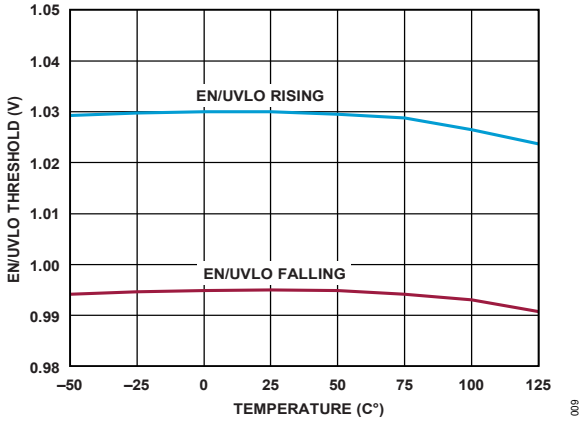


Figure 9. EN/UVLO Thresholds vs Temperature

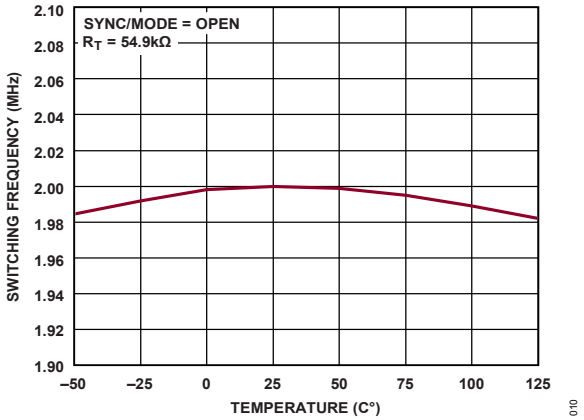


Figure 10.Switching Frequency vs Temperature

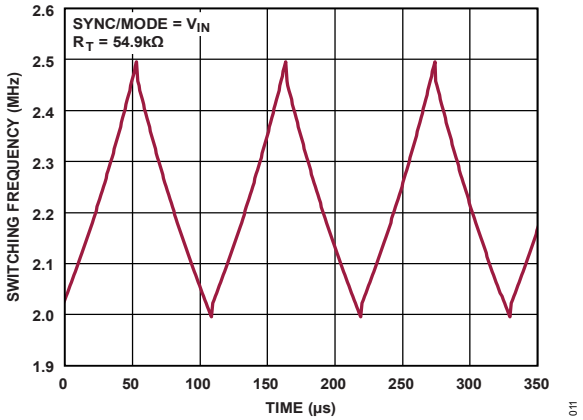


Figure 11.Switching Frequency with Spread Spectrum Modulation

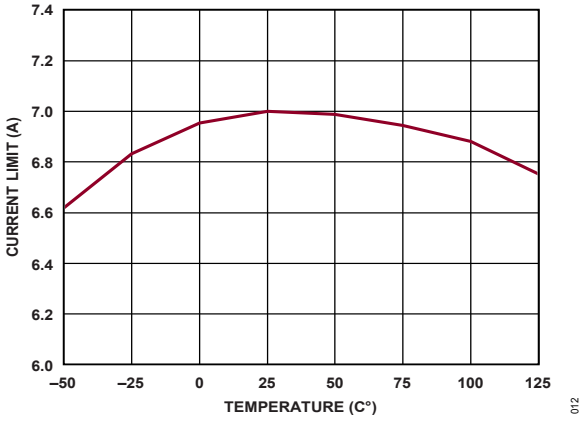


Figure 12.Bottom Switch Current Limit vs Temperature (Both channels)

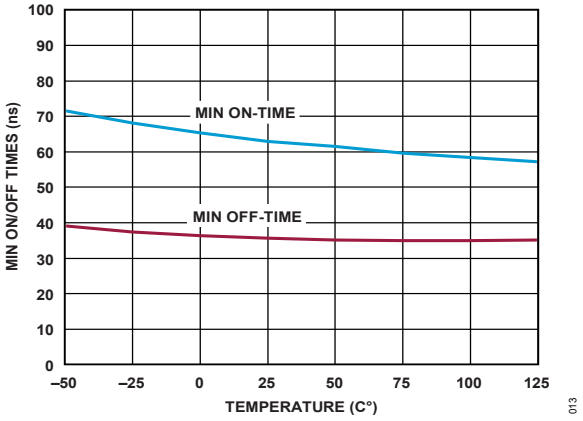


Figure 13.Bottom Switch Min. On/Off Times vs Temperature (Both Channels)

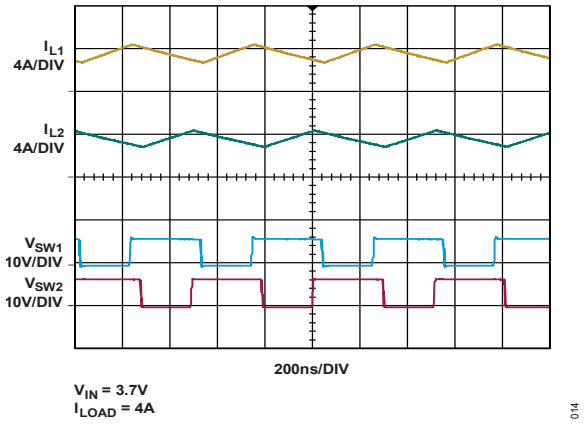


Figure 14.Switching Waveforms, Heavy Load 2-Phase Operation (Reference to Page 26 Circuit)

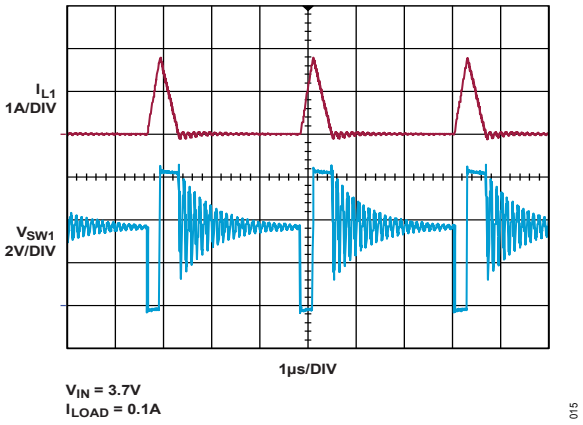


Figure 15.Switching Waveforms, Light Load 1-Phase Burst Mode Operation (Reference to Page 26 Circuit)

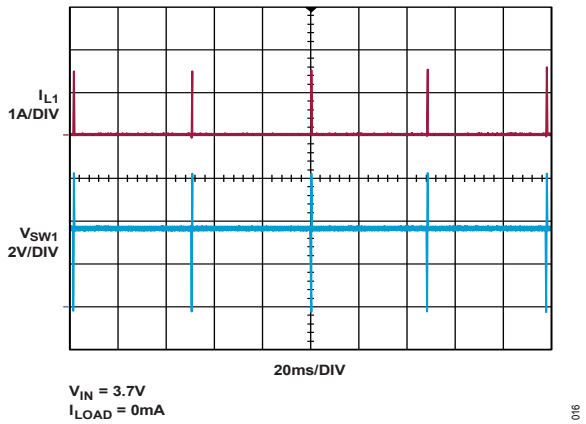


Figure 16.Switching Waveforms, Zero Load 1-Phase Burst Mode Operation (Reference to Page 26 Circuit)

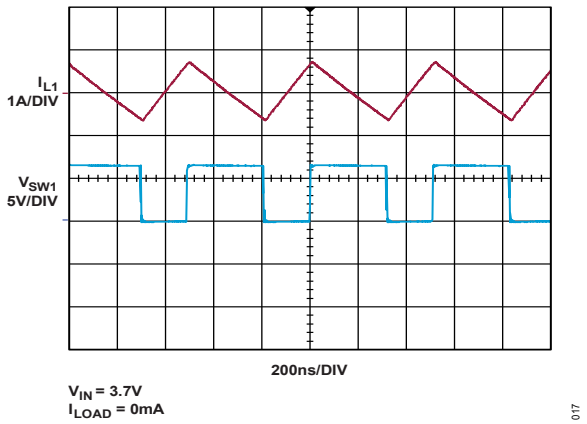


Figure 17. Switching Waveforms, Zero Load 1-Phase FCM Operation (Reference to Page 26 Circuit)

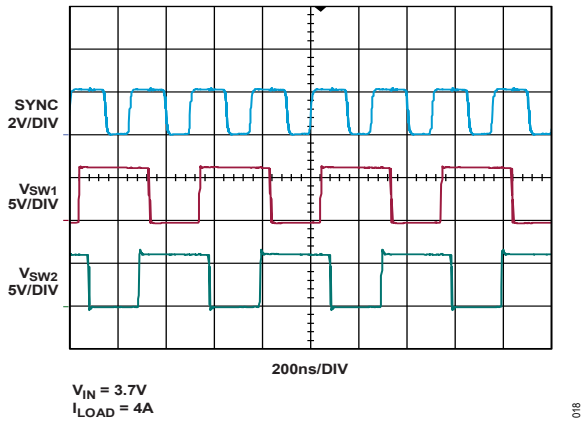


Figure 18. Switching Waveforms, Heavy Load 2-Phase Operation with SYNC (Reference to Page 26 Circuit)

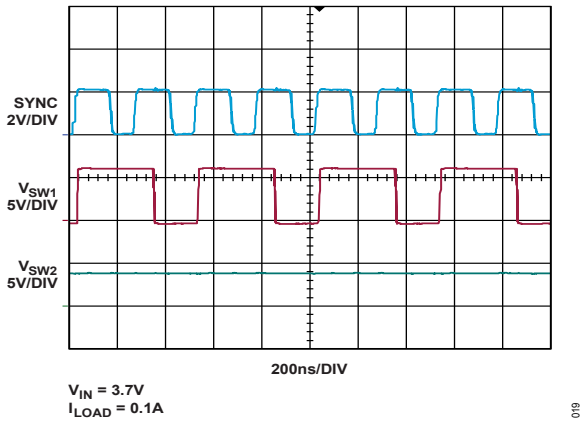


Figure 19. Switching Waveforms, Light Load 1-Phase Operation with SYNC (Reference to Page 26 Circuit)

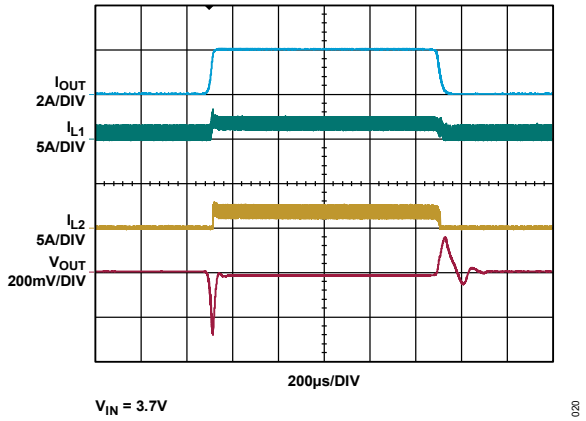


Figure 20. Transient Response Burst Mode Operation (Reference to Page 26 Circuit)

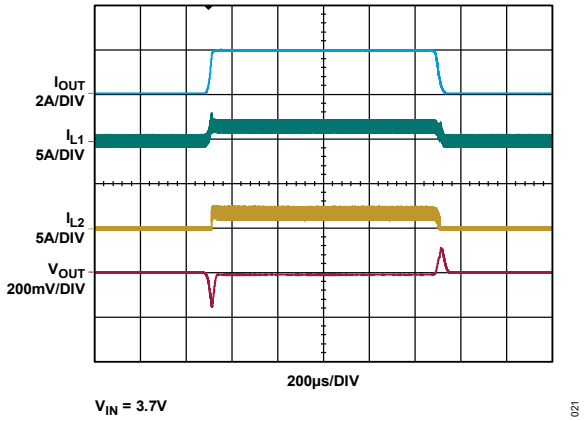


Figure 21. Transient Response FCM Mode Operation (Reference to Page 26 Circuit)

BLOCK DIAGRAM

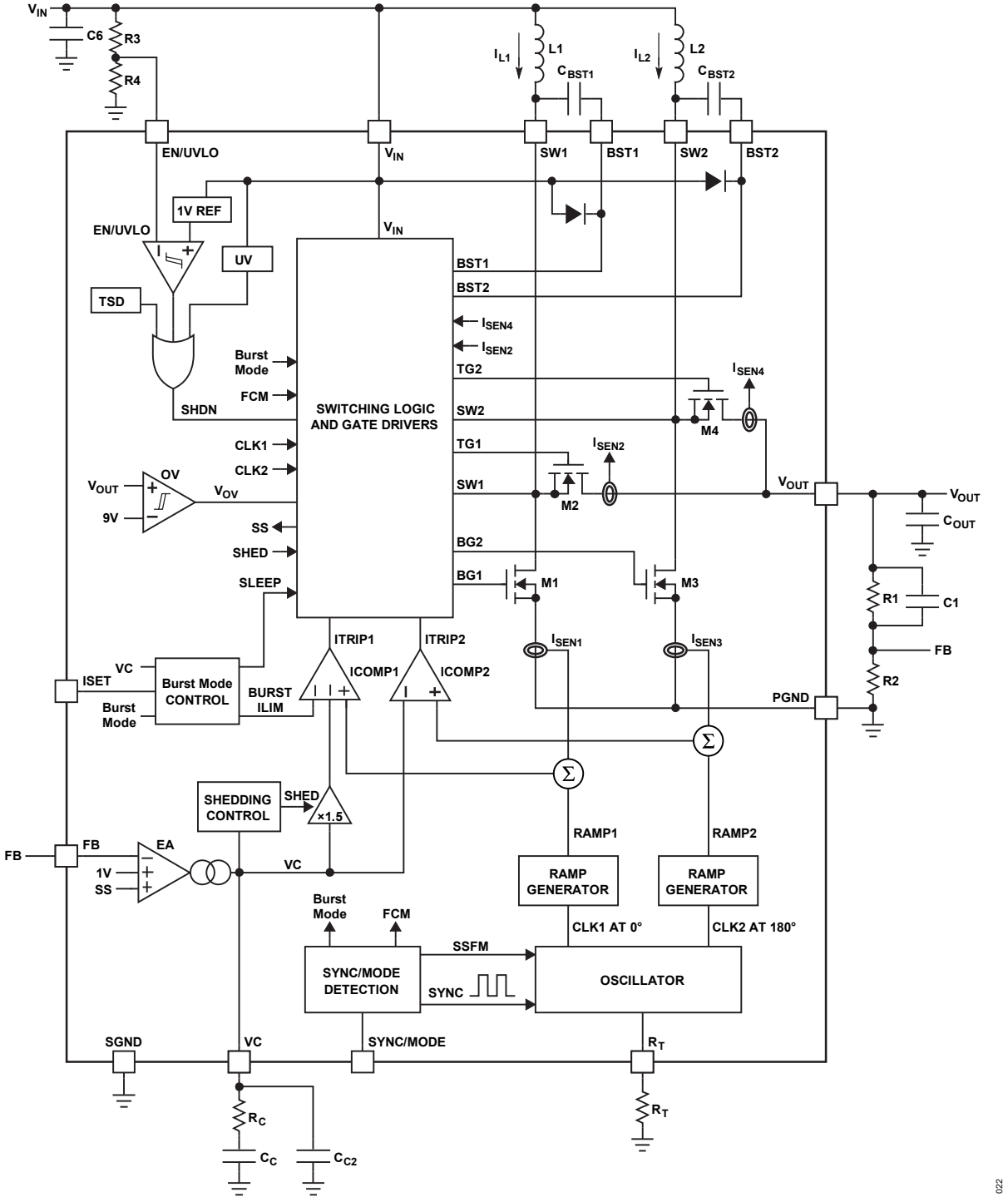


Figure 22. Block Diagram

THEORY OF OPERATION

The LT8349 is a dual-phase, adjustable frequency synchronous boost converter. Referring to the Block Diagram, the LT8349 uses a fixed frequency, current mode control scheme to provide excellent line and load regulation. The Switching Logic and Gate Drivers block turns on channel 1's power switch M1 at the start of each CLK1 cycle and turns on channel 2's power switch M3 at the start of each CLK2 cycle. CLK1 and CLK2 are 180° out-of-phase, generated by the Oscillator. During the M1 switch on-phase, the inductor current I_{L1} flows through M1. A signal I_{SEN1} proportional to the M1 switch current is added to a stabilizing slope compensation ramp RAMP1 and the resulting sum is fed into the positive terminal of the PWM comparator ICOMP1. The voltage at the negative input of ICOMP1, labeled "VC", is set by the error amplifier EA and is an amplified version of the difference between the feedback voltage FB and the reference voltage (1V). During the M1 on-phase, I_{L1} increases. When the signal at the positive input of ICOMP1 exceeds VC, ICOMP1 sends out a signal ITRIP1 to the Switching Logic and Gate Drivers block to turn off M1. When M1 turns off, the synchronous power switch M2 turns on until the next CLK1 cycle begins or inductor current I_{L1} falls to zero (in Burst Mode operation only). During the M1 off-phase and the M2 on-phase, I_{L1} decreases. Channel 2 operation follows Channel 1. I_{L1} and I_{L2} are designed to match each other (except they are 180° out-of-phase). Through this repetitive action, the EA sets the correct I_{L1} and I_{L2} peak current level to keep the V_{OUT} in regulation.

Multiphase Operation

The LT8349 uses a dual-phase architecture with two phases equally spaced 180° apart, rather than the conventional single phase of other boost converters. Although this architecture requires two inductors, rather than a single inductor, there are several important advantages.

- Substantially lower peak inductor current allows the use of smaller inductors.
- Significantly reduced output ripple current minimizes output capacitance requirement.
- Higher frequency output ripple is easier to filter for low noise applications.
- Input ripple current is reduced for lower noise on V_{IN}.

The peak inductor current, reduced nearly by a factor of 2 compared to a single-phase boost converter, is given by:

$$I_{LPEAK} \cong \frac{1}{2} \bullet \frac{I_O}{1 - D} + \frac{\Delta I_L}{2}$$

where I_O is the average load current, D is the PWM duty cycle, and ΔI_L is the inductor ripple current. With 2-phase operation, one of the phases is always delivering current to the load whenever V_{IN} is greater than one-half V_{OUT} (duty cycles less than 50%). As the duty cycle decreases further, load current delivery between the two phases begins to overlap, occurring simultaneously for a growing portion of each phase as the duty cycle approaches zero. This significantly reduces both the output ripple current and the peak current in each inductor, when compared with a single-phase converter. The comparison of output ripple current with single phase and dual phase boost converter operating at 50% duty cycle is shown graphically in *Figure 23*.

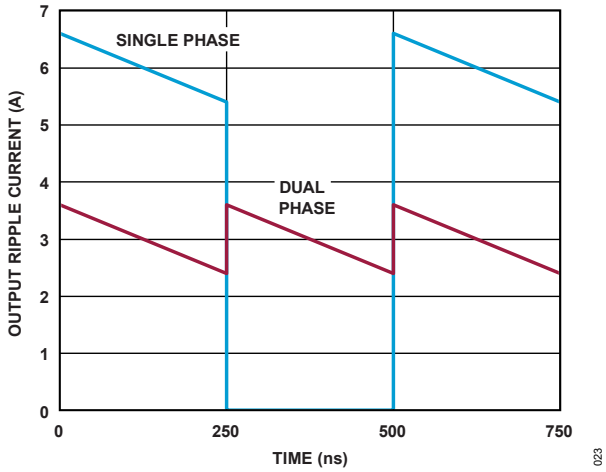


Figure 23. Comparison of Output Ripple Current with Single Phase and Dual Phase Boost Converter in a 3A Load Application Operating at 50% Duty Cycle

APPLICATIONS INFORMATION

Programming V_{IN} Turn-On and Turn-Off Thresholds with the EN/UVLO Pin

The EN/UVLO pin controls whether the LT8349 is enabled or is in shutdown state. A 1.0V reference and a comparator EN with 35mV hysteresis (Block Diagram) allow the user to accurately program the supply voltage at which the IC turns on and off. The falling threshold voltage and rising hysteresis voltage of the V_{IN} pin can be calculated by the following equations:

$$V_{VIN,FALLING} = 1V \bullet \frac{(R3 + R4)}{R4}$$

$$V_{VIN,RISING} = 35mV \bullet \frac{(R3 + R4)}{R4} + V_{VIN,FALLING}$$

When in Burst Mode operation with light load currents, the current through the resistor network R3 and R4 can easily be greater than the supply current consumed by the IC. Therefore, large resistors can be used for R3 and R4 to minimize their effect on efficiency at light loads. EN/UVLO pin can be tied to V_{IN} if the shutdown feature is not used, or alternatively, the pin may be tied to a logic level if shutdown control is required. The IC draws a low V_{IN} quiescent current of 0.5µA (typical) when EN/UVLO is below 0.15V.

Light Load Current Operation

The LT8349 features 2-phase with 180° out-of-phase operation at heavy loads. The LT8349 reduces to 1- phase operation (Stage Shedding operation) to enhance the efficiency at light loads. At very light loads, the LT8349 features selectable 1-phase low ripple Burst Mode operation or 1-phase Forced Continuous operation. *Figure 24* shows the simplified drawings of the LT8349 operations as the load current decreases from high current to very low current gradually. *Figure 24a* shows the load current. *Figure 24b* shows the I_{L1} and I_{L2} currents when Burst Mode operation is selected by SYNC/MODE pin. As shown in *Figure 24b*, LT8349 operates in 2-phase operation at heavy load. In 2-phase operation, the inductor peak current of each channel matches each other. As each inductor peak current of 2-phase operation reduces to the phase shedding threshold $I_{SHED,DUAL}$ (approximately 1.7A), the channel 2 is turned off (I_{L2} is kept to 0A), and LT8349 operates in 1-phase operation. At the same time, the current gain of channel 1 is increased by approximately 1.5 times to ensure a smooth transition, resulting in channel 1 inductor peak current phase shedding threshold in 1-phase operation ($I_{SHED,SINGLE}$) increasing by 1.5 (plus hysteresis 0.35A typ.) times:

$$I_{SHED,SINGLE} \approx (I_{SHED,DUAL} + 0.35A) \bullet 1.5$$

As the load current is further decreased, the channel 1 bottom switch minimum peak current (same as the inductor minimum peak current) is set to I_{BURST}, which is programmed by ISET pin, even though the VC node (Block Diagram) indicates a lower value. In this condition, the LT8349 maintains the output regulation voltage by reducing the switching frequency instead of reducing the inductor peak current. The LT8349 delivers single pulses of current to the output capacitor followed by sleep periods (*Figure 24b*) during which most of the internal circuits are turned off and the output power is supplied by the output capacitor. This low ripple Burst Mode operation minimizes the input quiescent current and minimizes output voltage ripple. As the output load decreases, the frequency of single current pulses decreases and the percentage of time the LT8349 is in sleep mode increases, resulting in much higher light load efficiency than for typical converters. By maximizing the time between pulses, the converter V_{IN} pin quiescent current approaches 15µA for a typical application when there is no output load. To optimize the quiescent current performance at light loads, the current in the feedback resistor divider should be minimized as it appears to the output as load current.

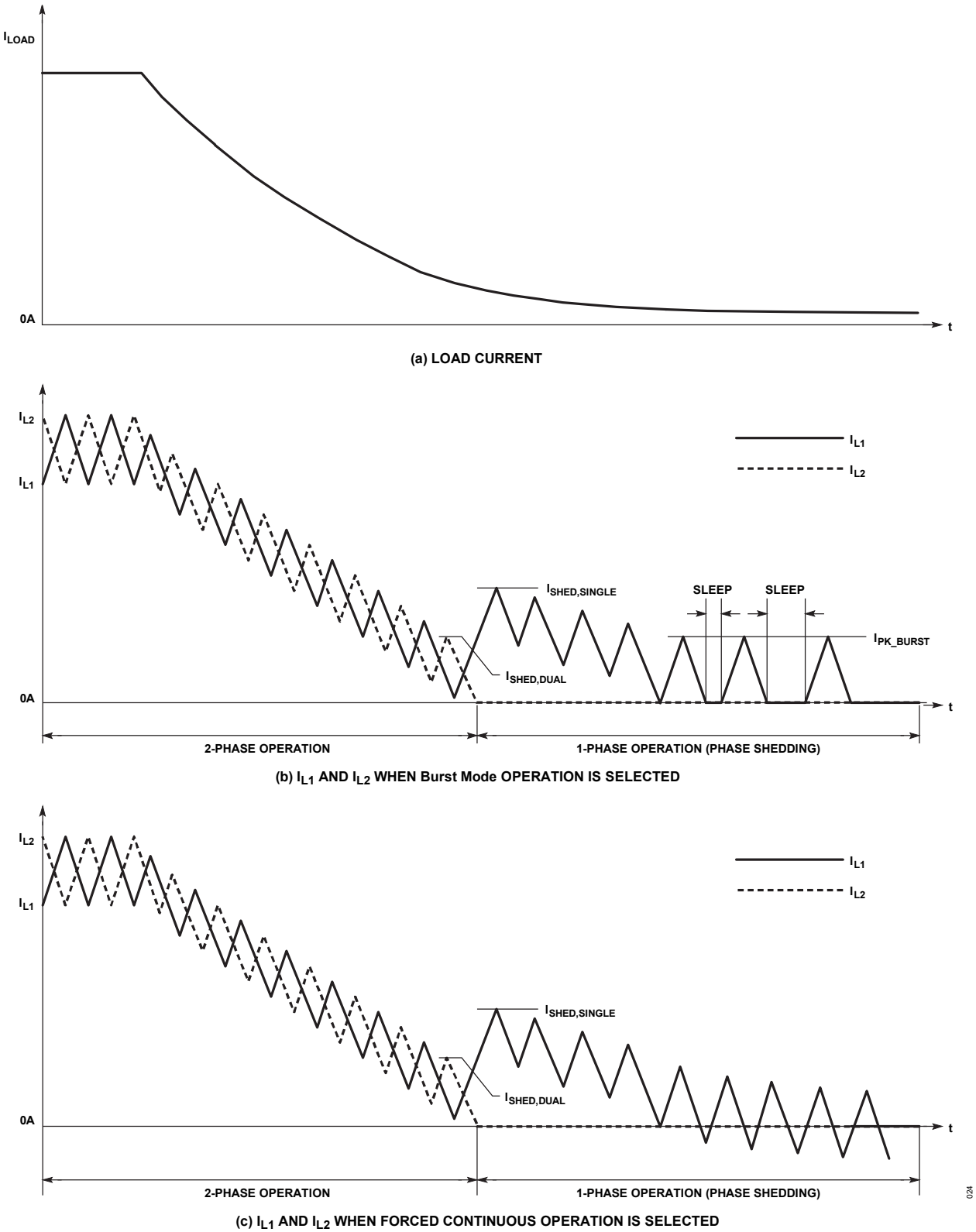


Figure 24. Simplified Drawings of LT8349 operations as the load current decreases from high current to very low current

In order to achieve higher light load efficiency, more energy should be delivered to the output during the single pulses in Burst Mode operation such that the LT8349 can stay in sleep mode longer between each pulse. This can be achieved by selecting a higher I_{BURST} current by the ISET pin (Pin Functions section). The light load efficiency can be further increased by using larger value inductors. The tradeoff is that while more energy is delivered to the output by the single pulses, the output voltage ripple will be larger at light load. However, the output voltage ripple can be reduced proportionally by increasing the output capacitance. When adjusting inductor and/or output capacitor values, a careful evaluation of system stability should be made to ensure adequate design margin. Larger inductors and/or output capacitors also increase cost and solution sizes.

Figure 24c shows the I_{L1} and I_{L2} currents when Forced Continuous operation (FCM) is selected by SYNC/MODE pin. As shown in *Figure 24c*, at light load the I_{L2} is kept to 0A and the I_{L1} is allowed to go negative so that the regulator can switch at the programmed frequency all the way down to zero output current. This has the advantage of maintaining the programmed switching frequency across the entire load range so that the switch harmonics and EMI are consistent and predictable. The disadvantage of FCM is that the light load efficiency will be lower compared to Burst Mode operation.

Switching Frequency and Synchronization

The choice of switching frequency is a trade-off between efficiency and component size. Low frequency operation improves efficiency by reducing the power switches' switching losses and gate drive current. However, lower frequency operation requires a physically larger inductor. The LT8349 uses a constant-frequency architecture that can be programmed over a 300kHz to 4MHz range with a single external resistor from the RT pin to ground, as shown in Block Diagram. A table for selecting the value of R_T for a given switching frequency is shown in *Table 4*. *Figure 25* shows the R_T Value vs Switching Frequency curve.

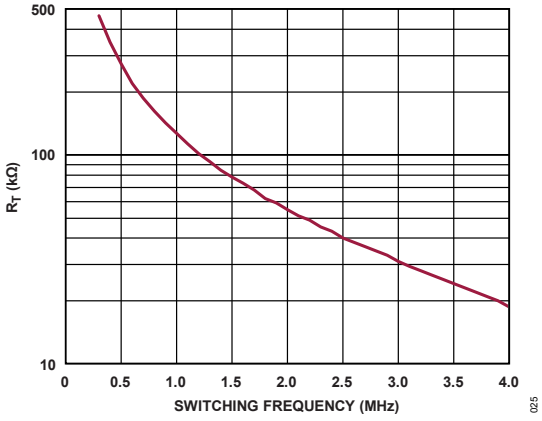


Figure 25. R_T Value vs Switching Frequency

Table 4. SW Frequency (f_{SW}) vs R_T Value

f_{SW} (MHz)	R_T (kΩ)	f_{SW} (MHz)	R_T (kΩ)
0.3	464	2.2	48.7
0.4	348	2.3	45.2
0.5	274	2.4	43.2
0.6	221	2.5	40.2
0.7	187	2.6	38.3
0.8	162	2.7	36.5
0.9	143	2.8	34.8

1.0	127	2.9	33.2
1.1	113	3.0	30.9
1.2	102	3.1	29.4
1.3	93.1	3.2	28.0
1.4	84.5	3.3	26.7
1.5	78.7	3.4	25.5
1.6	73.2	3.5	24.3
1.7	68.1	3.6	23.2
1.8	61.9	3.7	22.1
1.9	59.0	3.8	21.0
2.0	54.9	3.9	20.0
2.1	51.1	4.0	18.7

The operating frequency of the LT8349 can be synchronized to an external clock source with 100ns minimum pulse width. *Figure 26* shows the external clock threshold (typ) required at the SYNC pin for synchronization.

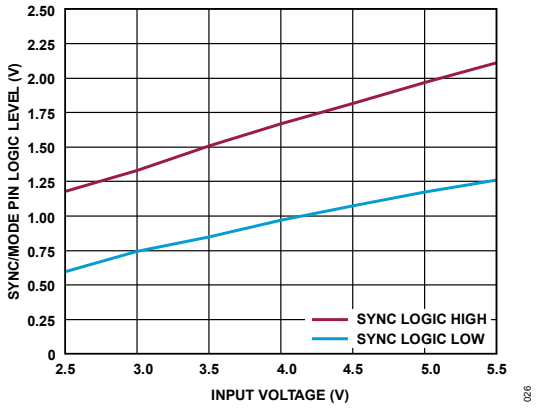


Figure 26. Sync/Mode Pin Logic Level (typ) vs Input Voltage

By providing a digital clock signal to the SYNC/MODE pin, the IC operates at the half of the SYNC clock frequency and automatically enters FCM operation at light load. While in FCM the oscillator operates continuously, and the falling SW1 and SW2 transitions are aligned to the rising edges of the clock alternatively (180° out-of-phase), with a delay time of 80ns (typical). *Figure 27* shows the synchronization between the SYNC/MODE pin input clock and the SW1 and SW2 transitions. If this feature is used, an R_T resistor should be chosen to program switching frequency as close as possible to the SYNC pulse frequency.

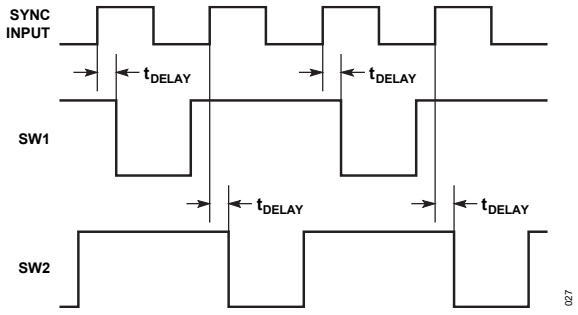


Figure 27. The synchronization between the SYNC/MODE pin input clock and the SW1 and SW2 transitions

Spread Spectrum Frequency Modulation

The LT8349 features spread spectrum frequency modulation to further reduce EMI emissions. The user can select spread spectrum frequency modulation with Burst Mode operation by connecting the SYNC/MODE pin to ground through a 50k resistor or spread spectrum frequency modulation with FCM operation by connecting the SYNC/MODE pin to V_{IN} pin. When spectrum frequency modulation is selected, a stepped triangular frequency modulation is used to vary the internal oscillator frequency between the value programmed by the R_T resistor to approximately 25% (at Fsw_set = 2MHz) higher than that value. Figure 28 shows spread spectrum depth (typ) variation with switching frequency. The modulation frequency is approximately 0.45% of the switching frequency. For example, when the LT8349 is programmed to 2MHz, and spread spectrum frequency modulation is selected, the oscillator frequency varies from 2MHz to 2.5MHz at a 9kHz rate (see Oscillator Frequency with Spread Spectrum Modulation curve in the Typical Performance Characteristics section). When operating at light load, the spread spectrum frequency modulation is more effective in FCM mode than in Burst Mode operation, due to the fact that FCM operation maintains the programmed switching frequency across entire load current range.

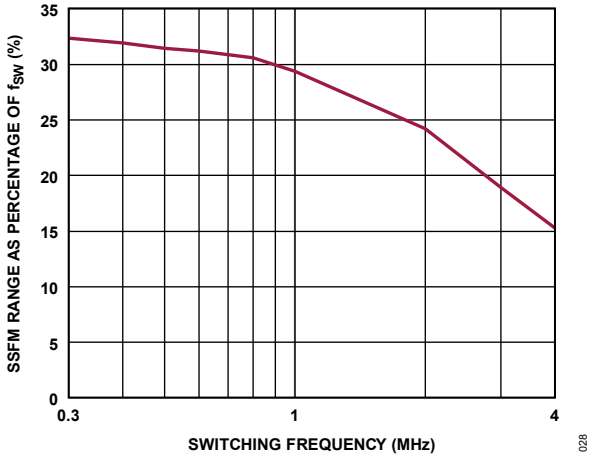


Figure 28. SSFM Range as Percentage of Fsw (typ) vs. Switching Frequency

FB Resistor Network and the Quiescent Current at No Load

The output voltage is programmed with a resistor divider between the output and the FB pin. Choose the resistor values according to the following equation:

$$R1 = R2 \bullet \left(\frac{V_{OUT}}{1V} - 1\right)$$

Reference designators refer to Block Diagram. The 1% resistors are recommended to maintain output voltage accuracy. If low input quiescent current and good light-load efficiency are desired, use large resistor values for the FB resistor divider. The current flowing in the divider acts as a load current and will increase the no load input current to the converter. The LT8349 converter Burst Mode quiescent current at no load can be estimated using the following Equation:

$$I_Q \approx 15\mu A + \left(\frac{V_{OUT}}{R1 + R2} + 1\mu A\right) \bullet \frac{V_{OUT}}{V_{IN}} \bullet 3$$

where 15µA is the V_{IN} pin quiescent current of the LT8349, and the second term is the current drawn by the feedback divider and V_{OUT} pin (1µA) reflected to the input of the boost operating. For a 3.7V input, 6V output boost converter with R1 = 1MΩ and R2 = 200kΩ, it can be calculated that the LT8349 converter draws approximately 45µA from the supply at no load.

When using large FB resistors, a 4.7pF to 22pF phase-lead capacitor should be connected from V_{OUT} to FB, and a careful evaluation of system stability should be made to ensure adequate design margin.

Overvoltage Lockout

The V_{OUT} pin voltage is constantly monitored by the LT8349. An overvoltage condition occurs when V_{OUT} pin voltage exceeds approximately 9V. Switching is stopped at such condition. Normal switching is resumed when the V_{OUT} pin voltage drops back to 8.9V or lower.

Start-Up

To limit the peak switch current and V_{OUT} overshoot during start-up, the LT8349 contains internal circuitry to provide soft-start operation (refer to the error amplifier EA in Block Diagram). During start-up, the internal soft-start circuity slowly ramps the internal SS signal from zero to 1V. When the SS voltage falls between the FB initial voltage and 1V, the LT8349 regulates the FB pin voltage to the SS voltage instead of 1V. In this way the output capacitor is charged gradually towards its final value while limiting the start-up peak switch currents.

Referring to *Figure 29*, the start-up time T_{START_UP} is the time period from EN/UVLO transitioning high to V_{OUT} having reached 90% of its regulation voltage programmed by FB resistor network. T_{START_UP} is approximately given by Equation:

$$T_{START\_UP} \approx 0.15ms + \frac{3.6V}{V_{IN} - 0.1V} \bullet \frac{2100}{f_{SW}}$$

The LT8349 selects fixed frequency operaton with no spread spectrum frequency modulation during startup, and the SYNC/MODE pin configuration is ignored.

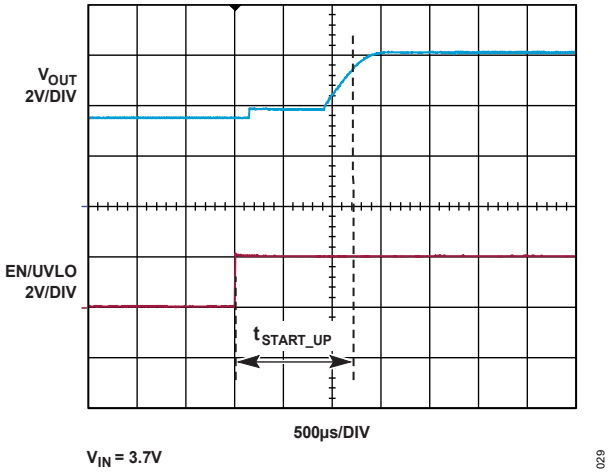


Figure 29. Typical Start-Up Waveforms

If the LT8349 boost converter is plugged into a live supply, the V_{OUT} could ring to twice the voltage of V_{IN}, due to the resonant circuit composed by L1, L2, C_{OUT}, and the body diode of M2 and M4 (refer to Block Diagram). If such over-shoot exceeds the V_{OUT} rating, it must be limited to protect the load and the converter. For these situations, a small Schottky diode or silicon diode can be connected between V_{IN} and V_{OUT} to deactivate the resonant circuit and limit the V_{OUT} over-shoot as shown in *Figure 30*. With the diode connected, the boost is also more robust against output fault conditions such as output short circuit or overload, due to the fact that the diode diverts a great amount of output current from the IC. D should be rated for short circuit current of V_{IN} source, example - the current limit of the input side battery or voltage source.

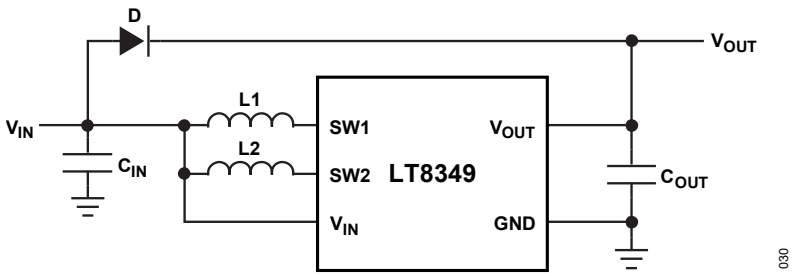


Figure 30. A Simplified LT8349 Power Stage with a Diode Added Between V_{IN} and V_{OUT}

Inductor Selection

When operating in continuous conduction mode (CCM), the duty cycle can be calculated based on the output voltage (V_{OUT}) and the input voltage (V_{IN}). The maximum duty cycle (D_{MAX})occurs when the converter has the minimum input voltage:

$$D_{MAX} = \frac{V_{OUT} - V_{IN(MIN)}}{V_{OUT}}$$

Discontinuous conduction mode (DCM) provides higher conversion ratios at a given frequency at the cost of reduced efficiencies and higher switching currents.

The ripple current ΔI_{SW} of each inductor has a direct effect on the choice of the inductor value, the converter's maximum output current capability, and the light load efficiency in Burst Mode operation. Choosing smaller values of ΔI_{SW} increases output current capability and improves light load efficiency in Burst Mode operation, but require large inductance values and reduce the current loop gain. Accepting larger values of ΔI_{SW} provides fast transient response and allows the use of low inductance values, but results in higher input current ripple, greater core losses, lower light load efficiency in Burst Mode operation, and lower output current capability. Large values of ΔI_{SW} at high duty cycle operation may result in sub-harmonic oscillation. ΔI_{SW} = 1.2A to 2A generally provides a good starting value for many applications, and careful evaluation of system stability should be made to ensure adequate design margin.

Given an operating input voltage range, and having chosen the operating frequency and ripple current in each of the inductors, each inductor value of the boost converter can be determined using the following Equation:

$$L1 = L2 = \frac{V_{IN(MIN)}}{\Delta I_{SW} \bullet f_{SW}} \bullet D_{MAX}$$

The peak current of each inductor is equal to the LT8349 bottom switch current limit as given in the Electrical Characteristics table. The user should choose an inductor with sufficient saturation and RMS current ratings to handle the inductor's peak current.

Input Capacitor Selection

The input ripple current in a boost converter is relatively low (compared with the output ripple current), because this current is continuous. The value of C_{IN} is a function of the source impedance, and in general, the higher the source impedance, the higher the required input capacitance. The RMS C_{IN} ripple current can be estimated by the following equation:

$$I_{RMS(CIN)} = 0.3 \bullet \Delta I_L$$

Output Capacitor Selection

The output capacitor has two essential functions. First, it filters the LT8349's discontinuous top switch current to produce the DC output. In this role, it determines the output ripple, thus low impedance at the switching frequency is important. The second function is to store energy in order to satisfy transient loads and stabilize the IC's control loop. The X5R or X7R type ceramic capacitors have very low equivalent series resistance (ESR), which provides low output ripple and good transient response. Transient performance can be improved with higher output capacitance and the addition of a feedforward capacitor placed between V_{OUT} and FB. When a feedforward capacitor is used or output capacitance is adjusted, a careful evaluation of system stability should be made to ensure adequate design margin. Increasing the output capacitance will also decrease the output voltage ripple. Lower value of output capacitance can be used to save space and cost, but transient performance will suffer, and may result in loop instability.

If there is significant inductance to the load due to long wires or cables, additional bulk capacitance may be necessary. This can be provided with an electrolytic capacitor When choosing a capacitor, special attention should be given to capacitor's data sheet to calculate the effective capacitance under the relevant operating conditions of voltage bias and temperature

Frequency Compensation

The LT8349 has a VC pin which can be used to optimize the loop compensation. Designing the compensation network is a bit complicated and the best values depend on the application and in particular the type of output capacitor. A practical approach is to start with one of the circuits in the data sheet that is similar to your application and tune the compensation network to optimize the performance. LTspice® simulations can help in this process. Stability should then be checked across all operating conditions, including load current, input voltage, and temperature.

Figure 31 shows a simplified circuit for the LT8349 control loop. The error amplifier is a transconductance amplifier (g_m) generating output current I_{VC} proportional to the voltage at FB pin. The two power sections, each consisting of a power stage and an inductor, is modeled as a transconductance amplifier (gm1 or gm2) generating output current (I_{OUT1} or I_{OUT2}) proportional to the voltage at the VC pin. Note that the output capacitor C_{OUT} integrates I_{OUT1} and I_{OUT2}, and that the capacitor on the VC pin (C_C) integrates the error amplifier output current I_{VC}, resulting in two poles in the loop. A zero is required and comes from a resistor R_C in series with C_C. This simple model works well as long as the value of the inductor is not too high, and the loop crossover frequency is much lower than the switching frequency. A small capacitor C_{C2} can be added to filter the switching noise that is coupled on the VC pin. A phase lead capacitor C1 across R1 in the feedback divider can be used to improve the transient response and is required to cancel the parasitic pole caused by the feedback node to ground capacitance.

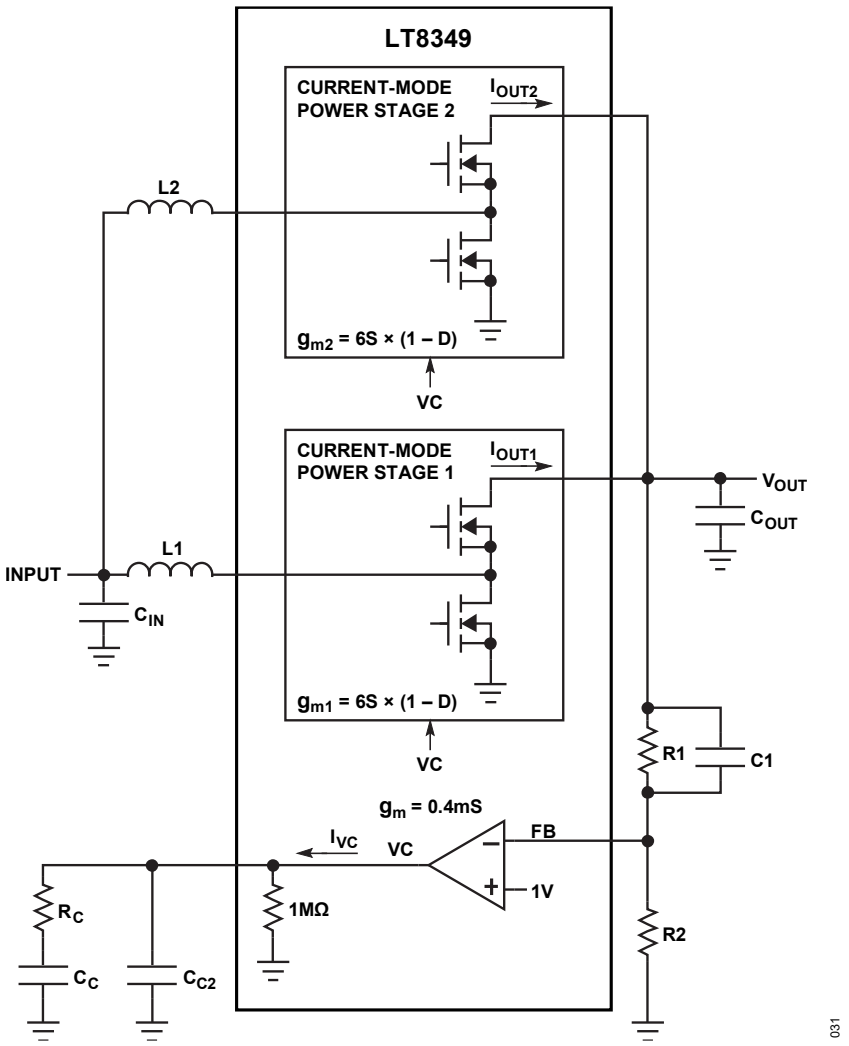


Figure 31. Simplified Model for Loop Response

Board Layout

The LT8349 is specifically designed to minimize the electromagnetic interference (EMI) emissions and to maximize efficiency when switching at high frequencies. *Figure 32* shows a recommended PCB layout (simplified) for LT8349 (circuits connected SYNC, EN, and ISET are not shown). For more detail and PCB design files refer to the evaluation board user guide for the LT8349.

To prevent radiation and high frequency resonance problems, proper layout of the components connected to the IC is essential, especially the power paths with higher di/dt. Refer to *Figure 32,* the following high di/dt loops should be kept as tight as possible to reduce inductive ringing and EMI emissions.

- The high di/dt loop of channel 1 is formed by the positive terminal of C_{OUT1}, LT8349's (C-G)1 pins, LT8349's PGND pins, and the negative terminal of C_{OUT1}.
- The high di/dt loop of channel 2 is formed by the positive terminal of C_{OUT2}, LT8349's (C-G)4 pins, LT8349's PGND pins, and the negative terminal of C_{OUT2}.

The output capacitors, along with the inductors and input capacitors, should be placed on the same side of the circuit board, and their connections should be made on that layer. It is recommended to make the layout identical between the two channels to improve the current sharing (refer to *Figure 32*).

Place a local, unbroken power ground plane under the application circuit on the layer closest to the surface layer. The SW1, SW2, BST1 and BST2 nodes should be as small as possible. Keep the FB and RT nodes small so that the ground traces will shield them from the noise generated by the SW1, SW2, BST1 and BST2 nodes.

To keep the thermal resistance low, extend the ground plane as much as possible, and add many thermal vias to additional power ground planes within the circuit board.

Thermal Considerations

Care should be taken in the layout of the PCB to ensure good heat sinking of the LT8349. The power ground plane should consist of large copper layers with thermal vias; these layers spread heat dissipated by the IC. Placing additional vias can reduce thermal resistance further. The maximum load current should be derated as the junction temperature approaches its maximum temperature rating. Power dissipation within the IC can be estimated by calculating the total power loss from an efficiency measurement and subtracting the inductor loss. The junction temperature can be calculated by multiplying the total IC power dissipation by the thermal resistance from junction to ambient and adding the ambient temperature. The LT8349 includes internal overtemperature protection that is intended to protect the device during momentary overload conditions. The overtemperature protection shuts down the IC when the junction temperature exceeds 170°C (typ). The internal soft start is triggered when the junction temperature drops below 165°C (typ). The maximum rated junction temperature is exceeded when this protection is active. Continuous operation above the specified absolute maximum operating junction temperature (see Absolute Maximum Ratings section) may impair device reliability or permanently damage the device.

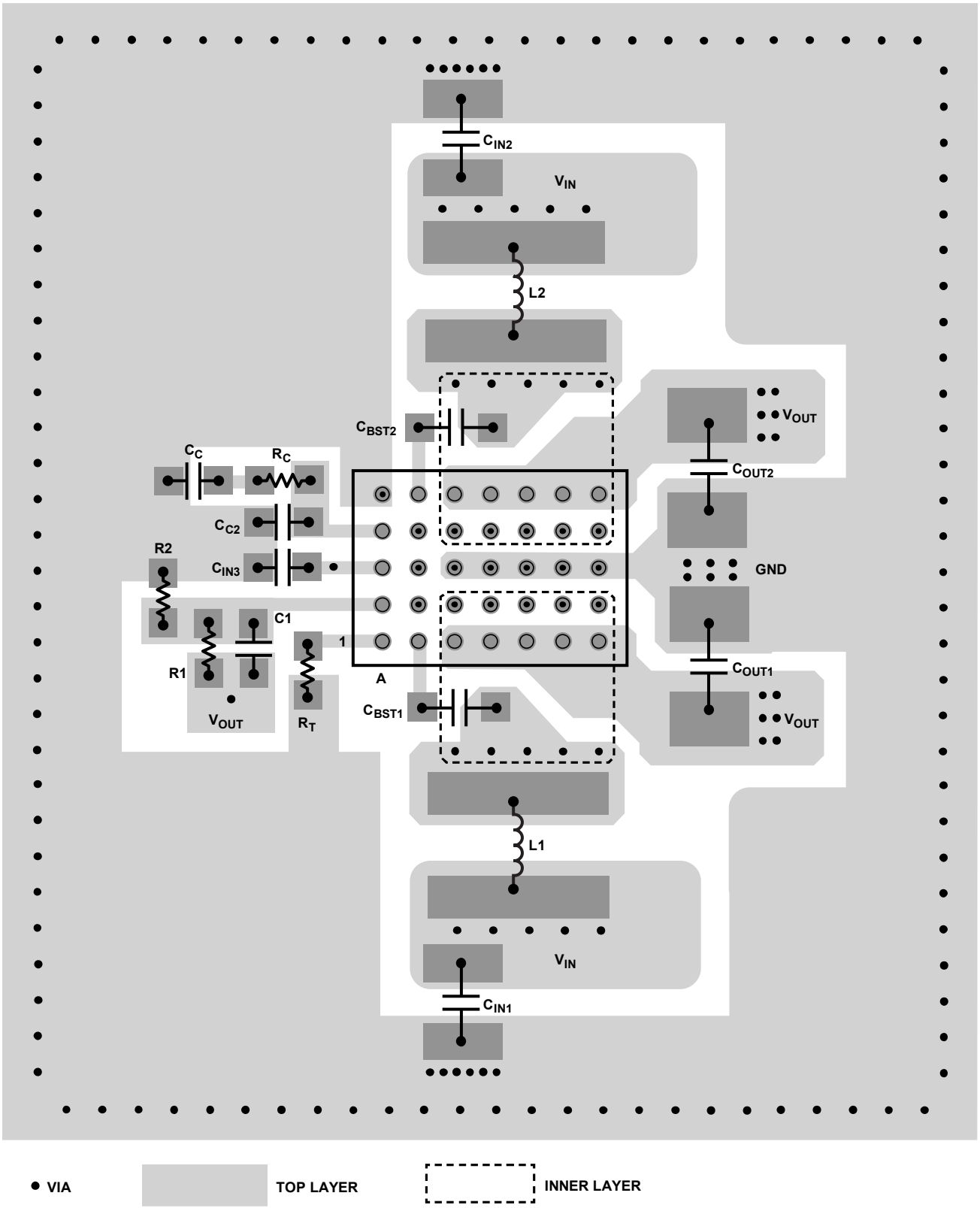


Figure 32. A Recommended PCB Layout for the LT8349

TYPICAL APPLICATIONS

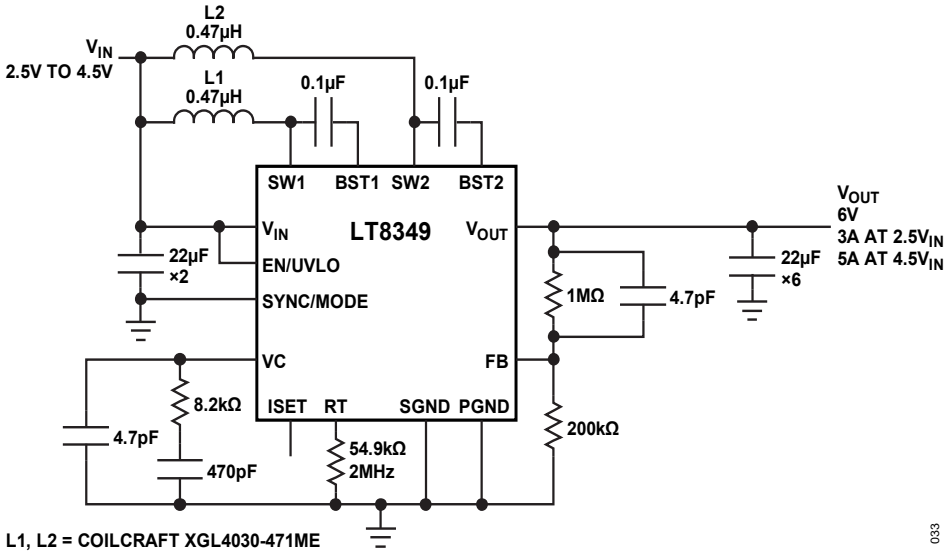


Figure 33. 2.5V to 4.5V Input, 6V Output Boost Converter

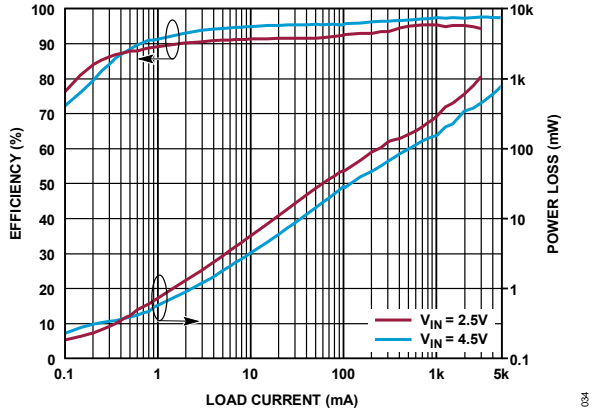


Figure 34. Efficiency and Power Loss vs Output Current

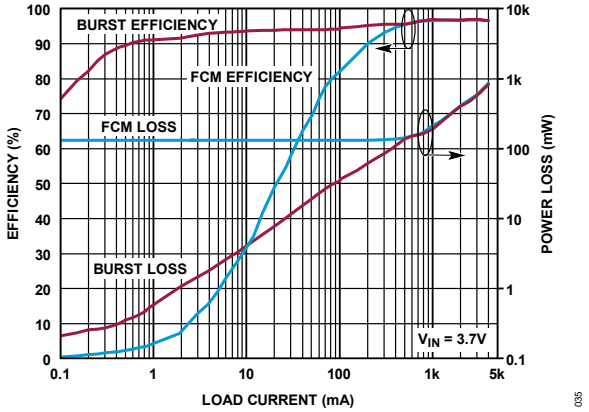


Figure 35. Efficiency and Power Loss vs Output Current

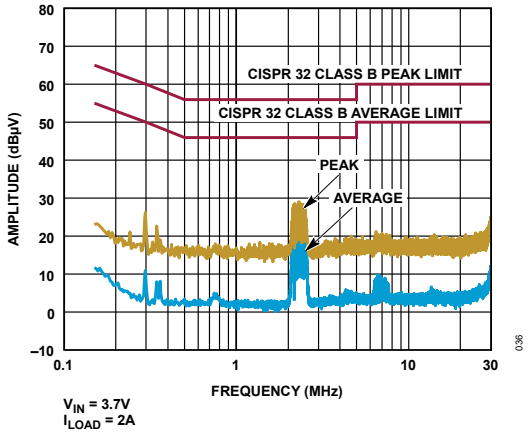


Figure 36. CISPR32 Conducted EMI measured on EVAL-LT8349-BZ with SSFM mode

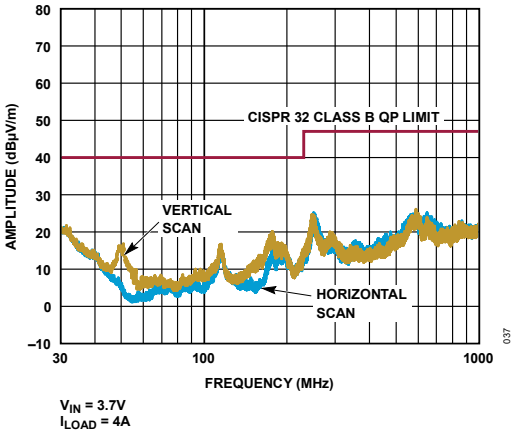
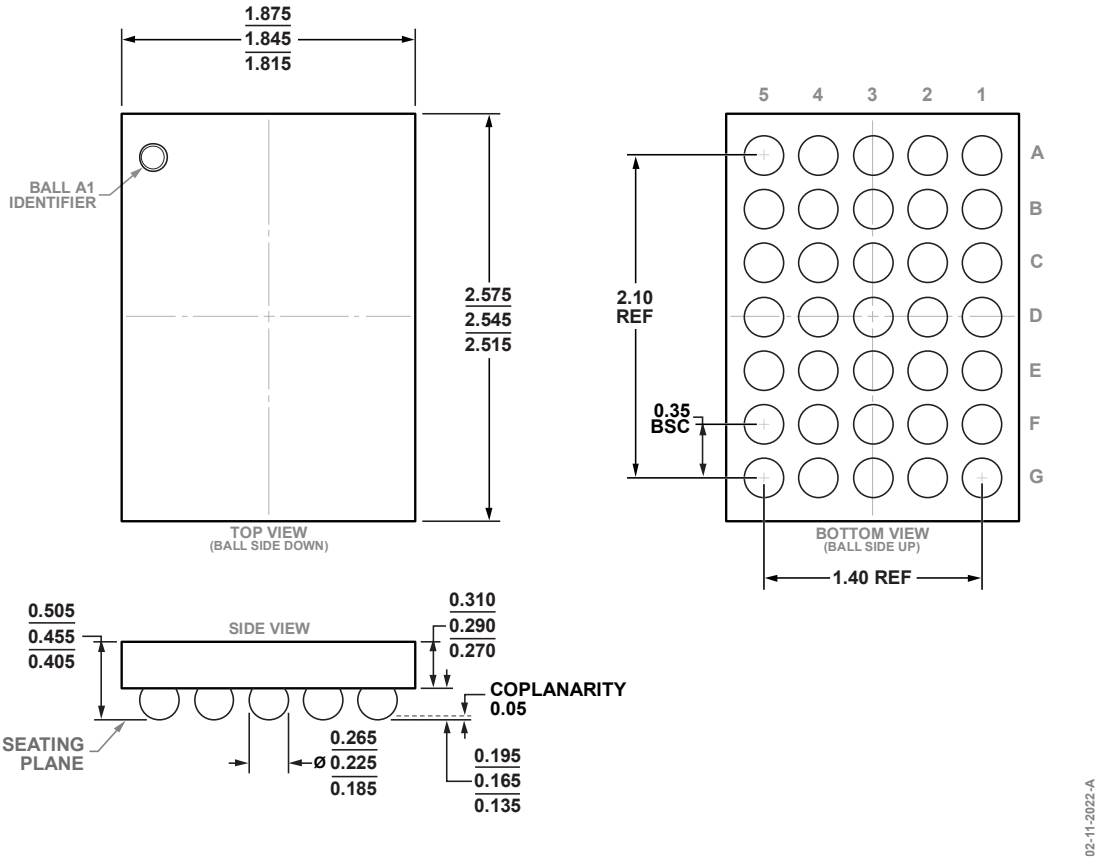


Figure 37. CISPR32 Radiated EMI measured on EVAL-LT8349-BZ with SSFM mode

PACKAGE DESCRIPTION

WLCSP PACKAGE
CB-35-4
35-BALL (1.845mm × 2.545mm × 0.455mm)
Dimensions shown in millimeters



Related Parts

PART NUMBER	DESCRIPTION	COMMENTS
LT8336	40V, 2.5A, Low IQ Synchronous Step-Up Silent Switcher	V_{IN} = 2.7V to 40V, $V_{OUT\ (MAX)}$ = 40V, I_Q = 4µA (Burst Mode Operation), 3mm × 3mm LQFN Package
LT8337/LT8337-1	28V, 5A, Low IQ Synchronous Step-Up Silent Switcher	V_{IN} = 2.7V to 28V, $V_{OUT\ (MAX)}$ = 28V, I_Q = 4µA (Burst Mode Operation), 3mm × 3mm LQFN Package
LTC3421	3A, 3MHz, Synchronous Step-Up DC/DC Converter with Output Disconnect	95% Efficiency, V_{IN} = 0.5V to 4.5V, $V_{OUT\ (MAX)}$ = 5.25V, I_Q= 12µA, I_{SD} < 1µA, QFN24 Package
LTC3428	4A, 2MHz (1MHz Switching), Dual Phase Step-Up DC/DC Converter	92% Efficiency, V_{IN} = 1.6V to 4.5V, $V_{OUT\ (MAX)}$ = 5.25V, I_{SD} < 1µA, 3mm × 3mm DFN Package
LTC3425	5A, 8MHz, Low Ripple, 4-Phase Synchronous Step-Up DC/DC Converter with Output Disconnect	95% Efficiency, V_{IN} = 0.5V to 4.5V, V_{OUT} (MAX) = 5.25V, I_Q= 12µA, I_{SD} < 1µA, QFN32 Package
LTC3124	15V, 5A 2-Phase Synchronous Step-Up DC/DC Converter with Output Disconnect	V_{IN} = 1.8V to 5.5V, $V_{OUT\ (MAX)}$ = 15V, I_Q = 25µA (Burst Mode Operation), 3mm × 5mm DFN and TSSOP Package

ORDERING GUIDE

Table 5. Ordering Guide

TAPE AND REEL	PART MARKING*	PACKAGE DESCRIPTION	TEMPERATURE RANGE
LT8349ACBZ-R7	8349	35-Ball (1.845mm × 2.545mm) WLCSP	−40°C to 125°C

Consult the factory for parts specified with wider operating temperature ranges. *The temperature grade is identified by a label on the shipping container.

Tape and reel specifications.