Dual Channel 9A, 16V PolyPhase Step-Down Silent Switcher 2 with Digital Power System Management

FEATURES

- **Silent Switcher®** 2 Architecture: Enables Compact, Efficient, Low EMI Solution
- PMBus/I²C Serial Interface
  - Telemetry Read Back Includes: V_{OUT}, I_{OUT}, V_{IN}, Die Temperature, Faults
  - Programmable Voltage, Current Limit, Digital Soft-Start/Stop, Sequencing, UV/OV, Phase, Frequency (up to 4MHz), Loop Compensation
  - Integrated EEPROM with Fault Event Log
- Set Key Parameters with Configuration Resistors for Operation without Programming
- ±0.25% Output Voltage Accuracy over Temperature from 0.6V to 1.375V
- PolyPhase® Load Sharing for up to Eight Phases
- Wide V_{IN} Range: Down to 2.9V, or 1.5V with $EXTV_{CC}$ up to 16V
- Over 94% Peak Efficiency at 1MHz, $12V_{IN}$ to $3.3V_{OUT}$
- V_{OUT} Range: 0.4V to 5.5V (up to 85% x V_{IN})
- Differential Remote V_{OUT} Sense
- External Frequency Synchronization
- 36-Lead (4mm x 5mm) LQFN Package

APPLICATIONS

- Communications, Storage, and Industrial Systems
- Data Center and Solid-State Drive Power Supplies

DESCRIPTION

The **LT7184S** is a dual-output monolithic PolyPhase DC/DC synchronous step-down regulator that delivers up to 7A of continuous current from both channels simultaneously and supports loads from -8A to +9A in either channel. The LT7184S features second-generation Silent Switcher® architecture with integrated V_{IN} bypass capacitors for fast, clean, low-overshoot switching edges to deliver high efficiency at high switching frequencies and minimize Electromagnetic interference (EMI) emissions. The I²C-based PMBus 1.3-compliant serial interface enables control of device functions and provides telemetry information for system monitoring. The LT7184S is supported by the **LTpowerPlay®** graphical user interface tool. The output voltage, frequency, phase, and device address can be configured using resistors for operation without programming. Settings can also be written via the serial interface and/or stored in EEPROM. The controlled on-time valley current mode control architecture with 25ns (typical) minimum on-time enables high switching frequency at low output voltage with excellent transient response in a small overall solution size.

TYPICAL APPLICATION

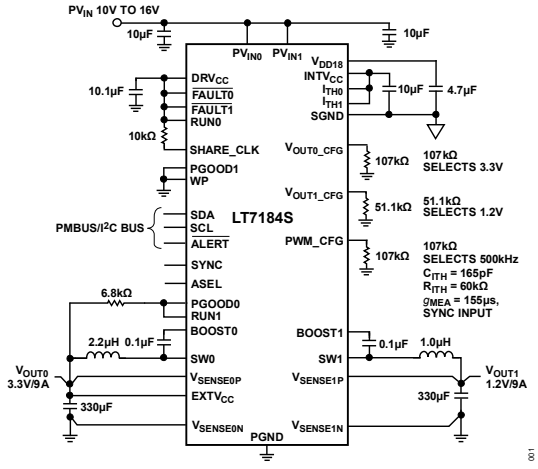

Figure 1. Typical Application for the LT7184S

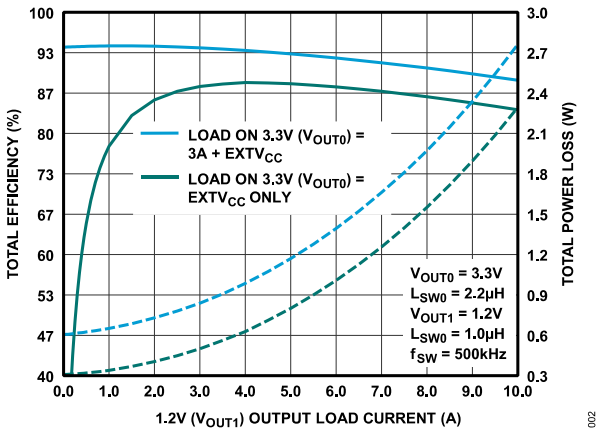

Figure 2. LT7184S 12V_{IN} Typical Application Efficiency

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REVISION HISTORY

REVISION NUMBER	REVISION DATE	DESCRIPTION	UNITS
0	10/24	Initial release	—
A	8/25	Updated Figure 16	18
B	2/26	Updated Table 16. PMBus Command Summary Updated link for the Packaging Drawing	45 51

ABSOLUTE MAXIMUM RATINGS

T_A = 25°C, unless otherwise specified.

Table 1. Absolute Maximum Ratings

PARAMETER	RATING
PV_{IN0}, PV_{IN1}	-0.3V to +20V
Average PV_{IN} Input Supply Current[2]	3A
$EXTV_{CC}$	-0.3V to +6V
$V_{SENSE0P}$, $V_{SENSE1P}$	-0.3V to +6V
$V_{SENSE0N}$, $V_{SENSE1N}$	-0.3V to +0.3V
I_{TH0}, I_{TH1}	-0.3V to +6V
SYNC, PWM_CFG, WP, SHARE_CLK, $\overline{ALERT}$, SDA, SCL, $\overline{FAULT0}$, $\overline{FAULT1}$, RUN0, RUN1, PGOOD0, PGOOD1, ASEL, V_{OUT0_CFG}, and V_{OUT1_CFG}	-0.3V to +6V
BOOST0 with respect to SW0	-0.3V to +6V
BOOST1 with respect to SW1	-0.3V to +6V
Operating Junction Temperature [3, 4, 5]	-40°C to +150°C
T_J	150°C
Storage Temperature Range	-65°C to +150°C
Maximum Peak Re-flow (Package Body) Temperature	260°C

1 Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

The average input current to each PV_{IN} pin on the LT7184S is a function of the PV_{IN} input voltage, the programmed output voltage that channels load current, and the efficiency as:

2
$$I_{PVIN} = \frac{V_{OUT} \times I_{OUT}}{PV_{IN} \times Efficiency}$$

The output voltage and current can be programmed so that the PV_{IN} input current exceeds the maximum average current rating for the LT7184S. Exceeding the maximum average input current rating for the LT7184S can affect device reliability and lifetime.

3 The LT7184S is specified over the -40°C to +150°C operating junction temperature range. High junction temperatures degrade operating lifetimes: operating lifetime is derated for junction temperatures greater than 125°C. Note that the maximum ambient temperature consistent with these specifications is determined by specific operating conditions in conjunction with board layout, the rated package thermal impedance, and other environmental factors.

4 The LT7184S includes overtemperature protection that is intended to protect the device during momentary overload conditions. The maximum rated junction temperature is exceeded when this protection is active.

Continuous operation above the specified maximum operating junction temperature will reduce the device's lifetime.

5 Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability and lifetime.

Thermal Resistance

Thermal performance is directly linked to PCB design and operating environment. Careful attention to PCB thermal design is required.

Table 2. Thermal Resistance

PACKAGE TYPE	θ_{JA}[3]	$\theta_{JC\text{-}TOP}$[4]	$\theta_{JC\text{-}BOTTOM}$[4]	UNIT
LQFN[1]	31.0	29.2	2.6	(°C/Watt)
LQFN[2]	19.9	29.2	2.6	(°C/Watt)

[1] Test Condition 1: Thermal impedance simulated values based upon use of 2S2P JEDEC FR-4 PCB 114mm x 76mm, 1.6mm thick in a one cubic foot sealed enclosure.

[2] Test Condition 2: Thermal impedance simulated values based upon the demonstration board in still air.

[3] θ_{JA} is the natural convection junction-to-ambient thermal resistance.

[4] $\theta_{JC\text{-}TOP}$ and $\theta_{JC\text{-}BOTTOM}$ are the natural conduction junction-to-case thermal resistances.

ESD Caution

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

SPECIFICATIONS

Table 3. Electrical Characteristics

(T_A = 25°C for typical values. For minimum and maximum values, specifications apply over the full operating temperature range unless otherwise noted.)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
INPUT SUPPLY					
Channel 0 Input Supply Range	$EXTV_{CC}$ < 3.0	2.9		16	V
Channel 0 Input Supply Range with $EXTV_{CC}$	3V ≤ $EXTV_{CC}$ ≤ 5.5V	1.5		16	V
Channel 1 Input Supply Range	PV_{IN0} ≥ 2.9V or 3V ≤ $EXTV_{CC}$ ≤ 5.5V	1.5		16	V
Optional $EXTV_{CC}$ Input Supply Range		3		5.5	V
$EXTV_{CC}$ + PV_{IN0} + PV_{IN1} Quiescent Current, both Channels Switching	$EXTV_{CC}$ = 4V, f_{SW} = 1MHz, PV_{IN0} = PV_{IN1} = 12V, No Load, T_A = 25°C		44		mA
$EXTV_{CC}$ + PV_{IN0} Current, Shutdown	Shutdown, T_A = 25°C		7.4		
Initialization Time[1]	With CFG Pins Enabled (Default), T_A = 25°C		13		ms
	CFG Pins Ignored, T_A = 25°C		10		ms
SWITCHING REGULATORS					
V_{OUT} Range	PV_{IN} ≥ 6.5V	0.4		5.5	V
	PV_{IN} < 6.5V	0.4		0.85 x PV_{IN}	V
V_{OUT} Set-Point Accuracy	High-Performance, Low V_{OUT} Mode, 0.6V ≤ V_{OUT} ≤ 1.375V	-0.25		0.25	%
	0.4V ≤ V_{OUT} ≤ 5.5V	-0.5		0.5	%
V_{OUT} Set-Point Resolution			1		mV
$V_{SENSE0P}$, $V_{SENSE1P}$ Input Resistance	Switcher (SWR0 or SWR1) Enabled, or 250Ω Pull-Down Disabled, T_A = 25°C		30		kΩ
Error Amplifier Transconductance Programming Resolution			3		bits
Error Amplifier Transconductance ($g_{m(MAX)}$)	Full V_{OUT} Range Mode, 0.4V ≤ V_{OUT} ≤ 5.5V, Includes Internal V_{OUT} Feedback Divider		1240		µS
Error Amplifier Transconductance ($g_{m(MIN)}$)	Full V_{OUT} Range Mode, 0.4V ≤ V_{OUT} ≤ 5.5V, Includes Internal V_{OUT} Feedback Divider		155		µS
Error Amplifier Transconductance (g_m step size)	Full V_{OUT} Range Mode, 0.4V ≤ V_{OUT} ≤ 5.5V, Includes Internal V_{OUT} Feedback Divider		155		µS

(T_A = 25°C for typical values. For minimum and maximum values, specifications apply over the full operating temperature range unless otherwise noted.)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Error Amplifier Transconductance ($g_{m(MAX)}$)	High-Performance, Low V_{OUT} Mode, 0.6V ≤ V_{OUT} ≤ 1.375V, Includes Internal V_{OUT} Feedback Divider		5000		µS
Error Amplifier Transconductance ($g_{m(MIN)}$)	High-Performance, Low V_{OUT} Mode, 0.6V ≤ V_{OUT} ≤ 1.375V, Includes Internal V_{OUT} Feedback Divider		625		µS
Error Amplifier Transconductance (g_m step size)	High-Performance, Low V_{OUT} Mode, 0.6V ≤ V_{OUT} ≤ 1.375V, Includes Internal V_{OUT} Feedback Divider		625		µS
Internal Compensation Resistor Programming Resolution	Internal Compensation (I_{TH} connected to $INTV_{CC}$)		3		Bits
Internal Compensation Capacitor Programming Resolution	Internal Compensation (I_{TH} connected to $INTV_{CC}$)		3		Bits
Positive Inductor Valley Current Limit: ($I_{LIM-POS}$)[2] (Sourcing Output Current)	I_{LIM} Range 0	3.4	4	4.5	A
	I_{LIM} Range 1	6.0	7	7.5	A
	I_{LIM} Range 2	7.8	9	10	A
	I_{LIM} Range 3	7.8	9	10	A
Negative Inductor Valley Current Limit ($I_{LIM-NEG}$)[2] (Sinking Output Current)	I_{LIM} Range 0	-4	-3.5	-3.0	A
	I_{LIM} Range 1	-6.5	-6	-5.5	A
	I_{LIM} range 2	-8.5	-7.5	-6.5	A
	I_{LIM} Range 3	-10	-9	-8	A
Minimum On-Time (t_{MIN-ON})	I_{LOAD} = +1A, FASTSLEW = 1		25	40	ns
Minimum Off-Time ($t_{MIN-OFF}$)			85	125	ns
POWER FETs					
On-Resistance (R_{DS-ON})	Top Switch		25		mΩ
	Bottom Switch		7		mΩ
SW Leakage	PV_{IN} = 16V, V_{SW} = 0V, 16V, T_A = 25°C	-20		20	µA
OUTPUT VOLTAGE SUPERVISORS					
V_{OUT} Undervoltage (UV) Fault/Warning Programming Range	T_A = 25°C	0.36		5.5	V
V_{OUT} Overvoltage (OV) Fault/Warning Programming Range	T_A = 25°C	0.4		6	V
V_{OUT} UV/OV Fault/Warning Threshold Accuracy	V_{OUT} UV/OV Threshold < 0.6V	-12		12	mV
	V_{OUT} UV/OV Threshold ≥ 0.6V	-2		2	%
V_{OUT} UV/OV Fault/Warning Programming Step-Size			4		mV

(T_A = 25°C for typical values. For minimum and maximum values, specifications apply over the full operating temperature range unless otherwise noted.)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
V_{OUT} UV/OV Fault/Warning Time	V_{OUT} = 10mV Beyond Threshold			25	µs
INPUT VOLTAGE SUPERVISORS					
ON Threshold Programming Range	PV_{IN} rising, T_A = 25°C	1.4		16	V
OFF Threshold Programming Range	PV_{IN} falling, T_A = 25°C	1.35		16	V
ON/OFF Threshold Programming Step Size			25		mV
ON/OFF Threshold Set Point Accuracy	$V_{IN\_ON/OFF} \le 5V$	-100		100	mV
	$5V \le V_{IN\_ON/OFF} \le 20V$	-2		2	%
PV_{IN} Overvoltage Lockout Threshold	PV_{IN0} or PV_{IN1} Rising	17.26	17.6	17.94	V
	PV_{IN0} or PV_{IN1} Falling	16.26	16.7	17.14	V
OSCILLATOR AND PHASE-LOCKED LOOP					
SYNC Input Frequency Range		500		4000	kHz
Switching Frequency Programmable Range	T_A = 25°C	500		4000	kHz
Switching Frequency Set Point Accuracy		-7.5		7.5	%
Switching Phase Programming Range		0		345	deg
Switching Phase Programmable Resolution			15		deg
TELEMETRY READBACK					
Telemetry Measurement Period, All Except Die Temperature	Standard Telemetry Mode		6.5		ms
Telemetry Measurement Period, All except Die Temperature	Low-Frequency Telemetry		110		ms
Telemetry Measurement Period, Die Temperature			26		ms
OUTPUT VOLTAGE READBACK					
READ_VOUT Accuracy	High-Performance Low-V_{OUT} Mode, $0.6V \le V_{OUT} \le 1.375V$	-0.2		0.2	%
	$0.4V < V_{OUT} < 5.5V$	-0.4		0.4	%
PV_{IN0}, PV_{IN1} INPUT VOLTAGE READBACK					
READ_VIN Accuracy	$1.5V \le PV_{IN} \le 3.0V$	-30		30	mV
	$3.0V \le PV_{IN} \le 16V$	-1		1	%

(T_A = 25°C for typical values. For minimum and maximum values, specifications apply over the full operating temperature range unless otherwise noted.)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
OUTPUT CURRENT READBACK					
READ_IOUT Accuracy[3]	I_{OUT} = 0A to 4A, $V_{OUT}/V_{IN} \le 0.25$, 500kHz ≤ f_{SW} ≤ 2MHz	-350		350	mA
	I_{OUT} = 4A to 8A, $V_{OUT}/V_{IN} \le 0.25$, 500kHz ≤ f_{SW} ≤ 2MHz	-5		5	%
	I_{OUT} = 0A to 4A, $V_{OUT}/V_{IN} > 0.25$	-600		600	mA
	All other conditions 4 ≤ I_{OUT} ≤ 8A	-15		15	%
FREQUENCY READBACK					
READ_FREQUENCY Accuracy	f_{SW} < 600kHz, T_A = 25°C	-30		30	kHz
	f_{SW} ≥ 600kHz, T_A = 25°C	-5		5	%
ELECTRICALLY ERASABLE PROGRAMMABLE READ-ONLY MEMORY (EEPROM) CHARACTERISTICS[4]					
Retention		10			years
Endurance		10,000			writes
Mass Write Time (STORE_USER_ALL)			250	500	ms
DIGITAL INPUTS: RUNN, $\overline{\text{FAULTN}}$, PGOODN, SHARE_CLK, SCL, SDA, $\overline{\text{ALERT}}$, WP					
Input High Threshold (V_{IH})			1.1	1.35	V
Input Low Threshold (V_{IL})		0.8	0.9		V
Hysteresis (V_{HYS})			200		mV
Leakage Current	Applied Voltage = 0V, 5.5V, T_A = 25°C			±10	µA
Input Capacitance[5]	T_A = 25°C			10	pF
DIGITAL CLOCK INPUT: SYNC					
Peak-To-Peak Input Voltage Swing	Sync Input Mode	1.4		5.5	V
Rise Time	Sync Input Mode			25	ns
Duty Cycle	Sync Input Mode	30		70	%
DIGITAL CLOCK OUTPUT: SYNC					
Output High Voltage (V_{OH})	SYNC Output Mode	1.6	1.88	1.98	V
Output Low Voltage (V_{OL})	SYNC Output Mode			0.2	V
Output Impedance	SYNC Output Mode		60		Ω
CURRENT-LIMITED OPEN-DRAIN OUTPUTS: RUNN, $\overline{\text{FAULTN}}$					
Pull-Down Current	Applied Voltage = 0.4V to 5.5V	1	1.5	2	mA
OPEN-DRAIN OUTPUTS: PGOODN, SHARE_CLK					
Output Low Voltage	I = 6mA			0.4	V
DIGITAL I/O: SCL, SDA, $\overline{\text{ALERT}}$					
	Data Output Hold-Time	0		450	ns

1 Delay from RESTORE_USER_ALL, MFR_RESET, or Application of PV_{IN0} or $EXTV_{CC}$ until the TON_DELAY timer can begin.

2 The LT7184S switching regulators use valley current mode control, so the current limits specified correspond to the valley of the inductor current waveform. Valley current limit moves with V_{OUT}/L and with

FREQUENCY_SWITCH and is guaranteed for duty cycles < 50%; current limits are specified at V_{OUT}/L = 2V/µH and FREQUENCY_SWITCH = 1000. Maximum load current is higher with positive loads and equals the valley current plus one-half of the inductor ripple current. Maximum load current is lower with negative loads and equals the valley current minus one-half of the inductor ripple current. See the *Applications Information* section and *Typical Performance Characteristics* for more details.

[3] READ_IOUT is tested in a production test mode at full rated current where I_{SW} flows through the synchronous switch at 100% duty cycle. In applications, READ_IOUT is calculated from sampled current measurements across the synchronous switch.

[4] EEPROM endurance is guaranteed by design, characterization, and correlation with statistical process controls. Data retention is production tested via a high-temperature bake at the wafer level. The minimum retention specification applies for devices whose EEPROM has been cycled less than the minimum endurance specification.

[5] Guaranteed by design, characterization, and correlation with statistical process controls.

Table 4. I²C/PMBus Timing

PARAMETER	SYMBOL	MIN	MAX	UNITS
Serial Bus Operating Frequency	f_{SCL}	10	1000	kHz
Bus Free Time Between Stop and Start	t_{BUF}	500		ns
Hold Time After Repeated Start Condition	t_{HD-STA}	260		ns
Repeated Start Condition Setup Time	t_{SU-STA}	260		ns
Stop Condition Setup Time	t_{SU-STO}	260		ns
Data Input Setup Time	t_{SU-DAT}	50		ns
Data Input Hold Time	t_{HD-DAT}	0		ns
Data Output Hold Time		0	450	ns
Bus Timeout	$t_{TIMEOUT}$	25	35	ms
Serial Clock Low Period	t_{LOW}	0.5	10000	µs
Serial Clock High Period	t_{HIGH}	260		ns

PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS

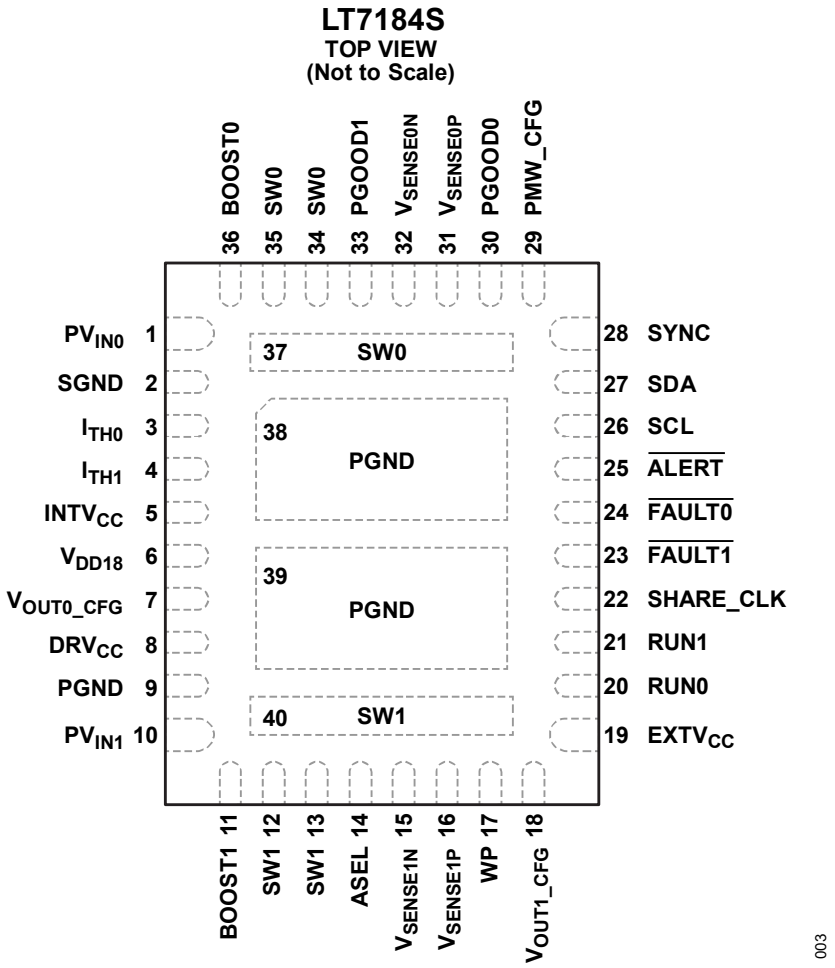

Figure 3. Pin Configuration

Table 5. Pin Descriptions

PIN	Name	DESCRIPTION
1	PV_{IN0}	Power Supply Input for Channel 0 and Internal LDO Regulators. This pin must be bypassed to SGND as close as possible to the LT7184S, with a low ESR capacitor of value 4.7µF or more using the top PCB layer. If $EXTV_{CC}$ < 3V, then the internal LDO regulators (for DRV_{CC}, $INTV_{CC}$, and V_{DD18}) pull power from PV_{IN0}.
2	SGND	Signal Ground. The return for the I_{TH0} and I_{TH1} compensation networks and the $INTV_{CC}$ and V_{DD18} supply pins should be connected to an isolated ground return connected as close as possible to the SGND pin. This pin is connected to PGND within the LT7184S package. Do not connect the SGND isolated ground return to PGND in more than one location in the application PCB. In PolyPhase applications the SGND and I_{THN} nodes should be symmetrically connected to each IC in the PolyPhase configuration.

PIN	Name	DESCRIPTION
3	I_{TH0}	Error amplifier output and switching regulator compensation for Channel 0. Connect the appropriate external components between I_{TH0} and SGND to compensate the regulator loop frequency response for Channel 0 or connect to $INTV_{CC}$ to select internal compensation for Channel 0.
4	I_{TH1}	Error amplifier output and switching regulator compensation for channel 1. Connect the appropriate external components between I_{TH1} and SGND to compensate the regulator loop frequency response for Channel 1, or connect to $INTV_{CC}$ to select internal compensation for Channel 1.
5	$INTV_{CC}$	Internal 3V LDO regulator bypass. This LDO regulator output provides a supply current for internal circuitry. This pin must be bypassed to SGND with a 10µF or greater, low ESR ceramic capacitor as close as possible to the IC on the top Printed Circuit Board (PCB) layer. Do not load the $INTV_{CC}$ pin with external circuitry.
6	V_{DD18}	Internal 1.8V regulator bypass. This pin must be bypassed to SGND with a 4.7µF or greater low ESR ceramic capacitor as close as possible to the LT7184S on the top PCB layer. Do not load the V_{DD18} pin with external circuitry.
7	V_{OUT0_CFG}	Output voltage configuration for channel 0. Connect a 1% resistor from V_{OUT0_CFG} to GND (SGND or PGND) according to *Table 7* in the *Applications Information* section to select one of sixteen output voltage set points. If left floating or connected to V_{DD18}, the LT7184S uses the value of VOUT_COMMAND programmed in EEPROM to set the output voltage set point. The V_{OUT0_CFG} pin is only read at the start-up.
8	DRV_{CC}	Internal 3.5V LDO regulator bypass. The DRV_{CC} regulator provides the supply current for the power FET drivers. This pin must be bypassed to PGND with a 100nF or greater low Equivalent series resistance (ESR) ceramic capacitor as close as possible to the LT7184S using the top PCB layer, and a bulk 10µF low ESR ceramic capacitor. Do not load the DRV_{CC} pin with external circuitry with the optional exceptions of the pull-up resistor for the SHARE_CLK pin and/or the RUN0, RUN1, $\overline{FAULT0}$, or $\overline{FAULT1}$ pins.
9, Exposed pads 38, 39	PGND	Power ground. The (-) terminal of the PV_{IN1} input bypass capacitors and the (-) terminal of the output capacitors (C_{OUT0} and C_{OUT1}) should be connected to these pins with low-impedance connections. The PCB must be designed to provide low electrical and thermal impedance to PGND.
10	PV_{IN1}	Power supply input for Channel 1. This pin must be bypassed to PGND as close as possible to the LT7184S with a low ESR capacitor of value 4.7µF or more using the top PCB layer.
11	BOOST1	Boosted floating driver supply for Channel 1. Connect a 0.1µF boost capacitor from BOOST1 to SW1 as close as possible to the LT7184S using only the top PCB layer. The normal operation voltage swing on this pin is from DRV_{CC} to PV_{IN1} + DRV_{CC}.
12, 13, Exposed pad 40	SW1	The output of the Channel 1 internal power switches. Connect these pins together and connect the Channel 1 inductor and BOOST1 capacitor. This node should be sized to support the maximum load current for Channel 1 and be spaced away from all other PCB metal.
14	ASEL	Serial bus address configuration pin. Connect a 1% resistor from ASEL to ground (SGND or PGND) to select one of sixteen serial bus interface addresses. The ASEL pin is read at start-up. If the ASEL pin is left floating, the factory default 7-Bit device address is 0x4F. If the ASEL pin is grounded, the factory default device address is 0x40.

PIN	Name	DESCRIPTION
15	$V_{SENSE1N}$	Output voltage negative sense input. Connect to the Channel 1 output voltage sense ground point.
16	$V_{SENSE1P}$	Output voltage positive sense input. Connect to the Channel 1 output voltage sense point.
17	WP	Write protect pin. When this pin is high, only the PAGE, OPERATION, MFR_EE_UNLOCK, and CLEAR_FAULTS commands are write-able. Clear individual fault bits by writing a 1 to the respective bits in the STATUS commands.
18	V_{OUT1_CFG}	Output voltage configuration for Channel 1 or poly phase configuration. If the PWM_CFG pin is NOT configured for PolyPhase, the 1% resistor from V_{OUT1_CFG} to the ground (either SGND or PGND) will be selected as the voltage set point according to *Table 7* in the *Applications Information* section. If the PWM_CFG pin is configured for poly phase operation, then the Channel 1 output is set to the same value as Channel 0 based on V_{OUT0_CFG}, and a 1% resistor from V_{OUT1_CFG} to ground selects a PolyPhase configuration according to *Table 10* in the *Applications Information* section. The V_{OUT1_CFG} pin is read at LT7184S start-up.
19	$EXTV_{CC}$	Optional Power Supply input. If connected to 3V to 5.5V, this pin is used to derive the DRV_{CC}, $INTV_{CC}$, and V_{DD18} supplies. If one of the regulator outputs is set to output 3V or greater, that output may be connected to $EXTV_{CC}$ to reduce power loss. If this pin is not connected to a regulator output, apply a 0.1µF or greater local bypass capacitor on this pin to GND as close as possible to the LT7184S.
20	RUN0	Channel 0 Regulator Enable Input. Logic high enables the Channel 0 regulator. The RUN0 pin is pulled down with 1.5mA (typical) during POR and reset to facilitate sequencing with other regulators but may be over-driven high by a digital output of another device. This pin may be connected directly to DRV_{CC} to enable the regulator when input power is present.
21	RUN1	Channel 1 Regulator Enable Input. Logic high enables the Channel 1 regulator. The RUN0 pin is pulled down with 1.5mA (typical) during POR and reset to facilitate sequencing with other regulators but may be over-driven high by a digital output of another device. This pin may be tied directly to DRV_{CC} to enable the regulator when input power is present.
22	SHARE_CLK	Bidirectional Open-Drain Sequence Time Base Share Clock. Nominally 100kHz. Used to align start-up and shutdown of regulator outputs among multiple Analog Devices' products when PolyPhase or time-based sequencing is employed. A pull-up resistor to 1.6V to 5.5V is required if SHARE_CLK is connected between multiple devices to synchronize sequencing. If time-based sequencing is not used, leave the SHARE_CLK pin floating. It is pulled up to V_{DD18} inside the chip through a diode and a 100kΩ resistor.
23	$\overline{FAULT1}$	Input/Open-Drain Output. The LT7184S pulls the $\overline{FAULT1}$ pin down with 1.5mA (typical) when an unmasked fault occurs on the Channel 1 regulator. If another device pulls down the $\overline{FAULT1}$ pin, the LT7184 Channel 1 regulator turns off immediately. If PolyPhase configuration is used, tie together the $\overline{FAULTN}$ pins of all PolyPhase channels. If the PolyPhase configuration is used, or if $\overline{FAULTN}$ pin reporting or sharing is required, a pull-up resistor of 6.8kΩ or greater to 1.6V to 5.5V is required. $\overline{FAULT1}$ pin may be connected directly to DRV_{CC} if the $\overline{FAULT1}$ pin function is not required.
24	$\overline{FAULT0}$	$\overline{FAULT0}$ Input/Open-Drain Output. The LT7184S pulls the $\overline{FAULT0}$ pin down with 1.5mA (typical) when an unmasked fault occurs on the Channel 0 regulator. If another device

PIN	Name	DESCRIPTION
		pulls down the FAULT0 pin, the LT7184 channel 0 regulator turns off immediately. If PolyPhase configuration is used, tie together the $\overline{\text{FAULTN}}$ pins of all PolyPhase channels. If the PolyPhase configuration is used, or if the Fault pin reporting or sharing is required, a pull-up resistor of 6.8kΩ or greater to 1.6V to 5.5V is required. $\overline{\text{FAULT0}}$ pin may be tied directly to DRV_{CC} if the $\overline{\text{FAULT0}}$ pin function is not required.
25	$\overline{\text{ALERT}}$	Open-Drain Alert Output. If the $\overline{\text{ALERT}}$ pin function is used, a pull-up resistor of 1.6V to 5.5V is required. If the $\overline{\text{ALERT}}$ pin function is not used, the pin may be connected to the ground.
26	SCL	Serial Bus Clock Input and Output. The LT7184S may hold SCL low if clock stretching is enabled (PMBus speeds 400kHz - 1MHz only). A pull-up resistor of 1.6V to 5.5V is required for PMBus/I^2C operation. If serial bus operation is not required, SCL may be connected to the ground.
27	SDA	Serial Bus Data Input and Output. A pull-up resistor of 1.6V to 5.5V is required for PMBus/I^2C operation. If serial bus operation is not required, the SDA may be connected to the ground.
28	SYNC	External Clock Synchronization Input/Output. When driven with an external clock, an internal phase-locked loop synchronizes the switching regulator output with the rising edge of the external clock. If configured as an output (MFR_SYNC_CONFIG_LT7184 bit 0 is set to 1), the LT7184S drives the SYNC pin output at the switching clock frequency set by the FREQUENCY_SWITCH command with a voltage swing of 0V to V_{DD18}.
29	PWM_CFG	PWM Configuration Resistor Pin. Connect a 1% resistor from PWM_CFG to the ground (SGND or PGND) according to *Table 9* in the *Applications Information* section to select frequency, phase, and mode configurations. The PWM_CFG pin is read at LT7184S start-up. See *Applications Information* for more details.
30	PGOOD0	Power Good Indicator Output for channel 0. PGOOD0 is pulled low when the channel 0 regulator output is outside of the OV/UV fault thresholds when Channel 0 is disabled, and during on/off sequencing. The PGOOD0 output is deglitched by an internal configurable timer. If the PGOOD0 pin function is not used, it may be connected to the ground.
31	$V_{SENSE0P}$	Output voltage positive sense input. Connect to the Channel 0 output voltage sense point.
32	$V_{SENSE0N}$	Output voltage negative sense input. Connect to the Channel 0 output voltage sense ground point.
33	PGOOD1	Power Good Indicator Output for Channel 1. PGOOD1 is pulled low when the Channel 0 regulator output is outside of the OV/UV fault thresholds when Channel 1 is disabled and during on/off sequencing. The PGOOD1 output is deglitched by an internal configurable timer. If the PGOOD1 pin function is not used, it may be connected to the ground.
34, 35, Exposed pad 37	SW0	Output of the Channel 0 internal power switches. Connect these pins together and connect the Channel 0 inductor and BOOST0 capacitor. This node should be sized to support the maximum load current for Channel 0 and be spaced away from all other PCB metal.
36	BOOST0	Boosted floating driver supply for Channel 0. Connect a 0.1µF boost capacitor from BOOST0 to SW0 as close as possible to the LT7184S using only the top PCB layer. The normal operation voltage swing on this pin is from DRV_{CC} to PV_{IN0} + DRV_{CC}.

TYPICAL PERFORMANCE CHARACTERISTICS

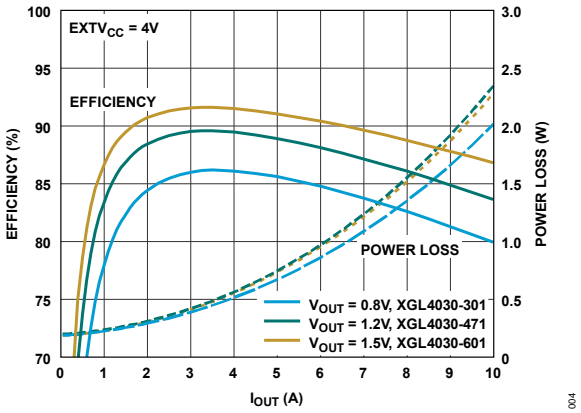

Figure 4. 12V PV_{IN} Efficiency/Power Loss at f_{SW} = 1000kHz, various V_{OUT}

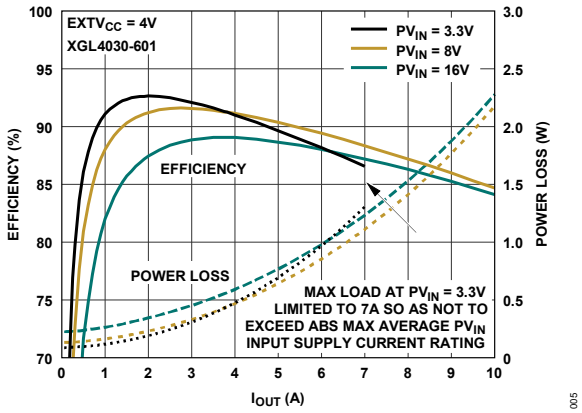

Figure 5. V_{OUT} = 1.2V, f_{SW} = 1000kHz Efficiency/ Power Loss, various PV_{IN}

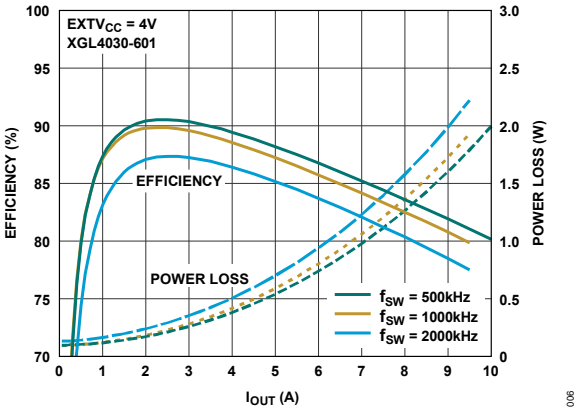

Figure 6. 5V PV_{IN} to 0.8V V_{OUT} Efficiency/ Power Loss various f_{SW}

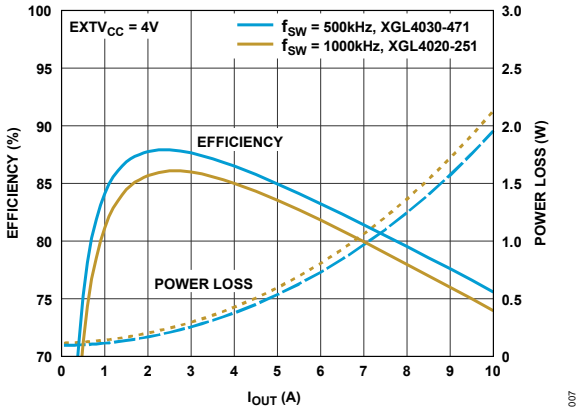

Figure 7. 5V PV_{IN} to 0.6V V_{OUT} Efficiency at various f_{SW}

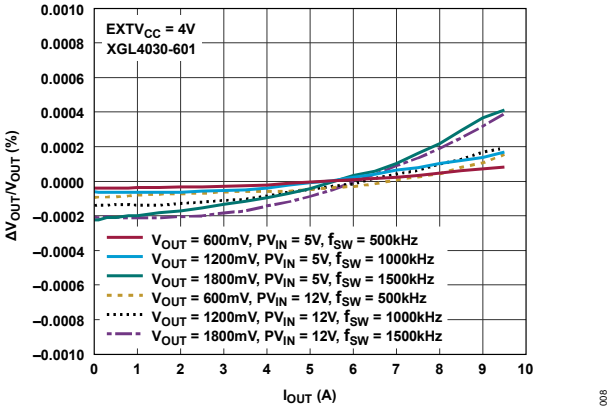

Figure 8. Load Regulation

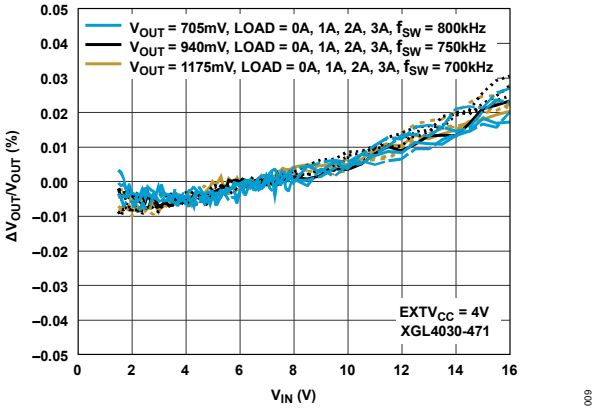

Figure 9. Line Regulation

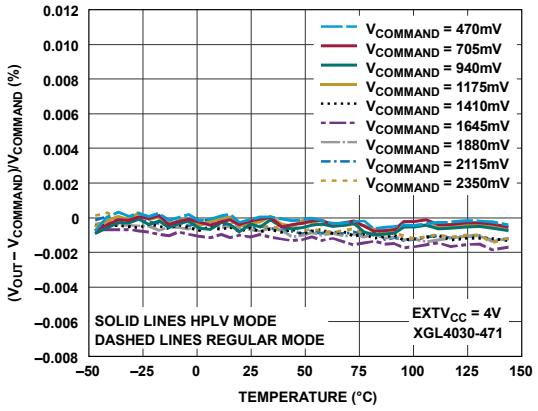

Figure 10. Temperature Regulation: $(V_{OUT} - V_{COMMAND})/V_{COMMAND}$ (%) vs Temperature

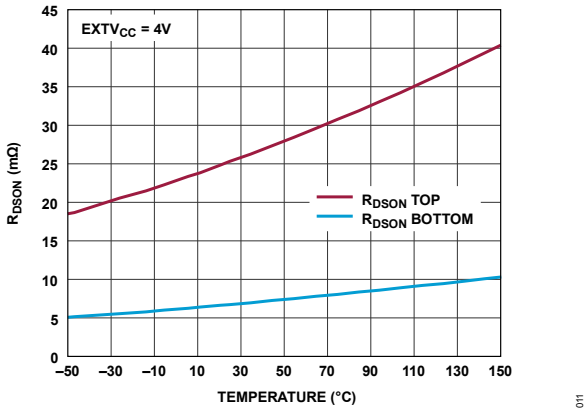

Figure 11. ON Resistance vs Temperature

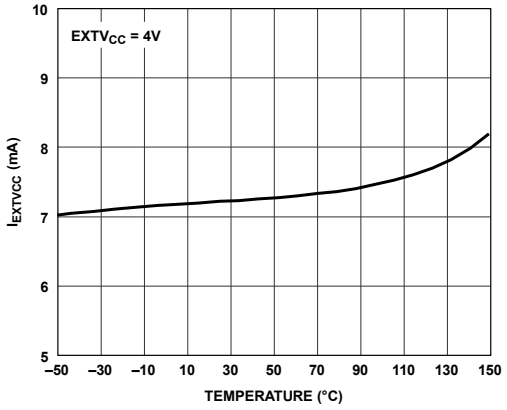

Figure 12. I_{EXTVCC} vs Temperature Shutdown

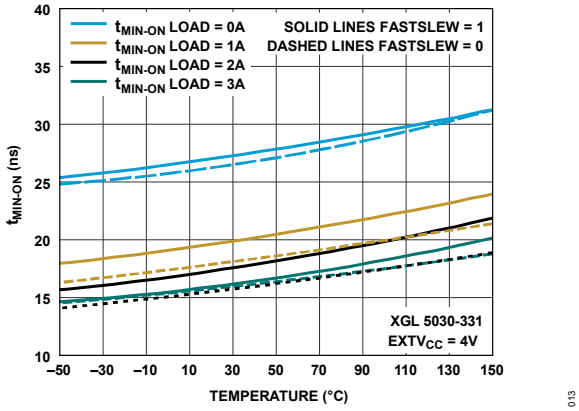

Figure 13. t_{MIN-ON} vs Temperature

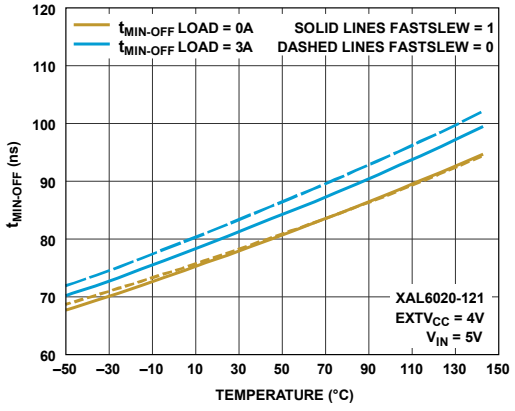

Figure 14. $t_{MIN-OFF}$ vs Temperature

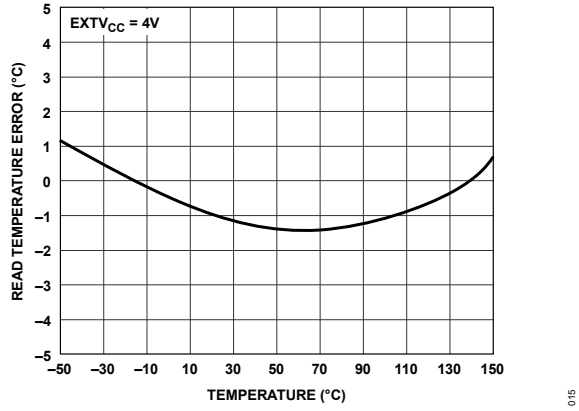

Figure 15. READ_TEMPERATURE Error vs Temperature

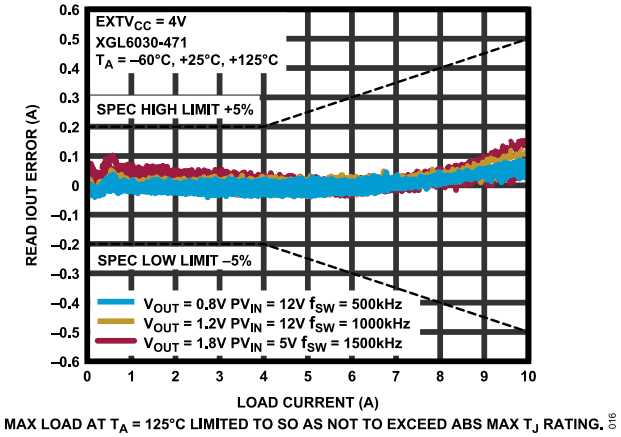

Figure 16. READ_IOUT Error vs I_{OUT}

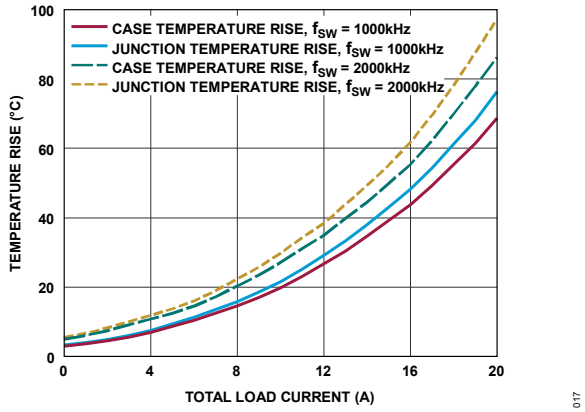

Figure 17. Temperature Rise vs Total Load Current

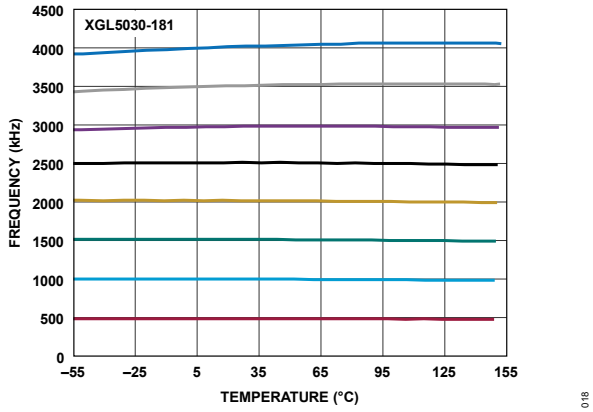

Figure 18. f_{SW} vs Temperature

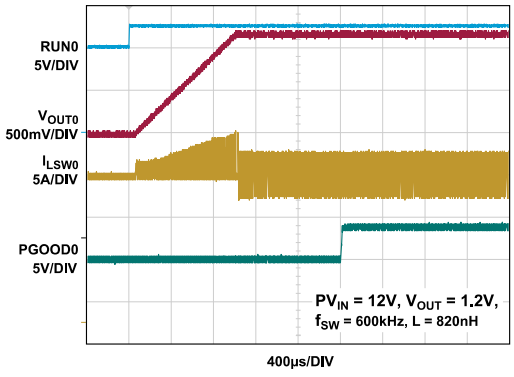

Figure 19. Soft-Start no Load

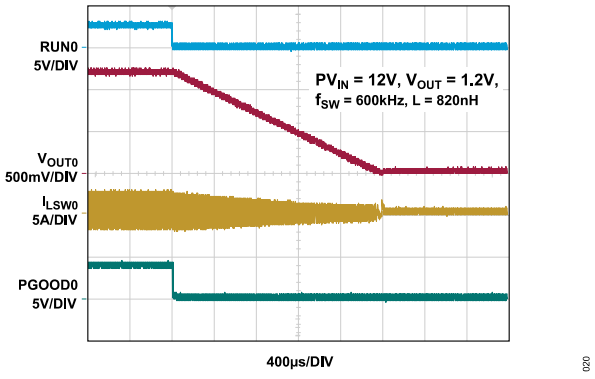

Figure 20. Soft-Stop no Load

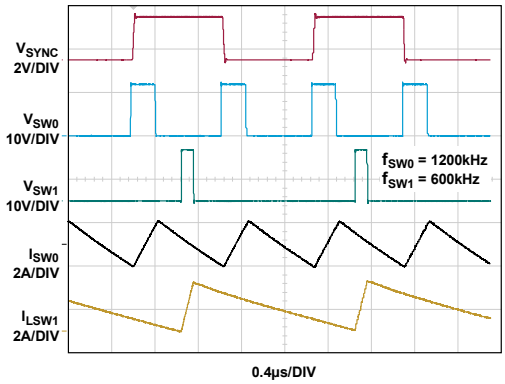

Figure 21. SYNC Waveforms Figure 45 Application, $EXTV_{CC} = V_{OUT0}$, $V_{OUT1} = 0.8V$, $I_{OUT1} = 1A$

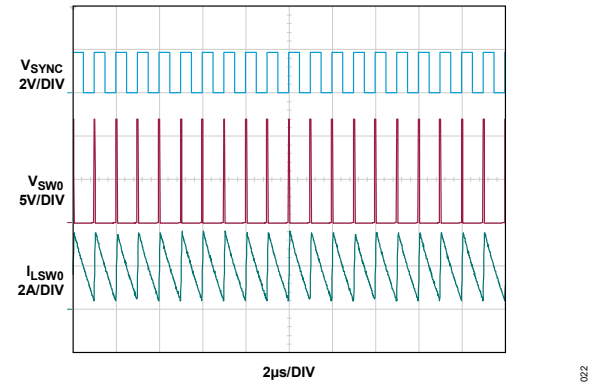

Figure 22. Continuous Conduction, PV_{IN} = 12V, V_{OUT} = 0.75V, L_{SW} = XGL4020-251, 2A load

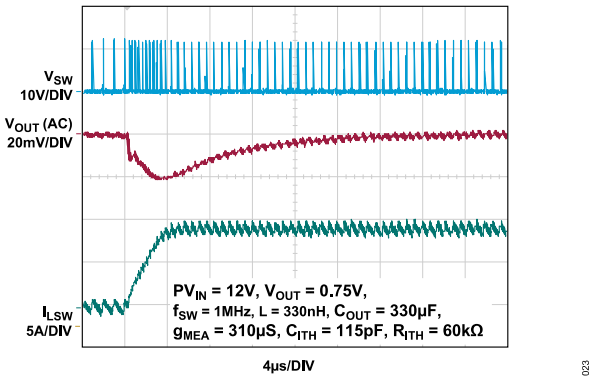

Figure 23. 9A Load Step, Default Internal Compensation, V_{OUT} = 0.75V

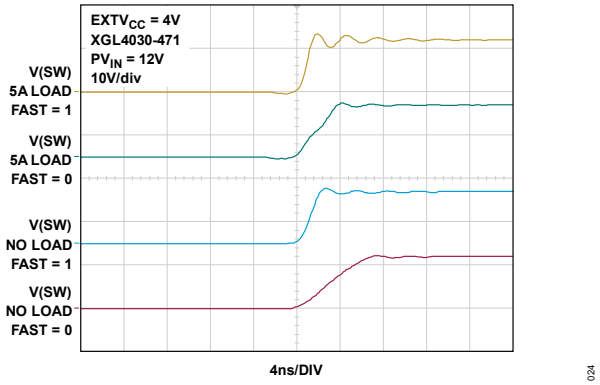

Figure 24. SW Rise Waveforms, V_{OUT} = 1.2V

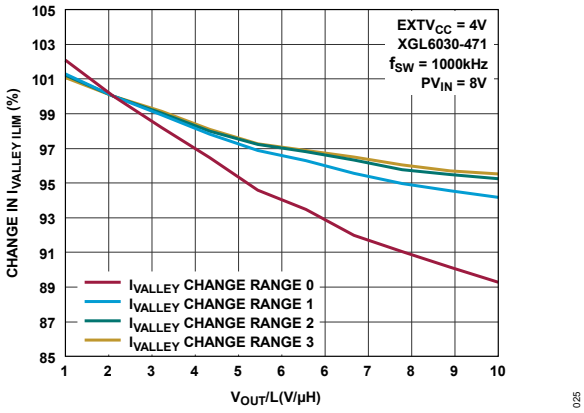

Figure 25. Positive Valley Current Limit Change with V_{OUT}/L

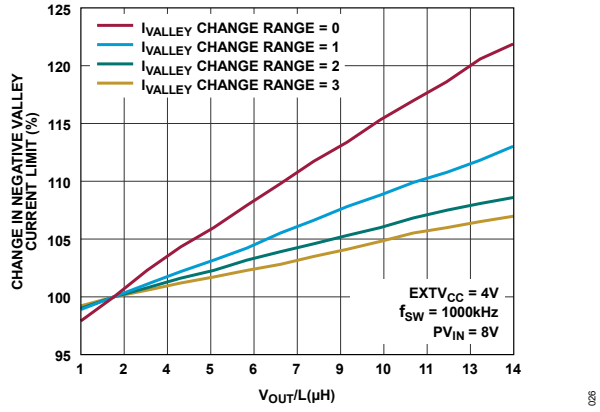

Figure 26. Negative Valley Current Limit Change with V_{OUT}/L

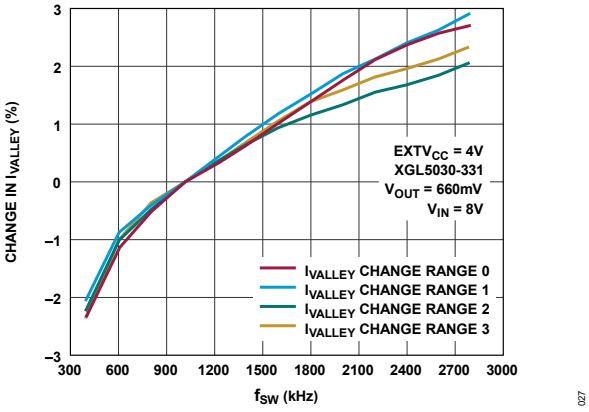

Figure 27. Valley Current Limit Change with f_{SW}

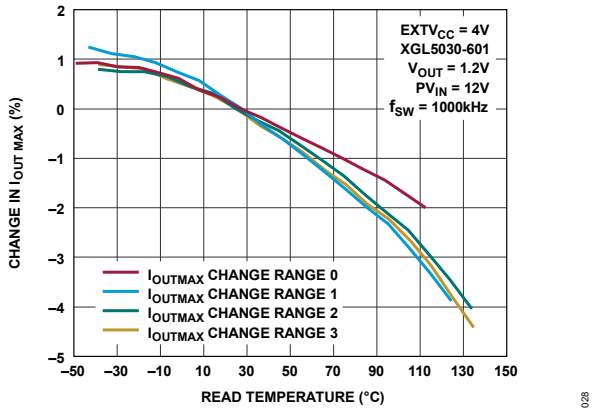

Figure 28. Maximum Output Current Change with Temperature

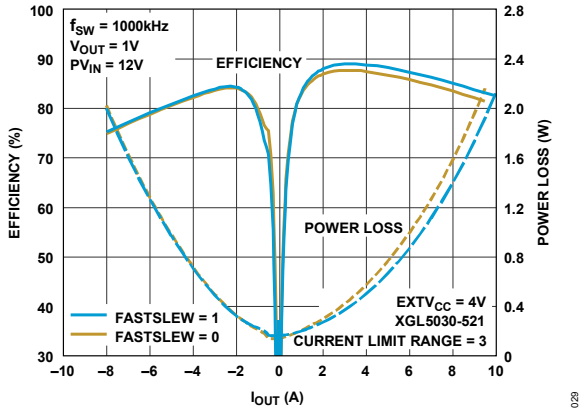

Figure 29. Efficiency/Power Loss, Full-Load Range

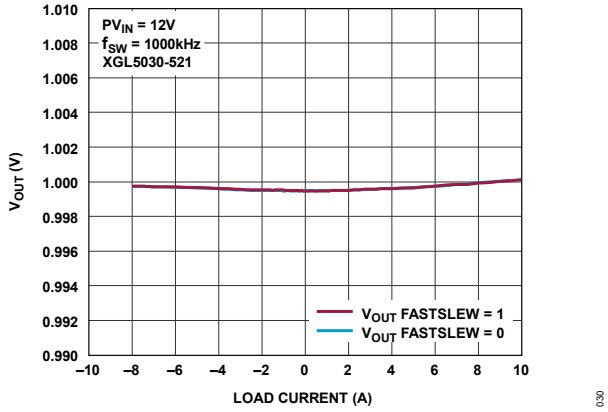

Figure 30. Load Regulation V_{OUT} = 1V, Full-Load Range

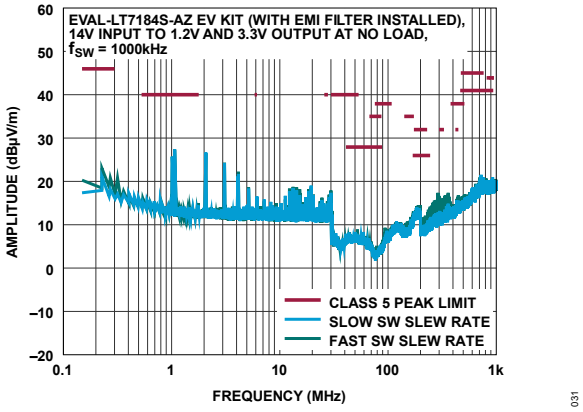

Figure 31. Radiated EMI Performance No-Load (CISPR25 Radiated Emission Test with Class 5 Peak Limits)

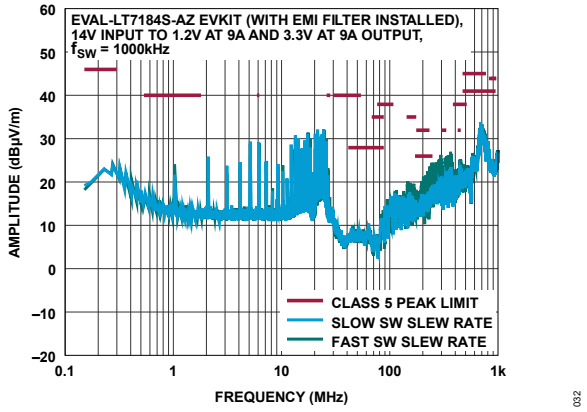

Figure 32. Radiated EMI Performance Full-Load (CISPR25 Radiated Emission Test with Class 5 Peak Limits)

BLOCK DIAGRAM

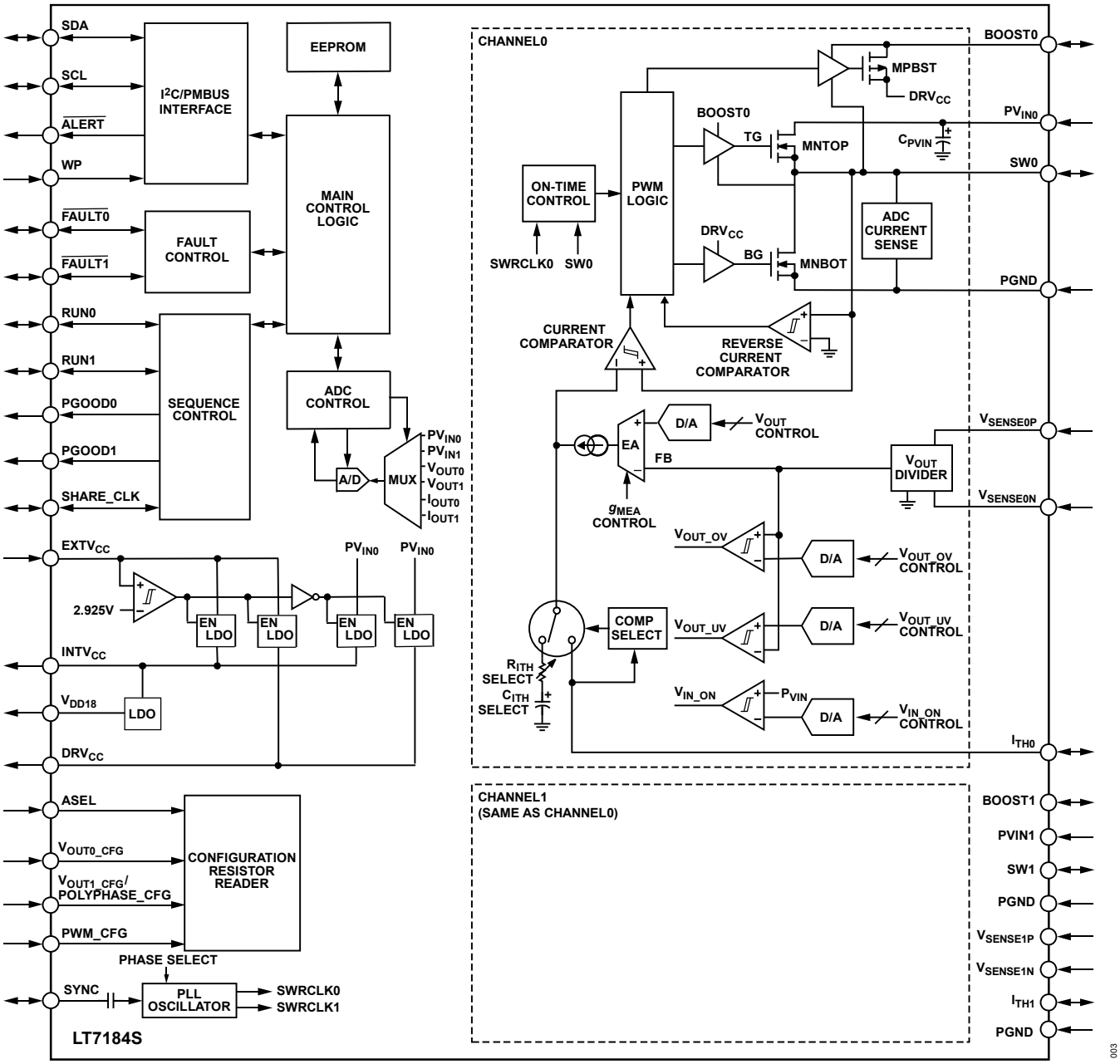

Figure 33. LT7184S Functional Block Diagram

THEORY OF OPERATION

Overview

The LT7184S is a dual-output monolithic PolyPhase DC/DC synchronous step-down regulator. The S in the LT7184S refers to the second-generation Silent Switcher® technology, which provides fast and clean switching edges, reduces overall solution size, improves efficiency, and minimizes EMI emissions. The I^2C-based serial interface is compatible with PMBus 1.3, which supports bus speeds up to 1MHz.

Major features include:

- Programmable Output Voltage.
- Programmable Current Limit.
- Programmable Switching Frequency.
- Programmable Output Overvoltage and Undervoltage Fault and Warning Thresholds.
- Programmable On and Off Delay Times.
- Programmable Output Rise/Fall Times.
- Programmable Control Loop Compensation.
- Programmable Input Undervoltage Threshold.
- Dedicated Power Good Output Pin for Each Channel.
- Phase-Locked Loop (PLL) for Synchronous, PolyPhase Operation (2, 3, 4, 6, or 8 Phases).
- Input and Output Voltage, Output Current, and Die Temperature Telemetry.
- Fully Differential Remote V_{OUT} Sense.
- Nonvolatile Configuration Memory (NVM) with Error Correcting Code (ECC).
- Nonvolatile Event-Based Fault Log.
- Optional External Configuration Resistors for Key Operating Parameters.
- Optional Time-Based Interconnect for Synchronization Between Multiple Devices.
- WP Pin to Write-Protect Internal Configuration.
- Standalone Operation using Configuration Resistors or NVM.

A variety of mechanisms for fault and warning handling are available. Fault and warning detection capabilities include:

- Output Undervoltage/Overvoltage Fault and Warning.
- Internal Overtemperature Fault and Warning.
- Communication, Memory, or Logic (CML) Fault.
- Input Overvoltage Fault and Undervoltage Warning.
- Output Overcurrent Fault and Warning.
- Internal Reference Fault.
- External Fault Detection via the Bidirectional $\overline{\text{FAULT}}$ Pins.

A dedicated $\overline{\text{ALERT}}$ pin is provided to indicate that faults or warnings have occurred.

Individual status commands enable fault and warning reporting to identify the specific event.

The LT7184S's $\overline{\text{FAULT}}$ pins enable fault sharing between channels and with other Analog Devices' power system management products, including the LTC3880, LTC2974, LTC2978, LTC4676 µModule®, etc. Fault reporting and shutdown behavior are fully configurable using the $\overline{\text{FAULT}}$ pins and the MFR_FAULT_PROPAGATE_LT7184S command. Faults can be individually masked, and the fault responses can be programmed to retry (unlatched) or latch off the regulator output.

Switching Regulator Control Loop

The LT7184S employs a controlled, on-time, valley current mode architecture. In normal operation, the internal top power Metal-oxide-semiconductor FET (MOSFET) is turned on for an interval determined by an on-time control circuit. When the top power MOSFET turns off, the bottom power MOSFET turns on until the valley current comparator trips, restarting the on-time control circuit and initiating the next cycle. The inductor current is determined by sensing the voltage drop across the bottom power MOSFET when it is on. The voltage on the I_{THN} pin sets the comparator threshold corresponding to the inductor valley current. The error amplifier (EA) adjusts the I_{TH} voltage by comparing the output voltage with an internal reference Digital-to-analog Converter (DAC) output. If the load current increases, the output voltage drops relative to the internal reference, which causes the I_{TH} voltage to rise until the average inductor current matches that of the load current.

An internal phase-locked loop synchronizes the oscillator frequency to an external clock signal if one is present on the SYNC pin. If no external clock is applied, the switching frequency is set by the FREQUENCY_SWITCH command, which may be initialized using configuration resistors (see the *Applications Information* section for more details).

Soft-Start

The LT7184S has two Pulse Width Modulation (PWM) modes of operation: Pulse-skip mode (PSM) and Forced continuous mode (FCM). Pulse-skip mode is only used during soft-start while the output voltage rises to the programmed regulation voltage. During PSM or discontinuous operation, the inductor current cannot be reversed. The reverse current comparator turns off the bottom switch when the inductor current reaches zero, preventing the inductor current from going negative and discharging the output. During discontinuous operation, the power MOSFETs remain off while the output capacitor supplies the load current. The LT7184S switches again when the I_{TH} voltage rises above the zero current level to initiate the next cycle as either the internal reference voltage rises above the V_{SENSE} voltage with the soft-start ramp, or the load discharges the V_{SENSE} voltage.

When all conditions required for startup have been met, and a channel is enabled with an OPERATION command or when the RUN pin is raised, a soft-start ramp begins. The soft-start ramp time is set by the TON_RISE command, which is 1ms by default. The soft start ramp begins after a programmable delay (TON_DELAY, default 0ms). Once the output voltage reaches the programmed regulation voltage (VOUT_COMMAND), the PGOOD flag is set, and the operating mode automatically switches to the FCM mode of operation.

FCM mode – where the inductor always conducts current, reversing below zero for some portion of the switching cycle when the average output current is below the ripple current and either the top or bottom power MOSFETs are always on - is also called as Continuous conduction mode (CCM). In this constant on-time current mode control architecture, the inductor valley current is always determined by the voltage on the I_{TH} node. The I_{TH} node voltage varies from about 0.6V to 1.5V depending on the load, with the zero load current when the I_{TH} voltage is about 980mV. When programmed to use internal compensation (I_{TH} pin connected to INT_{VCC}), the I_{TH} node is not visible on the I_{THN} pin. When a compensation network is connected to the I_{THN} pin at startup, the LT7184S uses the user-supplied compensation to control the loop dynamics. Care must be used in selecting compensation network components for correct operation.

EEPROM

The LT7184S contains internal EEPROM to store nonvolatile user configuration settings and fault log information.

The integrity of the onboard EEPROM is protected with ECC and checked with a cyclic redundancy check (CRC) calculation after a power-on, reset, or execution of a RESTORE_USER_ALL command. If an invalid CRC is detected, the $\overline{\text{ALERT}}$, SHARE_CLK, PGOOD, and RUN pins are pulled low, and both output channels remain disabled until the issue is resolved.

Refer to the *LT7184S PMBus/I²C Reference Manual* or contact the factory for details on efficient in-system EEPROM programming, including bulk EEPROM programming.

Power-up and Initialization

The LT7184S is capable of stand-alone supply sequencing and controlled turn-on and turn-off operation. It operates from either a single input supply or two independent input supplies (PV_{IN0} and PV_{IN1}). To reduce LT7184S power dissipation, $EXTV_{CC}$ can be driven with an external 3V to 5.5V supply or connected to an output of the LT7184S that provides 3V to 5.5V. If $EXTV_{CC}$ is connected to 3V to 5.5V, the supported PV_{IN0} input operating range is 1.5V to 16V. Without $EXTV_{CC}$, the PV_{IN0} operating range is 2.9V to 16V. The PV_{IN1} operating range is 1.5V to 16V. PV_{IN1} and $EXTV_{CC}$ or PV_{IN0} must be powered for Channel 1 to operate. $EXTV_{CC}$, $PV_{IN0,}$ and PV_{IN1} may be applied in any order without concern for power supply sequencing of the LT7184S.

The LT7184S is initialized upon application of power to PV_{IN0} or $EXTV_{CC}$ or when an MFR_RESET or RESTORE_USER_ALL command is sent. In the initialization step, the LT7184S reads the EEPROM configuration and/or resistor configuration pins to set the initial state of the PMBus commands.

During initialization, both channels, V_{SENSEP} and V_{SENSEN} pins, are tested for continuity by pulling up and down on V_{SENSEP} and only pulling up on V_{SENSEN} with a weak current for a short time window. If any of the V_{SENSE} pins are found to be high impedance, MFR_DISABLE_OUTPUT is asserted for both channels. This feature protects a system from overvoltage if a V_{SENSE} connection becomes open. Also, during initialization, the PGOODN pins are held low, SHARE_CLK is held low, the RUNN pins are pulled down with 1.5mA (typical), and the $\overline{FAULTN}$ pins are in a high-impedance state.

If the CFG resistor configuration pins are enabled, the LT7184S initializes certain commands based on the configuration resistor values, which supersede the EEPROM settings. Resistor configuration pins are enabled by factory default. Clear Bit 6 of MFR_CONFIG_ALL_LT7184S in EEPROM to disable CFG pins. See *Using Resistor Configuration Pins* in the *Applications Information* section for more details. For commands that are not initialized based on the configuration resistors, initial values are determined by EEPROM or factory defaults.

LT7184S initialization typically requires 13ms. If CFG pins are disabled (MFR_CONFIG_ALL_LT7184S bit 6 set to 1 in EEPROM), the initialization time is reduced to 10ms (typical).

After initialization is complete, comparators monitor PV_{IN0} and PV_{IN1}. The PV_{IN} voltage must exceed the channel's programmable V_{IN_ON} threshold for the channel to operate. By default, SHARE_CLK will be held low until PV_{IN0} exceeds V_{IN_ON} for PAGE0 or if PV_{IN0} falls below V_{IN_OFF}. By default, PV_{IN1} does not affect SHARE_CLK. The default behavior for both channels is to turn off and remain off if SHARE_CLK is low. Refer to the MFR_CHAN_CONFIG_LT7184S command in the *LT7184S PMBus/I²C Reference Manual* for information on configuring this behavior.

The RUN pin pull-down current (1.5mA typical) is released by the LT7184S after the device completes POR initialization and the first time the channel's PV_{IN} potential exceeds the V_{IN_ON} threshold.

Shutdown

The LT7184S can be programmed to turn off immediately or to sequence off.

When sequencing off, the LT7184S waits for the turn-off delay and then performs a soft-stop ramp in which the regulation target voltage is ramped down to zero. The turn-off delay is set by the TOFF_DELAY command, defaulting to 0ms. The target voltage ramp-down time is set by the TOFF_FALL command, defaulting to 2ms.

Sequencing off occurs if the OPERATION command is set to 0x40, or the RUN pin is de-asserted, and ON_OFF_CONFIG Bit 0 is set to 0, and Bit 2 is set to 1.

When immediate turn-off occurs, the regulator quickly ramps the inductor current to zero and then stops switching. In this case, the output voltage decays based only on the load current and the internal 260Ω pull-down resistor from $V_{SENSENP}$ to $V_{SENSENN}$. Immediate shutdown occurs in any of the following situations:

- PV_{IN} falls below the V_{IN_OFF} threshold.
- If the OPERATION command is cleared to 0x00, if ON_OFF_CONFIG bit 3 is set to 1.
- A fault condition occurs, which causes the output to turn off.

- The RUNN pin is de-asserted, and ON_OFF_CONFIG has been configured such that the RUN pin de-assertion causes immediate shutdown (ON_OFF_CONFIG Bit 0 and Bit 2 both set to 1).
- The $\overline{\text{FAULTN}}$ pin for the channel is pulled low externally unless MFR_FAULT_RESPONSE has been cleared to 0x00.
- Loss of SHARE_CLK, unless Bit 2 of MFR_CHAN_CONFIG_LT7184S has been cleared.

Warning and Fault Handling

The LT7184S continuously monitors the system for fault and warning conditions. The Fault responses are configurable using the corresponding FAULT_RESPONSE commands, such as VOUT_UV_FAULT_RESPONSE, VOUT_OV_FAULT_RESPONSE, etc. The possible list fault responses are as follows:

- Continue Operation (ignore).
- Shut down immediately and retry if the fault condition is no longer present.
- Shut down immediately and latch off.

The remainder of this section describes the factory default warning and fault behavior. See *Table 6*. Refer to the *LT7184S PMBus/I²C Reference Manual* for details on configuring fault and warning behavior. All faults and warnings are indicated in PMBus STATUS commands.

When a warning occurs related to output voltage, output current, or temperature, the LT7184S pulls the $\overline{\text{ALERT}}$ pin low, the corresponding bit is set in the appropriate STATUS command(s), and the channel continues to operate.

If the output falls below VOUT_UV_FAULT_LIMIT, the LT7184S responds as follows:

- The channel's PGOODN pin is pulled low.
- The ALERT pin is pulled low.
- The VOUT_UV fault bit is set in the STATUS_VOUT, STATUS_BYTE, and STATUS_WORD commands.
- The channel continues to operate while limiting the maximum valley current.

If a fault occurs due to an output overvoltage or input overvoltage, the LT7184S responds as follows:

- The faulted channel(s) are shut down immediately.
- The channel's $\overline{\text{FAULTN}}$ pin and PGOODN pin are pulled low.
- The $\overline{\text{ALERT}}$ pin is pulled low.
- The corresponding indicator bit(s) are set in the appropriate STATUS command(s).
- After 10ms (time defined by MFR_RETRY_DELAY), the channel attempts to restart when the fault condition is no longer present.

If a fault occurs due to overtemperature, the LT7184S responds as follows:

- Both channels are shut down immediately.
- Both channels' $\overline{\text{FAULTN}}$ pins and PGOODN pins are pulled low.
- The $\overline{\text{ALERT}}$ pin is pulled low.
- The overtemperature (OT) bit is set in the appropriate STATUS commands.
- When the ADC measures that the temperature is below the overtemperature threshold, the channel attempts to restart.

The LT7184S periodically compares the primary internal voltage reference against a secondary internal voltage reference using the Analog-to-digital converter (ADC). If a failure is detected, the LT7184S responds as follows:

- Both channels are shut down immediately
- The $\overline{\text{FAULTN}}$ pins, PGOODN pins, and $\overline{\text{ALERT}}$ pins are all pulled low.
- The internal reference fault bit is set in the STATUS commands.
- Both channels remain off unless the reference recovers (for example, due to temperature drift), a RESTOR_USER_ALL or MFR_RESET command is received, or input power is removed from both PV_{IN0} and $EXTV_{CC}$.

$\overline{\text{FAULT}}$ PINS

A fault will cause the $\overline{\text{FAULTN}}$ pin to pull low if the corresponding FAULT_RESPONSE command is programmed to shut down the regulator output and the MFR_FAULT_PROPAGATE_LT7184S command is configured to propagate the fault to the open drain $\overline{\text{FAULTN}}$ pin.

Once the LT7184S pulls down a $\overline{\text{FAULTN}}$ pin, the device will continue to hold the pin low until one of the following occurs:

- The channel retries for faults that are configured to retry.
- The faulted channel is disabled and then re-enabled.
- A RESTORE_USER_ALL or MFR_RESET command is received.
- Input power is removed from both PV_{IN0} and $EXTV_{CC}$.

The $\overline{\text{FAULTN}}$ pin can also be used as an input to provide a method for the LT7184S to respond to external faults. The channel turns off immediately if the channel's $\overline{\text{FAULTN}}$ pin is pulled low externally. This enables the coordination of faults among multiple power systems management products.

PGOOD PINS

The open-drain PGOODN pins are each pulled low if the corresponding channel is off for any reason, during soft-start and soft-stop, or if the output voltage is below the VOUT_UV_FAULT_LIMIT or above the VOUT_OV_FAULT_LIMIT.

$\overline{\text{ALERT}}$ PIN

The SMBALERT_MASK command configures which warning and fault indicators cause the LT7184S to pull down the open drain $\overline{\text{ALERT}}$ pin. Once the LT7184S pulls down the $\overline{\text{ALERT}}$ pin, the device will continue to hold the pin low until one of the following occurs:

- The faulted channel is disabled and then re-enabled.
- A CLEAR_FAULTS, RESTORE_USER_ALL or MFR_RESET command is received.
- All unmasked status bits are cleared by writing a 1 to each Bit.
- The LT7184S successfully transmits its address during a PMBus Alert Response Address (ARA).
- Input power is removed from both PV_{IN0} and $EXTV_{CC}$.

$\overline{\text{FAULT}}$ Event Logging

If a fault condition occurs that is configured to turn off the regulator output, an event is written in the fault log in EEPROM. Any preceding warning or fault that is not configured to turn off the output is written as a sub-event when an event is written. A timestamp is written with each event and sub-event. The fault log stores up to three fault-off events. The fault log may be read by the MFR_FAULT_LOG command. The fault log is cleared from EEPROM by writing the MFR_FAULT_LOG_CLEAR command. The fault log function is enabled by default and may be disabled by clearing Bit 7 of the MFR_CONFIG_ALL command. Refer to the MFR_FAULT_LOG command in the *LT7184S PMBus/I²C Reference Manual* for more details.

Table 6. Factory Default Warnings and Fault Behavior

WARNING OR FAULT TYPE[1]	DETECTION METHOD	DEFAULT THRESHOLD	DEFAULT REGULATOR RESPONSE	DEFAULT PIN RESPONSE		
				PGOODN	$\overline{\text{FAULTN}}$	$\overline{\text{ALERT}}$
V_{OUT} UV Warning	V_{SENSE} comparator	VOUT_COMMAND - 6.5%	Continue operation			Pull low
V_{OUT} OV Warning	V_{SENSE} comparator	VOUT_COMMAND + 7.5%	Continue operation			Pull low
V_{OUT} UV Fault	V_{SENSE} comparator	VOUT_COMMAND - 7%	Continue operation	Pull low		Pull low

WARNING OR FAULT TYPE[1]	DETECTION METHOD	DEFAULT THRESHOLD	DEFAULT REGULATOR RESPONSE	DEFAULT PIN RESPONSE		
				PGOODN	$\overline{\text{FAULTN}}$	$\overline{\text{ALERT}}$
V_{OUT} OV Fault	V_{SENSE} comparator	VOUT_COMMAND + 10%	Shutdown and retry	Pull low	Pull low	Pull low
V_{IN} OV Fault	PV_{IN} comparator	17.6V	Shutdown and retry	Pull low	Pull low	Pull low
V_{IN} UV Warning	ADC	-1V (disabled)	Continue operation			Pull low
OT Warning	ADC	140°C	Continue operation			Pull low
OT Fault	ADC	160°C	Shutdown and retry	Pull low	Pull low	Pull low
IOUT Overcurrent (IOUT_OC) Warning	ADC	I_{AVG} > 9A	Continue operation			Pull low
IOUT_OC Fault	I_{TH} comparator	V_{ITH} ≥ 1.6V[2]	Continue operation	Pull low	Pull low	Pull low
Turn-On Time (TON_MAX) Fault	V_{SENSE} comparator and timer	5ms without exceeding VOUT_UV_FAULT_LIMIT	Continue operation	Pull low		Pull low
Turn-Off Time (TOFF_MAX) Warning	ADC and timer	0 (Disabled)	N/A			
Pin Configuration Error[3]	I/O	N/A	Lock off until the next reset	Pull low	Pull low	Pull low
EEPROM Error	CRC, ECC	N/A	Lock off until the next reset	Pull low		Pull low
Internal Reference Fault	ADC and second reference	±5%	Shutdown and retry	Pull low	Pull low	Pull low
PMBus/I²C Communications Error (CML)	Logic	N/A	N/A			Pull low

[1] Refer to the *LT7184S PMBus/I²C Reference Manual* for detailed information, including configuring thresholds and responses.

[2] The IOUT_OC_FAULT valley current threshold is controlled by MFR_PWM_MODE_LT7184S bits [10:9], and the IOUT_OC analog comparator trips at typically 95% of the valley current limit programmed by these bits.

[3] When a pin configuration error is detected during initialization, the device pulls low the following pins: $\overline{\text{FAULT0}}$, $\overline{\text{FAULT1}}$, RUN0, RUN1, SHARE_CLK, PGOOD0, PGOOD1, and $\overline{\text{ALERT}}$.

APPLICATIONS INFORMATION

Using Resistor Configuration Pins

The LT7184S has four resistor configuration pins, each using a single ±1% resistor to select key operating parameters. The resistor configuration pins are ASEL, V_{OUT0_CFG}, V_{OUT1_CFG}, and PWM_CFG. The resistance from each of these pins to GND is measured upon power-up and/or execution of a RESTORE_USER_ALL or MFR_RESET command. The function of each resistor configuration pin is described in the following sections.

If bit 6 of the MFR_CONFIG_ALL_LT7184S command is set to 1 in EEPROM, the configuration resistors are ignored on V_{OUT0_CFG}, V_{OUT1_CFG}, and PWM_CFG while the ASEL resistor is always respected. Refer to the MFR_ADDRESS command in the *LT7184S PMBus/I²C Reference Manual* for information about setting the serial interface device address, including ASEL configuration resistor selection.

Setting Output Voltage

The VOUT_COMMAND specifies the output voltage when the channel is enabled. VOUT_COMMAND can be initialized using resistors on the V_{OUT0_CFG} and V_{OUT1_CFG} pins based on the values in *Table 7*. A resistor between V_{OUT0_CFG} and GND configures channel 0. If Channel 1 is configured as an independent output from Channel 0, then a resistor between V_{OUT1_CFG} and GND configures Channel 1. If PolyPhase configuration is selected (by connecting a 5.6kΩ ±10% resistor between PWM_CFG and GND), then V_{OUT0_CFG} configures both Channels 0 and 1, and V_{OUT1_CFG} is repurposed to configure the PolyPhase operation.

Table 7. V_{OUTN_CFG} Pin Configuration Resistor Selection

RESISTOR VALUE (±1%)[1]	OUTPUT VOLTAGE SET POINT (V)[2]	V_{OUT} RANGE MODE[3]	REGULATOR ENABLE[4]
Floating or V_{DD18}[5]	Initialized from NVM (Default 0.5V)	Initialized from NVM (Default full V_{OUT} range)	Initialized from NVM
124kΩ	5V	Full V_{OUT} range, Supports $0.4V \le V_{OUT} \le 5.5V$	Regulator is enabled if RUN is asserted high. (OPERATION = 0x80, ON_OFF_CONFIG initialized from NVM, default requires OPERATION = 0x80 and RUN pin asserted)
107kΩ	3.3V		
93.1kΩ	2.5V		
80.6kΩ	1.8V		
69.8kΩ	1.5V		
60.4kΩ	1.35V		
51.1kΩ	1.2V	High-performance low-V_{OUT} mode if set in NVM. Offers enhanced accuracy and transient response for $0.6V \le V_{OUT} \le 1.375V$	
43.2kΩ	1.1V		
36.5kΩ	1.0V		
30.9kΩ	0.9V		
25.5kΩ	0.85V		
21kΩ	0.8V		
16.5kΩ	0.75V		
11.8kΩ	0.7V		
6.65kΩ	0.6V		
0 (GND)	Initialized from NVM (default 0.5V)	Initialized from NVM (default full V_{OUT} range)	Regulator disabled and RUN pin ignored.

[1] If the PWM_CFG pin is connected to a 5.6kΩ ±10% resistor to select PolyPhase operation (See *Table 9*), then the V_{OUT1_CFG} configuration resistor controls PWM settings, including frequency and phase (See *Table 10*).

[2] Output voltage set point is controlled by VOUT_COMMAND.

[3] V_{OUT} Range Mode selection is controlled by MFR_PWM_MODE_LT7184S bit 1. A value of 1 selects high-performance Low V_{OUT} Mode, when this bit is set the output voltage cannot be programmed above 1.375V.

[4] The PMBus ON_OFF_CONFIG command selects whether the RUN pin and/or OPERATION command enables the regulator.

[5] If the V_{OUTN_CFG} pin is open or tied to V_{DD18}, the VOUT_COMMAND is loaded from EEPROM to determine the output voltage. The default EEPROM setting is to initialize with the regulator disabled unless the voltage configuration resistors are installed. The commands listed below are initialized based on a percentage of VOUT_COMMAND if the resistor configuration pins are used to initialize the output voltage.

Table 8. Command Initialization Defaults when Resistor Configuration Pins are used

COMMAND	DEFAULT % of VOUT_COMMAND
VOUT_OV_FAULT_LIMIT	+10%
VOUT_OV_WARN_LIMIT	+7.5%
VOUT_MAX	+7.5%
VOUT_MARGIN_HIGH	+5%
VOUT_MARGIN_LOW	-5%
VOUT_UV_WARN_LIMIT	-6.5%
VOUT_UV_FAULT_LIMIT	-7%

Switching Frequency and Phase

The PWM switching frequency can be established using the internal oscillator or applying an external clock on the SYNC pin. An internal phase-locked loop (PLL) synchronizes PWM control to this timing reference, whether the clock is provided internally or externally. The internal oscillator frequency is set by the FREQUENCY_SWITCH command. The MFR_PWM_PHASE_LT7184S command configures the phase of each channel.

The SYNC pin is a flexible multipurpose input/output pin, which can be used as a clock input or output. The LT7184S synchronizes PWM switching to an external clock input on SYNC unless the LT7184S has been configured as an output driver or has been programmed to ignore the input clock. The LT7184S continues PWM operation using its own internal oscillator if the external clock signal is lost. If an external clock is to be used, it is recommended to program the FREQUENCY_SWITCH command or to use a configuration resistor to set the internal oscillator frequency to a similar value as the external clock frequency. This ensures that the PWM switching frequency remains reasonable if the external clock is lost. The LT7184S can be programmed to ignore an external clock by writing a 1-to-Bit 1 of MFR_SYNC_CONFIG_LT7184S.

For an input clock frequency below 625kHz, it is recommended to use a configuration resistor that selects a PWM frequency of 500kHz. For an input clock frequency between 625kHz and 1.25MHz, it is recommended to use a configuration resistor that selects a PWM frequency of 1MHz. For an input clock frequency between 1.25MHz and 2.5MHz, it is recommended to use a configuration resistor that selects a PWM frequency of 2MHz. For an input clock frequency greater than 2.5MHz, it is recommended to use a configuration resistor that selects a PWM frequency of 4MHz.

The LT7184S can be configured to provide a synchronizing clock output on the SYNC pin to other devices by setting bit 0 of MFR_SYNC_CONFIG_LT7184S to 1. If the SYNC output clock is enabled, the LT7184S drives the SYNC pin as a square wave from 0V to 1.88V (typical) at the frequency programmed in FREQUENCY_SWITCH, leads the phase of

the PWM output by the value set in MFR_PWM_PHASE_LT7184S command. Only one device connected to SYNC may be configured as an output. When a clock is applied to SYNC, the MFR_PWM_PHASE_LT7184S command specifies the phase relationship between the rising edge of SYNC and the rising edge of SW for the channel.

The switching frequency of each channel of the LT7184S may be independently programmed to double the SYNC clock frequency or the FREQUENCY_SWITCH frequency by setting bit 15 of the MFR_PWM_MODE_LT7184S to 1. To prevent the switching frequency from exceeding 4MHz when bit 15 is set to 1, the FREQUENCY_SWITCH command is limited to 2MHz. If the FREQUENCY_SWITCH command is set to a value greater than 2MHz, then the user is prevented from setting Bit 15 to 1. When programming the 2x switching frequency, do not apply a clock with a frequency of more than 2MHz to the SYNC pin.

Table 9. PWM_CFG Pin Configuration Resistor Selection[8]

RESISTOR VALUE (±1%)	PWM FREQUENCY[1,2]	PWM PHASE[3]		POLYPHASE FOLLOWER/ LEADER[4]	INTERNAL COMPENSATION[5]			SYNC CLOCK OUTPUT or INPUT[7]
		CH0	CH1		C_{ITH}	R_{ITH}	g_{MEA}	
Floating or V_{DD18}	Initialized from NVM (default 1MHz)	Initialized from NVM (default 0°)	Initialized from NVM (default 180°)	Initialized from NVM (default 0 Leader)	Initialized from NVM (default 165pF)	Initialized from NVM (default 14kΩ)	Initialized from NVM (default 310µS)	Initialized from NVM (default Input)
124kΩ	500kHz	0°	180°	0 (Leader)	165pF	60kΩ	155µs	0 (Input)
80.6kΩ	1.5MHz				145pF	10kΩ	465µs	
51.1kΩ	2MHz				145pF	10kΩ	465µs	
30.9kΩ	4MHz				95pF	10kΩ	930µs	
107kΩ	500kHz	90°	270°		165pF	60kΩ	155µs	
69.8kΩ	1MHz				165pF	14kΩ	310µs	
43.2kΩ	2MHz				145pF	10kΩ	465µs	
5.6KΩ ±10%	PolyPhase configuration: PWM Configuration is controlled by the V_{OUT1_CFG} pin, as shown in *Table 10*. In this configuration, V_{OUT} for both channels is initialized to the value specified by the V_{OUT0_CFG} resistor.							

[1] PWM Switching frequency set point is controlled by the FREQUENCY_SWITCH command if no SYNC clock is present.

[2] In an external synchronization clock, as well as a configuration resistor, the configuration resistor should be chosen to set the internal PWM switching frequency to a similar value as the input clock frequency.

[3] Steady-state PWM switching phase is controlled by MFR_PWM_PHASE_LT7184S.

[4] POLYPHASE® follower/leader mode is controlled by MFR_CHAN_CONFIG_LT7184S bit 8. A value of 1 selects follower mode.

[5] Internal compensation is selected by connecting the I_{TH} pin to $INTV_{CC}$. For PWM_CFG resistor values ≤ 124kΩ, if external compensation is used, g_{MEA} is set to the maximum value (5.0ms for high-performance low-V_{OUT} Mode; 1.24ms for standard mode). For internal compensation, C_{ITH} is controlled by MFR_PWM_MODE_LT7184S bits [8:6], R_{ITH} is controlled by MFR_PWM_MODE_LT7184S bits [5:3], and g_{MEA} is controlled by MFR_PWM_MODE_LT7184S Bits [13:11]. When the NVM configuration selects high-performance Low V_{OUT} mode, the error amp transconductance (g_{MEA}) is multiplied by about 4.

[6] The SYNC pin is a clock output when the MFR_SYNC_CONFIG_LT7184S Bit 0 is set to 1.

[7] The NVM default for MFR_PWM_MODE_LT7184S bits [13:11] is 0b001, which corresponds to g_{MEA} = 1250µs for high-performance low-V_{OUT} mode and g_{MEA} = 310µs for standard mode, regardless of internal or external compensation.

[8] The PWM_CFG resistor selection is performed with a table lookup function within the device on power-up. Use only 1% resistors for the PWM_CFG resistor selection as shown in *Table 9*, or program the devices using the PMBus commands and NVM.

PolyPhase Load Sharing

Multiple LT7184S channels can be connected in parallel to provide a balanced PolyPhase load-share solution. The analog current mode control architecture of the LT7184S ensures that load-sharing remains balanced among the PolyPhase channels.

The corresponding I_{THN}, $\overline{FAULTN}$, PV_{IN}, $V_{SENSENP}$, and $V_{SENSENN}$ pins must be connected among all PolyPhase channels, and the SYNC and SHARE_CLK pins must be connected among all PolyPhase devices. The PWM switching phases should be separated by 360°/n degrees, where n is the number of phases in the PolyPhase array. In PolyPhase, exactly one device, either an LT7184S or an external clock source, must be configured to drive a clock on the common SYNC node.

In a PolyPhase array, exactly one LT7184S channel must be configured as a leader (MFR_CHAN_CONFIG_LT7184S Bit 8 set to 0), and all other PolyPhase channels must be configured as followers (Bit 8 set to 1).

The PolyPhase mode can be selected by connecting a 5.6kΩ ±10% resistor from PWM_CFG to GND if MFR_CONFIG_ALL_LT7184S Bit 6 is not set to ignore CFG pins. Resistor configuration options are available to support 2, 3, 4, or 6-phase PolyPhase solutions. When a 5.6kΩ resistor is connected on PWM_CFG, VOUT_COMMAND for Channel 1 is set to the same value as Channel 0 based on the V_{OUT0_CFG} resistor, and the V_{OUT1_CFG} resistor selects the PolyPhase configuration as shown in *Table 10*. For 2, 4, or 6-phase operation, the PWM_CFG pins of up to three LT7184S devices may be connected to a single 5.6k resistor. *Figure 34* illustrates two LT7184S devices configured for 4-phase operation. Separate PWM_CFG configuration resistors are required, as shown in *Typical Applications*, for PolyPhase arrays with 8 phases. PMBus programming is required for at least some of the devices in arrays with more than 6 phases: to set PolyPhase follower mode (MFR_CHAN_CONFIG_LT7184S Bit 8) and select the appropriate phase (MFR_PWM_PHASE_LT7814S) for every Channel in a large PolyPhase array.

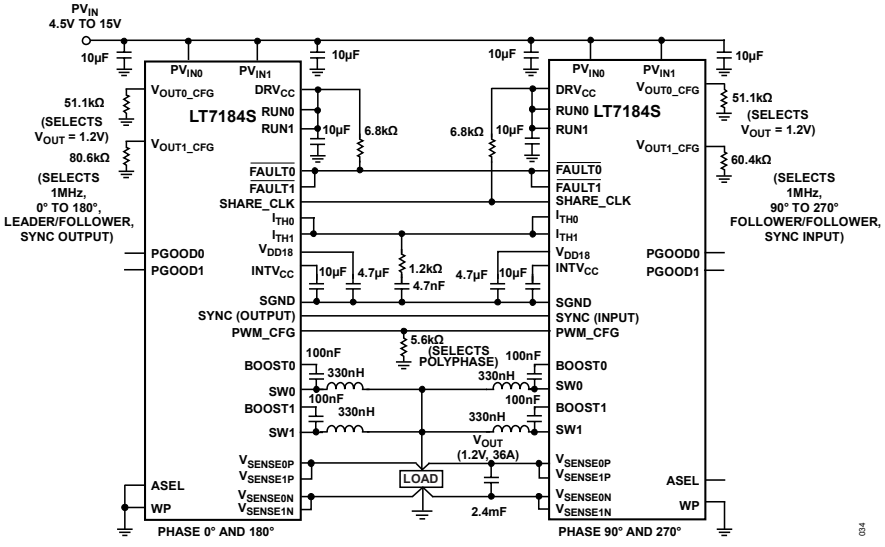

Figure 34.4-Phase PolyPhase 1.2V/36A Regulator

Table 10. PolyPhase Operation VOUT1_CFG Pin Configuration Resistor Selection

RESISTOR VALUE (±1%)[1]	PWM FREQUENCY[2]	PWM PHASE[3]		POLYPHASE® FOLLOWER[4]		SYNC CLOCK: OUTPUT / INPUT[5]
		CH0	CH1	CH0	CH1	
Floating or V_{DD18}	Initialized from NVM (default 1MHz)	Initialized from NVM (default 0°)	Initialized from NVM (default 180°)	Initialized from NVM (default 0, leader)		Initialized from NVM (default 0, input)
124kΩ	500kHz	0°	180°	0 (leader)	1 (follower)	1 (output)
80.6kΩ	1MHz					
36.5kΩ	2MHz					
16.5kΩ	4MHz					
107kΩ	500kHz					0 (input)
69.8kΩ	1MHz					
30.9kΩ	2MHz					
11.8kΩ	4MHz					
93.1kΩ	500kHz	90°	270°	1 (follower)	1 (follower)	
60.4kΩ	1MHz					
25.5kΩ	2MHz					
6.65kΩ	4MHz					
51.1kΩ	1MHz	120°	240°			1 (output)
21.0kΩ	2MHz					
43.2kΩ	1MHz	60°	300°			0 (input)
0kΩ (GND)	2MHz					

[1] *Table 10* applies only if PWM_CFG is connected to a 5.6kΩ configuration resistor. Otherwise, V_{OUT1_CFG} controls the output voltage for Channel 1 according to *Table 7*.

[2] PWM switching frequency is controlled by the FREQUENCY_SWITCH and MFR_PWM_MODE_ LT7184S Bit 15, if no SYNC input clock is present.

[3] Steady-state PWM switching phase is controlled by MFR_PWM_PHASE_LT7184S.

[4] POLYPHASE® follower mode is controlled by MFR_CHAN_CONFIG_LT7184S bit 8. A value of 1 selects follower mode, and a value of 0 selects leader mode. Exactly one channel must be selected as a leader.

[5] The SYNC pin is a clock output when MFR_SYNC_CONFIG_LT7184S bit 0 is set to 1.

Configuring Device Address with ASEL Pin

The MFR_ADDRESS command byte and ASEL pin set the 7-Bit device address on the PMBUS. Setting this command to a value of 0x80 disables device addressing. The GLOBAL device address, 0x5A and 0x5B, cannot be deactivated. If the ASEL pin is floating or connected to V_{DD18}, the device uses the full MFR_ADDRESS value. If a resistor is connected to ASEL according to *Table 10*, the four LSBs of the device address are determined by the ASEL resistor value.

Reading MFR_ADDRESS always returns the value loaded from EEPROM or written via PMBSus write. The value read from the MFR_ADRESS is not affected by the ASEL pin. The LT7184S does not ignore the ASEL pin, even when MFR_CONFIG_ALL_LT7184S is set to ignore the other resistor configuration pins. The 3 MSBs 6:4 of the device address are always determined by 6:4 of MFR_ADDRESS.

Table 11. ASEL Configuration Resistor and LSBs of Device Address

ASEL Resistor	PMBus Device Address
Floating or V_{DD18}	EEPROM
124kΩ	0x4F
107kΩ	0x4D
93.1kΩ	0x4D
80.6kΩ	0x4C
69.8kΩ	0x4B
60.4kΩ	0x4A
51.1kΩ	0x49
43.2kΩ	0x48
36.5kΩ	0x47
30.9kΩ	0x46
25.5kΩ	0x45
21.0kΩ	0x44
16.5kΩ	0x43
11.8kΩ	0x42
6.65kΩ	0x41
0 (grounded)	0x40

Operating Frequency Trade-Offs

The selection of the operating frequency is a trade-off between efficiency, component size, and input voltage range. The advantage of high-frequency operation is that smaller inductor and capacitor values may be used, while the primary disadvantage is lower efficiency and reduced maximum input voltage to avoid minimum on-time and minimum off-time.

Minimum On-Time and Minimum Off-Time Considerations

The minimum on-time, $t_{ON(MIN)}$, is the smallest duration of time in which the top power MOSFET can be in its on state. This time is a function of input and output voltage, switching frequency, and output load current, and typically, the smallest value that the LT7184S can support is about 25ns at 1A load. In continuous conduction, the worst-case minimum on-time limit imposes a maximum switching frequency of:

$$f_{SW\,MAX} = \frac{V_{OUT}}{V_{IN} \times 40ns} \quad (1).$$

Where 40ns corresponds to the worst-case upper limit of $t_{ON(MIN)}$ at no load, the maximum junction temperature is 150°C, and $f_{SW(MAX)}$ is the maximum supported switching frequency. If the frequency is set higher than $t_{ON(MIN)}$ allows, the LT7184S valley current control architecture keeps the output voltage in regulation, and the switching frequency decreases from it is programmed value. This is an acceptable result in many applications, so this constraint may not be of critical importance. High switching frequencies may be used in the design without causing output over-voltage. However, if frequency synchronization is required (such as in PolyPhase applications), f_{SW} should be set no higher than the maximum value achievable at the maximum $t_{ON(MIN)}$ of 40ns and the maximum PV_{IN} and minimum V_{OUT} for the application. Note that $t_{ON(MIN)}$ decreases with load current and increases with negative loads.

The minimum off-time, $t_{OFF(MIN)}$, is the smallest amount of time that the LT7184S can turn on the bottom power MOSFET, tripping the current comparator, and turning the bottom power MOSFET back off. This time is typically about 85ns. The minimum off-time imposes a maximum duty cycle of $t_{ON}/(t_{ON}+t_{OFF(MIN)})$. If the ratio V_{OUT}/PV_{IN} exceeds the maximum duty cycle, for example, due to an input voltage dropping, then the output voltage drops out of regulation.

To avoid the output voltage dropping out of regulation due to the $t_{OFF(MIN)}$ limitation, the switching frequency should be set to no higher than:

$$f_{SW} \leq \frac{\left(1-\frac{V_{OUT\,(MAX)}}{V_{IN\,(MIN)}}\right)}{120ns} \quad (2).$$

Based on the minimum input voltage and maximum output voltage for the application. Note that the 120ns in Equation 2 corresponds to the maximum $t_{OFF(MIN)}$ for the LT7184S at maximum junction temperature of 150 °C.

PROGRAMMABLE CURRENT LIMIT

The LT7184S current limit operates by limiting the output current based on the valley of the inductor current ripple waveform, as shown in *Figure 35* and *Figure 36*. As shown in *Figure 35*, when the positive valley current limit is engaged (providing an output current to the load), the inductor valley current is at $I_{LIM-POS}$, while the average output current is $I_{LIM-POS} + \Delta I_L/2$, and the peak inductor current is $I_{LIM-POS} + \Delta I_L$, where ΔI_L is the inductor ripple current. If $I_{LIM-POS}$ is reached, the IOUT_OC fault STATUS bit is set. Refer to the STATUS commands in the *LT7184S PMBus/I²C Reference Manual*.

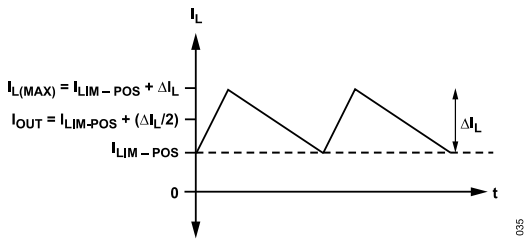

Figure 35. I_{LIM} (POS)

As shown in *Figure 36*, when negative valley current limit occurs (sinking output current due to the output being pulled up externally), the inductor valley current is $I_{LIM-NEG}$, the average output current is $I_{LIM-NEG} + \Delta I_L/2$, and the peak inductor current is $I_{LIM-NEG} + \Delta I_L$.

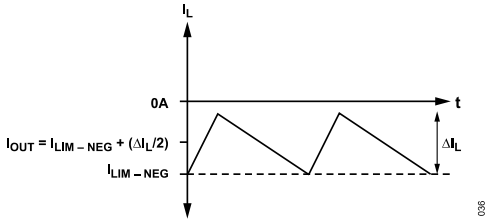

Figure 36.ILIM(NEG)

The LT7184S offers four settings for the valley's current limits. The valley current limit selection is controlled by MFR_PWM_MODE_LT7184S bits [10:9], as shown in *Table 12*. The factory default current limit setting is 9A (typical) positive valley current limit and -7.5A (typical) negative valley current limit. Note that the modulator's current sense gain (dI_{OUT}/dV_{ITH}) is also changed as the current limit selection is changed, which must be considered when optimizing control loop compensation. The valley Current Limits are affected by V_{OUT}/L (V/µH) and operating frequency. See the *Typical Performance Characteristics* for more information.

Table 12. Valley Current Limit Selection: MFR_PWM_MODE_LT7184S bits [10:9]

VALUE	POSITIVE VALLEY CURRENT LIMIT: $I_{LIM-POS}$ (TYP)	NEGATIVE VALLEY CURRENT LIMIT: $I_{LIM-NEG}$ (TYP)	CURRENT SENSE TRANSCONDUCTANCE: $g_{M(MOD)} = dI_{OUT}/dV_{ITH}$ (TYP)
3	9A	-9A	20.0 A/V
2 (default)	9A	-7.5A	18.33 (A/V)
1	7A	-6A	14.44 (A/V)
0	4A	-3.5A	8.33 (A/V)

Inductor Selection

For a given application's input voltage and output voltage, the inductor value and operating frequency determine the ripple current, as defined in Equation 3.

$$\Delta I_L = \frac{V_{OUT}}{f_{SW} \times L}\left(1 - \frac{V_{OUT}}{PV_{IN}}\right) \quad (3)$$

Lower ripple current reduces losses in the inductor and ESR losses in the output capacitors and reduces output voltage ripple. The highest efficiency operation is obtained at low frequency with a small ripple current. However, achieving this requires a large inductor.

A reasonable starting point is to choose a ripple current of about 50% of $I_{OUT(MAX)}$, up to a maximum of about 4A. To guarantee that the ripple current does not exceed a specified maximum, the inductance should be chosen according to the following:

$$L = \frac{V_{OUT}}{f_{SW} \times \Delta I_{L\,MAX}}\left(1 - \frac{V_{OUT}}{PV_{IN}}\right) \quad (4).$$

The inductor ripple current (ΔI_L), and maximum negative load current ($I_{LOADNEGMAX}$) must be chosen such that the most negative inductor valley current limit is above the maximum (least negative) valley current limit indicated in the Electrical Characteristics (See *Table 3*), or an output overvoltage will occur.

$$I_{LOADNEGMAX} - \Delta I_L/2 \geq I_{LIM\_NEG(MAX)} \quad (5)$$

For example, in the current limit range 2 with a negative current limit typical of -7.5A (max -6.5A) and ripple current of 2A, the most negative load that the LT7184S supports is -5.5A. A larger negative current load than that will risk an output overvoltage. When operating with a negative load, the current gets sunk at the output voltage, V_{OUT}, and is pushed out of the PV_{IN} input pin. The supply connected to PV_{IN} must be able to absorb this excess current, or an overvoltage at PV_{IN} will occur.

An inductor must be chosen with a saturation current (typically labeled I_{SAT}) higher than the maximum peak current when operating in the current limit.

$$I_{L\ (PEAK\ MAX)} = I_{LIM\_POS} + \Delta I_L \quad (6)$$

To avoid overheating and poor efficiency, an inductor must be chosen with an RMS current rating that is greater than the maximum expected output load of the application. Preferably, the inductor RMS rating supports the average inductor current in the current limit.

$$I_{L\ (AVG\ MAX)} = I_{LIM\ (POS)} + \frac{\Delta I_L}{2} \quad (7)$$

If the inductor current rating does not support $I_{L(AVG\ MAX)}$ described in Equation 7, either select a suitable current limit or set the VOUT_UV_FAULT_RESPONSE command to disable the channel if the output voltage falls below the VOUT_UV_FAULT_LIMIT. The default setting of VOUT_UV_FAULT_RESPONSE is to continue operation at the valley current limit while the VOUT_UV fault condition is present. For the highest efficiency, the inductor series resistance (DCR or ESR) should be minimized, and its core material should be intended for high-frequency applications.

Input and Output Capacitors

The Low ESR ceramic capacitors should be used at both the output and input supplies of the switching regulators. X5R or X7R ceramic capacitors are recommended for best performance overtemperature and applied voltage. Ensure that the selected capacitor's voltage ratings exceed the maximum application voltages.

Decouple the PV_{IN} pins with low ESL and ESR ceramic capacitors as close as possible to the two PV_{IN} pins with returns to the appropriate ground return pins, as shown in *Table 7* and bulk ceramic capacitors to support the input ripple current.

See the Typical Applications section in this data sheet for suggested output capacitor values. The output capacitor values must be selected to maintain stability over selected operating conditions including operating frequency, compensation (g_{MEA}, and compensation network, R_{ITH}, and C_{ITH}), as well as the programmed current limit, which selects the modulator transconductance.

Programmable PWM Control Loop Compensation

The LT7184S supports internal or external PWM control loop compensation, as shown in *Figure 37* and *Figure 38*. For single-phase applications, internal compensation is selected by tying the channel's I_{TH} pin to $INTV_{CC}$. The PolyPhase operation requires an external compensation, and the I_{TH} pins of all the PolyPhase channels must be connected to an external compensation network.

Control loop compensation can be programmed using the MFR_PWM_MODE_LT7184S command. In either internal or external compensation, the transconductance of the LT7184S PWM error amplifier can be adjusted using MFR_PWM_MODE_LT7184S buts [13:11], as shown in *Table 13*. When internal compensation is selected, the internal PWM loop compensation resistor, R_{ITH}, of the LT7184S can be adjusted in non-linear increments from 5kΩ to 60kΩ (typical) using the MFR_PWM_MODE_LT7184S buts [5:3], as shown in *Table 14*. The internal compensation capacitor,

C_{ITH}, can be adjusted in 10pF increments from 95pF to 165pF (typical) using the MFR_PWM_MODE_LT7184S bits [8:6], as shown in *Table 15*.

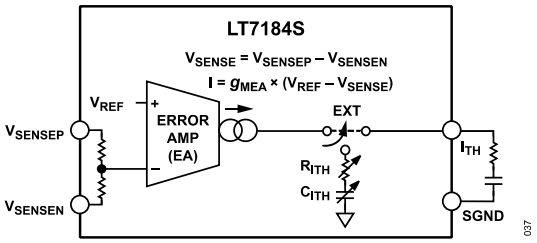

Figure 37. External Compensation

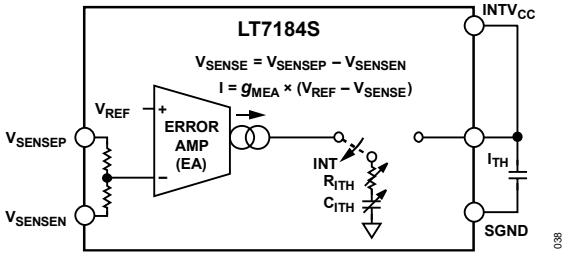

Figure 38. Programmable Internal Compensation

Control Loop Model

An equivalent circuit model for the LT7184S regulator is shown in *Figure 39*. The error amplifier is a transconductance amplifier with finite output impedance and programmable gain (R_{EA} and g_{MEA} as shown in *Table 13*). The error amplifier's input capacitance of about 220fF forms a parasitic pole with the input feedback divider with Thevenin equivalent resistance of about 24kΩ. The power section, consisting of the modulator, power switches current sense, and inductor is modeled as an RC network with a bandwidth of about 13MHz (R_{MOD}, C_{MOD}) followed by a transconductance amplifier, $g_{M(MOD)}$, see *Table 12*. The output capacitor, C_{OUT}, integrates this current, and the capacitance on the I_{TH} node (C_{ITH}, if internal, see *Table 15*) integrates the error amplifier output current, resulting in two dominant poles in the loop. A zero is required and comes from resistor R_{ITH} (if internal, see *Table 14*) in series with C_{ITH}. This simple model works well if the inductor value is not too high and the loop crossover frequency is much lower than the switching frequency, f_{SW}. When modeling PolyPhase applications, the error amplifiers are summed together, and the I_{THN} nodes must be connected to a single external compensation network. When using external compensation networks, care must be taken with the layout of the external I_{TH} network to limit the capacitance to ground C_{PARA}.

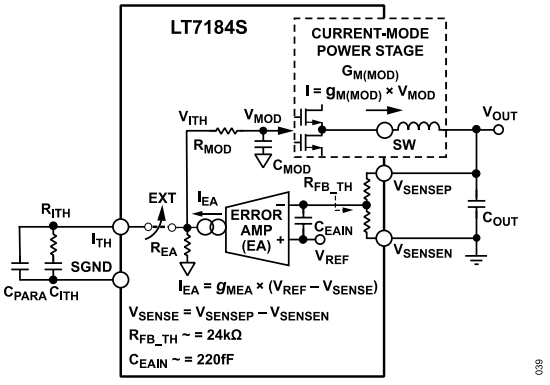

Figure 39.Control Loop Model

Table 13.Programmable Error Amp Transconductance: g_{MEA}/R_{EA}

MFR_PWM_MODE_LT7184S BITS [13:11]	Full V_{OUT} RANGE MODE	HIGH PERFORMANCE LOW-V_{OUT} MODE
7	1240µS/18MΩ	5000µS/4.6MΩ
6	1085µS/21MΩ	4375µS/5.3MΩ
5	930µS/25MΩ	3750µS/6.2MΩ
4	775µS/30MΩ	3125µS/7.4MΩ
3	620µS/37MΩ	2500µS/9.3MΩ
2	465µS/50MΩ	1875µS/12MΩ
1	310µS/75MΩ	1250µS/18MΩ
0	155µS/150MΩ	625µS/37MΩ

Table 14.Programmable Internal Compensation Lead Resistor: R_{ITH}

MFR_PWM_MODE_LT7184S BITS[5:3]	INTERNAL R_{ITH} VALUE
7	60kΩ
6	42kΩ
5	29kΩ
4	20kΩ
3	14kΩ
2	10kΩ
1	7kΩ
0	5kΩ

Table 15.Programmable Internal Compensation Capacitor: C_{ITH}

PFR_PWM_MODE_LT7184S BITS[8:6]	INTERNAL C_{ITH} VALUE
7	165pF
6	155pF
5	145pF
4	135pF
3	125pF
2	115pF
1	105pF
0	95pF

Software-Configurable Sequencing

Time-based sequencing offers a software-configurable means of defining a system's power-up and power-down sequence. To employ time-based sequencing, program TON_DELAY to independently delay each channel so that its soft-start ramp begins at the correct point in the sequence. The sequence starts when all channels are commanded simultaneously using the OPERATION command or RUN pins. Similarly, turn-off sequencing is coordinated using the TOFF_DELAY command.

When using time-based sequencing among multiple ADI devices, it is recommended that the SHARE_CLK pins of the devices be connected to a pull-up resistor to 1.6V to 5.5V.

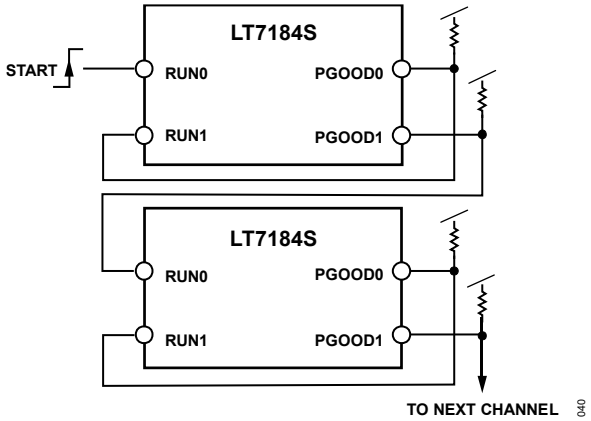

Figure 40. Event Based Sequencing

Event-Based Sequencing

Event-based sequencing offers a hardware-configurable means of defining a system's power-up and power-down sequence.

The PGOODN pin from one regulator may be connected to the RUNN pin of the next regulator in the sequence, as shown in *Figure 40*. The LT7184S holds the PGOODN pin low until the channel's soft-start ramp is complete and its output voltage exceeds the value set in the VOUT_UV_FAULT_LIMIT.

LTPowerPlay GUI

LTPowerPlay is a powerful Windows-based development environment that supports Analog Devices' digital power systems management products, including the LT7184S. LTPowerPlay can be used to evaluate Analog Devices products by connecting to a demo board or the user application board. LTPowerPlay can also be used in an offline mode (with no hardware present) to build multiple configuration files that can be saved and reloaded at a later time. LTPowerPlay provides valuable diagnostic information during system bring-up to program or adjust the power supplies or diagnose power issues. LTPowerPlay utilizes Analog Devices' *DC1613A* USB-to-I^2C/SMBus/PMBus adapter to communicate with one of the many potential targets, including the LT7184S demo board. In application, the 3.3V V_{CCIO} supply from the DC1613A can be connected to the $EXTV_{CC}$ pin of the LT7184S for programming without applying PVIN. The LTPowerPlay software also provides an automatic update feature to keep the revision current with the latest device drivers and documentation. Many context-sensitive help is available within LTPowerPlay, along with several tutorial demos. Refer to *LTpowerPlay* for more information.

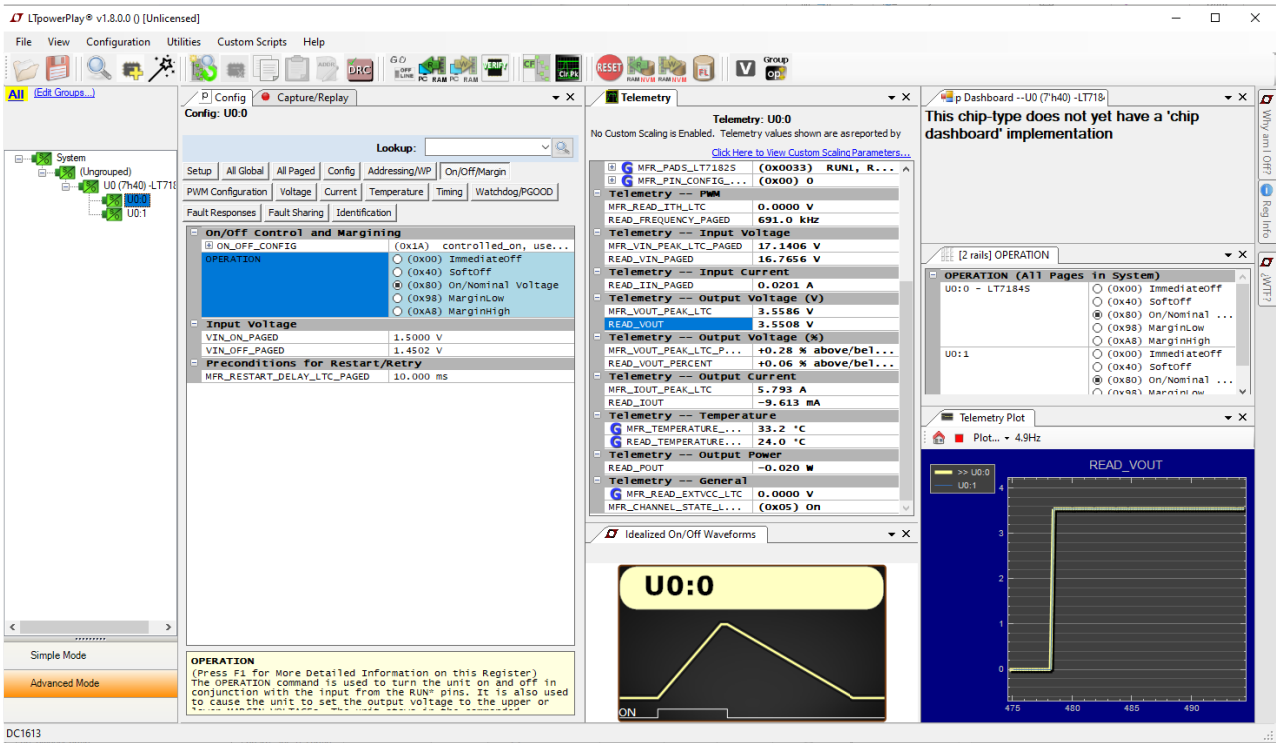

Figure 41. LTPowerPlay GUI

Board Layout Considerations

Note that large, switched currents flow between the LT7184S PV_{IN} and PGND pins and the input capacitors. The loops formed by the input capacitors should be made as small as possible by placing them adjacent to the PV_{IN} and PGND (or SGND) pins.

The input capacitors, inductors, and output capacitors should be placed on the same side of the circuit board. And their connections should be made on the same layer. Place a local, unbroken ground plane under the application circuit on the next layer closest to the surface layer that contains the LT7184S and the PV_{IN} capacitors, the inductor, and the output and boost caps. SGND should be connected to PCB ground at exactly one point adjacent to the SGND pin; SGND and PGND are connected within the LT7184S package.

The SW and BOOST nodes should be made as small as possible, while SW metal should be designed to support the full load current. Add extra spacing from adjacent GND or other signal nodes to SW and BOOST to reduce capacitance.

For more details and PCB design files, refer to the *LT7184S PMBus/I²C Reference Manual*.

Thermal Considerations

Care should be taken in the layout of the PCB to ensure good heat dissipation from the LT7184S package. The ground pins on the bottom of the package should be soldered to a ground plane. The ground pins should be connected to the large copper ground plane below the LT7184S with thermal vias; the ground plane will spread the heat dissipated by the LT7184S. Placing additional vias can reduce thermal resistance further. The maximum load current must be derated as the ambient temperature rises such that the junction temperature approaches the maximum junction temperature rating.

The temperature rise of the LT7184S is worst when operating at a very high load, high PV_{IN}, and high switching frequency. If the case temperature is too high for a given application, then either PV_{IN}, switching frequency, or load current can be decreased to reduce the temperature to an acceptable level.

The internal junction temperature of the LT7184S is reported via the READ_TEMPERATURE_1 command. When the internal READ_TEMPERATURE value passes the programmable OT_WARN_LIMIT, the STATUS_TEMPERATURE_OT Warning bit is set. When the internal READ_TEMPERATURE value passes the programmable OT_FAULT_LIMIT, then the STATUS_TEMPERATURE_OT Fault flag is set. The LT7184S can be programmed to latch off or restart when the overtemperature fault occurs. However, the STAUTS_TEMPERATURE_OT Warning and STATUS_TEMPERATURE_OT Fault flags can only be reset by issuing a CLEAR_FAULTS command or by cycling the OPERATION commands, the RUN pins, or the $EXTV_{CC}$ and PV_{IN0} power supplies.

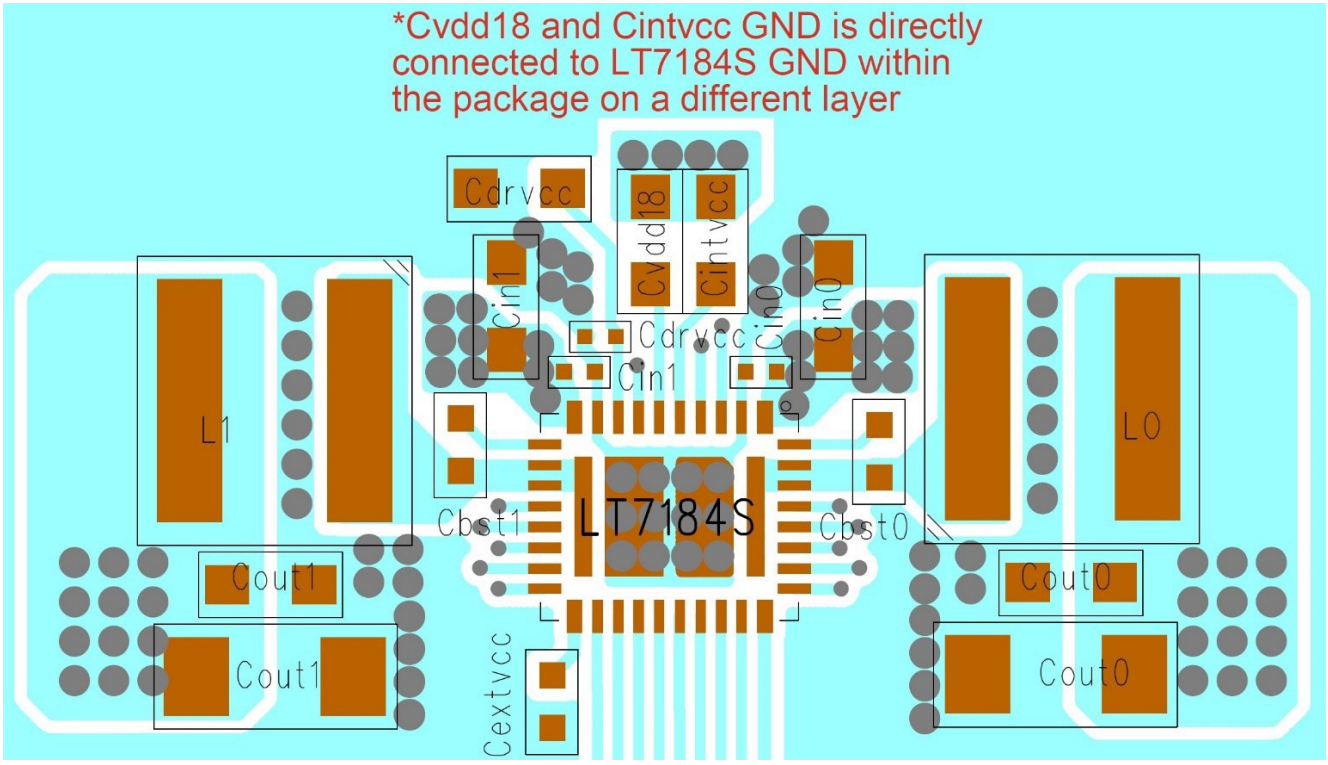

Figure 42. Recommended PCB Layout

TYPICAL APPLICATIONS

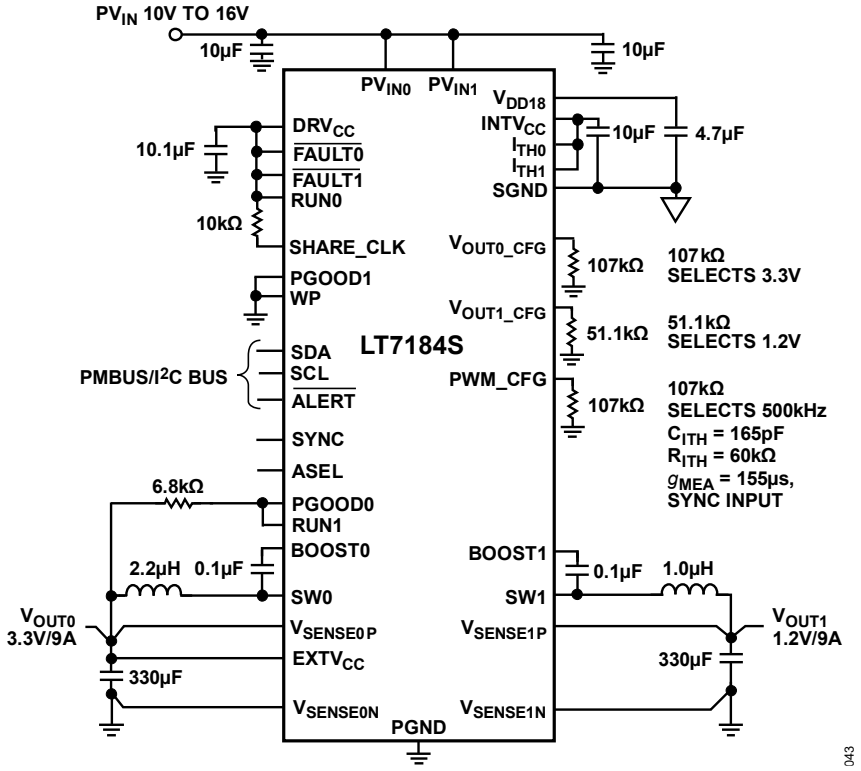

Figure 43. Dual Regulator with Pin-Strap Output Sequencing

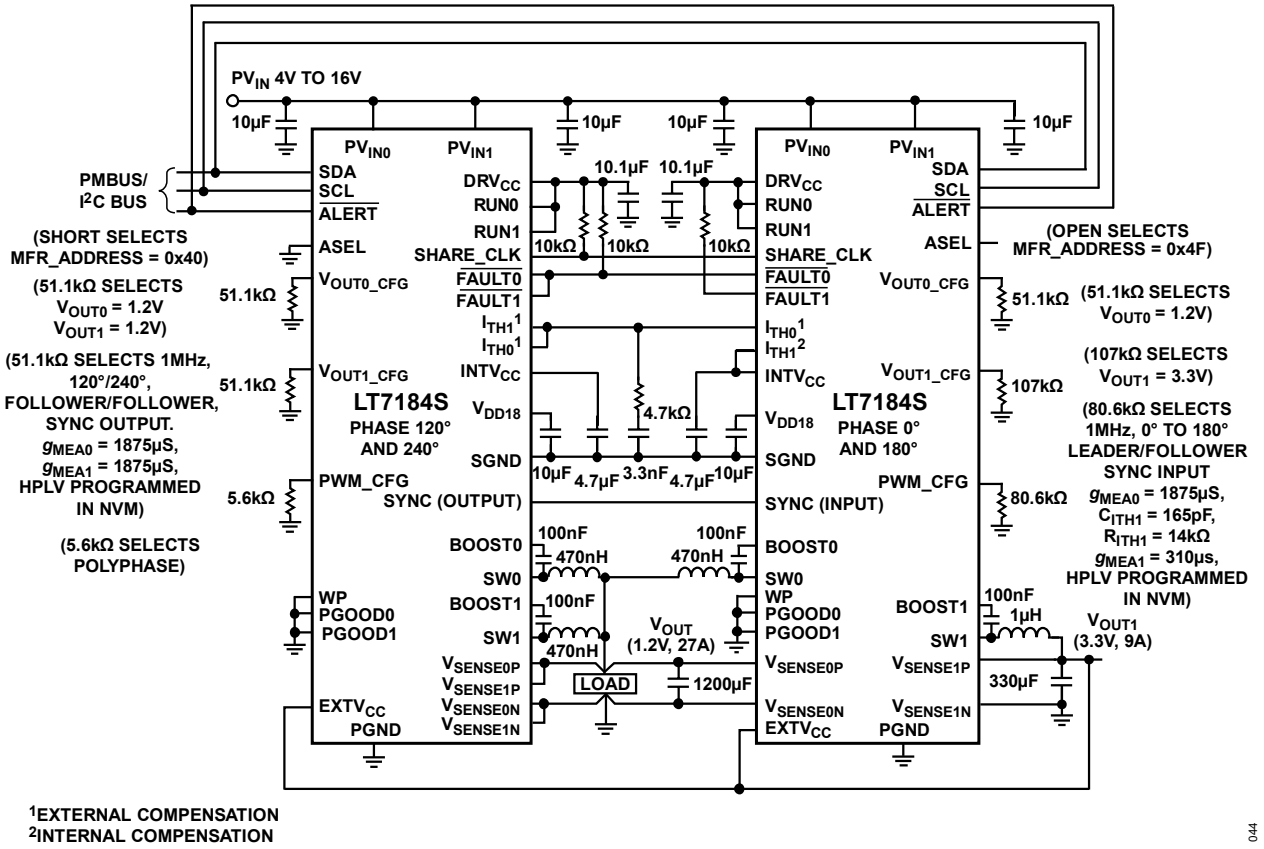

Figure 44. 3-Phase PolyPhase 1.2V/27A 1MHz Regulator and Single-Phase 3.3V/9A 1MHz Regulator

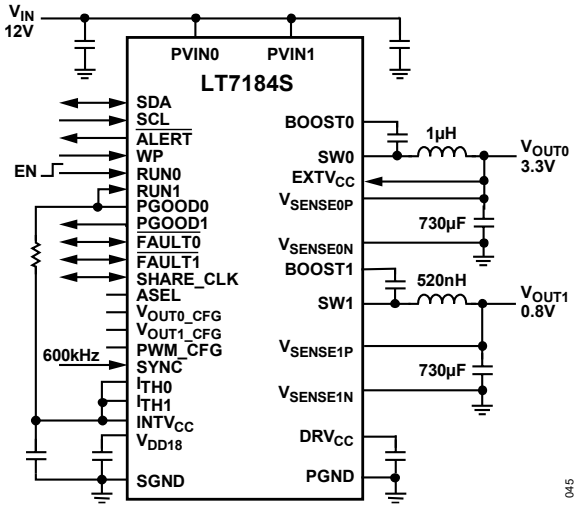

Figure 45.Dual regulator with V_{OUT0} = 3.3V, f_{SW0} = 1200kHz and V_{OUT1} = 0.8V, f_{SW1}= 600kHz

PMbus COMMAND SUMMARY

PMbus/I²C Serial Interface Summary

This data sheet provides an overview of some key features available via the LT7184S serial interface, but it is not exhaustive. Refer to the companion document **LT7184S PMBus/I²C Reference Manual**, which provides a detailed description of the available digital functionality. See *Table 16* for supported PMBus commands. The data format abbreviations are described at the end of this command summary. Floating point values listed in the DEFAULT VALUE column are half-precision IEEE floating point numbers.

Paged commands control and report telemetry for the selected channel. Refer to the *PMBUS Specification Revision 1.3.1* for more information.

Table 16. PMBus Command Summary

COMMAND	CODE	DESCRIPTION	TYPE	PAGED	FORMAT	UNITS	NVM	DEFAULT
PAGE	0x00	Provides integration with multiple PMBus devices.	R/W Byte	N	Register			0x00
OPERATION	0x01	Operating mode control. On/Off, margin high, and margin low.	R/W Byte	Y	Register		Y	0x80
ON_OFF_CONFIG	0x02	RUN pin and PMBus on/off command configuration.	R/W Byte	Y	Register		Y	0x1E
CLEAR_FAULTS	0x03	Clear any fault bits that have been set.	Send Byte	N				
PAGE_PLUS_WRITE	0x05	Write a command directly to a specified page.	W Block	N				
PAGE_PLUS_READ	0x06	Read a command directly from a specified page.	Block R/W	N				
ZONE_CONFIG	0x07	Assigns the current page to the specified zone number for ZONE_WRITE operations.	W Word	Y	Register		Y	0xFEFE
ZONE_ACTIVE	0x08	Selects the active zone for ZONE_WRITE operations.	W Word		Register			0xFEFE
WRITE_PROTECT	0x10	Level of protection provided by the device against accidental changes.	R/W Byte	N	Register		Y	0x00
STORE_USER_ALL	0x15	Store user operating memory to EEPROM.	Send Byte	N				
RESTORE_USER_ALL	0x16	Restore user operating memory from EEPROM.	Send Byte	N				
CAPABILITY	0x19	Summary of PMBus optional communication protocols supported by this device.	R Byte	N	Register			0xD8
QUERY	0x1A	Asks if a given command is supported and what data formats are supported.	Block R/W	N	Register			
SMBALERT_MASK	0x1B	Asks if a given command is supported and what data formats are supported.	Block R/W	N	Register		Y	

COMMAND	CODE	DESCRIPTION	TYPE	PAGED	FORMAT	UNITS	NVM	DEFAULT
VOUT_MODE	0x20	Output voltage format and exponent.	R Byte	N	Register			0x60
VOUT_COMMAND	0x21	Nominal output voltage set point.	R/W Word	Y	IEEE or UL16	V	Y	0.5V (0x3800)
VOUT_MAX	0x24	The upper limit on the commanded output voltage.	R/W Word	Y	IEEE or UL16	V	Y	0.537V (0X384c)
VOUT_MARGIN_HIGH	0X25	Margin high output voltage set point.	R/W Word	Y	IEEE or UL16	V	Y	0.525V (0X3833)
VOUT_MARGIN_LOW	0X26	Margin low output voltage set point.	R/W Word	Y	IEEE or UL16	V	Y	0.475V (0X379A)
VOUT_TRANSITION_RATE	0x27	Rate the output voltage changes when V_{OUT} is commanded to a new value.	R/W Word	Y	IEEE or L11	V/ms	Y	0.25V/ms (0x3400)
FREQUENCY_SWITCH	0x33	Switching frequency of the regulator.	R/W Word	N	IEEE or L11	kHz	Y	1000.0 (0x63D0)
VIN_ON	0x35	Input voltage at which the unit should start power conversion.	R/W Word	Y	IEEE or L11	V	Y	Ch0:1.5V (0x3E00) Ch1:1.4V (0x3D9A)
VIN_OFF	0x36	Input voltage at which the unit should stop power conversion.	R/W Word	y	IEEE or L11	V	Y	Ch0:1.45V (0x3DCD) Ch1:1.35V (0x3D66)
VOUT_OV_FAULT_LIMIT	0x40	Output overvoltage fault limit.	R/W Word	Y	IEEE or UL16	V	Y	0.55V (0x3866)
VOUT_OV_FAULT_RESPONSE	0x41	Action to be taken by the device when an output overvoltage fault is detected.	R/W Byte	Y	Register		Y	0xB8
VOUT_OV_WARN_LIMIT	0x42	Output overvoltage warning limit.	R/W Word	Y	IEEE or UL16	V	Y	0.537V (0x384C)
VOUT_UV_WARN_LIMIT	0x43	Output undervoltage warning limit.	R/W Word	Y	IEEE or UL16	V	Y	0.467V (0x3779)
VOUT_UV_FAULT_LIMIT	0x44	Output undervoltage fault limit	R/W Word	Y	IEEE or UL16	V	Y	0.465V (0x3771)
VOUT_UV_FAULT_RESPONSE	0x45	Action to be taken by the device when an output undervoltage fault is detected.	R/W Byte	Y	Register		Y	0x00
IOUT_OC_FAULT_RESPONSE	0x47	Action to be taken by the device when an output over the current fault is detected.	R/W Byte	Y	Register		Y	0x00
IOUT_OC_WARN_LIMIT	0x4A	Output overcurrent warning limit.	R/W Word	Y	IEEE or L11	A	Y	11.0A (0x4980)

COMMAND	CODE	DESCRIPTION	TYPE	PAGED	FORMAT	UNITS	NVM	DEFAULT
OT_FAULT_LIMIT	0x4F	Internal overtemperature fault limit.	R/W Word	N	IEEE or L11	C	Y	160.0C (0x5900)
OT_FAULT_RESPONSE	0x50	Action to be taken by the device when an internal overtemperature fault is detected.	R/W Byte	N	Register		Y	0xC0
OT_WARN_LIMIT	0x51	Internal overtemperature warning limit.	R/W Word	N	IEEE or L11	C	Y	140.0C (0x5860)
VIN_OV_FAULT_RESPONSE	0x56	Action to be taken by the device when an input overvoltage fault is detected.	R/W Byte	Y	Register		Y	0xB8
VIN_UV_WARN_LIMIT	0x58	Input supply undervoltage warning limit.	R/W Word	Y	IEEE or L11	V	Y	-1.0V (0xBC00)
IIN_OC_WARN_LIMIT	0x5D	Input supply overcurrent warning limit.	R/W Word	Y	IEEE or L11	A	Y	9.0A (0x4880)
TON_DELAY	0x60	Time from RUNN and/or Operation command till an output rail turns on.	R/W Word	Y	IEEE or L11	ms	Y	0.0ms (0x0000)
TON_RISE	0x61	Time from when the output starts to rise until the output voltage set point reaches the V_{OUT} commanded value.	R/W Word	Y	IEEE or L11	ms	Y	1.0ms (0x3C00)
TON_MAX_FAULT_LIMIT	0x62	Maximum time from the start of TON_RISE for V_{OUT} to cross the VOUT_UV_FAULT_LIMIT.	R/W Word	Y	IEEE or L11	ms	Y	5.0ms (0x4500)
TON_MAX_FAULT_RESPONSE	0x63	Action to be taken by the device when a TON_MAX_FAULT event is detected.	R/W Byte	Y	Register		Y	0x00
TOFF_DELAY	0x64	Time from RUNN and/or Operation command to the start of the TOFF_FALL ramp.	R/W Word	Y	IEEE or L11	ms	Y	0.0ms (0x0000)
TOFF_FALL	0x65	Time from when the output starts to fall until the output reaches zero volts.	R/W Word	Y	IEEE or L11	ms	Y	2.0ms (0x4000)
TOFF_MAX_WARN_LIMIT	0x66	Maximum allowed time after TOFF_FALL is completed for the output voltage to fall below the MFR_DISCHARGE _THRESHOLD.	R/W Word	Y	IEEE or L11	ms	Y	0.0ms (0x0000)
STATUS_BYTE	0x78	One-byte summary of the unit's fault condition.	R/W Byte	Y	Register			
STATUS_WORD	0x79	Two-byte summary of the unit's fault condition.	R/W Word	Y	Register			

COMMAND	CODE	DESCRIPTION	TYPE	PAGED	FORMAT	UNITS	NVM	DEFAULT
STATUS_VOUT	0x7A	Output voltage fault and warning status.	R/W Byte	Y	Register			
STATUS_IOUT	0x7B	Output current fault and warning status.	R/W Byte	Y	Register			
STATUS_INPUT	0x7C	Output current fault and warning status.	R/W Byte	Y	Register			
STATUS_TEMPERATURE	0x7D	Internal temperature fault and warning status for READ_TEMPERATURE_1.	R/W Byte	N	Register			
STATUS_CML	0x7E	Communications and memory fault and warning status.	R/W Byte	N	Register			
STATUS_MFR_SPECIFIC	0x80	Manufacturer-specific fault and state information	R/W Byte	Y	Register			
READ_VIN	0x88	Measured Input supply voltage.	R Word	Y	IEEE or L11	V		
READ_IIN	0x89	Calculated input supply current.	R Word	Y	IEEE or L11	A		
READ_VOUT	0x8B	Measured output voltage.	R Word	Y	IEEE or UL16	V		
READ_IOUT	0x8C	Measured output current.	R Word	Y	IEEE or L11	A		
READ_TEMPERATURE_1	0x8D	Measured internal temperature.	R Word	N	IEEE or L11	C		
READ_FREQUENCY	0x95	Measured PWM switching frequency.	R Word	Y	IEEE or L11	kHz		
READ_POUT	0x96	Calculated output power.	R Word	Y	IEEE or L11			
PMBUS_REVISION	0x98	PMBus revision is supported by this device. The current revision is 1.3.	R Byte	N	Register			0x33
MFR_ID	0x99	The manufacturer ID is in ASCII.	R Block	N	ASCII			ADI
MFR_MODEL	0x9A	The part number is in ASCII.	R Block	N	ASCII			LT7184S
MFR_REVISION	0x9B	Part revision number.	R Block	N				
MFR_SERIAL	0x9E	Unique part serial number.	R Block	N				
IC_DEVICE_ID	0xAD	Identification of the IC is in ASCII.	R Block	N	ASCII			LT7184S
IC_DEVICE_REV	0xAE	Revision of the IC.	R Block	N				
MFR_EE_UNLOCK	0xAE	Contact factory.						
MFR_EE_ERASE	0xBE	Contact factory.						
MFR_EE_DATA	0xBF	Contact factory.						

COMMAND	CODE	DESCRIPTION	TYPE	PAGED	FORMAT	UNITS	NVM	DEFAULT
MFR_USER_DATA_00	0xC9	EEPROM word available for user.	R/W Word	N	Register		Y	0x0000
MFR_USER_DATA_01	0xCA	EEPROM word available for user.	R/W Word	N	Register		Y	0x0000
MFR_USER_DATA_02	0xCB	EEPROM word available for user.	R/W Word	N	Register		Y	0x0000
MFR_USER_DATA_03	0xCC	EEPROM word available for user.	R/W Word	N	Register		Y	0x0000
MFR_READ_EXTVCC	0xCD	Measured $EXTV_{CC}$ voltage, when applied.	R Word	N	IEEE or L11	V		
MFR_READ_ITH	0xCE	Measured I_{TH} voltage, when enabled.	R Word	Y	IEEE or L11	V		
MFR_CHAN_CONFIG_LT7184S	0xD0	Configuration bits that are channel-specific.	R/W Word	Y	Register		Y	Ch0: 0x08D6 Ch1: 0x0856
MFR_CONFIG_ALL_LT7184S	0xD1	General configuration bits. Default to select IEEE half-precision floating-point format.	R/W Word	N	Register		Y	0x0100
MFR_FAULT_PROPAGATE_LT7184S	0xD2	Configuration that determines which faults are propagated to the $\overline{FAULTN}$ pins.	R/W Word	Y	Register		Y	0xE0D7
MFR_PWM_MODE_LT718 4S	0xD4	Configuration for the PWM engine.	R/W Word	Y	Register		Y	0x0DD8
MFR_FAULT_RESPONSE	0xD5	Action to be taken by the device when the channel's $\overline{FAULTN}$ pin is externally asserted low.	R/W Byte	Y	Register		Y	0xC0
MFR_IOUT_PEAK	0xD7	Report the maximum measured value of READ_IOUT since the last MFR_CLEAR_PEAKS.	R Word	Y	IEEE or L11	A		
MFR_ADC_CONTROL_ LT7184S	0xD8	Configures the update rate of the measurements taken by the ADC.	R/W Byte	N	Register		Y	0x00
MFR_RETRY_DELAY	0xDB	Retry interval during fault retry mode.	R/W Word	Y	IEEE or L11	ms	Y	10.0ms (0x4900)
MFR_RESTART_DELAY	0xDC	The minimum time the RUNN pin is held low by the LT7184S	R/W Word	Y	IEEE or L11	ms	Y	10.0ms (0x4900)
MFR_VOUT_PEAK	0xDD	The maximum measured value of READ_VOUT since the last MFR_CLEAR_PEAKS command.	R Word	Y	IEEE or UL16	V		

COMMAND	CODE	DESCRIPTION	TYPE	PAGED	FORMAT	UNITS	NVM	DEFAULT
MFR_VIN_PEAK	0xDE	The maximum measured READ_VIN since the last MFR_CLEAR_PEAKS command.	R Word	Y	IEEE or L11	V		
MFR_TEMPERATURE_1_PEAK	0xDF	The maximum measured value of internal temperature since the last MFR_CLEAR_PEAKS command.	R Word	N	IEEE or L11	C		
MFR_CLEAR_PEAKS	0xE3	Clears all peak values.	Send Byte	N				
MFR_DISCHARGE_ THRESHOLD	0xE4	The output voltage used to determine output has decayed sufficiently to re-enable the channel.	R/W Word	Y	IEEE or UL16	V	Y	0.2V (0x3266)
MFR_PADS_LT7184S	0xE5	Digital status of the I/O pads	R Word	N	Register			
MFR_ADDRESS	0xE6	Sets the 7-bit I^2C address byte.	R/W Word	N	Register		Y	0x4F
MFR_SPECIAL_ID	0xE7	ID Code used by the manufacturer.	R Word	N	Register			0x1C1D
MFR_FAULT_LOG_ TIMESTAMP_MSBS	0xE8	Sets the fault log time stamp upper 13 bits, clears lower 32 (read and write first).	R/W 32	N				
MFR_FAULT_LOG_TIMESTAM P_LSBS	0xE9	Sets the fault log time stamp lower by 32 bits.	R/W 32	N				
MFR_FAULT_LOG_STORE	0xEA	Force a fault log entry to be written	Send Byte	N				
MFR_FAULT_LOG_CLEAR	0xEC	Erases all fault log entries, if any.	Send Byte	N				
MFR_FAULT_LOG	0xEE	Read the contents of the fault log, if any.	R Block	N	Register			
MFR_COMMON	0xEF	Manufacturer status bits that are common across multiple Analog Devices' chips.	R Byte	N	Register			
MFR_COMPARE_USER_ALL	0xF0	Compares current command contents with EEPROM	Send Byte	N				
MFR_CHANNEL_STATE	0xF1	Returns the state of the channel.	R Byte	Y	Register			
MFR_PGOOD_DELAY	0xF2	Time output voltage must be between UV and OV before PGOODN transitions high	R/W Word	Y	IEEE or L11	ms	Y	1.0ms (0x3C00)
MFR_NOT_PGOOD_DELAY	0xF3	Time output voltage must be below UV or above OV before PGOODN transitions low.	R/W Word	Y	IEEE or L11	ms	Y	0.1ms (0x2E66)

COMMAND	CODE	DESCRIPTION	TYPE	PAGED	FORMAT	UNITS	NVM	DEFAULT
MFR_PWM_PHASE_LT7184S	0xF5	Set PWM phase.	R/W Word	Y	IEEE or L11	Degrees	Y	Ch0:0 (0x0000) Ch1:180.0 (0x59A0)
MFR_SYNC_CONFIG_LT7184S	0xF6	SYNC pin input/output configuration.	R/W Byte	N	Register		Y	0x00
MFR_PIN_CONFIG_STATUS	0xF7	Pin configuration fault status.	R Byte	N	Register			
MFR_RAIL_ADDRESS	0xFA	Common address for PolyPhase outputs to adjust common parameters.	R/W Byte	Y	Register		Y	0x80
MFR_DISABLE_OUTPUT	0xFB	Disables regulator outputs until reset.	R/W Byte	N	Register			0x00
MFR_EE_USER_WP	0xFC	Disables commands that write user NVM.	R/W Byte	N	Register		Y	0x00
MFR_RESET	0xFD	Command reset without requiring a power down.	Send Byte	N				

Table 17.Supported Data Formats

	PMBus		DEFINITION	EXAMPLES
	TERMINOLOGY	SPECIFICATION REFERENCE		
L11	Linear11	Rev 1.3.1 Part II 7.3	Floating point 16-bit data: Y x $2^{(N)}$, where the exponent N = b[15:11] and the value Y = b[10:0], both the two's compliment binary integers.	b[15:0] = 0x9807 = 7 x 2^{-13} = 8.54 x 10^{-4} b[15:0] = 0xB7D0 = -48 x 2^{-10} = -4.69 x 10^{-3} b[15:0] = 0xE058 = 88 x 2^{-4} = 5.50
UL16	ULinear16	Rev 1.3.1 Part II 8.4.1.1	Fixed point 16-bit data: Y x $2^{(-12)}$, where value Y = b[15:0] is an unsigned integer multiplied by 2 raised to the fixed exponent of -12.	b[15:0] = 0x4C00 = 19456 x 2^{-12} = 4.75 b[15:0] = 0x0600 = 1536 x 2^{-12} = 3.75 x 10^{-1}
Register			Per-bit meaning is defined in the command description in the **LT7184S PMBus/I²C Reference Manual**.	PMBus STATUS_BYTE command.
IEEE	IEEE-754 Half Precision Floating Point	Rev 1.3.1 Part II 8.4.4	IEEE Floating point 16-bit data: $(-1)^{S} \text{x}\ 2^{(N)} \text{x} \left(P + \frac{M}{1024}\right)$ where the sign bit S = b[15]. The bias encoding exponent N and factor P are coded from b[14:10] as: if (b[14:10] = 0), N = -14 P = 0 else, N = decimal(b[14:10]) - 15 P = 1 endif. and M = decimal(b[9:0]).	b[15:0] = 0x4580 $(-1)^{0} \text{x}\ 2^{(17-15)} \text{x} \left(1 + \frac{384}{1024}\right) = 5.50$ b[15:0] = 0x3A66 $(-1)^{0}\ x\ 2^{(16-15)} x \left(1 + \frac{614}{1024}\right) = 0.80$ b[15:0] = 0x8008 $(-1)^{1} \text{x}\ 2^{(-14)} \text{x} \left(0 + \frac{8}{1024}\right) = -4.77 \text{x} 10^{-7}$

OUTLINE DIMENSIONS

PACKAGE DRAWING (OPTION)	PACKAGE TYPE	PACKAGE DESCRIPTION
05-08-7080	LQFN	36-Lead Package

ORDERING GUIDE

Table 18.Ordering Guide

MODEL[1]	TEMPERATURE RANGE	PACKAGE DESCRIPTION	MSL RATING	MARKING CODE
LT7184SRV#PBF	-40°C to 150°C	(4mm x 5mm) 36-Lead LQFN	3	7184S
LT7184SRV#TRPBF	-40°C to 150°C	(4mm x 5mm) 36-Lead LQFN	3	7184S

[1] Z = RoHS Compliant Part