Data Sheet

LT7176P/LT7176P-1

24A, 4V, Single-Phase or Dual-Phase, Silent Switcher Step-Down Regulators with Digital Power System Management

FEATURES

- Silent Switcher® Architecture: Enables a Compact, Efficient, Low EMI Solution
- PMBus/I²C Serial Interface
  - Telemetry Read Back Includes V_{OUT}, I_{OUT}, V_{IN}, Die Temperature, and Faults
  - Programmable Voltage, Current Limit, Sequencing, Soft Start and Stop, Undervoltage and Overvoltage, Phase, Frequency (up to 3MHz), and Loop Compensation
  - Integrated Thrice Programmable NVM
- Key Parameters Selectable by Resistor
- V_{OUT} Set Point Range: 0.3V to 3.4V
- V_{OUT} Accuracy: ±0.25%, 0.6V ≤ V_{OUT} ≤ 1.375V
- PolyPhase Load Sharing up to Four Devices
- Optional Pulse-Skipping Mode Enables Low Quiescent Current
- Differential Remote V_{OUT} Sense
- Fast Transient Response
- Wide V_{IN} Supply Range: Down to 2.7V or 1.5V with $EXTV_{CC}$
- Programmable and Synchronizable: 1MHz to 3MHz
- *30-Lead (3.5mm × 4mm) LQFN*

APPLICATIONS

- Communications, Storage, and Industrial Systems
- Data Center and Solid-State Drives

GENERAL DESCRIPTION

The LT7176P/LT7176P-1 are monolithic PolyPhase DC/DC synchronous step-down regulators that deliver up to 24A of continuous output current. The LT7176P-1 option has two switching phases connected to two inductors to drive a single-regulated output supply. The quick, clean, low-overshoot switching edges deliver high efficiency while minimizing electromagnetic interference (EMI) emissions. The I²C-based PMBus 1.3-compliant serial interface enables control of device functions while providing telemetry information for system monitoring. The LT7176P/LT7176P-1 are supported by the LTpowerPlay® graphical user interface (GUI) tool.

The LT7176P/LT7176P-1 also feature an exposed back for heat sink attachment, which can be used to significantly improve performance.

The controlled on-time valley current-mode control with 25ns typical minimum on-time enables a high switching frequency (f_{SW}) at a low output voltage (V_{OUT}) with excellent transient response in a small overall solution size.

V_{OUT}, f_{SW}, and phase are selectable using external configuration resistors. Settings can also be set using the PMBus interface or stored in the on-chip, thrice programmable nonvolatile memory (NVM).

TYPICAL APPLICATION

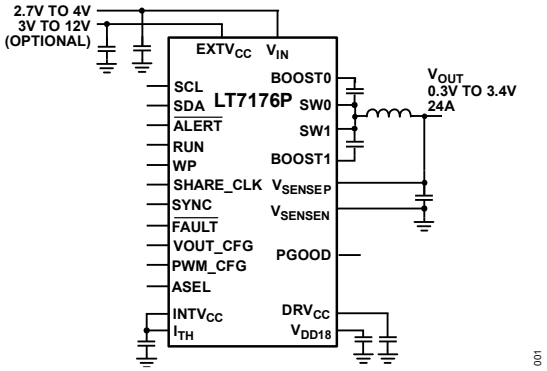


Figure 1. Typical Application for the LT7176P

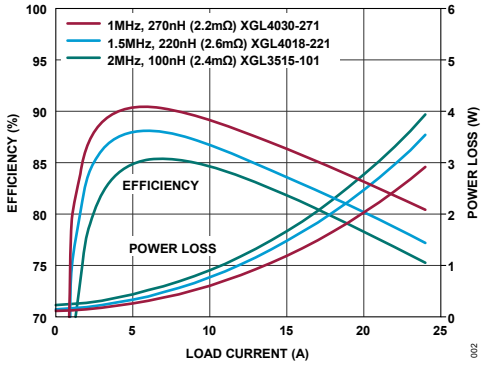


Figure 2. LT7176P-1 3.3V_{IN} to 0.5V_{OUT} Efficiency

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FUNCTIONAL BLOCK DIAGRAMS

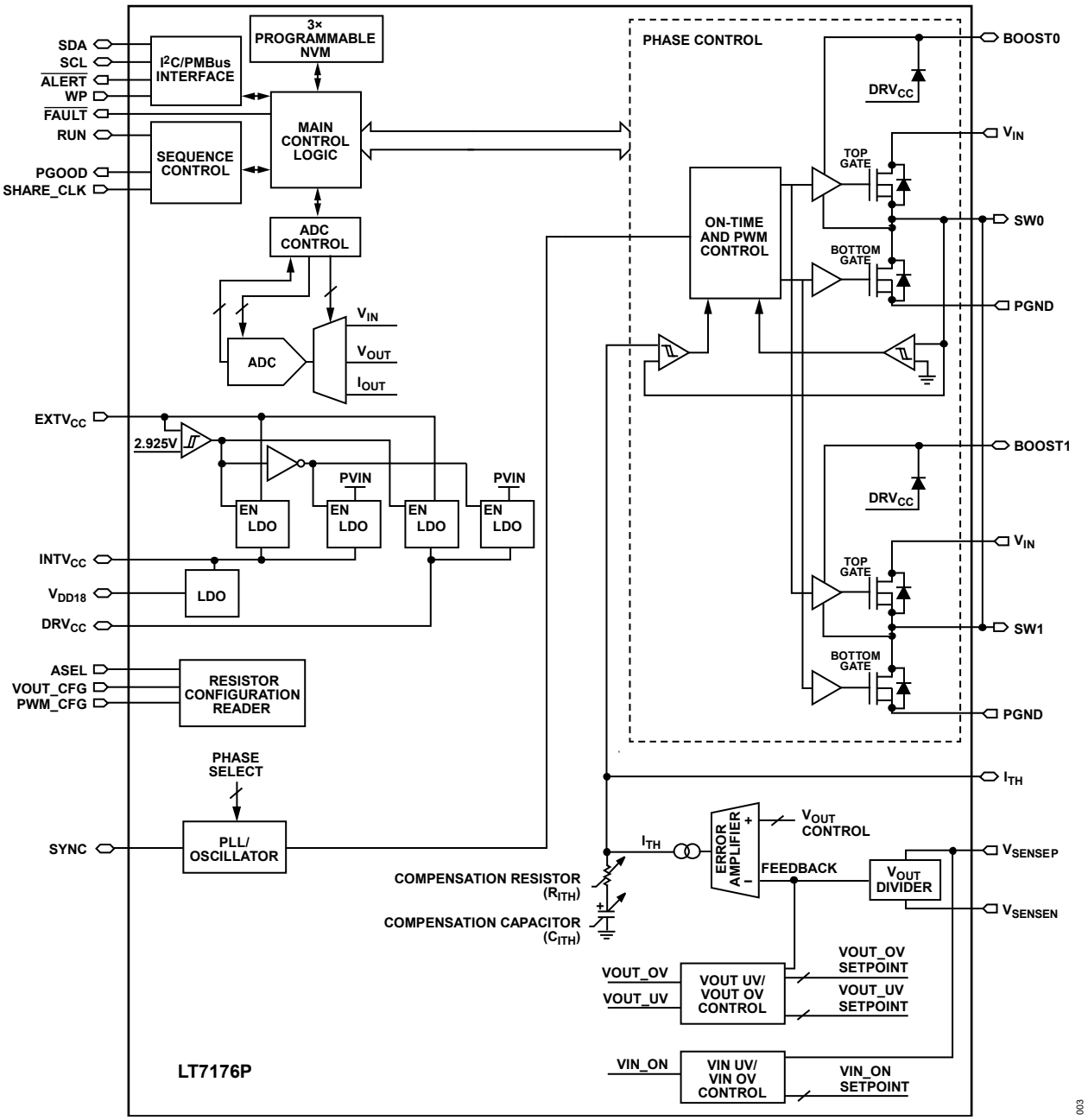


Figure 3. LT7176P Functional Block Diagram

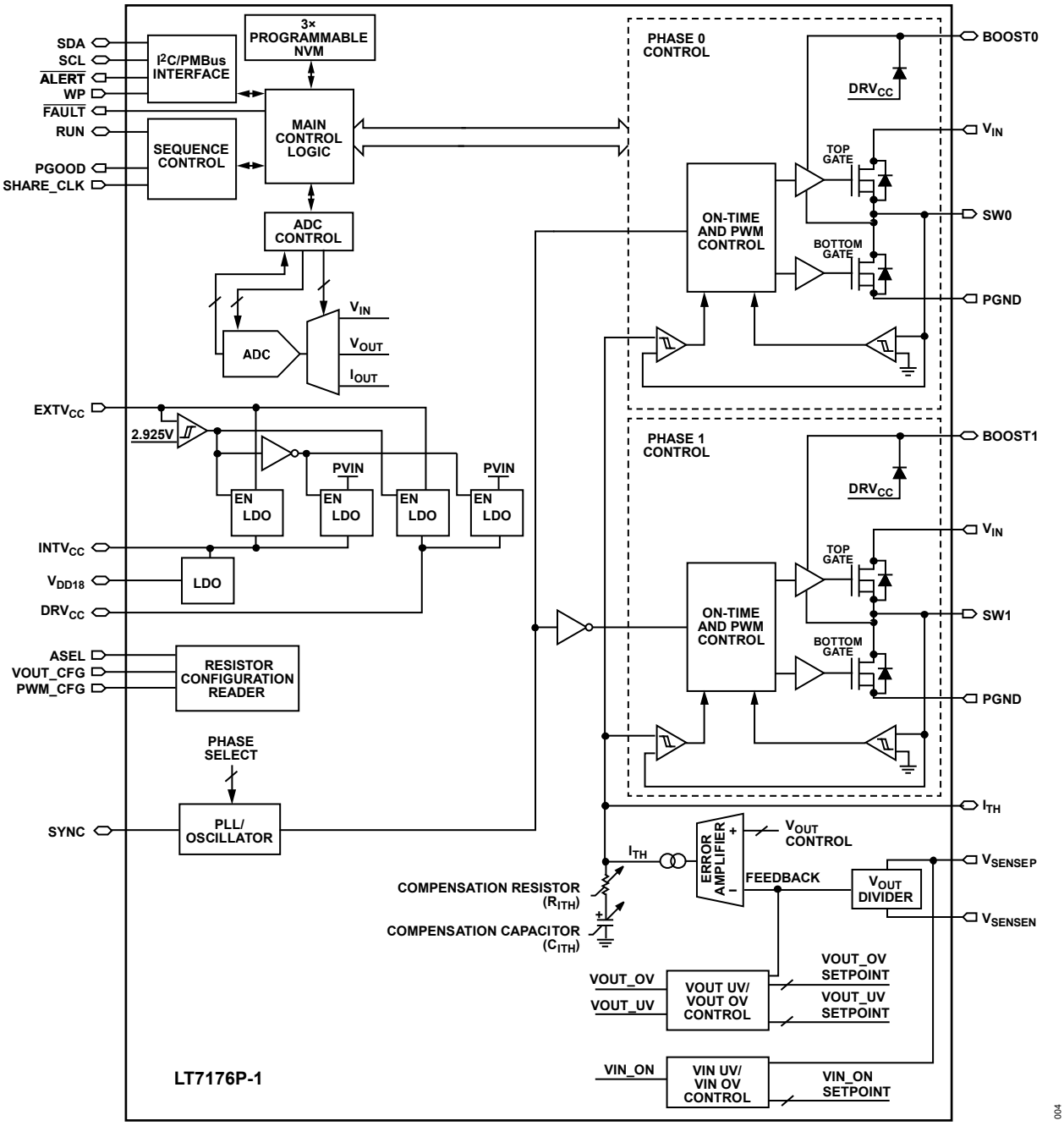


Figure 4. LT7176P-1 Functional Block Diagram

ELECTRICAL CHARACTERISTICS

Table 1. Electrical Characteristics

(T_A = 25°C for typical values. For minimum and maximum values, specifications apply over the full operating temperature range, unless otherwise noted.)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
INPUT SUPPLY					
Input Voltage (V_{IN}) Range	$EXTV_{CC}$ = 0V	2.7		4	V
V_{IN} Range with $EXTV_{CC}$	3.0V ≤ $EXTV_{CC}$ ≤ 12.0V	1.5		4	V
Optional $EXTV_{CC}$ Range		3.0		13.2	V
$EXTV_{CC}$ Rising Threshold		2.85	2.925	3.0	V
$EXTV_{CC}$ Quiescent Current	V_{IN} = 4V, f_{SW} = 1MHz, no load, $EXTV_{CC}$ = 5V, reduced power telemetry mode, forced continuous mode		22		mA
$EXTV_{CC}$ Plus V_{IN} Quiescent Current	V_{IN} = 4V, f_{SW} = 1MHz, no load, reduced power telemetry mode, shutdown		4		mA
Initialization Time Delay from RESTORE_USER_ALL, MFR_RESET, or Application of V_{IN} or $EXTV_{CC}$ Until Power on the TON_DELAY Timer Can Begin	VOUT_CFG and PWM_CFG pins enabled (default)		5		ms
	VOUT_CFG and PWM_CFG pins ignored		3		ms
SWITCHING REGULATOR					
V_{OUT} Accuracy	0.3V ≤ V_{OUT} ≤ 0.6V, Range 0	-0.4		+0.4	%
	0.6V ≤ V_{OUT} ≤ 1.375V, Range 0	-0.25		+0.25	%
	0.8V ≤ V_{OUT} ≤ 2.75V, Range 1	-0.5		+0.5	%
	1.6V ≤ V_{OUT}, Range 2	-0.5		+0.5	%
V_{OUT} Set-Point Range	V_{OUT} Range 0	0.3		1.375	V
	V_{OUT} Range 1	0.8		2.75	V
	V_{OUT} Range 2	1.6		3.4	V
V_{OUT} Set-Point Resolution			1		mV

(T_A = 25°C for typical values. For minimum and maximum values, specifications apply over the full operating temperature range, unless otherwise noted.)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
V_{SENSEP} Input Current	V_{SENSEP} = 3.0V, V_{SENSEN} = 0V, T_A = 25°C			300	µA
Error Amplifier Transconductance (g_{MEA}) Programming Resolution			5		Bits
g_{MEA} (Maximum)	V_{OUT} Range 0		4.8		mS
	V_{OUT} Range 1		2.4		mS
	V_{OUT} Range 2		1.2		mS
g_{MEA} (Minimum)	V_{OUT} Range 0		150		µS
	V_{OUT} Range 1		75		µS
	V_{OUT} Range 2		37.5		µS
g_{MEA} Step Size	V_{OUT} Range 0		150		µS
	V_{OUT} Range 1		75		µS
	V_{OUT} Range 2		37.5		µS
Positive Inductor Valley Current Limit, I_{LIM_POS} (Sourcing Output Current)[1] LT7176P	Current-Limit Selection 0	8	10	12	A
	Current-Limit Selection 1	10.6	14	17.4	A
	Current-Limit Selection 2	16.2	19	21.8	A
	Current-Limit Selection 3	21	24	27	A
Positive Inductor Valley Current Limit, I_{LIM_POS} (Sourcing Output Current)[1] LT7176P-1 Limit per Phase	Current-Limit Selection 0	4	5	6	A
	Current-Limit Selection 1	5.3	7	8.7	A
	Current-Limit Selection 2	8.1	9.5	10.9	A
	Current-Limit Selection 3	10.5	12	13.5	A
Negative Inductor Valley Current Limit, I_{LIM_NEG} (Sinking Output Current)[1] LT7176P	Current-Limit Selection 0	-8.8	-6.8	-4.8	A
	Current-Limit Selection 1	-10	-8.2	-6.4	A
	Current-Limit Selection 2	-13.8	-11.4	-9	A
	Current-Limit Selection 3	-16.4	-13.4	-10.4	A
Negative Inductor Valley Current Limit, I_{LIM_NEG} (Sinking Output Current)[1] LT7176P-1 Limit per Phase	Current-Limit Selection 0	-4.4	-3.4	-2.4	A
	Current-Limit Selection 1	-5	-4.1	-3.2	A
	Current-Limit Selection 2	-6.9	-5.7	-4.5	A
	Current-Limit Selection 3	-8.2	-6.7	-5.2	A
	Top, V_{IN} = 3.3V, $EXTV_{CC}$ = 0V		4.5		mΩ

(T_A = 25°C for typical values. For minimum and maximum values, specifications apply over the full operating temperature range, unless otherwise noted.)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
LT7176P Switch On Resistance	Bottom, V_{IN} = 3.3V, $EXTV_{CC}$ = 0V		1.3		mΩ
LT7176P-1 Switch On Resistance, Each Phase	Top, V_{IN} = 3.3V, $EXTV_{CC}$ = 0V		9		mΩ
	Bottom, V_{IN} = 3.3V, $EXTV_{CC}$ = 0V		2.6		mΩ
SWx Leakage	V_{IN} = 4V, SWx voltage = 0V and 4V, T_A = 25°C	-10		+10	µA
Minimum OnTime (t_{ON})	Load current (I_{OUT}) = 2.5A		25	40	ns
Minimum Off Time (t_{OFF})	Load current (I_{OUT}) = 2.5A		110	160	ns
OUTPUT VOLTAGE $\overline{\text{FAULT}}$ AND WARNING SUPERVISORS					
V_{OUT} Undervoltage (UV) Threshold Programming Range (VOUT_UV_FAULT_LIMIT and VOUT_UV_WARN_LIMIT)	T_A = 25°C	0.275		5.0	V
V_{OUT} Overvoltage (OV) Threshold Programming Range (VOUT_OV_FAULT_LIMIT and VOUT_OV_WARN_LIMIT)	T_A = 25°C	0.3		5.0	V
V_{OUT} UV and OV Fault and Warning Threshold Accuracy	<0.6V	-12		+12	mV
	≥0.6V	-2		+2	%
V_{OUT} UV and OV Threshold Programming Step Size			4		mV
V_{OUT} UV and OV Response Time	V_{OUT} = 10mV beyond threshold			25	µs
INPUT VOLTAGE $\overline{\text{FAULT}}$ AND WARNING SUPERVISORS					
VIN_ON Programming Range	T_A = 25°C	1.4		5.5	V
VIN_OFF Programming Range	T_A = 25°C	1.35		5.5	V
VIN_ON, VIN_OFF Programming Step Size			12.5		mV

(T_A = 25°C for typical values. For minimum and maximum values, specifications apply over the full operating temperature range, unless otherwise noted.)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
VIN_ON, VIN_OFF Set-Point Accuracy	VIN_ON/VIN_OFF ≤ 5.5V	-100		+100	mV
V_{IN} Overvoltage Lockout Threshold	V_{IN} rising	5.83	5.95		V
	V_{IN} falling	5.70	5.84		V
OSCILLATOR AND PHASE-LOCKED LOOP (PLL)					
SYNC Pin Input Frequency Range		1		3	MHz
f_{SW} Programming Range	T_A = 25°C	1		3	MHz
f_{SW} Set-Point Accuracy		-7.5		+7.5	%
Switching Phase Programming Range	T_A = 25°C	0		345	Degrees
Switching Phase Programming Resolution			15		Degrees
TELEMETRY READBACK					
Telemetry Measurement Period All Measurements	Standard telemetry mode		5.5		ms
Telemetry Measurement Period All Measurements	Low frequency telemetry		110		ms
Telemetry Measurement Period All Except Output Current	I_{OUT} scope telemetry mode		9		ms
Telemetry Measurement Period Output Current Only	I_{OUT} scope telemetry mode		2.5		ms
OUTPUT VOLTAGE READBACK					
READ_VOUT Accuracy	0.3V ≤ V_{OUT} ≤ 0.6V, V_{OUT} Range 0	-0.3		+0.3	%
	0.6V ≤ V_{OUT} ≤ 1.375V, V_{OUT} Range 0	-0.2		+0.2	%
	0.8V ≤ V_{OUT} ≤ 2.75V, V_{OUT} Range 1	-0.4		+0.4	%
	1.6V ≤ V_{OUT}, V_{OUT} Range 2	-0.4		+0.4	%
V_{IN} INPUT VOLTAGE READBACK					
READ_VIN Accuracy	1.5V < V_{IN} < 2.5V	-25		+25	mV
	2.5V < V_{IN} < 5.5V	-1		+1	%
OUTPUT CURRENT READBACK DC ACCURACY					

(T_A = 25°C for typical values. For minimum and maximum values, specifications apply over the full operating temperature range, unless otherwise noted.)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
READ_IOUT DC Accuracy[4]	$V_{OUT}/V_{IN} \le 0.25$, $0A \le I_{OUT} \le 10A$, $-25°C \le T_J \le 100°C$	-0.55		+0.55	A
	$V_{OUT}/V_{IN} \le 0.25$, $I_{OUT} > 10A$, $-25°C \le T_J \le 100°C$	-5.5		+5.5	%
	$V_{OUT}/V_{IN} \le 0.25$, $0A \le I_{OUT} \le 10A$, $-50°C \le T_J \le 125°C$	-0.75		+0.6	A
	$V_{OUT}/V_{IN} \le 0.25$, $I_{OUT} > 10_A$, $-50°C \le T_J \le 125°C$	-7.5		+6	%
	$V_{OUT}/V_{IN} \le 0.6$, $0A \le I_{OUT} \le 10A$, $-50°C \le T_J \le 125°C$	-1.1		+0.9	A
	$V_{OUT}/V_{IN} \le 0.6$, $I_{OUT} > 10A$, $-50°C \le T_J \le 125°C$	-11		+9	%
FREQUENCY READBACK					
READ_FREQUENCY Accuracy	T_A = 25°C	-5		+5	%
NVM CHARACTERISTICS					
Retention[2]		10			Years
Endurance[2, 3]		3			Writes
STORE_USER_ALL Mass Write Time			0.25	2	Sec
SYNC PIN					
Peak-to-Peak Input Voltage Swing	SYNC input mode	1.4		5.5	V
Rise Time	SYNC input mode			25	ns
Duty Cycle	SYNC input mode	30		70	%
Output High Voltage, V_{OH}	SYNC output mode, current = 1mA	1.6			V
Output Low Voltage, V_{OL}	SYNC output mode, current = 1mA			0.2	V
RUN, $\overline{\text{FAULT}}$, PGOOD, SCL, SDA, SHARE_CLK, WP, and $\overline{\text{ALERT}}$ INPUTS					
Input High Threshold			1.1	1.35	V
Input Low Threshold		0.8	0.9		V
Hysteresis		50	200	400	mV

(T_A = 25°C for typical values. For minimum and maximum values, specifications apply over the full operating temperature range, unless otherwise noted.)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
RUN, PGOOD, SCL, SDA, $\overline{\text{ALERT}}$, and WP Leakage Current	Applied voltage = 0V and 5.5V, T_A = 25°C	-10		+10	µA
$\overline{\text{FAULT}}$ and SHARE_CLK Leakage Current	Applied voltage = 0V and 5.5V, T_A = 25°C	-16		-8	µA
Input Capacitance, C_{IN}[2]	T_A = 25°C			10	pF
$\overline{\text{FAULT}}$, PGOOD, SHARE_CLK, and $\overline{\text{ALERT}}$ OPEN-DRAIN OUTPUTS					
Output Low Voltage, V_{OL}	Current = 6mA			0.4	V
SCL AND SDA OUTPUTS					
Output Low Voltage, V_{OL}	Current = 20mA			0.4	V

1 The LT7176P/LT7176P-1 switching regulators use valley current mode control so that the current limits specified correspond to the valley of the inductor current waveform. The maximum load current is higher and equals the valley current limit plus one half of the inductor ripple current.

2 Guaranteed by design, characterization, and correlation with statistical process controls.

3 The minimum retention specification for NVM applies for devices where NVM is programmed while the T_J of the devices is between -40°C and +125°C and while $EXTV_{CC}$ is biased at 9.6V to 13.2V.

4 Guaranteed in FCM. Read_IOUT is based on current passing through power MOSFETs. Because both power MOSFETs can be off in pulse-skipping mode, higher READ_IOUT error is expected under light load conditions.

Table 2. I²C/PMBus Timing

PARAMETER	SYMBOL	MIN	MAX	UNITS
Serial bus operating frequency	f_{SCL}	10	1000	kHz
Bus free time between stop and start	t_{BUF}	500		ns
Hold time after repeated start condition	$t_{HD:STA}$	260		ns
Repeated start condition setup time	$t_{SU:STA}$	260		ns
Stop condition setup time	$t_{SU:STO}$	260		ns
Data input setup time	$t_{SU:DAT}$	50		ns
Data input hold time	$t_{HD:DAT}$	0		ns
Data output hold time		0	450	ns
Bus timeout	$t_{TIMEOUT}$	25	35	ms
Serial clock low period	t_{LOW}	0.5	10000	µs
Serial clock high period	t_{HIGH}	260		ns

ABSOLUTE MAXIMUM RATINGS

T_A = 25°C, unless otherwise specified.

Table 3. Absolute Maximum Ratings

PARAMETER	RATING
V_{IN}	-0.3V to +6.0V
Average V_{IN} Input Supply Current[1]	3A
$EXTV_{CC}$	-0.3V to +16V
V_{SENSEP}	-0.3V to +6.0V
V_{SENSEN}	-0.3V to +0.3V
RUN, PGOOD, $\overline{ALERT}$, SDA, SCL, SYNC, PWM_CFG, $\overline{FAULT}$, ASEL, WP, SHARE_CLK, I_{TH}, and VOUT_CFG	-0.3V to +6V
Operating T_J[2]	-40°C to +150°C
Storage Temperature	-65°C to +150°C
Maximum Peak Reflow (Package Body) Temperature	260°C

1 The average V_{IN} input current to the LT7176P/LT7176P-1 is a function of V_{IN}, the programmed V_{OUT}, I_{OUT}, and the efficiency as $I_{VIN} = \frac{V_{OUT} \times I_{OUT}}{V_{IN} \times EFFICIENCY}$. Exceeding the maximum average input current rating for the LT7176P/LT7176P-1 may affect device reliability and lifetime.

2 The LT7176P/LT7176P-1 are specified over the -40°C to 150°C operating T_J range. Operating lifetime is derated for T_J greater than 110°C. The LT7176P/ LT7176P-1 include overtemperature protection intended to protect the device during momentary overload conditions. The maximum rated T_J is exceeded when this protection is active. Note the maximum T_A consistent with these specifications is determined by specific operating conditions in conjunction with the board layout, rated package thermal impedance, and other environmental factors.

Stresses beyond those listed under absolute maximum ratings may cause permanent damage to the device. These are stress ratings only. Functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

Thermal Resistance

Thermal performance is directly linked to printed circuit board (PCB) design and operating environment. Careful attention to PCB thermal design is required.

Using enhanced heat removal (PCB, heat sink, and airflow) techniques improve thermal resistance values.

θ_{JA} is the natural convection junction-to-ambient thermal resistance measured in a one cubic foot sealed enclosure, $\theta_{JC\text{-}TOP}$ is the junction-to-case top thermal resistance, and $\theta_{JC\text{-}BOTTOM}$ is the junction-to-case bottom thermal resistance.

Table 4. Thermal Resistance for Demonstration Board in Still Air

θ_{JA}	$\theta_{JC\text{-}TOP}$	$\theta_{JC\text{-}BOTTOM}$	UNIT
17.7	0.9	3.3	°C/W

ESD Caution



ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS

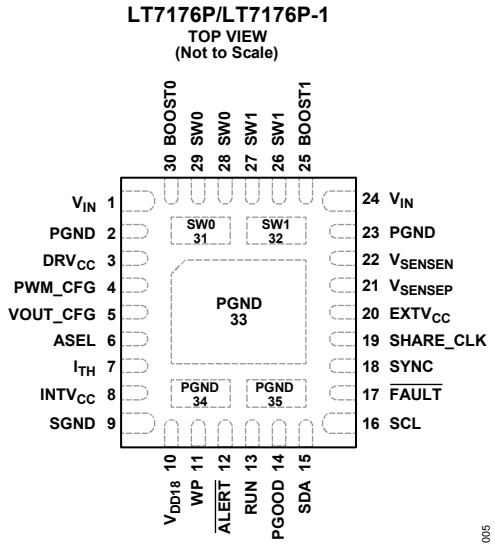


Figure 5. Pin Configuration

Pin Descriptions

Table 5. Pin Descriptions

PIN	NAME	DESCRIPTION
1, 24	V_{IN}	Power Supply Inputs for the Buck Regulators and Internal LDO Regulators. Two 0201 or 01005 capacitors must be placed between V_{IN} (pin 1) and PGND (pin 2), and between V_{IN} (pin 24) and PGND (pin 23). These capacitors must each have a 0.1µF value or greater capacitance and must be placed as close as possible to the LT7176P/LT7176P-1. Place a third larger capacitor of 10µF or more, close to LT7176P/LT7176P-1 with its positive terminal connected to either pin 1 or pin 24, and its negative terminal connected to ground.
2, 23, 33, 34, 35	PGND	Power Ground Pins. The negative terminals of the V_{IN} input bypass capacitors and regulator output capacitors must be tied to the PGND pins with low impedance connections. The printed circuit board (PCB) must be designed to provide low impedance electrical and thermal contact to power ground.
3	DRV_{CC}	Internal Low Dropout (LDO) Regulator Bypass Pin. This regulator provides the supply current for the power field-effect transistor (FET) drivers. Decouple the DRV_{CC} pin to PGND with 10µF or greater close to LT7176P/LT7176P-1, using the top printed circuit board (PCB) layer. Do not load the DRV_{CC} pin with external circuitry.
4	PWM_CFG	Pulse-Width Modulation (PWM) Configuration Resistor Pin (PWM_CFG). Connect a 1% resistor from PWM_CFG to either PGND or SGND according to *Table 9* and *Table 10* to select the frequency, phase, and mode configurations. The configuration resistor is read at LT7176P/LT7176P-1 start-up and reset. PWM_CFG may be floated. See the *Applications Information* section for more details.

PIN	NAME	DESCRIPTION
5	VOUT_CFG	Output Voltage Configuration Input Pin. Connect a 1% resistor from VOUT_CFG to either SGND or PGND according to *Table 8* to select the output voltage set point. If left floating or tied to V_{DD18}, the LT7176P/LT7176P-1 use the value for the VOUT_COMMAND command programmed in the NVM. The VOUT_CFG pin is read at LT7176P/LT7176P-1 start-up and reset.
6	ASEL	Serial Bus Address Configuration. Connect a 1% resistor from ASEL to ground (SGND or PGND) to select one of sixteen serial bus interface addresses according to *Table 7*. Refer to the description of MFR_ADDRESS in the *LT7176/LT7176-1 PMBus/I²C Reference Manual*. The ASEL pin is read at LT7176P/LT7176P-1 start-up and reset. If the ASEL pin is left floating, the factory default 7-bit device address is 0x4F. If the ASEL pin is grounded, the factory default device address is 0x40.
7	I_{TH}	Error Amplifier Output and Switching Regulator Compensation Point. Connect the appropriate external components between this pin and SGND to compensate the regulator loop frequency response, or connect the I_{TH} pin to $INTV_{CC}$ to select internal compensation.
8	$INTV_{CC}$	Internal 3V LDO Regulator Bypass Pin. This regulator provides the supply current for internal circuitry. Decouple the $INTV_{CC}$ pin to SGND with a 10µF or greater, low ESR ceramic capacitor, as close as possible to the LT7176P/LT7176P-1. Do not load the $INTV_{CC}$ pin with external circuitry.
9	SGND	Signal Ground Pin. The bypass capacitors for $INTV_{CC}$ and V_{DD18} must be connected to SGND. The SGND pin is connected to PGND inside the LT7176P/LT7176P-1. Do not connect SGND to PGND on the PCB.
10	V_{DD18}	Internal 1.8V Regulator Bypass Pin. Decouple the V_{DD18} pin to SGND with a 1µF or greater, low ESR ceramic capacitor. Do not load the V_{DD18} pin with external circuitry.
11	WP	Write Protect Input. When this pin is high, only the PAGE, OPERATION, MFR_NVM_UNLOCK, and CLEAR_FAULTS commands are writable. Clear individual fault bits by writing a 1 to the respective bits in the STATUS commands.
12	$\overline{ALERT}$	Open-Drain Output Pin. If the $\overline{ALERT}$ pin function is used, a pull-up resistor to a supply of up to 5.5V is required. The supply should be higher than 1.6V to ensure proper PMBus functionality and compliance. If the $\overline{ALERT}$ pin function is not used, the $\overline{ALERT}$ pin can be tied to ground.
13	RUN	Regulator Enable Input Pin. Logic high enables the regulators. The RUN pin can be tied directly to DRV_{CC} to enable the regulator when input power is present.
14	PGOOD	Power-Good Indicator Open-Drain Output. PGOOD is pulled low when the output is outside of the overvoltage and undervoltage fault thresholds, when the regulator is disabled, or during on and/or off sequencing. The PGOOD output is deglitched by internal configurable timers. If the PGOOD pin function is used, a pull-up resistor to a supply of up to 5.5V is required. The supply should be higher than 1.6V to ensure proper PMBus functionality and

PIN	NAME	DESCRIPTION
		compliance. If the PGOOD pin function is not required, PGOOD can be tied to ground.
15	SDA	Serial Bus Data Input and Output Pin. A pull-up resistor from a 1.6V to 5.5V supply is required for I²C/PMBus operation. If serial bus operation is not required, SDA can be tied to ground.
16	SCL	Serial Bus Clock Input Pin. The LT7176P/LT7176P-1 can hold SCL low if clock stretching is enabled (PMBus speeds, 400kHz to 1MHz only). A pull-up resistor from a 1.6V to 5.5V supply is required for I²C/PMBus operation. If serial bus operation is not required, SCL can be tied to ground.
17	$\overline{\text{FAULT}}$	$\overline{\text{FAULT}}$ Input/Open-Drain Output. The LT7176P/LT7176P-1 pull the pin down with 1.5mA (typical) when an unmasked fault occurs on the regulator. If another device pulls down on the $\overline{\text{FAULT}}$ pin, the LT7176P/LT7176P-1 regulator turns off immediately. If PolyPhase configuration is used, tie together the $\overline{\text{FAULT}}$ pins of all PolyPhase devices. If PolyPhase configuration is used, or if $\overline{\text{FAULT}}$ pin reporting or sharing is required, a pull-up resistor of 6.8k or greater to 1.6V to 5.5V is required. If the $\overline{\text{FAULT}}$ pin function is not required, the pin may be left floating.
18	SYNC	External Clock Synchronization Input (SYNC)/Output Pin. When configured as an input and driven by an external clock, an internal PLL synchronizes the regulator switching frequency to the rising edge of the external clock. When configured as an output, the LT7176P/LT7176P-1 drive the SYNC pin at the switching frequency set by the FREQUENCY_SWITCH command. If neither function is required, the SYNC pin may be left floating; do not connect it to ground. See the *Applications Information* section for more details.
19	SHARE_CLK	Bidirectional Open-Drain Sequence Time Base Share Clock Pin. Nominally 100kHz. Used to align the start-up and shutdown of regulator outputs among multiple ADI products when PolyPhase or time-based sequencing is employed. A pull-up resistor from 1.6V to 5.5V is required if the SHARE_CLK function is used. If SHARE_CLK is not connected to other devices, SHARE_CLK may be left floating.
20	$EXTV_{CC}$	Optional Power Supply Input. If connected to a supply higher than 3V, the $EXTV_{CC}$ pin is used to derive the $INTV_{CC}$ and DRV_{CC} supplies. If the LT7176P/LT7176P-1 output is 3V or greater, the output can be connected to $EXTV_{CC}$ to reduce power loss. If the $EXTV_{CC}$ pin is tied to a supply other than V_{OUT}, connect a 0.1µF or greater local bypass ceramic capacitor from this pin to PGND.
21	V_{SENSEP}	Output Voltage Positive Sense Input. Kelvin connect the V_{SENSEP} pin to the output voltage sense point.
22	V_{SENSEN}	Output Voltage Negative Sense Input. Kelvin connect the V_{SENSEN} pin to the output voltage ground sense point.
25	BOOST1	Boosted Floating Driver Supply Pin. Connect a 0.1µF boost capacitor from BOOST1 to SW1 as close as possible to the LT7176P/ LT7176P-1, using the top

PIN	NAME	DESCRIPTION
		PCB layer. The normal operating voltage swing of the BOOST1 pin is from DRV_{CC} to V_{IN} + DRV_{CC}.
26, 27, 32	SW1	Output of the Phase 1 Internal Power Switches. For the LT7176P-1, tie the SW1 pins together and connect these pins to the Phase 1 inductor and BOOST1 capacitor. For the LT7176P, tie the SW0 and SW1 pins together and connect these pins to the Phase 0 inductor and BOOST0 capacitor. For optimal performance, keep the SW1 node small on the PCB.
28, 29, 31	SW0	Output of the Phase 0 Internal Power Switches. Tie the SW0 pins together and connect these pins to the Phase 0 inductor and BOOST0 capacitor. For optimal performance, keep the SW0 node small on the PCB.
30	BOOST0	Boosted Floating Driver Supply Pin. Connect a 0.1µF boost capacitor from BOOST0 to SW0 as close as possible to the LT7176P/LT7176P-1, using the top PCB layer. The normal operating voltage swing of the BOOST0 pin is from DRV_{CC} to V_{IN} + DRV_{CC}.

TYPICAL PERFORMANCE CHARACTERISTICS

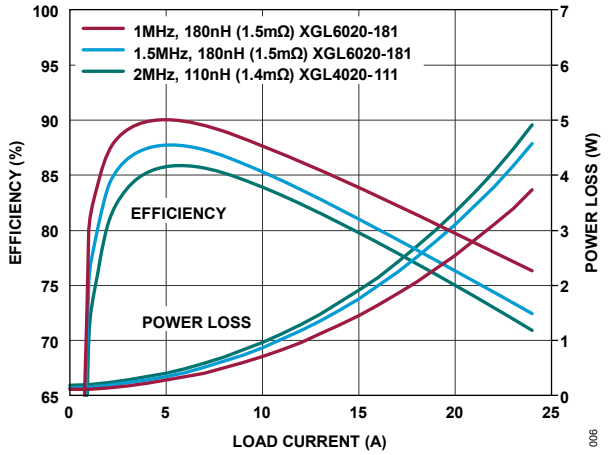


Figure 6. LT7176P 3.3V_{IN} to 0.5V_{OUT} Efficiency

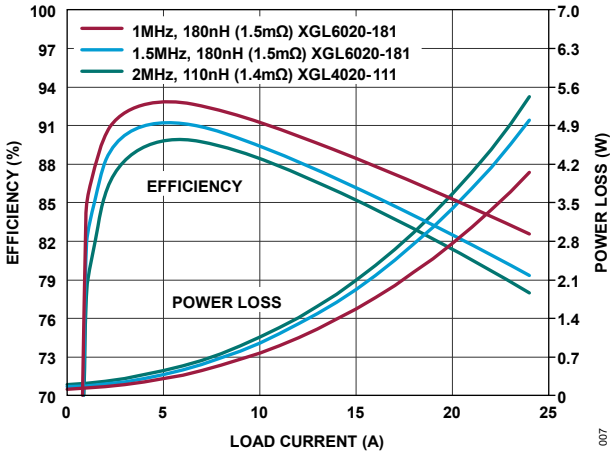


Figure 7. LT7176P 3.3V_{IN} to 0.8V_{OUT} Efficiency

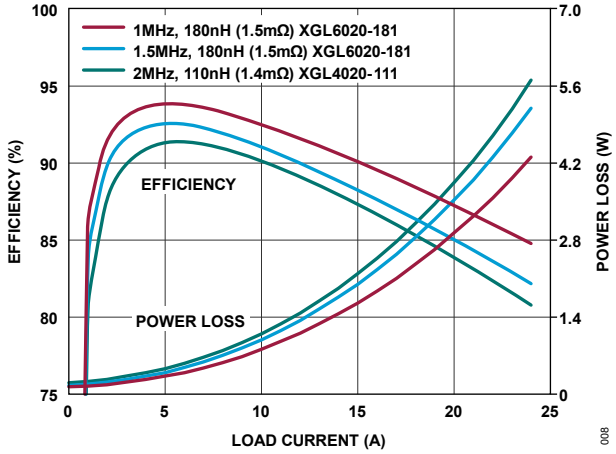


Figure 8. LT7176P 3.3V_{IN} to 1.0V_{OUT} Efficiency

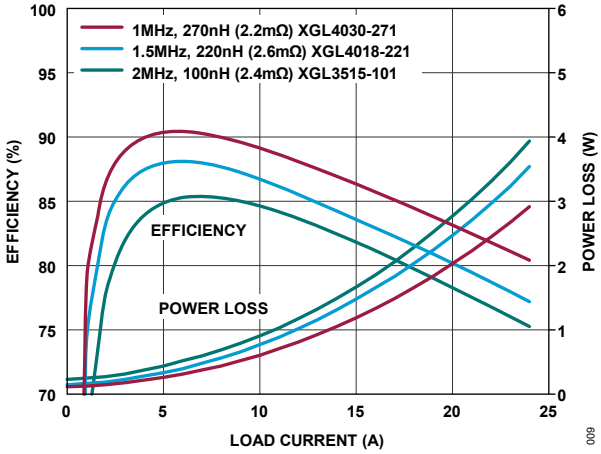


Figure 9. LT7176P-1 3.3V_{IN} to 0.5V_{OUT} Efficiency

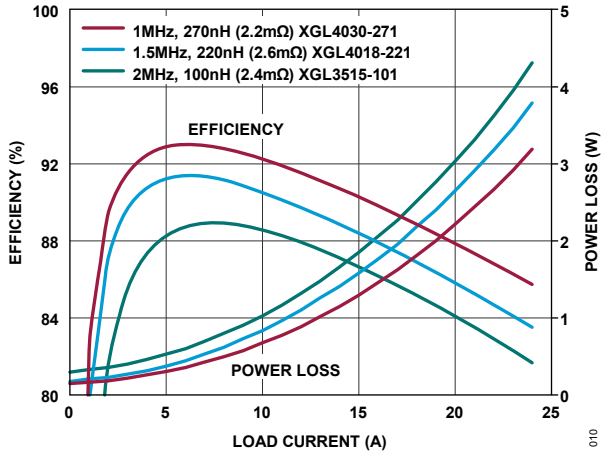


Figure 10. LT7176P-1 3.3V_{IN} to 0.8V_{OUT} Efficiency

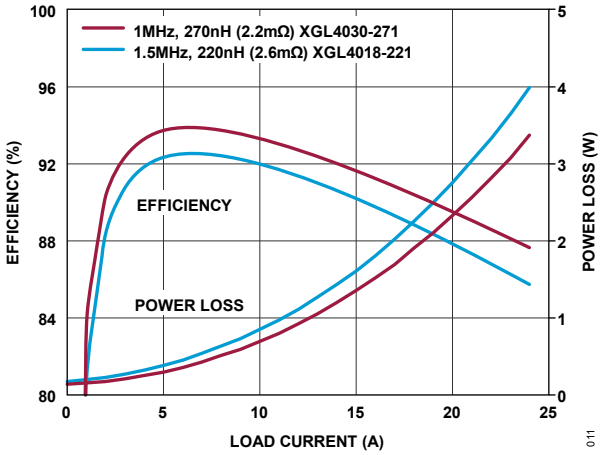


Figure 11. LT7176P-1 3.3V_{IN} to 1.0V_{OUT} Efficiency

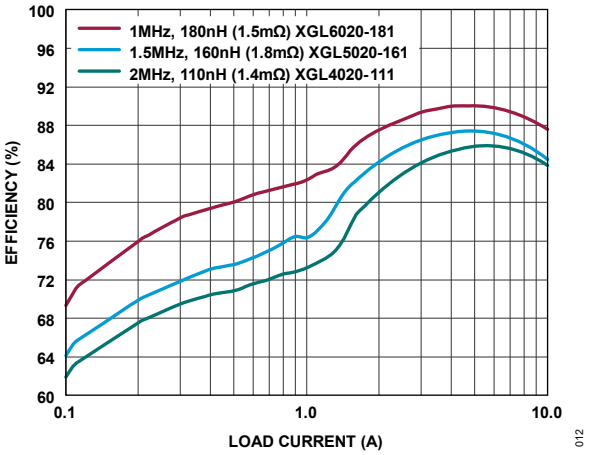


Figure 12. LT7176P 3.3V_{IN} to 0.5V_{OUT} PSM Efficiency

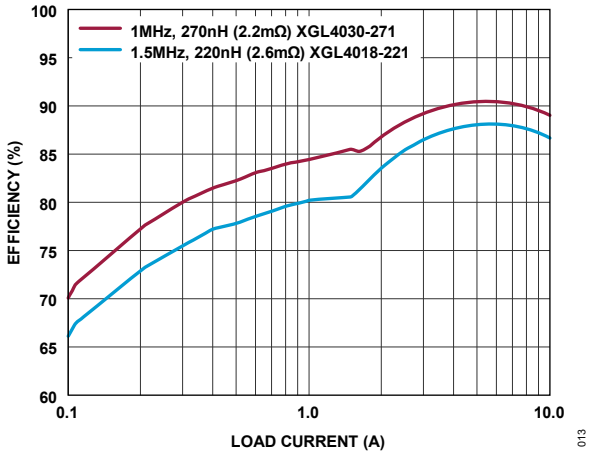


Figure 13. LT7176P-1 3.3V_{IN} to 0.5V_{OUT} PSM Efficiency

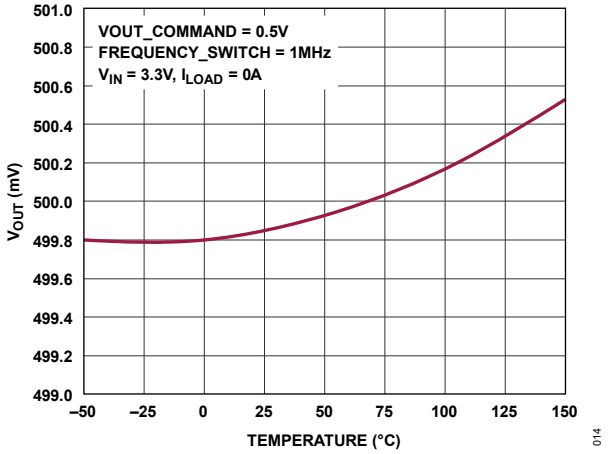


Figure 14. V_{OUT} vs. Temperature

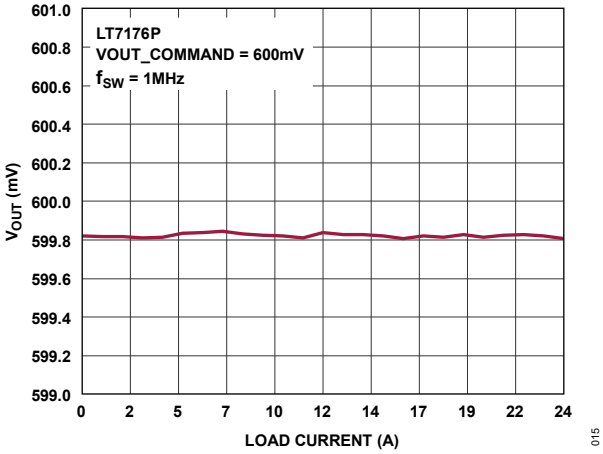


Figure 15. Load Regulation

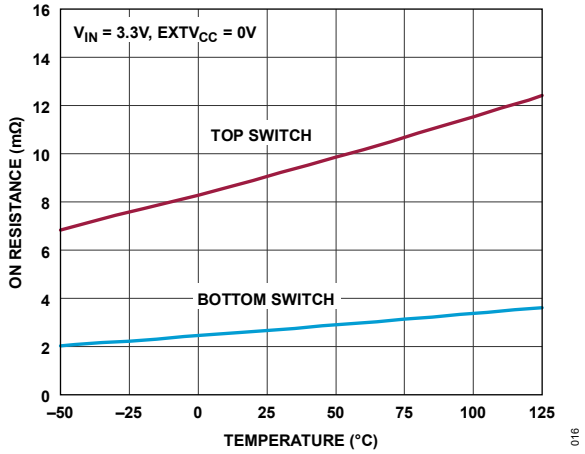


Figure 16. LT7176P-1 Switch On Resistance Per-Phase vs. Temperature

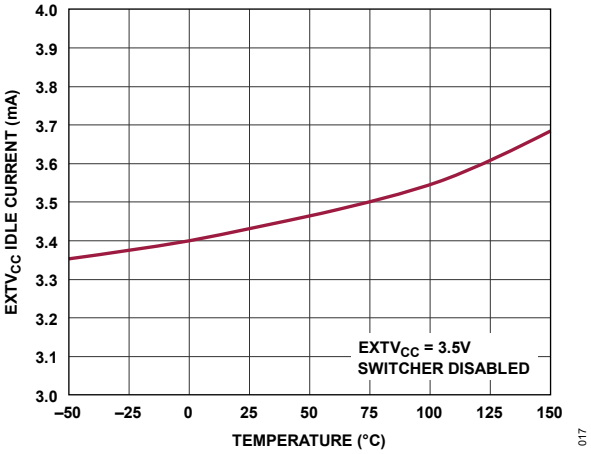


Figure 17. $EXTV_{CC}$ Idle Current vs. Temperature

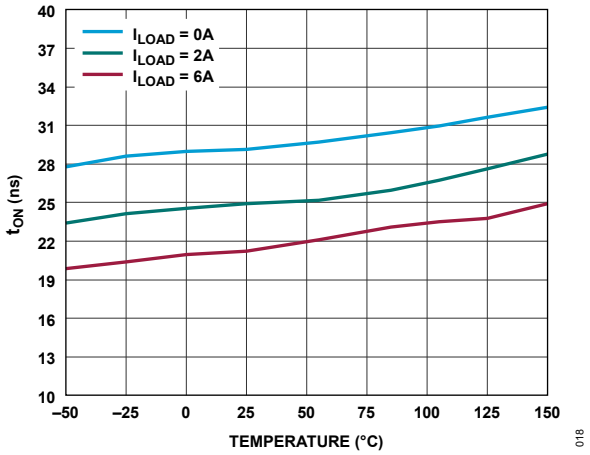


Figure 18. Minimum t_{ON}

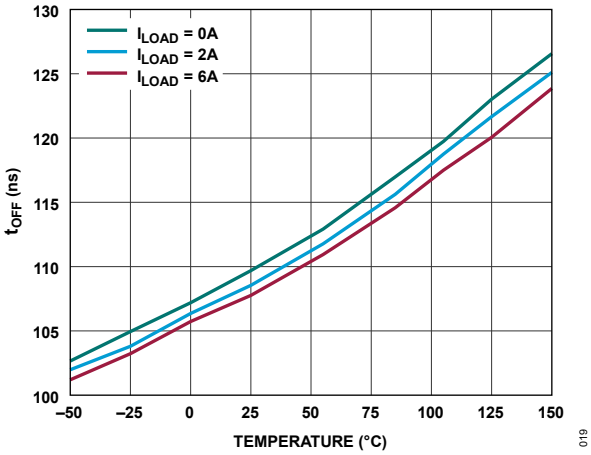


Figure 19. Minimum t_{OFF}

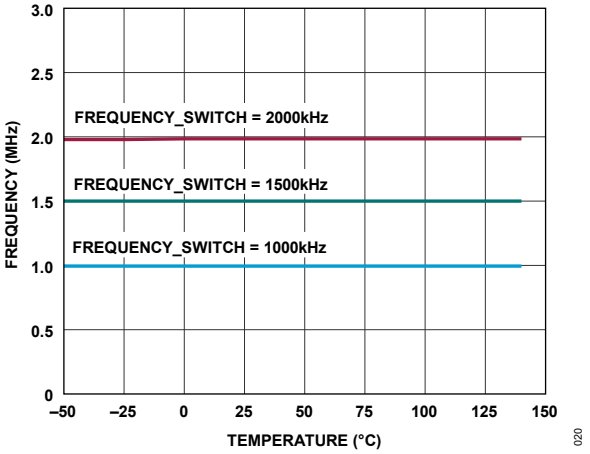


Figure 20. f_{SW} vs. Temperature

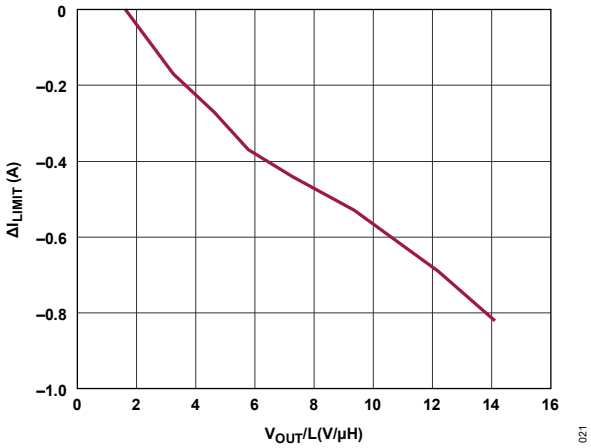


Figure 21. Valley Current-Limit Change (ΔI_{LIMIT}) vs. V_{OUT}/L

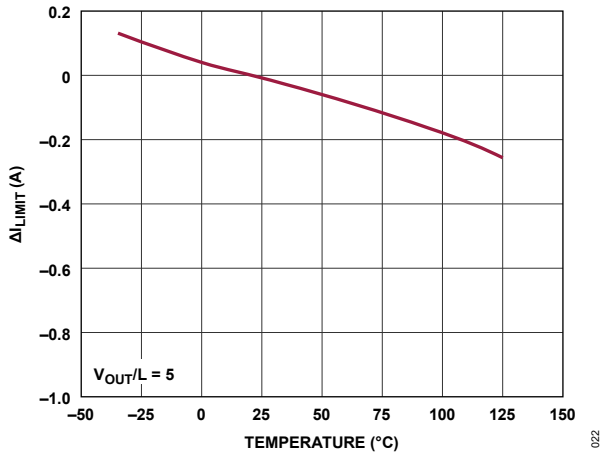


Figure 22. ΔI_{LIMIT} vs. Temperature

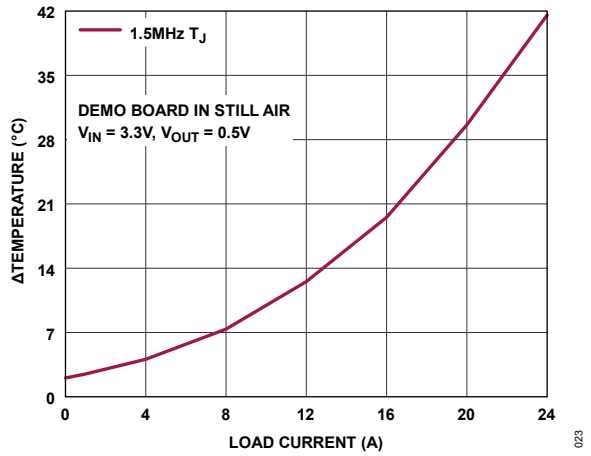


Figure 23. Temperature Rise vs. Load Current

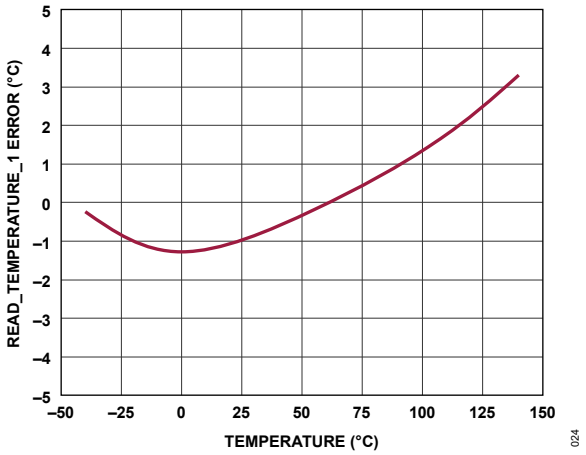


Figure 24. READ_TEMPERATURE_1 Error vs. Temperature

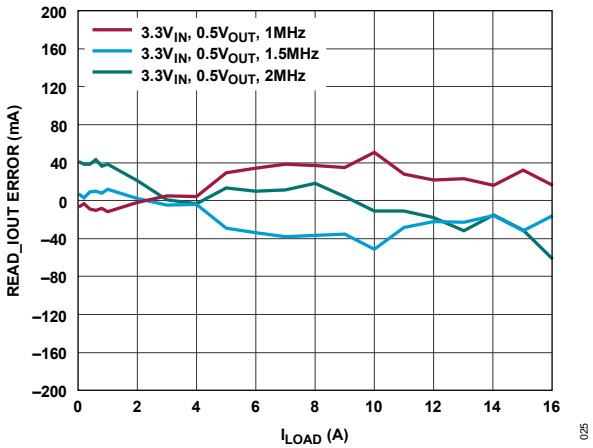


Figure 25. READ_IOUT Error vs. Load Current

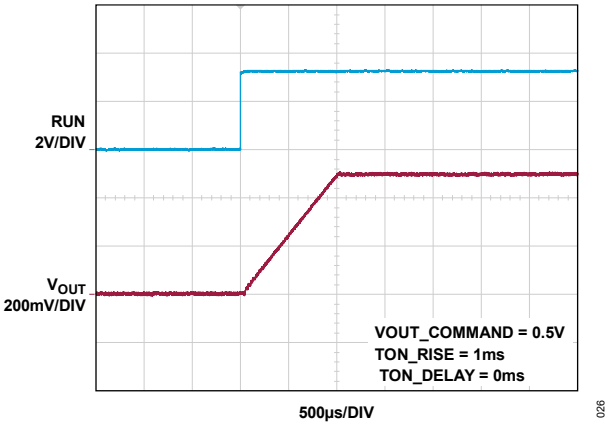


Figure 26. Soft-Start Ramp

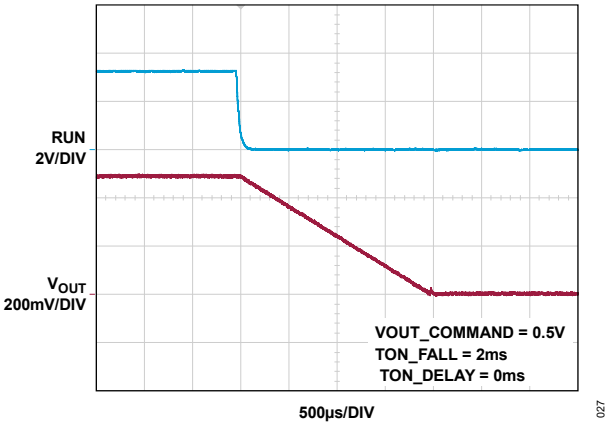


Figure 27. Soft-Off Ramp

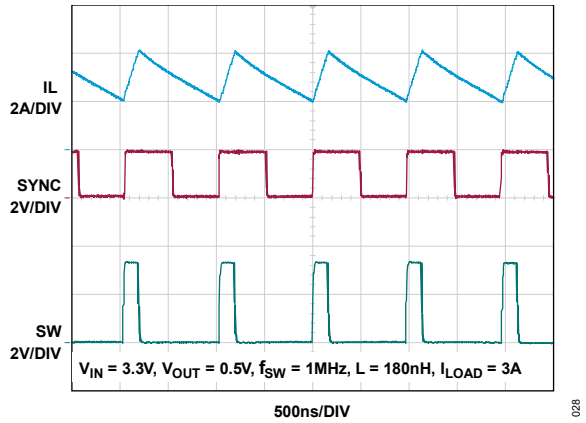


Figure 28. LT7176P Inductor Current, Switch Pin, and SYNC Output Waveforms

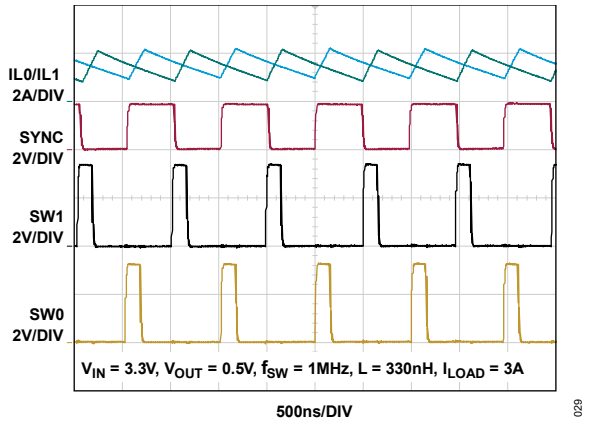


Figure 29. LT7176P-1 Inductor Currents, Switch Pins, and SYNC Output Waveforms

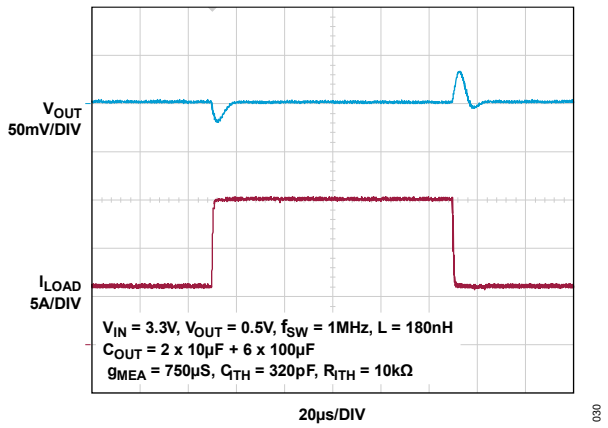


Figure 30. LT7176P, Single Phase, Transient Response: Load Current Step, 6A to 15A

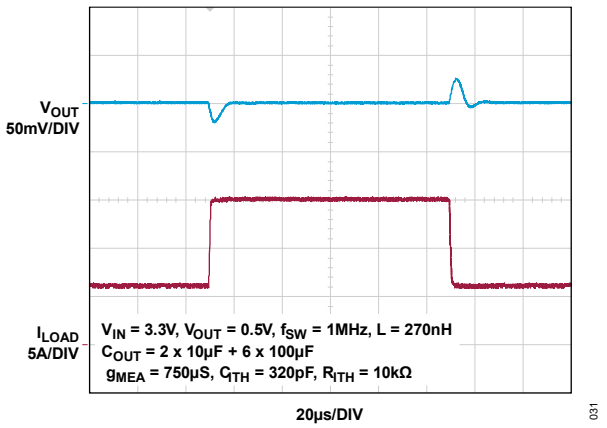


Figure 31. LT7176P-1, Dual Phase, Transient Response: Load Current Step, 6A to 15A

THEORY OF OPERATION

Overview

The LT7176P/LT7176P-1 are monolithic, PolyPhase, DC/DC synchronous step-down regulators capable of providing up to 24A of continuous output current with input supply voltages up to 4V. For the LT7176P, connect SW0 and SW1 together to a single inductor to drive a single-regulated output supply. For the LT7176P-1 dual-phase option, connect an inductor to each of the switch pins, SW0 and SW1, to drive a single-regulated output supply. The switching phases are set to 180° out-of-phase. The phase selected by configuration resistors or by the MFR_PWM_PHASE_LT7176 command sets the phase difference between the SYNC input and SW0 output. The I²C-based serial interface is compatible with PMBus 1.3, which supports bus speeds up to 1MHz.

Major features include the following:

- Programmable Output Voltage
- Programmable Current Limit
- Programmable Switching Frequency
- Programmable Overvoltage and Undervoltage Comparators
- Programmable On and Off Delay Times
- Programmable Output Rise and/or Fall Times
- Programmable Control Loop Compensation
- Programmable Input Undervoltage Threshold
- Selectable Switch Slew Rate for EMI and Efficiency Optimization
- Dedicated Power-Good Pin
- Phase-Locked Loop (PLL) for Synchronous Operation with an External Clock, PolyPhase Operation (up to Four Devices)
- Input and Output Voltage, Output Current, and Die Temperature Telemetry
- Programmable Output Current Readback Sampling Window
- Reduced Power Telemetry Mode that Slows Analog-to-Digital Converter (ADC) Sampling Frequency to Reduce Input Quiescent Current
- Fully Differential Remote V_{OUT} Sense
- 3× Programmable Nonvolatile Configuration Memory with Error Correcting Code (ECC)
- Optional External Configuration Resistors to Set Key Operating Parameters
- Standalone Operation Using Either Configuration Resistors or Nonvolatile Configuration Memory
- A Variety of Fault and Warning Handling and Reporting Mechanisms
- Optional Time-Base Interconnect for Synchronization Between Multiple Devices
- WP Pin to Write-Protect Internal Configuration

A dedicated $\overline{\text{ALERT}}$ pin is provided to indicate faults or warnings occurred. Individual status commands enable fault and warning reporting to identify the specific event.

The $\overline{\text{FAULT}}$ pins of the LT7176P/LT7176P-1 enable fault sharing between channels and with other ADI power system management products, including the LTC3880, LTC2974, LTC2978, LTC4676 µModule®, and more. Fault reporting and shutdown behavior are fully configurable using the $\overline{\text{FAULT}}$ pins and MFR_FAULT_PROPAGATE_LT7176P command. Faults can be individually masked, and the fault responses can be programmed to retry (unlatched) or remain shut down (latch-off) the regulator output. Fault and warning detection capabilities include the following:

- Output Undervoltage and Overvoltage Faults and Warnings
- Internal Overtemperature Fault and Warning
- Communication, Memory, or Logic (CML) Faults
- Input Overvoltage Fault and Undervoltage Warning
- Output Overcurrent Fault and Warning
- External Fault Detection Using the Bidirectional $\overline{\text{FAULT}}$ Pins

Switching Regulator Control Loop

The LT7176P/LT7176P-1 employ a controlled on-time, valley current mode architecture. In normal operation, the internal top power, metal-oxide semiconductor FET (MOSFET) is turned on for an interval determined by an on-time control circuit. When the top power MOSFET turns off, the bottom power MOSFET turns on until the valley current comparator trips, restarting the on-time control circuit and initiating the next cycle. Inductor current is determined by sensing the voltage drop across the bottom power MOSFET when it is on. The error amplifier adjusts the average inductor current (I_{TH}) pin voltage by comparing the regulator output voltage with an internal reference digital-to-analog converter (DAC) output. The voltage on the I_{TH} pin sets the comparator threshold, which is compared with the sensed-inductor valley current. An increase in load current causes a drop in the output voltage relative to the internal reference. The error amplifier responds by forcing the I_{TH} voltage higher until the average inductor current matches that of the load current.

An internal PLL synchronizes the oscillator frequency to an external clock signal if one is present on the SYNC pin. If no external clock is applied, the f_{SW} is set by the FREQUENCY_SWITCH command, which can be initialized by using configuration resistors (see the *Setting Switching Frequency, Compensation Components, PWM Mode, Phase, and PolyPhase Operation* section for more details).

Light-Load Current Operation

The LT7176P/LT7176P-1 have two PWM modes of operation: pulse- skipping mode and forced continuous conduction mode. The PWM operating mode is selected by the MFR_PWM_MODE_LT7176 command bit 0, which can be initialized using configuration resistors. Pulse-skipping mode is always used during soft-start.

If pulse-skipping mode (PSM) is enabled, the inductor current is not allowed to reverse. The reverse current comparator, I_{REV}, turns off the bottom switch just before the inductor current reaches zero, preventing it from reversing and going negative. Both power MOSFETs remain off while the output capacitor supplies the load current until the I_{TH} node voltage rises above the zero current threshold to initiate the next cycle. PSM is not supported in the polyphase configuration. When external clock applied to the SYNC pin or bit 8 of MFR_CHAN_CONFIG_LT7176 is set to 1, the channel operates in forced continuous mode regardless of the MFR_PWM_MODE_LT7176 setting.

In forced continuous mode (FCM), the inductor current is allowed to reverse at light loads or under transient conditions. The inductor valley current is determined by the voltage on the I_{TH} node. In this mode, the efficiency at light loads is lower than in pulse-skipping mode. However, forced continuous mode exhibits lower output ripple, more consistent switching frequency, and faster transient response.

Nonvolatile Memory (NVM)

The LT7176P/LT7176P-1 contain internal programmable NVM with ECC to store user configuration settings. The NVM can be programmed up to three times. During NVM write operations, T_J must be between -40°C and +125°C, and $EXTV_{CC}$ must be biased between 9.6V to 13.2V.

In addition to ECC, the integrity of the on-board NVM is checked with a cyclic redundancy check (CRC) calculation after a power-on reset or execution of a RESTORE_USER_ALL command. If an invalid CRC is detected, the $\overline{\text{ALERT}}$,

SHARE_CLK, PGOOD, and RUN pins are pulled low, and the regulator output remains disabled until the issue is resolved.
Refer to the *LT7176/LT7176-1 PMBus/I²C Reference Manual* for more information about NVM programming.

Power-Up and Initialization

The LT7176P/LT7176P-1 are capable of standalone supply sequencing and controlled turn-on and turn-off operation. To reduce LT7176P/ LT7176P-1 power dissipation, $EXTV_{CC}$ can be driven with an external 3.0V to 12V supply. If $EXTV_{CC}$ is driven by a 3.0V to 12V supply, the supported V_{IN} input operating range is from 1.5V to 4V. Note that without $EXTV_{CC}$, the V_{IN} operating range is from 2.7V to 4V.

The LT7176P/LT7176P-1 initialize upon application of power to V_{IN} or $EXTV_{CC}$, or when an MFR_RESET or RESTORE_USER_ALL command is sent. In the initialization step, the LT7176P/LT7176P-1 read the NVM configuration and/or resistor configuration pins to set the initial state of the PMBus commands.

The PGOOD pin is held low during initialization and released after the output voltage reaches the target value. During initialization, SHARE_CLK is held low, and the $\overline{FAULT}$ pin is in high impedance state.

If the resistor configuration pins are enabled, the LT7176P/LT7176P-1 initialize certain commands based on the configuration resistor values, which supersede the NVM settings. Resistor configuration pins are enabled by factory default. Set bit 6 of the MFR_CONFIG_ALL_LT7176 command in the NVM to disable the configuration pins. See the *Using Resistor Configuration Pins* section for additional information.

For commands not initialized based on the configuration resistors, initial values are determined by the NVM or factory defaults. The LT7176P/LT7176P-1 initialization typically requires 5ms. If the resistor configuration pins are disabled, the initialization time is reduced to 3ms (typical).

After initialization is complete, comparators monitor V_{IN}. For the devices to operate, V_{IN} must exceed the programmable threshold set by the VIN_ON command. By default, SHARE_CLK is held low until V_{IN} exceeds VIN_ON or if V_{IN} falls below VIN_OFF. The default behavior is to turn off and remain off if SHARE_CLK is low. Refer to the MFR_CHAN_CONFIG_ LT7176 command in the *LT7176/LT7176-1 PMBus/I²C Reference Manual* for information on how to configure this behavior.

Soft-Start

When all conditions required for start-up are met and the output of the LT7176P or LT7176P-1 is enabled, the device waits for the commanded turn-on delay and ramps the target output voltage up to the commanded voltage set point. The turn-on delay is set by the TON_DELAY command, which is 0ms by default. The soft-start ramp time is set by the TON_RISE command, which is 1ms by default. The time is internally rounded to the nearest 10us. The minimum output voltage rise time is limited by the internal digital ramp controller rise rate of 25V/ms and switch analog behavior, which is affected by output capacitance, current limit, and loop compensation. The LT7176P/LT7176P-1 always use pulse- skipping mode during soft-start, which allows the regulator to start up into a prebiased load. If forced continuous conduction mode is selected, the channel transitions to continuous conduction mode after the commanded voltage set point is reached.

Shutdown

The LT7176P/LT7176P-1 can be programmed to turn off immediately or to sequence off.

When sequencing off, the LT7176P/LT7176P-1 wait for the turn-off delay and then perform a soft stop ramp, by which the regulation target voltage is ramped down to zero. The turn-off delay is set by the TOFF_DELAY command, which defaults to zero. The target voltage ramp-down time is set by the TOFF_FALL command, which defaults to 2ms. By

default, the channel ramps off in forced continuous conduction mode.The ramp-off behavior can be configured using the MFR_PWM_MODE_ LT7176 command.

Sequencing off occurs if OPERATION is set to 0x40, or if the RUN pin is deasserted, and bit 0 of the ON_OFF_CONFIG command is set to 0 and bit 2 of the ON_OFF_CONFIG command is set to 1.

When immediate shutdown occurs, the regulators ramp the inductor current to zero as quickly as possible and then stop switching. In this case, the output voltage decays based only on the load current and the internal 250Ω pull-down on the V_{SENSEP} pin. Immediate shutdown occurs in any of the following situations:

- V_{IN} falls to less than the VIN_OFF threshold.
- If the OPERATION command is cleared to 0x00, or if bit 3 of the ON_OFF_CONFIG command is set to 1.
- A fault condition occurs that causes the output to turn off.
- The RUN pin is deasserted and the ON_OFF_CONFIG command is configured such that the RUN pin deassertion causes immediate shutdown as determined by bit 0 and bit 1 of the ON_OFF_CONFIG command.
- The $\overline{\text{FAULT}}$ pin for the channel is pulled low externally, unless MFR_FAULT_RESPONSE is cleared to 0x00.
- Loss of SHARE_CLK, unless bit 2 of MFR_CHAN_CONFIG_LT7176 is cleared.

Warning and Fault Handling

The LT7176P/LT7176P-1 continuously monitor the system for fault and warning conditions.

Fault responses are configurable using the corresponding FAULT_RESPONSE commands, such as VOUT_UV_FAULT_RESPONSE and VOUT_OV_FAULT_RESPONSE, and more. Possible fault responses are as follows:

- Ignores fault or warning condition and continues operation.
- Shuts down immediately and retries if the fault condition is no longer present.
- Shuts down immediately and latches off.

The remainder of this section describes the factory default warning and fault behavior. Refer to the supported PMBus and MFR commands table in the *LT7176/LT7176-1 PMBus/I²C Reference Manual* for details on configuring fault and warning behavior.

All faults and warnings are indicated in the PMBus status commands. The CLEAR_FAULTS command is used to clear any fault bits that are set. This command clears all bits in all status commands simultaneously. This command also deasserts the $\overline{\text{ALERT}}$ pin. If the fault is still present when the bit is cleared, the fault bit remains set, and the host is notified by asserting the $\overline{\text{ALERT}}$ pin low.

The CLEAR_FAULTS command does not cause a unit that has latched off for a fault condition to restart. Units that have shut down for a fault condition are restarted only when the fault condition is no longer present, and the following occurs:

- The output is commanded to turn off and then to turn back on using the RUN pin and/or OPERATION command.
- A MFR_RESET command is issued.
- V_{IN} and $EXTV_{CC}$ bias power are removed and reapplied to the LT7176P/LT7176P-1.

An LT7176P/LT7176P-1 retry following a fault does not clear the status command bits. Therefore, when the output powers on after a fault, the status bits can be read to determine the cause of the fault.

When a warning occurs related to the output voltage, output current, or temperature, the LT7176P/LT7176P-1 pull the $\overline{\text{ALERT}}$ pin low, the corresponding bit is set in the appropriate status commands, and the regulators continue to operate.

If the output voltage falls to less than VOUT_UV_FAULT_LIMIT, the LT7176P/LT7176P-1 respond as follows:

- The PGOOD pin pulls low.
- The $\overline{\text{ALERT}}$ pin pulls low.
- The VOUT_UV fault bit is set in the STATUS_VOUT, STATUS_BYTE, and STATUS_WORD commands.
- The devices continue to operate while limiting the maximum valley current.

If a fault occurs due to output overvoltage or input overvoltage, the LT7176P/LT7176P-1 respond as follows:

- The faulted device(s) are shut down immediately.
- The $\overline{\text{FAULT}}$ pin and PGOOD pin are pulled low.
- The $\overline{\text{ALERT}}$ pin pulls low.
- The corresponding indicator bits are set in the appropriate status commands.
- After 10ms MFR_RETRY_DELAY time, the LT7176P/LT7176P-1 attempt to restart when the fault condition is no longer present.

If a fault occurs due to overtemperature, the LT7176P/LT7176P-1 respond as follows:

- The faulted device(s) are shut down immediately.
- The $\overline{\text{FAULT}}$ pin and PGOOD pin are pulled low.
- The $\overline{\text{ALERT}}$ pin pulls low.
- The overtemperature (OT) bit is set in the appropriate status commands.
- When the ADC measures that the temperature is less than the overtemperature threshold, the LT7176P/LT7176P-1 attempt to restart.

Table 6. Factory Default Warnings and Faults Behavior

WARNING OR $\overline{\text{FAULT}}$ TYPE	DETECTION METHOD	DEFAULT THRESHOLD	DEFAULT REGULATOR RESPONSE	DEFAULT PIN RESPONSE		
				PGOOD	$\overline{\text{FAULT}}$	$\overline{\text{ALERT}}$
V_{OUT} UV Warning	Comparator	VOUT_COMMAND: -6.5%	Continues Operation	High-Z	High-Z	Pull Low
V_{OUT} OV Warning	Comparator	VOUT_COMMAND: 7.5%	Continues Operation	High-Z	High-Z	Pull Low
V_{OUT} UV Fault	Comparator	VOUT_COMMAND: -7%	Continues Operation	Pull low	High-Z	Pull Low
V_{OUT} OV Fault	Comparator	VOUT_COMMAND: 10%	Shuts Down and Retries	Pull low	Pull low	Pull Low
V_{IN} OV Fault	Comparator	6V	Shuts Down and Retries	Pull low	Pull low	Pull Low
V_{IN} UV Warning	ADC	-1.0V (Disabled)	Continues Operation	High-Z	High-Z	Pull Low
Overtemperature Warning	ADC	140°C	Continues Operation	High-Z	High-Z	Pull Low
Overtemperature Fault	ADC	160°C	Shuts Down and Retries	Pull low	Pull low	Pull Low

I_{OUT} Overcurrent (IOUT_OC) Warning	ADC	Average Current (I_{AVG}) > 24A	Continues Operation	High-Z	High-Z	Pull Low
I_{OUT} Overcurrent Fault	Valley comparator	I_{VALLEY} > 12A[1]	Continues Operation	High-Z	High-Z	High-Z
Turn-On Time (T_{ON_MAX}) Fault	Comparator and Timer	5ms Without Exceeding VOUT_UV_FAULT_LIMIT	Continues Operation	Pull Low	High-Z	Pull Low
Turn-Off Time (T_{OFF_MAX}) Warning	ADC and Timer	0 (Disabled)	Not Applicable	High-Z	High-Z	High-Z
SYNC Input Clock Error[2]	Input and Output	Not Applicable	Locks Off Until Next Reset	Pull Low	Pull Low	Pull Low
Pin Configuration Error[3]	I/O	Not Applicable	Locks Off Until Next Reset	Pull Low	Pull Low	Pull Low
NVM Error	CRC, ECC	Not Applicable	Locks Off Until Next Reset	Pull Low	High-Z	Pull Low
PMBus/I²C Communication Error (CML)	Logic	Not Applicable	Not Applicable	High-Z	High-Z	Pull Low

[1] The IOUT_OC_FAULT valley current threshold is controlled by MFR_PWM_MODE_LT7176, bits[10:9].

[2] When a SYNC input clock error is detected during initialization, the output of the devices is disabled.

[3] When a pin configuration error is detected during initialization, the device pulls low the following pins: $\overline{\text{FAULT}}$, SHARE_CLK, PGOOD, and $\overline{\text{ALERT}}$.

$\overline{\text{FAULT}}$ Pin

A fault causes the $\overline{\text{FAULT}}$ pin to pull low if the corresponding FAULT_RESPONSE command is programmed to shut down the regulator output and the MFR_FAULT_PROPAGATE_LT7176 command is configured to propagate the fault to the open-drain $\overline{\text{FAULT}}$ pin. Once the LT7176P/LT7176P-1 pull down the $\overline{\text{FAULT}}$ pin, the device continues to hold the pin low until one of the following occurs:

- The device retries for faults configured to retry.
- The faulted device is disabled and then re-enabled.
- A RESTORE_USER_ALL or MFR_RESET command is received.
- Input power is removed from both V_{IN} and $EXTV_{CC}$.

The $\overline{\text{FAULT}}$ pin can also be used as an input to provide a method for the LT7176P/LT7176P-1 to respond to external faults. The LT7176P/LT7176P-1 turn off immediately if the $\overline{\text{FAULT}}$ pin is pulled low externally. This enables coordination of faults among multiple power system management products. *Table 6* defines the default pin response of $\overline{\text{FAULT}}$.

PGOOD Pin

The open-drain PGOOD pin is pulled low when the output is off for any reason, during soft-start and soft-stop, or if the output voltage is less than the VOUT_UV_FAULT_LIMIT.

$\overline{\text{ALERT}}$ Pin

The SMBALERT_MASK command configures the warning and fault indicators that cause the LT7176P/LT7176P-1 to pull down the open-drain $\overline{\text{ALERT}}$ pin.

Once the LT7176P or LT7176P-1 pulls down the $\overline{\text{ALERT}}$ pin, the device continues to hold the $\overline{\text{ALERT}}$ pin low until one of the following occurs:

- The output is shut off and turned on.
- A CLEAR_FAULTS, RESTORE_USER_ALL, or MFR_RESET command is received.
- All unmasked status bits are cleared by writing a 1 to each bit.
- The device successfully transmits its address in response to the PMBus alert response address.
- Input power is removed from V_{IN} and $EXTV_{CC}$.

APPLICATIONS INFORMATION

Using Resistor Configuration Pins

The LT7176P/LT7176P-1 have three resistor configuration pins, ASEL, VOUT_CFG, and PWM_CFG. Each pin uses a single ±1% resistor to select key operating parameters. The resistors on the configuration pins are measured upon power-up and execution of a RESTORE_USER_ALL or MFR_RESET command. The function of each resistor configuration pin is described in the following sections.

When configuration resistors are present and bit 6 of the MFR_CONFIG_ALL_LT7176 command in NVM is set to 0 (default), the LT7176P/LT7176P-1 follow the configuration resistors rather than the NVM settings. When bit 6 of the MFR_CONFIG_ALL_LT7176 command is set to 1 in NVM, the device ignores the configuration resistors on the VOUT_CFG and PWM_CFG pins, while the ASEL resistor is always respected. The LT7176P/LT7176P-1 configuration can also be updated during operation using PMBus commands regardless of whether the initial configuration is based on configuration resistors or NVM.

Setting the Device Address

Connect a 1% resistor from ASEL to ground (SGND or PGND) to select one of sixteen serial bus interface addresses, as shown in *Table 7*. The ASEL resistor value defines the LSBs [3:0] of the PMBus device address. Three MSBs [6:4] of the device address are determined by bits 6:4 of MFR_ADDRESS (default 0x4F). The ASEL pin is read at LT7176P/LT7176P-1 start-up and during reset operation. If the ASEL pin is left floating, the factory default 7-bit device address is 0x4F. If the ASEL pin is grounded, the factory default device address is 0x40.

Table 7. LT7176P/LT7176P-1 Address Configuration Using ASEL Resistor

ASEL RESISTOR VALUE (±1%)	VALUE OF PMBus DEVICE ADDRESS LSBs 3:0:
Floating or V_{DD18}	NVM Value of MFR_ADDRESS
124kΩ	0xF
107kΩ	0xE
93.1kΩ	0xD
80.6kΩ	0xC
69.8kΩ	0xB
60.4kΩ	0xA
51.1kΩ	0x9
43.2kΩ	0x8
36.5kΩ	0x7
30.9kΩ	0x6
25.5kΩ	0x5
21kΩ	0x4
16.5kΩ	0x3
11.8kΩ	0x2
6.65kΩ	0x1
0 (SGND)	0x0

Setting Output Voltage

The VOUT_COMMAND command specifies the output voltage when the regulator is enabled.

VOUT_COMMAND can be initialized using a resistor connected between the VOUT_CFG pin and the PGND or SGND pin based on the values in *Table 8*. If the VOUT_CFG pin is open or tied to V_{DD18}, the VOUT_COMMAND command is loaded from the NVM to set the output voltage.

The following commands are initialized based on a percentage of the VOUT_COMMAND command if the resistor configuration pins are used to initialize the output voltage:

- VOUT_OV_FAULT_LIMIT: 10%
- VOUT_OV_WARN_LIMIT: 7.5%
- VOUT_MAX: 7.5%
- VOUT_MARGIN_HIGH: 5%
- VOUT_MARGIN_LOW: -5%
- VOUT_UV_WARN_LIMIT: -6.5%
- VOUT_UV_FAULT_LIMIT: -7%

Table 8. VOUT_CFG Pin Configuration Resistor Selection

RESISTOR VALUE (±1%)	OUTPUT VOLTAGE SET POINT (V)[1]	V_{OUT} RANGE	EFFECTIVE ERROR AMPLIFIER GAIN FOR EXTERNAL COMPENSATION[3]	REGULATOR ENABLE[2]
Floating or V_{DD18}	Initialized from the NVM (default 0.3V)	Initialized from the NVM (default 0.3V ≤ V_{OUT} ≤ 1.375V)	Depends on V_{OUT} range (default 2400µS)	Initialized from the NVM (default: regulator is enabled if the RUN pin is asserted high).
124kΩ	1.5	0.8V ≤ V_{OUT} ≤ 2.75V	1200µS	Enabled if the RUN pin is asserted high.
107kΩ	1.35	0.8V ≤ V_{OUT} ≤ 2.75V		Enabled if the RUN pin is asserted high.
93.1kΩ	1.2	0.3V ≤ V_{OUT} ≤ 1.375V	2400µS	Enabled if the RUN pin is asserted high.
80.6kΩ	1.0	0.3V ≤ V_{OUT} ≤ 1.375V		Enabled if the RUN pin is asserted high.
69.8kΩ	0.95	0.3V ≤ V_{OUT} ≤ 1.375V		Enabled if the RUN pin is asserted high.
60.4kΩ	0.9	0.3V ≤ V_{OUT} ≤ 1.375V		Enabled if the RUN pin is asserted high.
51.1kΩ	0.85	0.3V ≤ V_{OUT} ≤ 1.375V		Enabled if the RUN pin is asserted high.
43.2kΩ	0.8	0.3V ≤ V_{OUT} ≤ 1.375V		Enabled if the RUN pin is asserted high.
36.5kΩ	0.72	0.3V ≤ V_{OUT} ≤ 1.375V		Enabled if the RUN pin is asserted high.
30.9kΩ	0.65	0.3V ≤ V_{OUT} ≤ 1.375V		Enabled if the RUN pin is asserted high.

25.5kΩ	0.6	0.3V ≤ V_{OUT} ≤ 1.375V	2400µS	Enabled if the RUN pin is asserted high.
21kΩ	0.55	0.3V ≤ V_{OUT} ≤ 1.375V		Enabled if the RUN pin is asserted high.
16.5kΩ	0.5	0.3V ≤ V_{OUT} ≤ 1.375V		Enabled if the RUN pin is asserted high.
11.8kΩ	0.45	0.3V ≤ V_{OUT} ≤ 1.375V		Enabled if the RUN pin is asserted high.
6.65kΩ	0.4	0.3V ≤ V_{OUT} ≤ 1.375V		Enabled if the RUN pin is asserted high.
0 (SGND)	Initialized from the NVM (default 0.3V)	Initialized from the NVM (default 0.3V ≤ V_{OUT} ≤ 1.375V)	Depends on V_{OUT} range (default 2400µS)	Disabled and the RUN pin is ignored.

[1] Output voltage set point is controlled by VOUT_COMMAND.

[2] The PMBus ON_OFF_CONFIG command selects whether the RUN pin and/or the PMBus OPERATION command enables the regulator.

[3] When internal compensation is selected by connecting I_{TH} to $INTV_{CC}$ and resistor configuration is enabled, the effective error amplifier gain is 300µS, except when initialized from the NVM by connecting VOUT_CFG to SGND or V_{DD18} or floating.

Setting Switching Frequency, Compensation Components, PWM Mode, Phase, and PolyPhase Operation

A RPWM_CFG connected between the PWM_CFG pin and the PGND or SGND pin, as shown in *Table 9* and *Table 10*, can be used to initialize the PWM configuration including frequency, phase, loop compensation, operating mode, and Polyphase operation.

Table 9. PWM_CFG Pin Configuration Resistor Selection for LT7176P

RESISTOR VALUE (±1%)	SWITCHING FREQUENCY[1]	INTERNAL COMPENSATION[1, 2]		PWM MODE[4]	SYNC OUTPUT/INPUT	POLYPHASE FOLLOWER/ LEADER	PWM PHASE SW0
		INTERNAL C_{ITH}	INTERNAL R_{ITH}				
Floating or V_{DD18}	Initialized from the NVM (default 1MHz)	Initialized from the NVM (default 320pF)	Initialized from the NVM (default 14kΩ)	Initialized from the NVM (default FCM)	Initialized from the NVM (default input)	Initialized from the NVM (default leader)	Initialized from the NVM (default 0°)
16.5kΩ	1.5MHz	320pF	20kΩ	FCM	Output	Leader	0°
0Ω (Grounded)	2MHz	320pF	20kΩ	FCM	Output	Leader	0°
30.9kΩ	1MHz	320pF	14kΩ	PSM	Input	Leader	0°
21kΩ	1.5MHz	320pF	20kΩ	PSM	Input	Leader	0°
6.65kΩ	2MHz	320pF	20kΩ	PSM	Input	Leader	0°
36.5kΩ	1MHz	320pF	14kΩ	FCM	Input	Follower	90°
25.5kΩ	1.5MHz	320pF	20kΩ	FCM	Input	Follower	180°
11.8kΩ	2MHz	320pF	20kΩ	FCM	Input	Follower	180°
43.2kΩ	1MHz	320pF	14kΩ	FCM	Input	Follower	180°

51.1kΩ	1MHz	320pF	20kΩ	FCM	Input	Follower	270°
Clock active throughout power-on reset and reset	Measured at power-on reset and reset	Determined by measured SYNC frequency [3]	Determined by measured SYNC frequency [3]	FCM	Clock active throughout power-on reset and reset		

Table 10. PWM_CFG Pin Configuration Resistor Selection for LT7176P-1

RESISTOR VALUE (±1%)	SWITCHING FREQUENCY[1]	INTERNAL COMPENSATION[1, 2]		PWM MODE[4]	SYNC OUTPUT/ INPUT	POLYPHASE FOLLOWER	PWM PHASE SW0/SW1
		INTERNAL C_{ITH}	INTERNAL R_{ITH}				
Floating or V_{DD18}	Initialized from the NVM (default 1MHz)	Initialized from the NVM (default 320pF)	Initialized from the NVM (default 14kΩ)	Initialized from the NVM (default FCM)	Initialized from the NVM (default input)	Initialized from the NVM (default leader)	Initialized from the NVM (default 0°)
16.5kΩ	1.5MHz	320pF	14kΩ	FCM	Output	Leader	0 / 180
0Ω (Grounded)	2MHz	320pF	14kΩ	FCM	Output	Leader	0 / 180
30.9kΩ	1MHz	320pF	14kΩ	PSM	Input	Leader	0 / 180
21kΩ	1.5MHz	320pF	14kΩ	PSM	Input	Leader	0 / 180
6.65kΩ	2MHz	320pF	14kΩ	PSM	Input	Leader	0 / 180
36.5kΩ	1MHz	320pF	14kΩ	FCM	Input	Follower	90 / 270
25.5kΩ	1.5MHz	320pF	14kΩ	FCM	Input	Follower	90 / 270
11.8kΩ	2MHz	320pF	14kΩ	FCM	Input	Follower	90 / 270
43.2kΩ	1MHz	320pF	14kΩ	FCM	Input	Follower	60 / 240
51.1kΩ	1MHz	320pF	14kΩ	FCM	Input	Follower	120 / 300
Clock active throughout power-on reset and reset	Measured at power-on reset and reset	Determined by measured SYNC frequency [3]	Determined by measured SYNC frequency [3]	FCM	Clock active throughout power-on reset and reset		

[1] If an external synchronization clock is applied, the configuration resistor value should be chosen to set the internal PWM switching frequency to a similar value to the input clock.

[2] For internal compensation, C_{ITH} is controlled by MFR_PWM_MODE_LT7176, bits [8:6], and R_{ITH} is controlled by MFR_PWM_MODE_LT7176, bits [5:3].

[3] When an external clock is detected during power-on reset and/or reset of the LT7176P/LT7176P-1, the external clock frequency is measured and internal compensation parameters, C_{ITH} and R_{ITH}, are chosen automatically as R_{ITH} = 14kΩ and C_{ITH} = 320pF.

[4] PWM mode is controlled by MFR_PWM_MODE_LT7176 bit 0. A value of 1 enables pulse-skipping mode.

Synchronization

The LT7176P/LT7176P-1 automatically synchronize PWM switching to an external clock input on the SYNC pin unless configured as an output driver or programmed to ignore the input clock. The LT7176P/ LT7176P-1 continue PWM operation using their own internal oscillator if the external clock signal is lost. If an external synchronization clock is used, it is recommended to program the FREQUENCY_SWITCH command or to use R_{PWM_CFG} to set the internal oscillator frequency to a value close to the external clock frequency to ensure the PWM frequency remains consistent if the external clock is lost. The LT7176P/LT7176P-1 can be programmed to ignore an external clock by writing a 1 to MFR_SYNC_CONFIG_ LT7176, bit 1.

For an input clock frequency from 1MHz to 1.25MHz, it is recommended to use a R_{PWM_CFG} that selects a PWM frequency of 1MHz. For an input clock frequency from 1.25MHz to 3MHz, it is recommended to use a R_{PWM_CFG} that selects a PWM frequency of 2MHz.

The LT7176P/LT7176P-1 can be configured to provide a synchronizing clock output on the SYNC pin to other devices by setting bit 0 of MFR_SYNC_CONFIG_LT7176 to 1.

If the SYNC output clock is enabled, the LT7176P/ LT7176P-1 drive the SYNC pin as a square wave from 0V to 1.88V (typical) at the frequency programmed in the FREQUENCY_SWITCH command. The phase of SYNC leads the phase of the SW0 PWM output by the value set in the MFR_PWM_PHASE_ LT7176 command. When using multiple devices connected with a common SYNC pin, only one device can be configured as an output.

When a clock is active on the SYNC pin, the MFR_PWM_PHASE_LT7176 command specifies the phase relationship between the rising edges of the SYNC pin and LT7176P/LT7176P-1 SW0 pin.

If an external clock is applied to the SYNC pin throughout initialization, and the function of the resistor configuration pins is not disabled, the LT7176P/LT7176P-1 measure the clock frequency and initialize the FREQUENCY_SWITCH command to the measured frequency rounded to the nearest 100kHz. In this case, MFR_PWM_PHASE is set to 0°. Note that unless the functionality of the resistor configuration pins is disabled, an external clock applied to the SYNC pin must be either active or inactive throughout the entire LT7176P/LT7176P-1 initialization process. If the clock activity changes during initialization, for example, if the clock starts after initialization begins but before it completes, the frequency measurement may be inaccurate, which can lead to the LT7176P/LT7176P-1 incorrectly initializing the FREQUENCY_SWITCH command or declaring a pin configuration fault. Refer to the MFR_PIN_CONFIG_STATUS command in the *LT7176/LT7176-1 PMBus/I²C Reference Manual* for more information on pin configuration faults.

Single Phase for the LT7176P

The LT7176P is a single-phase, monolithic, DC/DC synchronous, step-down regulator that delivers up to 24A of continuous output current. A single phase drives the SW0 and SW1 pins tied to one inductor to drive a single-regulated output supply.

For single-phase operation, connect the LT7176P SW0 and SW1 pins together and to a single inductor.

The phase selected by the configuration resistors or by MFR_PWM_PHASE_LT7176 sets the phase difference between SW0 and SYNC.

Dual Phase for the LT7176P-1

The LT7176P-1 is a dual-phase, monolithic, DC/DC synchronous, step-down regulator that delivers up to 24A of continuous output current. The switching phases are set to 180° out-of-phase. Connect an inductor to each of the switch pins, SW0 and SW1, to drive a single-regulated output supply.

The phase selected by the configuration resistors or by MFR_PWM_PHASE_LT7176 sets the phase difference between SW0 and SYNC.

PolyPhase Load Sharing

Multiple LT7176P/LT7176P-1 parts can be connected in parallel to provide a balanced PolyPhase load-share solution. The analog current mode control architecture of the LT7176P/LT7176P-1 ensure that load-sharing remains balanced among the phases.

The corresponding I_{TH}, $\overline{FAULT}$, V_{IN}, V_{SENSEP}, V_{SENSEN}, SYNC, SHARE_CLK, and RUN pins must be connected among all PolyPhase devices. The phases should be separated by 360/n°, where n is the number of phases in the PolyPhase array. In PolyPhase, exactly one device, either an LT7176P/LT7176P-1 or an external clock source, must be configured to drive a clock on SYNC.

In a PolyPhase array, exactly one LT7176P-1 device must be configured as a leader (MFR_CHAN_CONFIG_LT7176 bit 8 value of 0), and all other PolyPhase devices must be configured as followers (value set to 1).

PolyPhase mode can also be selected by connecting an appropriate resistor to set one device as a leader and other devices as followers from PWM_CFG to ground if MFR_CONFIG_ALL_LT7176 bit 6 is not set to ignore the PWM_CFG pin, as shown in *Table 9* and *Table 10.*

Operating Frequency Trade-Offs

The selection of the operating frequency is a trade-off between efficiency, component size, and input voltage range. The advantage of high frequency operation is that smaller inductor and capacitor values may be used, while the primary disadvantage is lower efficiency.

Minimum On-Time and Minimum Off-Time Considerations

The minimum on-time, $t_{ON\ (MIN)}$, is the smallest time duration in which the top power MOSFET can be in its on state. This time is a function of the output load and is typically 25ns at a 2.5A load. In continuous conduction, the worst-case minimum on-time limit imposes a maximum switching frequency as following:

$$f_{SW\ (MAX)} = V_{OUT}/(V_{IN} \times 40ns)$$

where, 40ns is the worst-case upper limit of $t_{ON\ (MIN)}$ for a 2.5A load.

If the frequency is set higher than $t_{ON\ (MIN)}$ allows, the LT7176P/LT7176P-1 valley-current control architecture keeps the output voltage in regulation, and f_{SW} decreases from its programmed value. High switching frequencies can be used in the design without causing output overvoltage. The dual-phase LT7176P-1 cannot maintain 180° phase separation when the frequency is set higher than $t_{ON\ (MIN)}$ allows.

The minimum off-time, $t_{OFF\ (MIN)}$, is the smallest time duration the LT7176P/LT7176P-1 are capable of turning on the bottom power MOSFETs, tripping the current comparators, and turning the bottom power MOSFETs back off. This time is approximately 110ns typical for a 2.5A load. The minimum off-time imposes a maximum duty cycle of $t_{ON}/(t_{ON} + t_{OFF\ (MIN)})$. If the V_{OUT}/V_{IN} ratio exceeds the maximum duty cycle, for example, due to input voltage dropping, the output voltage drops out of regulation.

To avoid the output voltage dropping out of regulation due to the $t_{OFF\ (MIN)}$ limitation, set f_{SW} no higher than the following:

$$f_{SW\ (MAX)} \leq (1 - (V_{OUT\ (MAX)}/V_{IN\ (MIN)}))/160ns$$

where, 160ns is the maximum $t_{OFF\ (MIN)}$ for the LT7176P/LT7176P-1.

Programmable Current Limit

The LT7176P/LT7176P-1 current limit operates by limiting the output current based on the valley of the inductor-current ripple waveform, as shown in *Figure 32* and *Figure 33*.

As shown in *Figure 32*, when the positive valley current limit is engaged (providing output current (I_{OUT}) to the load), the positive inductor valley current is I_{LIM_POS}, the average I_{OUT} is $I_{LIM_POS} + \Delta I_L/2$, and the peak inductor current ($I_{L\ (PEAK,\ MAX)}$) is $I_{LIM_POS} + \Delta I_L$, where ΔI_L is the inductor ripple current. If I_{LIM_POS} is reached, the IOUT_OC fault status bit is set. Refer to the status commands in the *LT7176/LT7176-1 PMBus/I²C Reference Manual*.

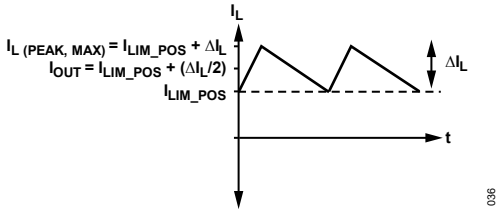


Figure 32. Positive Valley Current Limit

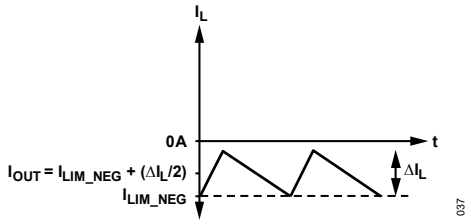


Figure 33. Negative Valley Current Limit

As shown in *Figure 33*, when the negative valley current limit occurs (sinking I_{OUT} due to the output being pulled up externally), the negative inductor valley current is I_{LIM_NEG}, the average I_{OUT} is $I_{LIM_NEG} + \Delta I_L/2$, and the peak inductor current is $I_{LIM_NEG} + \Delta I_L$.

The LT7176P/LT7176P-1 offer four settings for the valley current limit. The current-limit selection is controlled by MFR_PWM_MODE_LT7176, bits[10:9], as shown in *Table 11* and *Table 12*. The factory default current-limit setting for LT7176P-1 is a +12A (typical) I_{LIM_POS} and -6.7A (typical) I_{LIM_NEG}. Note that the modulator current sense gain, dI_{OUT}/dV_{ITH}, also changes as the current-limit selection changes, which must be considered in the control-loop compensation.

Table 11. LT7176P Valley Current-Limit Selection

MFR_PWM_MODE_LT7176 BITS[10:9]	I_{LIM_POS} TYPICAL (A)	I_{LIM_NEG} TYPICAL (A)	dI_{OUT}/dV_{ITH} TYPICAL (A/V)	MAXIMUM ΔI_L(A)
0	10	-6.8	18.66	9.6
1	14	-8.2	24.66	12
2	19	-11.4	33.78	7
3 (Default)	24	-13.4	41.56	6

Table 12. LT7176P-1 Valley Current-Limit Selection per Phase

MFR_PWM_MODE_LT7176 BITS[10:9]	I_{LIM_POS} TYPICAL (A)	I_{LIM_NEG} TYPICAL (A)	dI_{OUT}/dV_{ITH} TYPICAL (A/V)	MAXIMUM ΔI_L(A)
0	5	-3.4	9.33	4.8
1	7	-4.1	12.33	6
2	9.5	-5.7	16.89	4.5
3 (Default)	12	-6.7	20.78	3

Inductor Selection

For a given input voltage and output voltage application, the inductor value and operating frequency determine the ripple current as follows:

$$\Delta I_L = \frac{V_{OUT}}{f_{SW} \times L}\left(1 - \frac{V_{OUT}}{V_{IN}}\right)$$

Lower ripple current reduces core losses in the inductor and ESR losses in the output capacitors and reduces output voltage ripple. Do not exceed ripple current limits listed in *Table 11* and *Table 12*. To guarantee that ripple current does not exceed a specified maximum, choose the inductance according to the following:

$$L = \frac{V_{OUT}}{f_{SW} \times \Delta I_{L\,(MAX)}}\left(1 - \frac{V_{OUT}}{V_{IN}}\right)$$

Choose the inductor as follows such that the inductor current ripple is less than twice the maximum (least negative) negative valley current limit indicated in *Table 1*; otherwise, an output overvoltage occurs:

$$\Delta I_L \leq 2 \times I_{LIM_NEG(MAX)}$$

Choose an inductor with a saturation current (typically I_{SAT}) higher than the maximum peak current when operating in current limit as follows:

$$I_{L(PEAK,MAX)} = I_{LIM_POS} + \Delta I_L$$

To avoid overheating and poor efficiency, an inductor must be chosen with an RMS current rating greater than the maximum expected output load of the application. Preferably, the inductor RMS rating supports the average inductor current in current limit as follows:

$$I_{L\,(AVG,\,MAX)} = I_{LIM_POS} + \frac{\Delta I_L}{2}$$

Input and Output Capacitors

Use low ESR ceramic capacitors at both the input and output supplies of the switching regulators. Decouple the V_{IN} pins with 0201 low ESL ceramic capacitors of the largest value available to meet application temperature and voltage requirements. X5R or X7R ceramic capacitors are recommended for best performance over temperature and applied voltage.

Decouple the V_{IN} pins with low ESL and ESR ceramic capacitors as close as possible to the V_{IN} pins with returns to the appropriate ground return pins, as well as bulk ceramic capacitors to support the input ripple current.

See *Figure 40* and *Figure 41* for suggested output capacitor values. The output capacitor values must be selected to maintain stability over selected operating conditions including operating frequency, compensation (g_{MEA}, and compensation network, R_{ITH}, and C_{ITH}), as well as the programmed current limit, which selects the modulator transconductance.

Programmable PWM Control Loop Compensation

The LT7176P/LT7176P-1 support internal or external PWM control loop compensation, as shown in *Figure 34* and *Figure 35*.

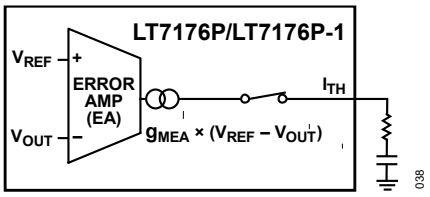


Figure 34. External Compensation with Programmable g_{MEA}

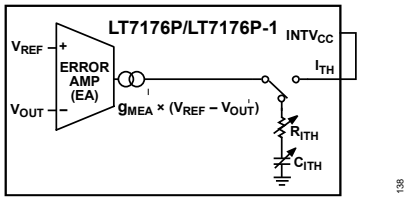


Figure 35. Programmable Internal Compensation

For single-phase applications, internal compensation is selected by tying the channel's I_{TH} pin to $INTV_{CC}$. PolyPhase operation requires external compensation, and the I_{TH} pins of all PolyPhase channels must be connected to one external compensation network.

Control loop compensation parameters can be programmed using the MFR_PWM_MODE_LT7176 command. In either internal or external compensation, the transconductance of the LT7176P/LT7176P-1 PWM error amplifier can be adjusted using MFR_PWM_MODE_LT7176, bits[15:11]. *Table 13* shows that the LT7176P/LT7176P-1 scale the value of g_{MEA} as a function of the selected V_{OUT} range set by MFR_CHAN_CONFIG_LT7176, bits [2:1].

When internal compensation is selected, the internal PWM loop compensation resistor, R_{ITH}, of the LT7176P/LT7176P-1 can be adjusted in nonlinear increments from 5kΩ to 60kΩ (typical) using MFR_PWM_MODE_LT7176, bit[5:3], as shown in *Table 14*. The internal compensation capacitor, C_{ITH}, can be adjusted in 40pF increments from 40pF to 320pF (typical) using MFR_PWM_MODE_LT7176, bits[8:6], as shown in *Table 15*.

Table 13. Programmable Error Amplifier Transconductance

V_{OUT} RANGE (V)	g_{MEA}
1.6 to 3.4	(MFR_PWM_MODE_LT7176, Bits[15:11] + 1) × 37.5µS
0.8 to 2.75	(MFR_PWM_MODE_LT7176, Bits[15:11] + 1) × 75.0µS
0.3 to 1.375	(MFR_PWM_MODE_LT7176, Bits[15:11] + 1) × 150µS

Table 14. Programmable Compensation Resistance (R_{ITH})

MFR_PWM_MODE_LT7176, BITS[5:3]	INTERNAL R_{ITH} VALUE (kΩ)
7	60
6	42
5	29
4	20
3	14
2	10
1	7
0	5

Table 15. Programmable Compensation Capacitance (C_{ITH})

MFR_PWM_MODE_LT7176, BITS[8:6]	INTERNAL C_{ITH} VALUE (pF)
7	320
6	280
5	240
4	200
3	160
2	120
1	80
0	40

Software-Configurable Sequencing

Time-based sequencing offers a software-configurable means of defining a system's power-up and power-down sequence. To employ time-based sequencing, program TON_DELAY to independently delay each device so that its soft-start ramp begins at the correct point in the sequence. The sequence begins when all devices are commanded on simultaneously using either the OPERATION command or RUN pins. Similarly, turn-off sequencing is coordinated using the TOFF_DELAY command.

When using time-based sequencing among multiple ADI devices, it is recommended that the SHARE_CLK pins of the devices be connected to a pull-up resistor from a 1.6V to 5.5V.

Event-Based Sequencing

Event-based sequencing offers a hardware configurable means of defining the power-up and power-down sequence of a multichannel system.

The PGOOD pin from one regulator can be connected to the RUN pin of the next regulator in the sequence, as shown in *Figure 36*.

The LT7176P/LT7176P-1 hold the PGOOD pin low until their soft-start ramp completes and their output voltage exceeds the value set in the VOUT_UV_FAULT_LIMIT command.

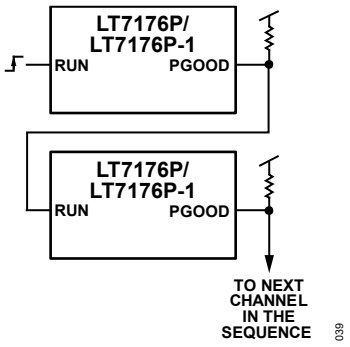


Figure 36. Event-Based Sequencing

LTpowerPlay GUI

LTpowerPlay is a powerful Windows®-based development environment that supports Analog Devices, Inc., digital power system management products, including the LT7176P/LT7176P-1. LTpowerPlay can be used to evaluate Analog Devices products by connecting to a demonstration board or the user application board. LTpowerPlay can also be used in offline mode (with no hardware present) to build multiple configuration files that can be saved and reloaded. LTpowerPlay provides valuable diagnostic information during initial system evaluation to program or adjust the power supplies or diagnose power issues. LTpowerPlay uses the Analog Devices *DC1613A* USB-to-I²C/SMBus/PMBus adapter to communicate with one of the many potential targets, including the EVAL-LT7176P-1-AZ demo board. In application, the 3.3V V_{CCIO} supply from the DC1613A can be connected to the $EXTV_{CC}$ pin of the LT7176P/LT7176P-1 for programming without applying V_{IN}. The LTpowerPlay software also provides an automatic update feature to keep the revision current with the latest set of device drivers and documentation. A great deal of context sensitive help is available within LTpowerPlay along with several tutorial demos. *https://www.analog.com/ltpowerplay* provides additional information on LTpowerPlay.

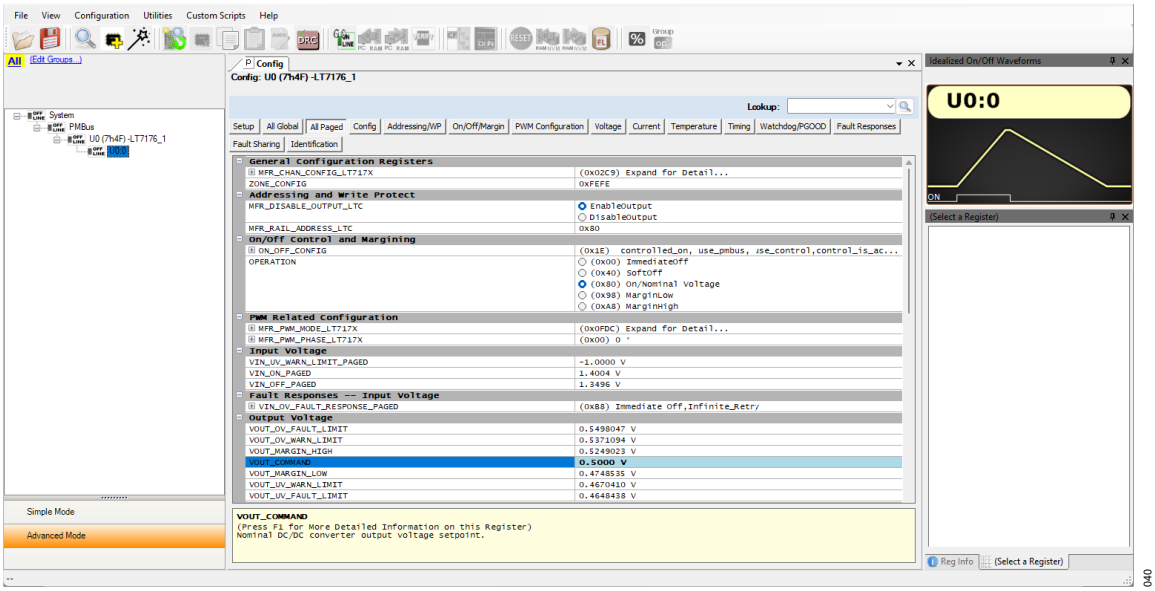


Figure 37. LTpowerPlay GUI Screenshot

PMBus/I²C SERIAL INTERFACE SUMMARY

This section provides an overview of some key features available through the LT7176P/LT7176P-1; however, it is not exhaustive. The companion document *LT7176/LT7176-1 PMBus/I²C Reference Manual* provides a detailed description of the available digital functionality. *Table 16* lists the supported commands.

The LT7176P/LT7176P-1 contain additional manufacturer-reserved commands not listed in *Table 16*. Reading these commands is harmless to the operation of the IC; however, the contents and meaning of these commands can change without notice.

Some of the unpublished commands are read only and generate a STATUS_CML, bit 6, fault if written to. Do not write to commands not published in *Table 16*.

Floating-point values listed in the default value column are half-precision IEEE floating-point numbers.

Do not assume compatibility of commands between different devices based upon command names. Always refer to the data sheet of the manufacturer of each device for a complete definition of the function of the command.

Table 16. Supported Commands (Cells Left Intentionally Blank)

COMMAND NAME	CMD CODE	DESCRIPTION	TYPE	DATA FORMAT	UNIT	NVM[1]	DEFAULT VALUE
PAGE	0x00	Provides integration with multipage PMBus devices.	R/W byte	Register			0x00
OPERATION	0x01	Operating mode control: on and/or off, margin high and margin low.	R/W byte	Register		Y	0x80
ON_OFF_CONFIG	0x02	RUN pin and PMBus bus on and/or off command configuration.	R/W byte	Register		Y	0x1E
CLEAR_FAULTS	0x03	Clears any fault bits that are set.	Send byte				
PAGE_PLUS_WRITE	0x05	Writes a command directly to a specified page.	W block				
PAGE_PLUS_READ	0x06	Reads a command directly from a specified page.	R/W block				
ZONE_CONFIG	0x07	Assigns current page to specified zone number for ZONE_WRITE operations.	R/W word	Register		Y	0xFEFE
ZONE_ACTIVE	0x08	Selects active zone for ZONE_WRITE operations.	R/W word	Register			0xFEFE

WRITE_PROTECT	0x10	Level of protection provided by the device against accidental changes.	R/W byte	Register		Y	0x00
STORE_USER_ALL	0x15	Stores user operating memory to the NVM and can be written to thrice.	Send byte				
RESTORE_USER_ALL	0x16	Restores user operating memory from the NVM.	Send byte				
CAPABILITY	0x19	Summary of PMBus optional communication protocols supported by this device.	R byte	Register			0xD8
QUERY	0x1A	Asks if a given command is supported, and what data formats are supported.	Block R/W	Register			
SMBALERT_MASK	0x1B	Masks ALERT activity.	Block R/W	Register		Y	
VOUT_MODE	0x20	Output voltage format and exponent.	R byte	Register			0x60
VOUT_COMMAND	0x21	Nominal output voltage set point.	R/W word	IEEE	V	Y	0.3, 0x34CD
VOUT_MAX	0x24	Upper limit on the commanded output voltage.	R/W word	IEEE	V	Y	0.323, 0x352B
VOUT_MARGIN_HIGH	0x25	Margin high output voltage set point.	R/W word	IEEE	V	Y	0.315, 0x350A
VOUT_MARGIN_LOW	0x26	Margin low output voltage set point.	R/W word	IEEE	V	Y	0.3, 0x34CD
VOUT_TRANSITION_RATE	0x27	Rates the output changes when V_{OUT} commanded to a new value.	R/W word	IEEE	V/ms	Y	0.25, 0x3400
FREQUENCY_SWITCH	0x33	f_{SW} of the regulator.	R/W word	IEEE	kHz	Y	1000.0, 0x63D0
VIN_ON	0x35	Input voltage at which the unit must start power conversion.	R/W word	IEEE	V	Y	1.4, 0x3D9A
VIN_OFF	0x36	Input voltage at which the unit must stop power conversion.	R/W word	IEEE	V	Y	1.35, 0x3D66

IOUT_CAL_OFFSET	0x39	Offset for READ_IOUT.	R/W word	IEEE	A	Y	0.32, 0x351F
VOUT_OV_FAULT_LIMIT	0x40	Output overvoltage fault limit.	R/W word	IEEE	V	Y	0.33, 0x3548
VOUT_OV_FAULT_RESPONSE	0x41	Action taken by the device when an output overvoltage fault is detected.	R/W byte	Register		Y	0xB8
VOUT_OV_WARN_LIMIT	0x42	Output overvoltage warning limit.	R/W word	IEEE	V	Y	0.323, 0x352B
VOUT_UV_WARN_LIMIT	0x43	Output undervoltage warning limit.	R/W word	IEEE	V	Y	0.278, 0x3473
VOUT_UV_FAULT_LIMIT	0x44	Output undervoltage fault limit.	R/W word	IEEE	V	Y	0.27, 0x3452
VOUT_UV_FAULT_RESPONSE	0x45	Action taken by the device when an output undervoltage fault is detected.	R/W byte	Register		Y	0x00
IOUT_OC_FAULT_RESPONSE	0x47	Action taken by the device when an output overcurrent fault is detected.	R/W byte	Register		Y	0x00
IOUT_OC_WARN_LIMIT	0x4A	Output overcurrent warning limit.	R/W word	IEEE	A	Y	24.0, 0x4E00
OT_FAULT_LIMIT	0x4F	Internal overtemperature fault limit.	R/W word	IEEE	C	Y	160.0, 0x5900
OT_FAULT_RESPONSE	0x50	Action taken by the device when an internal overtemperature fault is detected.	R/W byte	Register		Y	0xC0
OT_WARN_LIMIT	0x51	Internal overtemperature warning limit.	R/W word	IEEE	C	Y	140.0, 0x5860
VIN_OV_FAULT_RESPONSE	0x56	Action taken by the device when an input overvoltage fault is detected.	R/W byte	Register		Y	0xB8
VIN_UV_WARN_LIMIT	0x58	Input supply undervoltage warning limit.	R/W word	IEEE	V	Y	-1.0, 0xBC00

TON_DELAY	0x60	Time from RUN and/or OPERATION on to output rail turn-on.	R/W word	IEEE	ms	Y	0.0, 0x0000
TON_RISE	0x61	Time from when the output starts to rise until the output voltage reaches the V_{OUT} commanded value.	R/W word	IEEE	ms	Y	1.0, 0x3C00
TON_MAX_FAULT_LIMIT	0x62	Maximum time from the start of TON_RISE for V_{OUT} to cross the VOUT_UV_FAULT_LIMIT.	R/W word	IEEE	ms	Y	5.0, 0x4500
TON_MAX_FAULT_RESPONSE	0x63	Action taken by the device when a TON_MAX_FAULT event is detected.	R/W byte	Register		Y	0x00
TOFF_DELAY	0x64	Time from RUN and/or OPERATION off to the start of TOFF_FALL ramp.	R/W word	IEEE	ms	Y	0.0, 0x0000
TOFF_FALL	0x65	Time from when the output starts to fall until the output reaches 0V.	R/W word	IEEE	ms	Y	2.0, 0x4000
TOFF_MAX_WARN_LIMIT	0x66	Maximum allowed time, after TOFF_FALL completed, for the unit to decay to less than MFR_DISCHARGE_THRESHOLD.	R/W word	IEEE	ms	Y	0.0, 0x0000
STATUS_BYTE	0x78	One byte summary of the fault condition of the unit.	R/W byte	Register			
STATUS_WORD	0x79	Two byte summary of the fault condition of the unit.	R/W word	Register			
STATUS_VOUT	0x7A	Output voltage fault and warning status.	R/W byte	Register			
STATUS_IOUT	0x7B	Output current fault and warning status.	R/W byte	Register			
STATUS_INPUT	0x7C	Input supply fault and warning status.	R/W byte	Register			

STATUS_TEMPERATURE	0x7D	Internal temperature fault and warning status for READ_TEMPERATURE_1.	R/W byte	Register			
STATUS_CML	0x7E	Communication and memory fault and warning status.	R/W byte	Register			
STATUS_MFR_SPECIFIC	0x80	Manufacturer-specific fault and state information.	R/W byte	Register			
READ_VIN	0x88	Measured input supply voltage.	R word	IEEE	V		
READ_VOUT	0x8B	Measured output voltage.	R word	IEEE	V		
READ_IOUT	0x8C	Measured output current.	R word	IEEE	A		
READ_TEMPERATURE_1	0x8D	Measured internal temperature.	R word	IEEE	C		
READ_FREQUENCY	0x95	Measured PWM f_{SW}.	R word	IEEE			
PMBUS_REVISION	0x98	PMBus revision supported by this device. Current revision is 1.3.	R byte	Register			0x33
MFR_ID	0x99	The manufacturer ID in ASCII.	R block				ADI
MFR_SERIAL	0x9E	Unique part serial number.	R block				
IC_DEVICE_ID	0xAD	Identification of the IC in ASCII.	R block				LT7176P or LT7176P-1
IC_DEVICE_REV	0xAE	Revision of the IC.	R block				
MFR_NVM_UNLOCK	0xBD	Contact *Analog Devices, Sales*. Only used for MFR_NVM_DATA bulk programming.					

MFR_NVM_USER_WRITES_REMAINING	0xBE	Number of STORE_USER_ALL writes remaining.	R byte	Register			
MFR_NVM_DATA	0xBF	Contact *Analog Devices, Sales*. Used for bulk programming. Not needed for STORE_USER_ALL.					
MFR_USER_DATA_00	0xC9	NVM word available for the user.	R/W word	Register		Y	0x0000
MFR_USER_DATA_01	0xCA	NVM word available for the user.	R/W word	Register		Y	0x0000
MFR_READ_EXTVCC	0xCD	Measured $EXTV_{CC}$ voltage, when enabled.	R word	IEEE	V		
MFR_READ_ITH	0xCE	Measured I_{TH} voltage, when enabled.	R word	IEEE	V		
MFR_CHAN_CONFIG_LT7176	0xD0	Configuration bits that are channel specific.	R/W word	Register		Y	0x02C9
MFR_CONFIG_ALL_LT7176	0xD1	General configuration bits.	R/W word	Register		Y	0x0000
MFR_FAULT_PROPAGATE_LT7176	0xD2	Configuration that determines which faults are propagated to the $\overline{FAULT}$ pin.	R/W word	Register		Y	0xA097
MFR_READ_ASEL	0xD3	Read ASEL pin resistor value.	R word	IEEE	kΩ		
MFR_PWM_MODE_LT7176	0xD4	Configuration for the PWM engine.	R/W word	Register		Y	0x0FDC
MFR_FAULT_RESPONSE	0xD5	Action to be taken by the device when the $\overline{FAULT}$ pin is externally asserted low.	R/W byte	Register		Y	0xC0
MFR_IOUT_PEAK	0xD7	Reports the maximum measured value of READ_IOUT since the last MFR_CLEAR_PEAKS.	R word	IEEE	A		
MFR_ADC_CONTROL_LT7176	0xD8	Configures the update rate of the measurements taken by the ADC.	R/W byte	Register		Y	0x0E

MFR_RETRY_DELAY	0xDB	Retry interval during fault retry mode.	R/W word	IEEE	ms	Y	10.0, 0x4900
MFR_VOUT_PEAK	0xDD	Maximum measured value of READ_VOUT since the last MFR_CLEAR_PEAKS.	R/W word	IEEE	V		
MFR_VIN_PEAK	0xDE	Maximum measured value of READ_VIN since the last MFR_CLEAR_PEAKS.	R/W word	IEEE	V		
MFR_TEMPERATURE_1_PEAK	0xDF	Maximum measured value of internal temperature (READ_TEMPERATURE_1) since the last MFR_CLEAR_PEAKS.	R/W word	IEEE	C		
MFR_READ_PWM_CFG	0xE0	Measured PWM_CFG resistor value.	R word	IEEE	kΩ		
MFR_READ_VOUT_CFG	0xE1	Measured VOUT_CFG resistor value.	R word	IEEE	kΩ		
MFR_CLEAR_PEAKS	0xE3	Clears all peak values.	Send byte				
MFR_DISCHARGE_THRESHOLD	0xE4	Output voltage used to determine the output has decayed sufficiently to re-enable the channel.	R/W word	IEEE		Y	0.2, 0x3266
MFR_PADS_LT7176	0xE5	Digital status of the input and/or output pads.	R word	Register			
MFR_ ADDRESS	0xE6	Sets the 7-bit I^2C address byte.	R/W byte	Register		Y	0x4F
MFR_SPECIAL_ID	0xE7	ID code used by manufacturer.	R word	Register			0x1C1D
MFR_COMMON	0xEF	Manufacturer status bits common across multiple Analog Devices chips.	R byte	Register			
MFR_COMPARE_USER_ALL	0xF0	Compares current command contents with the NVM.	Send byte				
MFR_CHANNEL_STATE	0xF1	Returns the state of the channel.	R byte	Register			

MFR_PGOOD_DELAY	0xF2	Time output voltage must be between the undervoltage and overvoltage before PGOOD transitions high.	R/W word	IEEE		Y	1.0, 0x3C00
MFR_NOT_PGOOD_DELAY	0xF3	Time output voltage must be less than the undervoltage or more than the overvoltage before PGOOD transitions low.	R/W word	IEEE		Y	0.1, 0x2E66
MFR_PWM_PHASE_LT7176	0xF5	Sets the PWM phase.	R/W byte	Register		Y	0x00
MFR_SYNC_CONFIG_LT7176	0xF6	SYNC pin input/output configuration.	R/W byte	Register		Y	0x01
MFR_PIN_CONFIG_STATUS	0xF7	Pin configuration fault status.	R byte	Register			
MFR_RAIL_ADDRESS	0xFA	Common address for PolyPhase outputs to adjust common parameters.	R/W byte	Register		Y	0x80
MFR_DISABLE_OUTPUT	0xFB	Disables regulator outputs until reset.	R/W byte	Register			0x00
MFR_NVM_USER_WP	0xFC	Disables commands that write user NVM.	R/W byte	Register		Y	0x00
MFR_RESET	0xFD	Commanded reset without requiring a power down.	Send byte				

[1] A “Y” in the NVM column indicates these commands are stored and restored using the STORE_USER_ALL and RESTORE_USER_ALL commands, respectively.

LAYOUT CONSIDERATIONS

Note that large, switched currents flow in the LT7176P/LT7176P-1 V_{IN} and PGND pins and the input capacitors. Ensure the loops formed by the input capacitors are as small as possible by placing the input capacitors next to the V_{IN} and PGND pins.

Place the LT7176P/LT7176P-1 input capacitors, inductor, and output capacitors on the surface layer of the circuit board and make their connections on that layer. Place a local, unbroken ground plane under the application circuit on the layer closest to the surface layer.

Minimize the routing area of the SW and BOOST switching nodes to minimize electromagnetic interference (EMI) and reduce stray capacitance. For applications that use the full output current capacity of the LT7176P/LT7176P-1, ensure the selection of the PCB copper thickness and width supports the maximum SW current.

For more detail and PCB design files, refer to the *EVAL BOARD-LT7176* and *EVAL BOARD-LT7176-1* user guides for the LT7176P/LT7176P-1.

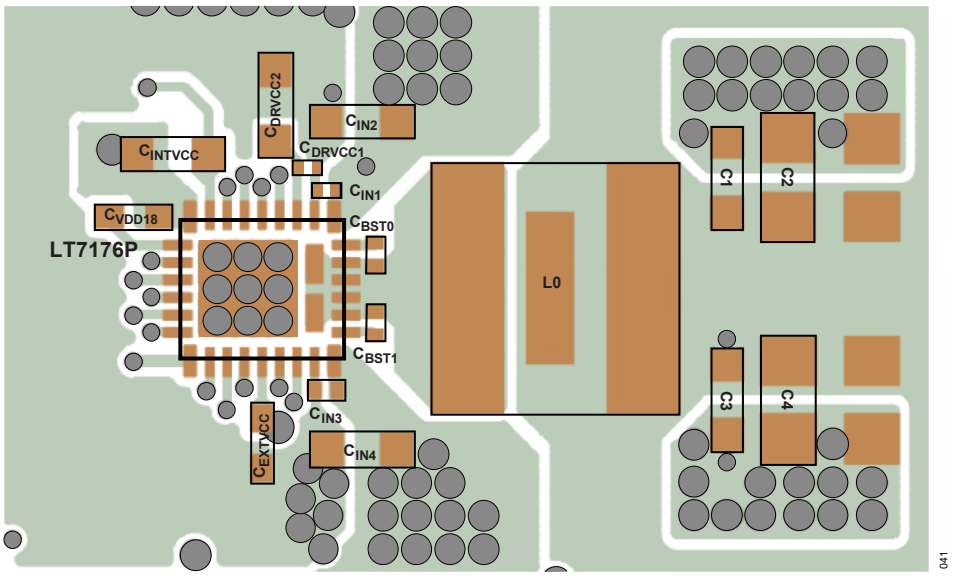


Figure 38. LT7176P Recommended PCB Layout

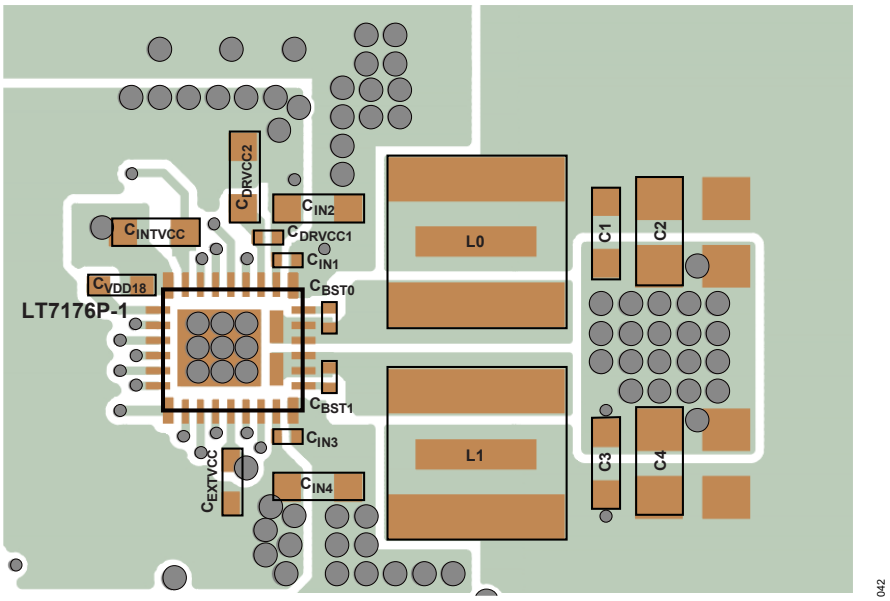


Figure 39. LT7176P-1 Recommended PCB Layout

THERMAL CONSIDERATIONS

Ensure the layout of the PCB includes good heat dissipation from the LT7176P/LT7176P-1. Solder the ground pins on the bottom of the package to a ground plane. Tie this ground to the large copper layers underneath with thermal vias. These layers spread heat dissipated by the LT7176P/LT7176P-1. Placing additional vias can reduce thermal resistance further. The LT7176P/LT7176P-1 offers exposed die back on the package top for heat sink mount. This option provides the capability to improve thermal performance for the same load if an appropriately sized heat sink is mounted correctly on the package. The maximum load current must be derated as the case temperature approaches the maximum junction rating.

The temperature rise of the LT7176P/LT7176P-1 is worst when operating at a high load, a high V_{IN}, and a high f_{SW}. If the case temperature is too high for a given application, either the V_{IN}, f_{SW}, or I_{LOAD} can be decreased to reduce the temperature to an acceptable level.

TYPICAL APPLICATIONS

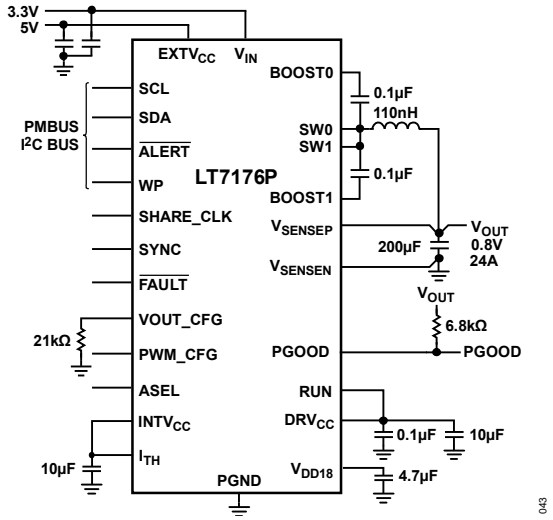


Figure 40. LT7176P 3.3V to 0.8V, 1MHz, 24A Single-Phase Regulator

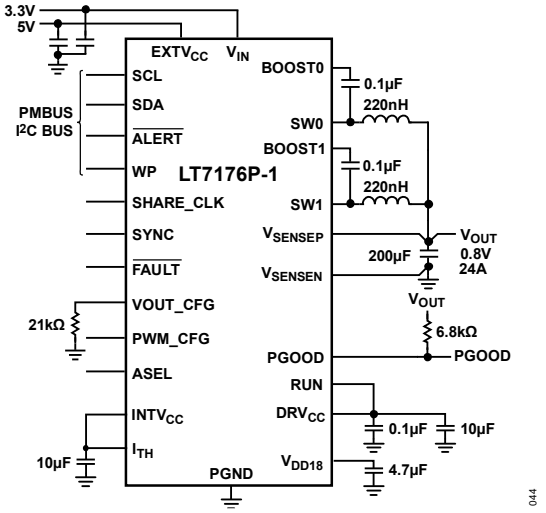


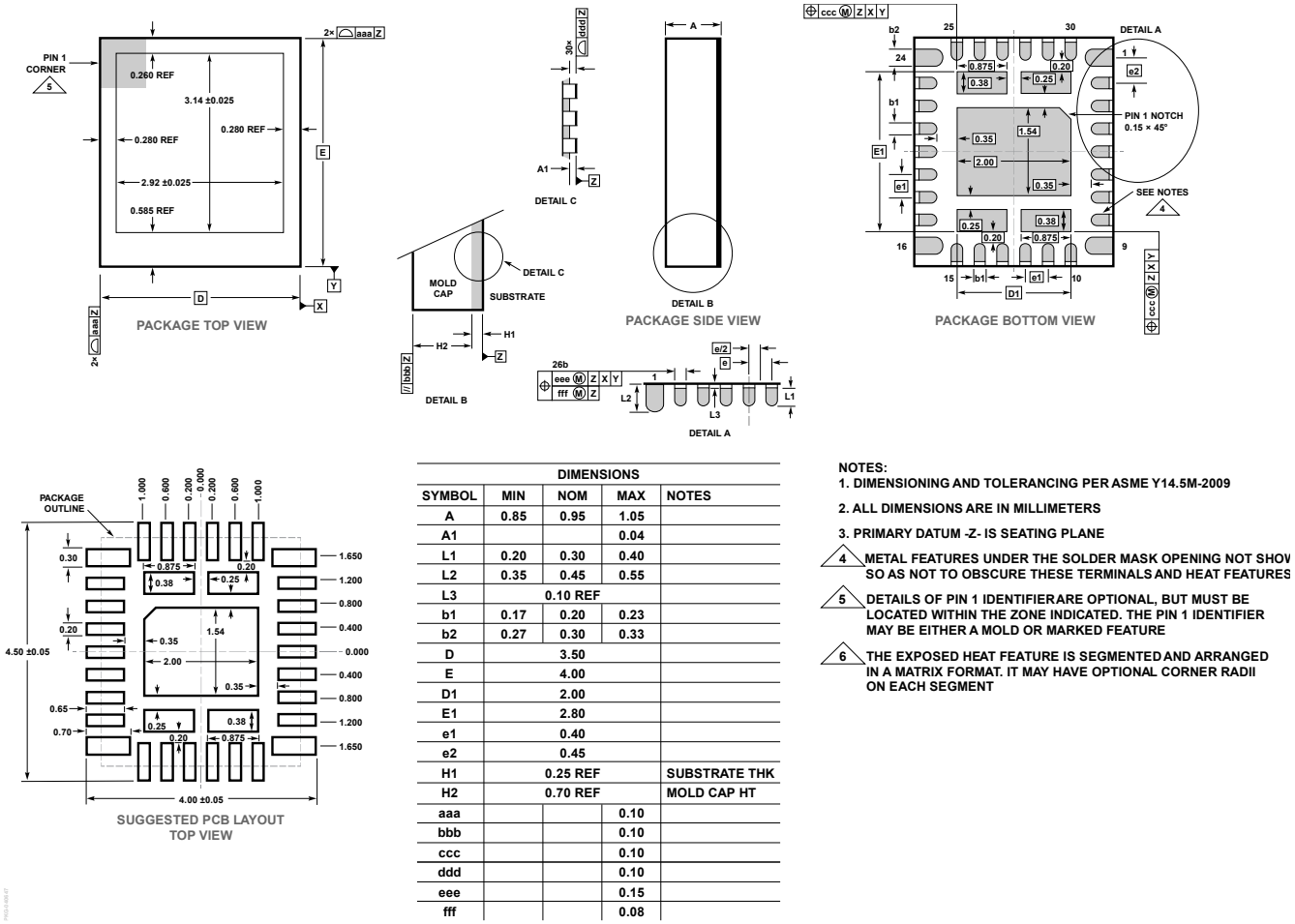
Figure 41. LT7176P-1 3.3V to 0.8V, 1MHz, 24A Dual-Phase Regulator

RELATED PARTS

Table 17. Related Parts

PART NUMBER	DESCRIPTION	COMMENTS
LT7182S	Dual-channel 6A, 20V PolyPhase Silent Switcher 2 step-down regulator with digital power system management	V_{IN}: 1.5V to 20V, $V_{OUT(MIN)}$ = 0.4V, 40-Lead, 7mm × 5mm × 0.9mm LQFN
LTC3887	Dual-output PolyPhase step-down DC/DC controller with digital power system management	V_{IN}: 4.5V to 24V, $V_{OUT(MIN)}$ = 0.5V, 40-Lead, 6mm × 6mm × 0.75mm QFN
LT8642-1	18V, 10A synchronous step-down Silent Switcher	V_{IN}: 2.5V to 18V, $V_{OUT(MIN)}$ = 0.6V, 20-Lead, 3mm × 4mm × 0.95mm LQFN

OUTLINE DIMENSIONS



DIMENSIONS				
SYMBOL	MIN	NOM	MAX	NOTES
A	0.85	0.95	1.05	
A1			0.04	
L1	0.20	0.30	0.40	
L2	0.35	0.45	0.55	
L3		0.10 REF		
b1	0.17	0.20	0.23	
b2	0.27	0.30	0.33	
D		3.50		
E		4.00		
D1		2.00		
E1		2.80		
e1		0.40		
e2		0.45		
H1		0.25 REF		SUBSTRATE THK
H2		0.70 REF		MOLD CAP HT
aaa			0.10	
bbb			0.10	
ccc			0.10	
ddd			0.10	
eee			0.15	
fff			0.08	

NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M-2009
2. ALL DIMENSIONS ARE IN MILLIMETERS
3. PRIMARY DATUM -Z- IS SEATING PLANE
4. METAL FEATURES UNDER THE SOLDER MASK OPENING NOT SHOV SO AS NOT TO OBSCURE THESE TERMINALS AND HEAT FEATURES
5. DETAILS OF PIN 1 IDENTIFIERARE OPTIONAL, BUT MUST BE LOCATED WITHIN THE ZONE INDICATED. THE PIN 1 IDENTIFIER MAY BE EITHER A MOLD OR MARKED FEATURE
6. THE EXPOSED HEAT FEATURE IS SEGMENTED AND ARRANGED IN A MATRIX FORMAT. IT MAY HAVE OPTIONAL CORNER RADII ON EACH SEGMENT

Figure 42. 30-Lead (3.5mm × 4mm) LQFN Package (CC-30-10) Dimensions Shown in Millimeters

ORDERING GUIDE

Table 18. Ordering Guide

MODEL[1]	PACKAGE MARK	TEMPERATURE RANGE	PACKAGE DESCRIPTION	PACKAGE OPTION
LT7176PRV#TRPBF	LHXY	-40°C to +150°C	30-Lead (3.5mm × 4mm) LQFN	CC-30-10
LT7176PRV-1#TRPBF	LHXZ			

[1] RoHS-compliant parts.

EVALUATION BOARDS

Table 19. Evaluation Boards

MODEL[1]	DESCRIPTION
EVAL-LT7176P-AZ	LT7176P Evaluation Board
EVAL-LT7176P-1-AZ	LT7176P-1 Evaluation Board

[1] Z = RoHS-compliant part.

REVISION HISTORY

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGE NUMBER
Sp0	05/26	Initial Release	—
A	07/26	Changed to open-market release, designated LT7176P as a future part	1, 54
B	10/26	Updated Ordering Information table	55

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