3A, Ultra-Low Noise, High PSRR, 45mV Dropout Ultra-Fast Linear Regulator

FEATURES

- **Ultra-low RMS Noise: 1.2µV$_{RMS}$ (10Hz to 100kHz)**
- **Ultra-low Spot Noise: 3nV/√Hz at 10kHz**
- **Ultra-low 1/f Noise: 7µV$_{P-P}$ from 0.1Hz to 10Hz**
- **High-Frequency PSRR: 52dB at 1MHz**
- **Ultra-fast Transient Response**
- **Dropout Voltage: 45mV Typical**
- **Digitally Programmable V$_{OUT}$: 0.5V to 4.2V**
- **Output Tolerance: ±1.5% Over Line, Load, and Temperature**
- **Precision Current Monitor: ±3% accuracy at 3A**
- Programmable Current Limit: ±3% at 3A
- Input Range: 0.6V to 5.5V
- Digital Output Margining: ±2.5%
- Stable with Ceramic Output Capacitors (10µF Minimum)
- Parallel Multiple Devices for Higher Current
- VIOC Pin to Control Upstream Switching Converter
- Precision Enable/Under Voltage Lock Out (UVLO)
- Power Good (PG) Flag
- Temperature Monitor
- 22-Lead (3mm x 4mm) LQFN Package

APPLICATIONS

- RF Power Supplies: PLLs, VCOs, Mixers, LNAs, PAs
- High Speed/High Precision Data Converters
- Low Noise Instrumentation
- Post-Regulator for Switching Supplies
- FPGA and DSP Power Supplies
- Medical Applications

GENERAL DESCRIPTION

The **LT®3073** is a low voltage, ultra-low noise, and ultra-fast transient response linear regulator. The device supplies up to 3A with a typical dropout voltage of 45mV. A 4.7µF reference bypass capacitor decreases output voltage noise to 1.2µV$_{RMS}$. The wide bandwidth and high PSRR permit the use of small ceramic capacitors, saving bulk capacitance and cost. The LT3073 is ideal for powering high-performance FPGAs, data converters, RF, and noise-sensitive signal chain applications.

The output voltage is digitally selectable in 50mV increments from 0.5V to 1.2V, 100mV increments from 1.2V to 1.8V, and discrete levels at 2V, 2.5V, 3V, 3.3V, and 4.2V. The LT3073's unity-gain operation provides virtually constant output noise, PSRR, bandwidth, and load regulation independent of the programmed output voltage. In addition, the LT3073 incorporates a unique tracking feature (VIOC) to control the upstream switching regulator to maintain a constant voltage across the LT3073 and minimize power dissipation.

A precision current monitor provides power monitoring for system energy management, while precision current limiting allows users to minimize input power supply size and cost. Built-in protection includes UVLO, internal current limit, and thermal shutdown with hysteresis. The LT3073 is available in a compact 22-lead (3mm X 4mm) LQFN package (Laminate package with QFN footprint).

SIMPLIFIED APPLICATION DIAGRAM

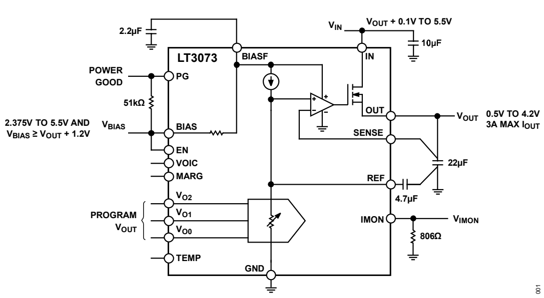

Figure 1. Simplified Application Diagram

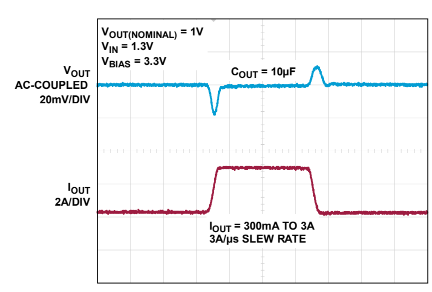

Figure 2. Transient Response

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REVISION HISTORY

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	01/23	Initial Release for Product Intro	—
A	05/25	Updated Electrical Characteristics table	
		Regulated Output Voltage Margining, Removed Min/Max Specifications	4
		BIAS Pin Current, VIN Voltage Specification	5
		Fast Start-Up Turn Off Threshold, Comments/Conditions Column	6
		Updated Figure 3	9
		Updated EN Pin Description	10
		Updated REF – Voltage Reference section	25
		Added Overdriving the REF Pin section	26
		Updated Enable Function – Turning ON and OFF section	27

SPECIFICATIONS

Table 1. Electrical Characteristics

(All typical specifications are at T_J (Junction Temperature) = 25°C and all min and max specifications are across the entire operating temperature range unless otherwise noted. C_{OUT} = 22µF, C_{REF} = 4.7µF, C_{BIASF} = 2.2µF, R_{MON} = 0.8kΩ, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS/COMMENTS	MIN	TYP	MAX	UNITS
IN Pin Voltage	V_{IN}				5.5	V
BIAS Pin Voltage[1]	V_{BIAS}		2.375		5.5	V
Regulated Output Voltage	V_{OUT}	V_{OUT} = 0.5V, 50mA ≤ I_{OUT} ≤ 3A, 0.7V ≤ V_{IN} ≤ 0.9V	0.4925	0.500	0.5075	V
		V_{OUT} = 1.2V, 10mA ≤ I_{OUT} ≤ 3A, 1.4V ≤ V_{IN} ≤ 1.6V	1.182	1.200	1.218	
		V_{OUT} = 3.3V, 10mA ≤ I_{OUT} ≤ 3A, 3.5V ≤ V_{IN} ≤ 3.7V	3.2505	3.300	3.3495	
		V_{OUT} = 4.2V, 10mA ≤ I_{OUT} ≤ 3A, 4.4V ≤ V_{IN} ≤ 4.6V	4.137	4.200	4.263	
Regulated Output Voltage Margining		MARG = V_{BIAS}		2.5		%
		MARG = GND		-2.5		
Output Offset Voltage [1,3]	V_{OS}	V_{OUT} = 1.2V, I_{LOAD} = 10mA, V_{BIAS} = 2.4V, V_{IN} = 1.4V, T_J = 25°C	-0.5		+0.25	mV
		0.5V ≤ V_{OUT} ≤ 4.2V, 50mA ≤ I_{LOAD} ≤ 3A, 0.6V ≤ V_{IN} ≤ 5.5V, 2.375V ≤ V_{BIAS} ≤ 5.5	-1.5		+0.5	
Line Regulation to V_{IN}	$\Delta V_{OUT} = f(\Delta V_{IN})$	V_{OUT} = 0. 5V, ΔV_{IN} = 0.7V to 5.5V, V_{BIAS} = 2.375V, I_{OUT} = 50mA			0.5	mV
		V_{OUT} = 4.2V, ΔV_{IN} = 4.4V to 5.5V, V_{BIAS} = 5.5V, I_{OUT} = 10mA			0.6	
Line Regulation to V_{BIAS}	$\Delta V_{OUT} = f(\Delta V_{BIAS})$	V_{OUT} = 0.5V, ΔV_{BIAS} = 2.375V to 5.5V, V_{IN} = 0.7V, I_{OUT} = 50mA			0.25	mV
		V_{OUT} = 3.3V, ΔV_{BIAS} = 4.5V to 5.5V, V_{IN} = 3.5V, I_{OUT} = 10mA			2	
Load Regulation [1]	$\Delta V_{OUT} = f(\Delta I_{OUT})$	ΔI_{OUT} = 50mA to 3A; V_{BIAS} = 2.375V, V_{IN} = 0.7V, V_{OUT} = 0.5V			0.6	mV
		ΔI_{OUT} = 10mA to 3A; V_{BIAS} = 2.4V, V_{IN} = 1.4V, V_{OUT} = 1.2V			1.2	
		V_{BIAS} = 4.5V, V_{IN} = 3.5V, V_{OUT} = 3.3V			3.3	
		V_{BIAS} = 5.4V, V_{IN} = 4.4V, V_{OUT} = 4.2V			4.2	
Dropout Voltage [2]	V_{DO}	V_{IN} = $V_{OUT(NOMINAL)}$, V_{BIAS} ≥ V_{OUT} + 1.2V, I_{OUT} = 1A; T_J = 25°C		15	22	mV
					33	

(All typical specifications are at T_J (Junction Temperature) = 25°C and all min and max specifications are across the entire operating temperature range unless otherwise noted. C_{OUT} = 22µF, C_{REF} = 4.7µF, C_{BIASF} = 2.2µF, R_{MON} = 0.8kΩ, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS/COMMENTS		MIN	TYP	MAX	UNITS
Dropout Voltage [2]	V_{DO}	$V_{IN} = V_{OUT(NOMINAL)}$, $V_{BIAS} \geq V_{OUT}$ + 1.2V, I_{OUT} = 2A	T_J = 25°C		30	44	mV
						66	
		$V_{IN} = V_{OUT(NOMINAL)}$, $V_{BIAS} \geq V_{OUT}$ + 1.2V, I_{OUT} = 3A	T_J = 25°C		45	65	
						100	
Minimum Load Current	$I_{OUT(MIN)}$	$V_{OUT} \geq$ 0.8V				10	mA
		V_{OUT} < 0.8V				50	
Ground Pin Current	I_{GND}	V_{BIAS} = 5.5V, V_{IN} = 1.5V, V_{OUT} = 1.2V, I_{OUT} = 10mA			4.3	6.5	mA
		V_{BIAS} = 5.5V, V_{IN} = 1.5V, V_{OUT} = 1.2V, I_{OUT} = 3A			5.2	7	
BIAS Pin Current	I_{BIAS}	V_{IN} = 1.5V, V_{OUT} = 1.2V, V_{BIAS} = 3.3V, I_{OUT} = 10mA			4.3	6.5	mA
		V_{IN} = 1.5V, V_{OUT} = 1.2V, V_{BIAS} = 3.3V, I_{OUT} = 3A			5.8	8	
BIAS Pin Current in Dropout [2]	I_{BIAS_DO}	$V_{BIAS} = V_{OUT}$ +1.2V, $V_{IN} = V_{OUT(NOMINAL)}$, I_{OUT} = 3A			5.4	7.5	mA
		V_{BIAS} = 5.5V, $V_{IN} = V_{OUT(NOMINAL)}$, I_{OUT} = 3A			35	50	
BIAS Pin Nap Mode Current	I_{BIAS_NAP}	V_{BIAS} = 5.5V, EN = 0V				10	µA
IN Pin Nap Mode Current	I_{IN_NAP}	V_{IN} = 5.5V, EN = 0V			20	500	µA
IMON Output Current		I_{OUT} = 3A, $V_{IN} - V_{OUT}$ = 0.2V		0.98	1.0	1.03	mA
		I_{OUT} = 1A, $V_{IN} - V_{OUT}$ = 0.2V		313.3	333.3	353.3	µA
I_{OUT}/I_{MON} Ratio		I_{OUT} = 3A, $V_{IN} - V_{OUT}$ = 0.2V		2912	3000	3060	
		I_{OUT} = 1A, $V_{IN} - V_{OUT}$ = 0.2V		2820	3000	3180	
IMON Shutdown Current		V_{BIAS} = 5.0V, EN = 0V				1	µA
Programmable Current Limit [3]	$I_{LIM(P)}$	R_{MON} = 1kΩ		2.93	3.0	3.07	A
		R_{MON} = 3kΩ		0.94	1.0	1.06	
Internal Current Limit [3]	$I_{LIM(I)}$	V_{IN} = 1.5V, ΔV_{OUT} = -5%, V_{BIAS} = 5.5V			4.5	5.5	A
V_{OUT} Threshold for Power Good		Percentage of $V_{OUT(NOMINAL)}$, V_{OUT} Rising		91	93	95	%
		Percentage of $V_{OUT(NOMINAL)}$, V_{OUT} Falling		88	90	92	
PG V_{OL}		I_{PG} = 200µA (Fault Condition)			60	100	mV
PG V_{OH} Leakage		$V_{PG} = V_{BIAS}$ = 5V				1	µA
Fast Start-Up REF Pin Current					2		mA

(All typical specifications are at T_J (Junction Temperature) = 25°C and all min and max specifications are across the entire operating temperature range unless otherwise noted. C_{OUT} = 22µF, C_{REF} = 4.7µF, C_{BIASF} = 2.2µF, R_{MON} = 0.8kΩ, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS/COMMENTS	MIN	TYP	MAX	UNITS
Fast Start-Up Turn Off Threshold		Measured as percentage of nominal REF pin voltage	96	98.8	101.5	%
TEMP Output Scale [4]				10		mV/°C
TEMP Output Error [4]		T_J = 25°C, V_{TEMP} = 250mV	–5		5	°C
		0°C < T_J ≤ 125°C	–9		9	
Thermal Shutdown		T_J Rising		168		°C
		Hysteresis		7		
V_{BIAS} Undervoltage Lockout		EN = V_{BIAS}, V_{IN} = 0V, V_{OUT} = 0V, V_{BIAS} Rising	2.16	2.2	2.24	V
		EN = V_{BIAS}, V_{IN} = 0V, V_{OUT} = 0V, V_{BIAS} Falling	2.03	2.07	2.11	
Input to Output Differential Voltage Control (VIOC) [5]		VIOC Amplifier Gain		1		V/V
		VIOC Amplifier Offset		800		mV
		VIOC Amplifier Accuracy, V_{IN} - V_{OUT} = 300mV	-20		20	
		VIOC Pin Source Current: V_{BIAS} > VIOC +1V	200			µA
V_{IL} Input Threshold (Logic-0 State) V_{O0}, V_{O1}, V_{O2}, MARG		Input Falling	0.3			V
V_{IZ} Input Range (Logic-Z State) V_{O0}, V_{O1}, V_{O2}, MARG			0.95		1.15	V
V_{IH} Input Threshold (Logic-1 State) V_{O0}, V_{O1}, V_{O2}, MARG		Input Rising			1.97	V
Input Hysteresis V_{O0}, V_{O1}, V_{O2}, MARG		Rising and Falling		80		mV
Input Pin Sink Current V_{O0}, V_{O1}, V_{O2}, MARG					50	µA
EN Pin Threshold		EN Trip Point Rising (Turn-On), V_{BIAS} = 2.375V	1.20	1.26	1.32	V
EN Pin Hysteresis		EN Trip Point Hysteresis, V_{BIAS} = 2.375V		80		mV
EN Pin Current	I_{EN}	V_{EN} = 0V, V_{BIAS} = 5.5V			±1	µA
		V_{EN} = 1.3V, V_{BIAS} = 5.5V		0.5		
		V_{EN} = 5.5V, V_{BIAS} = 0V		10	20	

(All typical specifications are at T_J (Junction Temperature) = 25°C and all min and max specifications are across the entire operating temperature range unless otherwise noted. C_{OUT} = 22µF, C_{REF} = 4.7µF, C_{BIASF} = 2.2µF, R_{MON} = 0.8kΩ, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS/COMMENTS		MIN	TYP	MAX	UNITS
V_{BIAS} Ripple Rejection	$PSRR_{BIAS}$	V_{BIAS} = 2.7V(Avg), V_{IN} = 1.5V, V_{OUT} = 1.2V	V_{RIPPLE} = 500mV_{P-P}, f_{RIPPLE} = 120Hz, I_{OUT} = 3A		106		dB
			V_{RIPPLE} = 500mV_{P-P}, f_{RIPPLE} = 1MHz, I_{OUT} = 3A		70		
V_{IN} Ripple Rejection	$PSRR_{IN}$	V_{BIAS} = 5V, V_{IN} =1.5V(Avg), V_{OUT} = 1.2V	V_{RIPPLE} = 50mV_{P-P}, f_{RIPPLE} = 120Hz, I_{OUT} = 3A		96		dB
			V_{RIPPLE} = 50mV_{P-P}, f_{RIPPLE} = 1MHz, I_{OUT} = 3A		52		
Output RMS Noise [6]	$V_{RMS(OUT)}$	V_{OUT} = 1V, I_{OUT} = 3A, V_{IN} = 1.3V, V_{BIAS} = 3.3V, C_{OUT} = 22µF	BW = 10Hz to 100kHz, C_{REF} = 4.7µF		1.2		µV_{RMS}
			BW = 10Hz to 100kHz, C_{REF} = 0.47µF		1.6		
Output Noise Spectral Density [6]	$V_{n(OUT)}$	V_{OUT} = 1V, I_{OUT} = 3A, V_{IN} = 1.3V, V_{BIAS} = 3.3V, C_{OUT} = 22µF	Frequency = 0.1Hz, C_{REF} = 4.7µF		1.4		µV/√Hz
			Frequency = 10Hz, C_{REF} = 4.7µF		40		nV/√Hz
			Frequency = 10Hz, C_{REF} = 0.47µF		320		
			Frequency = 10kHz, C_{REF} = 4.7µF		3		
			Frequency = 10kHz, C_{REF} = 0.47µF		3		
			Frequency = 100kHz, C_{REF} = 4.7µF		2.8		
			Frequency = 100kHz, C_{REF} = 0.47µF		2.8		

[1] To maintain proper performance and regulation, the BIAS supply voltage must satisfy the following conditions: $2.375V \leq V_{BIAS} \leq 5.5V$ and $V_{BIAS} \geq (V_{OUT} + 1.2V)$.

[2] Dropout voltage, V_{DO}, is the minimum input-to-output voltage differential at a specified output current. In dropout, the output voltage equals $V_{IN} - V_{DO}$.

[3] Operating conditions are limited by maximum junction temperature. The regulated output voltage specification does not apply to all possible input and output current combinations. When operating at maximum output current, limit the input voltage range to $V_{IN} \leq V_{OUT} + 600mV$.

[4] The TEMP output voltage represents the average temperature of the LT3073's power devices. Due to power dissipation, temperature gradients, and thermal time constants across the die, the TEMP output voltage measurement is not guaranteed to precisely track transient power excursions in the power device. The internal thermal shutdown sensor is designed to keep the LT3073 within its safe operating area.

[5] The VIOC buffer outputs a voltage equal to V_{IN}-V_{OUT}+800mV. See the *Applications Information* section for further information. The VIOC pin's source current can be set between 10µA and 200µA. The minimum voltage required from BIAS to VIOC is 1V.

[6] Adding a capacitor at the REF pin decreases output voltage noise. Adding this capacitor bypasses the REF pin internal resistor's thermal noise and the reference current's noise. The output noise then equals the error amplifier noise. The use of a REF pin bypass capacitor also increases start-up time.

ABSOLUTE MAXIMUM RATINGS

Table 2. Absolute maximum ratings

PARAMETER	RATING
IN Pin Voltage [1]	-0.3V to 6V
OUT Pin Voltage [1]	-0.3V to 6V
SENSE Pin Voltage [1]	-0.3V to 6V
BIAS, BIASF Pin Voltage [1]	-0.3V to 6V
V_{O0}, V_{O1}, V_{O2}, MARG Pin Voltage [1]	-0.3V to 5.5V
EN Pin Voltage [1]	-0.3V to 6V
VIOC Pin Voltage [1]	-0.3V to 6V
VIOC Pin Current	-1mA to 1mA
IMON Pin Voltage [1]	-0.3V to 6V
TEMP Pin Voltage [1]	-0.3V to 6V
PG Pin Voltage [1]	-0.3V to 6V
REF Pin Voltage [1]	-0.3V to 6V
Output Short Circuit Duration	Indefinite
Operating Junction Temperature [2]	-40°C to 125°C

PARAMETER	RATING
Storage Temperature Range	-65°C to 150°C
Maximum Reflow (Package Body) Temperature	260°C

[1] Parasitic diodes exist internally between IN, OUT, SENSE, BIAS, BIASF, V_{O0}, V_{O1}, V_{O2}, MARG, EN, VIOC, TEMP, IMON, PG, REF pins, and GND. Do not drive these pins more than 0.3V below the GND pin during a fault condition. These pins must remain at a voltage more positive than GND during normal operation.

[2] The LT3073A is tested and specified under pulse load conditions such that $T_J \approx T_A$ (ambient temperature). The LT3073A is tested at $T_A = 25°C$. Performance of the LT3073A over the full –40°C to 125°C operating temperature range is assured by design, characterization, and correlation with statistical process controls. The LT3073A is guaranteed over the full –40°C to 125°C operating junction temperature range.

Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

Thermal Resistance

Thermal performance is directly linked to PCB design and operating environment. Therefore, close attention to PCB thermal design is required.

Table 3. Thermal Resistance

PACKAGE TYPE[1]	θ_{JA}	$\theta_{JC\ TOP}$	$\theta_{JC\ BOT}$	UNIT
22-LEAD 3mm X 4mm LQFN	36	27	5	°C/W

[1]θ values are determined per JESD51 conditions. See *Table 7* for additional information.

Electrostatic Discharge (ESD)

The following ESD information is provided for handling of ESD-sensitive devices in an ESD protected area only. Human Body Model (HBM) per ANSI/ESDA/JEDEC JS-001 Charged Device Model (CDM) per ANSI/ESDA/JEDEC JS-002.

ESD Ratings

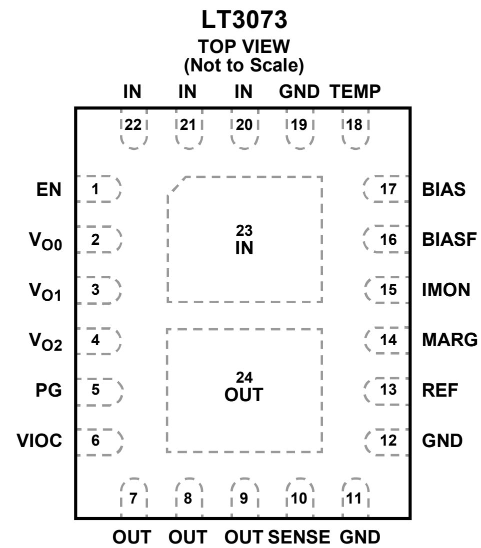
Table 4. LT3073, 22-Lead 3mm X 4mm LQFN

ESD Model	Withstand Threshold (V)	Class
HBM	2500	2
CDM	1250	C5

ESD Caution

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS



NOTES
1. EXPOSED PAD. SOLDER PINS 23 AND 24 TO THE PCB FOR BETTER THERMAL PERFORMANCE.

LQFN PACKAGE
22-LEAD (3mm × 4mm × 0.95mm)
T_{JMAX} = 125°C, θ_{JA} = 38°C/W, θ_{JCBOT} = 5°C/W, θJ_{CTOP} = 50°C/W

003

Figure 3. Pin Configuration

Table 5. Pin Descriptions

PIN	NAME	DESCRIPTION
1	EN	Device Enable. EN pin enables/disables the output. The LT3073 typically turns on when the EN voltage exceeds 1.26V on its rising edge, with an 80mV hysteresis on its falling edge. Pulling this pin low pulls down the reference, disables the output transistor, and disables auxiliary functions. Alternatively, the EN pin can set a Bias-supply UVLO threshold by using a resistor-divider between Bias, EN and GND. If unused, connect EN to Bias. Do not float the EN pin.
2, 3, 4	V_{O0}, V_{O1}, V_{O2}	Output Voltage Select. These tri-level pins combine to select a nominal output voltage from 0.5V to 4.2V. The input logic low threshold is less than 300mV referenced to GND, and the logic high threshold is greater than 1.97V referenced to GND. The range between 0.95V and 1.15V defines the logic Hi-Z state. See *Table 6* in the *Applications Information* section that defines the V_{OUT} versus V_{O0}, V_{O1}, and V_{O2} settings.
5	PG	Power Good. The PG pin is an open-drain NMOS output that actively pulls low if EN is low or if any one of these fault modes is detected: ▶ V_{OUT} is less than 93% of $V_{OUT(NOMINAL)}$ on the rising edge of V_{OUT}. ▶ V_{OUT} is less than 90% of $V_{OUT(NOMINAL)}$ on the falling edge of V_{OUT}. ▶ V_{BIAS} is less than its undervoltage lockout threshold. ▶ The OUT-over-IN voltage detector activates.
6	VIOC	Voltage for In-to-Out Control. The LT3073 incorporates a unique tracking feature (VIOC) to control the upstream switching regulator to maintain a constant voltage across the LT3073 and minimize power dissipation. See the *Applications Information* section for more information on proper control of the upstream switching regulator.
7, 8, 9, Exposed Pad 24	OUT	Output. Pins 7-9 and exposed pad 24 of the LQFN package are the electrical connection to OUT. These pins supply power to the load. Connect all OUT pins for proper performance and solder Pin 24 to the PCB for better thermal performance. A minimum output capacitance of 10μF is required for stability. ADI recommends low ESR, X5R or X7R dielectric ceramic capacitors for best performance. Large load transient applications require larger output capacitors to limit peak voltage transients.
10	SENSE	Kelvin Sense for OUT. The SENSE pin is the inverting input to the error amplifier. Optimum regulation is obtained when the SENSE pin is connected to the OUT pins of the regulator. However, in critical applications, the resistance of PCB traces between the regulator and the load causes small voltage drops, creating a load regulation error at the point of load. Connecting the SENSE pin to the load instead of directly to OUT eliminates this voltage error.
11, 12, 19	GND	Ground. To ensure proper electrical and thermal performance, connect all GND pins of the package to the PCB ground.
13	REF	Reference Filter. Bypassing the REF pin to GND with a 4.7μF capacitor decreases output voltage noise and provides a soft-start function to the reference. ADI recommends the use of a high-quality, low-leakage capacitor.

14	MARG	Output Voltage Digital Margining. Connecting this pin to GND adjusts the output voltage by -2.5%. Connecting this pin to V_{BIAS} adjusts the output voltage by +2.5%. Floating the MARG pin (Hi-Z state) sets nominal output voltage.
15	IMON	Output Current Monitor. The IMON pin sources a current typically equal to I_{OUT}/3000. Terminating this pin with a resistor to GND produces a voltage proportional to I_{OUT}. For example, at I_{OUT} = 3A, IMON typically sources 1mA. 0.8V is produced with a 0.8kΩ resistor to GND. The IMON pin can also be used to set the programmable current limit. IMON pin's current limit threshold is 1V.
16	BIASF	Bias Filter Pin. The LT3073 requires a minimum 2.2µF bypass capacitor on this pin.
17	BIAS	Bias Supply. This pin supplies current to the internal control circuitry and the output stage, driving the pass transistor. This pin doesn't require any bypass capacitor. To ensure proper operation, the BIAS voltage must satisfy the following conditions: 2.375V ≤ V_{BIAS} ≤ 5.5V and V_{BIAS} ≥ 1.2 + V_{OUT}.
18	TEMP	Output indicator of average die temperature scaled at 10mV/°C to a reference level of 0.25V at 25°C. The TEMP output is active when the part is enabled.
20, 21, 22, Exposed Pad 23	IN	Input Supply. Pins 20-22 and exposed pad 23 of the LQFN package are the electrical connection to IN. These pins supply power to the high-current pass transistor. Connect all IN pins for proper performance and solder Pin 23 to the PCB for better thermal performance. The LT3073 requires a bypass capacitor at IN to maintain stability and low input impedance over frequency. A 10µF input bypass capacitor suffices for most battery and power plane impedances. Minimizing input trace inductance optimizes performance. Applications with low V_{IN}-V_{OUT} differential voltage and large, fast load transients may require much higher input capacitor to prevent the input supply from drooping and allow the regulator to enter dropout.

TYPICAL PERFORMANCE CHARACTERISTICS

T_J = 25°C unless noted otherwise.

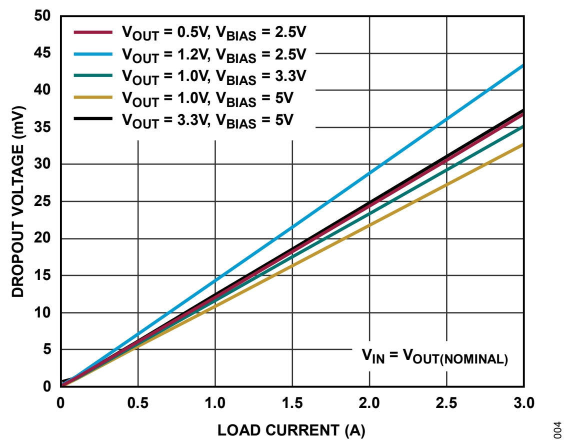


Figure 4. Dropout Voltage vs Load

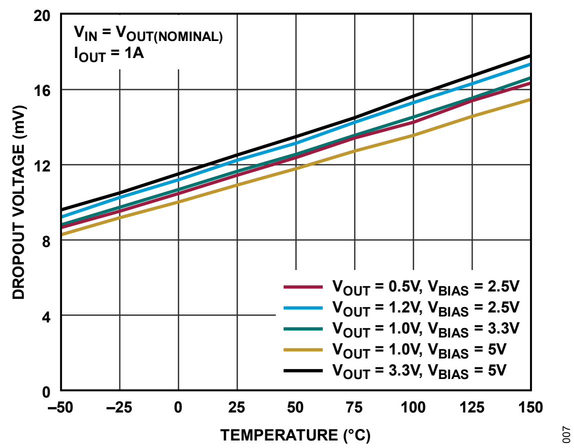


Figure 7. Dropout Voltage (1A)

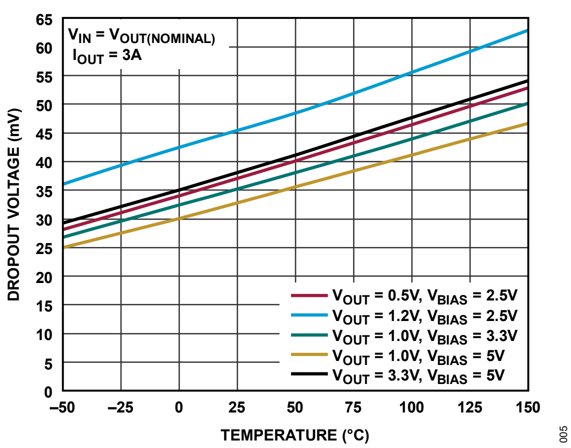


Figure 5. Dropout Voltage (3A)

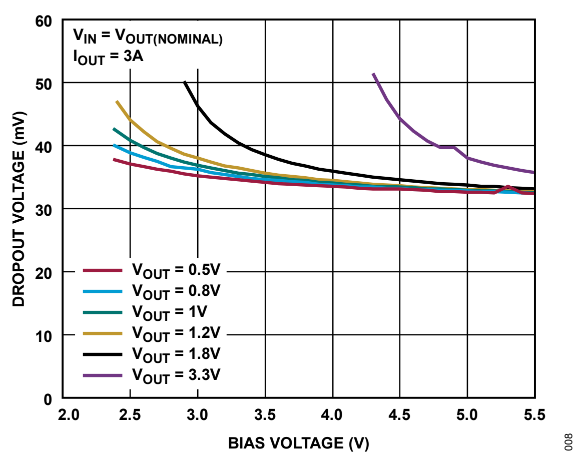


Figure 8. Dropout Voltage vs V_{BIAS}

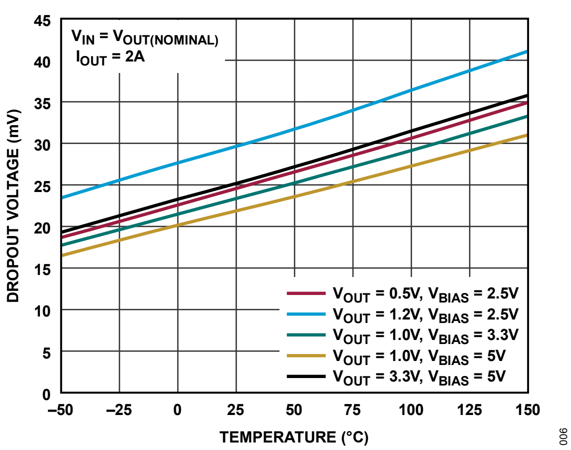


Figure 6. Dropout Voltage (2A)

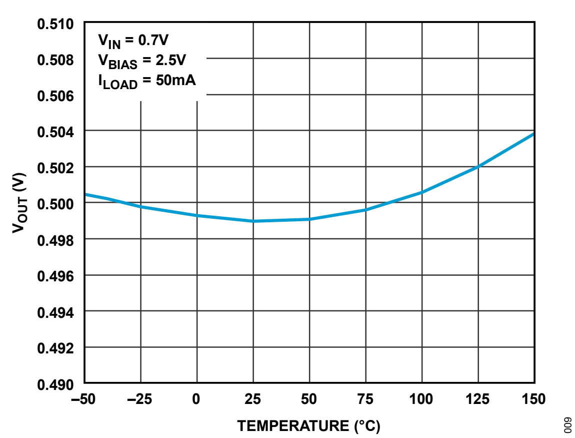


Figure 9. Output Voltage

TYPICAL PERFORMANCE CHARACTERISTICS

T_J = 25°C unless noted otherwise.

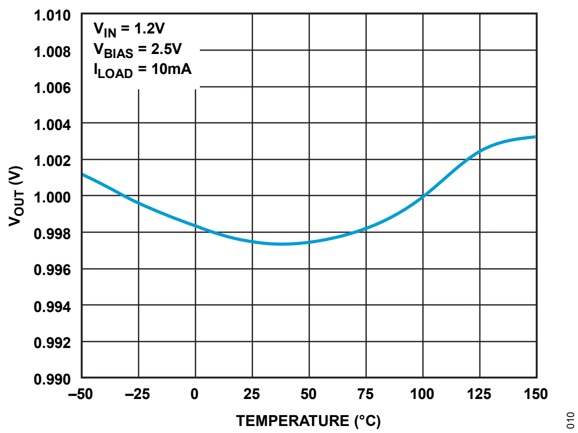


Figure 10. Output Voltage

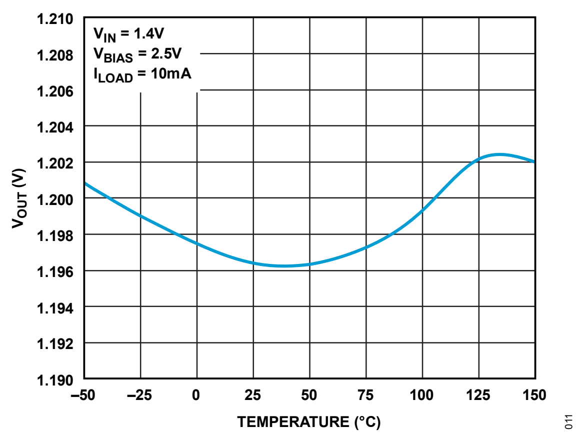


Figure 11. Output Voltage

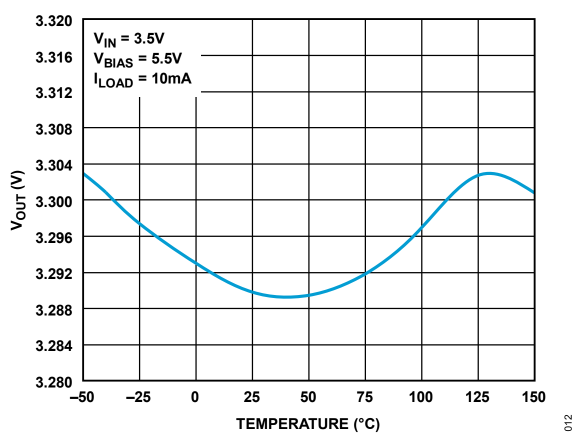


Figure 12. Output Voltage

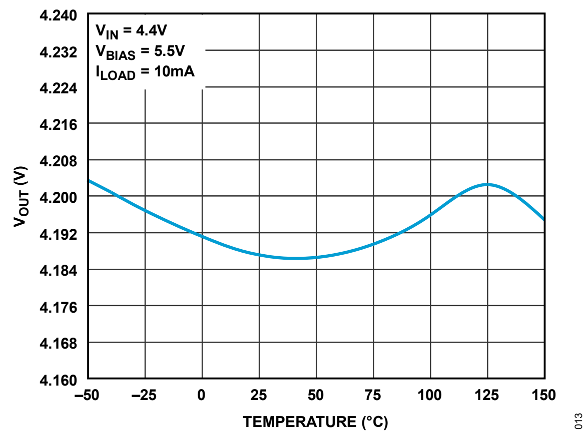


Figure 13. Output Voltage

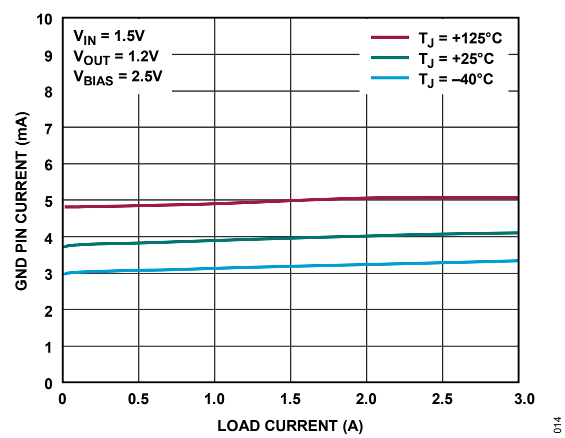


Figure 14. GND Pin Current

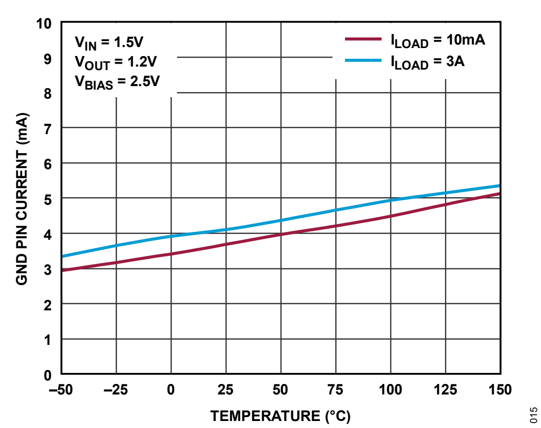


Figure 15. GND Pin Current

TYPICAL PERFORMANCE CHARACTERISTICS

T_J = 25°C unless noted otherwise.

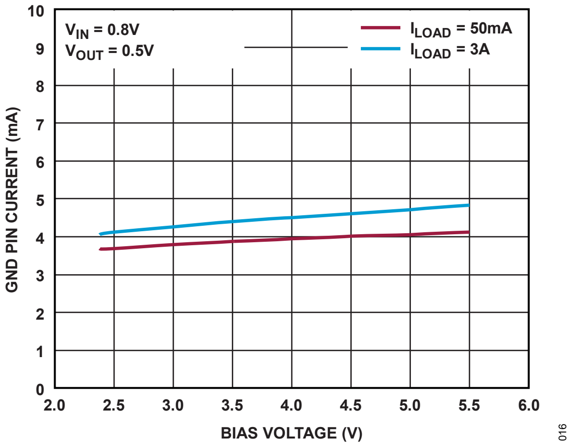


Figure 16. GND Pin Current

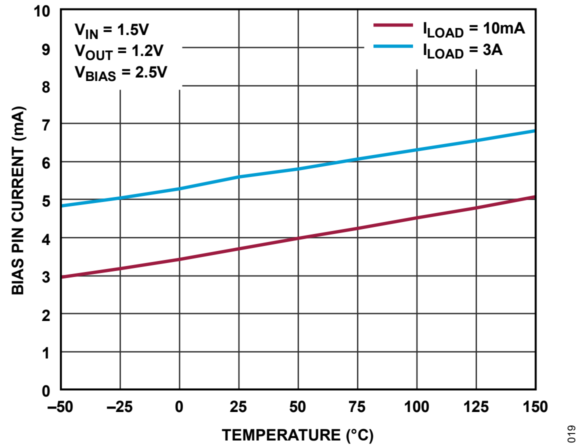


Figure 19. BIAS Pin Current

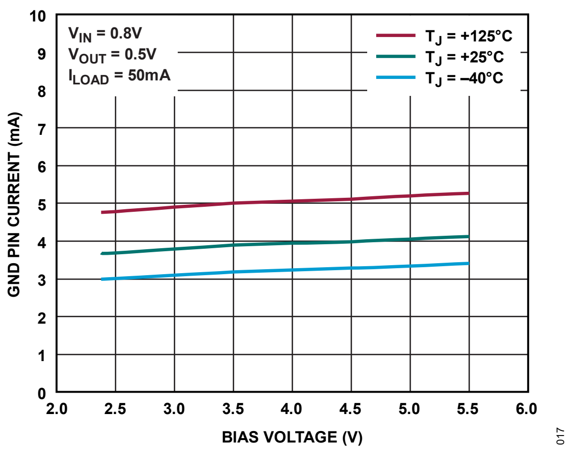


Figure 17. GND Pin Current

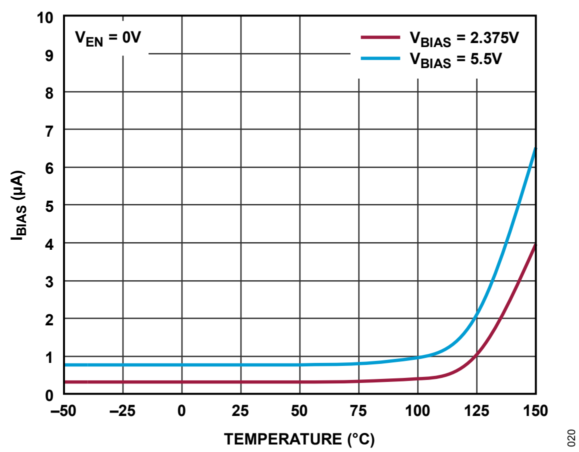


Figure 20. BIAS Pin Current in Nap Mode

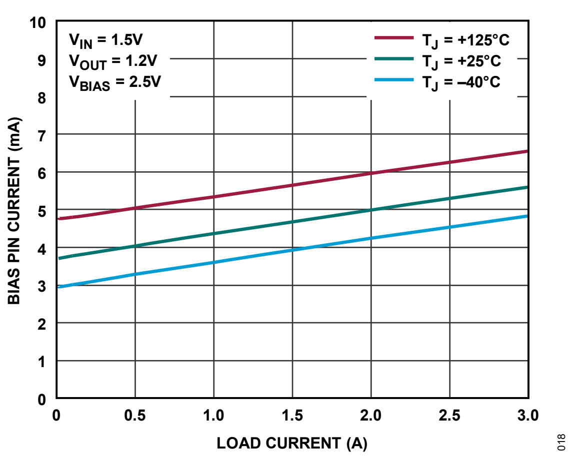


Figure 18. BIAS Pin Current

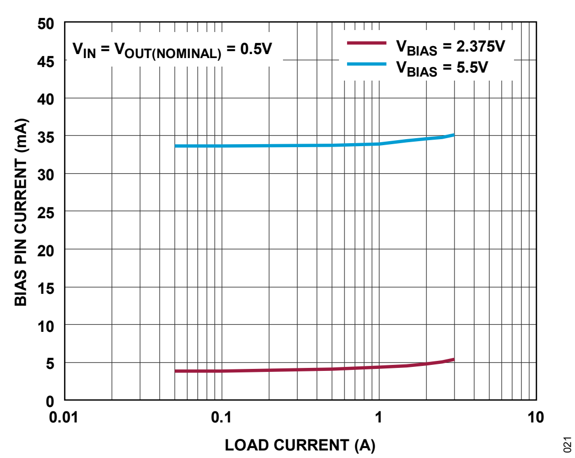


Figure 21. BIAS Pin Current in Dropout

TYPICAL PERFORMANCE CHARACTERISTICS

T_J = 25°C unless noted otherwise.

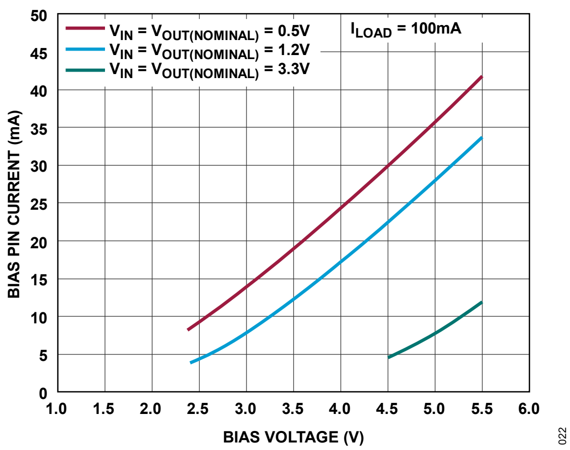


Figure 22. BIAS Pin Current in Dropout

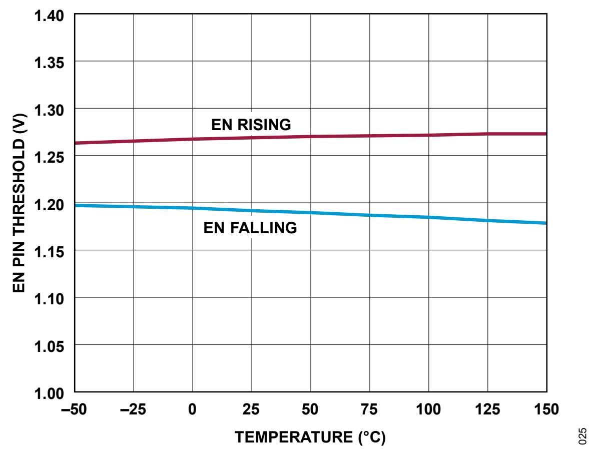


Figure 25. EN Pin Threshold

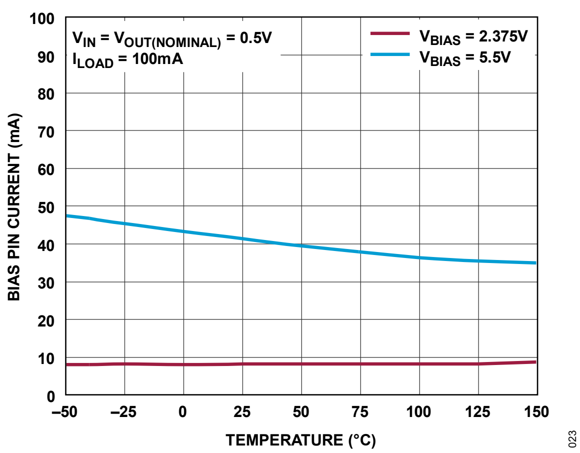


Figure 23. BIAS Pin Current in Dropout

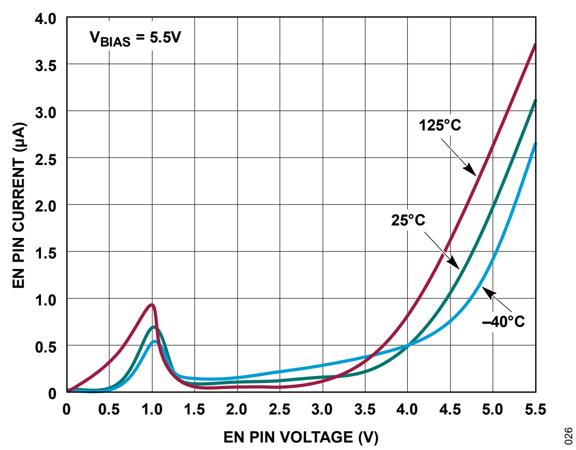


Figure 26. EN Pin Current

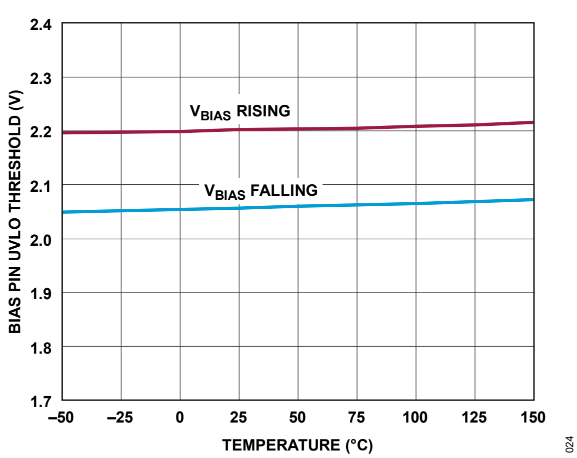


Figure 24. BIAS Pin Undervoltage Lockout Threshold

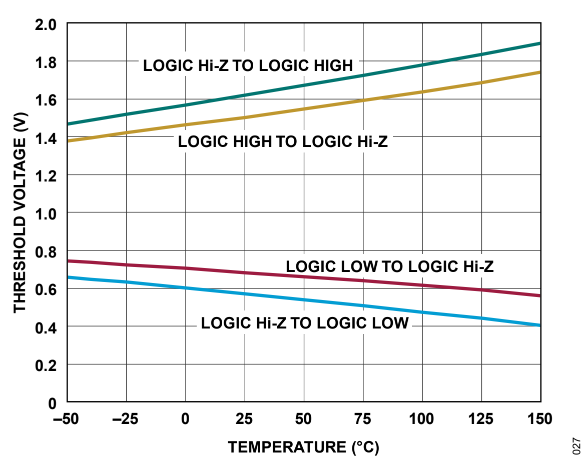


Figure 27. V_{O0}, V_{O1}, V_{O2} and MARG Pin Thresholds

TYPICAL PERFORMANCE CHARACTERISTICS

T_J = 25°C unless noted otherwise.

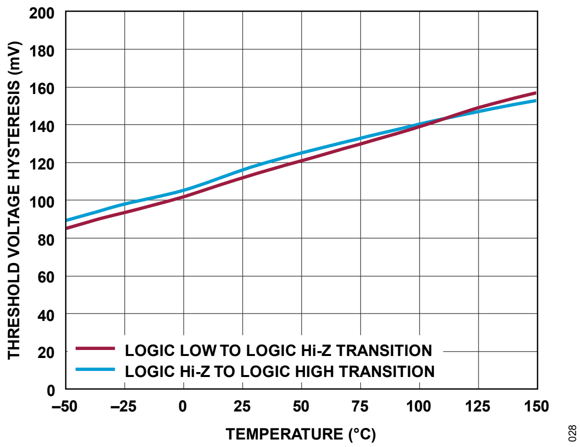


Figure 28. V_{O0}, V_{O1}, V_{O2} and MARG Pin Hysteresis

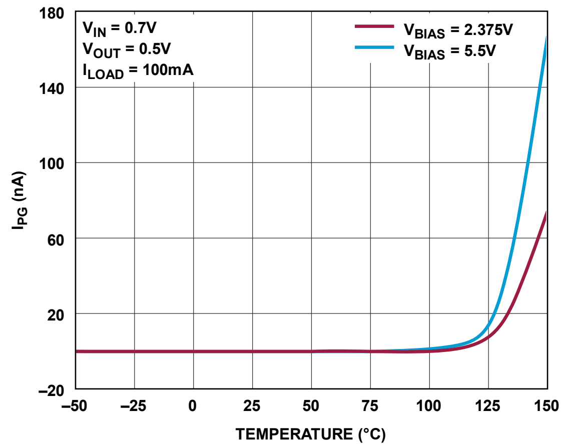


Figure 31. PG Pin Leakage Current

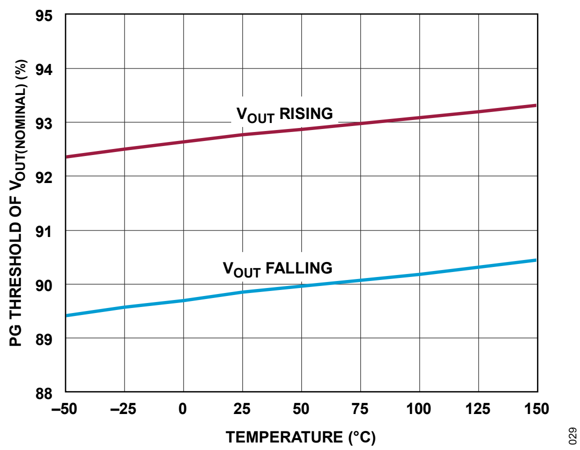


Figure 29. Power Good Threshold

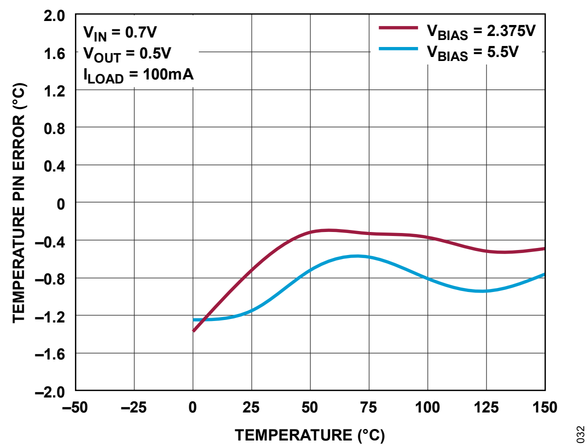


Figure 32. TEMP Pin Error

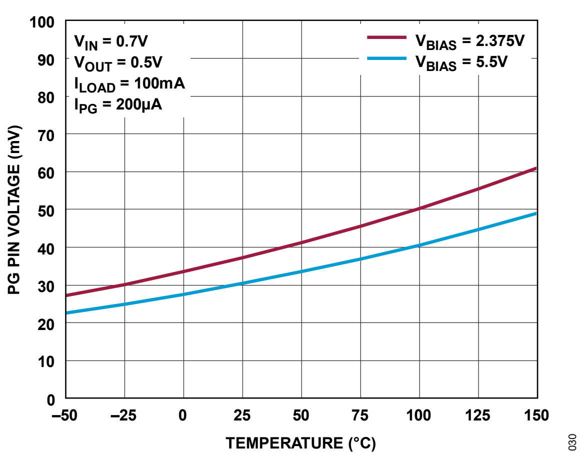


Figure 30. PG Pin Low Voltage

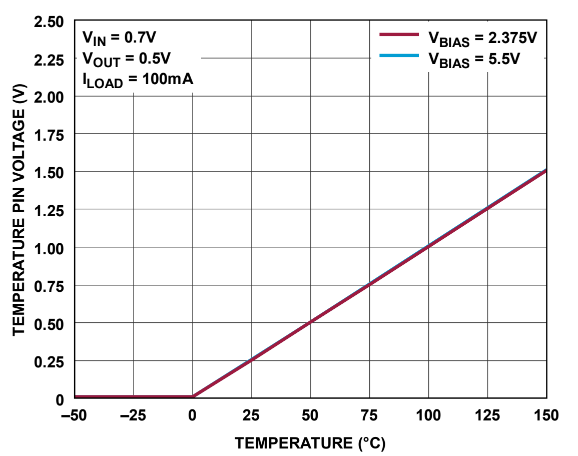


Figure 33. TEMP Pin Voltage vs Temperature

TYPICAL PERFORMANCE CHARACTERISTICS

T_J = 25°C unless noted otherwise.

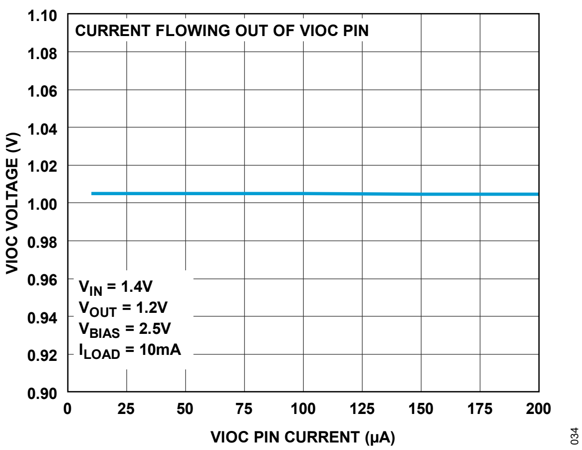


Figure 34. VIOC Pin Voltage

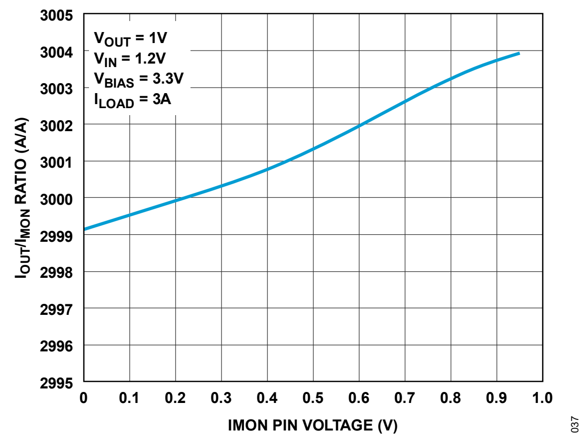


Figure 37. I_{OUT}/I_{MON} Ratio

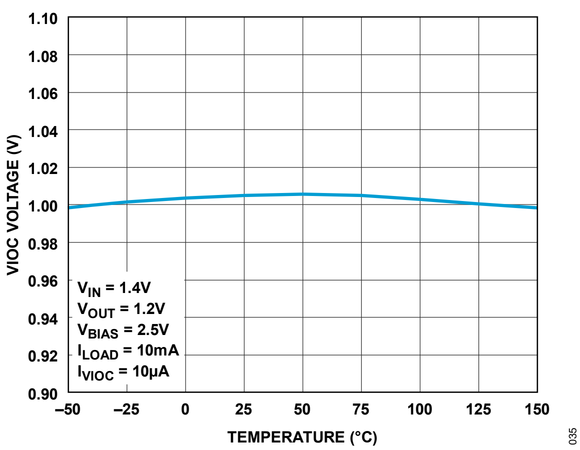


Figure 35. VIOC Pin Voltage

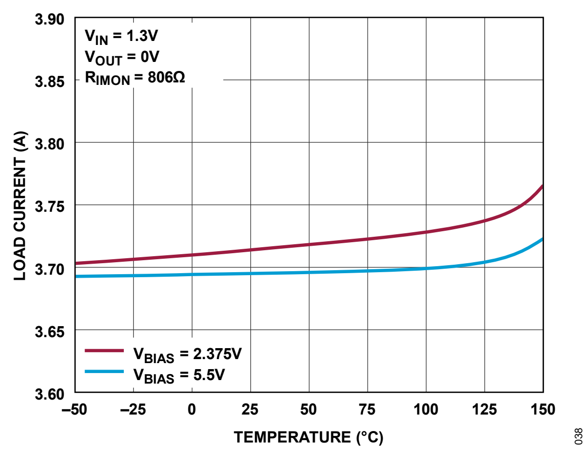


Figure 38. External Current Limit (3.72A)

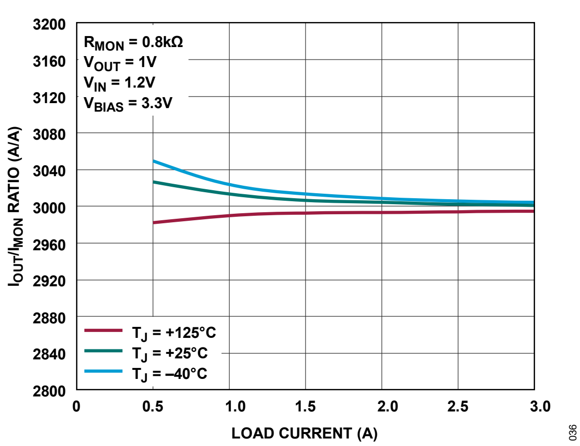


Figure 36. I_{OUT}/I_{MON} Ratio

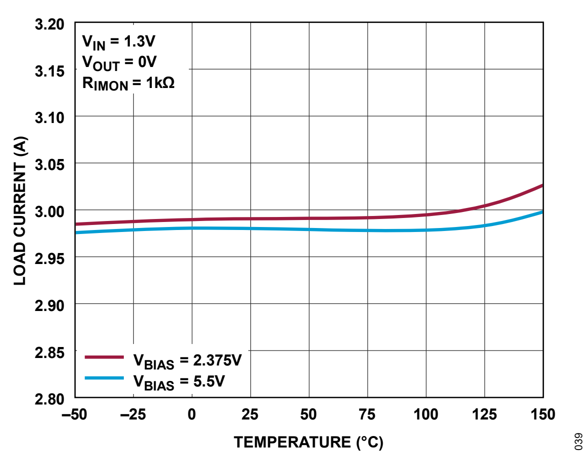


Figure 39. External Current Limit (3A)

TYPICAL PERFORMANCE CHARACTERISTICS

T_J = 25°C unless noted otherwise.

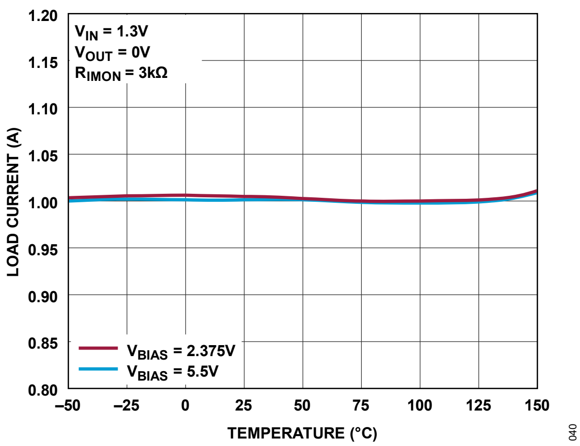


Figure 40. External Current Limit (1A)

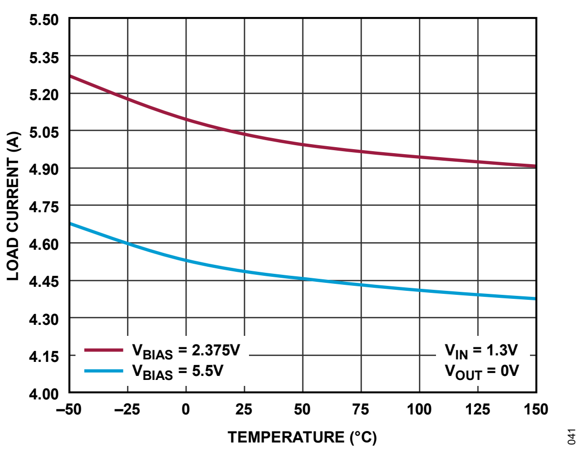


Figure 41. Internal Current Limit

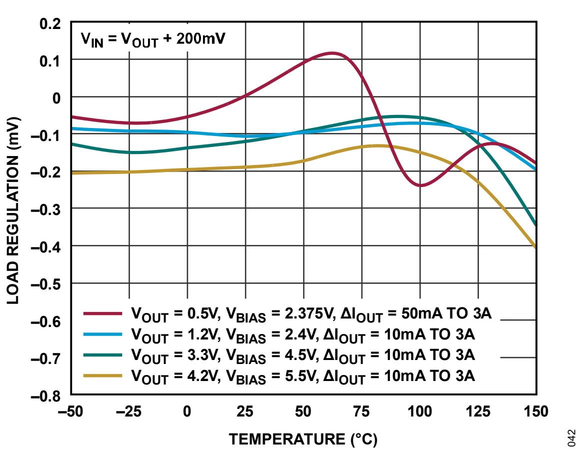


Figure 42. Load Regulation

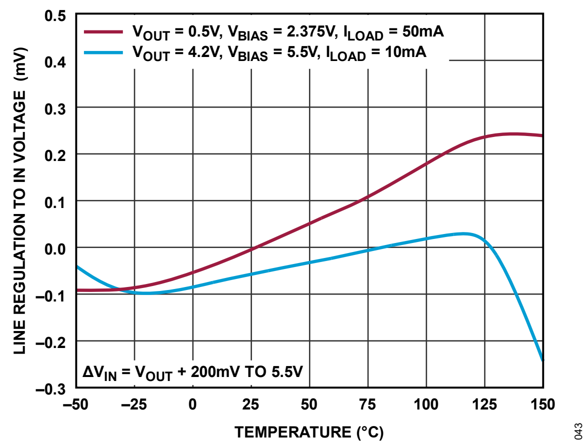


Figure 43. Line Regulation to IN

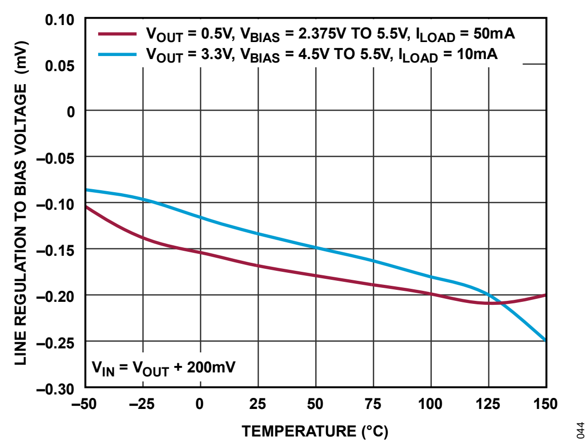


Figure 44. Line Regulation to BIAS

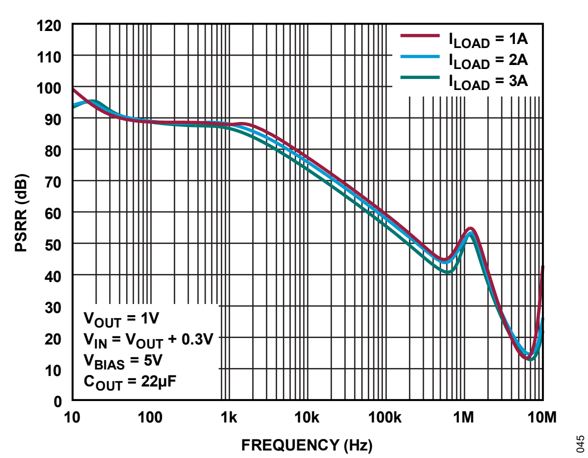


Figure 45. IN Pin PSRR

TYPICAL PERFORMANCE CHARACTERISTICS

T_J = 25°C unless noted otherwise.

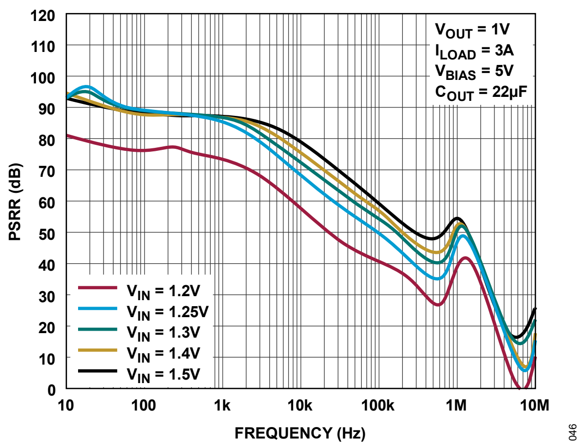


Figure 46. IN Pin PSRR

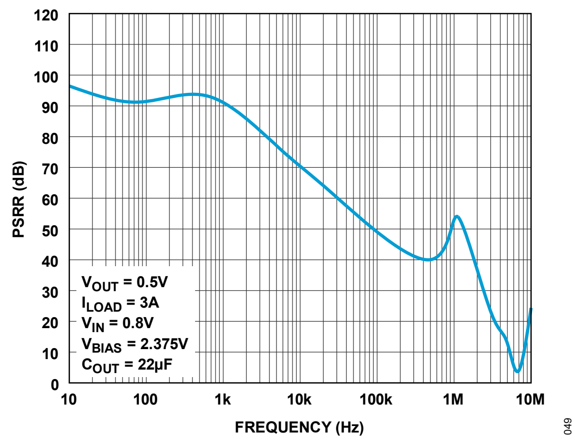


Figure 49. IN Pin PSRR

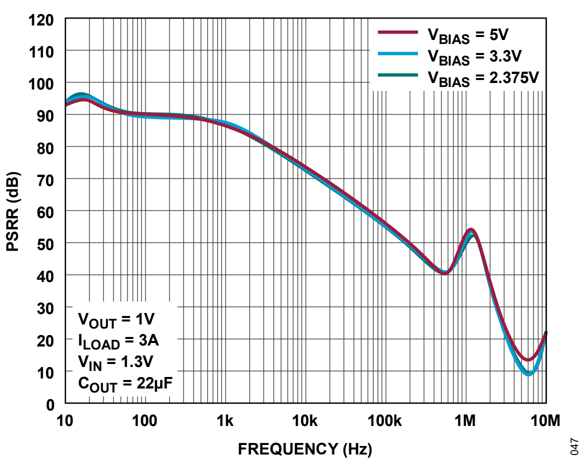


Figure 47. IN Pin PSRR

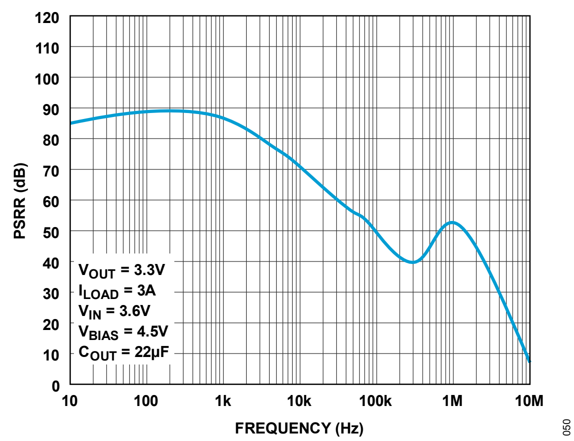


Figure 50. IN Pin PSRR

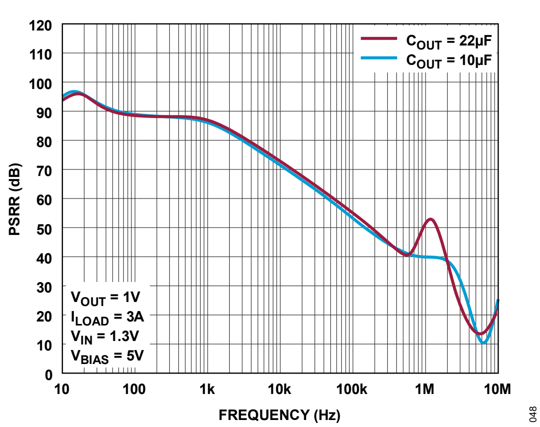


Figure 48. IN Pin PSRR

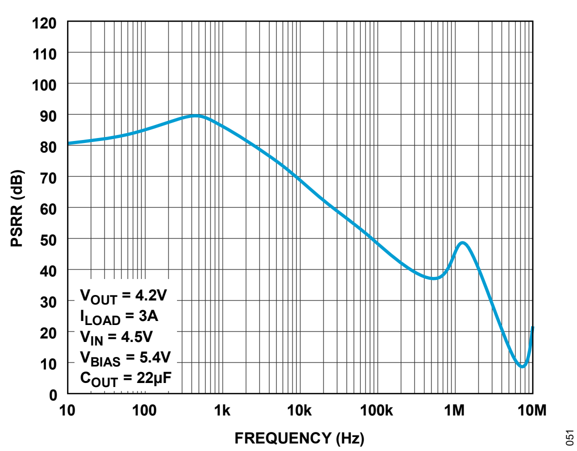


Figure 51. IN Pin PSRR

TYPICAL PERFORMANCE CHARACTERISTICS

T_J = 25°C unless noted otherwise.

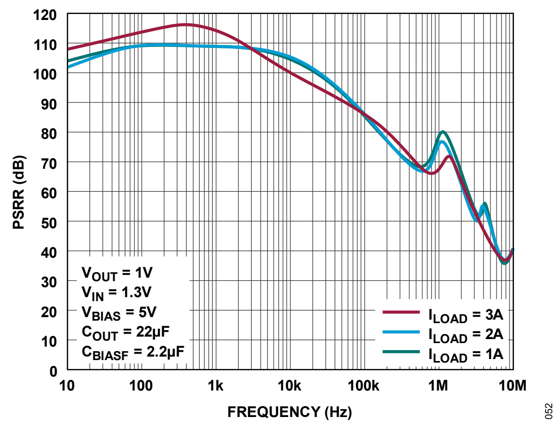


Figure 52. BIAS Pin PSRR

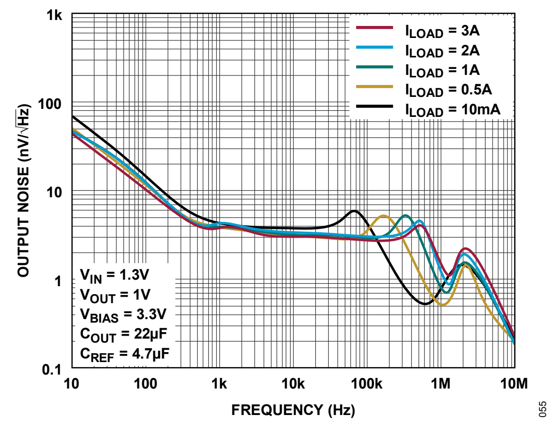


Figure 55. Noise Spectral Density

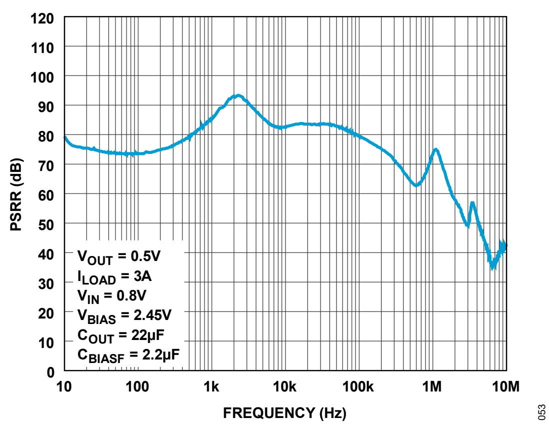


Figure 53. BIAS Pin PSRR

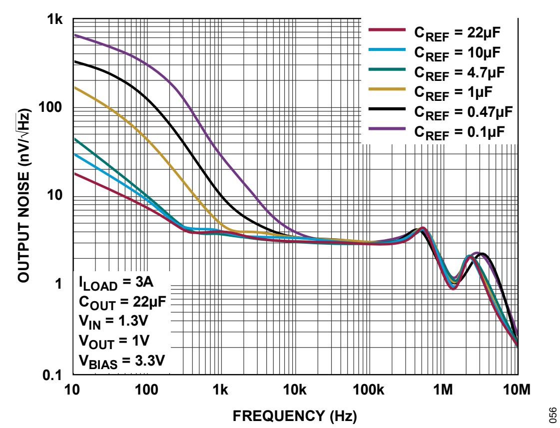


Figure 56. Noise Spectral Density

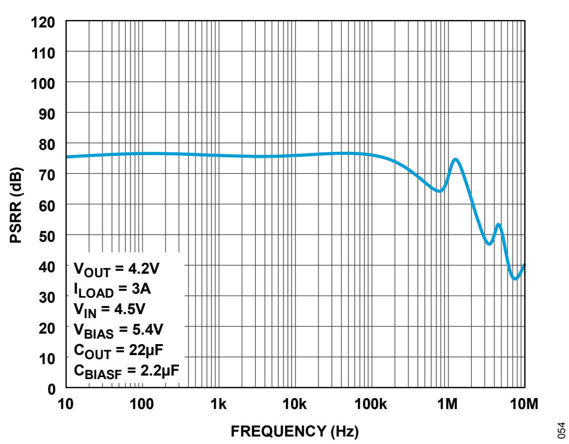


Figure 54. BIAS Pin PSRR

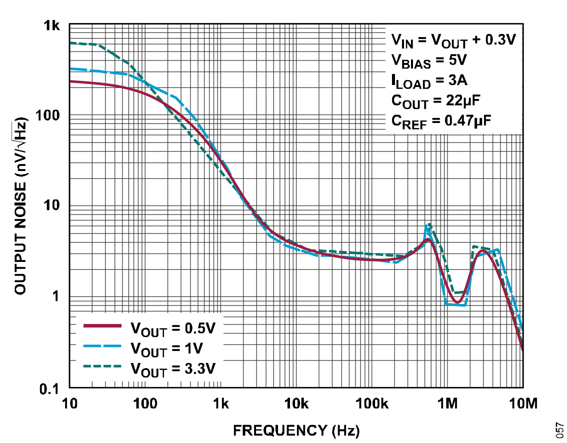


Figure 57. Noise Spectral Density

TYPICAL PERFORMANCE CHARACTERISTICS

T_J = 25°C unless noted otherwise.

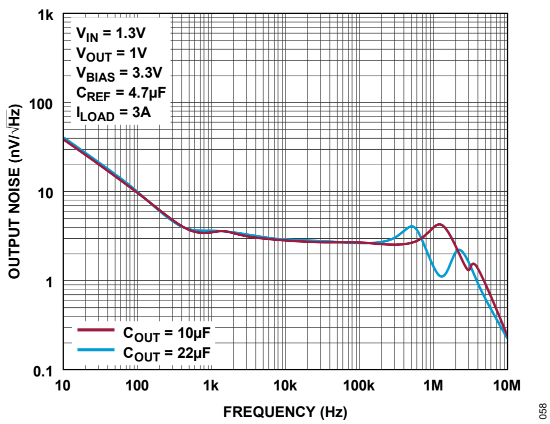


Figure 58. Noise Spectral Density

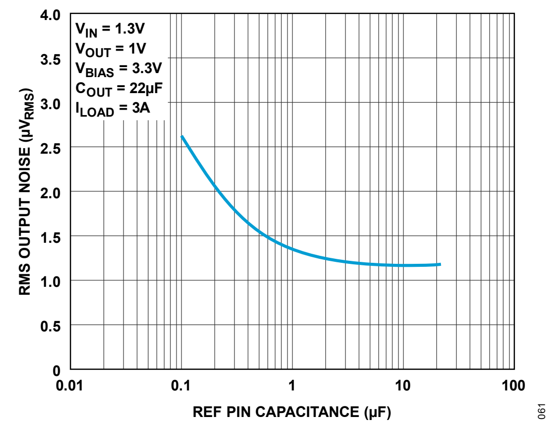


Figure 61. Integrated RMS Output Noise (10Hz to 100kHz)

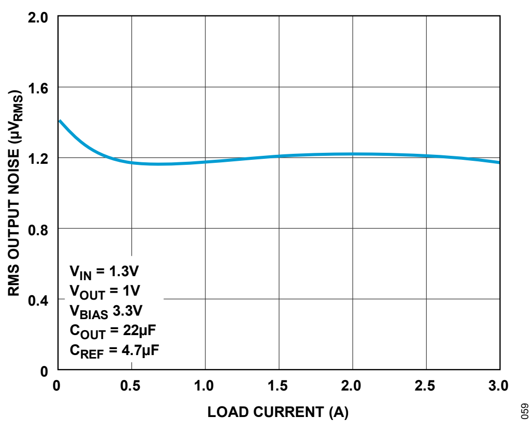


Figure 59. Integrated RMS Output Noise (10Hz to 100kHz)

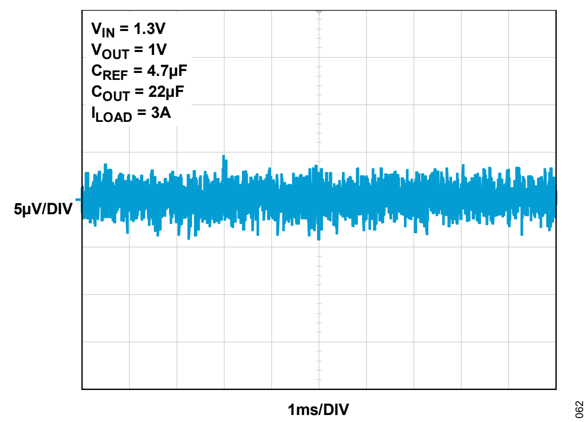


Figure 62. Output Noise (10Hz to 100kHz)

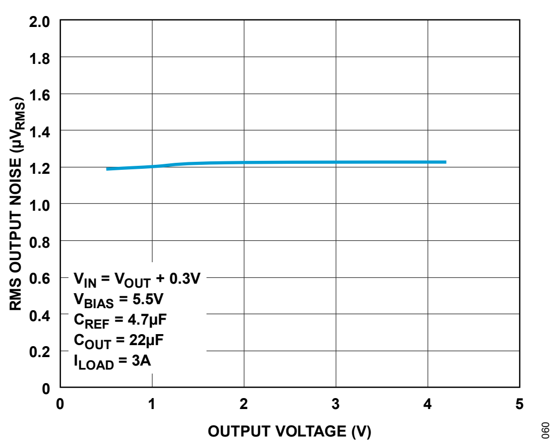


Figure 60. Integrated RMS Output Noise (10Hz to 100kHz)

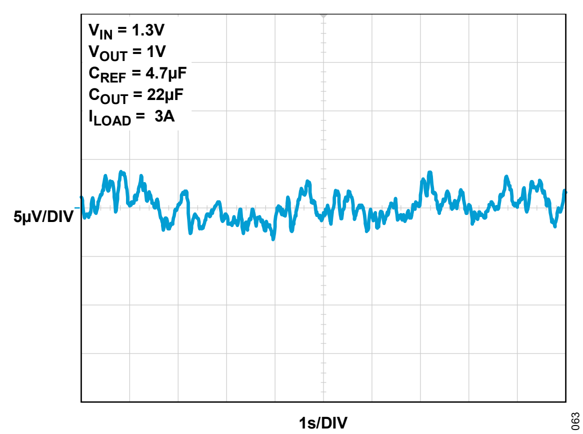


Figure 63. Output Noise (0.1Hz to 10Hz)

TYPICAL PERFORMANCE CHARACTERISTICS

T_J = 25°C unless noted otherwise.

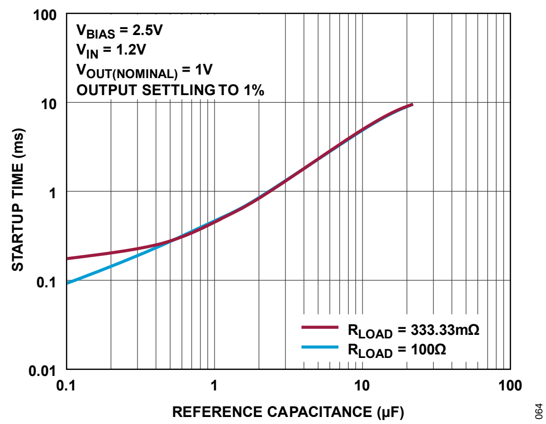


Figure 64. Startup Time

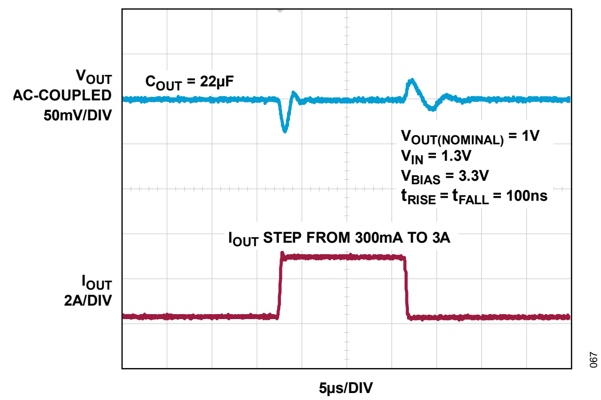


Figure 67. Load Transient

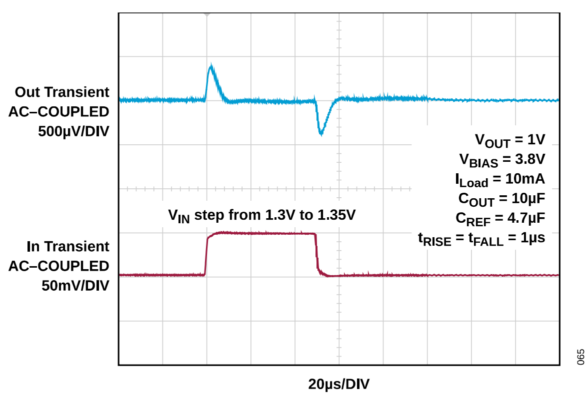


Figure 65. IN Pin Line Transient

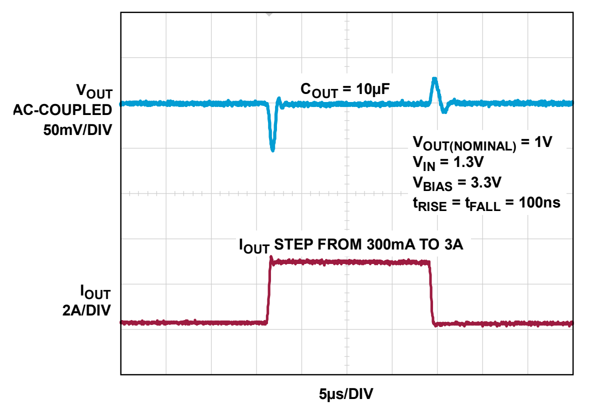


Figure 68. Load Transient

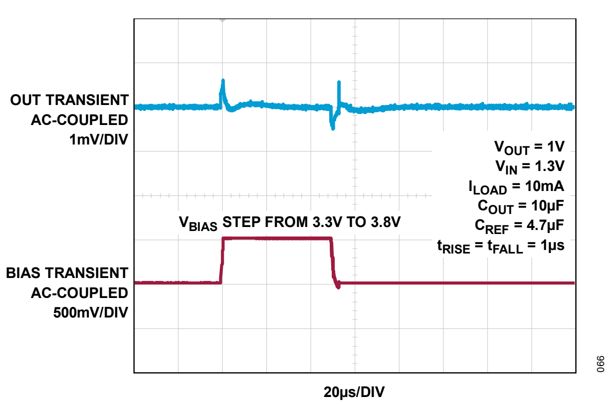


Figure 66. BIAS Pin Line Transient

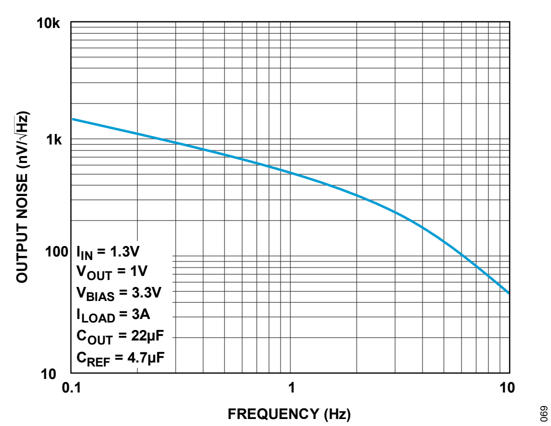
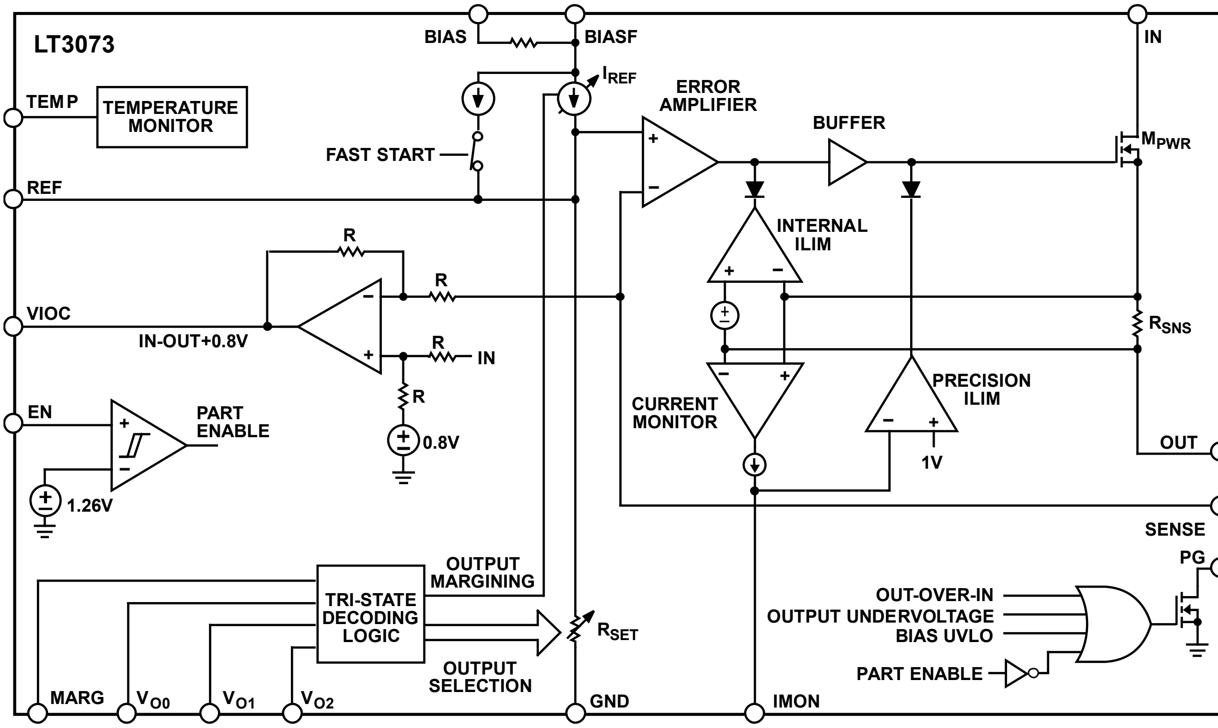
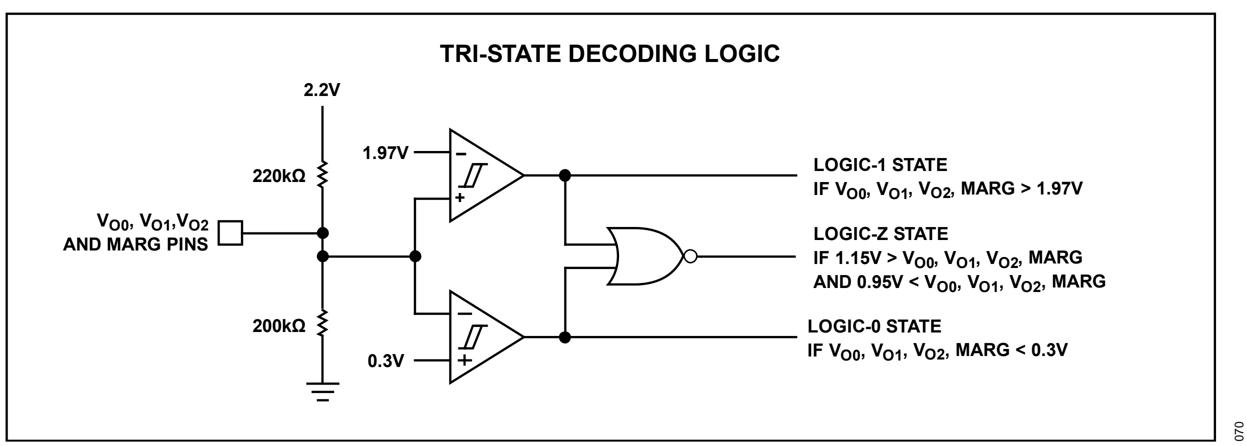


Figure 69. Noise Spectral Density

FUNCTIONAL DIAGRAMS





APPLICATIONS INFORMATION

The LT3073 is a low voltage, ultra-low noise, and ultra-fast transient response linear regulator. The device supplies up to 3A with a typical dropout voltage of 45mV. A 4.7µF reference bypass capacitor decreases output voltage noise to 1.2µV_{RMS}. The LDO's wide bandwidth and high PSRR permit the use of small ceramic capacitors, saving bulk capacitance and cost. The LT3073 is ideal for high-performance FPGAs, microprocessors, RF communication, and noise-sensitive supply applications.

Output Voltage

The LT3073's unity-gain operation provides virtually constant output noise, PSRR, bandwidth, and load regulation independent of the programmed output voltage. Output voltages are digitally selectable in 50mV increments from 0.5V to 1.2V; 100mV increments from 1.2V to 1.8V; and discrete levels at 2V, 2.5V, 3V, 3.3V, and 4.2V.

Three tri-level input pins, V_{O0}, V_{O1}, and V_{O2}, select the output voltage. *Table 6* illustrates the three-bit digital word-to-output voltage relationship resulting from setting these pins high, low, or allowing them to float. An input logic low state is guaranteed with less than 300mV referenced to GND, and a logic high state is guaranteed with greater than 1.97V. The range between 950mV to 1.15V defines the logic Hi-Z (input floating) state. These pins may be connected high by strapping them to V_{BIAS} or driving them with digital ports. Pins that float may either float or require logic that has Hi-Z output capability. This allows the output voltage to be dynamically changed if necessary.

Table 6. V_{OUT} Selection Matrix

V_{OUT} (V)	V_{O2}	V_{O1}	V_{O0}
0.50	0	0	0
0.55	0	0	Z
0.60	0	0	1
0.65	0	Z	0
0.70	0	Z	Z
0.75	0	Z	1
0.80	0	1	0
0.85	0	1	Z
0.90	0	1	1
0.95	Z	0	0
1.00	Z	0	Z
1.05	Z	0	1
1.10	Z	Z	0
1.15	Z	Z	Z
1.20	Z	Z	1
1.30	Z	1	0
1.40	Z	1	Z
1.50	Z	1	1
1.60	1	0	0
1.70	1	0	Z
1.80	1	0	1
2.00	1	Z	0
2.50	1	Z	Z
3.00	1	Z	1
3.30	1	1	0
4.20	1	1	Z
4.20	1	1	1

0 = Low, Z = Hi-Z (Float), 1 = High

REF – Voltage Reference

The REF pin is the voltage output of the internal current reference feeding into a resistor DAC. A 4.7µF REF capacitor to GND decreases reference voltage noise, and soft starts OUT at enable. Soft-start time is determined by the value of the REF capacitor used.

For applications that parallel multiple LT3073 regulators for higher output currents, tie the REF pins together. See the *Paralleling Devices for Higher Output Current* section for further details.

Overdriving the REF pin

The REF pin can be overdriven by an external source for applications that need to set the output voltage to a value other than those programmable using the V_{O0}, V_{O1}, and V_{O2} pins. The LT3073 uses a current source with a typical value of 100µA into a resistor DAC. The resistor DAC and the current source are inversely related and may vary up to ±15%, such that the IR product is constant. This variation in the internal current and resistor needs to be accounted for when externally driving the REF pin.

For most applications, choose the V_{OX} pin configuration to select a REF pin voltage lower than the desired overdriven REF voltage to ensure the fast start current is shut off when LT3073 regulates the output. As shown below, the REF can be overdriven directly by an external voltage source (*Figure 70*) or a voltage source followed by a resistor divider (*Figure 71*). In case where the REF pin is driven by an external voltage source followed by a resistor divider, the external voltage source can be a fixed voltage source or can be varied using a servo loop to achieve higher accuracy.

When using an external voltage source with a resistor divider, the resulting REF pin voltage can be calculated using the superposition principle as below.

$$V_{REF} = V_{EXT}\ X \left(\frac{(R_{INT}||R_{EXT2})}{(R_{INT}||R_{EXT2}) + R_{EXT1}}\right) + I_{INT}\ X\ (R_{INT}||R_{EXT1}||R_{EXT2})$$

Where I_{INT} is the internal 100µA current reference, R_{INT} is the nominal resistor value for the corresponding V_{OX} setting, R_{EXT1} and R_{EXT2} are the external resistors forming the resistor divider, and V_{EXT} is the external voltage source overdriving the REF pin.

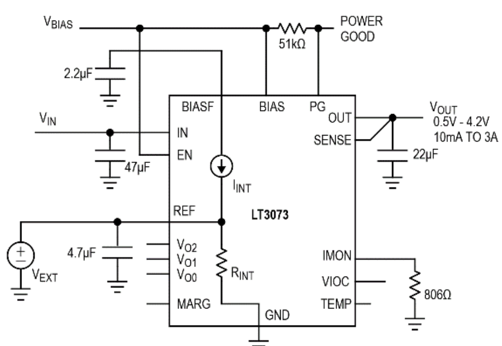


Figure 70. Overdriving REF directly with V_{EXT}

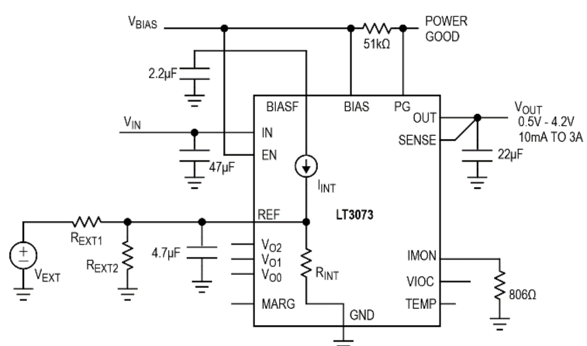


Figure 71. Overdriving REF with resistor divider off V_{EXT}

When using an external voltage source with resistor dividers, choose R_{EXT1} and R_{EXT2} such that the R_{EXT2} value is at most 10% of the nominal R_{INT} value to assure accuracy across process variations in R_{INT}.

Example: Setting REF to be 1.025V with a 1.25V external reference and using resistor dividers.
Set the V_{OX} pins such that LT3073 selects the 1V output setting (V_{O0} and V_{O2} are Hi-Z and V_{O1} is GND).
For a 1V setting, $R_{INT(NOMINAL)}$ = 1V/100µA = 10kΩ.

Select $R_{EXT2} = R_{INT}/10 = 1k\Omega$.
Using these values, the equation is $R_{EXT2} || R_{INT} = 1k\Omega || 10k\Omega = 909.0909\Omega$
Substituting in the above equation for V_{REF}, the equation derived is

$$1.025V = 1.25V\ X\ \left(\frac{909.0909\Omega}{909.0909\Omega + R_{EXT1}}\right) + 100\mu A\ X\ (909.0909\Omega||R_{EXT1})$$

Solving for R_{EXT1} gives $R_{EXT1} = 218.978\Omega$. The closest 1% resistor is 221Ω.

If overdriving the REF pin, the V_{OUT} thresholds for power good mentioned in the Electrical Characteristics table (*Table 1*) can no longer be guaranteed.

Output Voltage Digital Margining

A digital input pin, MARG, is employed by offsetting the internal reference and, likewise the output. Grounding the MARG pin offsets the output by –2.5%. Similarly, pulling the MARG pin up to the BIAS pin offsets the output by +2.5%. Floating the MARG pin (Hi-Z state) sets the nominal output voltage.

Enable Function – Turning ON and OFF

The EN pin enables/disables the reference, disables the output transistor, and disables auxiliary functions. Pulling the EN pin low places the regulator in “nap” mode. In nap mode, the quiescent current decreases to less than 10µA. The LT3073 has an accurate 1.26V turn-on threshold on the EN pin with 80mV of hysteresis. This threshold can be used with a resistor-divider from the bias supply to define an accurate UVLO threshold for the regulator. The EN pin current (I_{EN}) at the threshold from the Electrical Characteristic table (*Table 1*) must be considered when calculating the resistor divider network as follows:

$$V_{BIAS(UVLO)} = 1.26V\ X \left(1 + \frac{R_{EN2}}{R_{EN1}}\right) + I_{EN}\ X\ R_{EN2}$$

Where R_{EN1} and R_{EN2} are the resistors from the EN pin to GND and the EN pin to Bias, respectively. I_{EN} can be ignored if R_{EN1} is less than 100kΩ. If unused, connect the EN pin to Bias.

BIAS Under Voltage Lock Out

An internal under voltage lock out (UVLO) comparator monitors the BIAS rail. If V_{BIAS} drops below the UVLO threshold, all functions shut down, the pass transistors are gated off, and output currents fall to zero. The typical BIAS pin UVLO threshold is 2.2V on the rising edge of V_{BIAS}. The UVLO circuit incorporates about 130mV of hysteresis on the falling edge of V_{BIAS}.

High Efficiency Linear Regulator – Input-to-Output Voltage Control

The VIOC pin controls an upstream switching converter to maintain a constant voltage across the LT3073, regardless of the LDO’s output voltage. This maximizes efficiency while maintaining PSRR performance. The VIOC pin is the output of a fast amplifier and equals to (V_{IN} – V_{OUT}) + 800mV. As shown in *Figure 72*, the VIOC feature is simple to use. In the case of $V_{FB} \geq 1V$, connect the VIOC pin to the upstream switching converter’s feedback (FB) pin. This will regulate the LT3073’s input-to-output differential to the switching converter’s feedback voltage minus 800mV. When paralleling multiple LT3073s, connect the VIOC pin of one of the LT3073 to the upstream switching converter’s feedback pin and float the remaining VIOC pin(s). When LT3073 is turned off, V_{INLDO} is clamped to a voltage set by $V_{FBSWITCHER}$ x (R1 + R2)/R1.

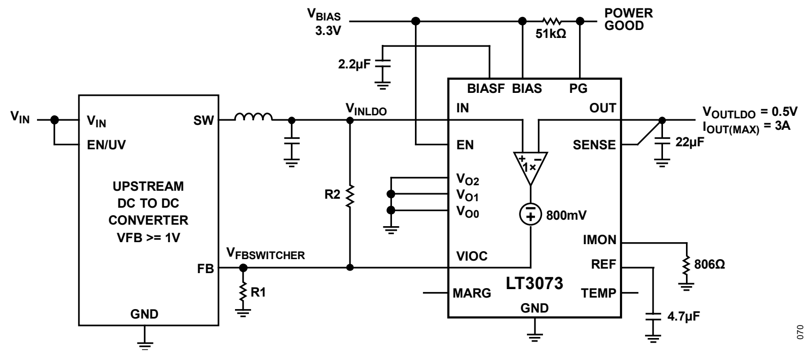


Figure 72. VIOC Basic Operation

While the VIOC buffer is inside the switching converter's feedback loop, given the VIOC buffer's high bandwidth, the switching converter's frequency compensation doesn't need to be adjusted. Phase delay through the VIOC buffer is typically less than 2° for frequencies as high as 100kHz; hence, within the switching converter's bandwidth (usually much less than 100kHz), the VIOC buffer will be transparent and act like an ideal wire.

For example, for a switching converter with less than 100kHz bandwidth and a phase margin of 50°, using the VIOC buffer, the phase margin will degrade by at most 2°. Hence, the phase margin for the switching converter (using the VIOC pin) will be at least 48°. Given that the VIOC buffer is inside the switching converter's feedback loop, the total capacitance on the VIOC pin must be below 20pF.

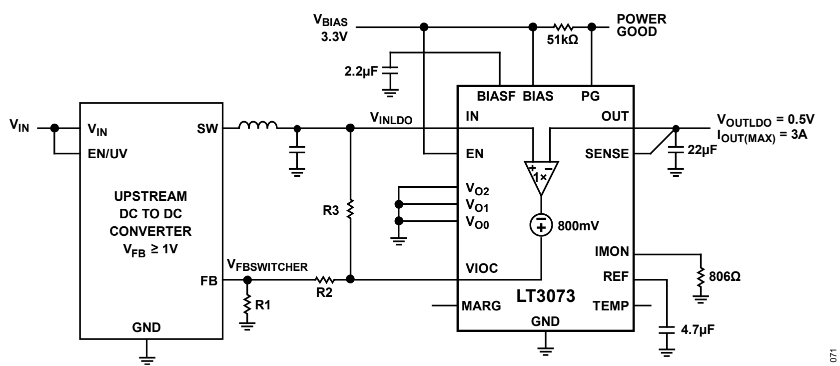


Figure 73. Programming input-to-Output Voltage Differential

As shown in *Figure 73*, the input-to-output differential voltage is easily programmable to support different application needs (PSRR vs power dissipation) using the following equation:

$$V_{INLDO} - V_{OUTLDO} + 800mv = V_{VIOC} = V_{FBSWITCHER} X \frac{R1 + R2}{R1}$$

Furthermore, if the LT3073 EN pin shorts to GND, the LT3073 input voltage can rise to the switcher's input voltage and thus potentially violate the LT3073's absolute maximum rating. To prevent this, the maximum LT3073 input voltage can be set using a resistor (R3) between the VIOC and IN pins of the regulator such that:

$$V_{(MAX)LDOIN} = V_{FBSWITCHER} X \frac{R1 + R2 + R3}{R1}$$

The VIOC pin is capable of sourcing 200µA. Choose R1 and R3 values such that the VIOC pin sources at least 10µA to ensure system stability.

Figure 78 shows a typical VIOC application used to post-regulate the output of the LT8610A buck converter. The VIOC voltage is set at 1.1V (V_{INLDO}-V_{OUTLDO} is set to 300mV). The maximum LDO input voltage $V_{INLDO(MAX)}$ is set to 5.08V.

Power Good

The PG pin is an open-drain NMOS output that actively pulls low if EN is low or if any one of these fault modes is detected:

- V_{OUT} is less than 93% of $V_{OUT(NOMINAL)}$ on the rising edge of V_{OUT}.
- V_{OUT} is less than 90% of $V_{OUT(NOMINAL)}$ on the falling edge of V_{OUT}.
- V_{BIAS} is less than its undervoltage lockout threshold.
- The OUT-over-IN voltage detector activates.

Stability and Output Capacitance

The LT3073 feedback loop requires a minimum output capacitance of 10µF for stability. ADI recommends mounting low ESR, X5R or X7R ceramic capacitors near the LT3073 OUT and GND pins. Include wide routing planes for OUT and GND to minimize inductance. If possible, mount the regulator immediately adjacent to the application load to minimize distributed inductance for optimal load transient performance. Point-of-load applications present the best-case layout scenario for extracting full LT3073 performance.

Additional ceramic capacitors distributed beyond the immediate decoupling capacitors are acceptable and recommended at the point of the load because the distributed PCB inductance isolates them from the primary compensation capacitors.

Many of the applications in which the LT3073 excels, such as FPGA, ASIC processor, or DSP supplies, typically require a high-frequency decoupling capacitor network for the device being powered. This network generally consists of many low-value ceramic capacitors in parallel. In parallel, multiple low-value capacitors present a favorable frequency characteristic that reduces the parasitic inductance of the capacitors.

Consider the use of ceramic capacitors. Ceramic capacitors are manufactured with various dielectrics, each with different temperatures and applied voltage behavior. The most common dielectrics are specified with EIA temperature characteristic codes of Z5U, Y5V, X5R and X7R. The Z5U and Y5V dielectrics are suitable for providing high capacitances in a small package, but they tend to have strong voltage and temperature coefficients, as shown in *Figure 74* and *Figure 75*. When used with a 5V regulator, a 16V 10µF Y5V capacitor can exhibit an effective value as low as 1µF to 2µF for the DC bias voltage applied and over the operating temperature range. The X5R and X7R dielectrics result in more stable characteristics and are more suitable for use as the output capacitor.

The X7R type has better stability across temperatures, while the X5R is less expensive and is available in higher values. Care still must be exercised when using X5R and X7R capacitors; the X5R and X7R codes only specify the operating temperature range and maximum capacitance change over temperature. Capacitance change due to DC bias with X5R and X7R capacitors is better than Y5V and Z5U capacitors but can still be significant enough to drop capacitor values below appropriate levels. Capacitor DC bias characteristics tend to improve as component case size increases but expected capacitance at operating voltage should be verified. Voltage and temperature coefficients are not the only sources of problems. Some ceramic capacitors have a piezoelectric response. A piezoelectric device generates a voltage across its terminals due to mechanical stress, similar to how a piezoelectric microphone works. For a ceramic capacitor, the stress can be induced by vibrations in the system or thermal transients.

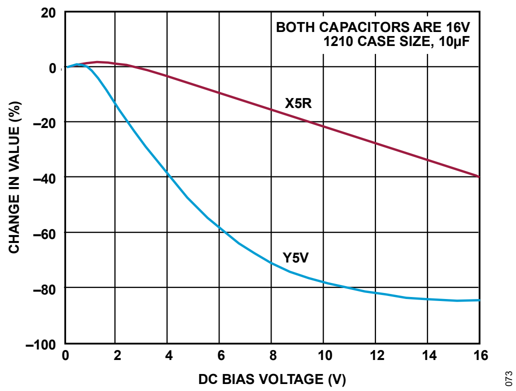


Figure 74. Ceramic Capacitor DC Bias Characteristics

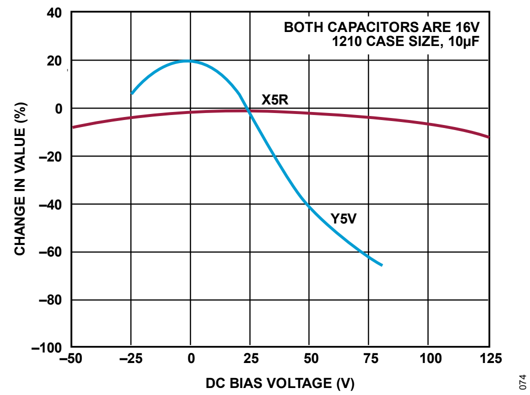


Figure 75. Ceramic Capacitor Temperature Characteristics

Stability and Input Capacitance

The LT3073 is stable with a minimum capacitance of 4.7µF connected to the IN pins. Use low ESR capacitors to minimize instantaneous voltage drops under large-load transient conditions. Large V_{IN} droops during large-load transients may cause the regulator to enter dropout with the corresponding degradation in load transient response. Therefore, increased input and output capacitance values may be necessary depending on an application's requirements. Sufficient input capacitance is critical as the circuit is intentionally operated close to dropout to minimize power. Ideally, the output impedance of the supply that powers IN should be less than 20mΩ to support a 3A load with large transients.

In cases where a wire is used to connect a power supply to the input of the LT3073 (and also from the ground of the LT3073 back to the power supply ground), large input capacitors are required to avoid an unstable application. This is due to the inductance of the wire forming an LC tank circuit with the input capacitor and not a result of the LT3073 being unstable. A wire's self-inductance, or isolated inductance, is directly proportional to its length. However, the diameter of a wire does not have a significant influence on its self-inductance. For example, one inch of 18-AWG, 0.04 inch diameter wire has 28nH of self-inductance. The self-inductance of a 2-AWG isolated wire with a diameter of 0.26 inch is about half the inductance of the 18-AWG wire. The overall self-inductance of a wire can be reduced in two ways. One is to divide the current flowing toward the LT3073 between two parallel conductors. In this case, the farther the wires are placed apart, the more the inductance is reduced, up to a 50% reduction when set a few inches apart. Splitting the wires connects two equal inductors in parallel. However, when placed near each other, mutual inductance is added to the overall self-inductance of the wires. The most effective way to reduce overall inductance is to place the forward and return-current conductors (the wire for the input and the wire for the return ground) in very close proximity. In this case, two 18-AWG wires separated by 0.05 inches reduce the overall self-inductance to about one-fourth of a single isolated wire. If the LT3073 is powered by a battery mounted near the ground and power planes on the same circuit board, a 10µF input capacitor is sufficient for stability. If a distant supply powers the LT3073, use a low ESR, large value input capacitor on the order of 220µF. As power supply output impedance varies, the minimum input capacitance needed for application stability also varies.

BIAS/BIASF Pin Requirements

The BIAS pin supplies current to most of the internal control circuitry and the output stage, driving the pass transistor. The LT3073 requires a minimum 2.2µF bypass capacitor on the BIASF pin for stability and proper operation. No bypass capacitor is needed on the BIAS pin. To ensure proper operation, the BIAS voltage must satisfy the following conditions: $2.375V \le V_{BIAS} \le 5.5V$ and $V_{BIAS} \ge (V_{OUT} + 1.2V)$. For $V_{OUT} \le 1.15V$, the minimum BIAS voltage is limited to 2.375V.

Load Regulation

The LT3073 corrects for a parasitic package, and PCB I-R drops when the SENSE pin is Kelvin connected to output capacitors. The LT3073 handles moderate levels of output line impedance, but excessive impedance between V_{OUT} and C_{OUT} causes an excessive phase shift in the feedback loop and adversely affects stability.

PCB Layout Considerations

Given the LT3073's high bandwidth and high PSRR, careful PCB layout must be employed to achieve full device performance. *Figure 76* shows the EVAL-LT3073-AZ evaluation board with a layout that delivers the full performance of the regulator. Refer to the *EVAL-LT3073-AZ evaluation board user guide* for further details.

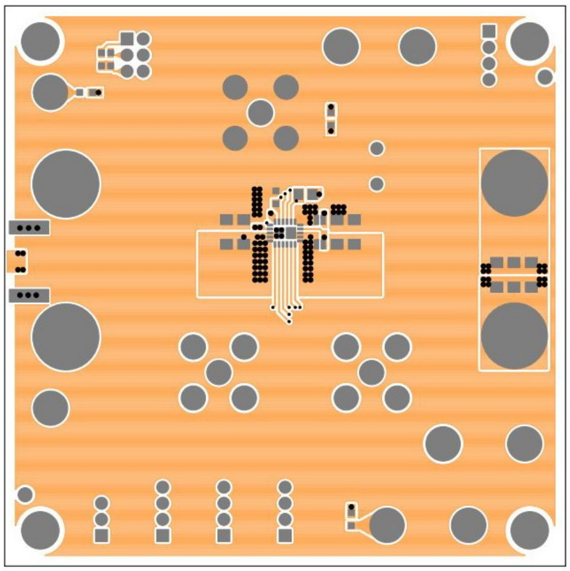


Figure 76. EVAL-LT3073-AZ Evaluation Board

Protection Features

The LT3073 has an internal current limit that clamps output current to 4.5A. In addition, the LT3073 has a ±3% accurate programmable precision current limit. The die junction temperature can exceed the 125°C maximum operating temperature if the ambient temperature is high enough. If this occurs, the LT3073 relies on an internal thermal safety feature. Typically at 168°C, the LT3073 thermal shutdown engages and the output is shut down until the IC temperature falls below its thermal hysteresis limit.

Current Monitor and Externally Programmable Current Limit

The IMON pin's current limit threshold is 1V. Connecting a resistor from IMON to GND sets the maximum current flowing out of the IMON pin, which in turn, programs LT3073's current limit. With a 3A•kΩ programming scale factor, the current limit can be calculated as follows:

$$Current\ Limit = \frac{3A \times k\Omega}{R_{ILIM}}$$

For example, a 1kΩ resistor programs the current limit to 3A, and a 2kΩ resistor programs the current limit to 1.5A. Kelvin connect this resistor to the LT3073's GND pin for good accuracy.

As shown in the electrical characteristic table (*Table 1*), the IMON pin sources current proportional (1:3000) to output current; if the external current limit is not used, connect IMON t GND, which sets the Internal current limit to 4.5A.

Thermal Considerations

For higher ambient temperatures, care should be taken in the layout of the PCB to ensure good heat sinking of the LT3073. The IN and OUT pins on the bottom of the package should be soldered to IN and OUT planes accordingly. In addition, the IN and OUT must be connected to large copper layers below with thermal vias; these layers will spread heat dissipated by the LT3073. Placing additional vias can reduce thermal resistance further. The die temperature is calculated by multiplying the LT3073 power dissipation by the thermal resistance from the junction to the ambient.

The internal overtemperature protection monitors the junction temperature of the LT3073. If the junction temperature reaches approximately 168°C, the LT3073 output is shut down until the temperature drops about 7°C.

Table 7 lists thermal resistance as a function of the copper area on a fixed board size. All measurements were taken in still air on a 4-layer FR-4 board with 1oz solid internal planes and 2oz top/bottom planes with a total board thickness of 1.6mm. The four layers were electrically isolated with no thermal vias present. PCB layers, copper weight, board layout, and thermal vias affect the thermal resistance result. For more information on thermal resistance and high thermal conductivity test boards, refer to JEDEC standard JESD51, notably JESD51-7 and JESD51-12. Achieving low thermal resistance necessitates attention to detail and careful PCB layout.

Table 7. Measured Thermal Resistance of LQFN Package

COPPER AREA		BOARD AREA	THERMAL RESISTANCE (θ_{JA})
TOP SIDE [1]	BOTTOM SIDE		
$2500mm^2$	$2500mm^2$	$2500mm^2$	33°C/W
$1000mm^2$	$2500mm^2$	$2500mm^2$	34°C/W
$225mm^2$	$2500mm^2$	$2500mm^2$	36°C/W
$100mm^2$	$2500mm^2$	$2500mm^2$	39°C/W

[1] Device is mounted on top side

Calculating Junction Temperature

Example: Given an output voltage of 1.2V, input voltage of 1.5V, and BIAS voltage of 5V, output current ranges from 10mA to 3A, and a maximum ambient temperature of 50°C, what is the maximum junction temperature?

The LT3073's power dissipation is:

$$I_{OUT(MAX)} \times (V_{IN} - V_{OUT}) + I_{GND} \times V_{BIAS}$$

where:

$$I_{OUT(MAX)} = 3A$$

$$V_{BIAS} = 5V$$

$$I_{GND}(at\ I_{OUT} = 3A\ and\ V_{BIAS} = 5V) = 5mA$$

thus:

$$P_{DISS} = 3A \times (1.5V - 1.2V) + 5mA \times 5V = 0.925W$$

When a 3mm x 4mm 4L LQFN package is used, the thermal resistance is in the range of 33°C/W to 39°C/W. Note that the θ_{JA} numbers will vary beyond the 33°C/W to 39°C/W depending on board composition and layout. Considering a θ_{JA} value of 36°C/W, the junction temperature rise above the ambient approximately equals:

0.925W × 36°C/W = 33.3°C

The maximum junction temperature equals the maximum ambient temperature plus the maximum junction temperature rise above ambient:

$$T_{JMAX} = 50°C + 33.3°C = 83.3°C$$

Paralleling Devices for Higher Output Current

As shown in *Figure 77*, multiple LT3073s may be paralleled to obtain a higher output current. This paralleling concept borrows from the scheme employed by the LT3080 product family.

To accomplish this paralleling, connect the IN and OUT pins of the multiple devices together. Also, connect the REF pins of the multiple devices. This effectively gives an averaged value of multiple reference voltage sources. The OUT of each LT3073 is connected to the common load using a small piece of PC trace as a ballast resistor (≅2mΩ) or an actual sense resistor beyond the feedback SENSE tap of each regulator. The ballast resistor ensures output current sharing. Keep this ballast trace area free of solder to maintain a controlled resistance.

Table 8 shows a simple guideline for PCB trace resistance as a function of weight and trace width.

Table 8. PC Board Trace Resistance

WEIGHT (oz)	10mil WIDTH	20mil WIDTH
1	54.3	27.1
2	27.1	13.6

Trace resistance is measured in mΩ/in.

Output Noise

The LT3073 offers many advantages for noise performance. Traditional linear regulators have several sources of noise. The most critical noise sources for a conventional regulator are its voltage reference, error amplifier, noise from the resistor divider network used for setting output voltage, and the noise gain created by this resistor divider.

LT3073's unity-gain follower architecture presents no gain from the REF pin to the output. Therefore, if a capacitor bypasses the REF pin internal resistor DAC, the output noise is independent of the programmed output voltage. The resultant output noise is set just by the error amplifier's noise — typically $3nV/\sqrt{Hz}$ from 10kHz to 1MHz and $1.2\mu V_{RMS}$ in a 10Hz to 100kHz bandwidth using a 4.7µF REF pin capacitor. Paralleling multiple LT3073s further reduces noise by $\sqrt{N}$ for N parallel regulators.

Filtering High Frequency Spikes

For applications where the LT3073 is used to post-regulate a switching converter, its high PSRR effectively suppresses any "noise" present at the switcher's switching frequency — typically 100kHz to 4MHz. However, the high frequency (hundreds of MHz) "spikes" — beyond the LT3073's bandwidth — associated with the switcher's power switch transition times will almost directly pass through the LT3073. While the output capacitor is partly intended to absorb these spikes, its ESL will limit its ability at these frequencies. A ferrite bead or the inductance associated with a short (example: 0.5 inch) PCB trace between the switcher's output and the LT3073's input can serve as an LC filter to suppress these very high-frequency spikes.

Fast Start-Up

For ultralow noise applications that require low 1/f noise (i.e., at frequencies below 100Hz), a larger value REF pin capacitor is required, up to 22µF. While this would normally significantly increase the regulator's start-up time, the LT3073 incorporates fast start-up circuitry that increases the REF pin current to about 2mA during start-up. For a 22µF capacitor, this will reduce the start-up time from 100ms to 5ms.

The 2mA current source remains engaged until REF is 98.8% of its final value on the rising edge. It will restart when REF is below 91% of the output setting on the falling edge unless the regulator is in the current limit, thermal shutdown or any UVLO situation.

Temperature Monitoring

The TEMP pin outputs a voltage proportional to the average junction temperature. The pin voltage is 250mV for 25°C and has a slope of 10mV/°C. The TEMP pin is stable with no bypass capacitor or a bypass capacitor with a value between 100pF and 1nF. A 100pF capacitor is recommended to improve TEMP pin power supply rejection. If not used, leave TEMP unconnected.

TYPICAL APPLICATION CIRCUITS

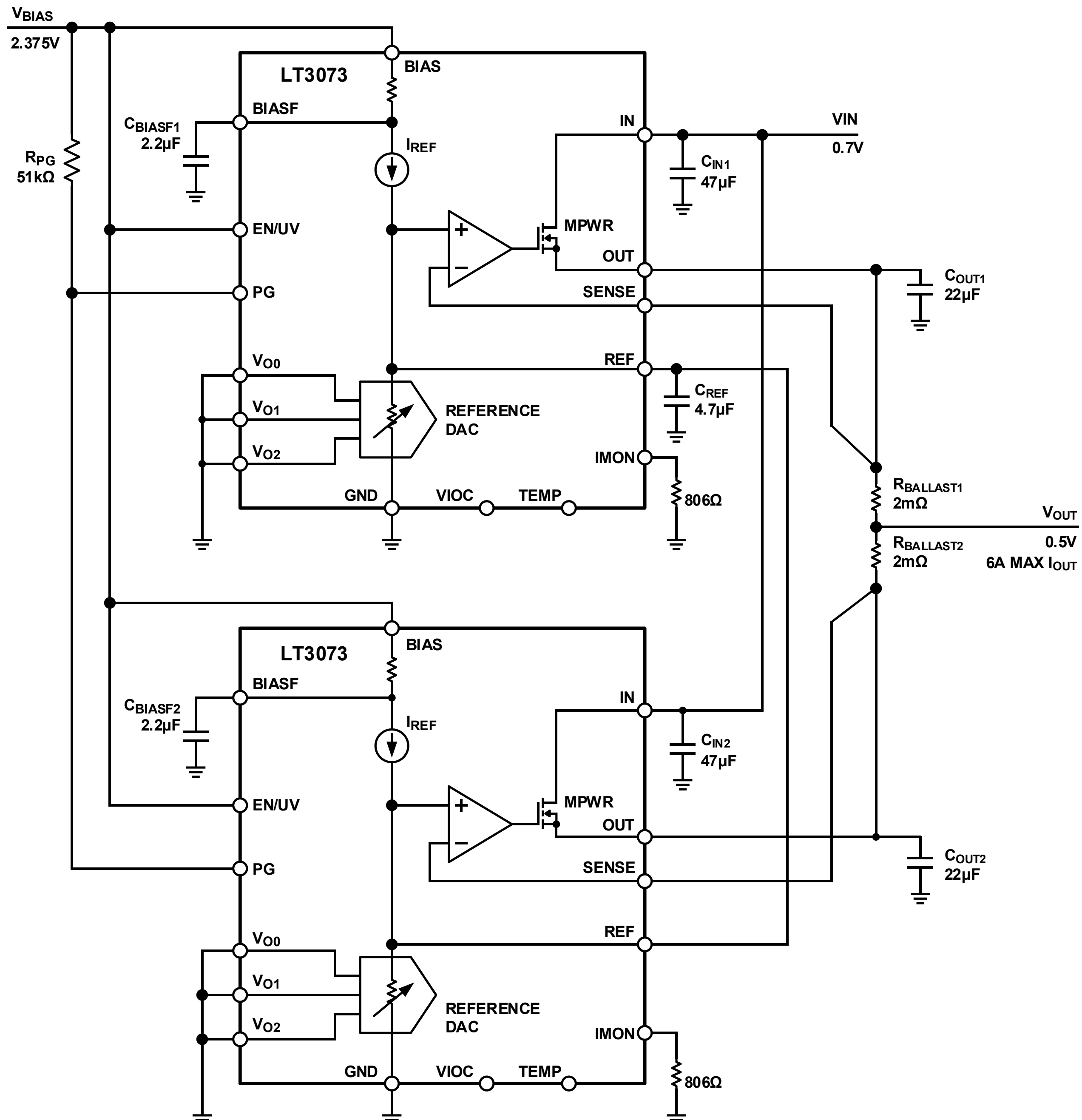


Figure 77. Paralleling Multiple LT3073s for Higher Output Current

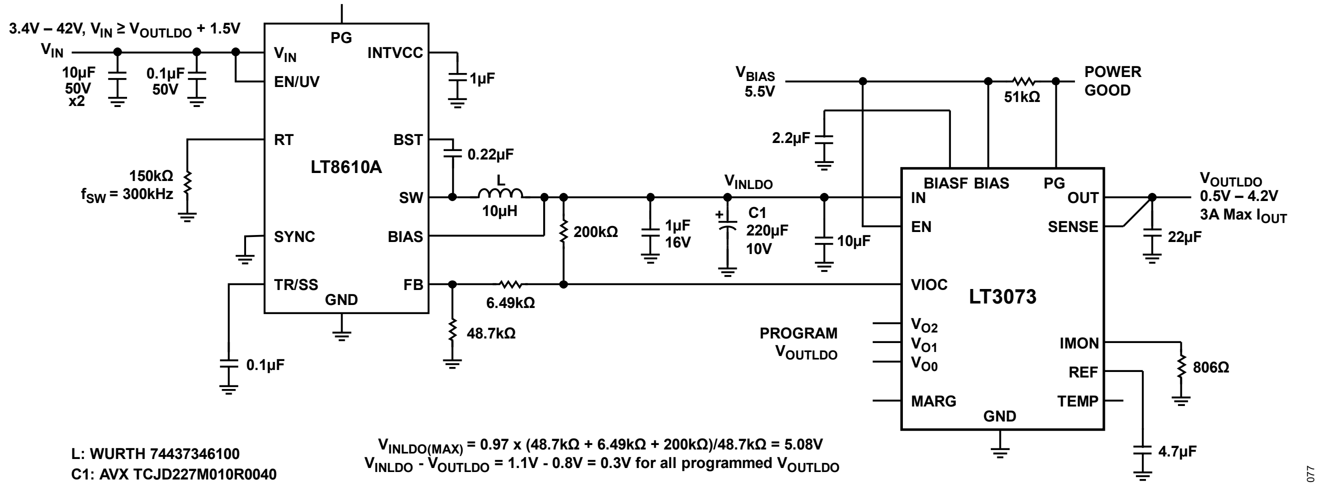
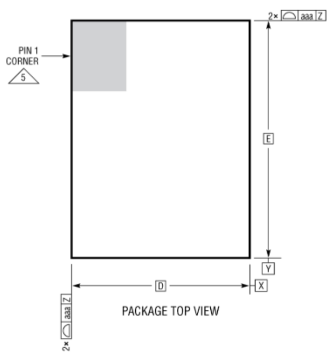


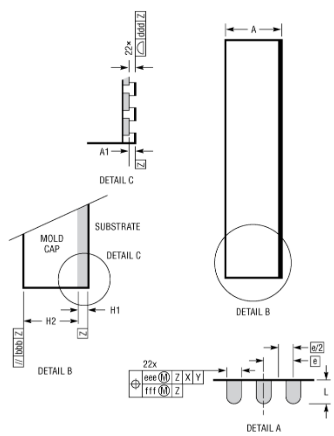
Figure 78. Regulator with VIOC Buck Control

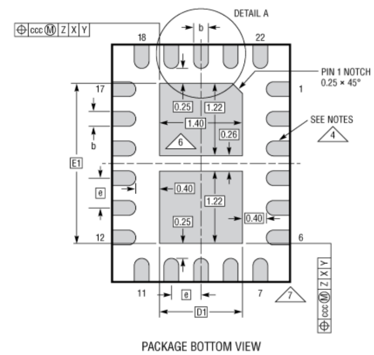
OUTLINE DIMENSIONS

ANALOG DEVICES

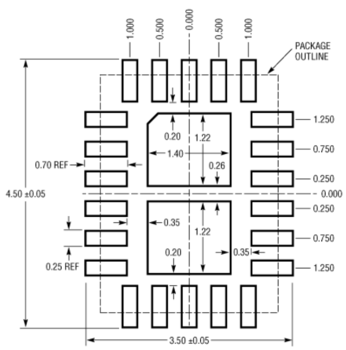
LQFN Package
22-Lead (3mm × 4mm × 0.95mm)
(Reference LTC DWG # 05-08-7054 Rev Ø)







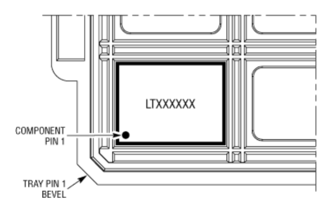
NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994
2. ALL DIMENSIONS ARE IN MILLIMETERS
3. PRIMARY DATUM -Z- IS SEATING PLANE
4. METAL FEATURES UNDER THE SOLDER MASK OPENING NOT SHOWN SO AS NOT TO OBSCURE THESE TERMINALS AND HEAT FEATURES
5. DETAILS OF PIN 1 IDENTIFIER ARE OPTIONAL, BUT MUST BE LOCATED WITHIN THE ZONE INDICATED. THE PIN 1 IDENTIFIER MAY BE EITHER A MOLD OR MARKED FEATURE
6. THE EXPOSED HEAT FEATURE MAY HAVE OPTIONAL CORNER RADII
7. CORNER SUPPORT PAD CHAMFER IS OPTIONAL



SUGGESTED PCB LAYOUT
TOP VIEW

DIMENSIONS

SYMBOL	MIN	NOM	MAX	NOTES
A	0.85	0.95	1.05	
A1			0.03	
L	0.30	0.40	0.50	
b	0.22	0.25	0.28	
D		3.00		
E		4.00		
D1		1.40		
E1		2.70		
e		0.50		
H1		0.25 REF		SUBSTRATE THK
H2		0.70 REF		MOLD CAP HT
aaa			0.10	
bbb			0.10	
ccc			0.10	
ddd			0.10	
eee			0.15	
fff			0.08	



PACKAGE IN TRAY LOADING ORIENTATION

LQFN 22 0720 REV Ø

ORDERING GUIDE

Table 9. Ordering Guide

MODEL [1]	TEMPERATURE RANGE	PACKAGE DESCRIPTION	MSL RATING	PACKING QUANTITY	PACKAGE OPTION
LT3073AV#PBF	-40°C to 125°C	22-LEAD (3mm x 4mm LQFN)	3	Tray, 490	05-08-7054
LT3073AV#TRPBF	-40°C to 125°C	22-LEAD (3mm x 4mm LQFN)	3	Reel, 2500	05-08-7054

[1] All models are RoHS compliant parts.

EVALUATION BOARDS

Table 10. Evaluation Boards

MODEL [1]	DESCRIPTION
EVAL-LT3073-AZ	Evaluation Board

[1] The EVAL-LT3073-AZ is a RoHS compliant part.

RELATED PARTs

Table 11. Related Parts

PART NUMBER	DESCRIPTION	COMMENTS
LT3070-1	5A, Low Noise, Programmable V_{OUT}, 85mV Dropout Linear Regulator with Digital Margining	85mV Dropout Voltage, Digitally Programmable V_{OUT}: 0.8V to 1.8V, Digital Output Margining: ±1%, ±3% or ±5%, Low Output Noise:25µV_{RMS}; Directly Parallelable, Soft Start, Stable with Low ESR Ceramic Output Capacitors (15µF Minimum), 28 Lead 4mm × 5mm QFN Package.
LT3071	5A, Low Noise, Programmable V_{OUT}, 85mV Dropout Linear Regulator with Analog Margining	85mV Dropout Voltage, Digitally Programmable V_{OUT}: 0.8V to 1.8V, Analog Margining: ±10%, Low Output Noise: 25µV_{RMS}; Directly Parallelable, Output Current Monitor, Stable with Low ESR Ceramic Output Capacitors (15µF Minimum), 28 Lead 4mm × 5mm QFN Package.
LT3072	Dual, Low Noise, 2.5A Programmable Output, 80mV Low Dropout Linear Regulator	Dual, Independent 2.5A Outputs, Dropout Voltage: 80mV, Low Output Noise: 12µV_{RMS} (10Hz to 100kHz), Digitally Programmable V_{OUT}: 0.6V to 2.5V, Output Tolerance: ±1.25%/±1.5% Over-load, Line and Temperature, Analog Output Margining: ±10% Range, 36-Lead 4mm × 7mm QFN Package.
ADP1763	3A, Low V_{IN}, Low Noise, CMOS Linear Regulator	95mV Dropout, Fixed (0.9V to 1.5V) and Adjustable (0.5V to 1.5V) V_{OUT}, V_{IN} = 1.1V to 1.98V, 2µV_{RMS} Noise (100Hz to 100kHz), Programmable Soft Start, Direct Parallelable, Stable with Ceramic Capacitors (10µF minimum), AEC-Q100 qualified, 16-Lead 3mm x 3mm LFCSP Package.
ADP1765	5A, Low V_{IN}, Low Noise, CMOS Linear Regulator	59mV Dropout, Fixed (0.55V to 1.5V) and Adjustable (0.5V to 1.5V) V_{OUT}, V_{IN} = 1.1V to 1.98V, 2µV_{RMS} Noise (100Hz to 100kHz), Programmable Soft Start, Direct Parallelable, Stable with Ceramic Capacitors (22µF minimum), 16-Lead 3mm x 3mm LFCSP Package.
MAX38907	4A, High-Performance LDO Linear Regulator	79mV Dropout, Digitally Programmable V_{OUT}: 0.6V to 5V, V_{IN} = 0.9V to 5.5V, Digital Margining: ±5%, Programmable Soft Start, Reverse Current Protection, Active Discharge, 20-Lead 5mm x 5mm TQFN Package.
LT3041	20V, 1A, Ultra-low Noise, Ultra-high PSRR Linear Regulator with VIOC Control	1µV_{RMS} Noise (10Hz to 100kHz), 8µV_{P-P} Noise (0.1Hz to 10Hz), 80dB PSRR at 1MHz, V_{IN} = 2.2V to 20V, V_{OUT} = 0.2V to 15V, 310mV Dropout, Direct Parallelable, Programmable Current Limit and Power Good, Stable with Low ESR Ceramic Capacitors (2x 10µF Minimum), 14-Lead 4mm x 3mm DFN Package.

PART NUMBER	DESCRIPTION	COMMENTS
LT3045	500mA, Ultra-low Noise and Ultra-high PSRR LDO	0.8µV_{RMS} Noise and 75dB PSRR at 1MHz, V_{IN} = 1.8V to 20V, 260mV Dropout Voltage, 3mm × 3mm DFN and MSOP Packages.
LT3042	200mA, Ultra-low Noise and Ultra-high PSRR LDO	0.8µV_{RMS} Noise and 79dB PSRR at 1MHz, V_{IN} = 1.8V to 20V, 350mV Dropout Voltage, Programmable Current Limit and Power Good, 3mm× 3mm DFN and MSOP Packages.
LT3083	3A, Parallelable, Low Noise, Low Dropout Linear Regulator	310mV Dropout Voltage (2-Supply Operation), Low Noise: 40µV_{RMS}, V_{IN}: 1.2V to 23V, V_{OUT}: 0V to 22.6V, Current-Based Reference with one Resistor V_{OUT} Set, Directly Parallelable (No Op Amp Required), Stable with Ceramic Capacitors; TO-220, DD-PAK, TSSOP, 4mm × 4mm DFN-12 Packages.