# 20 V, 1 A, Ultra-Low Noise, Ultra-High PSRR Linear Regulator with VIOC Control

## FEATURES

- Ultra-low output RMS noise: 1.0 µV rms (10 Hz to 100 kHz)
- Ultra-low output noise spectral density: 3 nV/√Hz at 10 kHz
- Ultra-low 1/f noise: 8 µV p-p (0.1 Hz to 10 Hz)
- Ultra-high PSRR: 80 dB at 1 MHz
- Output current: 1 A
- Wide input voltage range: 2.2 V to 20 V
- Single capacitor improves noise and PSRR
- SET pin current: 100 µA, ±0.5% initial accuracy
- VIOC pin to manage power dissipation
- Single resistor programs output voltage
- Programmable current limit
- Low-dropout voltage: 310 mV
- Output voltage range: 0.2 V to 19 V
- Programmable power good
- Fast start-up capability
- Precision enable/UVLO
- Parallelable for lower noise and higher current
- Internal current limit with foldback
- Minimum output capacitor: 2 parallel 10 µF ceramic
- Compact, low profile, 14-lead, 4 mm × 3 mm, DFN package

## APPLICATIONS

- RF power supplies: phase-locked loops, voltage-controlled oscillators, mixers, low-noise amplifiers, and power amplifiers
- Low-noise instrumentation
- High-speed and high-precision data converters
- Medical applications: imaging and diagnostics
- Postregulator for switching supplies

## TYPICAL APPLICATION

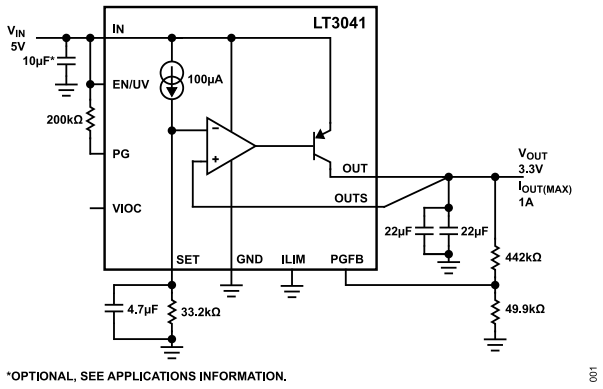


*Figure 1. Typical Application*

## GENERAL DESCRIPTION

The LT3041 is a high-performance, low-dropout linear regulator featuring Analog Devices, Inc., ultra-low noise and ultra-high power supply rejection ratio (PSRR) architecture for powering noise-sensitive applications. Designed as a precision-current reference followed by a high-performance voltage buffer, the LT3041 can be easily paralleled to further reduce noise, increase output current, and spread heat on the printed circuit board (PCB).

The LT3041 supplies 1 A at a typical 310 mV dropout voltage. The operating quiescent current is nominally 4.3 mA and drops to 18 µA in shutdown. The wide output voltage range (0.2 V to 19 V) of the LT3041 maintained by the unity-gain operation provides virtually constant output noise, PSRR, bandwidth, and load regulation, independent of the programmed output voltage. Additionally, the regulator features VIOC, programmable current limit, fast start-up capability, and programmable power good to indicate output-voltage regulation.

Built-in protection includes reverse-battery protection, reverse-current protection, internal current limit with foldback, and thermal limit with hysteresis. The LT3041 is available in a thermally enhanced, 14-lead 4 mm × 3 mm, DFN package.

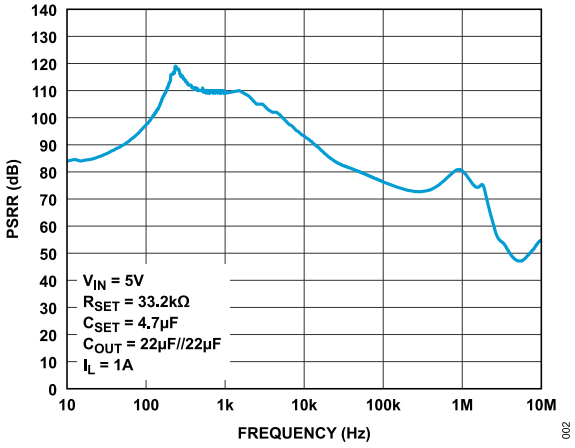


*Figure 2. PSRR vs. Frequency*


One Analog Way, Wilmington, MA 01887-2356, U.S.A.

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**10/2022—Revision 0: Initial Version**

## SPECIFICATIONS

### ELECTRICAL CHARACTERISTICS

$T_J$ = −40°C to +125°C for the minimum and maximum values, $T_A$ = 25°C for the typical values, output capacitance ($C_{OUT}$) = two parallel 10 µF ceramic capacitors, and SET capacitance ($C_{SET}$) = 4.7 µF, unless otherwise noted.

*Table 1. Electrical Characteristics*

| Parameter | Test Conditions/Comments | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| INPUT VOLTAGE RANGE | | 2.2 | | 20 | V |
| MINIMUM IN PIN VOLTAGE[1] | Input-voltage ($V_{IN}$) undervoltage lockout (UVLO) rising | | 2 | 2.2 | V |
| | $V_{IN}$ UVLO hysteresis | | 80 | | mV |
| OUTPUT VOLTAGE RANGE | $V_{IN}$ > output voltage ($V_{OUT}$) | 0.2 | | 19 | V |
| SET PIN CURRENT ($I_{SET}$) | $V_{IN}$ = 2.2 V, $I_L$ = 1 mA, $V_{OUT}$ = 1.3 V, $T_A$ = 25°C | 99.5 | 100 | 100.5 | µA |
| | 2.2 V < $V_{IN}$ < 20 V, 0.2 V < $V_{OUT}$ < 19 V, 1 mA < $I_L$ < 1 A[2] | 99 | 100 | 101 | µA |
| FAST STARTUP $I_{SET}$ | PGFB voltage ($V_{PGFB}$) = 289 mV, $V_{IN}$ = 2.8 V, SET voltage ($V_{SET}$) = 1.3 V | | 10 | | mA |
| OUTPUT OFFSET VOLTAGE, $V_{OS}$ ($V_{OUT}$ – $V_{SET}$)[3] | $V_{IN}$ = 2.2 V, $I_L$ = 1 mA, $V_{OUT}$ = 1.3 V, $T_A$ = 25°C | –1 | | +1 | mV |
| | 2.2 V < $V_{IN}$ < 20 V, 0.2 V < $V_{OUT}$ < 19 V, 1 mA < $I_L$ < 1 A[2] | –2 | | +2 | mV |
| LINE REGULATION | | | | | |
| $\Delta I_{SET}$ | $V_{IN}$ = 2.2 V to 20 V, $I_L$ = 1 mA, $V_{OUT}$ = 1.3 V | | 0.1 | ±12 | nA/V |
| $\Delta V_{OS}$ | $V_{IN}$ = 2.2 V to 20 V, $I_L$ = 1 mA, $V_{OUT}$ = 1.3 V[3] | | 1.5 | ±30 | µV/V |
| LOAD REGULATION | | | | | |
| $\Delta I_{SET}$ | $I_L$ = 1 mA to 1 A, $V_{IN}$ = 2.2 V, $V_{OUT}$ = 1.3 V | | 3 | | nA |
| $\Delta V_{OS}$ | $I_L$ = 1 mA to 1 A, $V_{IN}$ = 2.2 V, $V_{OUT}$ = 1.3 V[3] | | 0.1 | 0.8 | mV |
| CHANGE IN $I_{SET}$ WITH $V_{SET}$[4] | $V_{SET}$ = 1.3 V to 19 V, $V_{IN}$ = 20 V, $I_L$ = 1 mA | | 140 | 500 | nA |
| | $V_{SET}$ = 0.2 V to 0.75 V, $V_{IN}$ = 20 V, $I_L$ = 1 mA | | 10 | 200 | nA |
| CHANGE IN $V_{OS}$ WITH $V_{SET}$[4] | $V_{SET}$ = 1.3 V to 19 V, $V_{IN}$ = 20 V, $I_L$ = 1 mA[3] | | 0.06 | 0.6 | mV |
| | $V_{SET}$ = 0.2 V to 0.75 V, $V_{IN}$ = 20 V, $I_L$ = 1 mA[3] | | 0.004 | 0.2 | mV |
| ERROR-AMPLIFIER SWITCHOVER POINT | $V_{IN}$ = 2.2 V, $I_L$ = 1 mA, $V_{SET}$ rising | | 946 | | mV |
| PNP to NPN Input-Pair Switchover | $V_{IN}$ = 2.2 V, $I_L$ = 1 mA, $V_{SET}$ falling | | 922 | | mV |
| | Hysteresis | | 24 | | mV |
| DROPOUT VOLTAGE[5] | $I_L$ = 1 mA and 100 mA, $T_A$ = 25°C | | 290 | 370 | mV |
| | $I_L$ = 1 mA and 100 mA | | | 460 | mV |
| | $I_L$ = 500 mA, $T_A$ = 25°C | | 290 | 380 | mV |
| | $I_L$ = 500 mA | | | 470 | mV |
| | $I_L$ = 1 A, $T_A$ = 25°C | | 310 | 390 | mV |
| | $I_L$ = 1 A | | | 480 | mV |
| GND PIN CURRENT, $V_{IN}$ = $V_{OUT\ (NOMINAL)}$[6] | $I_L$ = 10 µA | | 4.3 | | mA |
| | $I_L$ = 1 mA | | 4.4 | 7 | mA |
| | $I_L$ = 100 mA | | 7 | 13 | mA |
| | $I_L$ = 500 mA | | 16 | 25 | mA |
| | $I_L$ = 1 A | | 32 | 50 | mA |
| OUTPUT NOISE[3, 7] | $I_L$ = 1 A, frequency = 10 Hz, $C_{SET}$ = 0.47 µF, $V_{OUT}$ = 3.3 V | | 287 | | nV/√Hz |
| | $I_L$ = 1 A, frequency = 10 Hz, $C_{SET}$ = 4.7 µF, 1.3 V ≤ $V_{OUT}$ ≤ 19 V | | 36 | | nV/√Hz |
| | $I_L$ = 1 A, frequency = 10 kHz, $C_{SET}$ = 0.47 µF, 1.3 V ≤ $V_{OUT}$ ≤ 19 V | | 3 | | nV/√Hz |
| | $I_L$ = 1 A, frequency = 10 kHz, $C_{SET}$ = 0.47 µF, 0.2 V ≤ $V_{OUT}$ < 1.3 V | | 9 | | nV/√Hz |

## SPECIFICATIONS

*Table 1. Electrical Characteristics (Continued)*

| Parameter | Test Conditions/Comments | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| OUTPUT RMS NOISE[3, 7] | $I_L$ = 1 A, bandwidth = 10 Hz to 100 kHz, $C_{SET}$ = 0.47 µF, $V_{OUT}$ = 3.3 V | | 2.2 | | µV rms |
| | $I_L$ = 1 A, bandwidth = 10 Hz to 100 kHz, $C_{SET}$ = 4.7 µF, 1.3 V ≤ $V_{OUT}$ ≤ 19 V | | 1.0 | | µV rms |
| | $I_L$ = 1 A, bandwidth = 10 Hz to 100 kHz, $C_{SET}$ = 4.7 µF, 0.2 V ≤ $V_{OUT}$ < 1.3 V | | 2.3 | | µV rms |
| OUTPUT PEAK-TO-PEAK 1/F NOISE[3, 7] | $I_L$ = 1 A, bandwidth = 0.1 Hz to 10 Hz, $C_{SET}$ = 4.7 µF, $V_{OUT}$ = 3.3 V | | 25 | | µV p-p |
| | $I_L$ = 1 A, bandwidth = 0.1 Hz to 10 Hz, $C_{SET}$ = 22 µF, $V_{OUT}$ = 3.3 V | | 8 | | µV p-p |
| REFERENCE CURRENT RMS OUTPUT NOISE[3, 7] | Bandwidth = 10 Hz to 100 kHz | | 6 | | nA rms |
| POWER-SUPPLY REJECTION RATIO (PSRR) | | | | | |
| 1.3 V ≤ $V_{OUT}$ ≤ 18.3 V ($V_{IN}$ – $V_{OUT}$ = 1.7 V (Avg)[3, 7]) | Ripple voltage ($V_{RIPPLE}$) = 500 mV p-p, ripple frequency ($f_{RIPPLE}$) = 120 Hz, $I_L$ = 1 A | | 100 | | dB |
| | $V_{RIPPLE}$ = 150 mV p-p, $f_{RIPPLE}$ = 10 kHz, $I_L$ = 1 A | | 90 | | dB |
| | $V_{RIPPLE}$ = 150 mV p-p, $f_{RIPPLE}$ = 100 kHz, $I_L$ = 1 A | | 77 | | dB |
| | $V_{RIPPLE}$ = 150 mV p-p, $f_{RIPPLE}$ = 1 MHz, $I_L$ = 1 A | | 70 | | dB |
| | $V_{RIPPLE}$ = 80 mV p-p, $f_{RIPPLE}$ = 10 MHz, $I_L$ = 1 A | | 56 | | dB |
| 0.2 V ≤ $V_{OUT}$ < 1.3 V ($V_{IN}$ – $V_{OUT}$ = 1.7 V (Avg) or $V_{IN(min)}$ = 2.2 V[3, 7]) | $V_{RIPPLE}$ = 500 mV p-p, $f_{RIPPLE}$ = 120 Hz, $I_L$ = 1 A | | 102 | | dB |
| | $V_{RIPPLE}$ = 50 mV p-p, $f_{RIPPLE}$ = 10 kHz, $I_L$ = 1 A | | 86 | | dB |
| | $V_{RIPPLE}$ = 50 mV p-p, $f_{RIPPLE}$ = 100 kHz, $I_L$ = 1 A | | 73 | | dB |
| | $V_{RIPPLE}$ = 50 mV p-p, $f_{RIPPLE}$ = 1 MHz, $I_L$ = 1 A | | 72 | | dB |
| | $V_{RIPPLE}$ = 50 mV p-p, $f_{RIPPLE}$ = 10 MHz, $I_L$ = 1 A | | 60 | | dB |
| EN/UV PIN | | | | | |
| Threshold | EN/UV trip-point rising (turn-on), $V_{IN}$ = 2.2 V | 1.20 | 1.28 | 1.36 | V |
| Hysteresis | EN/UV trip-point hysteresis, $V_{IN}$ = 2.2 V | | 110 | | mV |
| Current ($I_{EN/UV}$) | EN/UV voltage ($V_{EN/UV}$) = 0 V, $V_{IN}$ = 20 V | | | ±1 | µA |
| | $V_{EN/UV}$ = 1.28 V, $V_{IN}$ = 20 V | | 0.003 | | µA |
| | $V_{EN/UV}$ = 20 V, $V_{IN}$ = 0 V | | 1.5 | 8 | µA |
| QUIESCENT CURRENT IN SHUTDOWN ($V_{EN/UV}$ = 0 V) | $V_{IN}$ = 6 V, $T_A$ = 25°C | | 18 | 40 | µA |
| | $V_{IN}$ = 6 V | | | 100 | µA |
| CURRENT LIMIT | | | | | |
| Internal[8] | $V_{IN}$ = 2.2 V, $V_{OUT}$ = 0 V | 1.15 | 1.25 | 1.35 | A |
| | $V_{IN}$ = 12 V, $V_{OUT}$ = 0 V | | 1.1 | | A |
| | $V_{IN}$ = 20 V, $V_{OUT}$ = 0 V | 200 | 340 | 520 | mA |
| Programmable | Programming scale factor: 2.2 V < $V_{IN}$ < 20 V[9] | | 150 | | mA × kΩ |
| | $V_{IN}$ = 2.2 V, $V_{OUT}$ = 0 V, $R_{ILIM}$ = 150 Ω | 0.9 | 1 | 1.1 | A |
| | $V_{IN}$ = 2.2 V, $V_{OUT}$ = 0 V, $R_{ILIM}$ = 300 Ω | 450 | 500 | 550 | mA |
| PGFB PIN | | | | | |
| Trip Point | PGFB trip-point rising | 292 | 302 | 312 | mV |
| Hysteresis | PGFB trip-point hysteresis | | 7 | | mV |
| Current ($I_{PGFB}$) | $V_{IN}$ = 2.2 V, $V_{PGFB}$ = 300 mV | | 25 | | nA |
| PG PIN | | | | | |
| Output Low Voltage | PG current ($I_{PG}$) = 100 µA | | 40 | 120 | mV |
| Leakage Current | PG voltage ($V_{PG}$) = 20 V | | | 1 | µA |
| REVERSE CURRENT | | | | | |
| Input | $V_{IN}$ = –20 V, $V_{EN/UV}$ = 0 V, $V_{OUT}$ = 0 V, $V_{SET}$ = 0 V | | | 200 | µA |
| Output | $V_{IN}$ = 0 V, $V_{OUT}$ = 5 V, SET = open, $T_A$ = 25°C | | 16 | 1000 | µA |

## SPECIFICATIONS

*Table 1. Electrical Characteristics (Continued)*

| Parameter | Test Conditions/Comments | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| THERMAL SHUTDOWN | $T_J$ rising | | 169 | | °C |
| | Hysteresis | | 5 | | °C |
| START-UP TIME | $V_{OUT\ (NOM)}$ = 5 V, $I_L$ = 1 A, $C_{SET}$ = 0.47 µF, $V_{IN}$ = 6 V, $V_{PGFB}$ = 6 V | | 55 | | ms |
| | $V_{OUT\ (NOM)}$ = 5 V, $I_L$ = 1 A, $C_{SET}$ = 4.7 µF, $V_{IN}$ = 6 V, $V_{PGFB}$ = 6 V | | 550 | | ms |
| | $V_{OUT\ (NOM)}$ = 5 V, $I_L$ = 1 A, $C_{SET}$ = 4.7 µF, $V_{IN}$ = 6 V, Power-Good 1 resistance ($R_{PG1}$) = 50 kΩ, Power-Good 2 resistance ($R_{PG2}$) = 700 kΩ (with fast startup to 90% of $V_{OUT}$) | | 10 | | ms |
| THERMAL REGULATION | 10 ms pulse | | –0.01 | | %/W |
| DIFFERENTIAL VIOC[10] | VIOC amplifier gain | | 1 | | V/V |
| | VIOC pin voltage range: $V_{OUT}$ > VIOC voltage ($V_{VIOC}$) + 0.6 V | 1 | | 4 | V |
| | VIOC pin voltage: $V_{OUT}$ ≤ 1.5 V, $V_{IN}$ = 2.5 V | | 1 | | V |
| | VIOC pin source current | 300 | | | µA |
| | VIOC pin sink current: $V_{IN}$ ≥ 2.5 V | | | 2 | µA |

[1] The EN/UV pin threshold must be met to ensure device operation.

[2] The maximum $T_J$ limits operating conditions. The regulated output-voltage specification does not apply for all possible combinations of input voltage and output current, especially due to the internal current-limit foldback, which starts to decrease current limit at $V_{IN} – V_{OUT}$ > 11 V. If operating at the maximum output current, limit the input-voltage range. If operating at the maximum input voltage, limit the output-current range.

[3] OUTS ties directly to OUT.

[4] Changes in $I_{SET}$ and $V_{OS}$ with $V_{SET}$ are tested at 0.2 V, 0.75 V, 1.3 V, 15 V and 19 V to insure operation over the 0.2 V to 19 V SET pin voltage range.

[5] The dropout voltage is the minimum input-to-output differential voltage needed to maintain regulation at a specified output current. The dropout voltage is measured when output is 1% out of regulation. This definition results in a higher dropout voltage compared to hard dropout, which is measured when $V_{IN} = V_{OUT\ (NOMINAL)}$. For output voltages less than 1.7 V, the dropout voltage is limited by the minimum input-voltage specification. See Figure 18 for the dropout voltage as a function of the output current and for temperature see Figure 19, which was measured in a typical application circuit.

[6] The GND pin current is tested with $V_{IN} = V_{OUT\ (NOMINAL)}$ and a current source load. Therefore, the LT3041 is tested while operating in dropout, which is the worst-case GND pin current. The GND pin current decreases at higher input voltages. Note that the GND pin current does not include the SET pin or the ILIM pin current; however, quiescent current does include the SET and ILIM pins.

[7] Adding a capacitor across the SET pin resistor decreases the output voltage noise. Adding this capacitor bypasses the thermal noise of the resistor on the SET pin as well as the noise of the reference current. The output noise then equals the error-amplifier noise. Use of a SET pin bypass capacitor also increases the start-up time.

[8] The internal back-up current-limit circuitry incorporates foldback protection that decreases current limit for $V_{IN} – V_{OUT}$ > 11 V. Some level of output current is provided at all $V_{IN} – V_{OUT}$ differential voltages. See Figure 32 for the current limit as a function of $V_{IN} – V_{OUT}$.

[9] The current-limit programming scale factor is specified while the internal backup current limit is not active. Note that the internal current limit has foldback protection for $V_{IN} – V_{OUT}$ differentials greater than 11 V.

[10] The VIOC buffer outputs a voltage equal to $V_{IN} – V_{OUT}$ or $V_{IN}$ – 1.5 V for $V_{OUT}$ ≤ 1.5 V. See Figure 70 and the High-Efficiency Linear Regulator: Voltage Input-to-Output Control (VIOC) section for further information. Set the source current of the VIOC pin between 10 µA and 300 µA.

## ABSOLUTE MAXIMUM RATINGS

*Table 2. Absolute Maximum Ratings*

| Parameter | Value |
|---|---|
| IN Pin Voltage | ±22 V |
| VIOC Pin Voltage[1] | –0.3 V to +4 V |
| EN/UV Pin Voltage | ±22 V |
| IN-to-EN/UV Differential | ±22 V |
| PG Pin Voltage[1] | –0.3 V, +22 V |
| ILIM Pin Voltage[1] | –0.3 V, +1 V |
| PGFB Pin Voltage[1] | –0.3 V, +22 V |
| PGFB Pin Current | ±20 mA |
| SET Pin Voltage[1] | –0.3 V, +20 V |
| SET Pin Current[2] | ±20 mA |
| OUTS Pin Voltage[1] | –0.3 V, +20 V |
| OUTS Pin Current[2] | ±20 mA |
| OUT Pin Voltage[1] | –0.3 V, +20 V |
| OUT-to-OUTS Differential[3] | ±1.2 V |
| IN-to-OUT Differential | ±22 V |
| IN-to-OUTS Differential | ±22 V |
| Output Short-Circuit Duration | Indefinite |
| Temperature | |
| Operating $T_J$ Range[4], A Grade | –40°C to +125°C |
| Storage Range | –65°C to +150°C |

1 Parasitic diodes exist internally between the VIOC, ILIM, PG, PGFB, SET, OUTS, and OUT pins and the GND pin. Do not drive the VIOC, ILIM, PG, PGFB, SET, OUTS, and OUT pins more than 0.3 V less than the GND pin during a fault condition. The VIOC, ILIM, PG, PGFB, SET, OUTS, and OUT pins must remain at a voltage more positive than GND during normal operation.

2 SET and OUTS pins are clamped using diodes and two 25 Ω series resistors. For less than 5 ms transients, this clamp circuitry can carry more than the rated current. Refer to Figure 70 and the Protection Features section for more information.

3 Maximum OUT-to-OUTS differential is guaranteed by design.

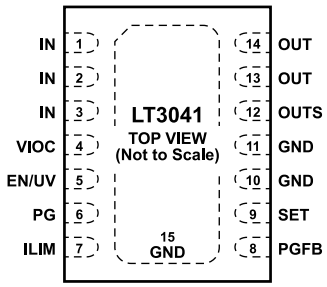
4 The LT3041 is tested and specified under pulse load conditions such that $T_J \approx T_A$. The LT3041 is tested at $T_A$ = 25°C. Performance of the LT3041 over the full –40°C to 125°C operating temperature range is assured by design, characterization, and correlation with statistical process controls. The LT3041 is guaranteed over the full –40°C to 125°C operating $T_J$ range.

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

## ESD CAUTION

**ESD (electrostatic discharge) sensitive device**. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

## PIN CONFIGURATION AND FUNCTION DESCRIPTIONS




$\theta_{JC(TOP)}$ = 42.8°C/W, $\theta_{JC(BOT)}$ = 4.7°C/W

THE EXPOSED PAD IS AN ELECTRICAL CONNECTION TO GND. TO ENSURE PROPER ELECTRICAL AND THERMAL PERFORMANCE, SOLDER THE EXPOSED BACKSIDE TO THE PCB GROUND AND CONNECT IT DIRECTLY TO THE GND PINS.

003

*Figure 3. Pin Configuration*

*Table 3. Pin Function Descriptions*

| Pin No. | Mnemonic | Description |
|---|---|---|
| 1, 2, 3 | IN | Input. The IN pins supply power to the regulator. The LT3041 requires a bypass capacitor at the IN pin. In general, the output impedance of a battery rises with frequency; therefore, it is best practice to include a bypass capacitor in battery-powered applications. While a 10 µF input bypass capacitor generally suffices, applications with large load transients can require higher input capacitance to prevent input-supply droop. Refer to the Stability and Input Capacitance and PSRR and Input Capacitance sections on the proper use of an input capacitor and its effect on circuit performance, in particular PSRR. The LT3041 withstands reverse voltages on IN with respect to GND, OUTS, and OUT. In the case of a reversed input, which occurs if a battery is plugged in backwards, the LT3041 acts as if a diode is in series with its input. Therefore, no reverse-current flows into the LT3041, and no negative voltage appears at the load. The device protects itself and the load. |
| 4 | VIOC | Voltage for Input-to-Output Control. The LT3041 incorporates a tracking function to control the switching preregulator powering the LT3041. The VIOC pin is the output of this tracking function that drives the feedback (FB) pin of the preregulator to maintain the input voltage of the LT3041 at $V_{OUT}$ + $V_{VIOC}$. This function minimizes power dissipation while maintaining PSRR performance. Refer to the High-Efficiency Linear Regulator: Voltage Input-to-Output Control (VIOC) section for further details. |
| 5 | EN/UV | Enable and UVLO. Pulling the EN/UV pin low moves the LT3041 to shutdown mode. Quiescent current in shutdown mode drops to 18 µA and the output voltage turns off. Alternatively, the EN/UV pin can set an input-supply UVLO threshold by using a resistor-divider between IN, EN/UV, and GND. The LT3041 typically turns on when the EN/UV voltage exceeds 1.28 V on its rising edge, with a 110 mV hysteresis on its falling edge. The EN/UV pin can be driven above the input voltage and maintain proper functionality. If unused, connect EN/UV to IN. Do not float the EN/UV pin. |
| 6 | PG | Power Good. PG is an open-drain flag that indicates output-voltage regulation. PG pulls low if PGFB is less than 302 mV. If the power-good functionality is not needed, float the PG pin. A parasitic substrate diode exists between the PG and GND pins of the LT3041; therefore, do not drive PG more than 0.3 V less than GND during normal operation or during a fault condition. |
| 7 | ILIM | Current-Limit Programming Pin. Connecting a resistor between ILIM and GND programs the current limit. For best accuracy, Kelvin connect this resistor directly to the GND pin of the LT3041. The programming-scale factor is nominally 150 mA × kΩ. The ILIM pin sources current proportional (1:500) to the output current. Therefore, ILIM also serves as a current-monitoring pin with a 0 V to 300 mV range. If the programmable current-limit functionality is not needed, connect ILIM to GND. A parasitic substrate diode exists between the ILIM and GND pins of the LT3041; therefore, do not drive ILIM more than 0.3 V less than GND during normal operation or during a fault condition. |
| 8 | PGFB | Power-Good Feedback. The PG pin pulls high if PGFB increases beyond 302 mV on its rising edge, with 7 mV hysteresis on its falling edge. Connecting an external resistor-divider between OUT, PGFB, and GND sets the programmable power-good threshold with the following transfer function: 0.302 V × (1 + $R_{PG2}/R_{PG1}$). As discussed further in the Fast Startup section, PGFB also activates the fast start-up circuitry. Connect PGFB to IN if the power-good and fast start-up functions are not needed. In addition, if reverse-input protection is additionally required, connect the anode of a 1N4148 diode to IN and its cathode to PGFB. Refer to Figure 96 for further details. A parasitic-substrate diode exists between the PGFB and GND pins of the LT3041; therefore, do not drive PGFB more than 0.3 V less than GND during normal operation or during a fault condition. |
| 9 | SET | The Inverting Input of the Error Amplifier and the Regulation Set Point for the LT3041. SET sources precision 100 µA current that flows through an external resistor connected between SET and GND. The output voltage of the LT3041 is determined by $V_{SET}$ = $I_{SET}$ × SET resistance ($R_{SET}$). The output voltage range is from 0.2 V to 19 V. Adding a capacitor from SET to GND improves noise, PSRR, and transient response at the expense of an increased start-up time. For optimum load regulation, Kelvin connect the ground side of the SET pin resistor directly to the load. A parasitic-substrate diode exists between the SET and GND pins of the LT3041; therefore, do not drive SET more than 0.3 V less than GND during normal operation or during a fault condition. |
| 10, 11 | GND | Ground. |

## PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

*Table 3. Pin Function Descriptions (Continued)*

| Pin No. | Mnemonic | Description |
|---|---|---|
| 12 | OUTS | Output Sense. The OUTS pin is the noninverting input to the error amplifier. For optimal transient performance and load regulation, Kelvin connect OUTS directly to the output capacitor and the load. In addition, connect the GND connections of the output capacitor and the SET pin capacitor directly together. A parasitic-substrate diode exists between the OUTS and GND pins of the LT3041; therefore, do not drive OUTS more than 0.3 V less than GND during normal operation or during a fault condition. |
| 13, 14 | OUT | Output. The OUT pins supply power to the load. For stability, use a minimum of two 10 µF output capacitors in parallel with an equivalent series resistance (ESR) of less than 20 mΩ and an effective series inductance (ESL) of less than 2 nH each. Large load transients require larger output capacitance to limit peak-voltage transients. Refer to the Stability and Output Capacitance section for more information on output capacitance. A parasitic-substrate diode exists between the OUT and GND pins of the LT3041; therefore, do not drive OUT more than 0.3 V less than GND during normal operation or during a fault condition. |
| 15 | EPAD (GND) | Exposed Pad. The exposed pad is an electrical connection to GND. To ensure proper electrical and thermal performance, solder the exposed backside to the PCB ground and connect it directly to the GND pins. |

## TYPICAL PERFORMANCE CHARACTERISTICS

$T_A$ = 25°C, unless otherwise noted.

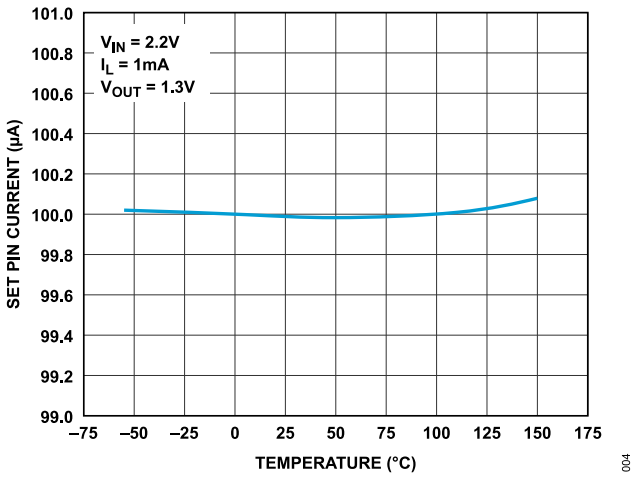



*Figure 4. SET Pin Current vs. Temperature*

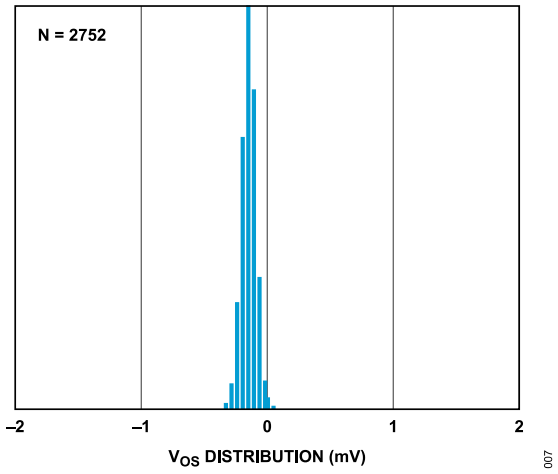



*Figure 7. Offset Voltage ($V_{OS}$) Distribution*

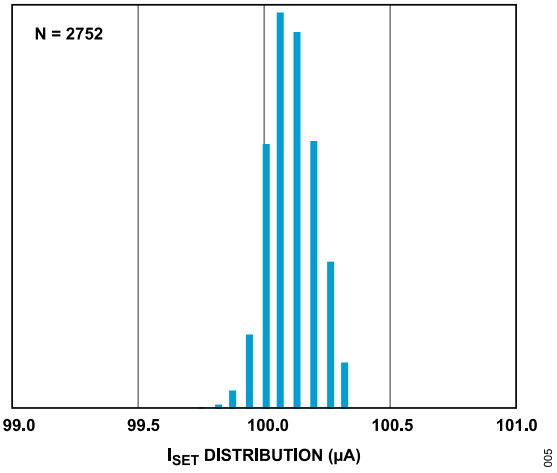



*Figure 5. $I_{SET}$ Distribution*

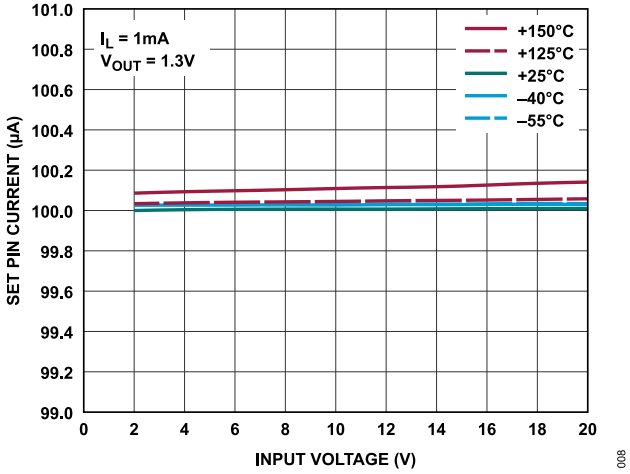



*Figure 8. SET Pin Current vs. Input Voltage*

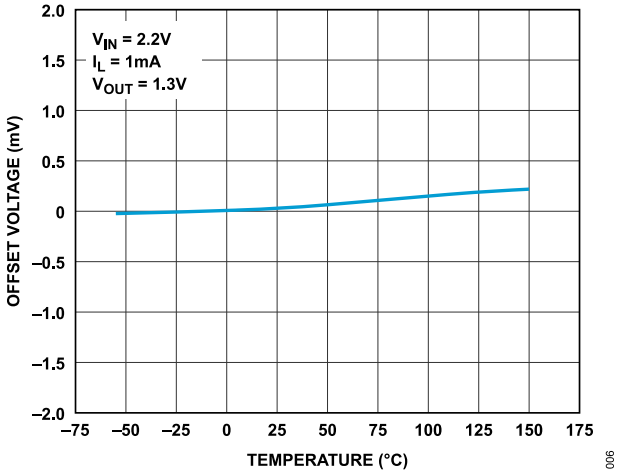



*Figure 6. Offset Voltage ($V_{OUT}$ – $V_{SET}$) vs. Temperature*

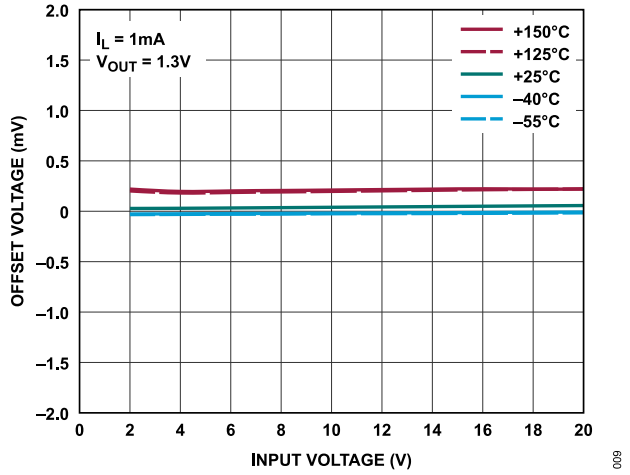



*Figure 9. Offset Voltage ($V_{OUT}$ – $V_{SET}$) vs. Input Voltage*

## TYPICAL PERFORMANCE CHARACTERISTICS

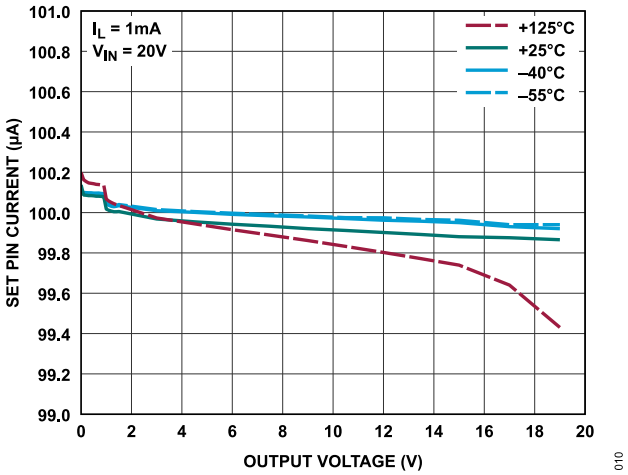



*Figure 10. SET Pin Current vs. Output Voltage*

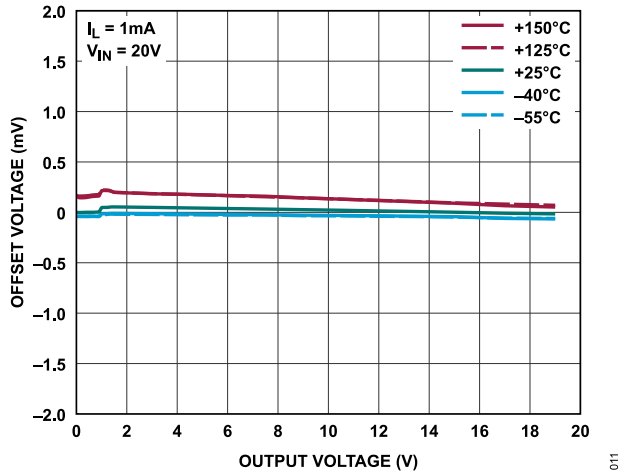



*Figure 11. Offset Voltage ($V_{OUT}$ – $V_{SET}$) vs. Output Voltage*

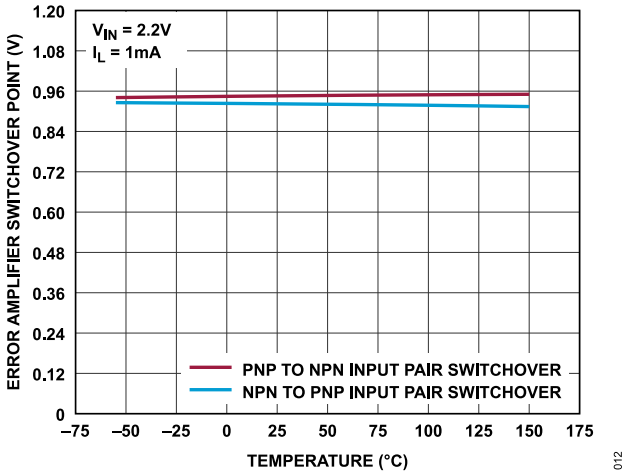



*Figure 12. Error Amplifier Switchover Point vs. Temperature*

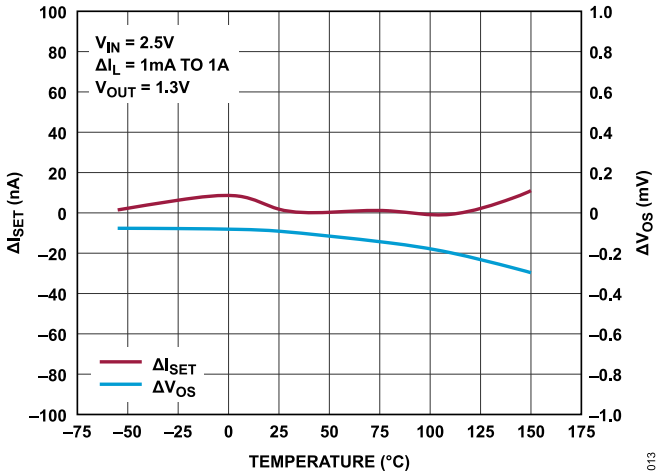



*Figure 13. $\Delta I_{SET}$ and $\Delta V_{OS}$ Load Regulation vs. Temperature*

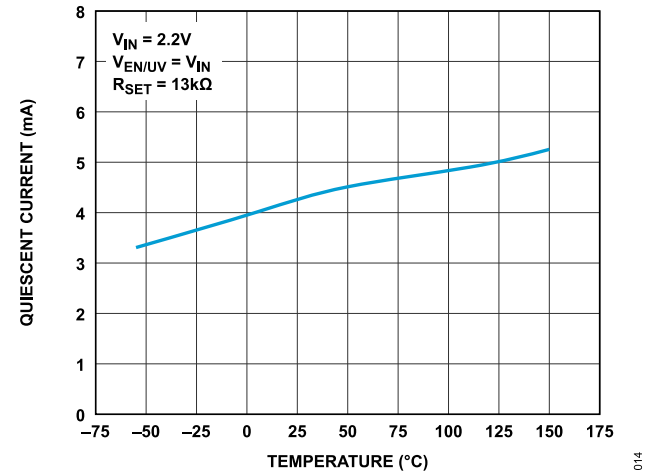



*Figure 14. Quiescent Current vs. Temperature ($V_{EN/UV}$ = $V_{IN}$)*

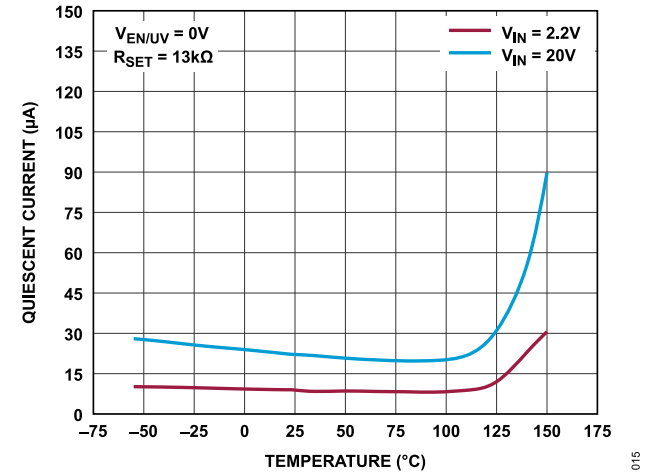



*Figure 15. Quiescent Current vs. Temperature ($V_{EN/UV}$ = 0 V)*

## TYPICAL PERFORMANCE CHARACTERISTICS

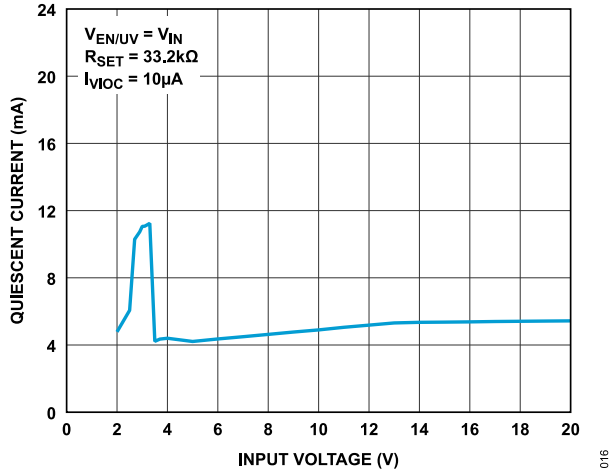



*Figure 16. Quiescent Current vs. Input Voltage ($I_{VIOC}$ Is the VIOC Current)*

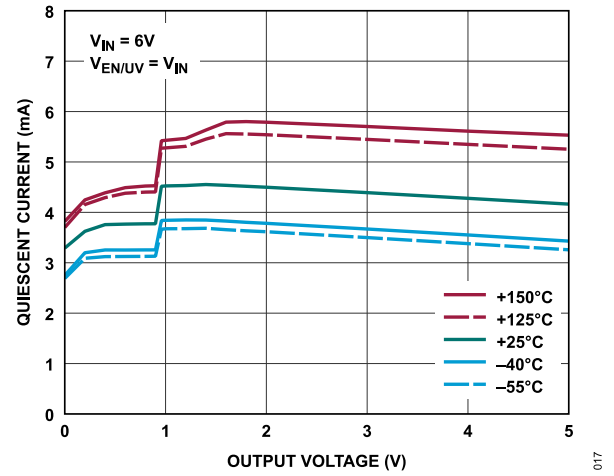



*Figure 17. Quiescent Current vs. Output Voltage*

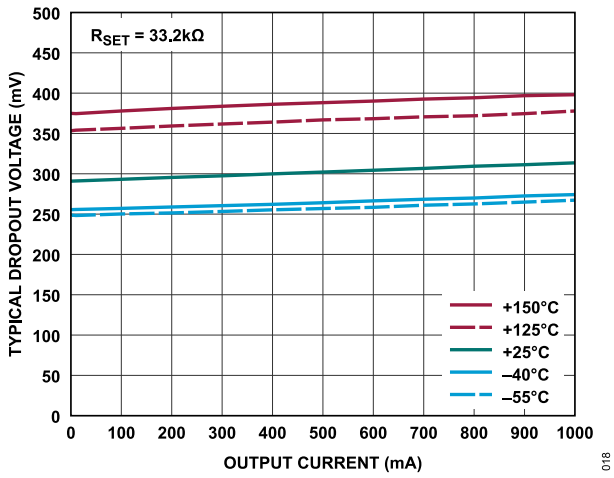



*Figure 18. Typical Dropout Voltage vs. Output Current*

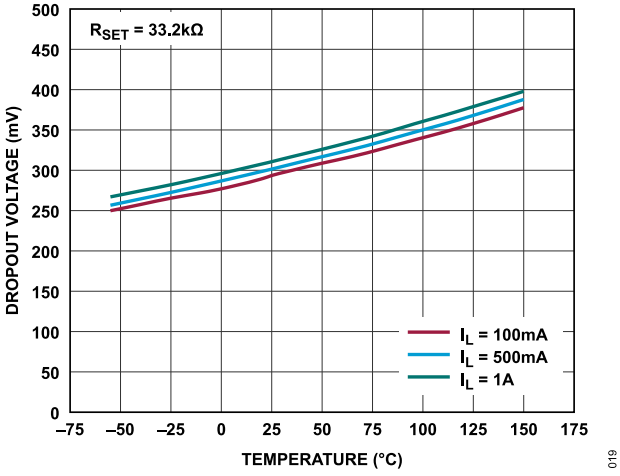



*Figure 19. Dropout Voltage vs. Temperature*

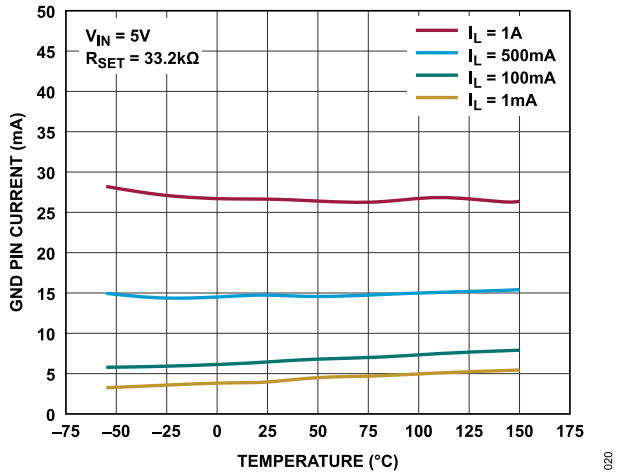



*Figure 20. GND Pin Current vs. Temperature*

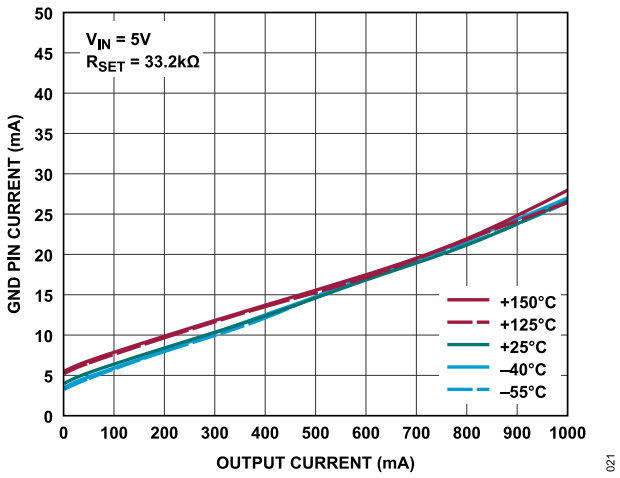



*Figure 21. GND Pin Current vs. Output Current*

## TYPICAL PERFORMANCE CHARACTERISTICS

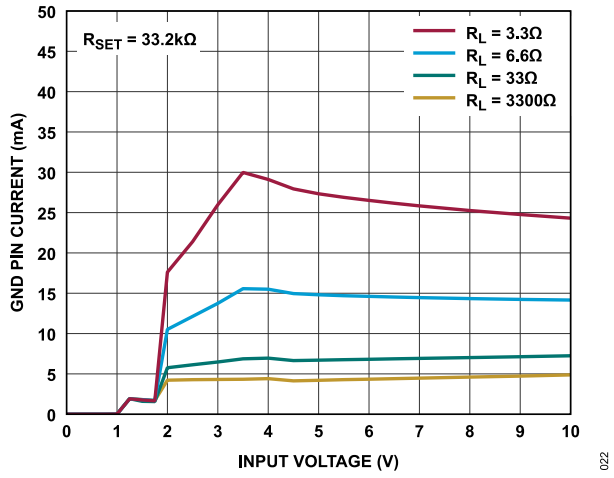



*Figure 22. GND Pin Current vs. Input Voltage ($R_L$ Is the Load Resistance)*

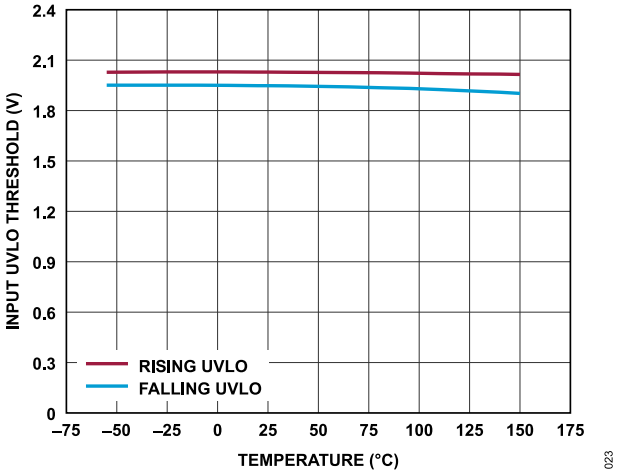



*Figure 23. Input UVLO Threshold vs. Temperature*

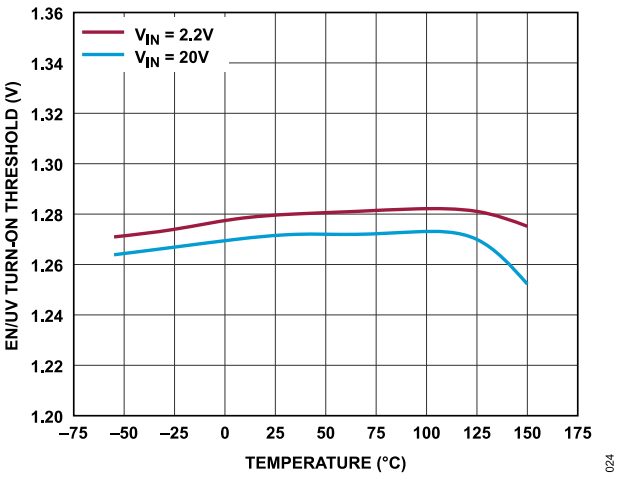



*Figure 24. EN/UV Turn-On Threshold vs. Temperature*

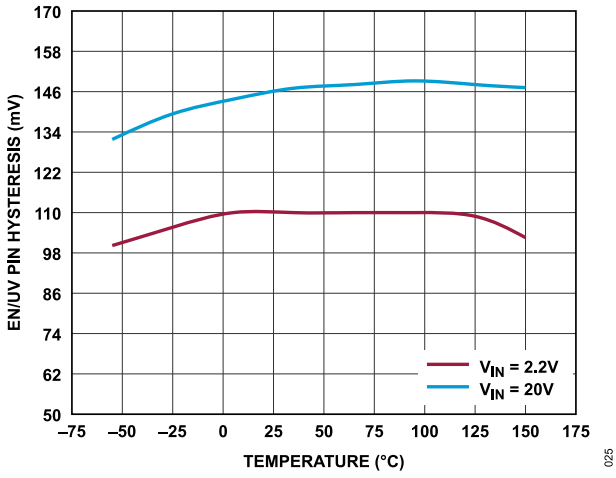



*Figure 25. EN/UV Pin Hysteresis vs. Temperature*

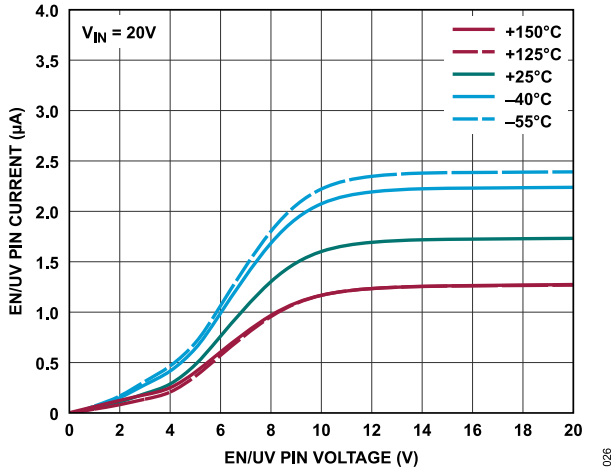



*Figure 26. EN/UV Pin Current vs. EN/UV Pin Voltage (Temperature Steps)*

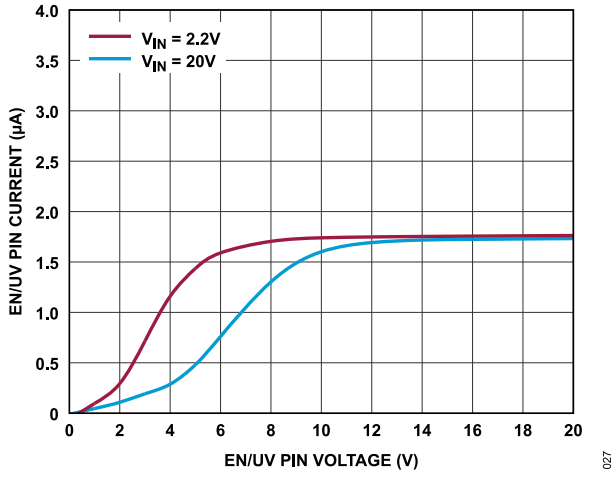



*Figure 27. EN/UV Pin Current vs. EN/UV Pin Voltage ($V_{IN}$ Steps)*

## TYPICAL PERFORMANCE CHARACTERISTICS

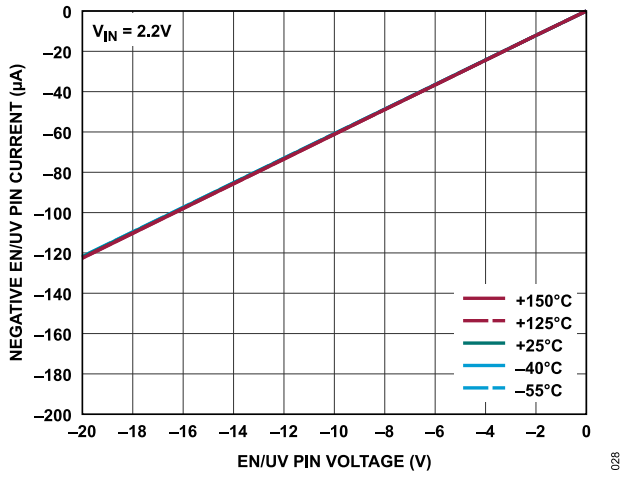



*Figure 28. Negative EN/UV Pin Current vs. EN/UV Pin Voltage*

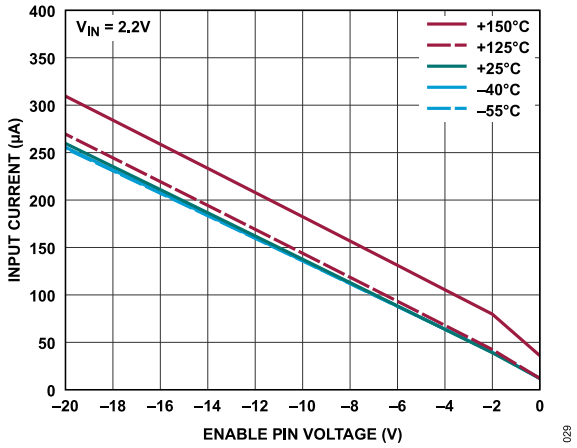



*Figure 29. Input Current vs. EN/UV Pin Voltage*

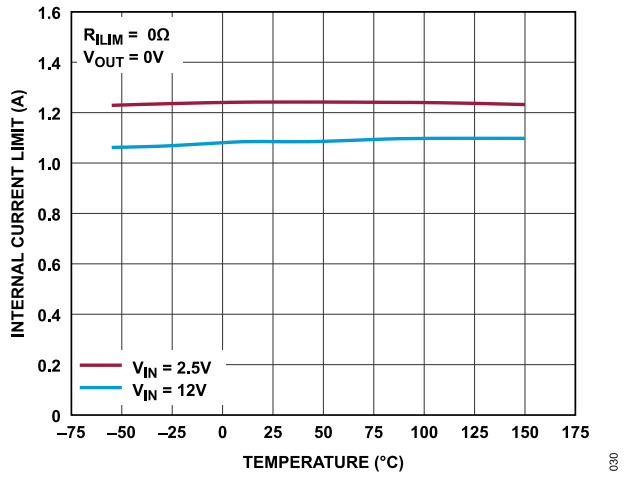



*Figure 30. Internal Current Limit vs. Temperature*

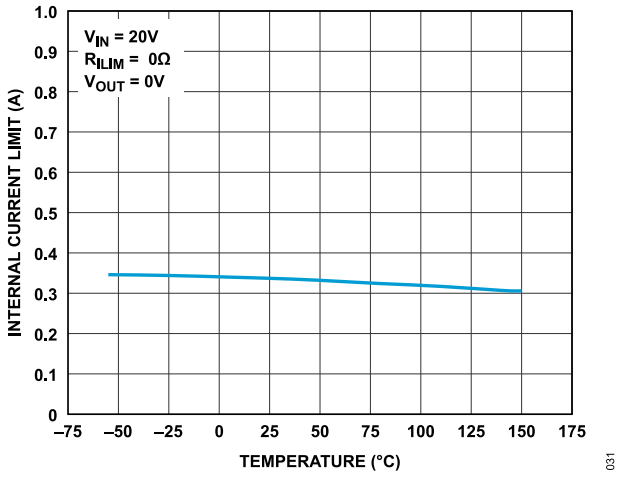



*Figure 31. Internal Current Limit vs. Temperature (Foldback)*

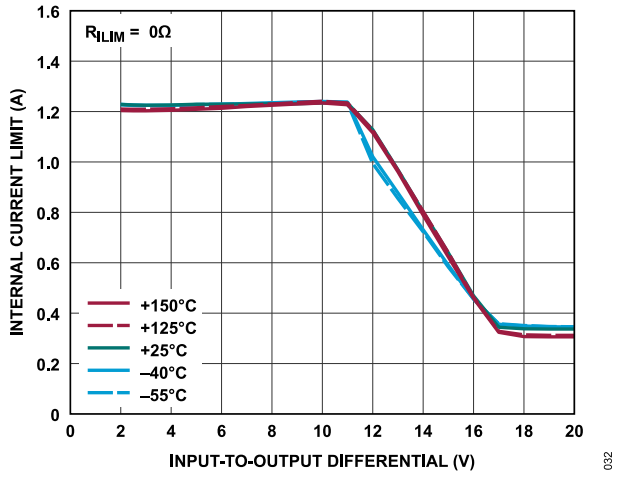



*Figure 32. Internal Current Limit vs. Input-to-Output Differential*

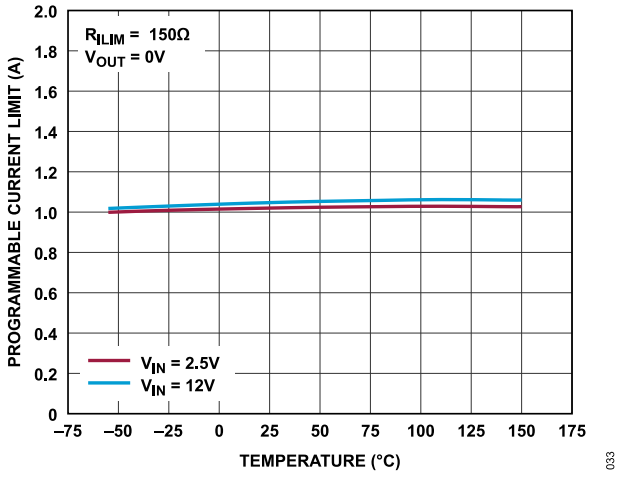



*Figure 33. Programmable Current Limit vs. Temperature (1 A)*

## TYPICAL PERFORMANCE CHARACTERISTICS

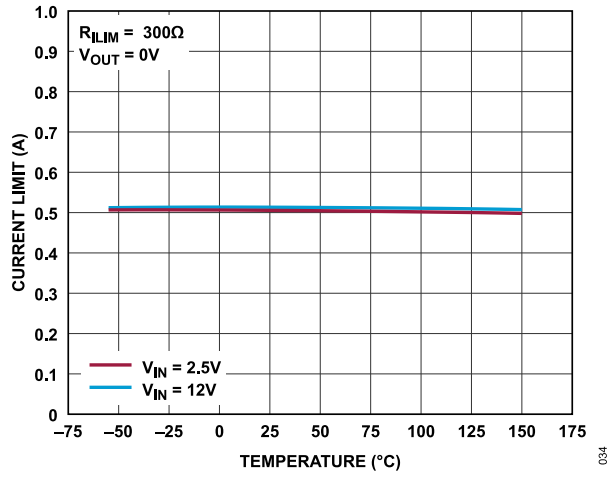



*Figure 34. Programmable Current Limit vs. Temperature (0.5 A)*

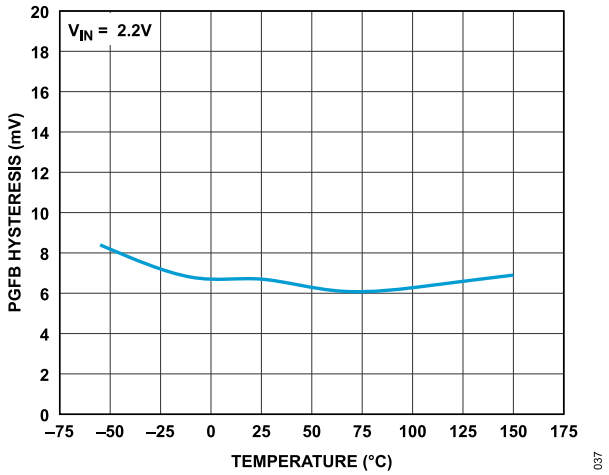



*Figure 37. PGFB Hysteresis vs. Temperature*

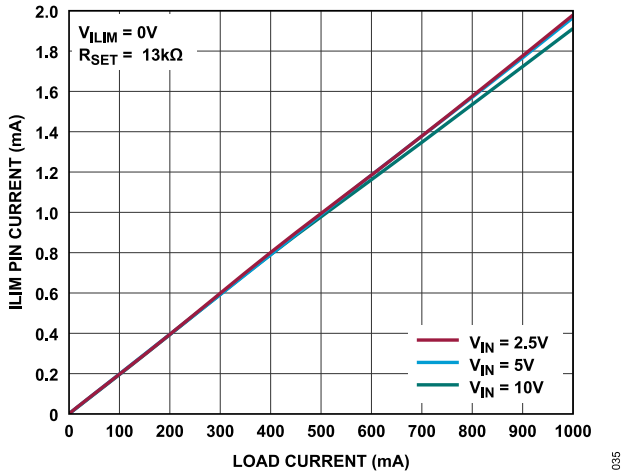



*Figure 35. ILIM Pin Current vs. Load Current*

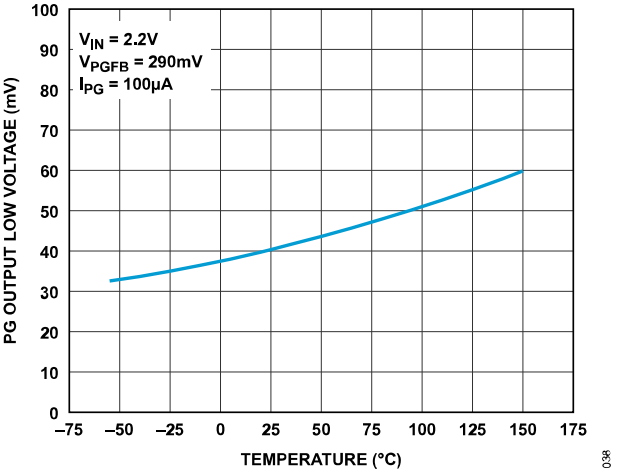



*Figure 38. PG Output Low Voltage vs. Temperature*

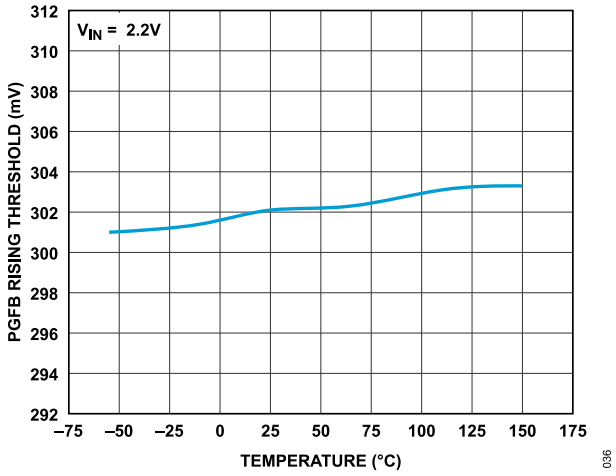



*Figure 36. PGFB Rising Threshold vs. Temperature*

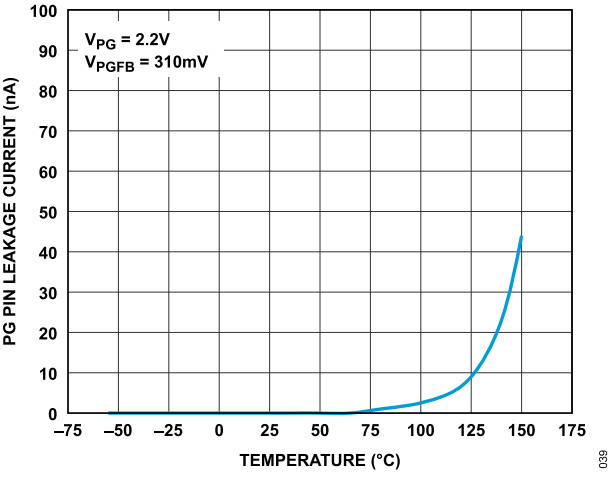



*Figure 39. PG Pin Leakage Current vs. Temperature*

## TYPICAL PERFORMANCE CHARACTERISTICS

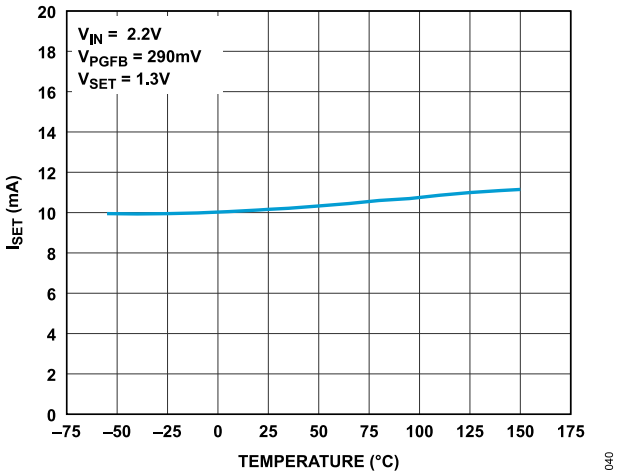



*Figure 40. $I_{SET}$ During Start-Up with Fast Start-Up Enabled vs. Temperature*

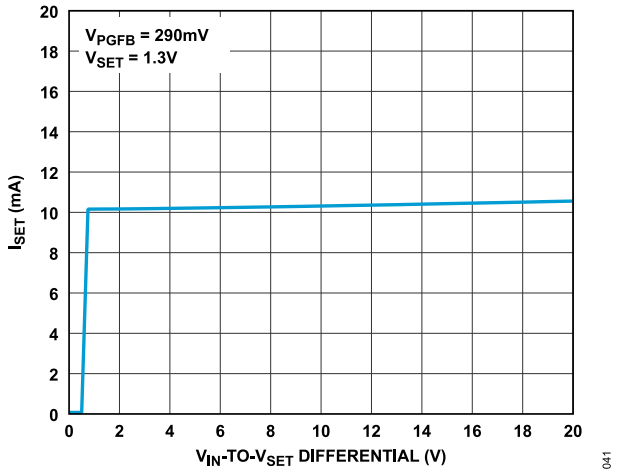



*Figure 41. $I_{SET}$ During Start-Up with Fast Start-Up Enabled vs. $V_{IN}$-to-$V_{SET}$ Differential*

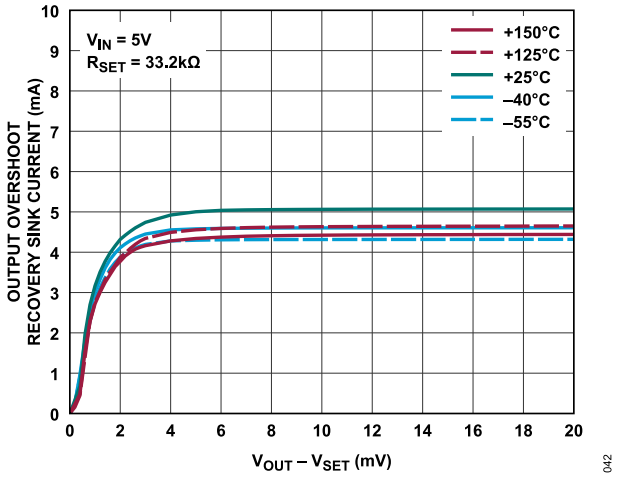



*Figure 42. Output Overshoot Recovery Sink Current vs. $V_{OUT}$ – $V_{SET}$*

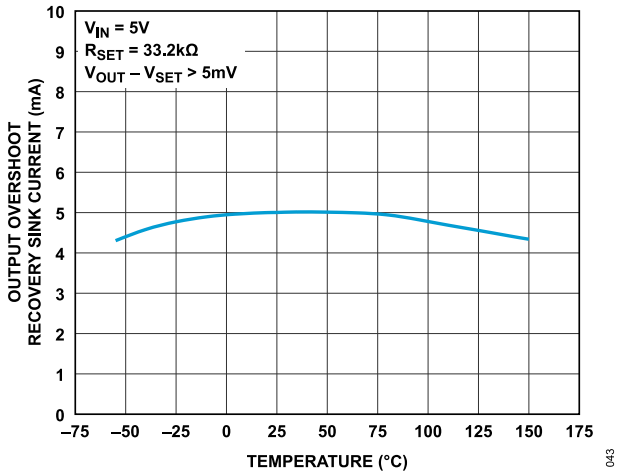



*Figure 43. Output Overshoot Recovery Sink Current vs. Temperature*

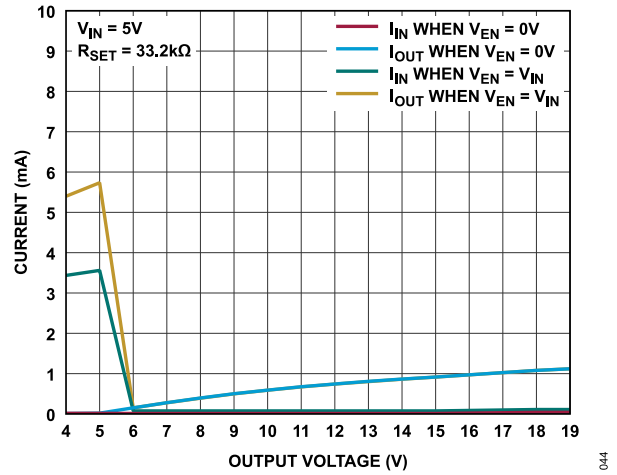



*Figure 44. Current when $V_{OUT}$ Forced Above $V_{OUT\ (NOMINAL)}$ vs. Output Voltage ($I_{IN}$ Is the Input Current, and $I_{OUT}$ Is the Output Current)*

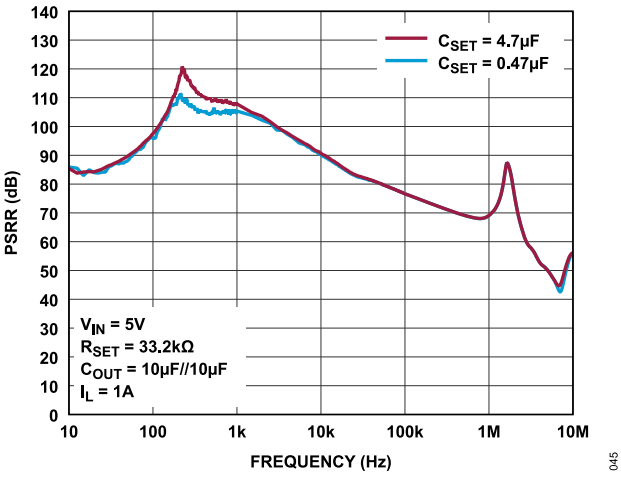



*Figure 45. PSRR vs. Frequency ($C_{SET}$ Steps)*

## TYPICAL PERFORMANCE CHARACTERISTICS

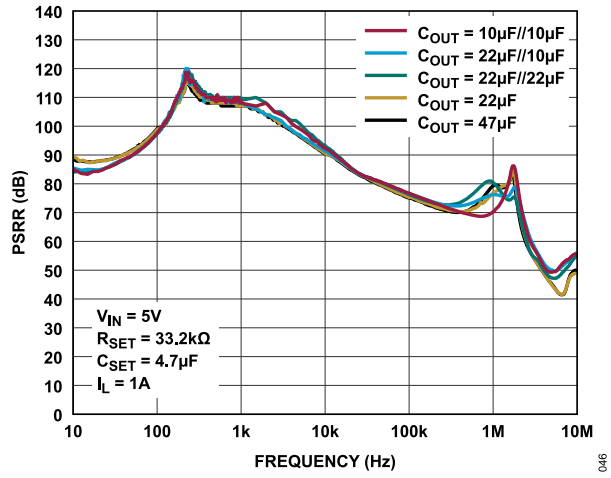



*Figure 46. PSRR vs. Frequency ($C_{OUT}$ Steps)*

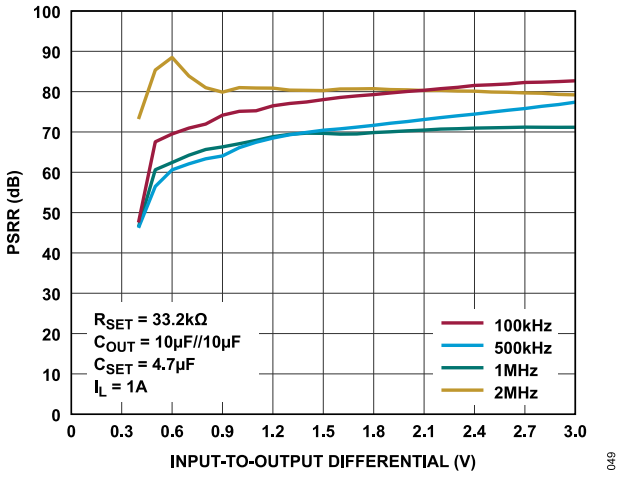



*Figure 49. PSRR vs. Input-to-Output Differential*

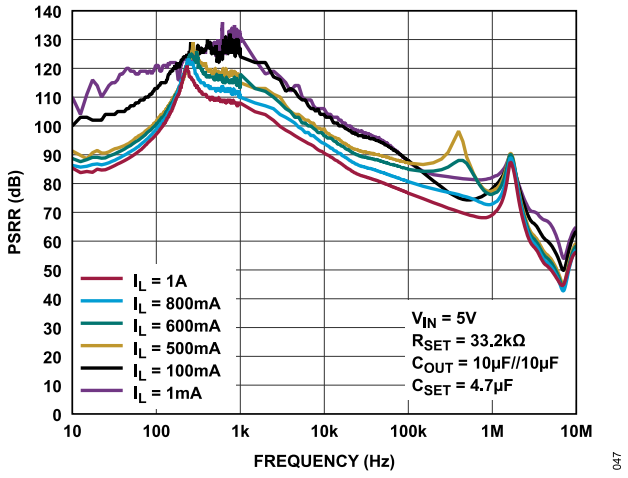



*Figure 47. PSRR vs. Frequency ($I_L$ Steps)*

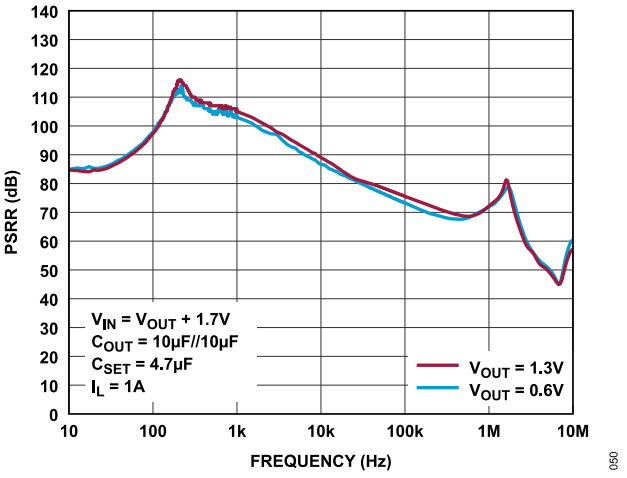



*Figure 50. PSRR as a Function of an Error-Amplifier Input Pair vs. Frequency*

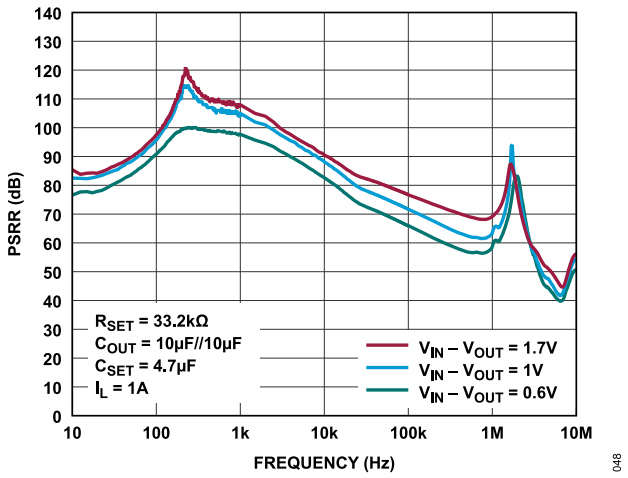



*Figure 48. PSRR vs. Frequency ($V_{IN}$ – $V_{OUT}$ Steps)*

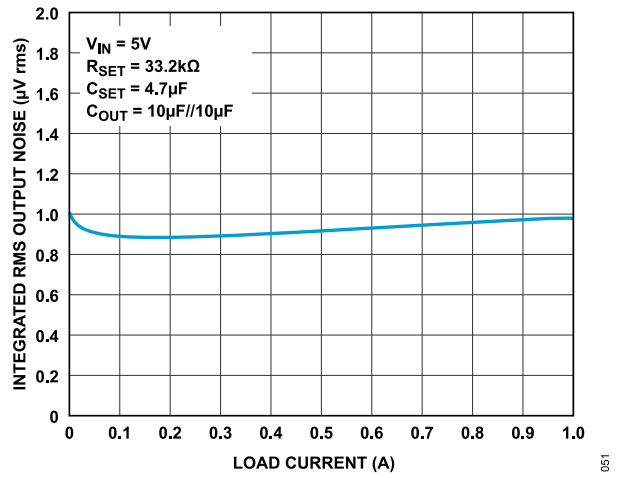



*Figure 51. Integrated RMS Output Noise (10 Hz to 100 kHz) vs. Load Current*

## TYPICAL PERFORMANCE CHARACTERISTICS

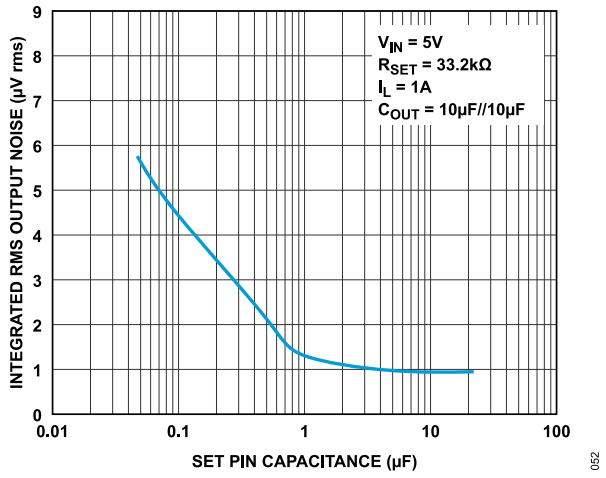



*Figure 52. Integrated RMS Output Noise (10 Hz to 100 kHz) vs. SET Pin Capacitance*

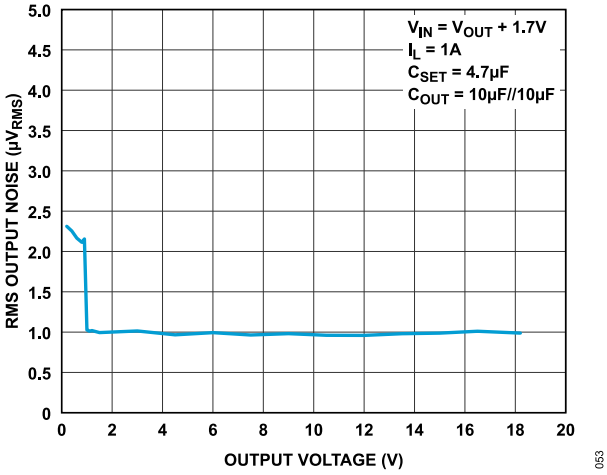



*Figure 53. Integrated RMS Output Noise (10 Hz to 100 kHz) vs. Output Voltage*

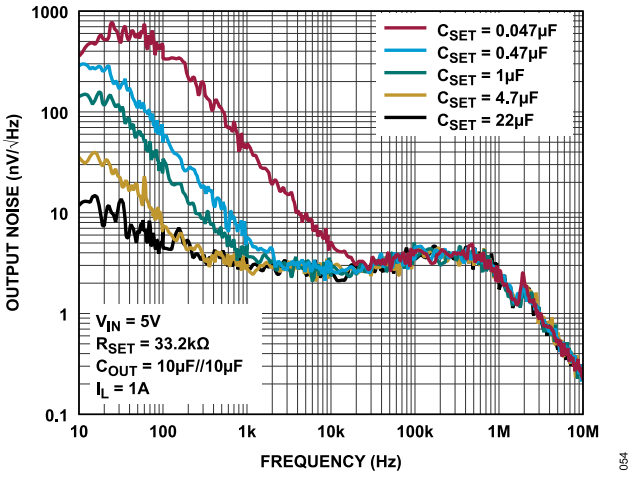



*Figure 54. Output Noise vs. Frequency ($C_{SET}$ Steps)*

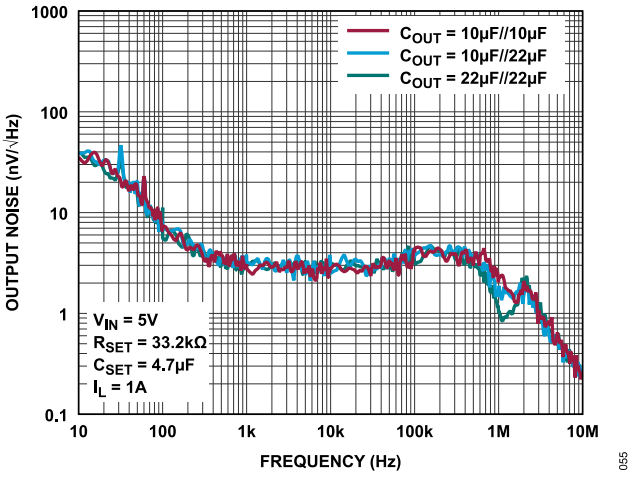



*Figure 55. Output Noise vs. Frequency ($C_{OUT}$ Steps)*

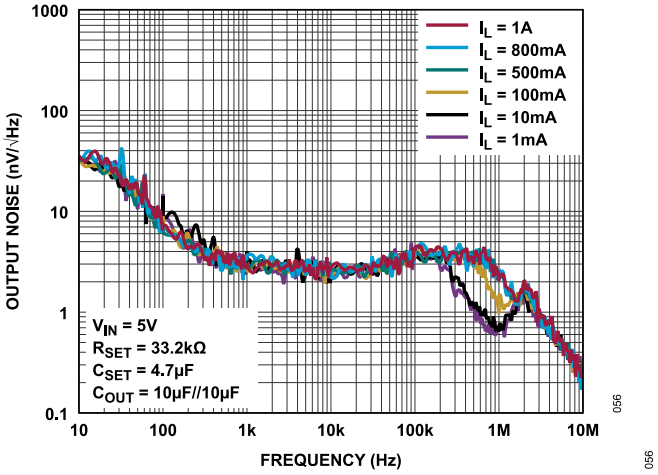



*Figure 56. Output Noise vs. Frequency ($I_L$ Steps)*

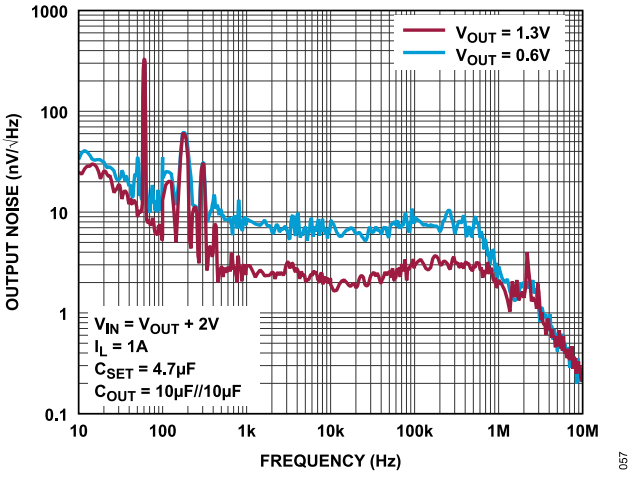



*Figure 57. Output Noise as a Function of an Error-Amplifier Input Pair vs. Frequency*

## TYPICAL PERFORMANCE CHARACTERISTICS

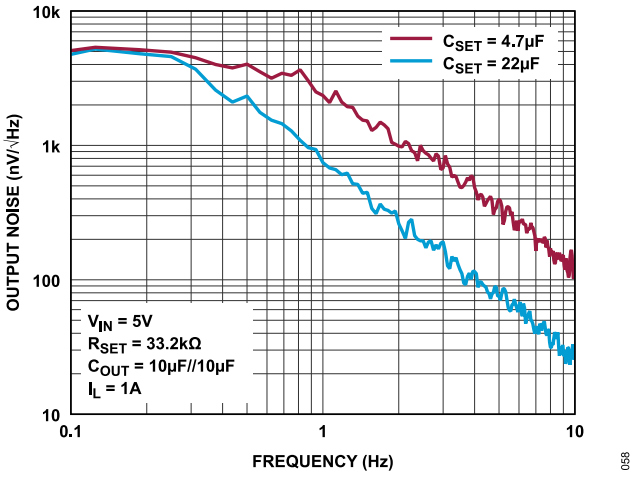



*Figure 58. Output Noise (0.1 Hz to 10 Hz) vs. Frequency*

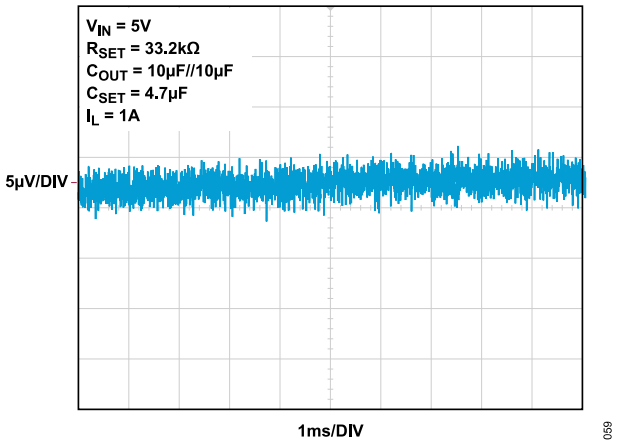



*Figure 59. Output Noise: 10 Hz to 100 kHz*

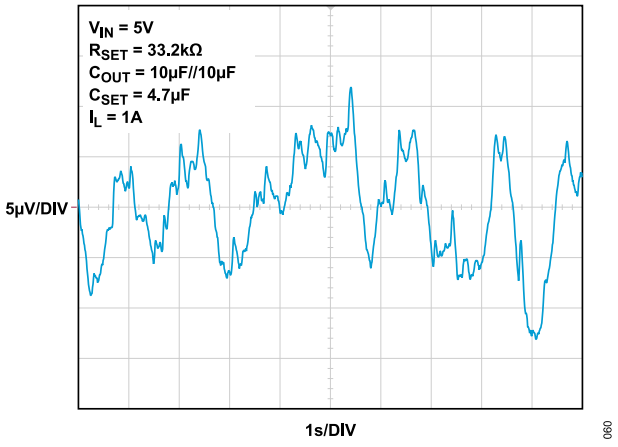



*Figure 60. Output Noise: 0.1 Hz to 10 Hz ($C_{SET}$ = 4.7 µF)*

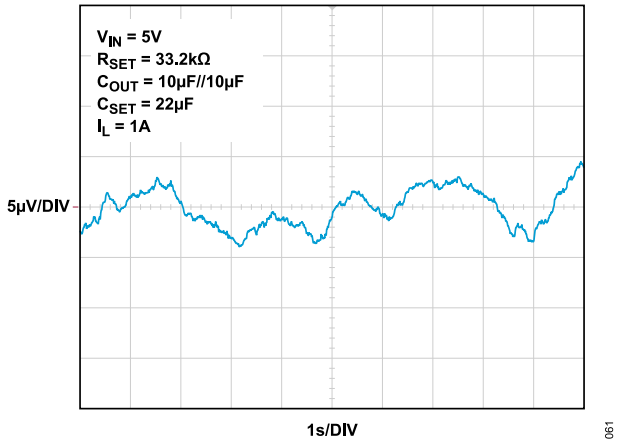



*Figure 61. Output Noise: 0.1 Hz to 10 Hz ($C_{SET}$ = 22 µF)*

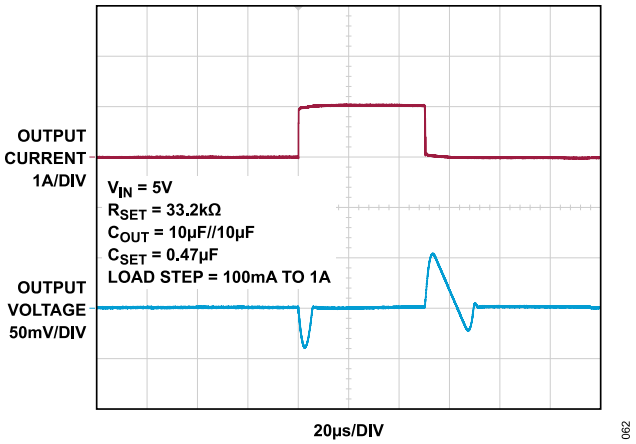



*Figure 62. Load-Transient Response*

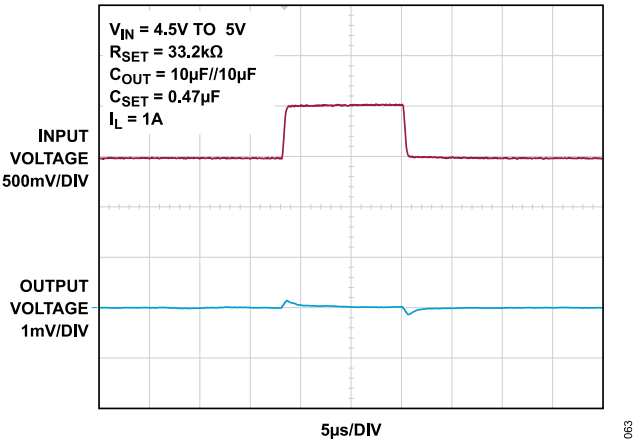



*Figure 63. Line-Transient Response*

## TYPICAL PERFORMANCE CHARACTERISTICS

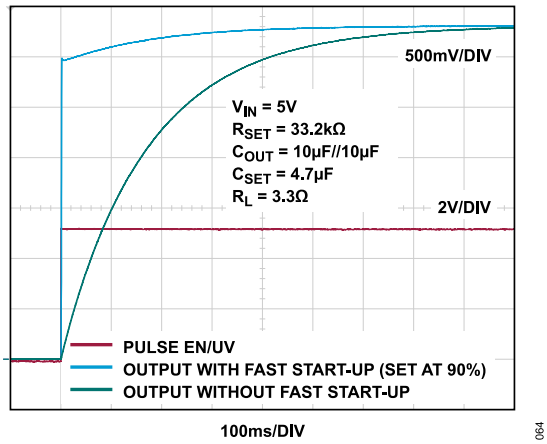



*Figure 64. Start-Up Time with and Without Fast Start-Up Circuitry for Large $C_{SET}$*

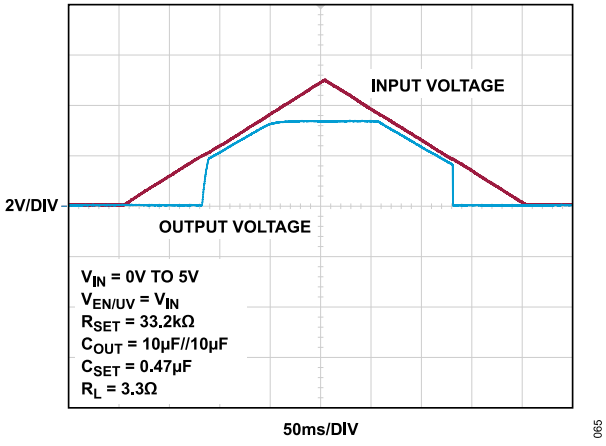



*Figure 65. Input Supply Ramp-Up and Ramp-Down*

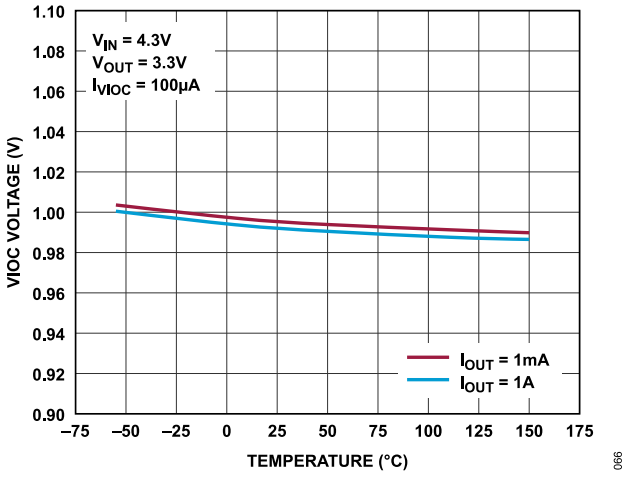



*Figure 66. VIOC Voltage vs. Temperature*

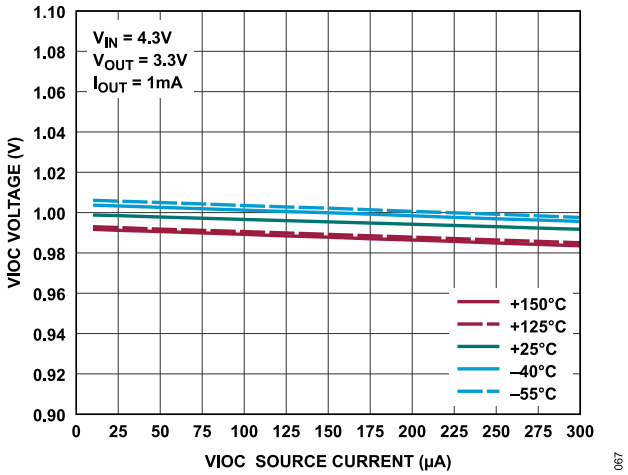



*Figure 67. VIOC Voltage vs. VIOC Source Current*

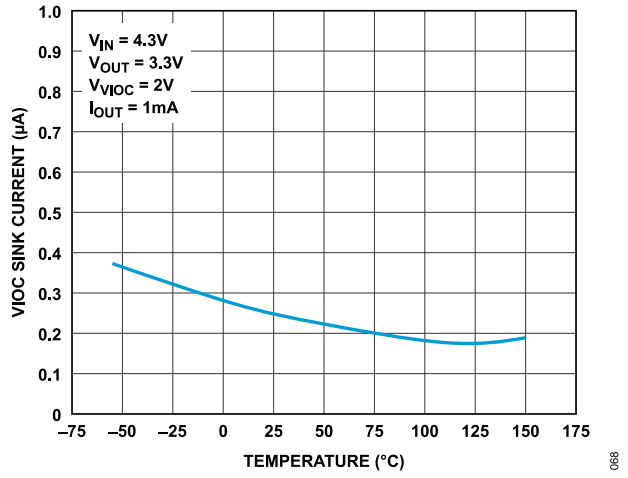



*Figure 68. VIOC Sink Current vs. Temperature*

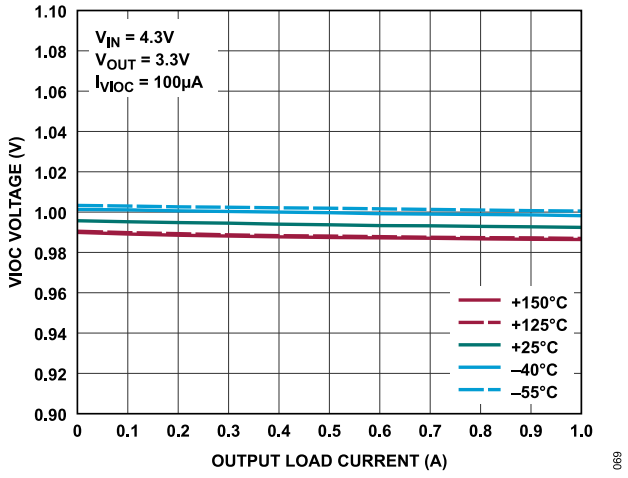



*Figure 69. VIOC Voltage vs. Output Load Current*

## THEORY OF OPERATION

Figure 70 shows the functional block diagram for the LT3041.

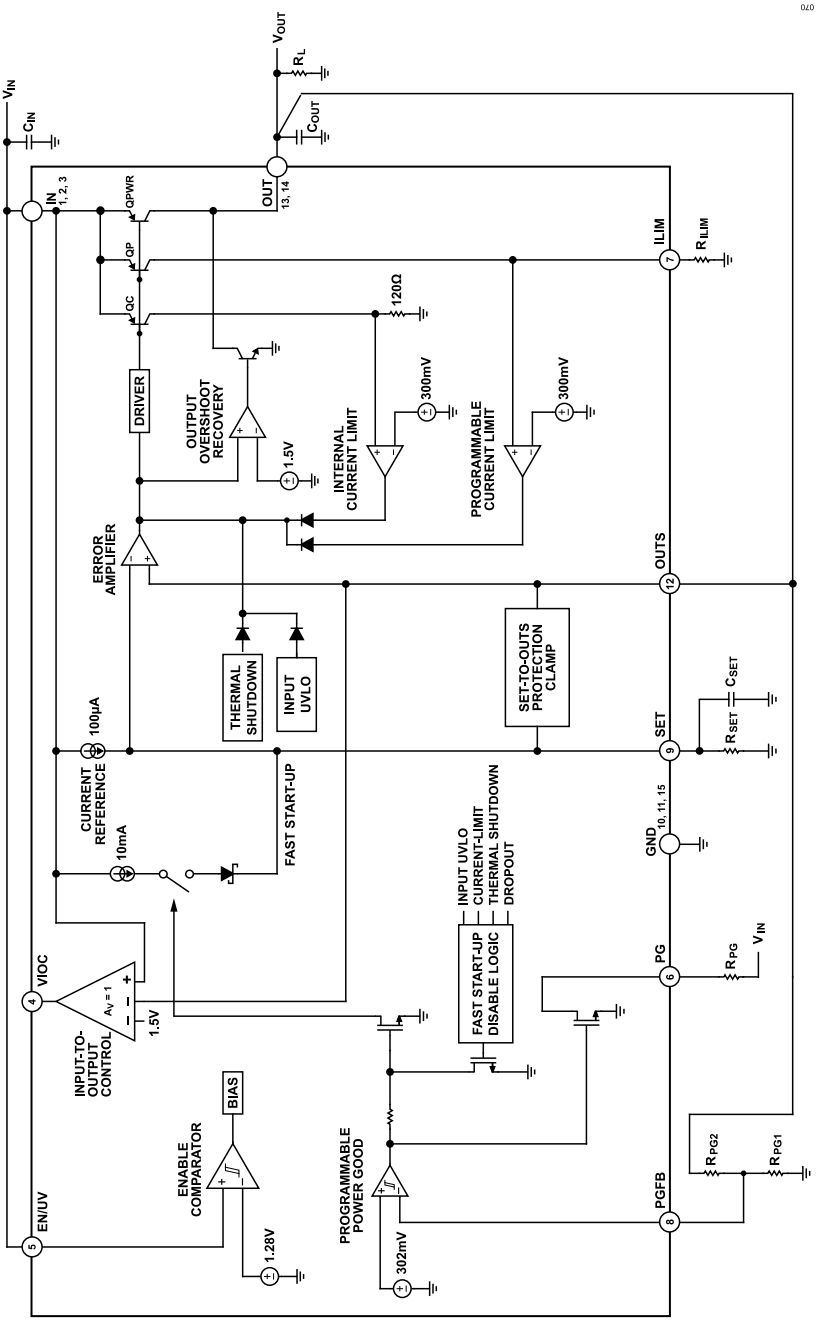



*Figure 70. Functional Block Diagram*

## APPLICATIONS INFORMATION

The LT3041 is a high-performance, low-dropout, linear regulator that features Analog Devices ultra-low noise (3 nV/√Hz at 10 kHz) and ultra-high PSRR (80 dB at 1 MHz) architecture for powering noise-sensitive applications. Designed as a precision-current source followed by a high-performance, rail-to-rail voltage buffer, the LT3041 can be easily paralleled to further reduce noise, increase output current, and spread heat on the PCB. The LT3041 additionally features programmable current limit, a fast start-up capability, and programmable power good.

The LT3041 is simple to use and incorporates all of the protection features expected in high-performance regulators. Included are short-circuit protection, safe-operating area protection, reverse-battery protection, reverse-current protection, and thermal shutdown with hysteresis.

In addition to the LT3041 feature set, the LT3041 incorporates a VIOC tracking function to control an upstream switching converter to maintain a constant voltage across the LT3041 and, therefore, to minimize power dissipation.

### OUTPUT VOLTAGE

The LT3041 incorporates precision 100 µA current source flowing out of the SET pin, which also connects to the inverting input of the error amplifier. Figure 71 illustrates that connecting a resistor from SET to ground generates a reference voltage for the error amplifier. This reference voltage is the product of the SET pin current and the SET pin resistor. The unity-gain configuration of the error amplifier produces a low-impedance version of this voltage on its noninverting input, that is, the OUTS pin, which is externally connected to the OUT pin.

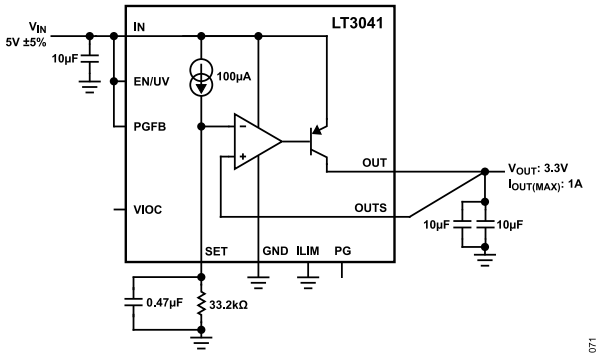



*Figure 71. Basic Adjustable Regulator*

The rail-to-rail error amplifier and current reference of the LT3041 allows for a wide output voltage range from 0.2 V to $V_{IN}$ minus dropout, up to 19 V. A PNP-based input pair is active for a 0.2 V to ~0.95 V output and an NPN-based input pair is active for output voltages greater than ~0.95 V, with an abrupt transition between the two input pairs at ~0.95 V output with approximately 24 mV of hysteresis. While the NPN-based input pair is designed to offer the best overall performance, refer to the Table 1 for details on the offset voltage, SET pin current, output noise, and PSRR variation with the error-amplifier input pair. Table 4 lists many common output voltages and their corresponding 1% $R_{SET}$ resistors. A lower limit of 0.2 V is specified for the PNP-based input pair, rather than 0 V because testing and validation at 0 V are not practical, but $V_{OUT}$ can be set to 0 V and this is guaranteed by design.

*Table 4. 1% Resistor for Common Output Voltages*

| $V_{OUT}$ (V) | $R_{SET}$ (kΩ) |
|---|---|
| 2.5 | 24.9 |
| 3.3 | 33.2 |
| 5 | 49.9 |
| 12 | 121 |
| 15 | 150 |

The benefit of using a current reference compared to the typical voltage reference used in conventional regulators is that the regulator always operates in a unity-gain configuration, independent of the programmed output voltage. This configuration allows the LT3041 to have loop gain, frequency response, and bandwidth independent of the output voltage. As a result, noise, PSRR, and transient performance do not change with output voltage. Moreover, because none of the error-amplifier gain is needed to amplify the SET pin voltage to a higher output voltage, output load regulation is more tightly specified in the hundreds of microvolts range and not as a fixed percentage of the output voltage.

Because the zero temperature-coefficient current source is highly accurate, the SET pin resistor can become a limiting factor in achieving high accuracy. Therefore, the SET pin resistor must be a precision resistor. Additionally, any leakage paths to or from the SET pin create errors in the output voltage. If necessary, use high-quality insulation (for example, Teflon or Kel-F). Moreover, cleaning of all insulating surfaces to remove fluxes and other residues can be required. High humidity environments can require a surface coating at the SET pin to provide a moisture barrier.

Minimize board leakage by encircling the SET pin with a guard ring that operates at a potential close to itself, ideally connected to the OUT pins. Guarding both sides of the circuit board is recommended. Bulk leakage reduction depends on the guard-ring width. Leakages of 100 nA into or out of the SET pin creates a 0.1% error in the reference voltage. Leakages of this magnitude, coupled with other sources of leakage, can cause significant errors in the output voltage, especially over a wide operating temperature range. Figure 72 illustrates a typical guard-ring layout technique.

## APPLICATIONS INFORMATION

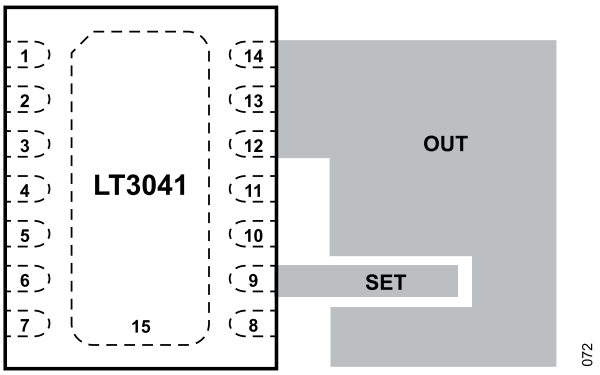



*Figure 72. DFN Guard Ring Layout*

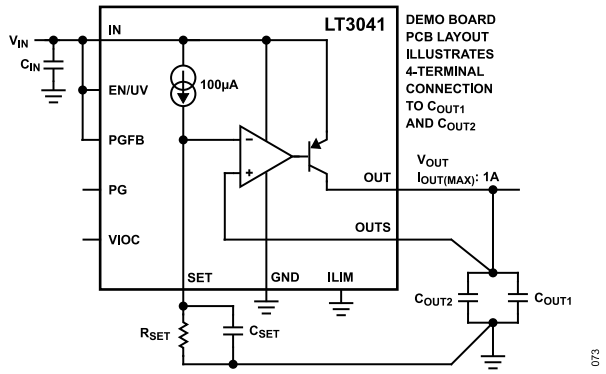



*Figure 73. $C_{OUT1}/C_{OUT2}$ and $C_{SET}$ Connections for Best Performance*

Because the SET pin is a high-impedance node, unwanted signals can couple into the SET pin and cause erratic behavior, which is most noticeable when operating with a minimum output capacitor at heavy load currents. Bypassing the SET pin with a small capacitance to ground resolves this issue, 10 nF is sufficient. For applications requiring higher accuracy or an adjustable output voltage, the SET pin can be actively driven by an external voltage source capable of sinking 100 µA. Connecting a precision-voltage reference to the SET pin eliminates any errors present in the output voltage due to the reference current and SET pin resistor tolerances.

### OUTPUT SENSING AND STABILITY

The OUTS pin of the LT3041 provides a Kelvin-sense connection to the output. The GND side of the SET pin resistor provides a Kelvin-sense connection to the GND side of the load.

Additionally, for ultra-high PSRR, the LT3041 bandwidth is made quite high (~750 kHz), making it close to the self-resonance frequency (~1.6 MHz) of a typical 10 µF (1206 case size), ceramic, output capacitor. Therefore, it is important to avoid adding extra impedance (ESR and ESL) outside the feedback loop. To that end, as shown in Figure 73, minimize the effects of PCB trace and solder inductance by connecting the OUTS pin directly to $C_{OUT1}/C_{OUT2}$ and the GND side of $C_{SET}$ directly to the GND side of $C_{OUT1}/C_{OUT2}$, as well as keep the GND sides of $C_{IN}$ and $C_{OUT1}/C_{OUT2}$ reasonably close. Refer to the LT3041 evaluation board user guide (DC3158A) for more information on the recommended layout that meets these requirements. While the LT3041 is robust enough not to oscillate if the recommended layout is not followed, depending on the actual layout, phase and gain margin, noise and PSRR performance can degrade.

### STABILITY AND OUTPUT CAPACITANCE

The LT3041 requires an output capacitor for stability. Given its high bandwidth, Analog Devices recommends low ESR and ESL ceramic capacitors. A minimum of 20 µF capacitance, preferably two paralleled 10 µF output capacitors with an ESR of less than 20 mΩ and an ESL of less than 2 nH, is required for stability for output voltages less than 7.5 V. For output voltages from 7.5 V to 15 V, use a minimum of 30 µF total output capacitance, preferably a parallel combination of 10 µF and 22 µF with an ESR of less than 20 mΩ and an ESL less than 2 nH. For output voltages greater than 15 V, use a minimum of 40 µF total output capacitance, preferably two paralleled 22 µF capacitors with an ESR of less than 20 mΩ and an ESL less than 2 nH.

Given the high PSRR and low-noise performance attained using a parallel combination of two 10 µF ceramic-output capacitors, larger values of output capacitors are not necessary. However, these capacitors can still improve the performance. Refer to the Typical Performance Characteristics section for additional information. Moreover, larger value output capacitance does decrease peak-output deviations during a load transient. Note that bypass capacitors used to decouple individual components powered by the LT3041 increase the effective-output capacitance.

Give extra consideration to the type of ceramic capacitors used. The capacitors are manufactured with a variety of dielectrics, each with different behaviors across temperature and applied voltage. The most common dielectrics used are specified with Electronic Industries Alliance (EIA) temperature characteristic codes of Z5U, Y5V, X5R, and X7R. The Z5U and Y5V dielectrics are good for providing high capacitance in the small packages, but these dielectrics tend to have stronger voltage and temperature coefficients as shown in Figure 74 and Figure 75. When used with a 5 V regulator, a 16 V, 10 µF Y5V capacitor can exhibit an effective value as low as 1 µF to 3 µF for the DC bias voltage applied over the operating temperature range.

## APPLICATIONS INFORMATION

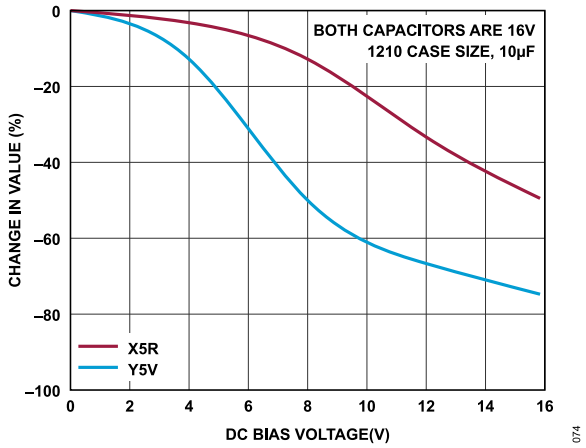



*Figure 74. Ceramic Capacitor DC Bias Characteristics*

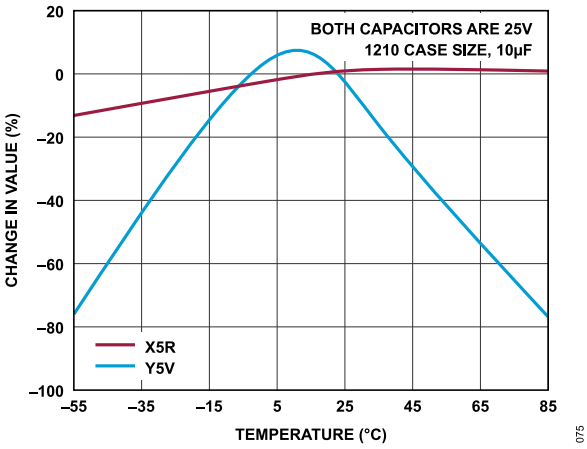



*Figure 75. Ceramic Capacitor Temperature Characteristics*

X5R and X7R dielectrics result in more stable characteristics and are thus more suitable for the LT3041. The X7R dielectric has better stability across temperature, while the X5R is less expensive and is available in higher values. Nonetheless, care must still be exercised when using X5R and X7R capacitors. The X5R and X7R codes only specify operating temperature range and the maximum capacitance change over temperature. While capacitance changes due to DC bias for X5R and X7R is better than Y5V and Z5U dielectrics, it can still be significant enough to drop capacitance to below sufficient levels. As shown in Figure 76, capacitor DC bias characteristics tend to improve as component case size increases. However, verification of expected capacitance at the operating voltage is highly recommended. Due to its good voltage coefficient in small case sizes, Analog Devices recommends using the Murata GCM series ceramic capacitors.

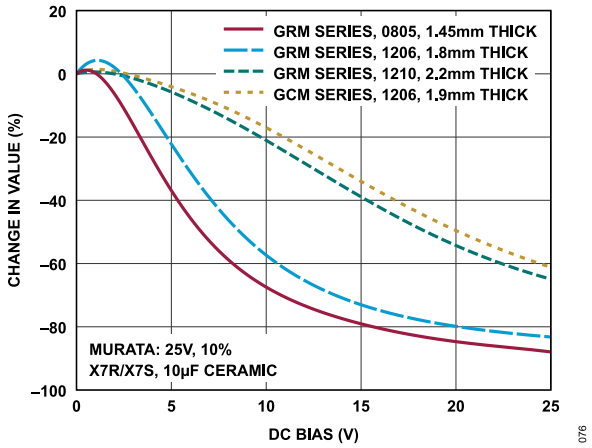



*Figure 76. Capacitor Voltage Coefficient for Different Case Sizes*

### HIGH VIBRATION ENVIRONMENTS

Voltage and temperature coefficients are not the only sources of problems. Some ceramic capacitors have a piezoelectric response. A piezoelectric device generates voltage across its terminals due to mechanical stress, similar to how a piezoelectric microphone works. For a ceramic capacitor, this stress can be induced by mechanical vibrations within the system or due to thermal transients.

LT3041 applications in high-vibration environments have three distinct, piezoelectric noise generators: ceramic output, input, and SET pin capacitors. However, due to the low output impedance over a wide frequency range of the LT3041, negligible output noise is generated using a ceramic-output capacitor. Similarly, due to the ultrahigh PSRR of the LT3041, negligible output noise is generated using a ceramic-input capacitor. Nonetheless, given the high SET pin impedance, any piezoelectric response from a ceramic SET pin capacitor generates significant output noise, peak-to-peak excursions of hundreds of mV. However, due to the high ESR and ESL tolerance of the SET pin capacitor, any nonpiezoelectrically responsive (tantalum, electrolytic, or film) capacitor can be used at the SET pin, although electrolytic capacitors tend to have high 1/f noise. In any case, use of a surface-mount capacitor is highly recommended.

### STABILITY AND INPUT CAPACITANCE

The LT3041 is stable with a minimum 10 µF IN pin capacitor. Analog Devices recommends using low ESR ceramic capacitors. In cases where long wires connect the power supply to the input and ground terminals of the LT3041, the use of low value input capacitors combined with a large load current can result in instability. The resonant LC tank circuit formed by the wire inductance and the input capacitor is the cause of this instability and not the LT3041.

The self-inductance, or isolated inductance, of a wire is directly proportional to its length. The wire diameter, however, has less influence on its self-inductance. For example, the self-inductance of a 2-AWG isolated wire with a diameter of 0.26" is about half the

## APPLICATIONS INFORMATION

inductance of a 30-AWG wire with a diameter of 0.01". One foot of 30-AWG wire has 465 nH of self-inductance.

Several methods exist to reduce the self-inductance of a wire. One method divides the current flowing toward the LT3041 between the two parallel conductors. In this case, placing the wires further apart reduces the inductance; up to a 50% reduction when placed only a few inches apart. Splitting the wires connect two equal inductors in parallel. However, when placed close to each other, their mutual inductance adds to the overall self inductance of the wires; therefore, a 50% reduction is not possible in such cases. The second and more effective technique to reduce the overall inductance is to place the forward and return current conductors (the input and ground wires) close. Two 30-AWG wires separated by 0.02" reduce the overall inductance to about one-fifth of a single wire.

If a battery mounted close powers the LT3041, a 10 µF input capacitor suffices for stability. However, if a distantly located supply powers the LT3041, use a larger value input capacitor. Use a rough guideline of 1 µF (in addition to the 10 µF minimum) per 6" of wire length. The minimum input capacitance required to stabilize the application also varies with the output capacitance as well as the load current. Place additional capacitance on the output of the LT3041 to help this issue. However, the additional capacitance requires significantly more capacitance compared to additional input bypassing. Series resistance between the supply and the input of the LT3041 also helps stabilize the application; as little as 0.1 Ω to 0.5 Ω suffices. This impedance dampens the LC tank circuit at the expense of the dropout voltage. A better alternative is to use a higher ESR tantalum or electrolytic capacitor at the input of the LT3041 in parallel with a 10 µF ceramic capacitor.

### PSRR AND INPUT CAPACITANCE

For applications using the LT3041 for post-regulating switching converters, placing a capacitor directly at the input of the LT3041 results in AC current (at the switching frequency) to flow near the LT3041. This relatively high-frequency switching current generates a magnetic field that couples to the output of the LT3041, degrading its effective PSRR. While highly dependent on the PCB, the switching preregulator, and the input capacitance, among other factors, the PSRR degradation can be easily more than 30 dB at 1 MHz. This degradation is present even if the LT3041 is desoldered from the board because it effectively degrades the PSRR of the PCB itself. While negligible for conventional, low PSRR, LDO regulators, the ultra-high PSRR of the LT3041 requires careful attention to higher order parasitics to extract the full performance offered by the regulator.

To mitigate the flow of the high-frequency switching current near the LT3041, as long as the output capacitor of the switching converter is located more than an inch away from the LT3041, remove the input capacitor of the LT3041. Magnetic coupling rapidly decreases with increasing distance. Nonetheless, if the switching preregulator is placed too far away (conservatively more than a couple inches) from the LT3041, with no input capacitor present, as with any regulator, the input of the LT3041 oscillates at the parasitic LC resonance frequency. In addition, it is generally a common (and a preferred) practice to bypass the regulator input with some capacitance. Therefore, this option is fairly limited in its scope and not the most palatable solution.

To that end, Analog Devices recommends using the LT3041 demonstration board layout for achieving the best possible PSRR performance (see the DC3158A user guide). The LT3041 evaluation board layout uses magnetic-field cancellation techniques to prevent PSRR degradation caused by this high-frequency current flow, while using the input capacitor.

### FILTERING HIGH-FREQUENCY SPIKES

For applications where the LT3041 is used to post regulate a switching converter, its high PSRR effectively suppresses any noise present at the switching frequency of the switching converter, typically 100 kHz to 4 MHz. However, the high-frequency (hundreds of MHz) spikes, beyond the bandwidth of the LT3041, associated with the power-switch transition times of the switching converter almost directly pass through the LT3041. While the output capacitor is intended partly to absorb these spikes, its ESL limits its ability at these frequencies. A ferrite bead or even the inductance associated with a short (for example, 0.5”) PCB trace between the output of the switching converter and the input of the LT3041 can serve as an LC filter to suppress these high-frequency spikes.

### OUTPUT NOISE

The LT3041 offers many advantages with respect to noise performance. Traditional linear regulators have several sources of noise. The most critical noise sources for a traditional regulator are its voltage reference, error amplifier, noise from the resistor-divider network used for setting the output voltage, and the noise gain created by this resistor-divider. Many low-noise regulators pin out their voltage reference to allow for noise reduction by bypassing the reference voltage.

Unlike most linear regulators, the LT3041 does not use a voltage reference. Instead, the LT3041 uses a 100 µA current reference. The current reference operates with a typical noise-current level of 20 pA/√Hz (6 nA rms over a 10 Hz to 100 kHz bandwidth). The resultant voltage noise equals the current noise multiplied by the resistor value, which, in turn, is RMS summed with the noise of the error amplifier and the thermal noise of the resistor, √4kTR, where k = Boltzmann’s constant ($1.380649 \times 10^{-23}$J/K), and T is the absolute temperature.

One problem that conventional linear regulators face is that the resistor-divider setting the output voltage gains up the reference noise. In contrast, the unity-gain follower architecture of the LT3041 presents no gain from the SET pin to the output. Therefore, if a capacitor bypasses the SET pin resistor, the output noise is independent of the programmed output voltage. The resultant output noise is then set just by the noise of the error amplifier, typically

## APPLICATIONS INFORMATION

3 nV/√Hz from a 10 kHz to 1 MHz bandwidth and 1 µV rms from a 10 Hz to 100 kHz bandwidth using a 4.7 µF SET pin capacitor. Paralleling multiple LT3041 devices further reduces noise by √N, for N parallel regulators.

Refer to the Figure 51, Figure 52, Figure 54, Figure 56, and Figure 58 for the noise spectral density (for the 10 Hz to 10 MHz frequency range and for the 0.1 Hz to 10 Hz 1/f noise frequency range) and RMS integrated noise over various load currents and SET pin capacitance information.

### SET PIN (BYPASS) CAPACITANCE: NOISE, PSRR, TRANSIENT RESPONSE, AND SOFT-START

In addition to reducing output noise, using a SET pin bypass capacitor also improves PSRR and transient performance. Note that any bypass-capacitor leakage deteriorates the DC regulation of the LT3041. Capacitor leakage of even 100 nA is a 0.1% DC error. Therefore, Analog Devices recommends the use of a good quality, low-leakage ceramic capacitor.

Using a SET pin bypass capacitor also soft starts the output and limits inrush current. The RC time constant, formed by the SET pin resistor and capacitor, controls the soft-start time. The ramp-up rate from 0% to 90% of nominal VOUT is the following:

$$t_{SS} \approx 2.3 \times R_{SET} \times C_{SET} \quad (Fast \quad Start-Up \quad Disabled) \tag{1}$$

### FAST STARTUP

For ultra-low noise applications that require low 1/f noise (that is, at frequencies below 100 Hz), a larger value, SET pin capacitor is required of up to 22 µF. Typically, this larger value significantly increases the start-up time of the regulator. However, the LT3041 incorporates fast start-up circuitry that increases the SET pin current to approximately 10 mA during startup.

As shown in the Figure 70, the 10 mA current source remains engaged while PGFB is less than 302 mV, unless the regulator is in current limit, dropout, thermal shutdown, or the input voltage is less than the minimum $V_{IN}$.

If the fast start-up capability is not used, connect PGFB to IN or to OUT for output voltages more than 302 mV, and note that this also disables the power-good functionality.

### EN/UV

The EN/UV pin is used to put the regulator into a micropower shutdown state. The LT3041 has an accurate 1.28 V turn-on threshold on the EN/UV pin with 110 mV of hysteresis. This threshold can be used with a resistor-divider from the input supply to define an accurate UVLO threshold for the regulator. The EN/UV pin current ($I_{EN/UV}$) at the threshold from Table 1 must be considered when calculating the resistor-divider network as follows:

$$V_{IN\,(UVLO)} = 1.28 \quad V \times \left(1 + \frac{R_{EN2}}{R_{EN1}}\right) + I_{EN/UV} \times R_{EN2} \tag{2}$$

where:
$R_{EN1}$ and $R_{EN2}$ are the resistors from the EN/UV pin to GND and the EN/UV pin to IN, respectively.
$I_{EN/UV}$ can be ignored if $R_{EN1}$ is less than 100 kΩ. If unused, connect the EN/UV pin to IN.

### PROGRAMMABLE POWER GOOD

As illustrated in the Figure 70, the power-good threshold is user-programmable using the ratio of two external resistors, $R_{PG2}$ and $R_{PG1}$:

$$V_{OUT(PG\_THRESHOLD)} = 0.302V \times \left(1 + \frac{R_{PG2}}{R_{PG1}}\right) + I_{PGFB} \times R_{PG2} \tag{3}$$

If the PGFB pin increases to more than 302 mV, the open-drain PG pin deasserts and becomes high impedance. The power-good comparator has 7 mV hysteresis and 20 µs of deglitching. The $I_{PGFB}$ from Table 1 must be considered when determining the resistor-divider network. The $I_{PGFB}$ can be ignored if $R_{PG1}$ is less than 30 kΩ. If the power-good functionality is not used, float the PG pin. Note that programmable power good and fast start-up capabilities are disabled for output voltages less than 302 mV.

### EXTERNALLY PROGRAMMABLE CURRENT LIMIT

The current-limit threshold of the ILIM pin is 300 mV. Connecting a resistor from ILIM to GND sets the maximum current flowing out of the ILIM pin, which, in turn, programs the current limit of the LT3041. With a 150 mA × kΩ programming scale factor, calculate the current limit as follows:

$$Current \quad Limit = \frac{150 \quad mA \times k\Omega}{R_{ILIM}} \tag{4}$$

For example, a 150 Ω resistor programs the current limit to 1 A and a 200 Ω resistor programs the current limit to 750 mA. For good accuracy, Kelvin connect this resistor to the GND pin of the LT3041.

When IN-to-OUT differential is greater than 11 V, the foldback circuitry of the LT3041 decreases the internal current limit. As a result, internal current limit can override the externally programmed current-limit level to keep the LT3041 within its safe-operating area (SOA). See Figure 32.

As shown in the Figure 70, the ILIM pin sources current proportional (1:500) to the output current; therefore, it also serves as a current monitoring pin with a 0 V to 300 mV range. If external current limit or current monitoring is not used, connect ILIM to GND.

### OUTPUT OVERSHOOT RECOVERY

During a load-step change from full load to no load (or light load), the output voltage overshoots before the regulator responds to turn

## APPLICATIONS INFORMATION

the power transistor off. Given that there is no load (or a light load) present at the output, it takes a long time to discharge the output capacitor.

As illustrated in the Figure 70, the LT3041 incorporates an overshoot recovery circuitry that turns on a current sink to discharge the output capacitor in the event OUTS is higher than SET. This current is typically about 5 mA. No load recovery is disabled for input voltages less than 2.5 V or output voltages less than 1.5 V.

If OUTS is externally held more than SET, the current sink turns on in an attempt to restore OUTS to its programmed voltage. The current sink remains on until the external circuitry releases OUTS.

### DIRECT PARALLELING FOR HIGHER CURRENT

Higher output current is obtained by paralleling multiple LT3041 devices. Connect all SET pins together and all IN pins together. Connect the OUT pins together using small pieces of PCB trace (used as a ballast resistor) to equalize currents in the LT3041 devices. PCB trace resistance in milliohms per inch is shown in Table 5.

*Table 5. PCB Trace Resistance (Measured in mΩ per Inch)*

| Weight (oz) | 10 mil Width | 20 mil Width |
|---|---|---|
| 1 | 54.3 | 27.1 |
| 2 | 27.1 | 13.6 |

The small worst-case offset of 2 mV for each paralleled LT3041 minimizes the required ballast resistor value. Figure 77 illustrates that two LT3041 devices, each using a 10 mΩ PCB trace ballast resistor, providing better than 20% accurate output current sharing at full load. The two 10 mΩ external resistors only add 10 mV of output regulation drop with a 2 A maximum current. With a 3.3 V output, this voltage drop only adds 0.3% to the regulation accuracy. As was discussed previously, connect the OUTS pin directly to the output capacitor.

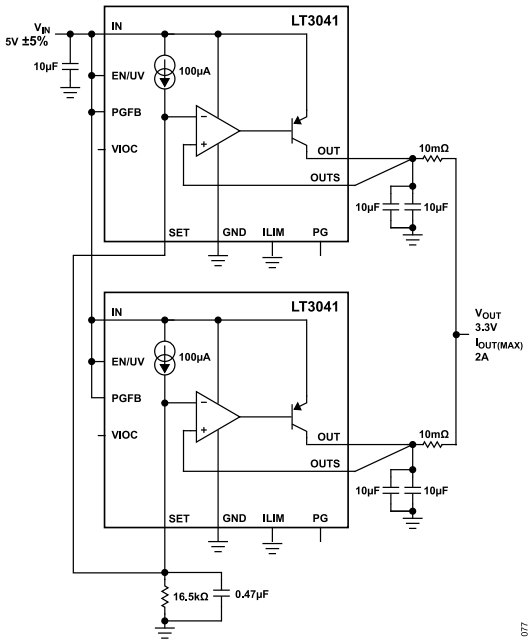



*Figure 77. Parallel Devices*

In addition, more than two LT3041 devices can be paralleled for even higher output current and lower output noise. Paralleling multiple LT3041 devices is also useful for distributing heat on the PCB. For applications with high input-to-output voltage differential, an input series resistor or resistor in parallel with the LT3041 can also be used to spread heat.

### PCB LAYOUT CONSIDERATIONS

Given the high bandwidth and ultra-high PSRR of the LT3041, careful PCB layout must be employed to achieve full device performance. Figure 78 shows a recommended layout that delivers full performance of the regulator. Refer to the LT3041 evaluation board user guide (DC3158A) for further details.

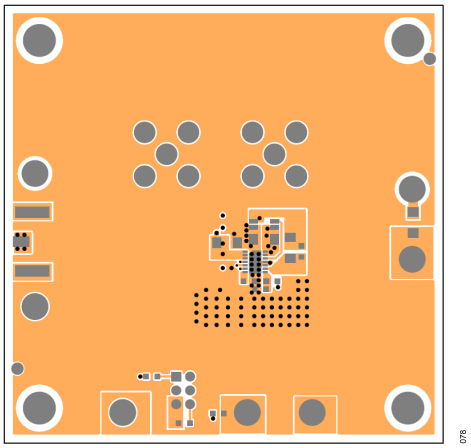



*Figure 78. Recommended Layout*

## APPLICATIONS INFORMATION

### HIGH-EFFICIENCY LINEAR REGULATOR: VOLTAGE INPUT-TO-OUTPUT CONTROL (VIOC)

The VIOC pin controls an upstream switching converter (for example, buck, boost, or buck-boost) to maintain a constant voltage across the LT3041, regardless of the output voltage of the LDO regulator. This constant voltage maximizes efficiency while maintaining PSRR performance. The VIOC pin is the output of a fast unity-gain amplifier that regulates the IN voltage to a voltage that is a fixed offset above the higher of OUT or 1.5 V. As shown in Figure 79, the VIOC feature is simple to use. Connect the VIOC pin to the feedback (FB) pin of the upstream switching converter ($V_{FBSWITCHER}$), which regulates the input-to-output differential of the LT3041 to the feedback voltage of the switching converter. When paralleling multiple LT3041 devices, connect the VIOC pin of one of the LT3041 devices to the feedback pin of the upstream switching converter and float the remaining VIOC pins.

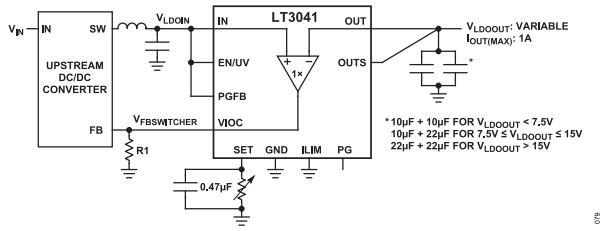



*Figure 79. VIOC Basic Operation ($V_{LDOIN}$ Is the LDO Input Voltage, and $V_{LDOOUT}$ Is the LDO Output Voltage.)*

While the VIOC buffer is inside the feedback loop of the switching converter, given the high bandwidth of the VIOC buffer, the frequency compensation of the switching converter does not need adjustment. Phase delay through the VIOC buffer is typically less than 2° for frequencies as high as 100 kHz. Therefore, within the bandwidth (usually much less than 100 kHz) of the switching converter, the VIOC buffer is transparent and acts like an ideal wire.

For example, for a switching converter with less than 100 kHz bandwidth and a phase margin of 50°, using the VIOC buffer, the phase margin degrades by at most 2°. Hence, the phase margin for the switching converter (using the VIOC pin) is at least 48°. Given that the VIOC buffer is inside the feedback loop of the switching converter, the total capacitance on the VIOC pin must be less than 20 pF.

As shown in Figure 80, the input-to-output differential voltage is easily programmable to support different application needs (PSRR vs. power dissipation) by using the following equation:

$$V_{LDOIN} - V_{LDOOUT} = V_{VIOC} = V_{FBSWITCHER} \times \frac{R1 + R2}{R1} \quad (5)$$

where:
*R1* is the resistance from the switching converter FB pin to ground.
*R2* is the resistance from the switching converter FB pin to the VIOC pin.

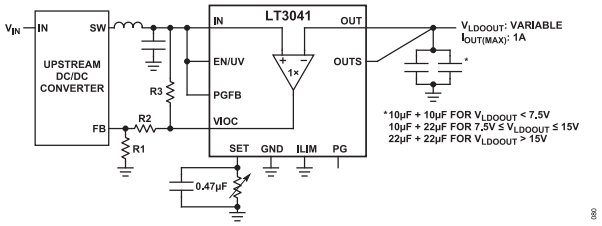



*Figure 80. Programming Input-to-Output Differential*

Furthermore, in the event that the LT3041 SET pin opens up, the LT3041 input voltage can rise up to the input voltage of the switching converter, and thus, potentially violate the Absolute Maximum Ratings of the LT3041. To prevent this violation, set the maximum LT3041 input voltage by using a resistor (R3) between the VIOC and IN pins of the regulator such that:

$$V_{(MAX)LDOIN} = V_{FBSWITCHER} \times \frac{R1 + R2 + R3}{R1} + I_{SINK} \times R3 \quad (6)$$

where $I_{SINK}$ is the sink current.

Moreover, the VIOC pin is capable of sourcing 300 µA and sinking 2 µA of current. To mitigate the effect of the sink current on the maximum LDO input voltage, choose R1 such that the resistor-divider typically runs at least 100 µA.

For $V_{OUT}$ > 1.5 V, $V_{IN}$ = $V_{OUT}$ + $V_{VIOC}$. The VIOC pin voltage (and hence the input-to-output differential) can be programmed anywhere between a minimum of 1 V and a maximum of 4 V or $V_{OUT}$ – 0.5 V (for $V_{OUT}$ > 1.5 V), or whichever is lower. For applications where the feedback pin of the switching regulator is less than 1 V, use the R1 and R2 resistors to make sure that the VIOC pin is within the previously mentioned range. Note that the VIOC pin voltage cannot be programmed to less than the feedback pin of the upstream switching converter. For $V_{OUT}$ ≤ 1.5 V, the VIOC programming range is 1 V ± 5%. If VIOC is set outside of this range, the input voltage of the LT3041 rises to the maximum value set using R3. If VIOC functionality is not used, float the VIOC pin.

Because the maximum VIOC programming voltage is dependent on $V_{OUT}$, care must be taken in setting the VIOC voltage. For instance, if VIOC is set to 1 V, the IN-to-OUT differential of the LT3041 regulates to 1 V for a $V_{OUT}$ > 1.5 V. Similarly, if VIOC is set to 2 V, the IN-to-OUT differential of the regulator regulates to 2 V for a $V_{OUT}$ > 2.5 V (that is, $V_{VIOC}$ + 0.5 V). However, if the output voltage is less than 2.5 V, for this example, the LDO regulator is not able to drive its VIOC pin to the right level of 2 V. As a result, the output of the upstream preregulator rises, causing the input voltage of the LT3041 to rise to the maximum voltage set using R3. Therefore, for protection under various fault conditions, the use of R3 to set the maximum $V_{IN}$ voltage (less than 20 V) is required and a programmed VIOC voltage of 1 V ± 5% is highly recommended.

## APPLICATIONS INFORMATION

### TYPICAL VIOC APPLICATION

Figure 81 shows a typical VIOC application used to post regulate the output of the buck converter of the LT8608. The VIOC voltage is set at 1 V with the maximum LDO input voltage set to 15.5 V. Figure 82 shows the input and output voltage of the LDO regulator when pulsing the EN/UV pin of the LT3041, and as can be seen, when the LDO regulator is disabled, the LDO input voltage goes to the maximum input voltage set by the resistor-divider on the VIOC pin. Figure 83 shows the load-step response of the LT8608 using the VIOC buffer. Figure 84 shows the input and output-voltage response of the LDO regulator to stepping the SET pin from 3 V to 4 V. Figure 85 shows the output and input voltage of the LDO regulator while ramping the SET pin from 0 V to 10 V, and as can be seen, the output voltage of the LT8608 tracks the output voltage of the LT3041 when it is greater than 1.5 V. Lastly, Figure 86 shows the noise spectral density at the input and output of the LT3041.

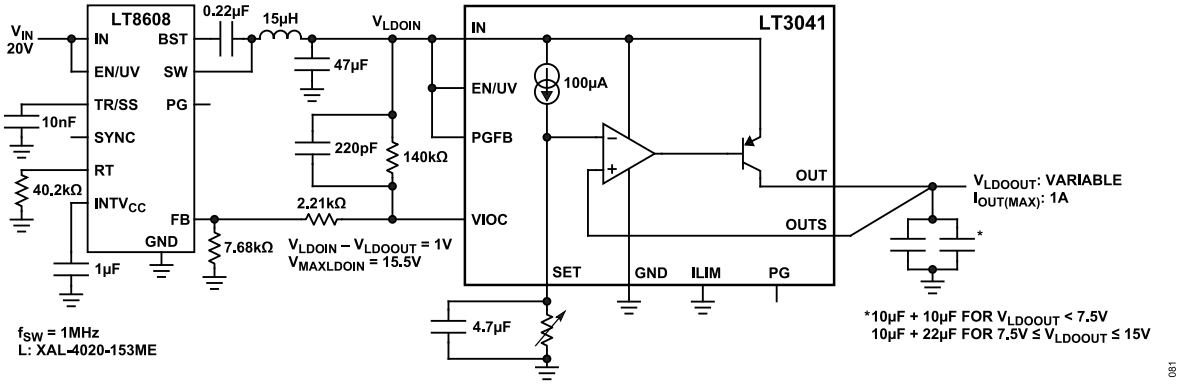



*Figure 81. Typical LT3041 Post-Regulating Application*

## APPLICATIONS INFORMATION

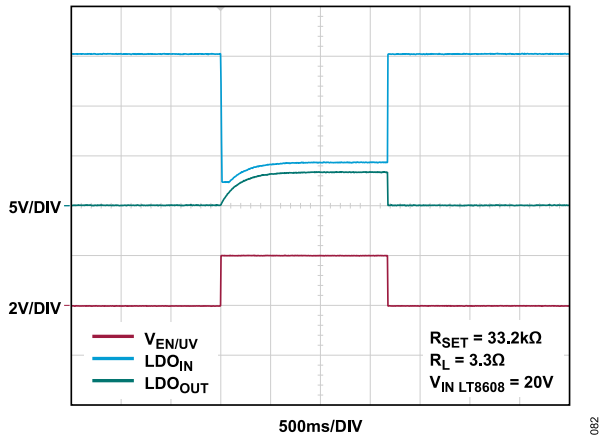



*Figure 82. EN/UV Pulse ($LDO_{IN}$ Is the Input of the LDO Regulator, and $LDO_{OUT}$ Is the Output of the LDO Regulator.)*

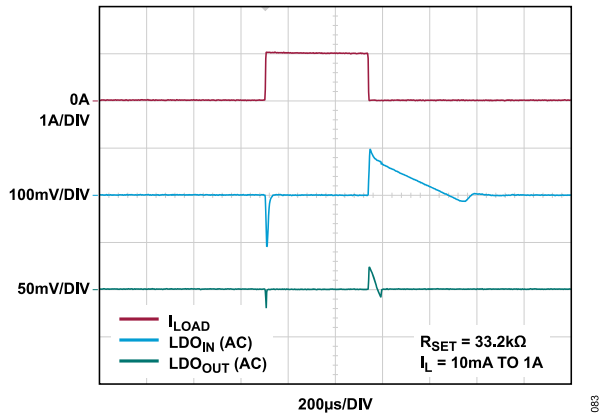



*Figure 83. Load-Step Response Using the VIOC Buffer*

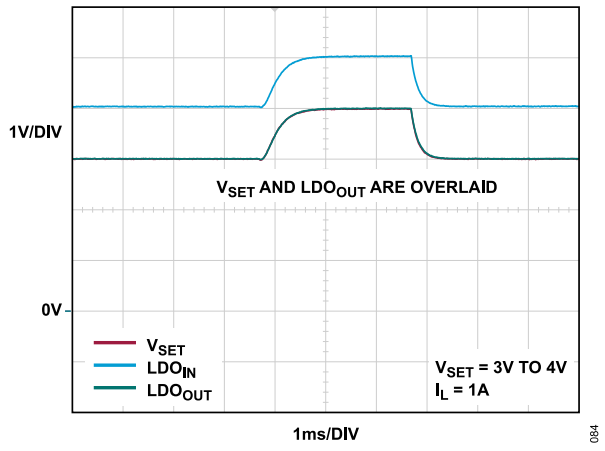



*Figure 84. Stepping $V_{SET}$ from 3 V to 4 V (and Back to 3 V)*

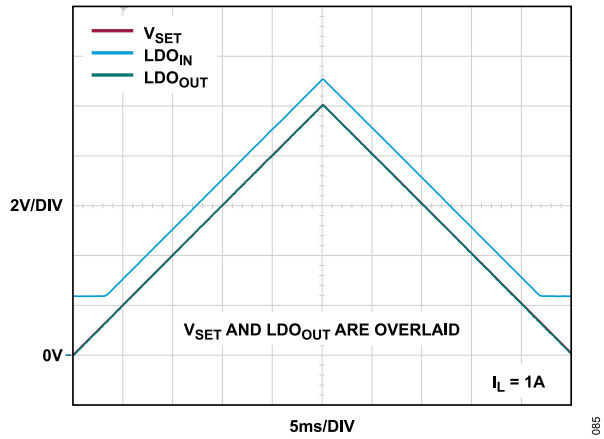



*Figure 85. Ramping $V_{SET}$ from 0 V to 10 V (and Back to 0 V)*

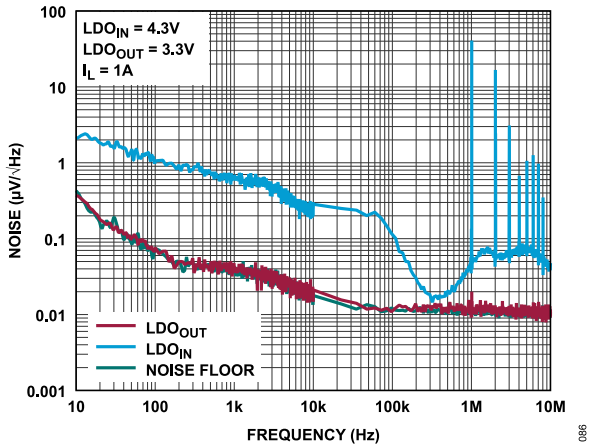



*Figure 86. Input and Output Noise Spectral Density of the LT3041*

## THERMAL CONSIDERATIONS

The LT3041 has internal power and thermal limiting circuits that protect the device under overload conditions. The thermal shutdown temperature is nominally 169°C with about 5°C of hysteresis. For continuous normal load conditions, do not exceed the maximum junction temperature, 125°C. It is important to consider all sources of thermal resistance from junction to ambient, which includes junction to case, case to heatsink interface, heatsink resistance, or circuit board to ambient as the application dictates. Additionally, consider all heat sources close to the LT3041.

The underside of the DFN package has exposed metal from the lead frame to the die attachment. This package allows heat to directly transfer from the die junction to the PCB metal to limit maximum operating junction temperature. The dual, inline pin arrangement allows metal to extend beyond the ends of the package on the topside (component side) of the PCB.

For surface-mount devices, heat sinking is accomplished by using the heat spreading capabilities of the PCB and its copper traces. Copper board stiffeners and plated throughholes can also be used to spread the heat generated by the LDO regulator.

## APPLICATIONS INFORMATION

Table 6 lists the thermal resistance as a function of the copper area on a fixed board size. All measurements were taken in still air on a 4 layer FR4 board with 1 oz solid internal planes and 2 oz top and bottom planes with a total board thickness of 1.6 mm. The four layers were electrically isolated with no thermal vias present. PCB layers, copper weight, board layout, and thermal vias affect the resultant thermal resistance. For more information on thermal resistance and high thermal conductivity test boards, refer to JEDEC standard JESD-51, JESD51-7, and JESD51-12. Achieving low thermal resistance necessitates careful PCB layout.

***Table 6. Measured Thermal Resistance for DFN Package***

| Copper Area | | | Junction-to-Ambient Thermal Resistance |
|---|---|---|---|
| Top Side[1] | Bottom Side | Board Area | |
| 2500 mm$^2$ | 2500 mm$^2$ | 2500 mm$^2$ | 34°C/W |
| 1000 mm$^2$ | 2500 mm$^2$ | 2500 mm$^2$ | 34°C/W |
| 225 mm$^2$ | 2500 mm$^2$ | 2500 mm$^2$ | 36°C/W |
| 100 mm$^2$ | 2500 mm$^2$ | 2500 mm$^2$ | 37°C/W |

[1] The device is mounted on the topside.

### CALCULATING JUNCTION TEMPERATURE

For example, given an output voltage of 3.3 V, an input voltage of 5 V ± 5%, an output current range from 1 mA to 1 A, and a maximum ambient temperature of 50°C, what is the maximum junction temperature?

The power dissipation of the LT3041 is the following:

$$I_{OUT(MAX)} \times \left(V_{IN(MAX)} - V_{OUT}\right) + I_{GND} \times V_{IN(MAX)} \quad (7)$$

where:
$I_{OUT(MAX)}$ = 1 A.
$V_{IN(MAX)}$ = 5.25 V.
$I_{GND}$ (at $I_{OUT}$ = 1 A and $V_{IN}$ = 5.25 V) = 27 mA.

Therefore, $P_{DISS}$ = 1 A × (5.25 V − 3.3 V) + 27 mA × 5.25 V = 2.1 W.

Using a DFN package, the thermal resistance is in the range of 34°C/W to 37°C/W depending on the copper area. Therefore, the junction temperature rise above ambient approximately equals 2.1 W × 35°C/W = 73.5°C.

The maximum junction temperature equals the maximum ambient temperature plus the maximum junction temperature rise above ambient, which calculates as follows:

$$T_{JMAX} = 50°C + 73.5°C = 123.5°C \quad (8)$$

### OVERLOAD RECOVERY

Like many IC power regulators, the LT3041 incorporates SOA protection. The SOA protection activates at input-to-output differential voltages greater than 11 V. The SOA protection decreases the current limit because the input-to-output differential increases and keeps the power transistor inside a safe operating region for all values of input-to-output voltages up to the Absolute Maximum Ratings of the LT3041. The LT3041 provides some level of output current for all values of input-to-output differentials. Refer to the Figure 32. When power is first applied and input voltage rises, the output follows the input and keeps the input-to-output differential low to allow the LDO regulator to supply the large output current and startup into high-current loads.

Due to current-limit foldback, however, at high-input voltages, a problem can occur if the output voltage is low, and the load current is high. Such situations occur after the removal of a short-circuit or if the EN/UV pin is pulled high after the input voltage is already turned on. The load-line in such cases intersects the output-current profile at two points. The regulator now has two stable operating points. With this double intersection, the input-power supply may need to be cycled down to zero and brought back up again to result in the output recover. Other LDO regulators with foldback current-limit protection (such as the LT1965 and LT1963A) also exhibit this phenomenon; therefore, it is not unique to the LT3041.

### PROTECTION FEATURES

The LT3041 incorporates several protection features for battery-powered applications. Precision current-limit and thermal-overload protection protect the LT3041 against overload and fault conditions at the output of the device. For normal operation, do not allow the junction temperature to exceed 125°C.

To protect the low-noise error amplifier of the LT3041, the SET-to-OUTS protection clamp limits the maximum voltage between SET and OUTS with a maximum DC current of 20 mA through the clamp. Therefore, for applications where SET is actively driven by a voltage source, the voltage source must be current limited to 20 mA or less. Moreover, to limit the transient current flowing through these clamps during a transient fault condition, limit the maximum value of the SET pin capacitor ($C_{SET}$) to 22 µF.

The LT3041 also incorporates reverse-input protection whereby the IN pin withstands reverse voltages of up to –20 V without causing any input-current flow and without developing negative voltages at the OUT pin. The regulator protects both itself and the load against batteries that are plugged in backwards.

In circuits where a backup battery is required, several different input and output conditions can occur. The output voltage can be held up while the input is either pulled to GND, pulled to some intermediate voltage, or left open-circuit. In all cases, the reverse-current protection circuitry prevents current flow from the output to the input. Nonetheless, due to the OUTS-to-SET clamp, unless the SET pin is floating, current can flow to GND through the SET pin resistor as well as up to 15 mA to GND through the output overshoot recovery circuitry. This current flow through the output overshoot recovery circuitry can be significantly reduced by placing a Schottky diode between the OUTS and SET pins, with its anode at the OUTS pin.

## TYPICAL APPLICATIONS

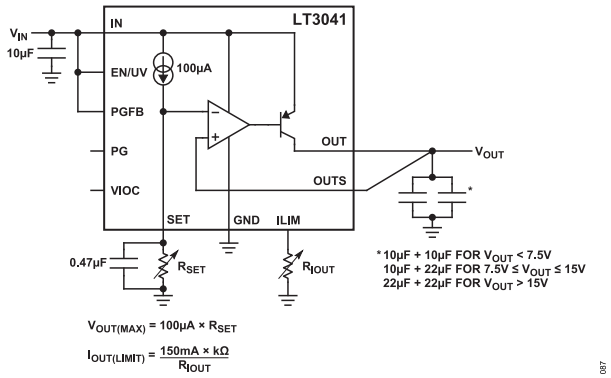



*Figure 87. Low Noise Constant-Current and Constant-Voltage Lab Power Supply*

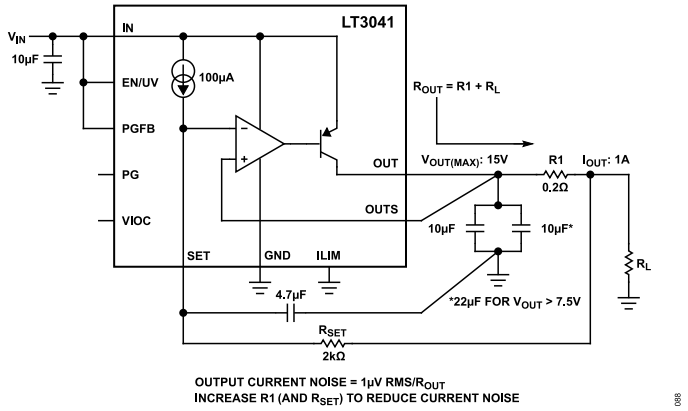



*Figure 88. Ultra-Low Noise-Current Source for RF Biasing Applications ($R_{OUT}$ Is the Output Resistance.)*

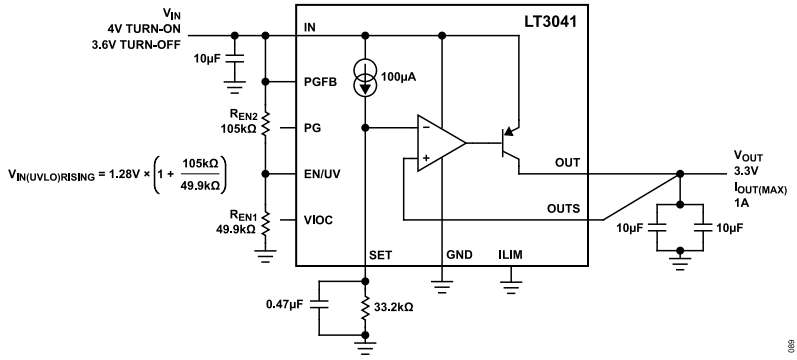



*Figure 89. Programming UVLO*

## TYPICAL APPLICATIONS

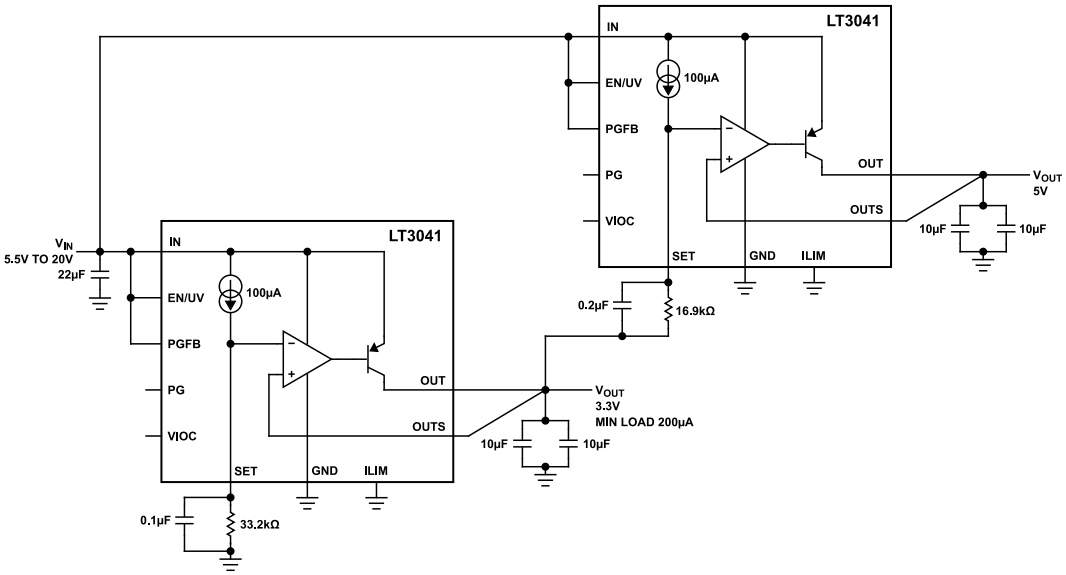



*Figure 90. Ratiometric Tracking*

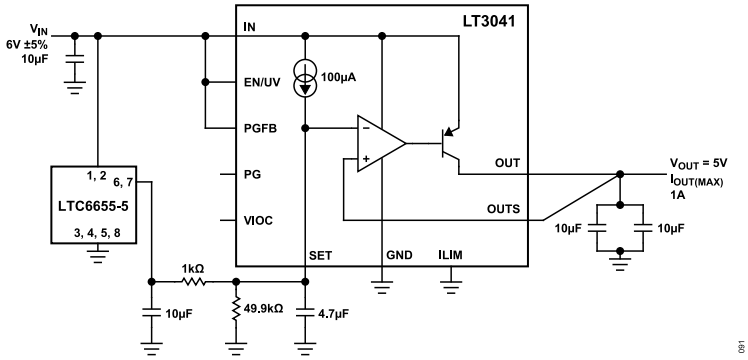



*Figure 91. Ultra-Low 1/f Noise Reference Buffer*

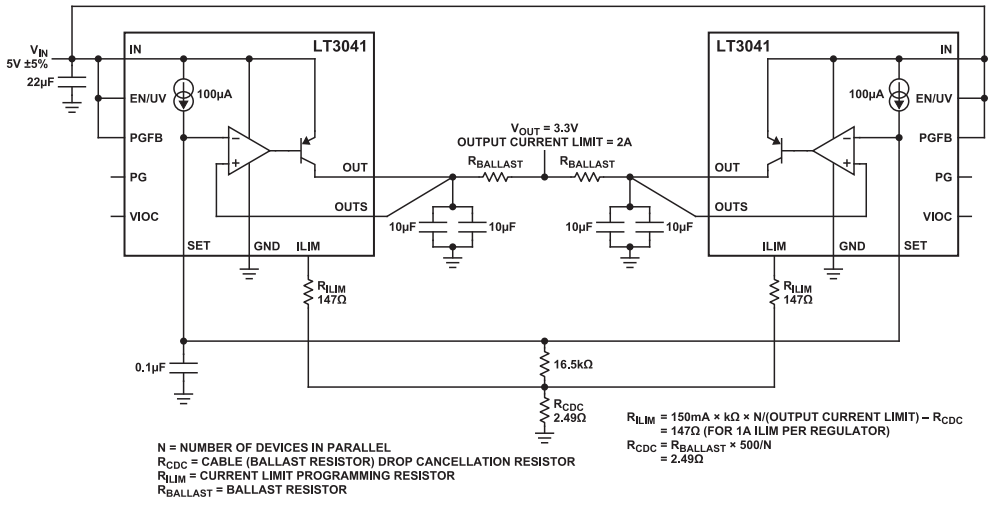



*Figure 92. Paralleling Multiple Devices Using ILIM*

## TYPICAL APPLICATIONS

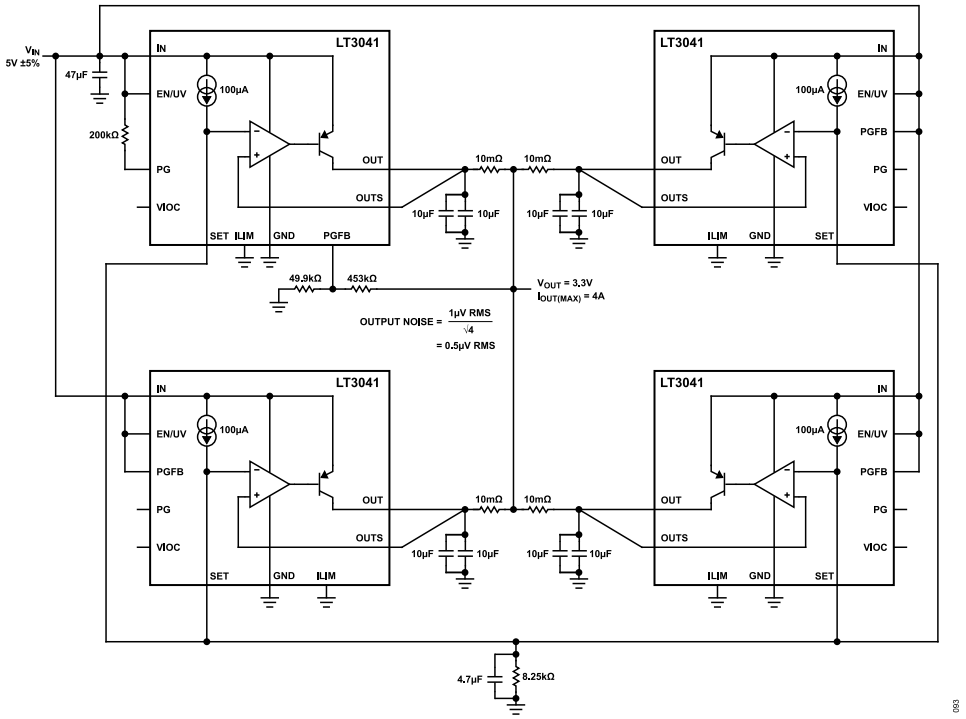



*Figure 93. Paralleling Multiple LT3041 Devices for 4 A Output Current*

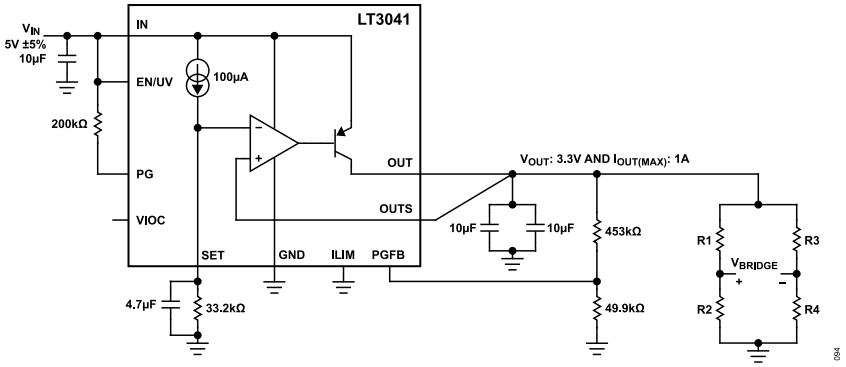



*Figure 94. Low-Noise Wheatstone Bridge Power Supply (See Table 7)*

In Table 7, for the LT1965, noise = 40 µV rms (10 Hz to 100 kHz), and for the LT3041, noise = 1 µV rms (10 Hz to 100 kHz). See Figure 94.

***Table 7. Noise at Bridge for the LT1965 and LT3041***

| Resistor Tolerance (%) | Bridge PSRR | Noise at Bridge Voltage ($V_{BRIDGE}$) Using the LT1965 (nV rms) | Noise at $V_{BRIDGE}$ Using the LT3041 (nV rms) |
|---|---|---|---|
| Perfect Matching | Infinite | Not applicable | Not applicable |
| 1 | 40 dB | 400 | 10 |
| 5 | 26 dB | 200 | 50 |

## TYPICAL APPLICATIONS

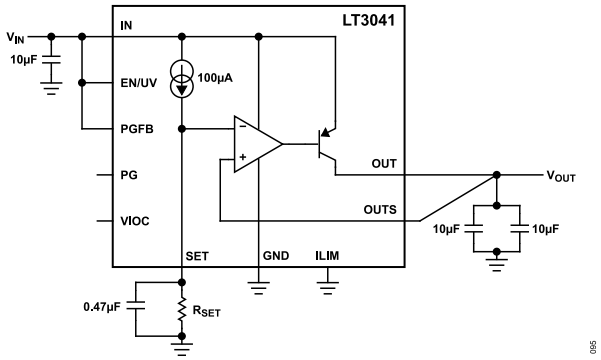



*Figure 95. PGFB Disabled Without Reverse-Input Protection*

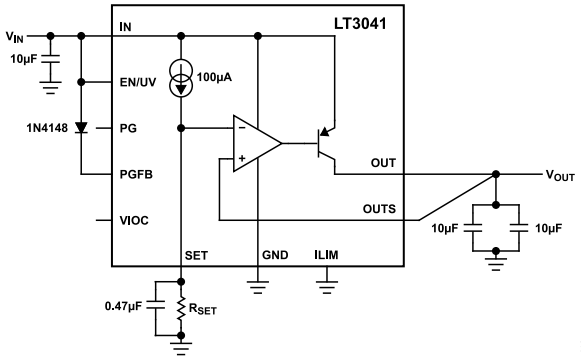



*Figure 96. PGFB Disabled with Reverse-Input Protection*

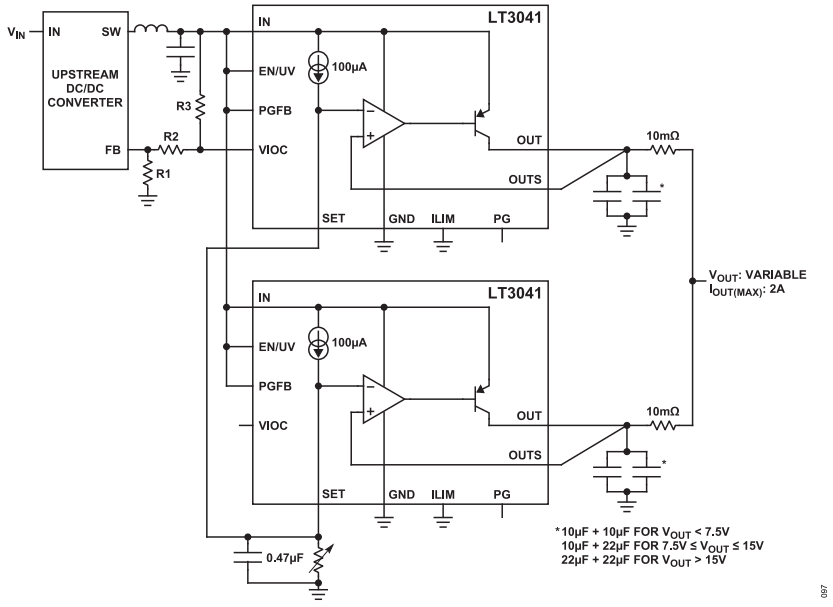


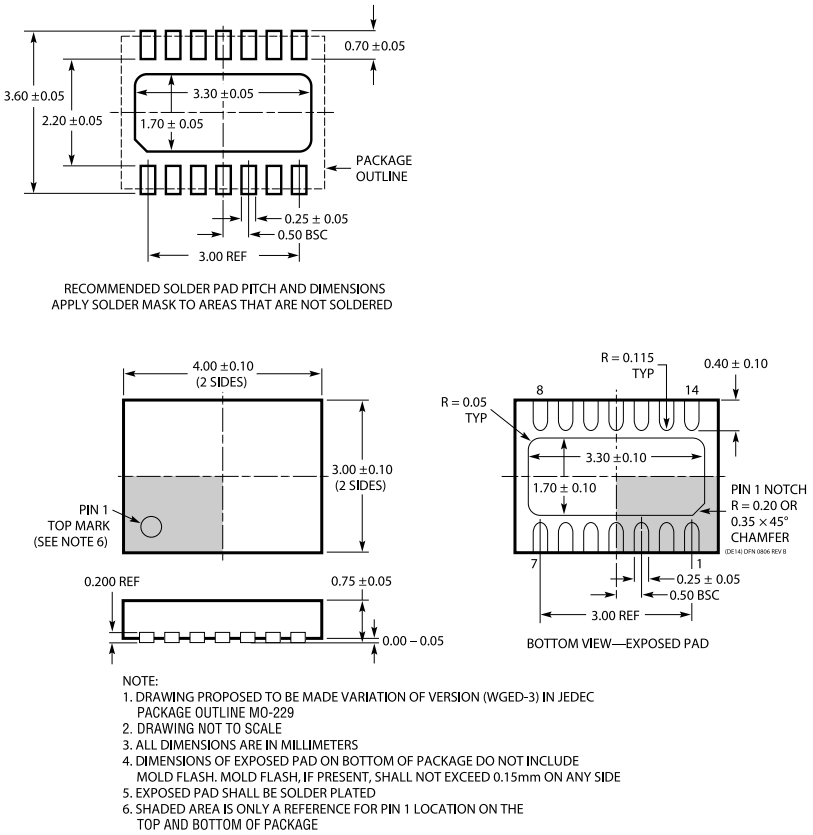

*Figure 97. Post Regulating Application with Parallel Devices*

## RELATED PRODUCTS

*Table 8. Related Products*

| Model | Description | Comments |
|---|---|---|
| LT3042 | 20 V, 200 mA, ultralow noise, ultrahigh PSRR RF linear regulator | 0.8 µV rms noise and 79 dB PSRR at 1 MHz, $V_{IN}$ = 1.8 V to 20 V, 350 mV dropout voltage, programmable current limit and power good, 3 mm × 3 mm DFN and MSOP packages |
| LT3045 | 20 V, 500 mA, ultralow noise, ultrahigh PSRR linear regulator | 0.8 µV rms noise and 75 dB PSRR at 1 MHz, $V_{IN}$ = 1.8 V to 20 V, 260 mV dropout voltage, 3 mm × 3 mm DFN and MSOP packages |
| LT3045-1 | 20 V, 500 mA, ultralow noise, ultrahigh PSRR linear regulator with VIOC control | 0.8 µV rms noise and 75 dB PSRR at 1 MHz, $V_{IN}$ = 1.8 V to 20 V, 260 mV dropout voltage, 3 mm × 3 mm DFN and MSOP packages |
| LT3040 | 20 V, 200 mA, ultralow noise, ultrahigh PSRR precision DAC/ reference buffer | 1.2 µV rms noise and 73dB PSRR at 1 MHz, $V_{IN}$ = 1.8 V to 20 V, 350 mV dropout voltage, 3 mm × 3 mm DFN and MSOP Packages |
| LT3094 | −20 V, 500 mA, ultralow noise, ultrahigh PSRR negative linear regulator | 0.8 µV rms noise and 74 dB PSRR at 1 MHz, $V_{IN}$ = –1.8 V to –20 V, 235 mV dropout voltage, programmable current limit and power good, 3 mm × 3 mm DFN and MSOP packages |
| LT3093 | −20 V, 200 mA, ultralow noise, ultrahigh PSRR negative linear regulator | 0.8 µV rms noise and 73 dB PSRR at 1 MHz, $V_{IN}$ = –1.8 V to –20 V, 190 mV dropout voltage, programmable current limit and power good, 3 mm × 3 mm DFN and MSOP packages |
| ADP1761 | 1 A, Low $V_{IN}$, low noise, CMOS linear regulator | 2 µV rms noise and 41 dB PSRR at 1 MHz, VIN = 1.10 V to 1.98 V, 30 mV dropout voltage, soft-start and power good, 3 mm x 3 mm LFCSP package |
| ADP7156 | 1.2 A, ultralow noise, high PSRR, fixed output, RF linear regulator | 1.6 µV rms noise and 60 dB PSRR at 1 MHz, VIN = 2.3 V to 5.5 V, 120 mV dropout voltage, 3 mm × 3 mm LFCSP and 8-lead SOIC packages |
| ADP7157 | 1.2 A, ultralow noise, high PSRR, adjustable output, RF linear regulator | 1.6 µV rms noise and 55 dB PSRR at 1 MHz, VIN = 2.3 V to 5.5 V, 120 mV dropout voltage, 3 mm × 3 mm LFCSP and 8-lead SOIC packages |
| ADM7150 | 800 mA, ultralow noise, high PSRR, fixed output, RF linear regulator | 1.6 µV rms noise and 60 dB PSRR at 1 MHz, VIN = 4.5 V to 16 V, 600 mV dropout voltage, 3 mm × 3 mm LFCSP and 8-lead SOIC packages |
| ADM7151 | 800 mA, ultralow noise, high PSRR, adjustable output, RF linear regulator | 1.6 µV rms noise and 60 dB PSRR at 1 MHz, VIN = 4.5 V to 16 V, 600 mV dropout voltage, 3 mm × 3 mm LFCSP and 8-lead SOIC packages |
| MAX38913 | 4 µV rms, ultra-low noise, 1 A, LDO with two-level, output-voltage selection | 4 µV rms noise and 50 dB PSRR at 1 MHz, VIN = 1.8 V to 5.5 V, 28 mV dropout voltage, fast active discharge and power-OK, 3 mm × 3 mm TDFN and WLP packages |

## OUTLINE DIMENSIONS




NOTE:
1. DRAWING PROPOSED TO BE MADE VARIATION OF VERSION (WGED-3) IN JEDEC PACKAGE OUTLINE MO-229
2. DRAWING NOT TO SCALE
3. ALL DIMENSIONS ARE IN MILLIMETERS
4. DIMENSIONS OF EXPOSED PAD ON BOTTOM OF PACKAGE DO NOT INCLUDE MOLD FLASH. MOLD FLASH, IF PRESENT, SHALL NOT EXCEED 0.15mm ON ANY SIDE
5. EXPOSED PAD SHALL BE SOLDER PLATED
6. SHADED AREA IS ONLY A REFERENCE FOR PIN 1 LOCATION ON THE TOP AND BOTTOM OF PACKAGE

***Figure 98. 14-Lead, 4 mm × 3 mm, Plastic DFN (05-08-1708) Dimensions shown in millimeters***

## ORDERING GUIDE

| Model[1] | Temperature Range | Package Description | Packing Quantity | Package Option |
|---|---|---|---|---|
| LT3041ADE#PBF | -40°C to +125°C | 14-Lead DFN (4mm x 3mm w/ EP) | Tray, 490 | 05-08-1708 |
| LT3041ADE#TRPBF | -40°C to +125°C | 14-Lead DFN (4mm x 3mm w/ EP) | Reel, 2500 | 05-08-1708 |

[1] Z = RoHS Compliant Part.

Updated: August 09, 2023

## EVALUATION BOARDS

***Table 9. Evaluation Boards***

| Model[1] | Description |
|---|---|
| DC3158A | Evaluation Board |

[1] The DC3158A is a RoHS compliant part.