High Performance, 3.2 GHz, 14-Output Clock Distributor with JESD204B/C Support

FEATURES

- JEDEC JESD204B and JESD204C support
- Low additive jitter: <15 fs rms at 2457.6 MHz (12 kHz to 20 MHz)
- Very low noise floor: −155.2 dBc/Hz at 983.04 MHz
- Up to 14 LVDS, LVPECL, or CML type device clocks (DCLKs)
  - Maximum CLKOUTx/$\overline{\text{CLKOUTx}}$ and SCLKOUTx/$\overline{\text{SCLKOUTx}}$ frequency of 3200 MHz
  - JESD204B and JESD204C compatible system reference (SYSREF) pulses
  - 25 ps analog and ½ clock input cycle digital delay independently programmable on each of 14 clock output channels
- SPI-programmable adjustable noise floor vs. power consumption
- SYSREF valid interrupt to simplify JESD204B synchronization
- Supports deterministic synchronization of multiple HMC7043 devices
- RFSYNCIN pin or SPI-controlled SYNC trigger for output synchronization of JESD204B/C
- GPIO alarm/status indicator to determine system health
- Clock input to support up to 6 GHz
- 48-lead, 7 mm × 7 mm LFCSP package

APPLICATIONS

- JESD204B and JESD204C clock generation
- Cellular infrastructure (multicarrier GSM, LTE, W-CDMA)
- Data converter clocking
- Phase array reference distribution
- Microwave baseband cards

GENERAL DESCRIPTION

The HMC7043 is a high performance clock buffer for the distribution of ultralow phase noise references for high speed data converters with either parallel or serial (JESD204B/C types) interfaces.

The HMC7043 is designed to meet the requirements of multicarrier GSM and LTE base station designs, and offers a wide range of clock management and distribution features to simplify baseband and radio card clock tree designs.

The HMC7043 provides 14 low noise and configurable outputs to offer flexibility in interfacing with many different components in a base transceiver station (BTS) system, such as data converters, local oscillators, transmit/receive modules, field programmable gate arrays (FPGAs), and digital front-end ASICs. The HMC7043 can generate up to seven DCLK and SYSREF clock pairs per the JESD204B/C interface requirements.

The system designer can generate a lower number of DCLK and SYSREF pairs, and configure the remaining output signal paths for independent phase and frequency. Both the DCLK and SYSREF clock outputs can be configured to support different signaling standards, including CML, LVDS, LVPECL, and LVCMOS, and different bias conditions to adjust for varying board insertion losses.

One of the unique features of the HMC7043 is the independent flexible phase management of each of the 14 channels. All 14 channels feature both frequency and phase adjustment. The outputs can also be programmed for 50 Ω or 100 Ω internal and external termination options.

The HMC7043 device features an RF SYNC feature that synchronizes multiple HMC7043 devices deterministically, that is, ensures that all clock outputs start with the same edge. This operation is achieved by rephasing the nested HMC7043 or SYSREF control unit/divider, deterministically, and then restarting the output dividers with this new phase.

The HMC7043 is offered in a 48-lead, 7 mm × 7 mm LFCSP package with an exposed pad connected to ground.

FUNCTIONAL BLOCK DIAGRAM

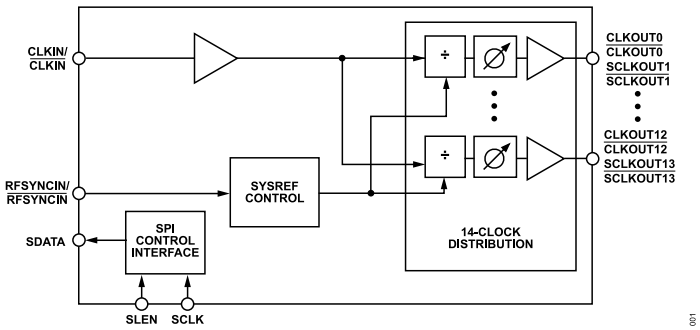

Figure 1.

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REVISION HISTORY

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SPECIFICATIONS

V_{CC} = 3.3 V ± 5%, and T_A = 25°C, unless otherwise noted. Minimum and maximum values are given over the full V_{CC} and T_A (−40°C to +85°C) variation, as listed in Table 1.

CONDITIONS

Table 1.

Parameter[1]	Min	Typ	Max	Unit	Test Conditions/Comments
SUPPLY VOLTAGE, V_{CC}					
VCC1_CLKDIST	3.135	3.3	3.465	V	3.3 V ± 5%, supply voltage for CLK distribution
VCC2_OUT	3.135	3.3	3.465	V	3.3 V ± 5%, supply voltage for Output Channel 2 and Output Channel 3
VCC3_OUT	3.135	3.3	3.465	V	3.3 V ± 5%, supply voltage for Output Channel 4, Output Channel 5, Output Channel 6, and Output Channel 7
VCC4_CLKIN	3.135	3.3	3.465	V	3.3 V ± 5%, supply voltage for the clock input path
VCC5_SYSREF	3.135	3.3	3.465	V	3.3 V ± 5%, supply voltage for the common SYSREF divider
VCC6_OUT	3.135	3.3	3.465	V	3.3 V ± 5%, supply voltage for Output Channel 8, Output Channel 9, Output Channel 10, and Output Channel 11
VCC7_OUT	3.135	3.3	3.465	V	3.3 V ± 5%, supply voltage for Output Channel 0, Output Channel 1, Output Channel 12, and Output Channel 13
TEMPERATURE					
Ambient Temperature Range, T_A	−40	+25	+85	°C	

[1] Maximum values are guaranteed by design and characterization.

SUPPLY CURRENT

For detailed test conditions, see Table 18 and Table 19.

Table 2.

Parameter[1, 2]	Min	Typ	Max	Unit	Test Conditions/Comments
CURRENT CONSUMPTION[3]					
VCC1_CLKDIST		87	125	mA	
VCC2_OUT[4]		90	250	mA	Typical value is given at T_A = 25°C with two LVDS clocks at divide by 8
VCC3_OUT[4]		52	500	mA	Typical value is given at 25°C with two LVDS high performance clocks, fundamental frequency of the clock input (f_O), two SYSREF clocks (off)
VCC4_CLKIN		16	25	mA	Typical value is given at T_A = 25°C with RF synchronization (RFSYNC) input buffer off
VCC5_SYSREF		23	35	mA	Typical value is given at T_A = 25°C with internal RF SYNC path off
VCC6_OUT[4]		90	500	mA	Typical value is given at 25°C with two LVDS high performance clocks at divide by 2, two SYSREF clocks (off)
VCC7_OUT[4]		100	500	mA	Typical value is given at 25°C with two LVDS clocks at divide by 8, two SYSREF clocks (off)
Total Current		458		mA	

[1] Maximum values are guaranteed by design and characterization.

[2] Currents include LVDS termination currents.

[3] Maximum values are for all circuits enabled in their worst case power consumption mode, PVT variations, and accounting for peak current draw during temporary synchronization events.

[4] Typical specification applies to a normal usage profile (Profile 1 in Table 18) but very low duty cycle currents (sync events) and some optional features are disabled. This specification assumes output configurations as described in the test conditions/comments column.

SPECIFICATIONS

DIGITAL INPUT/OUTPUT (I/O) ELECTRICAL SPECIFICATIONS

Table 3.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
DIGITAL INPUT SIGNALS (RESET, SLEN, SCLK)					
Safe Input Voltage Range	−0.1		+3.6	V	
Input Load		0.3		pF	
Input Voltage					
Input Logic High	1.2		V_{CC}	V	
Input Logic Low	0		0.5	V	
SPI Bus Frequency			10	MHz	
DIGITAL BIDIRECTIONAL SIGNALS CONFIGURED AS INPUTS (SDATA, GPIO)					
Safe Input Voltage Range	−0.1		+3.6	V	
Input Capacitance		0.4		pF	
Input Resistance		50		GΩ	
Input Voltage					
Input Logic High	1.22		V_{CC}	V	
Input Logic Low	0		0.24	V	
Input Hysteresis		0.2		V	Occurs around 0.85 V
GPIO ALARM MUXING/DELAY					
Delay from Internal Alarm/Signal to General-Purpose Output (GPO) Driver		2		ns	Does not include t_{DGPO}
DIGITAL BIDIRECTIONAL SIGNALS CONFIFURED AS OUTPUTS (SDATA, GPIO)					
CMOS Mode					
Logic 1 Level	1.6	1.9	2.2	V	
Logic 0 Level		0	0.1	V	
Output Drive Resistance (R_{DRIVE})		50		Ω	
Output Driver Delay (t_{DGPO})		1.5 + 42 × C_{LOAD}		ns	Approximately 1.5 ns + 0.69 × R_{DRIVE} × C_{LOAD} (C_{LOAD} in nF)
Maximum Supported DC Current[1]			0.6	mA	
Open-Drain Mode					External 1 kΩ pull-up resistor
Logic 1 Level			3.6	V	3.6 V maximum permitted; specifications set by external supply
Logic 0 Level		0.13	0.28	V	Against a 1 kΩ external pull-up resistor to 3.3 V
Pull-Down Impedance		60		Ω	
Maximum Supported Sink Current[1]			5	mA	

[1] Guaranteed by design and characterization for long-term reliability.

INPUT PATH SPECIFICATIONS

Table 4.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
CLOCK INPUT (CLKIN)					
Recommended Input Power, AC-Coupled					
Differential	−6		+8	dBm	
Single-Ended[1]	−10		+6	dBm	Noise floor degrade by 3 dB at f_{CLKIN} = 2400 MHz
Return Loss		−12		dB	When terminated with 100 Ω differential
Clock Input Frequency (f_{CLKIN})	200			MHz	When all channel dividers are equal to one or channels are in the fundamental mode. If <1 GHz, set the low frequency external VCO path bit (Register 0x0064, Bit 0)

SPECIFICATIONS

Table 4. (Continued)

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
	450			MHz	When channel dividers are larger than 1 and synchronization is needed
			3200	MHz	Clock Input Divider is disabled. Register 0x0064[1] = 0
			6000	MHz	Clock Input Divider is enabled. Register 0x0064[1] = 1
Common-Mode Range	0.4		2.4	V	
RFSYNC INPUT					
Differential Swing	0.375		1.4	V p-p	Differential, keep signal at reference input pin <2.8 V, measured at 800 MHz
Single-Ended Swing	0.375		1.4	V p-p	Keep signal at reference input pin <2.8 V
Common Mode Range	0.4		2.4	V	If user supplied, on-chip V_{CM} is approximately 2.1 V. DC coupling preferred
Input Impedance		100 to 2000		Ω	User selectable; differential
Return Loss		−12		dB	When terminated with 100 Ω differential
Setup/Hold Time		40		ps	V_{CM} set to self bias voltage

[1] Guaranteed by design and characterization.

ADDITIVE JITTER AND PHASE NOISE CHARACTERISTICS

Table 5.

Parameter[1]	Min	Typ	Max	Unit	Test Conditions/Comments
ADDITIVE JITTER					HMC7044 used as a clock source (see Figure 3)
RMS Additive Jitter		<30		fs rms	Clock output frequency (f_{CLKOUT}) = 983.04 MHz, BW = 12 kHz to 20 MHz, clock input slew rate ≥ 8 ns
		<15		fs rms	f_{CLKOUT} = 2457.6 MHz, BW = 12 kHz to 20 MHz, clock input slew rate ≥ 4 ns
CLOCK OUTPUT PHASE NOISE					HMC830 used as a clock source and configured to produce 983.04 MHz at the output (see Figure 4), input slew rate > 1 V/ns
Absolute Phase Noise					
Offset = 1 MHz		−144.3		dBc/Hz	f_{CLKOUT} = 983.04 MHz, f_{CLKOUT} = 983.04 MHz, divide by 1 at the output
Offset = 10 MHz		−154.8		dBc/Hz	f_{CLKOUT} = 983.04 MHz, f_{CLKOUT} = 2949.12 MHz, divide by 3 at the output
Offset = 20 MHz		−155.2		dBc/Hz	f_{CLKOUT} = 983.04 MHz, f_{CLKOUT} = 983.04 MHz, divide by 1 at the output

[1] Guaranteed by design and characterization.

CLOCK OUTPUT DISTRIBUTION SPECIFICATIONS

Table 6.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
CLOCK OUTPUT SKEW					Please refer to the Phase Behavior of Synchronized Divided Clocks section for the skew behavior of pulse generation
CLKOUTx/$\overline{\text{CLKOUTx}}$ to SCLKOUTx/$\overline{\text{SCLKOUTx}}$ Skew Within One Clock Output Pair		15		|ps|	Same pair, same type termination and configuration
Any CLKOUTx/$\overline{\text{CLKOUTx}}$ to Any SCLKOUTx/$\overline{\text{SCLKOUTx}}$		30		|ps|	Any pair, same type termination and configuration
PROPAGATION DELAY CLKIN to CLKOUTx and SCLKOUTx[1]	770	820	870	ps	f_{CLKIN} = 983.04 MHz, all V_{CC} set to 3.3 V
CLOCK OUTPUT DIVIDER CHARACTERISTICS					
12-Bit Divider Range	1		4094		1, 3, 5, and all even numbers up to 4094
SYSREF CLOCK OUTPUT DIVIDER CHARACTERISTICS					

SPECIFICATIONS

Table 6. (Continued)

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
12-Bit Divider Range	1		4094		1, 3, 5, and all even numbers up to 4094; pulse generator behavior is only supported for divide ratios ≥ 32
CLOCK OUTPUT ANALOG FINE DELAY					
Analog Fine Delay					
Adjustment Range[1]	135		670	ps	24 delay steps, f_{CLKOUT} = 983.04 MHz
Resolution		25		ps	f_{CLKOUT} = 983.04 MHz (2949.12 MHz/3)
Maximum Analog Fine Delay Frequency		1600		MHz	
CLOCK OUTPUT COARSE DELAY (FLIP FLOP BASED)					
Coarse Delay Adjustment Range	0		17	½ CLKIN period	17 delay steps
Coarse Delay Resolution		169.54		ps	f_{CLKIN} = 2949.12 MHz
Maximum Frequency Coarse Delay		1500		MHz	
CLOCK OUTPUT COARSE DELAY (SLIP BASED)					
Coarse Delay					
Adjustment Range		1 to ∞		CLKIN period	
Resolution		339.08		ps	f_{CLKIN} = 2949.12 MHz
Maximum Frequency Coarse Delay		1600		MHz	

[1] Guaranteed by design and characterization.

CLOCK OUTPUT DRIVER CHARACTERISTICS

Table 7.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
CML MODE (LOW POWER)					R_L = 100 Ω, 9.6 mA
−3 dB Bandwidth		1950		MHz	Differential output voltage = 980 mV p-p diff
Output Rise Time		175		ps	f_{CLKOUT} = 245.76 MHz, 20% to 80%
		145		ps	f_{CLKOUT} = 983.04 MHz, 20% to 80%
Output Fall Time		185		ps	f_{CLKOUT} = 245.76 MHz, 20% to 80%
		145		ps	f_{CLKOUT} = 983.04 MHz, 20% to 80%
Output Duty Cycle[1]	47.5	50	52.5	%	f_{CLKOUT} = 1075 MHz (2150 MHz/2)
Differential Output Voltage Magnitude		1390		mV p-p diff	f_{CLKOUT} = 245.76 MHz (2949.12 MHz/12)
		1360		mV p-p diff	f_{CLKOUT} = 983.04 MHz (2949.12 MHz/3)
Common-Mode Output Voltage		V_{CC} − 1.05		V	f_{CLKOUT} = 245.76 MHz (2949.12 MHz/12)
CML MODE (HIGH POWER)					R_L = 100 Ω, 14.5 mA
−3 dB Bandwidth		1500		MHz	Differential output voltage = 1470 mV p-p diff
Output Rise Time		250		ps	f_{CLKOUT} = 245.76 MHz, 20% to 80%
		165		ps	f_{CLKOUT} = 983.04 MHz, 20% to 80%
Output Fall Time		255		ps	f_{CLKOUT} = 245.76 MHz, 20% to 80%
		170		ps	f_{CLKOUT} = 983.04 MHz, 20% to 80%
Output Duty Cycle[1]	47.5	50	52.5	%	f_{CLKOUT} = 1075 MHz (2150 MHz/2)
Differential Output Voltage Magnitude		2000		mV p-p diff	f_{CLKOUT} = 245.76 MHz (2949.12 MHz/12)
		1800		mV p-p diff	f_{CLKOUT} = 983.04 MHz (2949.12 MHz/3)
Differential Output					
Voltage Magnitude		590		mV p-p diff	f_{CLKOUT} = 3200 MHz
Power		−3.6		dBm diff	f_{CLKOUT} = 3200 MHz
Common-Mode Output Voltage		V_{CC} − 1.6		V	f_{CLKOUT} = 245.76 MHz (2949.12 MHz/12)
LVPECL MODE					R_L = 150 Ω, 4.8 mA
−3 dB Bandwidth		2400		MHz	Differential output voltage = 1240 mV p-p diff

SPECIFICATIONS

Table 7. (Continued)

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
Output Rise Time		135		ps	f_{CLKOUT} = 245.76 MHz, 20% to 80%
		130		ps	f_{CLKOUT} = 983.04 MHz, 20% to 80%
Output Fall Time		135		ps	f_{CLKOUT} = 245.76 MHz, 20% to 80%
		130		ps	f_{CLKOUT} = 983.04 MHz, 20% to 80%
Output Duty Cycle[1]	47.5	50	52.5	%	f_{CLKOUT} = 1075 MHz (2150 MHz/2)
Differential Output Voltage Magnitude		1760		mV p-p diff	f_{CLKOUT} = 245.76 MHz (2949.12 MHz/12)
		1850		mV p-p diff	f_{CLKOUT} = 983.04 MHz (2949.12 MHz/3)
Differential Output					
Voltage Magnitude		930		mV p-p diff	f_{CLKOUT} = 3200 MHz
Power		0.3		dBm diff	f_{CLKOUT} = 3200 MHz
Common-Mode Output Voltage		V_{CC} − 1.3		V	f_{CLKOUT} = 245.76 MHz (2949.12 MHz/12)
LVDS MODE (LOW POWER)[2]					1.75 mA
Maximum Operating Frequency		1700		MHz	Differential output voltage = 320 mV p-p diff
Output Rise Time		135		ps	f_{CLKOUT} = 245.76 MHz, 20% to 80%
		100		ps	f_{CLKOUT} = 983.04 MHz, 20% to 80%
Output Fall Time		135		ps	f_{CLKOUT} = 245.76 MHz, 20% to 80%
		95		ps	f_{CLKOUT} = 983.04 MHz, 20% to 80%
Output Duty Cycle[1]	47.5	50	52.5	%	f_{CLKOUT} = 1075 MHz (2150 MHz/2)
Differential Output Voltage Magnitude		390		mV p-p diff	f_{CLKOUT} = 245.76 MHz (2949.12 MHz/12)
Common-Mode Output Voltage		1.1		V	f_{CLKOUT} = 245.76 MHz (2949.12 MHz/12)
LVDS MODE (HIGH POWER)[2]					3.5 mA
Maximum Operating Frequency		1700		MHz	Differential output voltage = 600 mV p-p diff
Output Rise Time		145		ps	f_{CLKOUT} = 245.76 MHz, 20% to 80%
		105		ps	f_{CLKOUT} = 983.04 MHz, 20% to 80%
Output Fall Time		145		ps	f_{CLKOUT} = 245.76 MHz, 20% to 80%
		100		ps	f_{CLKOUT} = 983.04 MHz, 20% to 80%
Output Duty Cycle[1]	47.5	50	52.5	%	f_{CLKOUT} = 1075 MHz (2150 MHz/2)
Differential Output Voltage Magnitude		750		mV p-p diff	f_{CLKOUT} = 245.76 MHz (2949.12 MHz/12)
		730		mV p-p diff	f_{CLKOUT} = 983.04 MHz (2949.12 MHz/3)
Common-Mode Output Voltage		1.1		V	f_{CLKOUT} = 245.76 MHz (2949.12 MHz/12)
CMOS MODE					
Maximum Operating Frequency		600		MHz	Single-ended output voltage = 940 mV p-p diff
Output Rise Time		425		ps	f_{CLKOUT} = 245.76 MHz, 20% to 80%
Output Fall Time		420		ps	f_{CLKOUT} = 245.76 MHz, 20% to 80%
Output Duty Cycle[1]	47.5	50	52.5	%	f_{CLKOUT} = 1075 MHz (2150 MHz/2)
Output Voltage					
High		V_{CC}		V	Load current = 1 mA
		V_{CC} − 0.5		V	Load current = 10 mA
Low		0.07		V	Load current = 1 mA
		0.5		V	Load current = 10 mA

[1] Guaranteed by design and characterization.

[2] Refer to the Clock Output Network section for the N-Pulse SYSREF generation operation.

ABSOLUTE MAXIMUM RATINGS

Table 8.

Parameter	Rating
VCC1, VCC2, VCC3, VCC4, VCC5, VCC6, VCC7 to Ground	−0.3 V to +3.6 V
Maximum Junction Temperature	125°C
Storage Temperature Range	−65°C to +125°C
Operating Temperature Range	−40°C to +85°C
Peak Reflow Temperature	260°C
ESD Sensitivity Level	
Human Body Model (HBM)	Class 1C
Charged Device Model (CDM)	Class 2B

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

THERMAL RESISTANCE

Thermal performance is directly linked to printed circuit board (PCB) design and operating environment. Close attention to PCB thermal design is required. θ_{JA} is the natural convection, junction to ambient thermal resistance measured in a one cubic foot sealed enclosure. θ_{JC} is the junction to case thermal resistance. θ_{JB} is the junction to bottom ground paddle thermal resistance.

Table 9. Thermal Resistance

PCB Type	θ_{JA}	θ_{JC}	θ_{JB}	Unit
JEDEC 2s2p Board	N/A[1]	13.40	6.92	°C/W

[1] N/A means not applicable.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

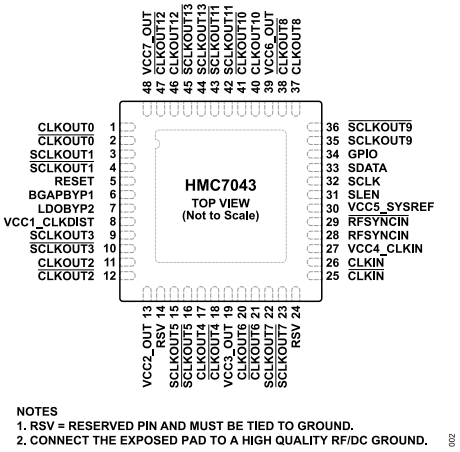

Figure 2.

Table 10. Pin Function Descriptions

Pin No.	Mnemonic	Type[1]	Description
1	CLKOUT0	O	True Clock Output Channel 0. Default DCLK profile.
2	$\overline{\text{CLKOUT0}}$	O	Complementary Clock Output Channel 0. Default DCLK profile.
3	SCLKOUT1	O	True Clock Output Channel 1. Default SYSREF profile.
4	$\overline{\text{SCLKOUT1}}$	O	Complementary Clock Output Channel 1. Default SYSREF profile.
5	RESET	I	Device Reset Input. Active high. For normal operation, set RESET to 0.
6	BGAPBYP1		Band Gap Bypass Capacitor Connection. Connect a 4.7 µF capacitor to ground. This pin affects all internally regulated supplies.
7	LDOBYP2		LDO Bypass 2. Connect a 4.7 µF capacitor to ground. The internal digital supply is 1.8 V. This pin is the LDO bypass for the SYSREF section.
8	VCC1_CLKDIST	P	3.3 V Supply for CLK Distribution.
9	SCLKOUT3	O	True Clock Output Channel 3. Default SYSREF profile.
10	$\overline{\text{SCLKOUT3}}$	O	Complementary Clock Output Channel 3. Default SYSREF profile.
11	CLKOUT2	O	True Clock Output Channel 2. Default DCLK profile.
12	$\overline{\text{CLKOUT2}}$	O	Complementary Clock Output Channel 2. Default DCLK profile.
13	VCC2_OUT	P	Power Supply for Clock Group 1 (Southwest)—Channel 2 and Channel 3. See the Clock Grouping, Skew, and Crosstalk section.
14	RSV	R	Reserved Pin. This pin must be tied to ground.
15	SCLKOUT5	O	True Clock Output Channel 5. Default SYSREF profile.
16	$\overline{\text{SCLKOUT5}}$	O	Complementary Clock Output Channel 5. Default SYSREF profile.
17	CLKOUT4	O	True Clock Output Channel 4. Default DCLK profile.
18	$\overline{\text{CLKOUT4}}$	O	Complementary Clock Output Channel 4. Default DCLK profile.
19	VCC3_OUT	P	Power Supply for Clock Group 2 (South)—Channel 4, Channel 5, Channel 6, and Channel 7. See the Clock Grouping, Skew, and Crosstalk section.
20	CLKOUT6	O	True Clock Output Channel 6. Default DCLK profile.
21	$\overline{\text{CLKOUT6}}$	O	Complementary Clock Output Channel 6. Default DCLK profile.
22	SCLKOUT7	O	True Clock Output Channel 7. Default SYSREF profile.
23	$\overline{\text{SCLKOUT7}}$	O	Complementary Clock Output Channel 7. Default SYSREF profile.
24	RSV	R	Reserved Pin. This pin must be tied to ground.
25	$\overline{\text{CLKIN}}$	I	Complementary Clock Input.
26	CLKIN	I	True Clock Input.
27	VCC4_CLKIN	P	Power Supply for the Clock Input Path.
28	RFSYNCIN	I	True RF Synchronization Input with Deterministic Delay.
29	$\overline{\text{RFSYNCIN}}$	I	Complementary RF Synchronization Input with Deterministic Delay.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

Table 10. Pin Function Descriptions (Continued)

Pin No.	Mnemonic	Type[1]	Description
30	VCC5_SYSREF	P	Power Supply for Common SYSREF Divider.
31	SLEN	I/O	SPI Latch Enable.
32	SCLK	I/O	SPI Clock.
33	SDATA	I/O	SPI Data.
34	GPIO	I/O	Programmable General-Purpose Input/Output.
35	SCLKOUT9	O	True Clock Output Channel 9. Default SYSREF profile.
36	$\overline{\text{SCLKOUT9}}$	O	Complementary Clock Output Channel 9. Default SYSREF profile.
37	CLKOUT8	O	True Clock Output Channel 8. Default DCLK profile.
38	$\overline{\text{CLKOUT8}}$	O	Complementary Clock Output Channel 8. Default DCLK profile.
39	VCC6_OUT	P	Power Supply for Clock Group 3 (North)—Channel 8, Channel 9, Channel 10, and Channel 11. See the Clock Grouping, Skew, and Crosstalk section.
40	CLKOUT10	O	True Clock Output Channel 10. Default DCLK profile.
41	$\overline{\text{CLKOUT10}}$	O	Complementary Clock Output Channel 10. Default DCLK profile.
42	SCLKOUT11	O	True Clock Output Channel 11. Default SYSREF profile.
43	$\overline{\text{SCLKOUT11}}$	O	Complementary Clock Output Channel 11. Default SYSREF profile.
44	SCLKOUT13	O	True Clock Output Channel 13. Default SYSREF profile.
45	$\overline{\text{SCLKOUT13}}$	O	Complementary Clock Output Channel 13. Default SYSREF profile.
46	CLKOUT12	O	True Clock Output Channel 12. Default DCLK profile.
47	$\overline{\text{CLKOUT12}}$	O	Complementary Clock Output Channel 12. Default DCLK profile.
48	VCC7_OUT	P	Power Supply for Clock Group 0 (Northwest)—Channel 0, Channel 1, Channel 12, and Channel 13. See the Clock Grouping, Skew, and Crosstalk section.
	EP		Exposed Pad. Connect the exposed pad to a high quality RF/dc ground.

[1] O is output, I is input, P is power, R is reserved, and I/O is input/output.

TYPICAL PERFORMANCE CHARACTERISTICS

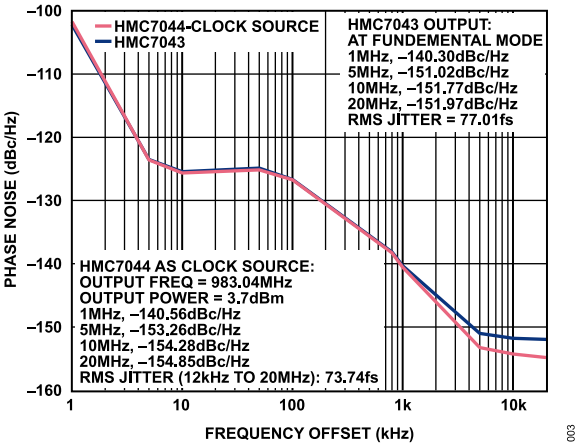

Figure 3. Additive Jitter at 983.04 MHz at Output

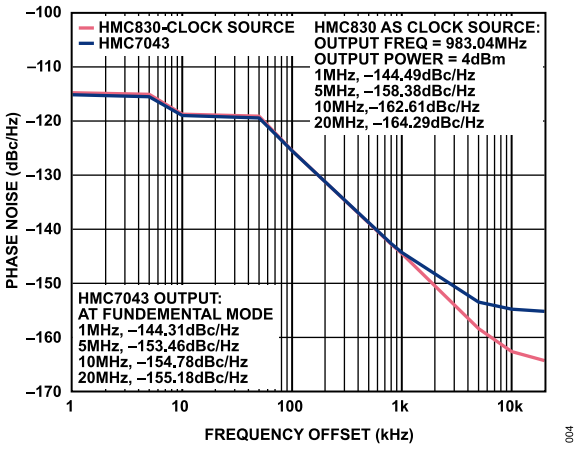

Figure 4. Absolute Phase Noise Measured at 983.04 MHz at Output

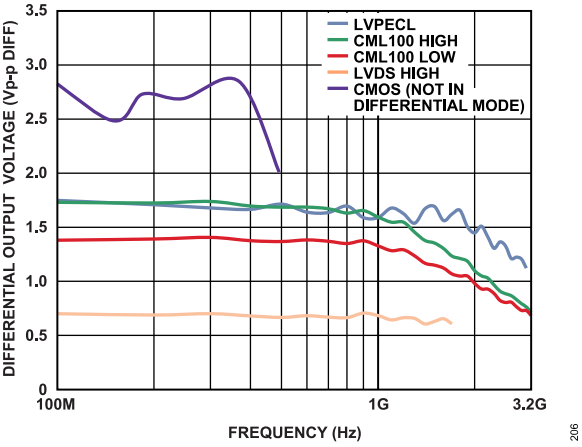

Figure 5. Differential Output Power vs. Frequency over Various Modes

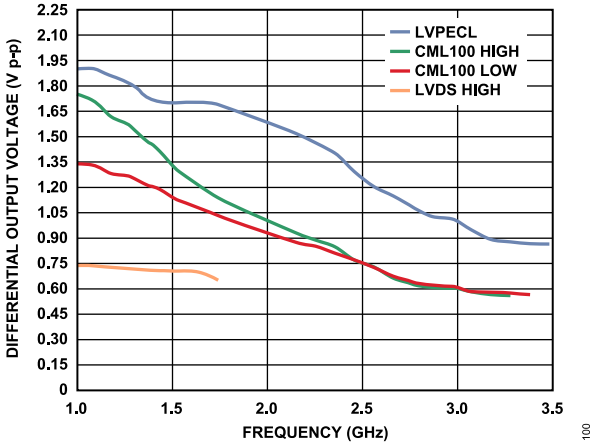

Figure 6. Differential Output Voltage vs. Frequency over Various Modes

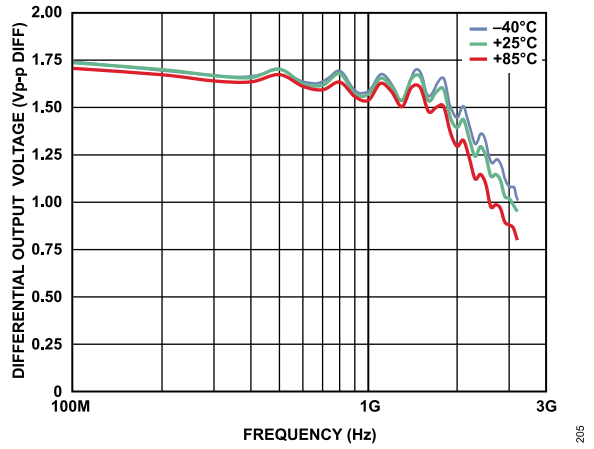

Figure 7. LVPECL Differential Output Power vs. Frequency over Various Temperatures

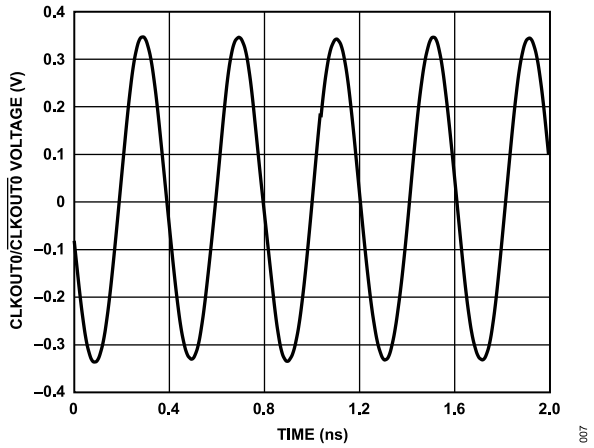

Figure 8. Differential CLKOUT0/$\overline{\text{CLKOUT0}}$ at 2457 MHz, LVPECL

TYPICAL PERFORMANCE CHARACTERISTICS

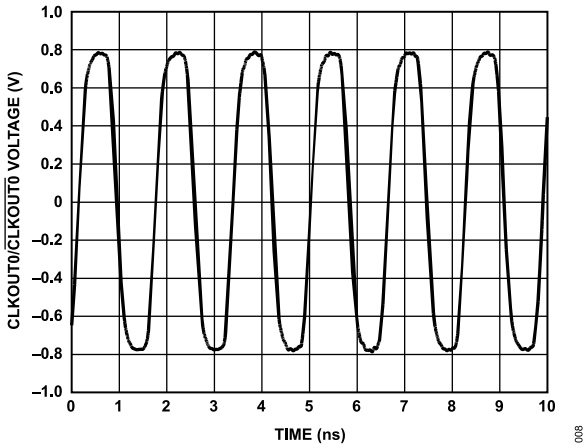

Figure 9. Differential CLKOUT0/CLKOUT0 Voltage at 614.4 MHz, LVPECL

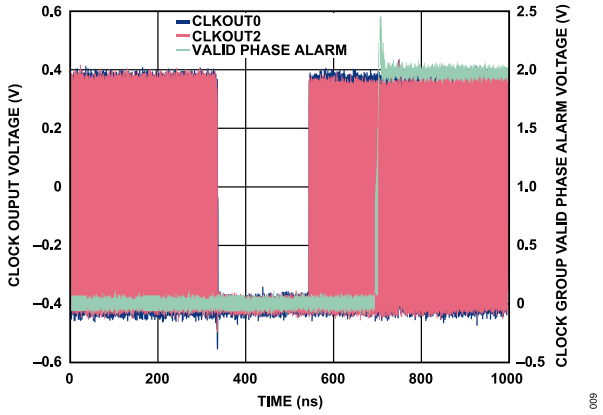

Figure 10. Output Channel Synchronization Before and After Rephase

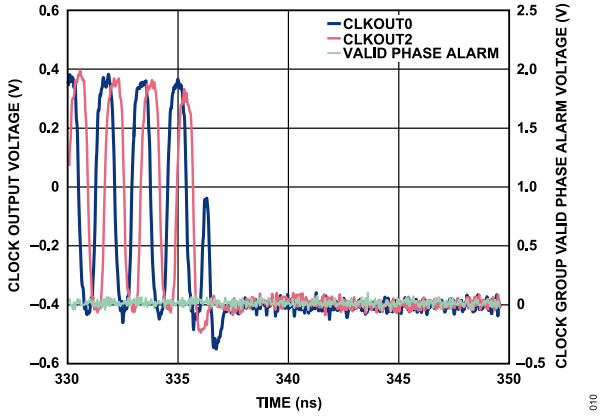

Figure 11. Output Channel Synchronization Before Rephase

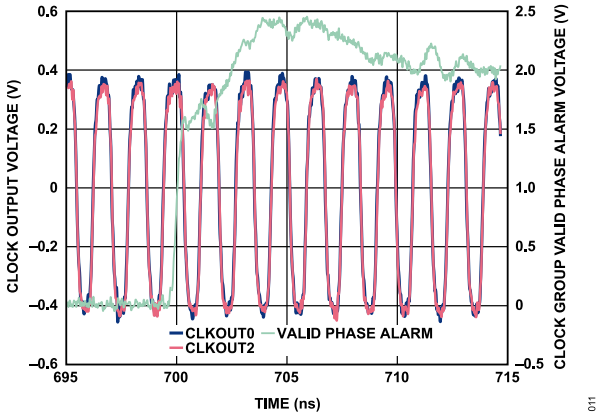

Figure 12. Output Channel Synchronization After Rephase

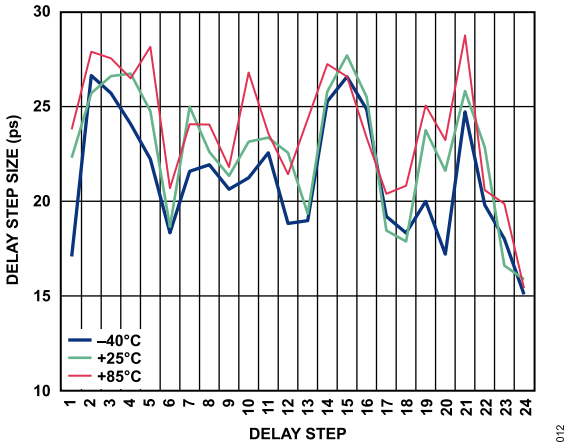

Figure 13. Analog Delay Step Size vs. Delay Step over Temperature, LVPECL at 983.04 MHz

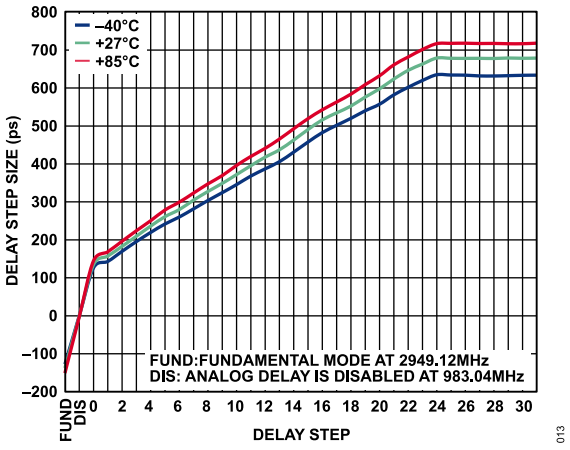

Figure 14. Analog Delay vs. Delay Setting over Temperature, LVPECL at 983.04 MHz

TYPICAL APPLICATION CIRCUITS

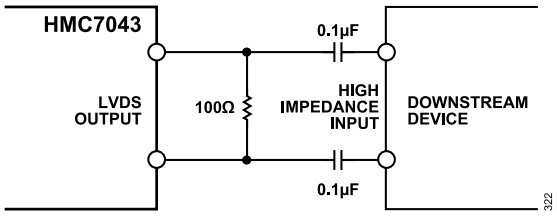

Figure 15. AC-Coupled LVDS Output Driver

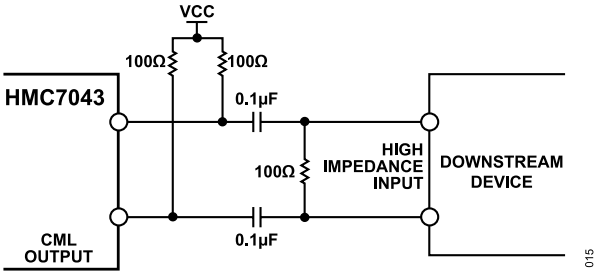

Figure 16. AC-Coupled CML (Configured High-Z) Output Driver

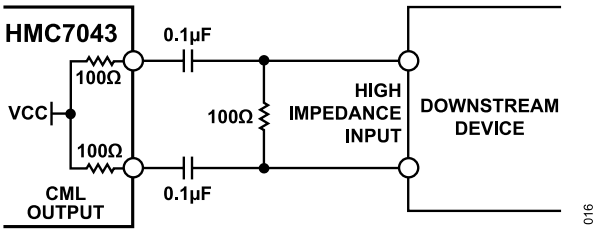

Figure 17. AC-Coupled CML (Internal) Output Driver

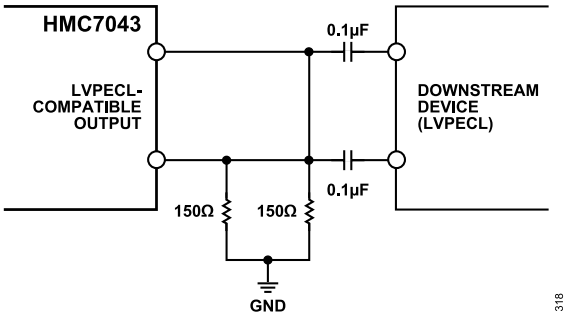

Figure 18. AC-Coupled LVPECL Output Driver

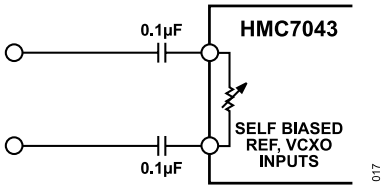

Figure 19. CLKIN/ $\overline{\text{CLKIN}}$, RFSYNCIN Input Differential Mode

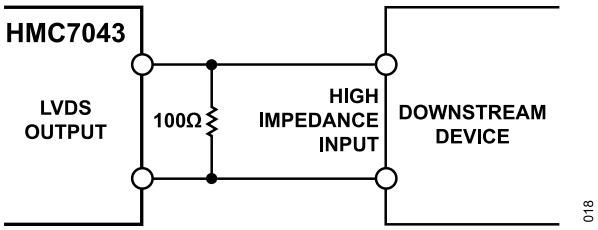

Figure 20. DC-Coupled LVDS Output Driver

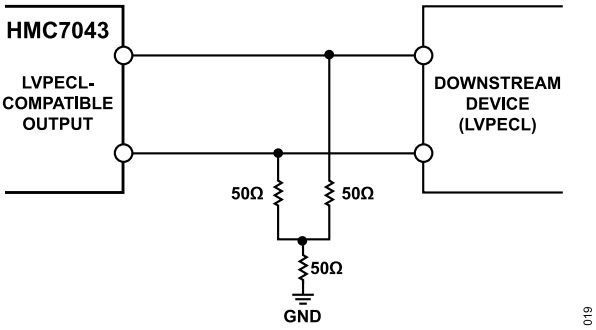

Figure 21. DC-Coupled LVPECL Output Driver

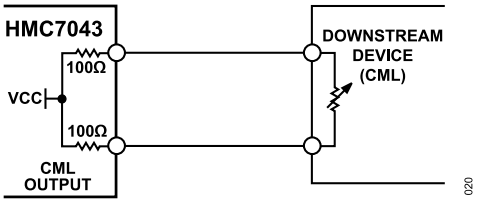

Figure 22. DC-Coupled CML (Internal) Output Driver

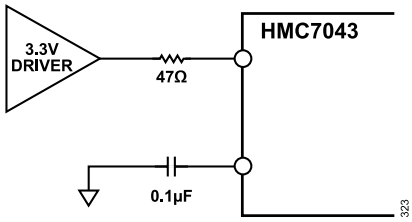

Figure 23. CLKIN, RFSYNCIN Input Single-Ended Mode

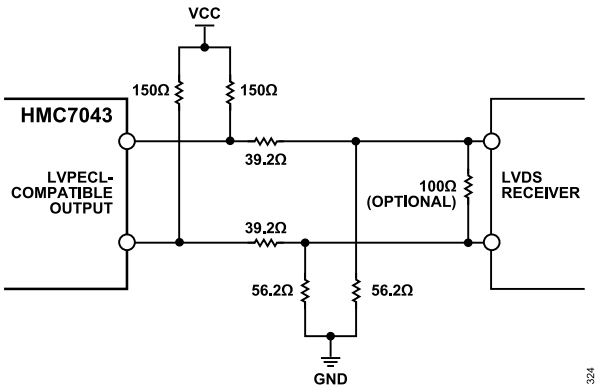

Figure 24. Level Translation for LVDS N-Pulse Operation (Place 100 Ω Termination Resistor If Receiver Does Not Have It.)

TERMINOLOGY

Phase Jitter and Phase Noise

An ideal sine wave has a continuous and even progression of phase with time from 0° to 360° for each cycle. Actual signals, however, display a certain amount of variation from ideal phase progression over time. This phenomenon is phase jitter. Although many causes can contribute to phase jitter, one major cause is random noise, which is characterized statistically as being Gaussian (normal) in distribution.

This phase jitter leads to the energy of the sine wave in the frequency domain spreading out, producing a continuous power spectrum. This power spectrum is usually reported as a series of values whose units are dBc/Hz at a given offset in frequency from the sine wave (carrier). The value is a ratio (expressed in decibels) of the power contained within a 1 Hz bandwidth with respect to the power at the carrier frequency. For each measurement, the offset from the carrier frequency is also given.

It is meaningful to integrate the total power contained within some interval of offset frequencies (for example, 10 kHz to 10 MHz). This is the integrated phase noise over that frequency offset interval and can be readily related to the time jitter due to the phase noise within that offset frequency interval.

Phase noise has a detrimental effect on the performance of analog-to-digital converters (ADCs), digital-to-analog converters (DACs), and RF mixers. It lowers the achievable dynamic range of the converters and mixers, although they are affected in somewhat different ways.

Time Jitter

Phase noise is a frequency domain phenomenon. In the time domain, the same effect is exhibited as time jitter. When observing a sine wave, the time of successive zero crossings varies. In a square wave, the time jitter is a displacement of the edges from their ideal (regular) times of occurrence. In both cases, the variations in timing from the ideal are the time jitter. Because these variations are random in nature, the time jitter is specified in seconds root mean square (rms) or 1 sigma of the Gaussian distribution.

Time jitter that occurs on a sampling clock for a DAC or an ADC decreases the signal-to-noise ratio (SNR) and dynamic range of the converter. A sampling clock with the lowest possible jitter provides the highest performance from a given converter.

Additive Phase Noise

Additive phase noise is the amount of phase noise that is attributable to the device or subsystem being measured. The phase noise of any external oscillators or clock sources is subtracted, which makes it possible to predict the degree to which the device impacts the total system phase noise when used in conjunction with the various oscillators and clock sources, each of which contributes a phase noise to the total. In many cases, the phase noise of one element dominates the system phase noise. When there are multiple contributors to phase noise, the total is the square root of the sum of squares of the individual contributors.

Additive Time Jitter

Additive time jitter is the amount of time jitter that is attributable to the device or subsystem being measured. The time jitter of any external oscillators or clock sources is subtracted, which makes it possible to predict the degree to which the device impacts the total system time jitter when used in conjunction with the various oscillators and clock sources, each of which contributes a time jitter to the total. In many cases, the time jitter of the external oscillators and clock sources dominates the system time jitter.

THEORY OF OPERATION

The HMC7043 is a high performance, clock distribution IC designed for extending the number of clock signals across the system with minimal noise contribution. The device can be used for distributing the noise sensitive reference clocks for high speed data converters with either parallel or serial (JESD204B/C) interfaces, FPGAs, and local oscillators. The HMC7043 is designed to meet the requirements of demanding base station designs, and offers a wide range of clock management and distribution features to simplify baseband and radio card clock tree designs. The device provides 14 low noise and configurable outputs to offer flexibility in distributing clocks while applying frequency division, phase adjustment, cycle slip, and external signal synchronization options.

The HMC7043 generates up to seven DCLK and SYSREF clock pairs per the JESD204B/C interface requirements. The system designer can generate a lower number of DCLK and SYSREF pairs, and configure the remaining output signal paths as DCLKs, additional SYSREFs, or other reference clocks with independent phase and frequency adjustment. Frequency adjustment can be accomplished by selecting the appropriate output divider values.

One of the unique features of the HMC7043 is the independent flexible phase management of each of the 14 channels. Using a combination of divider slip based, digital (coarse) and analog (fine) delay adjustments, each channel can be programmed to have a different phase offset. The phase adjustment capability allows the designer to offset board flight time delay variations, match data converter sample windows, and meet JESD204B/C synchronization challenges. The output signal path design of the HMC7043 is implemented to ensure both linear phase adjustment steps and minimal noise perturbation when phase adjustment circuits are turned on.

The HMC7043 provides output clock signals of up to 3.2 GHz, while having the flexibility to support input reference frequencies of up to 6 GHz when the internal clock division blocks are turned on. The higher frequency support enables higher bandwidth RF designs, and allows for distribution of low noise RF phase-locked loop (PLL) voltage controlled oscillator (VCO) outputs as well as other critical clocks across the system.

One of the key challenges in JESD204B/C system designs is ensuring the synchronization of data converter frame alignment across the system, from the FPGA or digital front end (DFE) to ADCs and DACs through a large clock tree that may comprise multiple clock generation and distribution ICs.

There are two input paths on the HMC7043; one is for the clock signal that is distributed, and the other may be used as an external synchronization signal. In typical JESD204B/C systems, serial data converter interfaces, there may be a need to ensure that all clock signals that are sent to the data converters have phases which are controlled by an FPGA. By virtue of the RF SYNC input, the device ensures that output signals have a deterministic phase alignment to this synchronization input. The RF SYNC input can also implement multiple device clock trees by nesting more than one HMC7043 to generate an even larger clock distribution network, while still maintaining phase alignment across the clock tree.

Offering excellent crosstalk, frequency isolation, and spurious performance, the device generates independent frequencies in both single-ended and differential formats including LVPECL, LVDS, CML, and CMOS, and different bias conditions to offset varying board insertion losses. The outputs can also be programmed for AC or DC coupling and 50 Ω or 100 Ω internal and external termination options.

The HMC7043 is programmed via a 3-wire serial port interface (SPI). The HMC7043 is offered in a 48-lead, 7 mm × 7 mm, LFCSP package with the exposed pad to ground.

THEORY OF OPERATION

DETAILED BLOCK DIAGRAM

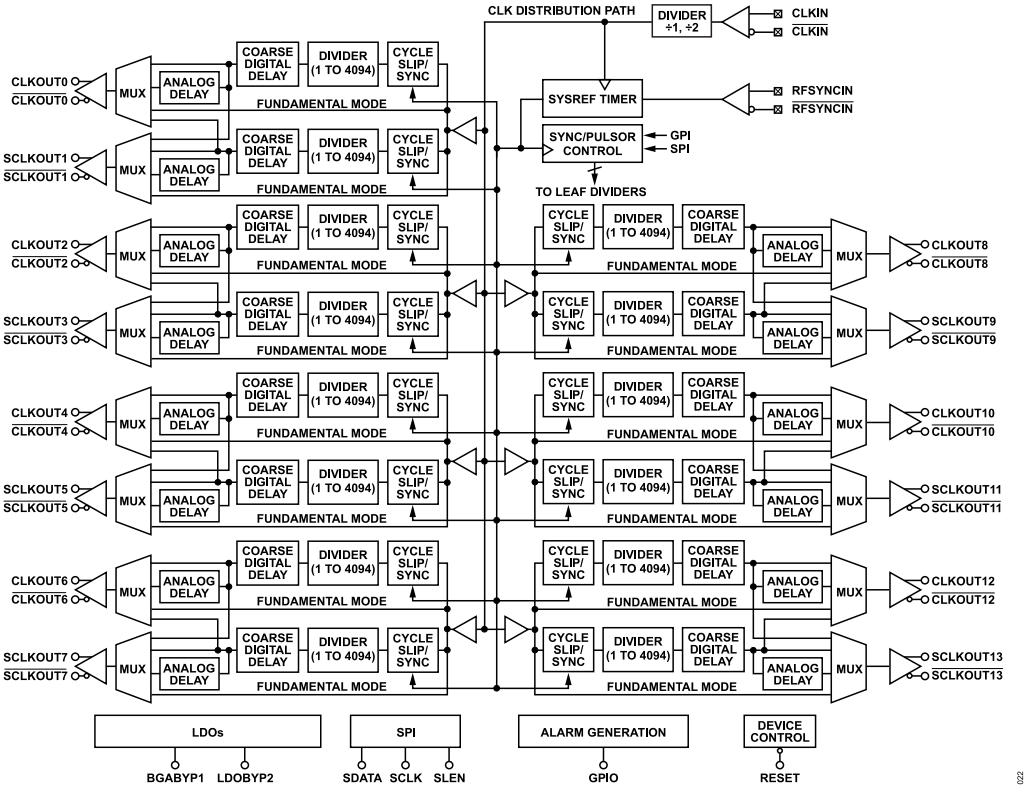

Figure 25. Detailed Block Diagram

CLOCK INPUT NETWORK

Input Termination Network—Common for All Input Buffers

The two clock and RFSYNC input buffers share similar architecture and control features. The input termination network is configurable to 100 Ω, 200 Ω, and 2 kΩ differentially. It is typically AC-coupled on the board, and uses the on-chip resistive divider to set the internal common-mode voltage, V_{CM}, to 2.1 V.

By closing the 50 Ω termination switch (see Figure 26), the network also can serve as the termination system for an LVPECL driver. Although the input termination network for the two clock and RFSYNC input buffers is identical, the buffer behind the network is different.

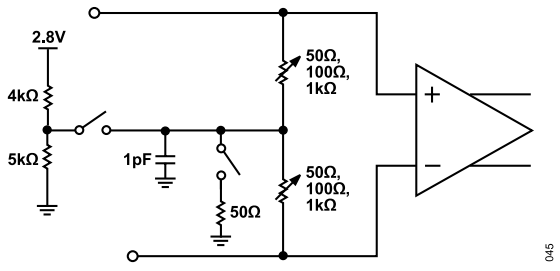

Figure 26. On-Chip Termination Network for Clock and RFSYNC Buffers

Recommendations for Normal Use

For both buffer types, unless there are extenuating circumstances in the application, use 100 Ω differential termination resistors to control reflections, to use the on-chip dc bias network to set the common mode level, and to externally ac couple the input signals in. Do not use a receiver side dc termination of the LVPECL signal.

Single-Ended Operation

The buffers can support a single-ended signal with slightly reduced input sensitivity and bandwidth. If driving any of the buffers single-ended, ac couple the unused leg of the buffer to ground at the input of the die.

Maximum Signal Swing Considerations

The internal supplies to these input buffers are supplied directly from 3.3 V. The ESD network and parasitic diodes can generally shunt away excess power and protect the internal circuits (withstanding reference powers above 13 dBm). Nevertheless, to protect from latch-up concerns, the signals on the reference inputs must not exceed the 3.3 V internal supply. For a 2.1 V common mode, 50 Ω single-ended source, this allows ~1200 mV of amplitude, or 11 dBm maximum reference power.

THEORY OF OPERATION

CLOCK OUTPUT NETWORK

The HMC7043 is a high performance clock buffer, is appropriate for JESD204B/C data converters, and much of the uniqueness of a JESD204B/C clock generation chip relates to the array of output channels. In this device, the output network requirements include the following:

- A large number of device clock (DCLK) and synchronization (SYSREF) channels
- Very good phase noise floor of the DCLK channels that can be connected to critical data converter sample clock inputs
- Deterministic phase alignment between all output channels relative to one another
- Fine phase control of synchronization channels with respect to the DCLK channel
- Frequency coverage to satisfy typical clock rates in systems
- Skew between SYSREF and DCLK channels that is much less than a DCLK period
- Spur and crosstalk performance that does not impact system budgets

The HMC7043 output network supports the following recommended features, which are sometimes critical in user applications:

- Deterministic synchronization of the output channels with respect to an external signal (RFSYNC), which allows multichip synchronization and clean expansion to larger systems
- Pulse generator behavior to temporarily generate a synchronization pulse stream at a user request
- The flexibility to define unused JESD204B/C SYSREF and DCLK channels for other purposes
- Glitchless phase control of signals relative to each other
- 50% duty cycle clocks with odd division ratios
- Multimode output buffers with a variety of swings and termination options
- Skew between all channels is much less than a DCLK period
- Adjustable performance vs. power consumption for less sensitive clock channels

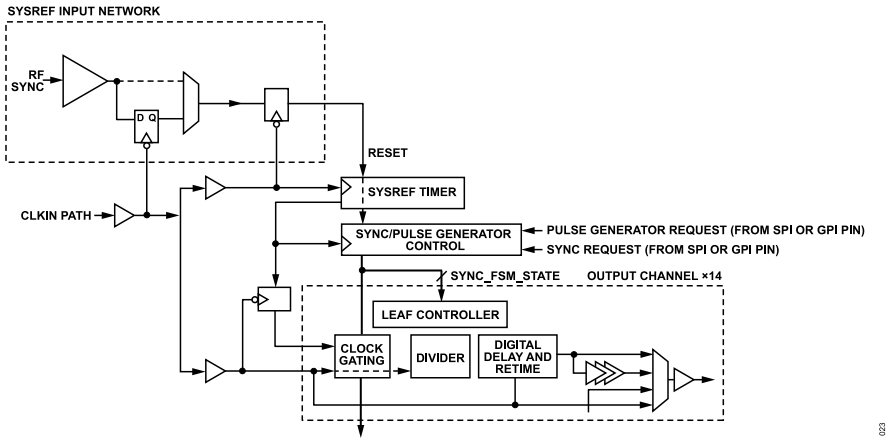

Figure 27. Clock Output Network Simplified Diagram

THEORY OF OPERATION

Each of the 14 output channels are logically identical. The only distinction between the SYSREF and DCLK channels is in the SPI configuration, and in how they are used. Each channel contains independent dividers, phase adjustment, and analog delay circuits. This combination provides the ultimate flexibility, cleanly accommodating nonJESD204B/C devices in the system.

In addition to the 14 output channel dividers, an internal SYSREF timer continually operates, and the synchronization of the output channel dividers occurs deterministically with respect to this timer, which the user can rephased deterministically by the user through GPI or SPI or deterministically by using the RFSYNCIN/ $\overline{\text{RFSYNCIN}}$ differential pins.

The pulse generator functionality of the JESD204B and JES204C standards involves temporarily generating SYSREF output pulses, with appropriate phasing, to downstream devices. The centralized SYSREF timer and the associated SYNC/pulse generator control manage the process of enabling the intended SYSREF channels, phasing them, and then disabling them for signal integrity and power saving advantages.

HMC7043 can provide continuous SYSREF clocks in LVPECL, CML, LVDS, and CMOS modes and N-pulse SYSREF clocks in LVPECL, CML, and CMOS modes. If N-pulse LVDS SYSREF clock is needed, output driver type must be set as LVPECL and level translation circuitry given in Figure 24 must be placed between clock channel and LVDS downstream device.

Basic Output Divider Channel

Each of the 14 output channels are logically identical, and support divide ratios from 1 to 4094. The supported odd divide ratios (1, 3, or 5) have 50.0% duty cycle. The only distinction between a SYSREF channel and a device clock channel is in the SPI configuration and the typical usage of a given channel.

For basic functionality and phase control, each output path consists of the following:

- Divider—generates the logic signal of the appropriate frequency and phase
- Digital phase adjust—adjusts the phase of each channel in increments of ½ clock input cycles
- Retimer—a low noise flip flop to retime the channel, removing any accumulated jitter
- Analog fine delay—provides a number of ~25 ps delay steps
- Selection mux—selects the fundamental, divider, analog delay, or an alternate path
- Multimode output buffer—low noise LVDS, CML, CMOS, or LVPECL

The digital phase adjuster and retimer launch on either clock phase of the clock input, depending on the digital phase adjust setpoint (Coarse Digital Delay[4:0]).

To support divider synchronization, arbitrary phase slips, and pulse generator modes, the following blocks are included:

- A clock gating stage pauses the clock for synchronization or slip operations
- An output channel leaf (×14) controller that manages slip, synchronization, and pulse generators with information from the SYSREF finite state machine (FSM)

Each channel has an array of control signals. Some of the controls are described in Table 11.

System wide broadcast signals can be triggered from the SPI or general-purpose input (GPI) port to issue a SYNC command (to align dividers to the system internal SYSREF timer), issue a pulse generator stream, (temporarily exporting SYSREF signals to receivers), or to cause the dividers to slip a number of clock input cycles to adjust their phases.

Individual dividers can be made sensitive to these events by adjusting their slip enable, SYNC enable, and Start-Up Mode[1:0] configuration, as described in Table 12.

When output buffers are configured in CMOS mode and phase alignment is required among the outputs, additional multislip delays must be issued for Channel 0, Channel 3, Channel 5, Channel 6, Channel 9, Channel 10, and Channel 13. The value of the delay must be as large as half of the selected divider ratio. Note that this requirement of having additional multislip delays is not needed when the channels are used in LVPECL, CML, or LVDS mode.

If a channel is configured to behave as a pulse generator, to temporarily power up and power down according to the GPI and SPI pulse generator commands; additional controls define the behavior outside of the pulse generator chain (see Table 13).

Each divider has an additional phase offset register that adjusts the start phase or influences the behavior of slip events sent via the SPI (see Table 14).

Table 15 outlines the typical configuration combinations for a DCLK channel relative to a SYSREF synchronization channel. Note that other combinations are possible. Synchronization of downstream devices can be managed manually, or by using the pulse generator functionality of the HMC7043. See the Typical Programming Sequence section for more information about the differences between the two methods.

THEORY OF OPERATION

Table 11. Basic Divider Controls

Bit Name	Description
Channel Enable	Channel enable. If set to 0, the channel is disabled. If set to 1, the channel can be enabled depending on the settings of the Start-Up Mode[1:0], Seven Pairs of 14-Channel Outputs Enable[6:0], and sleep mode bits.
12-Bit Channel Divider[11:0]	Divide ratio.12-bit divide ratio, split across two words (MSB and LSB). Set to 0 if not using the channel divider (Output Mux Selection[1:0] = 2 or 3)
High Performance Mode	High performance mode. Adjusts the divider and buffer bias to improve swing/phase noise slightly at the expense of power. The performance advantage is about 1 dB, and the current penalty depends on whether the divider is enabled.
Coarse Digital Delay[4:0]	Digital delay. Adjusts the phase of the divider signal by up to 17 ½ cycles of the clock input. This circuit is practically noiseless; however, note that a low amount of additional current is consumed.
Fine Analog Delay[4:0]	Analog delay. Adjusts the delay of the divider signal in increments of ~25 ps. Set Output Mux Selection[1:0] = 1 to expose this channel. Exposing this channel causes phase noise degradation of up to 12 dB; therefore, do not use on noise sensitive DCLK channels.
Output Mux Selection[1:0]	Output mux selection. 00 = divider channel, 01 = analog delay, 10 = other channel of pair, 11 = input clock. Fundamental mode can be generated with the divider (12-Bit Channel Divider[11:0] = 1), or via Output Mux Selection[1:0] = 10 and 12-Bit Channel Divider[11:0] = 0. Because the divider path consumes power and degrades phase noise slightly, the fundamental mux path is recommended, but at a cost of a deterministic skew vs. a path that is divider-based. Such skew can be compensated for with delay (digital and analog) on the divider-based path.
Force Mute[1]	Force mute. If 1, and the channel enable is true (channel enable = 1) and Force Mute[0] = 0, the signal just before the output buffer is asynchronously forced to Logic 0. To see the effect of this, the output buffer must be enabled, which is dependent on the dynamic driver enable and Start-Up Mode[1:0] controls.

Table 12. Channel Features

Bit Name	Description
Slip Enable	Slip enable. A channel processes slip requests broadcast from the SPI or GPI (or, if multislip enable = 1, initiated following a recognized SYNC or pulse generator startup).
SYNC Enable	SYNC enable. A channel processes synchronization events broadcast from the SPI or GPI or due to SYNC/RF SYNC (via the SYSREF FSM) to reset the phase. This signal can be safely toggled on and off to adjust SYNC sensitivity without risking the state of the divider.
Start-Up Mode[1:0]	00 = asynchronous (normal mode). The divider starts with uncontrolled phase. It is rephased by SYNC events if SYNC enable = 1. 11 = dynamic (pulse generator mode). The divider monitors pulse generator events broadcast from the SYSREF controller. It is powered up just before a pulse generator chain, rephased at the start, and powered down after the pulse generator chain. This mode is only supported for divide ratios > 31.

Table 13. Pulse Generator Mode Behavior Options

Bit Name	Description
Dynamic Driver Enable	Dynamic output buffer enable (pulse generator mode only). 0 = the output buffer is simply enabled/disabled with the main channel enable. 1 = the output buffer enable is controlled together with the channel divider, which allows it to dynamically power down outside pulse generator events.
Force Mute[0]	Idle at Logic 0 (pulse generator mode only). 1 = if the buffer remains on outside of the pulse generator chain, drive to Logic 0. 0 = if the buffer remains on outside of the pulse generator chain, allow the outputs to float naturally to approximately V_{CM}.

Table 14. Multislip Configuration

Bit Name	Description
Multislip Enable	Allow multislip. This bit determines whether the 12-Bit Multislip Digital Delay[11:0] parameter is used for multislip operations. Note that a multislip operation is automatically started following a SYNC or pulse generator initiation if multislip enable = 1.
12-Bit Multislip Digital Delay[11:0]	Multislip amount. If multislip enable = 1, any slip events (caused by GPI, SPI, SYNC, or pulse generator events) repeat the number of times set by 12-Bit Multislip Digital Delay[11:0] to adjust the phase by the multislip amount × clock input cycles. A value of 0 is not supported if multislip enable = 1. Note that phase slips are free from a noise and current perspective, that is, no additional power is needed and with no noise degradation, but they take some time to occur. Each slip operation takes a number of nanoseconds to complete, and thus the phases do not necessarily stabilize immediately. An alarm is available for the user to indicate when all phase operations are complete.

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Table 15. Typical Configuration Combinations

Bit Name	DCLK	Pulse Generator SYSREF	Manual SYSREF	NonJESD204B
12-Bit Channel Divider[11:0]	Small	Big	Big	Any
Start-Up Mode-Bit	Normal	Pulse generator	Normal	Normal
Fine Analog Delay[4:0]	Off	Optional	Optional	Off
Coarse Digital Delay[4:0]	Optional	Optional	Optional	Optional
Slip Enable	Optional	Optional	Optional	Optional
Multislip Enable	Optional	Off	Optional	Optional
High Performance Mode	Optional	Off	Off	Optional
Sync Enable	On	On	On	Optional
Dynamic Driver Enable	Don't care	On	Don't care	Don't care
Force Mute[1:0]	Don't care	On	Don't care	Don't care

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Synchronization FSM/Pulse Generator Timing

Figure 27 show a block diagram of the interface of the SYNC/ pulse generator control to the divider channels and the internal SYSREF timer.

The SYSREF timer counts in periods defined by SYSREF Timer[11:0], a 12-bit setting from the SPI. The SYSREF timer sequences the enable, reset, and startup, and disables the downstream dividers in the event of sync or pulse generator requests. Program the SYSREF timer count to a submultiple of the lowest output frequency in the clock network, and never faster than 4 MHz. To synchronize the divider channels, it is recommended, though not required, that the SYSREF Timer[11:0] bits be set to a related frequency that is either a factor or multiple of other frequencies on the IC.

The pulse generator is defined with respect to the periods of this SYSREF timer, not with respect to the output period. This behavior of the pulse generator leads to a timing constraint that must be considered to prevent any runt pulses from affecting the pulse generator stream.

Figure 29 shows the start-up behavior of an example divider that is configured as a pulse generator, with a period matching the internal SYSREF period.

The startup of the pulse stream occurs a fixed number of clock input cycles after the FSM transitions to the start phase. Disabling the pulse generator stream where the logic path is forced to zero comes from a combinational path directly from the FSM.

Because the divider has the option for nearly arbitrary phase adjustment, the stop condition can arrive when the pulse stream is a Logic 1 and create a runt pulse.

For phase offsets of zero to (50% − 8) clock input cycles, and at clock input frequencies <3 GHz, this condition is met naturally within the design. For clock input frequencies >3 GHz, it is recommended to use digital delay or slip offsets to increase the natural phase offset and avoid the stress conditions.

The situation is avoided by never applying phase offset more than (50% − 8) clock input cycles to an output channel configured as a pulse generator.

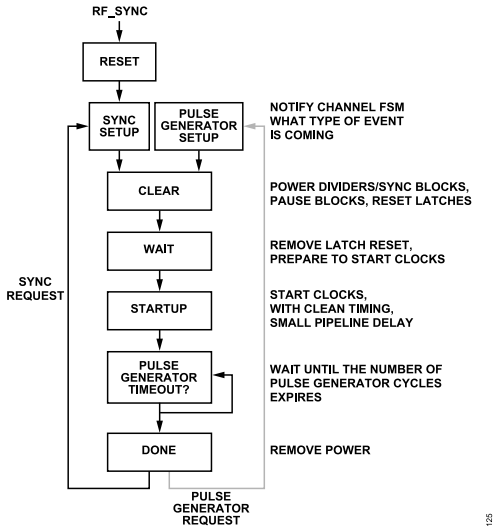

Figure 28. Synchronization FSM Flowchart

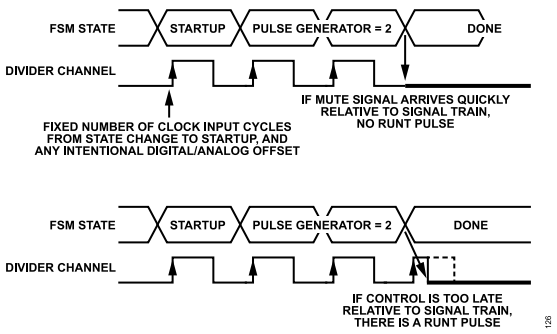

Figure 29. Start-Up Behavior of an Example Divider Configured as a Pulse Generator

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Clock Grouping, Skew, and Crosstalk

Although the output channels are logically independent, for physical reasons, they are first grouped into pairs, called clock groups. Each clock group shares a reference, an input buffer, and a SYNC retime flip flop originating from the clock distribution network.

The second level of grouping is according to the supply pin. Clock Group 1 (Channel 2 and Channel 3) is on an independent supply, and the other supply pins are each responsible for two clock groups.

As the output channels are more tightly coupled (by sharing a clock group or by sharing a supply pin), the skew is minimized. However, the isolation between those channels suffers.

Table 16 shows the clock grouping by location, and Table 17 show the typical skew and isolation that can be expected and how it scales with distance between output channels.

Isolation improves as either the aggressor or the affected frequencies decrease. Nevertheless, for particularly important clock channels where spurious tones must be minimized, carefully consider their frequency and channel configurations to isolate continuously running frequencies onto different supply domains. Channels configured as pulse generators are normally not an issue, because they are disabled during normal operation.

Table 16. Supply Pin Clock Grouping by Location

Supply Pin	Location	Clock Group	Channel
VCC2_OUT	Southwest	1	2
			3
VCC3_OUT	South	2	4
			5
		3	6
			7
VCC6_OUT	Northeast	4	8
			9
		5	10
			11
VCC7_OUT	Northwest	6	12
			13
		0	0
			1

Table 17. Typical Skew and Isolation vs. Distance

Distance	Typical Skew (ps)	1 GHz Isolation, Differential (dB)
Distant Supply Group	±20	90 to 100
Closest Neighbor on Different Supply Group	±15	70
Shared Supply	±10	60
Same Clock Group	±10	45

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Output Buffer Details

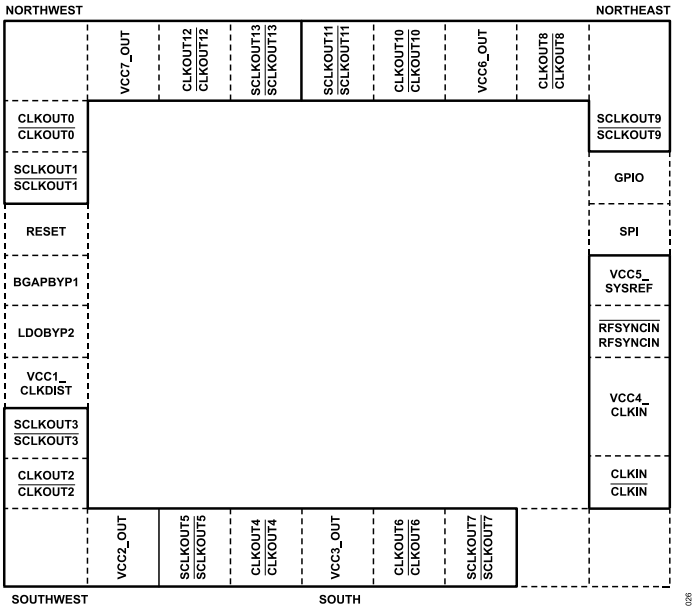

Figure 30. Clock Grouping

Figure 30 shows the clock groups by supply pin location on the package. With appropriate supply pin bypassing, the spurious noise of the outputs is improved.

Table 16 describes how the supply pins of each of the 14 clock channels are connected within the seven clock groups. Clock channels that are closest to each other have the best channel to channel skew performance, but they also have the lowest isolation from each other. Select critical signals that require high isolation from each other from groups with distant supply pin locations. An example of the expected isolation and channel to channel skew performance of the HMC7043 at 1 GHz is provided in Table 17.

SYSREF Valid Interrupt

One of the challenges in JESD204B/C systems is to control and minimize the latency from the primary system controller IC, typically an ASIC or FPGA, to the data converters. To estimate the correct amount of latency in the system, the designer must know the time required for a main clock generator like the HMC7043 to provide the correct output phases at each output channel after receiving the synchronization request. Typically, a period of time is required on the device to implement the change requests on the outputs due to internal state machine cycles, data transfers, and any propagation delays. The SYSREF valid interrupt is a function to notify the user that the correct output settings and phase relationships are established, allowing the user to identify quickly that the desired SYSREF and device clock states are presented at the outputs of the HMC7043.

The user has the flexibility to assign the SYSREF valid interrupt to a GPO pin or to use a software flag, set via Register 0x007D, Bit 2, which the user may poll as necessary. The flag notifies the user when the system is configured and operating in the desired state, or conversely when it is not ready.

PHASE BEHAVIOR OF SYNCHRONIZED DIVIDED CLOCKS

When the output dividers of HMC7043 are synchronized, division ratios larger than 1 may lead to instances of synchronization failure under cold temperatures or low supply voltages. This may result in the first falling edge shifting by ±4 VCO (ΔT) cycles, causing all following pulses or clock cycles to shift by the same number of VCO cycles. Figure 31 shows the timing diagram of this behavior. This issue was resolved on the HMC7043B, which is a form, fit, and functional compatible device with the HMC7043. For new designs, the HMC7043B is recommended for use instead of the HMC7043. Contact the factory for more information.

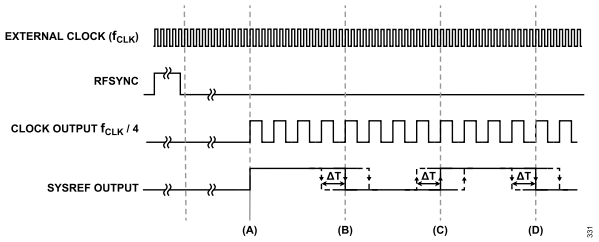

Figure 31. Timing Diagram of Intermittent Edge Shift Behavior

TYPICAL PROGRAMMING SEQUENCE

To initialize the HMC7043 to an operational state, use the following programming procedure:

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1. Connect the HMC7043 to the rated power supplies. No specific power supply sequencing is necessary.
2. Release the hardware reset by switching from Logic 1 to Logic 0 when all supplies are stable.
3. Load the configuration updates (provided by Analog Devices, Inc.) to specific registers (see Table 41).
4. Program the SYSREF timer. Set the divide ratio (a submultiple of the lower output channel frequency). Set the pulse generator mode configuration, for example, selecting the level sensitivity option and the number of pulses desired.
5. Program the output channels. Set the output buffer modes (for example, LVPECL, CML, and LVDS). Set the divide ratio, channel start-up mode, coarse/analog delays, and performance modes.
6. Ensure the clock input signal are provided to CLKIN.
7. Issue a software restart to reset the system and initiate calibration. Toggle the restart dividers/FSMs bit to 1 and then back to 0.
8. Send a sync request via the SPI (set the reseed request bit) to align the divider phases and send any initial pulse generator stream.
9. Wait six SYSREF periods (6 × SYSREF Timer[11:0]) to allow the outputs to phase appropriately (~3 µs in typical configurations).
10. Confirm that the outputs have all reached their phases by checking that the clock outputs phases status bit = 1.
11. At this time, initialize any other devices in the system. Configure the JESD204B/C nodes in the system to operate with the SYSREF signal outputs from the HMC7043. The SYSREF channels from the HMC7043 can be on either asynchronously or dynamically, and may temporarily turn on for a pulse generator stream.
12. JESD204B/C node devices in the system must be configured to monitor the input SYSREF signal exported from the HMC7043 At this point, SYSREF channels from the HMC7043 can either be on asynchronously (running) or on dynamically (temporarily turn on for a pulse generator train).
13. When all JESD204B/C nodes are powered and ready, send a pulse generator request to send out a pulse generator chain on any SYSREF channels programmed for pulse generator mode.

The system is initialized.

For power savings and the reduction of the cross coupling of frequencies on the HMC7043 shut down the SYSREF channels.

1. Program each JESD204B/C node to ignore the SYSREF input channel.
2. On the HMC7043, disable the individual channel enable bits of each SYSREF channel.

To resynchronize one or more of the JESD204B/C nodes, use the following procedure:

1. Set the channel enable and SYNC enable bit of the SYSREF channel of interest.
2. To prevent an output channel from responding to a sync request, disable the SYNC enable mask of each channel so that it continues to run normally without a phase adjustment.
3. Issue a reseed request to phase the SYSREF channel properly with respect to the DCLK.
4. Enable the JESD204B/C node sensitivity to the SYSREF channel.
5. If the SYSREF channel is in pulse generator mode, wait at least 20 SYSREF periods from Step 3, and issue a pulse generator request.

POWER SUPPLY CONSIDERATIONS

The output buffers are susceptible to supply with a certain extent. The output buffers are also susceptible to supply noise, but to a lesser extent. A noise tone of −60 dBV at a 40 MHz offset results in a −90 dBc tone at the output of the buffers in CML mode and −85 dBc in LVPECL mode. This result is a relatively flat frequency response, and these numbers are measured differentially. Phase noise/spurs caused by supply noise on the output buffers do not scale with output frequency.

Table 18 lists the supply network of the HMC7043 by pin, showing the relevant functional blocks. Three different usage profiles are defined for the network, not including the output channel supplies, which are accounted for separately.

The values listed under Profile 0 to Profile 2 in Table 18 and Table 19 are the typical currents of that block or feature. If a number is not listed in a profile column, a typical profile does not exist for that block or feature, but the user can mix and match features outside of the profile list, and can determine what the power consumption is going to be given the current listings per feature.

Table 18. Supply Network of the HMC7043 by Pin for the Clock Output Network

			Profile[1]		
Circuit Block	**Comment**	**Typical Current (mA)**	**0**	**1**	**2**
VCC1_CLKDIST					
Regulator to 1.8 V, Bypassed on LDOBYP2		2	2	2	2
SYSREF Timer		1		1	
GPO Driver in High Speed Mode[2]					
Clock Input Distribution Network	Minimum possible value	84	8	84	34

THEORY OF OPERATION

Table 18. Supply Network of the HMC7043 by Pin for the Clock Output Network (Continued)

Circuit Block	Comment	Typical Current (mA)	Profile[1] 0	1	2
Sync Retiming Network	Minimum possible value[3]	8			
Subtotal for VCC1_CLKDIST			10	87	36
VCC4_CLKIN					
CLKIN/ $\overline{\text{CLKIN}}$ Buffer		16		16	16
CLKIN/ $\overline{\text{CLKIN}}$ Path	Extra current for divide by 2	7			
RFSYNCIN/$\overline{\text{RFSYNCIN}}$[4] Retimer		3			
RFSYNCIN/$\overline{\text{RFSYNCIN}}$ Buffer		9			
Subtotal or VCC4_CLKIN			0	16	16
VCC5_SYSREF					
SYSREF Input Network		11		11	
SYSREF Counter Base		12		12	
SYSREF Counter, SYNC Network		4			
Subtotal for VCC5_SYSREF		27	0	23	0
Subtotal (Without Output Paths)			10	126	52

[1] Profile 0 is sleep mode; Profile 1 is power-up defaults, SYSREF timer running and RFSYNC buffer is disabled; Profile 2 is only one clock output enabled, SYSREF timer is not running and RFSYNC buffer is disabled.

[2] The current is highly dependent on rate of input/output and load of input/output traces. For heavily loaded traces, it is recommended to use a series resistance of ~100 Ω to minimize the IR drop on the internal regulator during transitions.

[3] A temporary current only.

[4] Transient current in synchronization mode, can be temporarily enabled when using external synchronization.

Table 19. Supply Network of the HMC7043 by Block for the Clock Output Network

Per Output Channel	Comment	Typical Current (mA)	Profile[1] 0	1	2	3	4
Digital Regulator and Other Sources		2.5	0.5	2.5	2.5	2.5	2.5
Buffer							
LVPECL	Including term currents	43		43	43		43
CML100							
High Power	Including term currents	31					
Low Power		24					
LVDS							
High Power	At 307 MHz	10				10	
Low Power		8					
CMOS	At 100 MHz, both sections	25					
Channel Mux		Included[2]					
Different Power Modes Deleted		2	2	2			2
Digital Delay							
Off		Included[2]					
Setpoint > 1		3			3		3
Analog Delay							
Off		Included[2]		0			
Minimum Setting	Glitchless mode enabled	9			9		
Maximum Setting		9					9
Divider Logic							
0	Not using divider path	Included[2]		0		0	
÷1		27					

THEORY OF OPERATION

Table 19. Supply Network of the HMC7043 by Block for the Clock Output Network (Continued)

Per Output Channel	Comment	Typical Current (mA)	Profile[1]				
			0	1	2	3	4
÷2		24					
÷3		31					
÷4		28					
÷5		30					
÷6		26					
÷8		28					
÷16		29			29		
÷32		29					
÷2044		29					29
SYNC Logic[3]		4					
Slip Logic[3]		4					
Subtotal			2.5	48	87	13	89

[1] Profile 0 is sleep mode; Profile 1 is fundamental mode; Profile 2 is SYSREF channel matched to fundamental mode; Profile 3 is LVDS—high power signal source from other channel; and Profile 4 is worst case configuration for power consumption of a channel.

[2] The base current consumption of the circuit (for example, mux) is included in the buffer typical current.

[3] Currents only occur temporarily during a synchronization event.

SERIAL CONTROL PORT

SERIAL PORT INTERFACE (SPI) CONTROL

The HMC7043 can be controlled via the SPI using 24-bit registers and three pins: serial port enable (SLEN) serial data input/output (SDATA), and serial clock (SCLK).

The 24-bit register, shown in Table 20, consists of the following:

- 1-bit read/write command
- 2-bit multibyte field (W1, W0)
- 13-bit address field (A12 to A0)
- 8-bit data field (D7 to D0)

Table 20. SPI Bit Map

MSB				LSB
Bit 23	**Bit 22**	**Bit 21**	**Bits[20:8]**	**Bits[7:0]**
R/W	W1	W0	A12 to A0	D7 to D0

Typical Read Cycle

A typical read cycle is shown in Figure 32 and occurs as follows:

1. The controller asserts both SLEN and SDATA to indicate a read, followed by a rising edge SCLK. The HMC7043 reads SDATA on the first rising edge of SCLK after SLEN. Setting SDATA high initiates a read.
2. The host places the 2-bit multibyte field to be written to low (0) on the next two falling edges of SCLK. The HMC7043 registers the 2-bit multibyte field on the next two rising edges of SCLK.
3. The host places the 13-bit address field (A12 to A0) MSB first on SDATA on the next 13 falling edges of SCLK. The HMC7043 registers the 13-bit address field (MSB first) on SDATA over the next 13 rising edges of SCLK.
4. The host registers the 8-bit data on the next eight rising edges of SCLK. The HMC7043 places 8-bit data (D7 to D0) MSB first on the next eight falling edges of SCLK.
5. Deassertion of SLEN completes the register read cycle.

Typical Write Cycle

A typical write cycle is shown in Figure 33 and occurs as follows:

1. The host asserts both SLEN and SDATA to indicate a read, followed by a rising edge SCLK. The HMC7043 reads SDIO on the first rising edge of SCLK after SLEN. Setting SDATA low initiates a write.
2. The host places the 2-bit multibyte field to be written to low (0) on the next two falling edges of SCLK. The HMC7043 registers the 2-bit multibyte field on the next two rising edges of SCLK.
3. The host places the13-bit address field (A12 to A0), MSB first, on SDATA on the next 13 falling edges of SCLK. The HMC7043 registers the 13-bit address field (MSB first) on SDIO over the next 13 rising edges of SCLK.
4. The host places the 8-bit data (D7 to D0) MSB first on the next eight falling edges of SCLK. The HMC7043 register the 8-bit data (D7 to D0) MSB first on the next eight rising edges of SCLK.
5. The final rising edge of SCLK performs the internal data transfer into the register file, updating the configuration of the device.
6. Deassertion of SLEN completes the register write cycle.

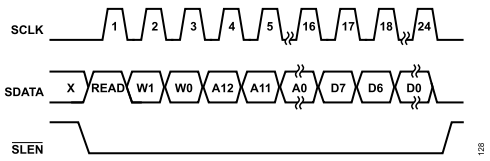

Figure 32. SPI Timing Diagram, Read Operation

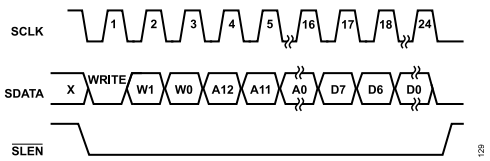

Figure 33. SPI Timing Diagram, Write Operation

CONTROL REGISTERS

CONTROL REGISTER MAP

Table 21. Control Register Map

Address (Hex)	Register Name	Bit 7 (MSB)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSB)	Default Value (Hex)
Global Control										
0x0000	Global soft reset control	Reserved							Soft reset	0x00
0x0001	Global request and mode control	Reseed request	High performance distribution path	Reserved	Reserved	Mute output drivers	Pulse generator request	Restart dividers/ FSMs	Sleep mode	0x00
0x0002		Reserved						Multislip request	Reserved	0x00
0x0003	Global enable control	Reserved		RF reseeder enable	Reserved		SYSREF timer enable	Reserved	Reserved	0x34
0x0004		Reserved	Seven Pairs of 14-Channel Outputs Enable[6:0]							0x7F
0x0005	Global mode and enable control	Reserved								0x0F
0x0006	Global clear alarms	Reserved							Clear alarms	0x00
0x0007	Global miscellaneous control	Reserved								0x00
0x0008		Reserved (scratchpad)								0x00
0x0009		Reserved								0x00
Input Buffer										
0x000A	RFSYNCIN/ $\overline{\text{RFSYNCIN}}$ input buffer control	Reserved			Input Buffer Mode[3:0]				Buffer enable	0x07
0x000B	CLKIN/ $\overline{\text{CLKIN}}$ input buffer control	Reserved			Input Buffer Mode[3:0]				Buffer enable	0x07
GPIO/SDATA Control										
0x0046	GPI control	Reserved				GPI Selection [2:0]			GPI enable	0x00
0x0050	GPO control	Reserved	GPO Selection[4:0]					GPO mode	GPO enable	0x37
0x0054	SDATA control	Reserved						SDATA mode	SDATA enable	0x03
SYSREF/SYNC										
0x005A	Pulse generator control	Reserved					Pulse Generator Mode Selection[2:0]			0x00
0x005B	SYNC control	Reserved					SYNC retime	Reserved	SYNC invert polarity	0x04
0x005C	SYSREF timer control	SYSREF Timer[7:0] (LSB)								0x00
0x005D		Reserved				SYSREF Timer[11:8](MSB)				0x01
Clock Distribution Network										
0x0064	Clock input control	Reserved						Divide by 2 on clock input	Low frequency clock input	0x00
0x0065	Analog delay common control	Reserved							Analog delay low power mode	0x00
Alarm Masks Register										

CONTROL REGISTERS

Table 21. Control Register Map (Continued)

Address (Hex)	Register Name	Bit 7 (MSB)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSB)	Default Value (Hex)
0x0071	Alarm mask control	Reserved			Sync request mask	Reserved	Clock outputs phase status mask	SYSREF sync status mask	Reserved	0x10
Product ID Registers										
0x0078	Product ID	Product ID Value[7:0] (LSB)								0xF1
0x0079		Product ID Value[15:8] (Mid)								0x79
0x007A		Product ID Value[23:16] (MSB)								0x04
Alarm Readback Status Registers										
0x007B	Readback register	Reserved							Alarm signal	
0x007D	Alarm readback	Reserved			Sync request status	Reserved	Clock outputs phases status	SYSREF sync status	Reserved	
0x007F	Alarm readback	Reserved								
SYSREF Status Register										
0x0091	SYSREF status register	Reserved			Channel outputs FSM busy	SYSREF FSM State[3:0]				0x00
Other Controls										
0x0098	Reserved	Reserved								0x00
0x0099	Reserved	Reserved								0x00
0x009D	Reserved	Reserved								0xAA
0x009E	Reserved	Reserved								0xAA
0x009F	Reserved	Reserved (Clock output driver low power setting, set to 0x4D instead of default value)								0x55
0x00A0	Reserved	Reserved (Clock output driver low power setting, set to 0xDF instead of default value)								0x56
0x00A2	Reserved	Reserved								0x03
0x00A3	Reserved	Reserved								0x00
0x00A4	Reserved	Reserved								0x00
0x00AD	Reserved	Reserved								0x00
0x00B5	Reserved	Reserved								0x00
0x00B6	Reserved	Reserved								0x00
0x00B7	Reserved	Reserved								0x00
0x00B8	Reserved	Reserved								0x00
Clock Distribution										
0x00C8	Channel Output 0 control	High performance mode	SYNC enable	Slip enable	Reserved	Start-Up Mode[1:0]		Multislip enable	Channel enable	0xF3
0x00C9		12-Bit Channel Divider[7:0] (LSB)								0x04
0x00CA		Reserved				12-Bit Channel Divider[11:8] (MSB)				0x00
0x00CB		Reserved			Fine Analog Delay[4:0]					0x00
0x00CC		Reserved			Coarse Digital Delay[4:0]					0x00
0x00CD		12-Bit Multislip Digital Delay[7:0] (LSB)								0x00
0x00CE		Reserved				12-Bit Multislip Digital Delay[11:8] (MSB)				0x00
0x00CF		Reserved						Output Mux Selection[1:0]		0x00

CONTROL REGISTERS

Table 21. Control Register Map (Continued)

Address (Hex)	Register Name	Bit 7 (MSB)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSB)	Default Value (Hex)
0x00D0		Idle at Zero[1:0]		Dynamic driver enable	Driver Mode[1:0]		Reserved	Driver Impedance[1:0]		0x01
0x00D2	Channel Output 1 control	High performance mode	SYNC enable	Slip enable	Reserved	Start-Up Mode[1:0]		Multislip enable	Channel enable	0xFD
0x00D3		12-Bit Channel Divider[7:0] (LSB)								0x00
0x00D4		Reserved				12-Bit Channel Divider[11:8] (MSB)				0x01
0x00D5		Reserved			Fine Analog Delay[4:0]					0x00
0x00D6		Reserved			Coarse Digital Delay[4:0]					0x00
0x00D7		12-Bit Multislip Digital Delay[7:0] (LSB)								0x00
0x00D8		Reserved				12-Bit Multislip Digital Delay[11:8] (MSB)				0x00
0x00D9		Reserved						Output Mux Selection[1:0]		0x00
0x00DA		Idle at Zero[1:0]		Dynamic driver enable	Driver Mode[1:0]		Reserved	Driver Impedance[1:0]		0x30
0x00DC	Channel Output 2 control	High performance mode	SYNC enable	Slip enable	Reserved	Start-Up Mode[1:0]		Multislip enable	Channel enable	0xF3
0x00DD		12-Bit Channel Divider[7:0] (LSB)								0x08
0x00DE		Reserved				12-Bit Channel Divider[11:8] (MSB)				0x00
0x00DF		Reserved			Fine Analog Delay[4:0]					0x00
0x00E0		Reserved			Coarse Digital Delay[4:0]					0x0
0x00E1		12-Bit Multislip Digital Delay[7:0] (LSB)								0x00
0x00E2		Reserved				12-Bit Multislip Digital Delay[11:8] (MSB)				0x00
0x00E3		Reserved						Output Mux Selection[1:0]		0x00
0x00E4		Idle at Zero[1:0]		Dynamic driver enable	Driver Mode[1:0]		Reserved	Driver Impedance[1:0]		0x01
0x00E6	Channel Output 3 control	High performance mode	SYNC enable	Slip enable	Reserved	Start-Up Mode[1:0]		Multislip enable	Channel enable	0xFD
0x00E7		12-Bit Channel Divider[7:0] (LSB)								0x00
0x00E8		Reserved				12-Bit Channel Divider[11:8] (MSB)				0x01
0x00E9		Reserved			Fine Analog Delay[4:0]					0x00
0x00EA		Reserved			Coarse Digital Delay[4:0]					0x00
0x00EB		12-Bit Multislip Digital Delay[7:0] (LSB)								0x00
0x00EC		Reserved				12-Bit Multislip Digital Delay[11:8] (MSB)				0x00
0x00ED		Reserved						Output Mux Selection[1:0]		0x00
0x00EE		Idle at Zero[1:0]		Dynamic driver enable	Driver Mode[1:0]		Reserved	Driver Impedance[1:0]		0x30
0x00F0	Channel Output 4 control	High performance mode	SYNC enable	Slip enable	Reserved	Start-Up Mode[1:0]		Multislip enable	Channel enable	0xF3
0x00F1		12-Bit Channel Divider[7:0] (LSB)								0x02
0x00F2		Reserved				12-Bit Channel Divider[11:8] (MSB)				0x00
0x00F3		Reserved			Fine Analog Delay[4:0]					0x00
0x00F4		Reserved			Coarse Digital Delay[4:0]					0x00

CONTROL REGISTERS

Table 21. Control Register Map (Continued)

Address (Hex)	Register Name	Bit 7 (MSB)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSB)	Default Value (Hex)
0x00F5		12-Bit Multislip Digital Delay[7:0] (LSB)								0x00
0x00F6		Reserved				12-Bit Multislip Digital Delay[11:8] (MSB)				0x00
0x00F7		Reserved						Output Mux Selection[1:0]		0x00
0x00F8		Idle at Zero[1:0]		Dynamic driver enable	Driver Mode[1:0]		Reserved	Driver Impedance[1:0]		0x01
0x00FA	Channel Output 5 control	High performance mode	SYNC enable	Slip enable	Reserved	Start-Up Mode[1:0]		Multislip enable	Channel enable	0xFD
0x00FB		12-Bit Channel Divider[7:0] (LSB)								0x00
0x00FC		Reserved				12-Bit Channel Divider[11:8] (MSB)				0x01
0x00FD		Reserved			Fine Analog Delay[4:0]					0x00
0x00FE		Reserved			Coarse Digital Delay[4:0]					0x00
0x00FF		12-Bit Multislip Digital Delay[7:0] (LSB)								0x00
0x0100		Reserved				12-Bit Multislip Digital Delay[11:8] (MSB)				0x00
0x0101		Reserved						Output Mux Selection[1:0]		0x00
0x0102		Idle at Zero[1:0]		Dynamic driver enable	Driver Mode[1:0]		Reserved	Driver Impedance[1:0]		0x30
0x0104	Channel Output 6 control	High performance mode	SYNC enable	Slip enable	Reserved	Start-Up Mode[1:0]		Multislip enable	Channel enable	0xF3
0x0105		12-Bit Channel Divider[7:0] (LSB)								0x02
0x0106		Reserved				12-Bit Channel Divider[11:8] (MSB)				0x00
0x0107		Reserved			Fine Analog Delay[4:0]					0x00
0x0108		Reserved			Coarse Digital Delay[4:0]					0x00
0x0109		12-Bit Multislip Digital Delay[7:0] (LSB)								0x00
0x010A		Reserved				12-Bit Multislip Digital Delay[11:8] (MSB)				0x00
0x010B		Reserved						Output Mux Selection[1:0]		0x00
0x010C		Idle at Zero[1:0]		Dynamic driver enable	Driver Mode[1:0]		Reserved	Driver Impedance[1:0]		0x01
0x010E	Channel Output 7 control	High performance mode	SYNC enable	Slip enable	Reserved	Start-Up Mode[1:0]		Multislip enable	Channel enable	0xFD
0x010F		12-Bit Channel Divider[7:0] (LSB)								0x00
0x0110		Reserved				12-Bit Channel Divider[11:8] (MSB)				0x01
0x0111		Reserved			Fine Analog Delay[4:0]					0x00
0x0112		Reserved			Coarse Digital Delay[4:0]					0x00
0x0113		12-Bit Multislip Digital Delay[7:0] (LSB)								0x00
0x0114		Reserved				12-Bit Multislip Digital Delay[11:8] (MSB)				0x00
0x0115		Reserved						Output Mux Selection[1:0]		0x00
0x0116		Idle at Zero[1:0]		Dynamic driver enable	Driver Mode[1:0]		Reserved	Driver Impedance[1:0]		0x30
0x0118	Channel Output 8 control	High performance mode	SYNC enable	Slip enable	Reserved	Start-Up Mode[1:0]		Multislip enable	Channel enable	0xF3
0x0119		12-Bit Channel Divider[7:0] (LSB)								0x02

CONTROL REGISTERS

Table 21. Control Register Map (Continued)

Address (Hex)	Register Name	Bit 7 (MSB)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSB)	Default Value (Hex)
0x011A		Reserved				12-Bit Channel Divider[11:8] (MSB)				0x00
0x011B		Reserved			Fine Analog Delay[4:0]					0x00
0x011C		Reserved			Coarse Digital Delay[4:0]					0x00
0x011D		12-Bit Multislip Digital Delay[7:0] (LSB)								0x00
0x011E		Reserved				12-Bit Multislip Digital Delay[11:8] (MSB)				0x00
0x011F		Reserved						Output Mux Selection[1:0]		0x00
0x0120		Idle at Zero[1:0]		Dynamic driver enable	Driver Mode[1:0]		Reserved	Driver Impedance[1:0]		0x01
0x0122	Channel Output 9 control	High performance mode	SYNC enable	Slip enable	Reserved	Start-Up Mode[1:0]		Multislip enable	Channel enable	0xFD
0x0123		12-Bit Channel Divider[7:0] (LSB)								0x00
0x0124		Reserved				12-Bit Channel Divider[11:8] (MSB)				0x01
0x0125		Reserved			Fine Analog Delay[4:0]					0x00
0x0126		Reserved			Coarse Digital Delay[4:0]					0x00
0x0127		12-Bit Multislip Digital Delay[7:0] (LSB)								0x00
0x0128		Reserved				12-Bit Multislip Digital Delay[11:8] (MSB)				0x00
0x0129		Reserved						Output Mux Selection[1:0]		0x00
0x012A		Idle at Zero[1:0]		Dynamic driver enable	Driver Mode[1:0]		Reserved	Driver Impedance[1:0]		0x30
0x012C	Channel Output 10 control	High performance mode	SYNC enable	Slip enable	Reserved	Start-Up Mode[1:0]		Multislip enable	Channel enable	0xF3
0x012D		12-Bit Channel Divider[7:0] (LSB)								0x02
0x012E		Reserved				12-Bit Channel Divider[11:8] (MSB)				0x00
0x012F		Reserved			Fine Analog Delay[4:0]					0x00
0x0130		Reserved			Coarse Digital Delay[4:0]					0x00
0x0131		12-Bit Multislip Digital Delay[7:0] (LSB)								0x00
0x0132		Reserved				12-Bit Multislip Digital Delay[11:8] (MSB)				0x00
0x0133		Reserved						Output Mux Selection[1:0]		0x00
0x0134		Idle at Zero[1:0]		Dynamic driver enable	Driver Mode[1:0]		Reserved	Driver Impedance[1:0]		0x01
0x0136	Channel Output 11 control	High performance mode	SYNC enable	Slip enable	Reserved	Start-Up Mode[1:0]		Multislip enable	Channel enable	0xFD
0x0137		12-Bit Channel Divider[7:0] (LSB)								0x00
0x0138		Reserved				12-Bit Channel Divider[11:8] (MSB)				0x01
0x0139		Reserved			Fine Analog Delay[4:0]					0x00
0x013A		Reserved			Coarse Digital Delay[4:0]					0x00
0x013B		12-Bit Multislip Digital Delay[7:0] (LSB)								0x00
0x013C		Reserved				12-Bit Multislip Digital Delay[11:8] (MSB)				0x00
0x013D		Reserved						Output Mux Selection[1:0]		0x00
0x013E		Idle at Zero[1:0]		Dynamic driver enable	Driver Mode[1:0]		Reserved	Driver Impedance[1:0]		0x30

CONTROL REGISTERS

Table 21. Control Register Map (Continued)

Address (Hex)	Register Name	Bit 7 (MSB)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSB)	Default Value (Hex)
0x0140	Channel Output 12 control	High performance mode	SYNC enable	Slip enable	Reserved	Start-Up Mode[1:0]		Multislip enable	Channel enable	0xF3
0x0141		12-Bit Channel Divider[7:0] (LSB)								0x10
0x0142		Reserved				12-Bit Channel Divider[11:8] (MSB)				0x00
0x0143		Reserved			Fine Analog Delay[4:0]					0x00
0x0144		Reserved			Coarse Digital Delay[4:0]					0x00
0x0145		12-Bit Multi-Slip Digital Delay[7:0] (LSB)								0x00
0x0146		Reserved				12-Bit Multislip Digital Delay[11:8] (MSB)				0x00
0x0147		Reserved						Output Mux Selection[1:0]		0x00
0x0148		Idle at Zero[1:0]		Dynamic driver enable	Driver Mode[1:0]		Reserved	Driver Impedance[1:0]		0x01
0x014A	Channel Output 13 control	High performance mode	SYNC enable	Slip enable	Reserved	Start-Up Mode [1:0]		Multislip enable	Channel enable	0xFD
0x014B		12-Bit Channel Divider[7:0] (LSB)								0x00
0x014C		Reserved				12-Bit Channel Divider[11:8] (MSB)				0x01
0x014D		Reserved			Fine Analog Delay[4:0]					0x00
0x014E		Reserved			Coarse Digital Delay[4:0]					0x00
0x014F		12-Bit Multislip Digital Delay[7:0] (LSB)								0x00
0x0150		Reserved				12-Bit Multislip Digital Delay[11:8] (MSB)				0x00
0x0151		Reserved						Output Mux Selection[1:0]		0x00
0x0152		Idle at Zero[1:0]		Dynamic driver enable	Driver Mode[1:0]		Reserved	Driver Impedance[1:0]		0x30

CONTROL REGISTER MAP BIT DESCRIPTIONS

Global Control (Register 0x0000 to Register 0x0009)

Table 22. Global Soft Reset Control

Address	Bits	Bit Name	Settings	Description	Access
0x0000	[7:1]	Reserved		Reserved	RW
	0	Soft reset		Resets all registers, dividers, and FSMs to default values	

Table 23. Global Request and Mode Control

Address	Bits	Bit Name	Settings	Description	Access
0x0001	7	Reseed request		Requests the centralized resync timer and FSM to reseed any of the output dividers that are programmed to pay attention to sync events. This signal is rising edge sensitive, and is only acknowledged if the resync FSM has completed all events (has finished any previous pulse generator and/or sync events, and is in the done state (SYSREF FSM State[3:0] = 0010).	RW
	6	High performance distribution path	0 1	High performance distribution path select. The clock distribution path has two modes. Power priority. Noise priority. Provides the option for better noise floors on the divided output signals.	
	5	Reserved		Reserved.	
	4	Reserved		Reserved.	

CONTROL REGISTERS

Table 23. Global Request and Mode Control (Continued)

Address	Bits	Bit Name	Settings	Description	Access
	3	Mute output drivers		Mutes the output drivers (dividers still run in the background).	
	2	Pulse generator request		Asks for a pulse stream (see the Typical Programming Sequence section).	
	1	Restart dividers/FSMs		Resets all dividers and FSMs. Does not affect configuration registers.	
	0	Sleep mode		Forces shutdown. Output network, and I/O buffers are disabled.	
0x0002	[7:2]	Reserved		Reserved.	RW
	1	Multislip request		Requests a slip or multislip event from all divider channels that are sensitive to slip or multislip commands. The dividers are rising edge sensitive and take some time to process the request, after which the phase synchronization alarm is asserted.	
	0	Reserved		Reserved.	

Table 24. Global Enable Control

Address	Bits	Bit Name	Settings	Description	Access
0x0003	[7:6]	Reserved		Reserved	RW
	5	RF reseeder enable		Enable RF reseed for SYSREF	
	[4:3]	Reserved		Reserved	
	2	SYSREF timer enable		Enable internal SYSREF time reference	
	1	Reserved		Reserved	
	0	Reserved		Reserved	
0x0004	7	Reserved		Reserved	RW
	[6:0]	Seven Pairs of 14-Channel Outputs Enable[6:0]	[0]	Enable Channel 0 and 1	
			[1]	Enable Channel 2 and 3	
			[2]	Enable Channel 4 and 5	
			[3]	Enable Channel 6 and 7	
			[4]	Enable Channel 8 and 9	
			[5]	Enable Channel 10 and 11	
			[6]	Enable Channel 12 and 13	

Table 25. Global Mode and Enable Control

Address	Bits	Bit Name	Settings	Description	Access
0x0005	[7:0]	Reserved		Reserved	RW

Table 26. Global Clear Alarms

Address	Bits	Bit Name	Settings	Description	Access
0x0006	[7:1]	Reserved		Reserved	RW
	0	Clear alarms		Clear latched alarms	

Table 27. Global Miscellaneous Control

Address	Bits	Bit Name	Settings	Description	Access
0x0007	[7:0]	Reserved		Reserved.	RW
0x0008	[7:0]	Reserved (scratchpad)		Reserved. The user can write/read to this register to confirm input/outputs to the HMC7043. This register does not affect device operation.	RW
0x0009	[7:0]	Reserved		Reserved.	RW

Input Buffer (Register 0x000A to Register 0x000B)

Table 28. CLKIN/ $\overline{\text{CLKIN}}$ and RFSYNCIN/ $\overline{\text{RFSYNCIN}}$ Input Buffer Control

Address	Bits	Bit Name	Settings	Description	Access
0x000A, 0x000B	[7:5]	Reserved		Reserved	RW

CONTROL REGISTERS

Table 28. CLKIN/ $\overline{\text{CLKIN}}$ and RFSYNCIN/ $\overline{\text{RFSYNCIN}}$ Input Buffer Control (Continued)

Address	Bits	Bit Name	Settings	Description	Access
	[4:1]	Input Buffer Mode[3:0]		Input buffer control	
			[0]	Enable internal 100 Ω termination	
			[1]	Enable ac coupling input mode	
			[2]	Enable LVPECL input mode	
			[3]	High-Z input enable	
	0	Buffer enable		Enable input buffer	

GPIO/SDATA Control (Register 0x0046 to Register 0x0054)

Table 29. GPI Control

Address	Bits	Bit Name	Settings	Description	Access
0x0046	[7:4]	Reserved		Reserved	RW
	[3:1]	GPI Selection[2:0]		Select the GPI functionality, Bits[2:0]	
			0000	Select the GPI functionality, Bits[2:0]	
			0001	Reserved	
			0010	Put the chip into sleep mode	
			0011	Issue a mute	
			0100	Issue a pulse generator request	
			0101	Issue a reseed request	
			0110	Issue a restart request	
			0111	Reserved	
			1000	Issue a slip request	
			1001	Reserved	
			1010	Reserved	
			1011	Reserved	
			1100	Reserved	
			1101	Reserved.	
			1110	Reserved	
			1111	Reserved.	
	0	GPI enable		GPI function enable. Before changing the function of the pin, disable it first, and then reenable it after the function change.[1]	

[1] Note that it is possible to have a GPIO delete pin configured as both an output and an input.

Table 30. GPO Control

Address	Bits	Bit Name	Settings	Description	Access
0x0050	7	Reserved		Reserved	RW
	[6:2]	GPO Selection[4:0]		Select the GPO functionality, Bits[4:0]	
			00000	Alarm signal	
			00001	SDATA from SPI communication	
			00010	SYSREF sync status has not synchronized since reset	
			00011	Clock outputs phase status	
			00100	Sync request status signal	
			00101	Channel outputs FSM busy	
			00110	SYSREF FSM State 0	
			00111	SYSREF FSM State 1	
			01000	SYSREF FSM State 2	
			01001	SYSREF FSM State 3	
			01010	Force Logic 1 to GPO	

CONTROL REGISTERS

Table 30. GPO Control (Continued)

Address	Bits	Bit Name	Settings	Description	Access
			01011	Force Logic 0 to GPO	
			01100	Reserved	
			01101	Reserved	
			01110	Reserved	
			01111	Reserved	
			10000	Reserved	
			10001	Reserved	
			10010	Reserved	
			10011	Reserved	
			10100	Reserved	
			10101	Reserved	
			10110	Reserved	
			10111	Reserved	
			11000	Reserved	
			11001	Pulse generator request status signal	
			11010	Reserved	
			11011	Reserved	
			11100	Reserved	
			11101	Reserved	
			11110	Reserved	
			11111	Reserved	
	1	GPO mode		Selects the mode of GPO driver	
			0	Open-drain mode	
			1	CMOS mode	
	0	GPO enable		GPO driver enable	

Table 31. SDATA Control

Address	Bits	Bit Name	Settings	Description	Access
0x0054	[7:2]	Reserved		Reserved	RW
	1	SDATA mode		Selects the mode of SDATA driver	
			0	Open-drain mode	
			1	CMOS mode	
	0	SDATA enable		SDATA driver enable	

SYSREF/SYNC (Register 0x005A to Register 0x005D)

Table 32. Pulse Generator Control

Address	Bits	Bit Name	Settings	Description	Access
0x005A	[7:3]	Reserved		Reserved.	RW
	[2:0]	Pulse Generator Mode Selection[2:0]		SYSREF output enable with pulse generator.	
			000	Level sensitive. When the GPI is configured to issue a pulse generator request (GPI Selection[2:0] = 100), or a pulse generator request is issued through the SPI or as a SYNC pin-based pulse generator, run the pulse generator. Otherwise, stop the pulse generator.	
			001	1 pulse.[1]	
			010	2 pulses.[1]	
			011	4 pulses.[1]	
			100	8 pulses.[1]	
			101	16 pulses.[1]	
			110	16 pulses.[1]	

CONTROL REGISTERS

Table 32. Pulse Generator Control (Continued)

Address	Bits	Bit Name	Settings	Description	Access
			111	Continuous mode (50% duty cycle).[2]	

[1] Only LVPECL and CML buffer modes support N-Pulse SYSREF operation. When using N-Pulse SYSREF generation, refer to the Clock Output Network section.

[2] For continuous SYSREF generation, using an asynchronous start-up mode results in lower power consumption than compared to dynamic start-up mode with a continuous SYSREF mode.

Table 33. SYNC Control

Address	Bits	Bit Name	Settings	Description	Access
0x005B	[7:3]	Reserved		Reserved	RW
	2	SYNC retime			
			0	Bypass the retime (non-deterministic SYNC event condition)	
			1	Retime the external SYNC (deterministic SYNC event condition)	
	1	Reserved		Reserved	
	0	SYNC polarity		SYNC polarity (must be 0 if not using CLKIN/ $\overline{\text{CLKIN}}$ as the input)	
			0	Positive	
			1	Negative	

Table 34. SYSREF Timer Control

Address	Bits	Bit Name	Settings	Description	Access
0x005C	[7:0]	SYSREF Timer[7:0] (LSB)		12-bit SYSREF timer setpoint LSB. This sets the internal beat frequency of the main SYSREF timer, which controls synchronization and pulse generator events. Set the 12-bit timer to a submultiple of the lowest output SYSREF frequency, and program it to be no faster than 4 MHz.	RW
0x005D	[7:4]	Reserved		Reserved.	RW
	[3:0]	SYSREF Timer[11:8] (MSB)		12-bit SYSREF timer setpoint MSB.	

Clock Distribution Network (Register 0x0064 to Register 0x0065)

Table 35. Clock Input Control

Address	Bits	Bit Name	Settings	Description	Access
0x0064	[7:2]	Reserved		Reserved	RW
	1	Divide by 2 on clock input		Use divide by 2 on clock input path	
	0	Low frequency clock input		Changes bias to Class A for low frequency clock input	

Table 36. Analog Delay Common Control

Address	Bits	Bit Name	Settings	Description	Access
0x0065	[7:1]	Reserved		Reserved.	RW
	0	Analog delay low power mode		Analog delay is low power mode. Can save power for low settings of analog delay, but is not glitchless between setpoints.	

Alarm Masks Register (Register 0x0071)

Table 37. Alarm Mask Control Register

Address	Bits	Bit Name	Settings	Description	Access
0x0071	[7:5]	Reserved		Reserved	RW
	4	Sync request mask		If set, allow sync request signals to generate an alarm signal	
	3	Reserved		Reserved	
	2	Clock outputs phase status mask		If set, allow clock output phases status signal to generate an alarm signal	

CONTROL REGISTERS

Table 37. Alarm Mask Control Register (Continued)

Address	Bits	Bit Name	Settings	Description	Access
	1	SYSREF sync status mask		If set, allow SYSREF sync status signal to generate an alarm signal	
	0	Reserved		Reserved	

Product ID Registers (Register 0x0078 to 0x007A)

Table 38. Product ID Registers

Address	Bits	Bit Name	Settings	Description	Access
0x0078	[7:0]	Product ID Value[7:0] (LSB)		24-bit product ID value low	R
0x0079	[7:0]	Product ID Value[15:8] (Mid)		24-bit product ID value mid	R
0x007A	[7:0]	Product ID Value[23:16] (MSB)		24-bit product ID value high	R

Alarm Readback Status Registers (Register 0x007B to 0x007F)

Table 39. Alarm Readback Status Registers

Address	Bits	Bit Name	Settings	Description	Access
0x007B	[7:1]	Reserved		Reserved.	R
	0	Alarm signal		Readback alarm status from SPI.	
0x007D	[7:5]	Reserved		Reserved.	R
	4	Sync request status		Unsynchronized.	
	3	Reserved		Reserved.	
	2	Clock outputs phases status		SYSREF alarm.	
			0	SYSREF of the HMC7043 is not valid; that is, the phase output is not stable.	
			1	SYSREF of the HMC7043 is valid; that is, the phase output is stable.	
	1	SYSREF sync status		SYSREF SYNC status alarm.	
			0	The HMC7043 has been synchronized with an external sync pulse or a sync request from the SPI.	
			1	The HMC7043 never synchronized with an external sync pulse or a sync request from the SPI.	
	0	Reserved	1	Reserved.	
0x007F	[7:0]	Reserved		Reserved.	R

SYSREF Status Register (Register 0x0091)

Table 40. SYSREF Status

Address	Bits	Bit Name	Settings	Description	Access
0x0091	[7:5]	Reserved		Reserved.	R
	4	Channel outputs FSM busy		One of clock outputs FSM requested clock, and it is running.	
	[3:0]	SYSREF FSM State[3:0]		Indicates the current step of the SYSREF reseed process. Note that the three different progressions are caused by different trigger events (reseed, pulse generator, reserved).	
			0000	Reset.	
			0010	Done.	
			0100	Get ready.	
			0101	Get ready.	
			0110	Get ready.	
			1010	Running (pulse generator).	
			1011	Start.	
			1100	Power up.	

CONTROL REGISTERS

Table 40. SYSREF Status (Continued)

Address	Bits	Bit Name	Settings	Description	Access
			1101	Power up.	
			1110	Power up.	
			1111	Clear reset.	

Bias Settings (Register 0x0096 to Register 0x00B8)

For optimum performance of the chip, Register 0x0098 to Register 0x00B8 must be programmed to a different value than their default value.

Table 41. Reserved Registers

Address	Bits	Bit Name	Settings	Description	Access
0x0098	[7:0]	Reserved		Reserved	RW
0x0099	[7:0]	Reserved		Reserved	RW
0x009D	[7:0]	Reserved		Reserved	RW
0x009E	[7:0]	Reserved		Reserved	RW
0x009F	[7:0]	Reserved		Clock output driver low power setting (set to 0x4D instead of default value)	RW
0x00A0	[7:0]	Reserved		Clock output driver high power setting (set to 0xDF instead of default value)	RW
0x00A2	[7:0]	Reserved		Reserved	RW
0x00A3	[7:0]	Reserved		Reserved	RW
0x00A4	[7:0]	Reserved		Reserved	RW
0x00AD	[7:0]	Reserved		Reserved	RW
0x00B5	[7:0]	Reserved		Reserved	RW
0x00B6	[7:0]	Reserved		Reserved	RW
0x00B7	[7:0]	Reserved		Reserved	RW
0x00B8	[7:0]	Reserved		Reserved	RW

Clock Distribution (Register 0x00C8 to Register 0x0152)

The bit descriptions in Table 42 apply to all 14 channels.

Table 42. Channel 0 to Channel 13 Control

Address	Bits	Bit Name	Settings[1]	Description	Access
0x00C8, 0x00D2, 0x00DC, 0x00E6, 0x00F0, 0x00FA, 0x0104, 0x010E, 0x0118, 0x0122, 0x012C, 0x0136, 0x0140, 0x014A	7	High performance mode		High performance mode. Adjusts the divider and buffer bias to improve swing/phase noise at the expense of power.	RW
	6	SYNC enable		Susceptible to SYNC event. The channel can process a SYNC event to reset the phase.	
	5	Slip enable		Susceptible to slip event. The channel can process a slip request from SPI or GPI. Note that if slip enable is true, but multislip is off, a channel slips by 1 clock input cycle on an explicit slip request broadcast from the SPI/GPI.	
	4	Reserved		Reserved.	
	[3:2]	Start-Up Mode[1:0]		Configures the channel to normal mode with asynchronous startup, or to a pulse generator mode with dynamic start-up. Note that this must be set to asynchronous mode if the channel is unused.	
			00	Asynchronous.	
			01	Reserved.	
			10	Reserved.	
			11	Dynamic.	
	1	Multislip enable		Allow multislip operation (default = 0 for SYSREF, 1 for DCLK).	
			0	Do not engage automatic multislip on channel startup.	

CONTROL REGISTERS

Table 42. Channel 0 to Channel 13 Control (Continued)

Address	Bits	Bit Name	Settings[1]	Description	Access
			1	Multislip events after SYNC or pulse generator request, if the slip enable bit = 1.	
	0	Channel enable		Channel enable. If this bit is 0, channel is disabled.	
0x00C9, 0x00D3, 0x00DD, 0x00E7, 0x00F1, 0x00FB, 0x0105, 0x010F, 0x0119, 0x0123, 0x012D, 0x0137, 0x0141, 0x014B	[7:0]	12-Bit Channel Divider[7:0] (LSB)		12-bit channel divider setpoint LSB. The divider supports even divide ratios from 2 to 4094. The supported odd divide ratios are 1, 3, and 5. All even and odd divide ratios have 50.0% duty cycle.	RW
0x00CA, 0x00D4, 0x00DE, 0x00E8, 0x00F2, 0x00FC, 0x0106, 0x0110, 0x011A, 0x0124, 0x012E, 0x0138, 0x0142, 0x014C	[7:4]	Reserved		Reserved.	RW
	[3:0]	12-Bit Channel Divider[11:8] (MSB)		12-bit channel divider setpoint MSB.	
0x00CB, 0x00D5, 0x00DF, 0x00E9, 0x00F3, 0x00FD, 0x0107, 0x0111, 0x011B, 0x0125, 0x012F, 0x0139, 0x0143, 0x014D	[7:5]	Reserved		Reserved.	RW
	[4:0]	Fine Analog Delay[4:0]		24 fine delay steps. Step size = 25 ps. Values bigger than 23 has no effect on analog delay.	
0x00CC, 0x00D6, 0x00E0, 0x00EA, 0x00F4, 0x00FE, 0x0108, 0x0112, 0x011C, 0x0126, 0x0130, 0x013A, 0x0144, 0x014E	[7:5]	Reserved		Reserved.	RW
	[4:0]	Coarse Digital Delay[4:0]		17 coarse delay steps. Step size = ½ input clock cycle. This flip flop (FF)-based digital delay does not increase noise level at the expense of power. Values bigger than 17 have no effect on coarse delay.	
0x00CD, 0x00D7, 0x00E1, 0x00EB, 0x00F5, 0x00FF, 0x0109, 0x0113, 0x011D, 0x0127, 0x0131, 0x013B, 0x0145, 0x014F	[7:0]	12-Bit Multislip Digital Delay[7:0] (LSB)		12-bit multislip digital delay amount LSB. Step size = (delay amount: MSB + LSB) × input clock cycles. If multislip enable bit = 1, any slip events (caused by GPI, SPI, SYNC, or pulse generator events) repeat the number of times set by 12-Bit Multislip Digital Delay[11:0] to adjust the phase by step size.	RW
0x00CE, 0x00D8, 0x00E2, 0x00EC, 0x00F6, 0x0100, 0x010A, 0x0114, 0x011E, 0x0128, 0x0132, 0x013C, 0x0146, 0x0150	[7:4]	Reserved		Reserved.	RW
	[3:0]	12-Bit Multislip Digital Delay[11:8] (MSB)		12-bit multislip digital delay amount MSB.	
0x00CF, 0x00D9, 0x00E3, 0x00ED, 0x00F7, 0x0101, 0x010B, 0x0115, 0x011F, 0x0129, 0x0133, 0x013D, 0x0147, 0x0151	[7:2]	Reserved		Reserved.	RW
	[1:0]	Output Mux Selection[1:0]		Channel output mux selection.	
			00	Channel divider output.	
			01	Analog delay output.	
			10	Other channel of the clock group pair.	
			11	Input clock (fundamental). Fundamental can also be generated with 12-bit channel divider ratio = 1.	
0x00D0, 0x00DA, 0x00E4, 0x00EE, 0x00F8, 0x0102, 0x010C, 0x0116, 0x0120, 0x012A, 0x0134, 0x013E, 0x0148, 0x0152	[7:6]	Idle at Zero[1:0]		Idle at Logic 0 selection (pulse generator mode only). Force to Logic 0 or VCM.	RW
			00	Normal mode (selection for DCLK).	
			01	Reserved.	
			10	Force to Logic 0.	
			11	Force outputs to float, goes naturally to VCM.	
	5	Dynamic driver enable		Dynamic driver enable (pulse generator mode only).	
			0	Driver is enabled/disabled with channel enable bit.	
			1	Driver is dynamically disabled with pulse generator events.	
	[4:3]	Driver Mode[1:0]		Output driver mode selection.	
			00	CML mode.	
			01	LVPECL mode.	
			10	LVDS mode.	
			11	CMOS mode.	
	2	Reserved		Reserved.	

CONTROL REGISTERS

Table 42. Channel 0 to Channel 13 Control (Continued)

Address	Bits	Bit Name	Settings[1]	Description	Access
	[1:0]	Driver Impedance[1:0]		Output driver impedance selection for CML mode. Output enable selection for CMOS mode.	
			00	CML: internal resistor disable. CMOS: disable both output.	
			01	CML: internal 100 Ω resistor enable per output pin. CMOS: enable OUT_P[2]	
			10	CML: reserved. CMOS: enable OUT_N[3]	
			11	CML: internal 50 Ω resistor enable per output pin. CMOS: enable both output	

[1] X means don't care.

[2] For Channel 0, Channel 3, Channel 5, Channel 6, Channel 9, Channel 10, and Channel 13, setting b'01 enables the OUT_N.

[3] For Channel 0, Channel 3, Channel 5, Channel 6, Channel 9, Channel 10, and Channel 13, setting b'10 enables the OUT_P.

APPLICATIONS INFORMATION

EVALUATION PCB AND SCHEMATIC

For the circuit board in this application, use RF circuit design techniques. Ensure that signal lines have 50 Ω impedance. Connect the package ground leads and exposed paddle directly to the ground plane similar to that shown in Figure 35 and Figure 36. Use a sufficient number of via holes to connect the top and bottom ground planes. The evaluation circuit board is available from Analog Devices, Inc., upon request.

The typical Pb-free reflow solder profile shown in Figure 34 is based on JEDEC J-STD-20C.

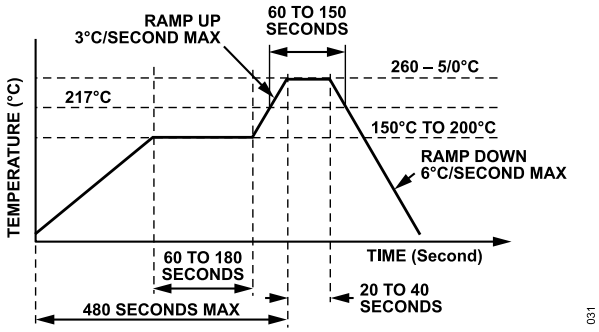

Figure 34. Pb-Free Reflow Solder Profile

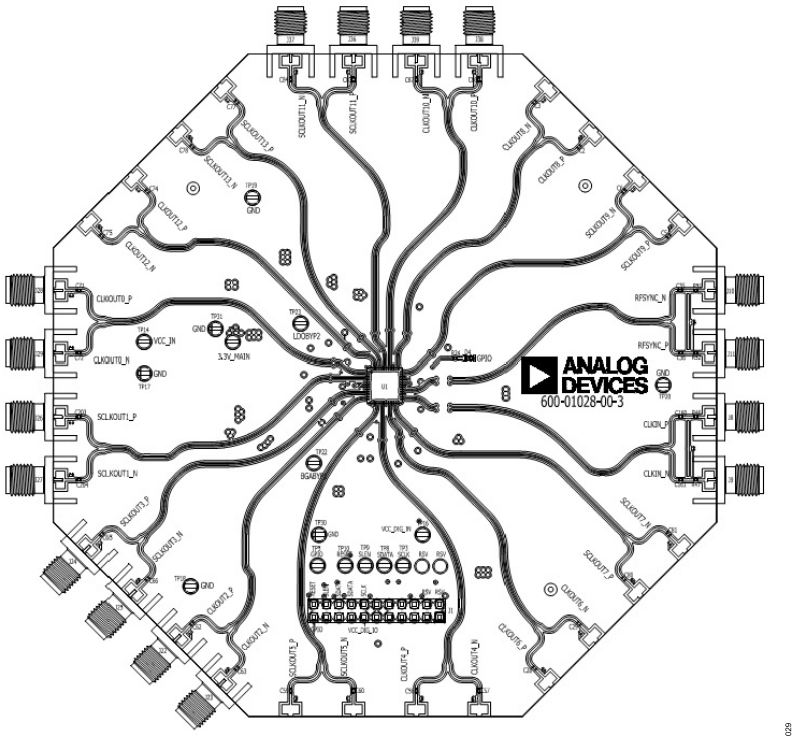

Figure 35. Evaluation PCB Layout, Top Side

APPLICATIONS INFORMATION

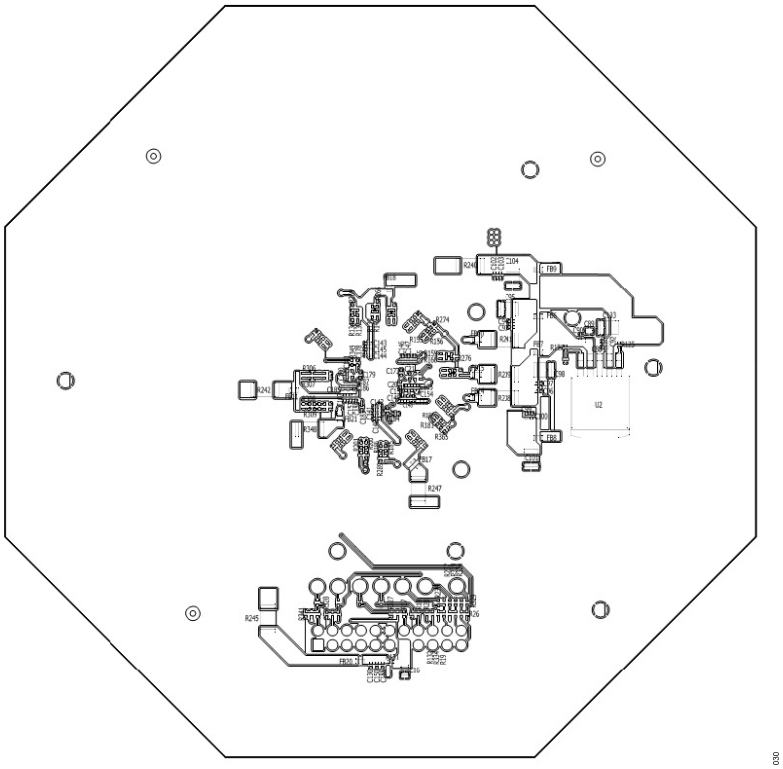

Figure 36. Evaluation PCB Layout, Bottom Side

OUTLINE DIMENSIONS

Package Drawing (Option)	Package Type	Package Description
HCP-48-1	LFCSP	48-Lead Lead Frame Chip Scale Package

For the latest package outline information and land patterns (footprints), go to Package Index.

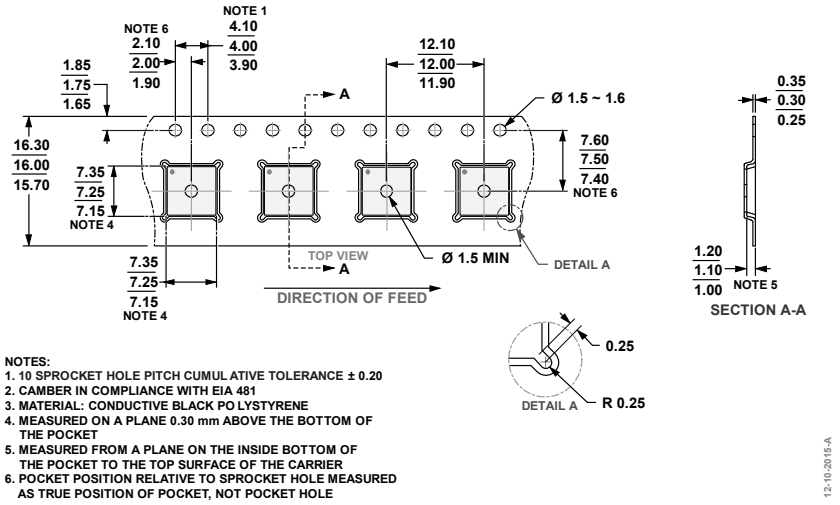

Figure 37. LFCSP Tape and Reel Outline Dimensions
Dimensions shown in millimeters

ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Packing Quantity	Package Option	Marking Code[2]
HMC7043LP7FE	−40°C to +85°C	48-Lead Lead Frame Chip Scale Package [LFCSP]	Cut Tape, 500	HCP-48-1	7043 XXXX
HMC7043LP7FETR	−40°C to +85°C	48-Lead Lead Frame Chip Scale Package [LFCSP]	Reel, 500	HCP-48-1	7043 XXXX

1 E = RoHS Compliant Part.

2 Four-digit lot number represented by XXXX.

LEAD FINISH AND MSL RATING OPTIONS

Model[1]	Lead Finish	MSL Rating[2]
HMC7043LP7FE	NiPdAu	MSL-3
HMC7043LP7FETR	NiPdAu	MSL-3

1 E = RoHS Compliant Part.

2 The maximum peak reflow temperature is 260°C for the HMC7043LP7FE.

EVALUATION BOARDS

Model[1]	Description
EK1HMC7043LP7F	Evaluation Kit

1 E = RoHS Compliant Part.