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REVISION HISTORY

<b>4/2025—Rev. A to Rev. B</b>	
Changed Master to Main and Slave to Subordinate (Throughout).....	1
Updated Outline Dimensions.....	9
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## SPECIFICATIONS

## ELECTRICAL SPECIFICATIONS

Table 1.

Parameter	Test Conditions/Comments	Temp	Test Level <sup>1</sup>	Min	Typ	Max	Unit
<b>DIGITAL INPUTS</b>							
Data Inputs—Video and Audio, CEC_CLK							
Input Voltage, High ( $V_{IH}$ )		Full	VI	1.35		3.5	V
Input Voltage, Low ( $V_{IL}$ )		Full	VI	−0.3		+0.7	V
Input Capacitance		25°C	VIII		1.0	1.5	pF
DDC I <sup>2</sup> C Lines (DDCSDA, DDCSCL)							
Input Voltage, High ( $V_{IH}$ )		Full	VI	1.4		5.5	V
Input Voltage, Low ( $V_{IL}$ )		Full	VI	−0.3		+0.7	V
I <sup>2</sup> C Lines (SDA, SCL)							
Input Voltage, High ( $V_{IH}$ )		Full	?	1.4		5.5	V
Input Voltage, Low ( $V_{IL}$ )		Full	?	−0.3		+0.7	V
CEC							
Input Voltage, High ( $V_{IH}$ )		Full	VI	2.0		5.5	V
Input Voltage, Low ( $V_{IL}$ )		Full	VI	−0.3		+0.8	V
Output Voltage, High ( $V_{OH}$ )		Full	VI	2.5		3.63	V
Output Voltage, Low ( $V_{OL}$ )		Full	VI	−0.3		+0.6	V
HPD							
Input Voltage, High ( $V_{IH}$ )		Full	VI	1.3		5.5	V
Input Voltage, Low ( $V_{IL}$ )		Full	VI	−0.3		+0.8	V
<b>THERMAL CHARACTERISTICS</b>							
Thermal Resistance							
$\theta_{JC}$ Junction-to-Case		Full	V		20		°C/W
$\theta_{JA}$ Junction-to-Ambient		Full	V		43		°C/W
Ambient Temperature		Full	V	−40	+25	+105	°C
<b>DC SPECIFICATIONS</b>							
Input Leakage Current ( $I_{IL}$ )		25°C	VI	−1		+1	μA
<b>POWER SUPPLY</b>							
1.8 V Supply Voltage (DVDD, AVDD, PVDD, BGVDD)		Full	IV	1.71	1.8	1.90	V
3.3 V Supply Voltage (DVDD_3V)		Full		3.15	3.3	3.45	V
Power-Down Current		25°C				100	μA
Transmitter Total Power (1.8 V Power = 200 mW and 3.3 V Power = 1 mW)	1080 p, 24 bit, typical random pattern	Full	VI		201		mW
<b>AC SPECIFICATIONS</b>							
TMDS Output Clock Frequency		25°C	IV	20		165	MHz
TMDS Output Clock Duty Cycle		25°C	IV	48		52	%
Input Video Clock Frequency		Full				165	MHz
Input Video Data Setup Time ( $t_{VSU}$ ) <sup>2</sup>		Full	IV	1.8			ns
Input Video Data Hold Time ( $t_{VHLD}$ ) <sup>2</sup>		Full	IV	1.3			ns
TMDS Differential Swing		25°C	VII	900	1100	1200	mV
Differential Output Timing							
Low-to-High Transition Time		25°C	VII	75	95		ps
High-to-Low Transition Time		25°C	VII	75	95		ps
VSYNC and HSYNC Delay							
From DE Falling Edge		25°C	IV		1		UI <sup>3</sup>
To DE Rising Edge		25°C	IV		1		UI <sup>3</sup>

## SPECIFICATIONS

Table 1. (Continued)

Parameter	Test Conditions/Comments	Temp	Test Level <sup>1</sup>	Min	Typ	Max	Unit
AUDIO AC TIMING							
SCLK Duty Cycle							
When N/2 Is an Even Number		Full	IV	40	50	60	%
When N/2 Is an Odd Number		Full	IV	49	50	51	%
I <sup>2</sup> S[3:0], SPDIF Setup Time (t <sub>ASU</sub> )		Full	IV	2			ns
I <sup>2</sup> S[3:0], SPDIF Hold Time (t <sub>AHLD</sub> )		Full	IV	2			ns
LRCLK Setup Time (t <sub>ASU</sub> )		Full	IV	2			ns
LRCLK Hold Time (t <sub>AHLD</sub> )		Full	IV	2			ns
CEC							
CEC_CLK Frequency		Full	VIII	3	12 <sup>4</sup>	100	MHz
CEC_CLK Accuracy		Full	VIII	-2		+2	%
I <sup>2</sup> C INTERFACE							
SCL Clock Frequency		Full				400	kHz
SDA Setup Time (t <sub>DSU</sub> )		Full		100			ns
SDA Hold Time (t <sub>DHO</sub> )		Full		100			ns
Setup for Start (t <sub>STASU</sub> )		Full		0.6			μs
Hold Time for Start (t <sub>STAH</sub> )		Full		0.6			μs
Setup for Stop (t <sub>STOSU</sub> )		Full		0.6			μs

<sup>1</sup> See the [Explanation of Test Levels](#) section.<sup>2</sup> This is measured at 0.9 V. The relationship between clock and data is programmable in 400 ps steps.<sup>3</sup> UI is the unit interval.<sup>4</sup> 12 MHz crystal oscillator for default register settings.

## ABSOLUTE MAXIMUM RATINGS

Table 2.

Parameter	Rating
Digital Inputs (SDA, SCL, DDCSDA, DDCSCL, HPD, PD, CEC)	-0.3 V to +5.5 V
Audio/Video Digital Inputs (MCLK, SPDIF, I2S[3:0], SCLK, HSYNC, DE, VSYNC, CEC_CLK)	-0.3 V to +3.63 V
Digital Output Current	20 mA
Operating Temperature Range	-40°C to +105°C
Storage Temperature Range	-65°C to +150°C
Maximum Junction Temperature	150°C
Maximum Case Temperature	150°C

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

## EXPLANATION OF TEST LEVELS

Table 3.

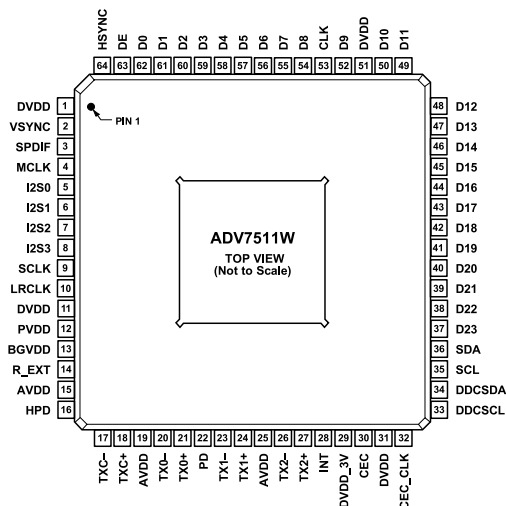
Test Level	Description
I.	100% production tested.
II.	100% production tested at 25°C and sample tested at specified temperatures.
III.	Sample tested only.
IV.	Parameter is guaranteed by design and characterization testing.
V.	Parameter is a typical value only.
VI.	100% production tested at 25°C; guaranteed by design and characterization testing.
VII.	Limits defined by HDMI specification; guaranteed by design and characterization testing.
VIII.	Parameter is guaranteed by design.

## ESD CAUTION



**ESD (electrostatic discharge) sensitive device.** Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

## PIN CONFIGURATION AND FUNCTION DESCRIPTIONS



NOTES  
1. THE LQFP HAS AN EXPOSED PAD THAT SHOULD BE CONNECTED TO GROUND.

002

Figure 2. Pin Configuration

Table 4. Pin Function Descriptions

Pin No.	Mnemonic	Type	Description
1, 11, 31, 51	DVDD	Power	1.8 V Power Supply. These pins should be filtered and as quiet as possible.
2	VSYNC	Input	Vertical Sync Input.
3	SPDIF	Input	SPDIF (Sony/Philips Digital Interface) Audio Input.
4	MCLK	Input	Audio Reference Clock Input.
5	I2S0	Input	I <sup>2</sup> S Channel 0 Audio Data Input.
6	I2S1	Input	I <sup>2</sup> S Channel 1 Audio Data Input.
7	I2S2	Input	I <sup>2</sup> S Channel 2 Audio Data Input.
8	I2S3	Input	I <sup>2</sup> S Channel 3 Audio Data Input.
9	SCLK	Input	I <sup>2</sup> S Audio Clock Input.
10	LRCLK	Input	Left/Right Channel Signal Input.
12	PVDD	Power	1.8 V PLL Power Supply.
13	BGVDD	Power	Band Gap Power Supply.
14	R_EXT	Input	This pin sets the internal reference currents.
15, 19, 25	AVDD	Power	1.8 V Power Supply for TMDS Outputs.
16	HPD	Input	Hot Plug™ Detect Signal Input.
17, 18	TXC-, TXC+	Differential output	Differential TMDS Clock Output.
20, 21	TX0-, TX0+	Differential output	Differential TMDS Output Channel 0.
22	PD	Input	Power-Down Control and I <sup>2</sup> C Address Selection.
23, 24	TX1-, TX1+	Differential output	Differential TMDS Output Channel 1.
26, 27	TX2-, TX2+	Differential output	Differential TMDS Output Channel 2.
28	INT	Output	Interrupt Signal Output.
29	DVDD_3V	Power	3.3 V Power Supply.
30	CEC	Input/output	CEC Data Signal.
32	CEC_CLK	Input	CEC clock is an oscillator from 3 MHz to 100 MHz.
33	DDCSCL	Control	Serial Port Data Clock to Sink.
34	DDCSDA	Control	Serial Port Data I/O to Sink.
35	SCL	Control	Serial Port Data Clock Input.
36	SDA	Control	Serial Port Data I/O.
37 to 50, 52, 54 to 62	D[23:0]	Input	Video Data Input
53	CLK	Input	Video Input Clock.

**PIN CONFIGURATION AND FUNCTION DESCRIPTIONS****Table 4. Pin Function Descriptions (Continued)**

Pin No.	Mnemonic	Type	Description
63	DE	Input	Data Enable Signal Input for Digital Video.
64	HSYNC	Input	Horizontal Sync Input.
	EPAD	Power	The LQFP has an exposed pad that should be connected to ground.

## APPLICATIONS INFORMATION

### DESIGN RESOURCES

Evaluation kits, reference design schematics, hardware and software guides, and other support documentation are available from Analog Devices, Inc., [Engineer Zone](#).

Other references include the following:

- ▶ *EIA/CEA-861D*, a technical specifications document, describes audio and video InfoFrames, as well as the E-EDID structure for HDMI. It is available from the Consumer Electronics Association (CEA).
- ▶ *High-Definition Multimedia Interface Specification Version 1.4a*, a defining document for HDMI v.1.4a, and the *High-Definition Multimedia Interface Compliance Test Specification Version 1.4a* are available from HDMI Licensing, LLC.
- ▶ *High-Bandwidth Digital Content Protection System Revision 1.3*, the defining technical specifications document for the HDCP v.1.3, is available from Digital Content Protection, LLC.



## OUTLINE DIMENSIONS

Package Drawing (Option)	Package Type	Package Description
SW-64-3	LQFP_EP	64-Lead Low Profile Quad Flat Package, with Exposed Pad

For the latest package outline information and land patterns (footprints), go to [Package Index](#).

## ORDERING GUIDE

Model <sup>1,2</sup>	Temperature Range	Package Description	Package Option
ADV7511WBSWZ	−40°C to +105°C	64-Lead Low Profile Quad Flat Package with Exposed Pad [LQFP_EP]	SW-64-3
ADV7511WBSWZ-RL	−40°C to +105°C	64-Lead Low Profile Quad Flat Package with Exposed Pad [LQFP_EP], Tape and Reel	SW-64-3

<sup>1</sup> Z = RoHS Compliant Part.

<sup>2</sup> W = Qualified for Automotive Applications.

## EVALUATION BOARDS

Model <sup>1,2</sup>	Description
EVAL-ADV7511W-AKZ	Evaluation Kit

<sup>1</sup> Z = RoHS Compliant Part.

<sup>2</sup> W = Qualified for Automotive Applications.

## AUTOMOTIVE PRODUCTS

The ADV7511W models are available with controlled manufacturing to support the quality and reliability requirements of automotive applications. Note that these automotive models may have specifications that differ from the commercial models; therefore, designers should review the [Specifications](#) section of this data sheet carefully. Only the automotive grade products shown are available for use in automotive applications. Contact your local Analog Devices account representative for specific product ordering information and to obtain the specific Automotive Reliability reports for these models.

I<sup>2</sup>C refers to a communications protocol originally developed by Philips Semiconductors (now NXP Semiconductors).

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