Data Sheet

ADuM6221A

Dual-Channel Isolator with Integrated DC-to-DC Converter

FEATURES

- *iso*Power integrated, isolated DC-to-DC converter
- 100 mA output supply
- Meets CISPR 32/EN55032 Class B emission limits up to 5 Mbps at full load on a 2-layer PCB
- Dual DC to 100 Mbps signal isolation channels
- 28-lead, fine pitch, SOIC with 8.3 mm minimum creepage
- High temperature operation: 125°C maximum
- High common-mode transient immunity: 100 kV/µs
- Safety and regulatory approvals
  - UL 1577
    - V_{ISO} = 5000 V rms for 1 minute
  - IEC/EN/CSA 62368-1
  - IEC/CSA 60601-1
  - IEC/CSA 61010-1
  - CQC GB 4943.1
  - DIN EN IEC 60747-17 (VDE 0884-17) (pending)
    - V_{IORM} = 596 V peak

APPLICATIONS

- RS-232 transceivers
- Power supply start-up bias and gate drives
- Isolated sensor interfaces
- Automotive on-board charger (OBC) and DC-to-DC
- Industrial programmable logic controllers (PLCs)

GENERAL DESCRIPTION

The ADuM6221A is a dual-channel digital isolators with an *iso*Power®, integrated, isolated DC-to-DC converter. Based on the Analog Devices, Inc., *i*Coupler® technology, the DC-to-DC converter provides regulated, isolated power that meets CISPR 32/EN 55032 Class B limits at full load on a 2-layer printed circuit board (PCB) with ferrites. Popular voltage combinations and the associated output current levels are listed in Table 1.

The ADuM6221A eliminates the need for a separate, isolated DC-to-DC converter in 500 mW, isolated designs. The *i*Coupler chip scale transformer technology is used for isolated logic signals and for the magnetic components of the DC-to-DC converter. The result is a small form factor and total isolation solution.

The ADuM6221A isolators provide two independent isolation channels (for more details, see the Pin Configurations and Function Descriptions section).

Table 1. ADuM6221A Output Current Levels

		ISO Current, I_{ISO} (mA)		
V_{DDP} (V)[1]	V_{ISO} (V)	85°C	105°C	125°C
5	5	100	65	30
5	3.3	100	65	30
3.3	3.3	60	60	20

[1] The ADUM6221ABRNZ3 is to be used in the 3.3 V to 3.3. V configuration. The ADuM6221ABRNZ5 is to be used in the 5 V to 3.3 V and 5 V to 5 V configurations.

FUNCTIONAL BLOCK DIAGRAM

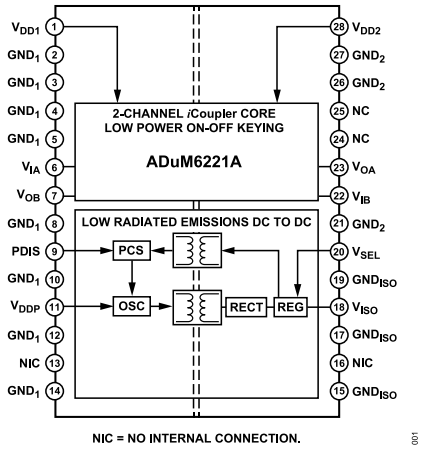

Figure 1. Functional Block Diagram

Rev. B

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3/2024—Revision 0: Initial Version

SPECIFICATIONS

ELECTRICAL CHARACTERISTICS—5 V PRIMARY INPUT SUPPLY/5 V SECONDARY ISOLATED SUPPLY

All typical specifications are at T_A = 25°C, V_{DDP} = V_{ISO} = 5 V. Minimum and maximum specifications apply over the entire recommended operation range, which is 4.5 V ≤ V_{DDP}, V_{ISO} ≤ 5.5 V and −40°C ≤ T_A ≤ +125°C, unless otherwise noted.

Table 2. DC-to-DC Converters Static Specifications

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
DC-TO-DC CONVERTERS SUPPLY						
Set Point	V_{ISO}	4.75	5.0	5.25	V	ISO current (I_{ISO}) = 10 mA
Line Regulation	$V_{ISO (LINE)}$		20		mV/V	I_{ISO} = 50 mA, V_{DDP} = 4.5 V to 5.5 V
Load Regulation	$V_{ISO (LOAD)}$		1	5	%	I_{ISO} = 10 mA to 90 mA
Output Ripple	$V_{ISO (RIP)}$		75		mV p-p	20 MHz bandwidth, bulk output capacitance (C_{BO}) = 0.1 µF||10 µF, I_{ISO} = 90 mA
Output Noise	$V_{ISO (NOISE)}$		200		mV p-p	C_{BO} = 0.1 µF||10 µF, I_{ISO} = 90 mA
Switching Frequency	f_{OSC}		180		MHz	
Pulse-Width Modulation (PWM) Frequency	f_{PWM}		625		kHz	
Output Supply[1]	$I_{ISO (MAX)}$	100			mA	4.5 V < V_{ISO} < 5.25 V
		50			mA	4.75 V < V_{ISO} < 5.25 V
Efficiency at $I_{ISO (MAX)}$[1]			33		%	I_{ISO} = 100 mA
V_{DD1} Supply Current						
No V_{ISO} Load	$I_{DDP (Q)}$		14	25	mA	
Full V_{ISO} Load	$I_{DDP (MAX)}$		310		mA	
Thermal Shutdown						
Shutdown Temperature			154		°C	
Thermal Hysteresis			10		°C	

[1] Maximum V_{ISO} output current is derated by 1.75 mA/°C for T_A > 85°C.

ELECTRICAL CHARACTERISTICS—5 V PRIMARY INPUT SUPPLY/3.3 V SECONDARY ISOLATED SUPPLY

All typical specifications are at T_A = 25°C, V_{DDP} = 5.0 V, V_{ISO} = 3.3 V. Minimum and maximum specifications apply over the entire recommended operation range, which is 4.5 V ≤ V_{DDP} ≤ 5.5 V, 3.0 V ≤ V_{ISO} ≤ 3.6 V, and −40°C ≤ T_A ≤ +125°C, unless otherwise noted.

Table 3. DC-to-DC Converters Static Specifications

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
DC-TO-DC CONVERTERS SUPPLY						
Set Point	V_{ISO}	3.135	3.3	3.465	V	I_{ISO} = 10 mA
Line Regulation	$V_{ISO (LINE)}$		20		mV/V	I_{ISO} = 50 mA, V_{DDP} = 3.0 V to 3.6 V
Load Regulation	$V_{ISO (LOAD)}$		1	5	%	I_{ISO} = 10 mA to 90 mA
Output Ripple	$V_{ISO (RIP)}$		50		mV p-p	20 MHz bandwidth, C_{BO} = 0.1 µF||10 µF, I_{ISO} = 90 mA
Output Noise	$V_{ISO (NOISE)}$		130		mV p-p	C_{BO} = 0.1 µF||10 µF, I_{ISO} = 90 mA
Switching Frequency	f_{OSC}		180		MHz	
PWM Frequency	f_{PWM}		625		kHz	
Output Supply[1]	$I_{ISO (MAX)}$	100			mA	3.0 V < V_{ISO} < 3.4 V
		50			mA	3.135 V < V_{ISO} < 3.465 V
Efficiency at $I_{ISO (MAX)}$[1]			27		%	I_{ISO} = 100 mA
V_{DDP} Supply Current						
No V_{ISO} Load	$I_{DDP (Q)}$		14	20	mA	
Full V_{ISO} Load	$I_{DDP (MAX)}$		250		mA	

SPECIFICATIONS

Table 3. DC-to-DC Converters Static Specifications (Continued)

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
Thermal Shutdown						
Shutdown Temperature			154		°C	
Thermal Hysteresis			10		°C	

[1] Maximum V_{ISO} output current is derated by 1.75 mA/°C for T_A > 85ºC.

ELECTRICAL CHARACTERISTICS—3.3 V PRIMARY INPUT SUPPLY/3.3 V SECONDARY ISOLATED SUPPLY

All typical specifications are at T_A = 25°C, V_{DDP} = V_{ISO} = 3.3 V. Minimum and maximum specifications apply over the entire recommended operation range, which is 3.0 V ≤ V_{DDP}, V_{ISO} ≤ 3.6 V, and −40°C ≤ T_A ≤ +125°C, unless otherwise noted.

Table 4. DC-to-DC Converters Static Specifications

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
DC-TO-DC CONVERTERS SUPPLY						
Set Point	V_{ISO}	3.135	3.3	3.465	V	I_{ISO} = 10 mA
Line Regulation	$V_{ISO (LINE)}$		20		mV/V	I_{ISO} = 30 mA, V_{DDP} = 3.0 V to 3.6 V
Load Regulation	$V_{ISO (LOAD)}$		1	5	%	I_{ISO} = 6 mA to 54 mA
Output Ripple	$V_{ISO (RIP)}$		50		mV p-p	20 MHz bandwidth, C_{BO} = 0.1 µF||10 µF, I_{ISO} = 60 mA
Output Noise	$V_{ISO (NOISE)}$		130		mV p-p	C_{BO} = 0.1 µF||10 µF, I_{ISO} = 60 mA
Switching Frequency	f_{OSC}		180		MHz	
PWM Frequency	f_{PWM}		625		kHz	
Output Supply[1]	$I_{ISO (MAX)}$	60			mA	3.0 V < V_{ISO} < 3.465 V
		30			mA	3.135 V < V_{ISO} < 3.465 V
Efficiency at $I_{ISO (MAX)}$[1]			34		%	I_{ISO} = 60 mA
V_{DDP} Supply Current						
No V_{ISO} Load	$I_{DDP (Q)}$		14	20	mA	
Full V_{ISO} Load	$I_{DDP (MAX)}$		190		mA	
Thermal Shutdown						
Shutdown Temperature			154		°C	
Thermal Hysteresis			10		°C	

[1] Maximum V_{ISO} output current is derated by 2.0 mA/°C for T_A > 85ºC.

ELECTRICAL CHARACTERISTICS—5.0 V OPERATION DIGITAL ISOLATOR CHANNELS ONLY

All typical specifications are at T_A = 25°C, V_{DD1} = V_{DD2} = 5.0 V. Minimum and maximum specifications apply over the entire recommended operation range: 4.5 V ≤ V_{DD1}, V_{DD2} ≤ 5.5 V and −40°C ≤ T_A ≤ +125°C, unless otherwise noted. Switching specifications are tested with C_L = 15 pF and CMOS signal levels, unless otherwise noted. Supply currents are specified with 50% duty cycle signals.

Table 5. Data Channel Supply Current Specifications

		1 Mbps			10 Mbps			100 Mbps				
Parameter	Symbol	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Unit	Test Conditions/Comments
SUPPLY CURRENT												C_L = 0 pF
ADuM6221ABRNZ5												
	I_{DD1}		4.2	8.4		4.5	8.5		8.0	12.0	mA	
	I_{DD2}		2.3	4.5		2.8	5.7		8.8	12.0	mA	
ADuM6221ABRNZ3												
	I_{DD1}		4.2	8.4		4.5	8.5		8.0	12.0	mA	
	I_{DD2}		2.3	4.5		2.8	5.7		9.4	15.0	mA	

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Table 6. Switching Specifications

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
SWITCHING SPECIFICATIONS						
Pulse Width	PW	10			ns	Within pulse-width distortion (PWD) limit
Data Rate				100	Mbps	Within PWD limit
Propagation Delay	t_{PHL}, t_{PLH}	7.0	10	15	ns	50% input to 50% output
Pulse-Width Distortion	PWD		1	5	ns	$\lvert t_{PLH} - t_{PHL} \rvert$
Change vs. Temperature			1.5		ps/°C	
Propagation Delay Skew	t_{PSK}			8.0	ns	Between any two units at the same temperature, voltage, and load
Channel Matching			1	5.0	ns	
Jitter			816		ps p-p	

Table 7. Input and Output Characteristics

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
DC SPECIFICATIONS						
Input Threshold						
Logic High	V_{IH}	0.7 × V_{DDx}			V	
Logic Low	V_{IL}			0.3 × V_{DDx}	V	
Output Voltage						
Logic High	V_{OH}	V_{DDx} − 0.2	V_{DDx}		V	I_{Ox}[1] = −20 µA, V_{Ix} = V_{IxH}[2]
		V_{DDx} − 0.5	V_{DDx} − 0.2		V	I_{Ox}[1] = −3.2 mA, V_{Ix} = V_{IxH}[2]
Logic Low	V_{OL}		0.0	0.1	V	I_{Ox}[1] = 20 µA, V_{Ix} = V_{IxL}[3]
			0.0	0.4	V	I_{Ox}[1] = 3.2 mA, V_{Ix} = V_{IxL}[3]
Undervoltage Lockout	UVLO					V_{DD1}, V_{DD2}, and V_{DDP} supply
Positive Going Threshold	V_{UV+}		1.6		V	
Negative Going Threshold	V_{UV-}		1.5		V	
Hysteresis	V_{UVH}		0.1		V	
Input Current per Channel	I_I	−10	+0.01	+10	µA	0 V ≤ V_{Ix} ≤ V_{DDx}
Quiescent Supply Current						
	$I_{DD1 (Q)}$		0.5	1.4	mA	V_{Ix} = Logic 0
	$I_{DD2 (Q)}$		0.9	1.5	mA	V_{Ix} = Logic 0
	$I_{DD1 (Q)}$		7.5	14	mA	V_{Ix} = Logic 1
	$I_{DD2 (Q)}$		3.3	6.2	mA	V_{Ix} = Logic 1
Dynamic Supply Current						
Input	$I_{DDI (D)}$		0.01		mA/Mbps	Inputs switching, 50% duty cycle
Output	$I_{DDO (D)}$		0.02		mA/Mbps	Inputs switching, 50% duty cycle
AC SPECIFICATIONS						
Output Rise Time/Fall Time	t_R/t_F		2.5		ns	10% to 90%
Common-Mode Transient Immunity[4]	$\lvert CM_H \rvert$	75	100		kV/µs	V_{Ix} = V_{DD1} or V_{ISO}, common-mode voltage V_{CM} = 1000 V
	$\lvert CM_L \rvert$	75	100		kV/µs	V_{Ix} = 0 V, V_{CM} = 1000 V

[1] I_{Ox} is the Channel x output current, where x means A or B.

[2] V_{IxH} is the input side logic high.

[3] V_{IxL} is the input side logic low.

[4] $\lvert CM_H \rvert$ is the maximum common-mode voltage slew rate that can be sustained while maintaining the voltage output V_O > 0.8 V_{DDx}. $\lvert CM_L \rvert$ is the maximum common-mode voltage slew rate that can be sustained while maintaining V_O < 0.8 V. The common-mode voltage slew rates apply to both the rising and falling common-mode voltage edges.

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ELECTRICAL CHARACTERISTICS—3.3 V OPERATION DIGITAL ISOLATOR CHANNELS ONLY

All typical specifications are at T_A = 25°C, V_{DD1} = V_{DD2} = 3.3 V. Minimum and maximum specifications apply over the entire recommended operation range: 3.0 V ≤ V_{DD1}, V_{DD2} ≤ 3.6 V, and −40°C ≤ T_A ≤ +125°C, unless otherwise noted. Switching specifications are tested with C_L = 15 pF and CMOS signal levels, unless otherwise noted. Supply currents are specified with 50% duty cycle signals.

Table 8. Data Channel Supply Current Specifications

		1 Mbps			10 Mbps			100 Mbps				
Parameter	**Symbol**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Unit**	**Test Conditions/Comments**
SUPPLY CURRENT												C_L = 0 pF
ADuM6221ABRNZ5												
	I_{DD1}		4.0	8.3		4.3	8.4		7.1	11.6	mA	
	I_{DD2}		2.1	4.4		2.7	5.6		8.0	11.6	mA	
ADuM6221ABRNZ3												
	I_{DD1}		4.0	8.3		4.3	8.4		7.1	11.6	mA	
	I_{DD2}		2.1	4.4		2.7	5.6		8.0	12.0	mA	

Table 9. Switching Specifications

Parameter	**Symbol**	**Min**	**Typ**	**Max**	**Unit**	**Test Conditions/Comments**
SWITCHING SPECIFICATIONS						
Pulse Width	PW	10			ns	Within PWD limit
Data Rate				100	Mbps	Within PWD limit
Propagation Delay	t_{PHL}, t_{PLH}	7.0	10	16	ns	50% input to 50% output
Pulse-Width Distortion	PWD		1.0	5.0	ns	$\lvert t_{PLH} - t_{PHL} \rvert$
Change vs. Temperature			1.5		ps/°C	
Propagation Delay Skew	t_{PSK}			8.0	ns	Between any two units at the same temperature, voltage, and load
Channel Matching			1	5.0	ns	
Jitter			816		ps p-p	

Table 10. Input and Output Characteristics

Parameter	**Symbol**	**Min**	**Typ**	**Max**	**Unit**	**Test Conditions/Comments**
DC SPECIFICATIONS						
Input Threshold						
Logic High	V_{IH}	0.7 × V_{DDx}			V	
Logic Low	V_{IL}			0.3 × V_{DDx}	V	
Output Voltage						
Logic High	V_{OH}	V_{DDx} − 0.2	V_{DDx}		V	I_{Ox}[1] = −20 μA, V_{Ix} = V_{IxH}[2]
		V_{DDx} − 0.5	V_{DDx} − 0.2		V	I_{Ox}[1] = −3.2 mA, V_{Ix} = V_{IxH}[2]
Logic Low	V_{OL}		0.0	0.1	V	I_{Ox}[1] = 20 μA, V_{Ix} = V_{IxL}[3]
			0.0	0.4	V	I_{Ox}[1] = 3.2 mA, V_{Ix} = V_{IxL}[3]
Undervoltage Lockout	UVLO					V_{DD1}, V_{DD2}, and V_{DDP} supply
Positive Going Threshold	V_{UV+}		1.6		V	
Negative Going Threshold	V_{UV-}		1.5		V	
Hysteresis	V_{UVH}		0.1		V	
Input Current per Channel	I_I	−10	+0.01	+10	μA	0 V ≤ V_{Ix} ≤ V_{DDx}
Quiescent Supply Current						
	$I_{DD1 (Q)}$		0.48	1.1	mA	V_{Ix} = Logic 0
	$I_{DD2 (Q)}$		0.8	1.5	mA	V_{Ix} = Logic 0
	$I_{DD1 (Q)}$		7.4	13.5	mA	V_{Ix} = Logic 1
	$I_{DD2 (Q)}$		3.2	6.2	mA	V_{Ix} = Logic 1

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Table 10. Input and Output Characteristics (Continued)

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
Dynamic Supply Current						
Dynamic Input	$I_{DDI (D)}$		0.01		mA/Mbps	Inputs switching, 50% duty cycle
Dynamic Output	$I_{DDO (D)}$		0.01		mA/Mbps	Inputs switching, 50% duty cycle
AC SPECIFICATIONS						
Output Rise/Fall Time	t_R/t_F		2.5		ns	10% to 90%
Common-Mode Transient Immunity[4]	$\lvert CM_H \rvert$	75	100		kV/µs	$V_{Ix} = V_{DD1}$ or V_{ISO}, V_{CM} = 1000 V
	$\lvert CM_L \rvert$	75	100		kV/µs	V_{Ix} = 0 V, V_{CM} = 1000 V

[1] I_{Ox} is the Channel x output current, where x means A or B.

[2] V_{IxH} is the input side logic high.

[3] V_{IxL} is the input side logic low.

[4] $\lvert CM_H \rvert$ is the maximum common-mode voltage slew rate that can be sustained while maintaining the voltage output $V_O > 0.8\ V_{DDx}$. $\lvert CM_L \rvert$ is the maximum common-mode voltage slew rate that can be sustained while maintaining $V_O < 0.8$ V. The common-mode voltage slew rates apply to both the rising and falling common-mode voltage edges.

ELECTRICAL CHARACTERISTICS—2.5 V OPERATION DIGITAL ISOLATOR CHANNELS ONLY

All typical specifications are at T_A = 25°C, $V_{DD1} = V_{DD2}$ = 2.5 V. Minimum and maximum specifications apply over the entire recommended operation range: 2.25 V ≤ V_{DD1}, V_{DD2} ≤ 2.75 V, and −40°C ≤ T_A ≤ +125°C, unless otherwise noted. Switching specifications are tested with C_L = 15 pF and CMOS signal levels, unless otherwise noted. Supply currents are specified with 50% duty cycle signals.

Table 11. Data Channel Supply Current Specifications

		1 Mbps			10 Mbps			100 Mbps				
Parameter	Symbol	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Unit	Test Conditions/Comments
SUPPLY CURRENT												C_L = 0 pF
ADuM6221ABRNZ5 and ADuM6221ABRNZ3												
	I_{DD1}		4.2	8.0		4.4	8.2		6.7	11.5	mA	
	I_{DD2}		2.3	4.4		2.4	5.4		6.5	10.0	mA	

Table 12. Switching Specifications

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
SWITCHING SPECIFICATIONS						
Pulse Width	PW	10			ns	Within PWD limit
Data Rate				100	Mbps	Within PWD limit
Propagation Delay	t_{PHL}, t_{PLH}	8.0	11	16	ns	50% input to 50% output
Pulse-Width Distortion	PWD		1.0	5.0	ns	$\lvert t_{PLH} - t_{PHL} \rvert$
Change vs. Temperature			1.5		ps/°C	
Propagation Delay Skew	t_{PSK}			8.0	ns	Between any two units at the same temperature, voltage, and load
Channel Matching			1	5.0	ns	
Jitter			816		ps p-p	

Table 13. Input and Output Characteristics

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
DC SPECIFICATIONS						
Input Threshold						
Logic High	V_{IH}	0.7 × V_{DDx}			V	
Logic Low	V_{IL}			0.3 × V_{DDx}	V	

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Table 13. Input and Output Characteristics (Continued)

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
Output Voltage						
Logic High	V_{OH}	V_{DDx} − 0.2	V_{DDx}		V	I_{Ox}[1] = −20 µA, V_{Ix} = V_{IxH}[2]
		V_{DDx} − 0.5	V_{DDx} − 0.2		V	I_{Ox}[1] = −3.2 mA, V_{Ix} = V_{IxH}[2]
Logic Low	V_{OL}		0.0	0.1	V	I_{Ox}[1] = 20 µA, V_{Ix} = V_{IxL}[3]
			0.0	0.4	V	I_{Ox}[1] = 3.2 mA, V_{Ix} = V_{IxL}[3]
Undervoltage Lockout	UVLO					V_{DD1}, V_{DD2}, and V_{DDP} supply
Positive Going Threshold	V_{UV+}		1.6		V	
Negative Going Threshold	V_{UV-}		1.5		V	
Hysteresis	V_{UVH}		0.1		V	
Input Current per Channel	I_I	−10	+0.01	+10	µA	0 V ≤ V_{Ix} ≤ V_{DDx}
Quiescent Supply Current						
	$I_{DD1 (Q)}$		0.5	1.0	mA	V_{Ix} = Logic 0
	$I_{DD2 (Q)}$		0.9	1.5	mA	V_{Ix} = Logic 0
	$I_{DD1 (Q)}$		7.4	13.5	mA	V_{Ix} = Logic 1
	$I_{DD2 (Q)}$		3.2	6.2	mA	V_{Ix} = Logic 1
Dynamic Supply Current						
Dynamic Input	$I_{DDI (D)}$		0.01		mA/Mbps	Inputs switching, 50% duty cycle
Dynamic Output	$I_{DDO (D)}$		0.01		mA/Mbps	Inputs switching, 50% duty cycle
AC SPECIFICATIONS						
Output Rise/Fall Time	t_R/t_F		2.5		ns	10% to 90%
Common-Mode Transient Immunity[4]	$\|CM_H\|$	75	100		kV/µs	V_{Ix} = V_{DD1} or V_{ISO}, V_{CM} = 1000 V
	$\|CM_L\|$	75	100		kV/µs	V_{Ix} = 0 V, V_{CM} = 1000 V

[1] I_{Ox} is the Channel x output current, where x means A or B.

[2] V_{IxH} is the input side logic high.

[3] V_{IxL} is the input side logic low.

[4] $|CM_H|$ is the maximum common-mode voltage slew rate that can be sustained while maintaining the voltage output V_O > 0.8 V_{DDx}. $|CM_L|$ is the maximum common-mode voltage slew rate that can be sustained while maintaining V_O < 0.8 V. The common-mode voltage slew rates apply to both the rising and falling common-mode voltage edges.

ELECTRICAL CHARACTERISTICS—1.8 V OPERATION DIGITAL ISOLATOR CHANNELS ONLY

All typical specifications are at T_A = 25°C, V_{DD1} = V_{DD2} = 1.8 V. Minimum and maximum specifications apply over the entire recommended operation range: 1.7 V ≤ V_{DD1}, V_{DD2} ≤ 1.9 V, and −40°C ≤ T_A ≤ +125°C, unless otherwise noted. Switching specifications are tested with C_L = 15 pF and CMOS signal levels, unless otherwise noted. Supply currents are specified with 50% duty cycle signals.

Table 14. Data Channel Supply Current Specifications

		1 Mbps			10 Mbps			100 Mbps				
Parameter	Symbol	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Unit	Test Conditions/Comments
SUPPLY CURRENT												C_L = 0 pF
ADuM6221ABRNZ5 and ADuM6221ABRNZ3												
	I_{DD1}		4.1	8.0		4.4	8.0		6.7	11.5	mA	
	I_{DD2}		2.3	4.4		2.6	5.3		6.5	9.5	mA	

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Table 15. Switching Specifications

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
SWITCHING SPECIFICATIONS						
Pulse Width	PW	10			ns	Within PWD limit
Data Rate				100	Mbps	Within PWD limit
Propagation Delay	t_{PHL}, t_{PLH}	8.0	12	17	ns	50% input to 50% output
Pulse-Width Distortion	PWD		1.0	5.0	ns	$\lvert t_{PLH} - t_{PHL} \rvert$
Change vs. Temperature			1.5		ps/°C	
Propagation Delay Skew	t_{PSK}			8.0	ns	Between any two units at the same temperature, voltage, and load
Channel Matching			1	5.0	ns	
Jitter			816		ps p-p	

Table 16. Input and Output Characteristics

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
DC SPECIFICATIONS						
Input Threshold						
Logic High	V_{IH}	0.7 × V_{DDx}			V	
Logic Low	V_{IL}			0.3 × V_{DDx}	V	
Output Voltages						
Logic High	V_{OH}	V_{DDx} − 0.1	V_{DDx}		V	I_{Ox}[1] = −20 µA, V_{Ix} = V_{IxH}[2]
		V_{DDx} − 0.4	V_{DDx} − 0.2		V	I_{Ox}[1] = −3.2 mA, V_{Ix} = V_{IxH}[2]
Logic Low	V_{OL}		0.0	0.1	V	I_{Ox}[1] = 20 µA, V_{Ix} = V_{IxL}[3]
			0.2	0.4	V	I_{Ox}[1] = 3.2 mA, V_{Ix} = V_{IxL}[3]
Undervoltage Lockout	UVLO					V_{DD1}, V_{DD2}, and V_{DDP} supply
Positive Going Threshold	V_{UV+}		1.6		V	
Negative Going Threshold	V_{UV-}		1.5		V	
Hysteresis	V_{UVH}		0.1		V	
Input Current per Channel	I_I	−10	+0.01	+10	µA	0 V ≤ V_{Ix} ≤ V_{DDx}
Quiescent Supply Current						
	$I_{DD1 (Q)}$		0.5	1.0	mA	V_{Ix} = Logic 0
	$I_{DD2 (Q)}$		0.9	1.4	mA	V_{Ix} = Logic 0
	$I_{DD1 (Q)}$		7.5	13.5	mA	V_{Ix} = Logic 1
	$I_{DD2 (Q)}$		3.2	6.2	mA	V_{Ix} = Logic 1
Dynamic Supply Current						
Input	$I_{DDI (D)}$		0.01		mA/Mbps	Inputs switching, 50% duty cycle
Output	$I_{DDO (D)}$		0.01		mA/Mbps	Inputs switching, 50% duty cycle
AC SPECIFICATIONS						
Output Rise/Fall Time	t_R/t_F		2.5		ns	10% to 90%
Common-Mode Transient Immunity[4]	$\lvert CM_H \rvert$	75	100		kV/µs	V_{Ix} = V_{DD1} or V_{ISO}, V_{CM} = 1000 V
	$\lvert CM_L \rvert$	75	100		kV/µs	V_{Ix} = 0 V, V_{CM} = 1000 V

[1] I_{Ox} is the Channel x output current, where x means A or B.

[2] V_{IxH} is the input side logic high.

[3] V_{IxL} is the input side logic low.

[4] $\lvert CM_H \rvert$ is the maximum common-mode voltage slew rate that can be sustained while maintaining the voltage output V_O > 0.8 V_{DDx}. $\lvert CM_L \rvert$ is the maximum common-mode voltage slew rate that can be sustained while maintaining V_O < 0.8 V. The common-mode voltage slew rates apply to both the rising and falling common-mode voltage edges.

SPECIFICATIONS

PACKAGE CHARACTERISTICS

Table 17. Thermal and Isolation Characteristics

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
Resistance (Input to Output)[1]	R_{I-O}		10^{13}		Ω	
Capacitance (Input to Output)[1]	C_{I-O}		2.2		pF	Frequency = 1 MHz
Input Capacitance[2]	C_I		4.0		pF	
IC Junction to Ambient Thermal Resistance	θ_{JA}		45		°C/W	Thermocouple located at center of package underside, test conducted on 4-layer board with thin traces[3]

[1] The device is considered a 2-terminal device: Pin 1 to Pin 14 are shorted together, and Pin 15 to Pin 28 are shorted together.

[2] Input capacitance is from any input data pin to ground.

[3] For thermal model definitions, see the Thermal Analysis section.

REGULATORY APPROVALS

The ADuM6221A certification approvals are listed in Table 18.

Table 18. Regulatory Approvals

Regulatory Agency	Standard Certification/Approval	File
UL	1577 Single protection, 5000 V rms[1]	E214100
VDE (Pending)	DIN EN IEC 60747-17 (VDE 0884-17) Reinforced insulation, V_{IORM} = 596 V peak[2]	Certificate No. (pending)
CSA[3]	IEC/EN/CSA 62368-1 Basic insulation, 830 V rms Reinforced insulation, 415 V rms IEC/CSA 61010-1 Basic insulation, 600 V rms Reinforced insulation, 300 V rms IEC/CSA 60601-1 Basic insulation (1 MOPP), 519 V rms	File No. 205078
TÜV Süd (Pending)	Certified as component level device EN 62368-1: 2020+A11:2020	Pending
CQC (Pending)	CQC GB4943.1 Basic insulation, 830 V rms Reinforced insulation, 415 V rms	Certificate No. CQC22001370855

[1] In accordance with UL 1577, each product is proof tested by applying an insulation test voltage ≥ 6000 V rms for 1 sec.

[2] In accordance with DIN EN IEC 60747-17 (VDE 0884-17), each product is proof tested by applying an insulation test voltage ≥ 1118 V peak for 1 sec (partial discharge detection limit = 5 pC).

[3] Working voltages are quoted for Pollution Degree 2, Material Group III.

SPECIFICATIONS

INSULATION AND SAFETY RELATED SPECIFICATIONS

Table 19. Critical Safety Related Dimensions and Material Properties

Parameter	Symbol	Value	Unit	Test Conditions/Comments
Rated Dielectric Insulation Voltage		5000	V rms	1-minute duration
Minimum External Air Gap (Clearance)[1, 2]	L(I01)	8.3	mm	Measured from input terminals to output terminals, shortest distance through air
Minimum External Tracking (Creepage)	L(I02)	8.3	mm	Measured from input terminals to output terminals, shortest distance path along body
Minimum Clearance in the Plane of the PCB	L (PCB)	8.3	mm	Measured from input terminals to output terminals, shortest distance through air, line of sight, in the PCB mounting plane
Minimum Internal Gap (Internal Clearance)		21.5	µm	Minimum distance through insulation
Tracking Resistance (Comparative Tracking Index)	CTI	>600	V	DIN IEC 112/VDE 0303, Part 1
Material Group		I		Material group per IEC 60664-1

[1] In accordance with IEC 62368-1/IEC 60601-1 guidelines for the measurement of creepage and clearance distances for a pollution degree of 2 and altitudes ≤2000 m.

[2] Consideration must be given to pad layout to ensure the minimum required distance for clearance is maintained.

DIN EN IEC 60747-17 (VDE 0884-17) INSULATION CHARACTERISTICS

These isolators are suitable for reinforced electrical isolation only within the safety limit data. Maintenance of the safety data is ensured by the protective circuits. The asterisk (*) marking on packages denotes DIN EN IEC 60747-17 (VDE 0884-17) approval.

Table 20. VDE Characteristics

Description	Test Conditions/Comments	Symbol	Characteristic	Unit
Overvoltage Category per IEC 60664-1				
For Rated Mains Voltage ≤ 150 V rms			I to IV	
For Rated Mains Voltage ≤ 300 V rms			I to IV	
For Rated Mains Voltage ≤ 400 V rms			I to IV	
Climatic Classification			40/125/21	
Pollution Degree per DIN VDE 0110, Table 1			2	
Maximum Repetitive Isolation Voltage		V_{IORM}	596	V peak
Maximum Working Insulation Voltage		V_{IOWM}	421	V rms
Input to Output Test Voltage, Method b1	$V_{IORM} \times 1.875 = V_{pd(m)}$, 100% production test, t_m = 1 sec, partial discharge < 5 pC	$V_{pd(m)}$	1118	V peak
Input to Output Test Voltage, Method a				
After Environmental Tests Subgroup 1	$V_{IORM} \times 1.6 = V_{pd(m)}$, t_{ini} = 60 sec, t_m = 10 sec, partial discharge < 5 pC	$V_{pd(m)}$	954	V peak
After Input and/or Safety Test Subgroup 2 and Subgroup 3	$V_{IORM} \times 1.2 = V_{pd(m)}$, t_{ini} = 60 sec, t_m = 10 sec, partial discharge < 5 pC	$V_{pd(m)}$	715	V peak
Maximum Transient Isolation Voltage	$V_{TEST} = 1.2 \times V_{IOTM}$, t = 1 sec (100% production)	V_{IOTM}	8000	V peak
Maximum Impulse Voltage	Surge voltage in air, waveform per IEC 61000-4-5	V_{IMP}	8000	V peak
Withstand Isolation Voltage	1-minute withstand rating	V_{ISO}	5000	V rms
Maximum Surge Isolation Voltage	$V_{TEST} \geq 1.3 \times V_{IMP}$ (sample test), tested in oil, waveform per IEC 61000-4-5	V_{IOSM}	12,800	V peak
Safety Limiting Values				
	Maximum value allowed in the event of a failure (see Figure 2)			
Case Temperature		T_S	150	°C
Total Power Dissipation at 25°C		P_{S1}	2.78	W
Insulation Resistance at T_S	V_{IO} = 500 V	R_S	$>10^9$	Ω

SPECIFICATIONS

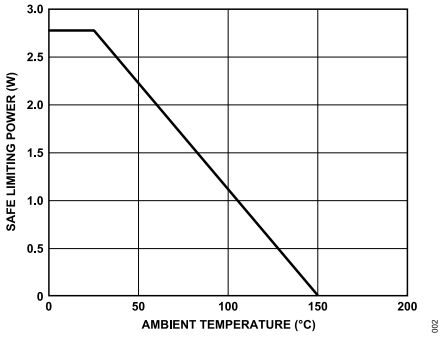

Figure 2. Thermal Derating Curve, Dependence of Safety Limiting Values on Case Temperature, per DIN EN IEC 60747-17 (VDE 0884-17)

ABSOLUTE MAXIMUM RATINGS

T_A = 25°C, unless otherwise noted.

Table 21. Absolute Maximum Ratings

Parameter	Rating
Supply Voltages (V_{DD1}, V_{DDP}, V_{DD2}, V_{ISO})[1]	−0.5 V to +7.0 V
V_{ISO} Supply Current[2]	100 mA
Input Voltage (V_{IA}, V_{IB},V_{SEL}, PDIS)[1, 3]	−0.5 V to V_{DDI} + 0.5 V
Output Voltage (V_{OA}, V_{OB})[1, 3]	−0.5 V to V_{DDO} + 0.5 V
Average Output Current Per Data Output Pin[4]	−10 mA to +10 mA
Common-Mode Transients[5]	−200 kV/µs to +200 kV/µs
Temperature	
Storage (T_{ST})	−55°C to +150°C
Ambient Operating	−40°C to +125°C

1 All voltages are relative to their respective ground.

2 The V_{ISO} pin may provide current for DC and dynamic loads when connected to V_{DD2}. This current must be included when determining the total V_{ISO} supply current. For ambient temperatures between 85°C and 125°C, the maximum allowed current is reduced.

3 V_{DDI} and V_{DDO} refer to the supply voltages on the input and output sides of a given channel, respectively. For more details, see the PCB Layout section.

4 For the maximum rated current values for various temperatures, see Figure 2.

5 Common-mode transients refer to common-mode transients across the insulation barrier. Common-mode transients exceeding the absolute maximum ratings may cause latch-up or permanent damage.

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

MAXIMUM CONTINUOUS WORKING VOLTAGE

Table 22. ADuM6221A Maximum Continuous Working Voltage[1]

Parameter	Rating	Unit	Applicable Certification
AC Voltage			
Bipolar Waveform	596	V peak	Reinforced insulation rating per IEC 60747-17 (VDE 0884-17)

1 Maximum continuous working voltage refers to the continuous voltage magnitude imposed across the isolation barrier.

PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS

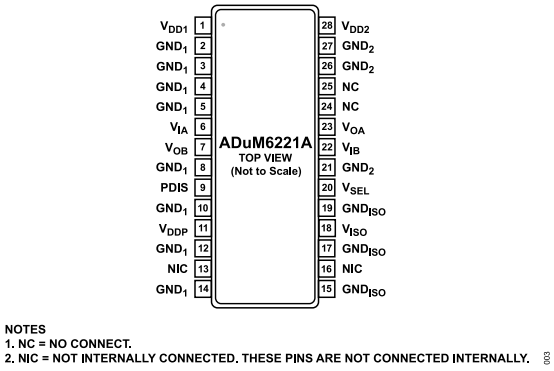

Figure 3. ADuM6221A Pin Configuration

Table 23. ADuM6221A Pin Function Descriptions

Pin Number	Mnemonic	Description
1	V_{DD1}	Power Supply for the Side 1 Logic Circuits of the Device. V_{DD1} requires a 0.10 µF bypass capacitor to GND_1. V_{DD1} is independent of V_{DDP} and can operate with power supply voltages between 1.7 V and 5.5 V.
2, 3, 4, 5, 8, 10, 12, 14	GND_1	Ground 1. Ground references for the primary isolator. Pin 2, Pin 3, Pin 4, Pin 5, Pin 8, Pin 10, Pin 12, and Pin 14 are internally connected, and it is recommended to connect the GND_1 pins to a common ground.
6	V_{IA}	Logic Input A.
7	V_{OB}	Logic Output B.
9	PDIS	Power Disable. When PDIS is connected to GND_1, the power converter is active. When a logic high voltage is applied to PDIS, the power supply enters low power standby mode.
11	V_{DDP}	DC-to-DC Converter Supply Voltage. 3.0 V to 5.5 V. V_{DDP} requires 0.10 µF and 10 µF bypass capacitors to GND_1. ADuM6221ABRNZ3 is to be used in the 3.3 V to 3.3 V configuration. ADuM6221ABRNZ5 is to be used in the 5 V to 3.3 V and 5 V to 5 V configuration.
13, 16	NIC	Not Internally Connected. These pins are not connected internally.
15, 17, 19	GND_{ISO}	Grounds for the Isolated DC-to-DC Converter. For low EMI, see recommendations listed under PCB layout. The GND_{ISO} pins are internally isolated from GND_2.
18	V_{ISO}	Secondary Supply Voltage Output for External Loads. V_{ISO} requires 0.10 µF and 10 µF capacitors to GND_{ISO}. For low EMI, see the recommendations shown in the PCB Layout section. ADuM6221ABRNZ3 is to be used in the 3.3 V to 3.3 V configuration. ADuM6221ABRNZ5 is to be used in the 5 V to 3.3 V and 5 V to 5 V configuration.
20	V_{SEL}	Output Voltage Select Input. Connect V_{SEL} to V_{ISO} for a 5 V output or to GND_{ISO} for a 3.3 V output.
21, 26, 27	GND_2	Ground References for V_{DD2} on Side 2. It is recommended that the GND_2 pins be connected together. The GND_2 pins are internally isolated from GND_{ISO}.
22	V_{IB}	Logic Input B.
23	V_{OA}	Logic Output A.
24, 25	NC	No Connect.
28	V_{DD2}	Power Supply for the Side 2 Logic Circuits of the Device. V_{DD2} requires a 100 nF bypass capacitor. V_{DD2} is independent of V_{ISO} and can operate with power supply voltages between 1.7 V and 5.5 V.

PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS

TRUTH TABLE

Table 24. Data Section Truth Table (Positive Logic)

V_{DDI} State[1]	V_{Ix} Input[1]	V_{DDO} State[1]	V_{Ox} Output[1]	Notes
Powered	High	Powered	High	Normal operation, data is high.
Powered	Low	Powered	Low	Normal operation, data is low.
Do not care	Do not care	Unpowered	High-Z	Output is off.
Unpowered	Low	Powered	Low	Output default low.
Unpowered	High	Powered	Indeterminate	If a high level is applied to an input when no supply is present, the input can parasitically power the input side, which may cause unpredictable operation.

[1] V_{DDI} and V_{DDO} refer to the supply voltages on the input and output sides of the given channel, respectively. V_{Ix} and V_{Ox} refer to the input and output signals of a given channel (Channel A or Channel B).

Table 25. Power Section Truth Table (Positive Logic)

V_{DDP} (V)	V_{SEL} Input	PDIS Input	V_{ISO} (V)
5	High	Low	5
5	Do not care	High	0
5	Low	Low	3.3
3.3	Low	Low	3.3
3.3	High	Low	Condition not supported
3.3	Do not care	High	0

TYPICAL PERFORMANCE CHARACTERISTICS

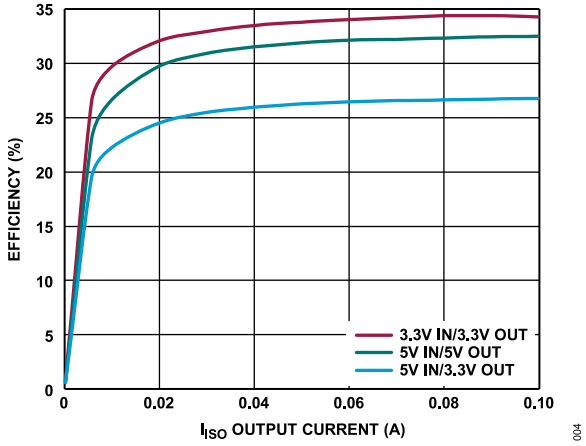

Figure 4. Power Supply Efficiency in Supported Power Configurations

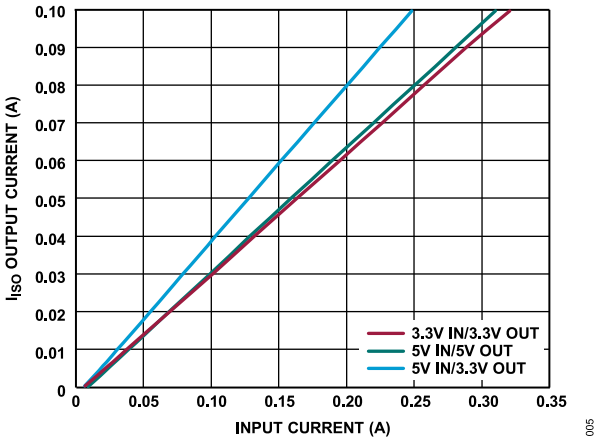

Figure 5. I_{ISO} Output Current vs. Input Current in Supported Power Configurations

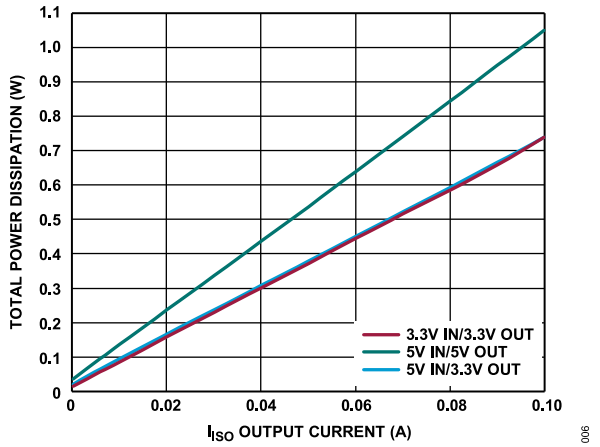

Figure 6. Total Power Dissipation vs. I_{ISO} Output Current in Supported Power Configurations

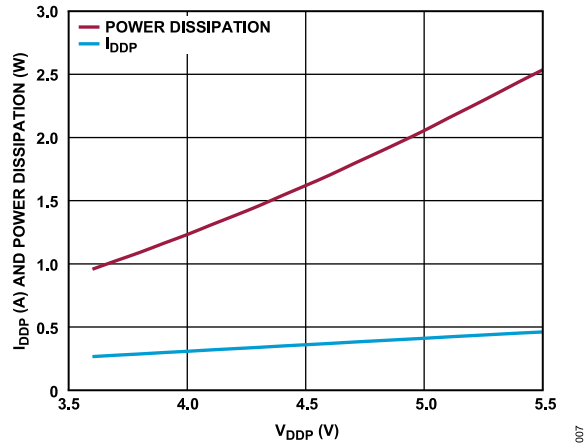

Figure 7. Short-Circuit Input Current (I_{DDP}) and Power Dissipation vs. V_{DDP}

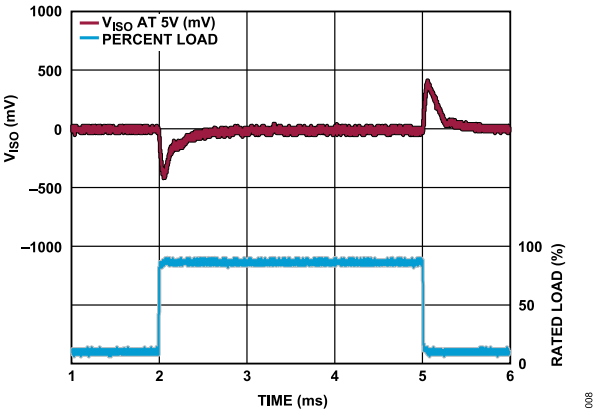

Figure 8. V_{ISO} Transient Load Response, 5 V Output, 10% to 90% Load Step

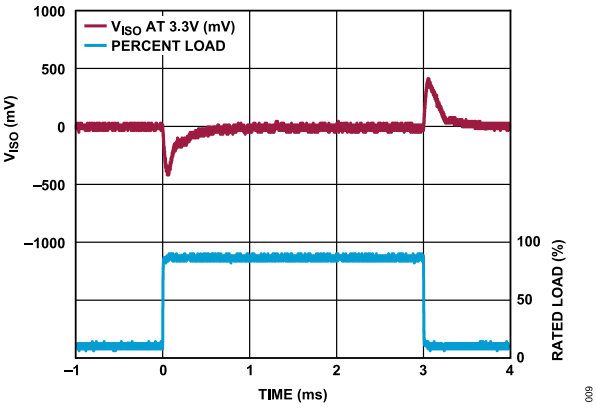

Figure 9. V_{ISO} Transient Load Response, 5 V Input, 3.3 V Output, 10% to 90% Load Step

TYPICAL PERFORMANCE CHARACTERISTICS

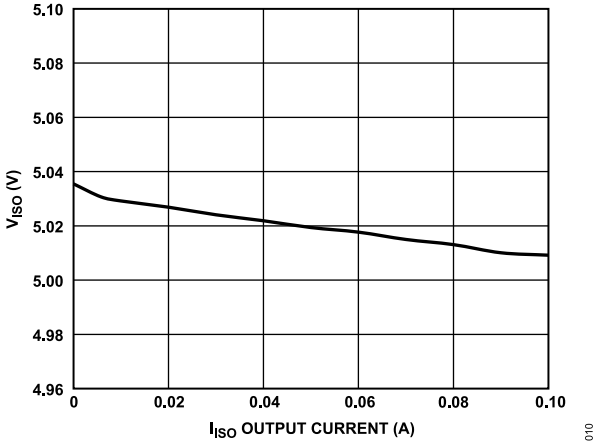

Figure 10. V_{ISO} vs. I_{ISO} Output Current, Input = 5 V, V_{ISO} = 5 V

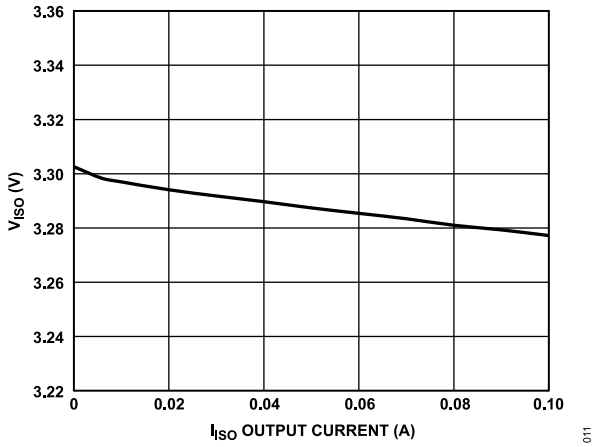

Figure 11. V_{ISO} vs. I_{ISO} Output Current, Input = 5 V, V_{ISO} = 3.3 V

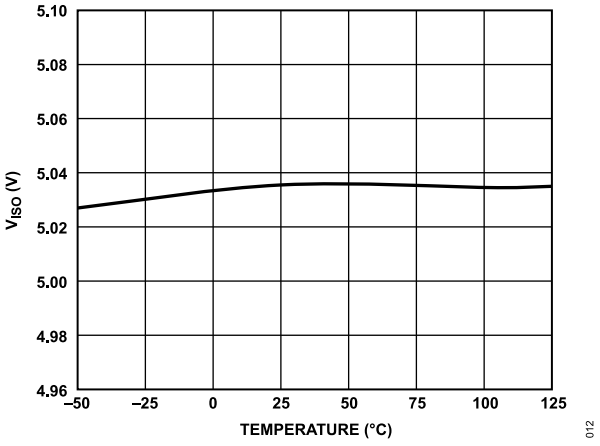

Figure 12. V_{ISO} vs. Temperature, Input = 5 V, V_{ISO} = 5 V

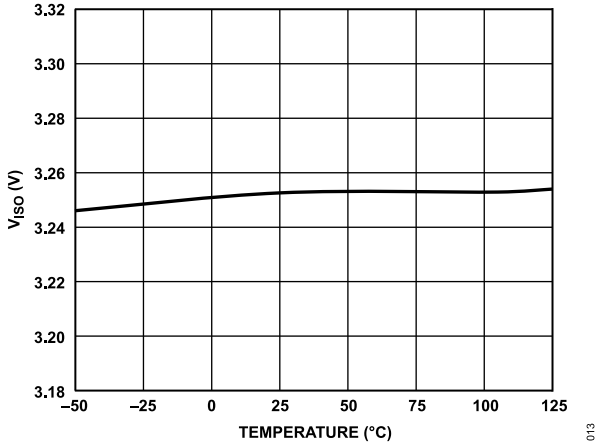

Figure 13. V_{ISO} vs. Temperature, Input = 3.3 V, V_{ISO} = 3.3 V

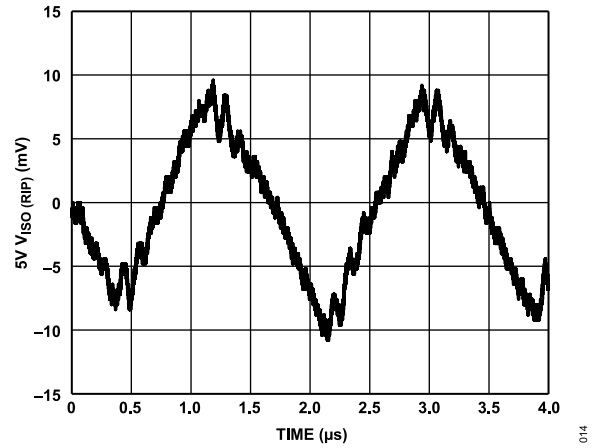

Figure 14. Output Voltage Ripple at 90% Load, V_{ISO} = 5 V

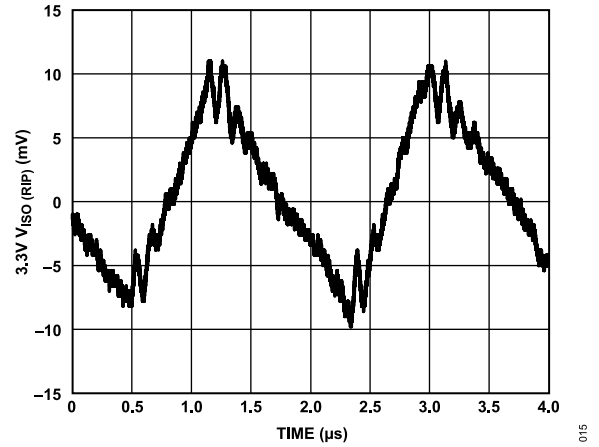

Figure 15. Output Voltage Ripple at 90% Load, V_{ISO} = 3.3 V

TYPICAL PERFORMANCE CHARACTERISTICS

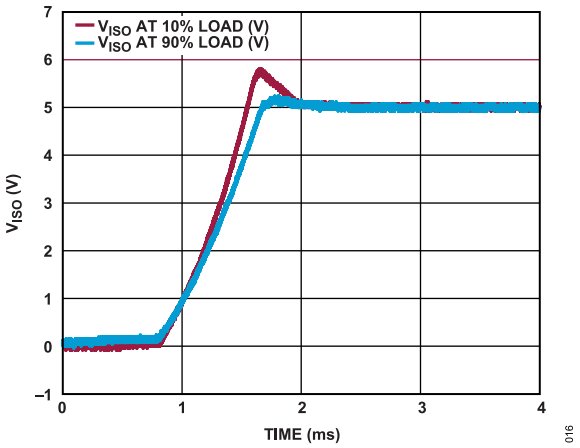

Figure 16. 5 V Input to 5 V Output V_{ISO} Start-Up Transient at 10% and 90% Load

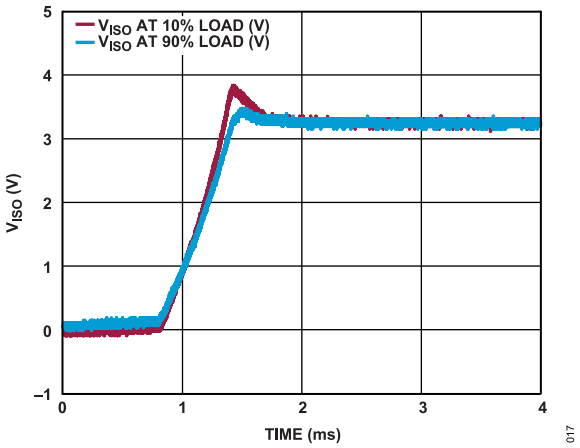

Figure 17. 5 V Input to 3.3 V Output V_{ISO} Start-Up Transient at 10% and 90% Load

TERMINOLOGY

I_{DD1}

I_{DD1} is the supply current required for the primary side of the digital isolator.

I_{DD2}

I_{DD2} is the supply current required for the secondary side of the digital isolator.

I_{DDP}

I_{DDP} is the supply current required for the primary side of the isolated DC-to-DC converter.

I_{ISO}

I_{ISO} is the available isolated current supply available to an external load.

Propagation Delay, t_{PHL}

t_{PHL} is measured from the 50% level of the falling edge of the V_{Ix} signal to the 50% level of the falling edge of the V_{Ox} signal.

Propagation Delay, t_{PLH}

t_{PLH} is measured from the 50% level of the rising edge of the V_{Ix} signal to the 50% level of the rising edge of the V_{Ox} signal.

Propagation Delay Skew, t_{PSK}

t_{PSK} is the magnitude of the worst-case difference in t_{PHL} and/or t_{PLH} that is measured between units at the same operating temperature, supply voltages, and output load within the recommended operating conditions.

Minimum Pulse Width

The minimum pulse width is the shortest pulse width at which the specified pulse width distortion is guaranteed.

Maximum Data Rate

The maximum data rate is the fastest data rate at which the specified pulse width distortion is guaranteed.

THEORY OF OPERATION

The DC-to-DC converter section of the ADuM6221A works on principles that are common to most modern power supplies. The ADuM6221A have a split controller architecture with isolated PWM feedback. V_{DDP} power is supplied to an oscillating circuit that switches current into a chip scale, air core transformer. Power transferred to the secondary side is rectified and regulated to a value of 3.3 V or 5 V, which depends on the setting of the V_{SEL} pin. The secondary (V_{ISO}) side controller regulates the output by creating a PWM control signal that is sent to the primary (V_{DDP}) side by a dedicated *i*Coupler data channel. The PWM modulates the oscillator circuit to control the power being sent to the secondary side. Feedback allows for significantly higher power and efficiency.

The ADuM6221A implement undervoltage lockout (UVLO) with hysteresis on the primary and the secondary side input and output pins as well as the V_{DDP} power input. This feature ensures that the converter does not enter oscillation due to noisy input power or slow power-on ramp rates.

The digital isolator channels use a high frequency carrier to transmit data across the isolation barrier using *i*Coupler chip scale transformer coils separated by layers of polyimide isolation. Using an on/off keying technique and the differential architecture shown in Figure 18, the digital isolator channels have low propagation delay and high speed. Internal regulators and input and output design techniques allow logic and supply voltages over a wide range from 1.7 V to 5.5 V, which offers the voltage translation of 1.8 V, 2.5 V, 3.3 V, and 5 V logic. The architecture is designed for high common-mode transient immunity and high immunity to electrical noise and magnetic interference. Radiated emissions are minimized with a spread spectrum on/off keying carrier and other techniques.

Figure 18 shows the waveforms of the digital isolator channels that have the condition of the fail-safe output state equal to low, where the carrier waveform is off when the input state is low. If the input side is off or not operating, the low fail-safe output state sets the output to low.

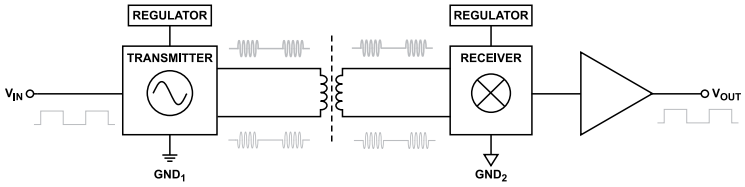

Figure 18. Operational Block Diagram of a Single Channel with a Low Fail-Safe Output State, V_{IN} is the Input Voltage and V_{OUT} is the Output Voltage

APPLICATIONS INFORMATION

PCB LAYOUT

The ADuM6221A digital isolator with an *iso*Power integrated DC-to-DC converter require no external interface circuitry for the logic interfaces. Power supply bypassing is required at the input and output supply pins (see Figure 19, Figure 20, and Figure 21). For proper data channel operation, low equivalent series resistance (ESR) bypass capacitors of 0.01 µF to 0.1 µF are required between the V_{DD1} and GND_1 pins as close to the chip pads as possible. Low ESR bypass capacitors of 0.1 µF or 0.22 µF are required between the V_{ISO} and GND_{ISO} pins as close to the chip pads as possible (see the C_{ISO} notes in Figure 20 and Figure 21). Installing the bypass capacitor with traces more than 2 mm in length may result in data corruption. The *iso*Power inputs require several passive components to bypass the power effectively, as well as set the output voltage.

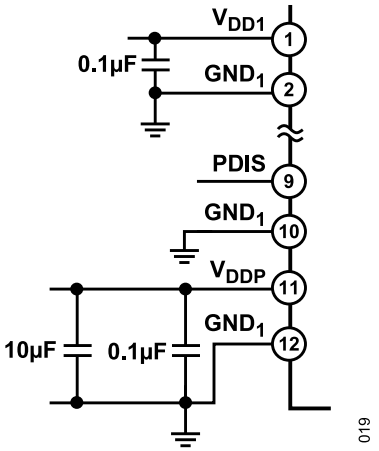

Figure 19. V_{DD1} and V_{DDP} Bias and Bypass Components

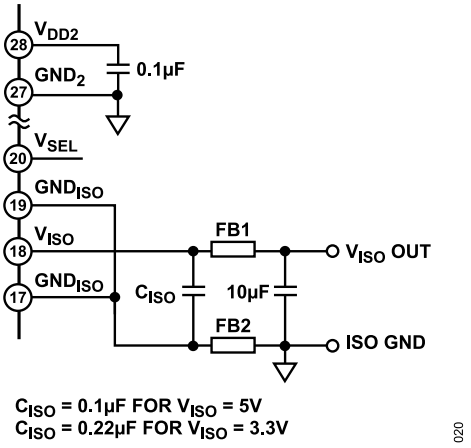

Figure 20. V_{DD2} and V_{ISO} Bias and Bypass Components

The power supply section of the ADuM6221A use a 180 MHz oscillator frequency to efficiently pass power through the chip scale transformers. Bypass capacitors are required for several operating frequencies. Noise suppression requires a low inductance and high frequency capacitor. Ripple suppression and proper regulation require a large value capacitor. These capacitors are connected between the V_{DDP} and GND_1 pins and between the V_{ISO} and GND_{ISO} pins. To suppress noise and reduce ripple, a parallel combination of at least two capacitors is required. The required capacitor values are 0.1 µF and 10 µF for V_{DD1}. The smaller capacitor must have a low ESR. For example, use of a ceramic capacitor is advised. The total lead length between the ends of the low ESR capacitor and the input power supply pin must not exceed 2 mm.

To reduce the level of electromagnetic radiation, the impedance to high frequency currents between the V_{ISO} and the GND_{ISO} pins and the PCB trace connections can be increased. Using this method of electromagnetic interference (EMI) suppression controls the radiating signal at the signal source by placing surface-mount ferrite beads in series with the V_{ISO} and GND_{ISO} pins, as seen in Figure 21. Note that if ferrite beads are used, all guaranteed electrical specifications may not be met due to the additional series resistance (DCR). The impedance of the ferrite beads must be approximately 1.8 kΩ between the 100 MHz and 1 GHz frequency range to reduce the emissions at the 180 MHz primary switching frequency and the 360 MHz secondary side, which rectifies frequency and harmonics. For examples of appropriate surface-mount ferrite beads, see Table 26.

Table 26. Surface-Mount Ferrite Bead Examples

Manufacturer	Part Number	Size	DCR (Ω)
Taiyo Yuden	BKH1005LM182-T	0402	2.0
Murata Electronics	BLM15HD182SN1	0402	2.2
Murata Electronics	BLM18HE152SN1	0603	0.5

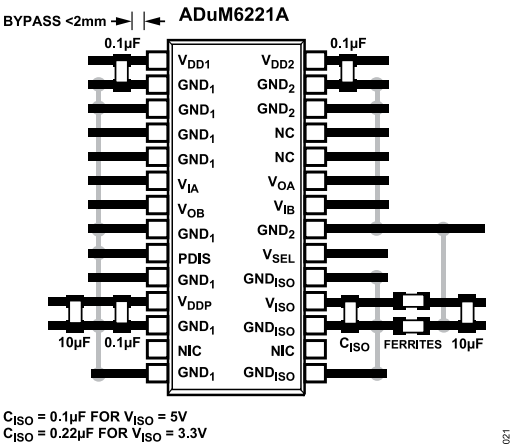

Figure 21. Recommended PCB Layout

In applications involving high common-mode transients, ensure that the board coupling across the isolation barrier is minimized. Furthermore, design the board layout such that any coupling that does occur equally affects all pins on a given component side. Failure to ensure these steps can cause voltage differentials between pins, which exceeds the absolute maximum ratings specified in Table 21, thereby leading to latch-up and/or permanent damage.

APPLICATIONS INFORMATION

THERMAL ANALYSIS

The ADuM6221A consists of five internal die attached to a split lead frame with two die attach pads. For the purposes of thermal analysis, the die is treated as a thermal unit, with the highest junction temperature reflected in the θ_{JA} value from Table 17. The value of θ_{JA} is based on measurements taken with the devices mounted on a JEDEC standard, 4-layer board with fine width traces and still air. Under normal operating conditions, the ADuM6221A can operate at full load. However, at temperatures above 85°C, derating the output current may be needed, as shown in Figure 2.

PROPAGATION DELAY RELATED PARAMETERS

Propagation delay is a parameter that describes the time it takes a logic signal to propagate through a component (see Figure 22). The propagation delay to a logic low output may differ from the propagation delay to a logic high.

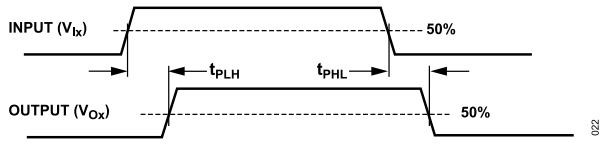

Figure 22. Propagation Delay Parameters

PWD is the maximum difference between these two propagation delay values and is an indication of how accurately the input signal timing is preserved.

Channel-to-channel matching refers to the maximum amount the propagation delay differs between channels within a single ADuM6221A component.

Propagation delay skew refers to the maximum amount the propagation delay differs between multiple ADuM6221A components operating under the same conditions.

ELECTROMAGNETIC COMPATIBILITY

The DC-to-DC converter section of the ADuM6221A components must, of necessity, operate at a high frequency to allow efficient power transfer through the small transformers, which creates high frequency currents that can propagate in circuit board ground and power planes, which requires proper power supply bypassing at the input and output supply pins (see Figure 21). Using proper layout and bypassing techniques, the DC-to-DC converter is designed to provide regulated and isolated power that is below CISPR 32/EN 55032 Class B limits up to 5 Mbps at full load on a 2-layer PCB with ferrites.

POWER CONSUMPTION

The V_{DDP} power supply input only provides power to the converter. Power for the data channels is provided through V_{DD1} and V_{DD2}. These power supplies can be connected to V_{DDP} and V_{ISO} if required, or the supplies can receive power from an independent source. Treat the converter as a standalone supply to be utilized at the discretion of the designer.

The V_{DD1} or V_{DD2} supply current at a given channel of the ADuM6221A isolator is a function of the supply voltage, the data rate of the channel, and the output load of the channel.

The V_{DD1} and V_{DD2} supply current and the total supply currents as a function of data rate for the ADuM6221A for an unloaded output condition are shown under typical supply and room temperature conditions in the figures shown in the Typical Performance Characteristics section. The total I_{ISO} output current as a function of input current for the ADuM6221A is shown in Figure 5. In addition, the total power dissipation as a function of output current is shown in Figure 6.

OUTLINE DIMENSIONS

Package Drawing (Option)	Package Type	Package Description
RN-28-1	SOIC_W_FP	28-Lead Standard Small Outline, Wide Body, with Finer Pitch

For the latest package outline information and land patterns (footprints), go to Package Index.

ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Packing Quantity	Package Option
ADuM6221ABRNZ3	−40°C to +125°C	28-Lead SOIC_W_FP		RN-28-1
ADuM6221ABRNZ3-RL	−40°C to +125°C	28-Lead SOIC_W_FP	Reel, 1000	RN-28-1
ADuM6221ABRNZ5	−40°C to +125°C	28-Lead SOIC_W_FP		RN-28-1
ADuM6221ABRNZ5-RL	−40°C to +125°C	28-Lead SOIC_W_FP	Reel, 1000	RN-28-1

[1] Z = RoHS-Compliant Part.

Updated: February 05, 2024

EVALUATION BOARDS

Model[1, 2]	Description
EVAL-ADuM6421AURNZ	Evaluation Board

[1] Z = RoHS-Compliant Part.

[2] The EVAL-ADuM6421AURNZ is packaged without a device installed. The ADuM6221A must be ordered separately and installed.