ADuM6210/ADuM6211/ADuM6212

Dual-Channel Isolators with Integrated DC-to-DC Converters

FEATURES

- *iso*Power integrated, isolated dc-to-dc converter
- Regulated 3.135 V to 5.25 V output
- Up to 150 mW output power
- Dual dc-to-100 Mbps (NRZ) signal isolation channels
- Soft start power supply
- 20-lead SSOP package with 5.3 mm creepage
- Supports SPI up to 15 MHz
- High temperature operation: 105°C
- High common-mode transient immunity: >25 kV/μs
- Safety and regulatory approvals
  - UL 1577
    - V_{ISO} = 3750 V rms for 1 minute
  - IEC/CSA 62368-1
  - IEC/CSA 61010-1
  - DIN EN IEC 60747-17 (VDE 0884-17)
    - V_{IORM} = 600 V peak

APPLICATIONS

- RS-232 transceivers
- Power supply start-up bias and gate drives
- Isolated sensor interfaces
- Industrial PLCs

GENERAL DESCRIPTION

The ADuM6210/ADuM6211/ADuM6212[1] are dual-channel digital isolators with *iso*Power®, an integrated, isolated dc-to- dc converter. Based on the Analog Devices, Inc., *i*Coupler® technology, the dc-to-dc converter provides regulated, isolated power that is adjustable between 3.135 V and 5.25 V. Input supply voltages can range from slightly below the required output to significantly higher. Popular voltage combinations and their associated power levels are shown in Table 2.

The ADuM6210/ADuM6211/ADuM6212 eliminate the need for a separate, isolated dc-to-dc converter in low power, isolated designs. The *i*Coupler chip-scale transformer technology is used for isolated logic signals and for the magnetic components of the dc-to-dc converter. The result is a small form factor, total isolation solution.

*iso*Power uses high frequency switching elements to transfer power through its transformer. Take special care during printed circuit board (PCB) layout to meet emissions standards. See the AN-0971 Application Note for board layout recommendations.

FUNCTIONAL BLOCK DIAGRAM

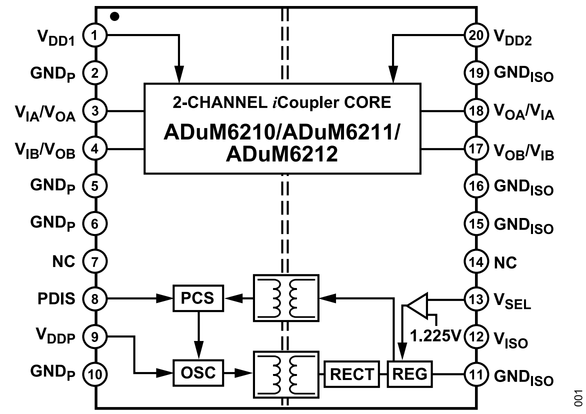

Figure 1. ADuM6210/ADuM6211/ADuM6212

Table 1. Data I/O Port Assignments

Channel	Pin	ADuM6210	ADuM6211	ADuM6212
V_{IA}/V_{IA}	3	V_{IA}	V_{OA}	V_{OA}
V_{IB}/V_{OB}	4	V_{IB}	V_{IB}	V_{OB}
V_{OA}/V_{IA}	18	V_{OA}	V_{IA}	V_{IA}
V_{OB}/V_{IB}	17	V_{OB}	V_{OB}	V_{IB}

Table 2. Power Levels

Input Voltage (V)	Output Voltage (V)	Output Power (mW)
5	5	150
5	3.3	100
3.3	3.3	66

[1] Protected by U.S. Patents 5,952,849; 6,873,065; 6,903,578; and 7,075,329. Other patents are pending.

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REVISION HISTORY

1/2026—Rev. F to Rev. G

Change to Features Section.. 1
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Added Regulatory Approvals Section and Table 15; Renumbered Sequentially........ 9
Changed DIN EN IEC 60747-17 (VDE 0884-17) Insulation Characteristics Section to Insulation Specifications Section........ 10
Changes to Insulation Specifications Section........ 10
Changes to Table 16........ 10
Deleted Table 21........ 13
Changes to Thermal Analysis Section........ 22
Changes to Insulation Lifetime Section........ 23

3/2025—Rev. E to Rev. F

Changes to Features Section........ 1
Changed Regulatory Approvals Section to Regulatory Information Section........ 9
Changes to Regulatory Information Section and Table 16........ 9
Changes to Table 17........ 9
Changed DIN V VDE V 0884-10 (VDE V 0884-10) Insulation Characteristics Section to DIN EN IEC 60747-17 (VDE 0884-17) Insulation Characteristics Section........ 10
Changes to DIN EN IEC 60747-17 (VDE 0884-17) Insulation Characteristics Section, Table 18, and Figure 2 Caption........ 10
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5/2024—Rev. D to Rev. E

SPECIFICATIONS

ELECTRICAL CHARACTERISTICS—5 V PRIMARY INPUT SUPPLY/5 V SECONDARY ISOLATED SUPPLY

All typical specifications are at T_A = 25°C, V_{DD1} = V_{DD2} = V_{DDP} = 5 V, V_{SEL} resistor network: R1 = 10 kΩ, R2 = 30.9 kΩ between V_{ISO} and GND_{ISO}. Minimum/maximum specifications apply over the entire recommended operation range, which is 4.5 V ≤ V_{DD1}, V_{DD2}, V_{DDP} ≤ 5.5 V and −40°C ≤ T_A ≤ +105°C, unless otherwise noted. Switching specifications are tested with C_L = 15 pF and CMOS signal levels, unless otherwise noted.

Table 3. DC-to-DC Converter Static Specifications

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
DC-TO-DC CONVERTER SUPPLY						
Setpoint	V_{ISO}	4.675	5.0	5.325	V	I_{ISO} = 15 mA, R1 = 10 kΩ, R2 = 30.9 kΩ
Thermal Coefficient	$V_{ISO\ (TC)}$		−44		µV/°C	
Line Regulation	$V_{ISO\ (LINE)}$		20		mV/V	I_{ISO} = 15 mA, V_{DDP} = 4.5 V to 5.5 V
Load Regulation	$V_{ISO\ (LOAD)}$		1.3	3	%	I_{ISO} = 3 mA to 27 mA
Output Ripple	$V_{ISO\ (RIP)}$		75		mV p-p	20 MHz bandwidth, C_{BO} = 0.1 µF‖10 µF, I_{ISO} = 27 mA
Output Noise	$V_{ISO\ (NOISE)}$		200		mV p-p	C_{BO} = 0.1 µF‖10 µF, I_{ISO} = 27 mA
Switching Frequency	f_{OSC}		125		MHz	
Pulse-Width Modulation Frequency	f_{PWM}		600		kHz	
Output Supply	$I_{ISO\ (MAX)}$	30			mA	V_{ISO} > 4.675 V
Efficiency at $I_{ISO\ (MAX)}$		20	29	36	%	I_{ISO} = 27 mA
I_{DDP}, No V_{ISO} Load	$I_{DDP\ (Q)}$		6.8	12	mA	
I_{DDP}, Full V_{ISO} Load	$I_{DDP\ (MAX)}$	80	104	142	mA	
Thermal Shutdown						
Shutdown Temperature			154		°C	
Thermal Hysteresis			10		°C	

Table 4. Data Channel Supply Current

		1 Mbps—A, B, C Grades			25 Mbps—B, C Grades			100 Mbps—C Grade				
Parameter	Symbol	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Unit	Test Conditions/ Comments
SUPPLY CURRENT												
ADuM6210	I_{DD1}		1.1	1.6		6.2	7.0		20	25	mA	C_L = 0 pF
	I_{DD2}		2.7	4.5		4.8	7.0		9.5	15	mA	C_L = 0 pF
ADuM6211	I_{DD1}		2.1	2.7		4.9	6.5		15	19	mA	C_L = 0 pF
	I_{DD2}		2.3	2.9		4.7	6.5		15.6	19	mA	C_L = 0 pF
ADuM6212	I_{DD1}		2.7	4.5		4.8	7.0		9.5	15	mA	C_L = 0 pF
	I_{DD2}		1.1	1.6		6.2	7.0		20	25	mA	C_L = 0 pF

Table 5. Switching Specifications

		A Grade			B Grade			C Grade				
Parameter	Symbol	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Unit	Test Conditions/Comments
SWITCHING SPECIFICATIONS												
Data Rate				1			25			100	Mbps	Within PWD limit
Propagation Delay	t_{PHL}, t_{PLH}			50			35	20	23	29	ns	50% input to 50% output
Pulse Width Distortion	PWD			10			3			2	ns	$\lvert t_{PLH} - t_{PHL} \rvert$
Pulse Width	PW	1000			40			10			ns	Within PWD limit
Propagation Delay Skew	t_{PSK}			38			12			9	ns	Between any two units
Channel Matching												
Codirectional	t_{PSKCD}			5			3			2	ns	
Opposing Direction	t_{PSKOD}			10			6			5	ns	
Jitter			2			2			1		ns	

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Table 6. Input and Output Characteristics

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
DC SPECIFICATIONS						
Logic High Input Threshold	V_{IH}	0.7 V_{ISO}, 0.7 V_{DD1}			V	
Logic Low Input Threshold	V_{IL}			0.3 V_{ISO}, 0.3 V_{DD1}	V	
Logic High Output Voltages	V_{OH}	V_{DD1} − 0.1, V_{DD2} − 0.1	V_{DD1}, V_{DD2}		V	I_{Ox} = −20 µA, V_{Ix} = V_{IxH}
		V_{DD1} − 0.4, V_{DD2} − 0.4	V_{DD1} − 0.2, V_{DD2} − 0.2		V	I_{Ox} = −3.2 mA, V_{Ix} = V_{IxH}
Logic Low Output Voltages	V_{OL}		0.0	0.1	V	I_{Ox} = 20 µA, V_{Ix} = V_{IxL}
			0.2	0.4	V	I_{Ox} = 3.2 mA, V_{Ix} = V_{IxL}
Undervoltage Lockout						V_{DD1}, V_{DD2} ,V_{DDP} supply
Positive Going Threshold	V_{UV+}		2.75		V	
Negative Going Threshold	V_{UV-}		2.65		V	
Hysteresis	V_{UVH}		0.2		V	
Supply Current per Channel						
Quiescent Input Supply Current	$I_{DDI(Q)}$		0.54	0.8	mA	
Quiescent Output Supply Current	$I_{DDO(Q)}$		1.6	2.0	mA	
Dynamic Input Supply Current	$I_{DDI(D)}$		0.09		mA/Mbps	
Dynamic Output Supply Current	$I_{DDO(D)}$		0.04		mA/Mbps	
Input Currents per Channel	I_I	−10	+0.01	+10	µA	0 V ≤ V_{Ix} ≤ V_{DDx}
AC SPECIFICATIONS						
Output Rise/Fall Time	t_R/t_F		2.5		ns	10% to 90%
Common-Mode Transient Immunity[1]	|CM|	25	35		kV/µs	V_{Ix} = V_{DD1} or V_{ISO}, V_{CM} = 1000 V, transient magnitude = 800 V
Refresh Rate	t_r		1.6		µs	

[1] |CM| is the maximum common-mode voltage slew rate that can be sustained while maintaining V_{Ox} > 0.8 × V_{DD1} or 0.8 × V_{ISO} for a high input or V_{Ox} < 0.8 × V_{DD1} or 0.8 × V_{ISO} for a low input. The common-mode voltage slew rates apply to both rising and falling common-mode voltage edges.

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ELECTRICAL CHARACTERISTICS—3.3 V PRIMARY INPUT SUPPLY/3.3 V SECONDARY ISOLATED SUPPLY

All typical specifications are at T_A = 25°C, V_{DD1} = V_{DD2} = V_{DDP} = 3.3 V, V_{SEL} resistor network: R1 = 10 kΩ, R2 = 16.9 kΩ between V_{ISO} and GND_{ISO}. Minimum/maximum specifications apply over the entire recommended operation range, which is 3.135 V ≤ V_{DD1}, V_{DD2}, V_{DDP} ≤ 3.6 V, and −40°C ≤ T_A ≤ +105°C, unless otherwise noted. Switching specifications are tested with C_L = 15 pF and CMOS signal levels, unless otherwise noted.

The digital isolator channels and the power section work independently, and under the operating voltages in this section, there may not be sufficient current from the V_{ISO} to run both data channels at the maximum data rate. Verify that the application is within the power capability of V_{ISO} if that supply is providing power to V_{DD2}.

Table 7. DC-to-DC Converter Static Specifications

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
DC-TO-DC CONVERTER SUPPLY						
Setpoint	V_{ISO}	3.135	3.3	3.51	V	I_{ISO} = 10 mA, R1 = 10 kΩ, R2 = 16.9 kΩ
Thermal Coefficient	$V_{ISO (TC)}$		−26		μV/°C	I_{ISO} = 20 mA
Line Regulation	$V_{ISO (LINE)}$		20		mV/V	I_{ISO} = 10 mA, V_{DDP} = 3.135 V to 3.6 V
Load Regulation	$V_{ISO (LOAD)}$		1.3	3	%	I_{ISO} = 2 mA to 18 mA
Output Ripple	$V_{ISO (RIP)}$		50		mV p-p	20 MHz bandwidth, C_{BO} = 0.1 μF‖10 μF, I_{ISO} = 18 mA
Output Noise	$V_{ISO (NOISE)}$		130		mV p-p	C_{BO} = 0.1 μF‖10 μF, I_{ISO} = 18 mA
Switching Frequency	f_{OSC}		125		MHz	
Pulse-Width Modulation Frequency	f_{PWM}		600		kHz	
Output Supply	$I_{ISO (MAX)}$	20			mA	V_{ISO} > 3.135 V
Efficiency at $I_{ISO (MAX)}$		18	27	33	%	I_{ISO} = 18 mA
I_{DDP}, No V_{ISO} Load	$I_{DDP (Q)}$		3.3	10.5	mA	
I_{DDP}, Full V_{ISO} Load	$I_{DDP (MAX)}$	60	77	105	mA	
Thermal Shutdown						
Shutdown Temperature			154		°C	
Thermal Hysteresis			10		°C	

Table 8. Data Channel Supply Current

		1 Mbps—A, B, C Grades			25 Mbps—B, C Grades			100 Mbps—C Grade				
Parameter	Symbol	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Unit	Test Conditions/ Comments
SUPPLY CURRENT												
ADuM6210	I_{DD1}		0.75	1.4		5.1	9.0		17	23	mA	C_L = 0 pF
	I_{DD2}		2.0	3.5		2.7	4.6		4.8	9	mA	C_L = 0 pF
ADuM6211	I_{DD1}		1.6	2.1		3.8	5.0		11	15	mA	C_L = 0 pF
	I_{DD2}		1.7	2.3		3.9	6.2		11	15	mA	C_L = 0 pF
ADuM6212	I_{DD1}		2.0	3.5		2.7	4.6		4.8	9	mA	C_L = 0 pF
	I_{DD2}		0.75	1.4		5.1	9.0		17	23	mA	C_L = 0 pF

Table 9. Switching Specifications

		A Grade			B Grade			C Grade				
Parameter	Symbol	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Unit	Test Conditions/ Comments
SWITCHING SPECIFICATIONS												
Data Rate				1			25			100	Mbps	Within PWD limit
Propagation Delay	t_{PHL}, t_{PLH}			50			35	22	27	35	ns	50% input to 50% output
Pulse Width Distortion	PWD			10			3			2.5	ns	$\|t_{PLH} - t_{PHL}\|$
Pulse Width	PW	1000			40			10			ns	Within PWD limit
Propagation Delay Skew	t_{PSK}			38			16			12	ns	Between any two units

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Table 9. Switching Specifications (Continued)

Parameter	Symbol	A Grade			B Grade			C Grade			Unit	Test Conditions/ Comments
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max		
Channel Matching												
Codirectional	t_{PSKCD}			5			3			2.5	ns	
Opposing Direction	t_{PSKOD}			10			6			5	ns	
Jitter			2			2			1		ns	

Table 10. Input and Output Characteristics

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
DC SPECIFICATIONS						
Logic High Input Threshold	V_{IH}	0.7 V_{ISO}, 0.7 V_{DD1}			V	
Logic Low Input Threshold	V_{IL}			0.3 V_{ISO}, 0.3 V_{DD1}	V	
Logic High Output Voltages	V_{OH}	V_{DD1} − 0.1, V_{DD2} − 0.1	V_{DD1}, V_{DD2}		V	I_{Ox} = −20 μA, $V_{Ix} = V_{IxH}$
		V_{DD1} − 0.4, V_{DD2} − 0.4	V_{DD1} − 0.2, V_{DD2} − 0.2		V	I_{Ox} = −3.2 mA, $V_{Ix} = V_{IxH}$
Logic Low Output Voltages	V_{OL}		0.0	0.1	V	I_{Ox} = 20 μA, $V_{Ix} = V_{IxL}$
			0.2	0.4	V	I_{Ox} = 3.2 mA, $V_{Ix} = V_{IxL}$
Undervoltage Lockout						V_{DD1}, V_{DD2} ,V_{DDP} supply
Positive Going Threshold	V_{UV+}		2.75		V	
Negative Going Threshold	V_{UV-}		2.65		V	
Hysteresis	V_{UVH}		0.2		V	
Supply Current per Channel						
Quiescent Input Supply Current	$I_{DDI(Q)}$		0.4	0.6	mA	
Quiescent Output Supply Current	$I_{DDO(Q)}$		1.2	1.7	mA	
Dynamic Input Supply Current	$I_{DDI(D)}$		0.08		mA/Mbps	
Dynamic Output Supply Current	$I_{DDO(D)}$		0.015		mA/Mbps	
Input Currents per Channel	I_I	−10	+0.01	+10	μA	0 V ≤ V_{Ix} ≤ V_{DDx}
AC SPECIFICATIONS						
Output Rise/Fall Time	t_R/t_F		3		ns	10% to 90%
Common-Mode Transient Immunity[1]	|CM|	25	35		kV/μs	V_{Ix} = V_{DD1} or V_{ISO}, V_{CM} = 1000 V, transient magnitude = 800 V
Refresh Rate	t_r		1.6		μs	

1 |CM| is the maximum common-mode voltage slew rate that can be sustained while maintaining V_{Ox} > 0.8 × V_{DD1} or 0.8 × V_{ISO} for a high input or V_{Ox} < 0.8 × V_{DD1} or 0.8 × V_{ISO} for a low input. The common-mode voltage slew rates apply to both rising and falling common-mode voltage edges.

SPECIFICATIONS

ELECTRICAL CHARACTERISTICS—5 V PRIMARY INPUT SUPPLY/3.3 V SECONDARY ISOLATED SUPPLY

All typical specifications are at T_A = 25°C, V_{DD1} = V_{DDP} = 5 V, V_{DD2} = 3.3 V, V_{SEL} resistor network: R1 = 10 kΩ, R2 = 16.9 kΩ between V_{ISO} and GND_{ISO}. Minimum/maximum specifications apply over the entire recommended operation range, which is 4.5 V ≤ V_{DD1}, V_{DDP} ≤ 5.5 V, 3.135 V ≤ V_{DD2} ≤ 3.6 V, and −40°C ≤ T_A ≤ +105°C, unless otherwise noted. Switching specifications are tested with C_L = 15 pF and CMOS signal levels, unless otherwise noted.

Table 11. DC-to-DC Converter Static Specifications

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
DC-TO-DC CONVERTER SUPPLY						
Setpoint	V_{ISO}	3.135	3.3	3.51	V	I_{ISO} = 15 mA, R1 = 10 kΩ, R2 = 16.9 kΩ
Thermal Coefficient	$V_{ISO (TC)}$		−26		µV/°C	
Line Regulation	$V_{ISO (LINE)}$		20		mV/V	I_{ISO} = 15 mA, V_{DDP} = 4.5 V to 5.5 V
Load Regulation	$V_{ISO (LOAD)}$		1.3	3	%	I_{ISO} = 3 mA to 27 mA
Output Ripple	$V_{ISO (RIP)}$		50		mV p-p	20 MHz bandwidth, C_{BO} = 0.1 µF‖10 µF, I_{ISO} = 27 mA
Output Noise	$V_{ISO (NOISE)}$		130		mV p-p	C_{BO} = 0.1 µF‖10 µF, I_{ISO} = 27 mA
Switching Frequency	f_{OSC}		125		MHz	
Pulse-Width Modulation Frequency	f_{PWM}		600		kHz	
Output Supply	$I_{ISO (MAX)}$	30			mA	V_{ISO} > 3.135 V
Efficiency at $I_{ISO (MAX)}$		20	24	35	%	I_{ISO} = 27 mA
I_{DDP}, No V_{ISO} Load	$I_{DDP (Q)}$		3.2	8	mA	
I_{DDP}, Full V_{ISO} Load	$I_{DDP (MAX)}$	70	85	105	mA	
Thermal Shutdown						
Shutdown Temperature			154		°C	
Thermal Hysteresis			10		°C	

Table 12. Data Channel Supply Current

Parameter	Symbol	1 Mbps—A, B, C Grades			25 Mbps—B, C Grades			100 Mbps—C Grade			Unit	Test Conditions/ Comments
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max		
SUPPLY CURRENT												
ADuM6210	I_{DD1}		1.1	1.6		6.2	7.0		20	25	mA	C_L = 0 pF
	I_{DD2}		2.0	3.5		2.7	4.6		4.8	9.0	mA	C_L = 0 pF
ADuM6211	I_{DD1}		2.1	2.7		4.9	6.5		15	19	mA	C_L = 0 pF
	I_{DD2}		1.7	2.3		3.9	6.2		11	15	mA	C_L = 0 pF
ADuM6212	I_{DD1}		2.0	3.5		2.7	4.6		4.8	9.0	mA	C_L = 0 pF
	I_{DD2}		1.1	1.6		6.2	7.0		20	25	mA	C_L = 0 pF

Table 13. Switching Specifications

Parameter	Symbol	A Grade			B Grade			C Grade			Unit	Test Conditions/ Comments
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max		
SWITCHING SPECIFICATIONS												
Data Rate				1			25			100	Mbps	Within PWD limit
Propagation Delay	t_{PHL}, t_{PLH}			50			35	20	25	31	ns	50% input to 50% output
Pulse Width Distortion	PWD			10			3			2.5	ns	$\lvert t_{PLH} - t_{PHL}\rvert$
Pulse Width	PW	1000			40			10			ns	Within PWD limit
Propagation Delay Skew	t_{PSK}			38			16			12	ns	Between any two units
Channel Matching												
Codirectional	t_{PSKCD}			5			3			2	ns	
Opposing Direction	t_{PSKOD}			10			6			5	ns	
Jitter			2			2			1		ns	

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Table 14. Input and Output Characteristics

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
DC SPECIFICATIONS						
Logic High Input Threshold	V_{IH}	0.7 V_{ISO}, 0.7 V_{DD1}			V	
Logic Low Input Threshold	V_{IL}			0.3 V_{ISO}, 0.3 V_{DD1}	V	
Logic High Output Voltages	V_{OH}	V_{DD1} − 0.1, V_{DD2} − 0.1	V_{DD1}, V_{DD2}		V	I_{Ox} = −20 µA, V_{Ix} = V_{IxH}
		V_{DD1} − 0.4, V_{DD2} − 0.4	V_{DD1} − 0.2, V_{DD2} − 0.2		V	I_{Ox} = −3.2 mA, V_{Ix} = V_{IxH}
Logic Low Output Voltages	V_{OL}		0.0	0.1	V	I_{Ox} = 20 µA, V_{Ix} = V_{IxL}
			0.2	0.4	V	I_{Ox} = 3.2 mA, V_{Ix} = V_{IxL}
Undervoltage Lockout						V_{DD1}, V_{DD2} ,V_{DDP} supply
Positive Going Threshold	V_{UV+}		2.75		V	
Negative Going Threshold	V_{UV-}		2.65		V	
Hysteresis	V_{UVH}		0.2		V	
Supply Current per Channel						
Quiescent Input Supply Current	$I_{DDI(Q)}$		0.54	0.75	mA	
Quiescent Output Supply Current	$I_{DDO(Q)}$		1.2	2.0	mA	
Dynamic Input Supply Current	$I_{DDI(D)}$		0.09		mA/Mbps	
Dynamic Output Supply Current	$I_{DDO(D)}$		0.02		mA/Mbps	
Input Currents per Channel	I_I	−10	+0.01	+10	µA	0 V ≤ V_{Ix} ≤ V_{DDx}
AC SPECIFICATIONS						
Output Rise/Fall Time	t_R/t_F		2.5		ns	10% to 90%
Common-Mode Transient Immunity[1]	|CM|	25	35		kV/µs	V_{Ix} = V_{DD1} or V_{ISO}, V_{CM} = 1000 V, transient magnitude = 800 V
Refresh Rate	t_r		1.6		µs	

[1] |CM| is the maximum common-mode voltage slew rate that can be sustained while maintaining V_{Ox} > 0.8 × V_{DD1} or 0.8 × V_{ISO} for a high input or V_{Ox} < 0.8 × V_{DD1} or 0.8 × V_{ISO} for a low input. The common-mode voltage slew rates apply to both rising and falling common-mode voltage edges.

REGULATORY APPROVALS

The ADuM6210/ADuM6211/ADuM6212 certification approvals are listed in Table 15. Copies of the relevant certifications are available at Safety and Regulatory Certification for Digital Isolators.

Table 15. RS-20 [20-Lead Shrink Small Outline Package]

UL	CSA[1]	VDE
UL 1577 Component Recognition Program	IEC/CSA 62368-1	DIN EN IEC 60747-17 (VDE 0884-17)
Single Protection at 3750 V rms	Basic insulation at 530 V rms	Reinforced insulation at 600 V peak
	Reinforced insulation at 265 V rms	
	IEC/CSA 61010-1	
	Basic insulation at 300 V rms	
	Reinforced insulation, 150 V rms	
File E214100	File No. 205078	Certificate No. 40051926

[1] Working voltages are quopted for Pollution Degree 2, Material Group 3 and Overvoltage Category 2 except where otherwise specified. The ADuM6210/ADuM6211/AD-uM6212 case material has been evaluated as Material Group I.

SPECIFICATIONS

INSULATION SPECIFICATIONS

The ADuM6210/ADuM6211/ADuM6212 are only suitable for "safe electrical insulation" only within the safety limiting ratings. Compliance with the safety limiting ratings shall be ensured by means of suitable protective circuits.

Table 16. RS-20 [20-Lead SSOP] Package

Description	Symbol	Characteristic	Unit	Test Conditions/Comments
GENERAL				
Minimum External Clearance Distance	CLR	5.3	mm	Measured from input terminals to output terminals, shortest distance through air per IEC 60664-1
Minimum External Creepage Distance	CRP	5.3	mm	Measured from input terminals to output terminals, shortest distance along body per IEC 60664-1
Distance Through Insulation	DTI	18	μm	Minimum internal
Comparative Tracking Index	CTI	>600	V	Per IEC 60112
Material Group		I		
Overvoltage Category per IEC 60664-1				
		I to IV		For Rated Mains Voltage ≤ 150 V rms
		I to IV		For Rated Mains Voltage ≤ 300 V rms
		I to III		For Rated Mains Voltage ≤ 400 V rms
SAFETY LIMITING VALUES				
Maximum Ambient Safety Temperature	T_S	150	°C	
Maximum Junction Temperature, Safety	$T_{JMAX,S}$	150	°C	Maximum junction temperature for isolation barrier safety
Maximum Total Power Dissipation	P_{TOT}	2.5	W	$T_A \leq 25°C$, $P_{TOT} = P_{SI} = P_{SO}$
Derating above Ambient		20	mW/°C	
Junction-to-Air Thermal Impedance	θ_{JA}	50	°C/W	See Thermal Analysis
IEC 60747-17 (REINFORCED RATING)				
Maximum Repetitive Peak Isolation Voltage	V_{IORM}	600	V peak	AC voltage, end of life test, f = 60 Hz
Maximum Isolation Working Voltage	V_{IOWM}	424	V rms	DC Voltage
		600	V peak	
Maximum Transient Isolation Voltage	V_{IOTM}	5300	V peak	$V_{TEST} = 1.2 \times V_{IOTM}$, t = 1 sec (100% production)
Maximum Impulse Voltage	V_{IMP}	5300	V peak	Surge voltage in air, waveform per IEC 61000-4-5
Maximum Surge Isolation Voltage	V_{IOSM}	10,000	V peak	$V_{TEST} \geq 1.3 \times V_{IMP}$ (sample test), tested in oil, waveform per IEC 61000-4-5
Apparent Charge	q_{pd}	≤5	pC	Method a (sample test), $V_{ini} = V_{IOTM}$, t_{ini} = 60 s, $V_{pd(m)} = 1.6 \times V_{IORM}$, t_m = 10s Method b1 (100% production), $V_{ini} = 1.2 \times V_{IOTM}$, t_{ini} = 1 s, $V_{pd(m)} = 1.875 \times V_{IORM}$, t_m = 1 s
Resistance (Input to Output)[1]	R_{IO}	10^{12}	Ω	T_A = 25°C, V_{TEST} = 500 V dc, t = 60 s
	R_{IO-S}	$>10^9$	Ω	$T_A = T_S$, V_{TEST} = 500 V dc, t = 60 s
Capacitance (Input to Output)[1]	C_{IO}	2.2	pF	f_{TEST} = 1MHz
Climate Category		40/125/21		
Pollution Degree		2		Per IEC 60664-1
UL 1577				
Maximum Withstanding Isolation Voltage	V_{ISO}	3750	V rms	$V_{TEST} = 1.2 \times V_{ISO}$

[1] Device measured as a 2-terminal device with Pin 1 and Pin 10 connected to Pin 11 and Pin 20.

SPECIFICATIONS

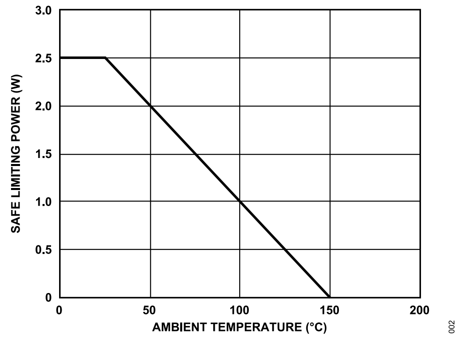

Figure 2. Thermal Derating Curve, Dependence of Safety Limiting Values on Case Temperature, per DIN EN IEC 60747-17 (VDE 0884-17)

SPECIFICATIONS

RECOMMENDED OPERATING CONDITIONS

Table 17.

Parameter	Symbol	Min	Max	Unit
Operating Temperature[1]	T_A	−40	+105	°C
Supply Voltages[2]				
V_{DDP} at V_{ISO} = 3.135 V to 3.6 V	V_{DDP}	3.135	5.5	V
V_{DDP} at V_{ISO} = 4.5 V to 5.5 V		4.5	5.5	V
V_{DD1}, V_{DD2}	V_{DD1}, V_{DD2}	3.135	5.5	V

1 Operation at 105°C requires reduction of the maximum load current as specified in Table 18.

2 Each voltage is relative to its respective ground.

ABSOLUTE MAXIMUM RATINGS

Ambient temperature = 25°C, unless otherwise noted.

Table 18. Absolute Maximum Ratings

Parameter	Rating
Storage Temperature Range (T_{ST})	−55°C to +150°C
Ambient Operating Temperature Range (T_A)	−40°C to +105°C
Supply Voltages (V_{DDP}, V_{DD1}, V_{DD2}, V_{ISO})[1]	−0.5 V to +7.0 V
V_{ISO} Supply Current[2]	
T_A = −40°C to +105°C	30 mA
Input Voltage (V_{IA}, V_{IB}, PDIS, V_{SEL})[1, 3]	−0.5 V to V_{DDI} + 0.5 V
Output Voltage (V_{OA}, V_{OB})[1, 3]	−0.5 V to V_{DDO} + 0.5 V
Average Output Current Per Data Output Pin[4]	−10 mA to +10 mA
Common-Mode Transients[5]	−100 kV/µs to +100 kV/µs

1 All voltages are relative to their respective ground.

2 The V_{ISO} provides current for dc and dynamic loads on the V_{ISO} I/O channels. This current must be included when determining the total V_{ISO} supply current. For ambient temperatures between 85°C and 105°C, maximum allowed current is reduced.

3 V_{DDI} and V_{DDO} refer to the supply voltages on the input and output sides of a given channel, respectively. See the PCB Layout section.

4 See Figure 2 for the maximum rated current values for various temperatures.

5 Refers to common-mode transients across the insulation barrier. Common-mode transients exceeding the absolute maximum ratings may cause latch-up or permanent damage.

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS

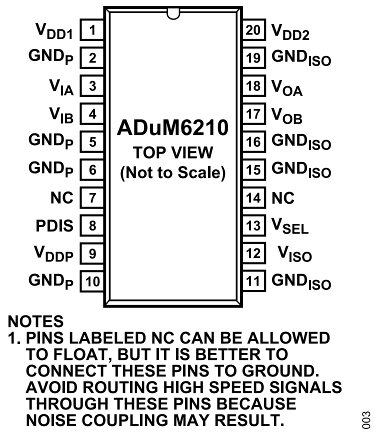

Figure 3. ADuM6210 Pin Configuration

Table 19. ADuM6210 Pin Function Descriptions

Pin No.	Mnemonic	Description
1	V_{DD1}	Power Supply for the Side 1 Logic Circuits of the Device. It is independent of V_{DDP} and can operate between 3.135 V and 5.5 V.
2, 5, 6, 10	GND_P	Ground Reference for Isolator Side 1. All of these pins are internally connected, and it is recommended that all GND_P pins be connected to a common ground.
3	V_{IA}	Logic Input A.
4	V_{IB}	Logic Input B.
7, 14	NC	No Connect. Pins labeled NC can be allowed to float, but it is better to connect these pins to ground. Avoid routing high speed signals through these pins because noise coupling may result.
8	PDIS	Power Disable. When this pin is tied to a logic low, the power converter is active; when tied to a logic high, the power supply enters a low power standby mode.
9	V_{DDP}	Primary *iso*Power Supply Voltage, 3.135 V V to 5.5 V.
11, 15, 16, 19	GND_{ISO}	Ground Reference for Isolator Side 2. All of these pins are internally connected, and it is recommended that all GND_{ISO} pins be connected to a common ground.
12	V_{ISO}	Secondary Supply Voltage Output for External Loads, 3.3 V (V_{SEL} Low) or 5.0 V (V_{SEL} High).
13	V_{SEL}	Output Voltage Select. Provide a thermally matched resistor network between V_{ISO} and GND_{ISO} to divide the required output voltage to match the 1.25 V reference voltage. V_{ISO} voltage can be programmed up to 20% higher or 75% lower than V_{DDP} but must be within the allowed output voltage range.
17	V_{OB}	Logic Output B.
18	V_{OA}	Logic Output A.
20	V_{DD2}	Power Supply for the Side 2 Logic Circuits of the Device. It is independent of V_{ISO} and can operate between 3.135 V and 5.5 V.

PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS

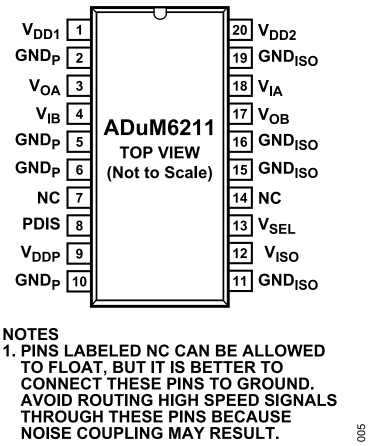

Figure 4. ADuM6211 Pin Configuration

Table 20. ADuM6211 Pin Function Descriptions

Pin No.	Mnemonic	Description
1	V_{DD1}	Power Supply for the Side 1 Logic Circuits of the Device. It is independent of V_{DDP} and can operate between 3.135 V and 5.5 V.
2, 5, 6, 10	GND_P	Ground Reference for Isolator Side 1. All of these pins are internally connected, and it is recommended that all GND_P pins be connected to a common ground.
3	V_{OA}	Logic Output A.
4	V_{IB}	Logic Input B.
7, 14	NC	No Connect. Pins labeled NC can be allowed to float, but it is better to connect these pins to ground. Avoid routing high speed signals through these pins because noise coupling may result.
8	PDIS	Power Disable. When this pin is tied to a logic low, the power converter is active; when tied to a logic high, the power supply enters a low power standby mode.
9	V_{DDP}	Primary *iso*Power Supply Voltage, 3.135 V to 5.5 V.
11, 15, 16, 19	GND_{ISO}	Ground Reference for Isolator Side 2. All of these pins are internally connected, and it is recommended that all GND_{ISO} pins be connected to a common ground.
12	V_{ISO}	Secondary Supply Voltage Output for External Loads, 3.3 V (V_{SEL} Low) or 5.0 V (V_{SEL} High).
13	V_{SEL}	Output Voltage Select. Provide a thermally matched resistor network between V_{ISO} and GND_{ISO} to divide the required output voltage to match the 1.25 V reference voltage. V_{ISO} voltage can be programmed up to 20% higher or 75% lower than V_{DDP} but must be within the allowed output voltage range.
17	V_{OB}	Logic Output B.
18	V_{IA}	Logic Input A.
20	V_{DD2}	Power Supply for the Side 2 Logic Circuits of the Device. It is independent of V_{ISO} and can operate between 3.135 V and 5.5 V.

PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS

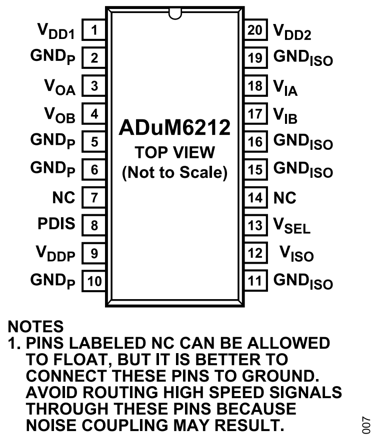

Figure 5. ADuM6212 Pin Configuration

Table 21. ADuM6212 Pin Function Descriptions

Pin No.	Mnemonic	Description
1	V_{DD1}	Power Supply for the Side 1 Logic Circuits of the Device. It is independent of V_{DDP} and can operate between 3.135 V and 5.5 V.
2, 5, 6, 10	GND_P	Ground Reference for Isolator Side 1. All of these pins are internally connected, and it is recommended that all GND_P pins be connected to a common ground.
3	V_{OA}	Logic Output A.
4	V_{OB}	Logic Output B.
7, 14	NC	No Connect. Pins labeled NC can be allowed to float, but it is better to connect these pins to ground. Avoid routing high speed signals through these pins because noise coupling may result.
8	PDIS	Power Disable. When this pin is tied to a logic low, the power converter is active; when tied to a logic high, the power supply enters a low power standby mode.
9	V_{DDP}	Primary *iso*Power Supply Voltage, 3.135 V to 5.5 V.
11, 15, 16,19	GND_{ISO}	Ground Reference for Isolator Side 2. All of these pins are internally connected, and it is recommended that all GND_{ISO} pins be connected to a common ground.
12	V_{ISO}	Secondary Supply Voltage Output for External Loads, 3.3 V (V_{SEL} Low) or 5.0 V (V_{SEL} High).
13	V_{SEL}	Output Voltage Select. Provide a thermally matched resistor network between V_{ISO} and GND_{ISO} to divide the required output voltage to match the 1.25 V reference voltage. V_{ISO} voltage can be programmed up to 20% higher or 75% lower than V_{DDP} but must be within the allowed output voltage range.
17	V_{IB}	Logic Input B.
18	V_{IA}	Logic Input A.
20	V_{DD2}	Power Supply for the Side 2 Logic Circuits of the Device. It is independent of V_{ISO} and can operate between 3.135 V and 5.5 V.

PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS

TRUTH TABLES

Table 22. Power Section Truth Table (Positive Logic)

V_{DDP} (V)	V_{SEL} Input	PDIS Input	V_{ISO} Output (V)	Notes
5	R1 = 10 kΩ, R2 = 30.9 kΩ	Low	5	
5	R1 = 10 kΩ, R2 = 30.9 kΩ	High	0	
3.3	R1 = 10 kΩ, R2 = 16.9 kΩ	Low	3.3	
3.3	R1 = 10 kΩ, R2 = 16.9 kΩ	High	0	
5	R1 = 10 kΩ, R2 = 30.9 kΩ	Low	3.3	
5	R1 = 10 kΩ, R2 = 30.9 kΩ	High	0	
3.3	R1 = 10 kΩ, R2 = 16.9 kΩ	Low	5	Configuration not recommended
3.3	R1 = 10 kΩ, R2 = 16.9 kΩ	High	0	

Table 23. Data Section Truth Table (Positive Logic)

V_{DDI} State[1]	V_{Ix} Input[1]	V_{DDO} State[1]	V_{Ox} Output[1]	Notes
Powered	High	Powered	High	Normal operation, data is high
Powered	Low	Powered	Low	Normal operation, data is low
X[2]	X[2]	Unpowered	Z[3]	Output is off
Unpowered	Low	Powered	Low	Output default low
Unpowered	High	Powered	Indeterminate	If a high level is applied to an input when no supply is present, it can parasitically power the input side, causing unpredictable operation

1 The references to I and O in this table refer to the input side and output side of a given data path and the associated power supply.

2 X = don't care.

3 Z = high impedance state.

TYPICAL PERFORMANCE CHARACTERISTICS

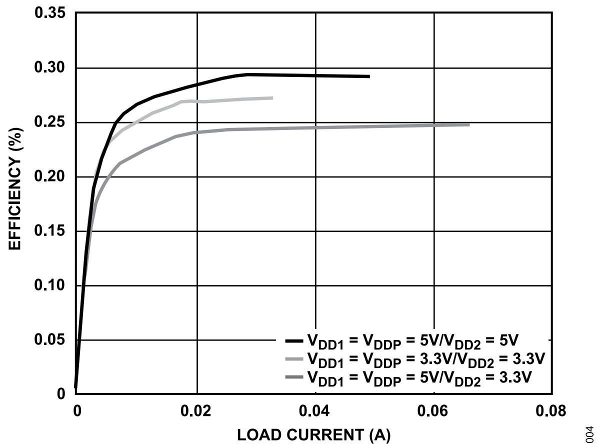

Figure 6. Typical Power Supply Efficiency at 5 V/5 V, 3.3 V/3.3 V, and 5 V/3.3 V

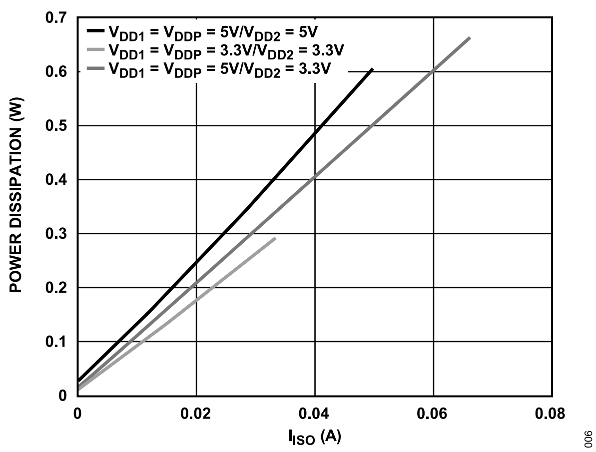

Figure 7. Typical Total Power Dissipation vs. I_{ISO}

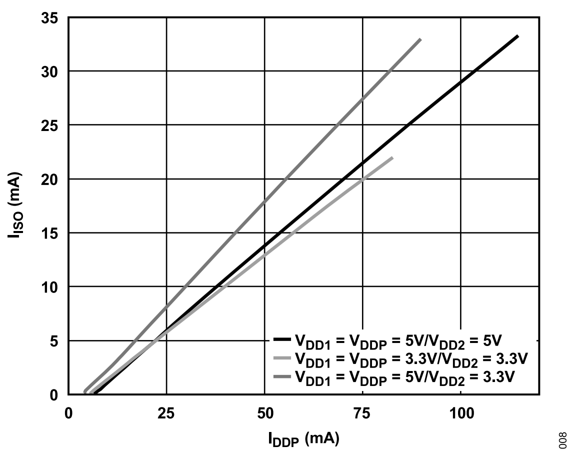

Figure 8. Typical Isolated Output Supply Current, I_{ISO}, as a Function of External Load at 5 V/5 V, 3.3 V/3.3 V, and 5 V/3.3 V

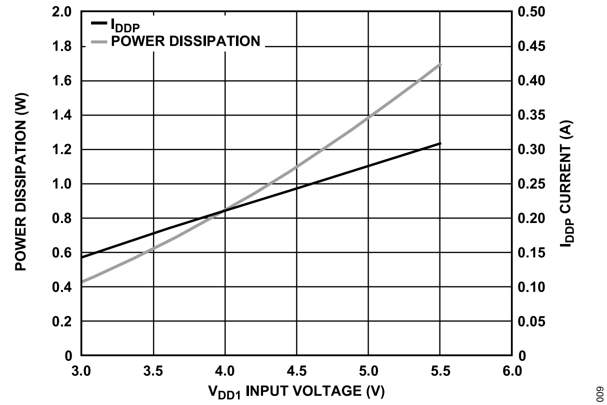

Figure 9. Typical Short-Circuit Input Current and Power Dissipation vs. V_{DD1} Supply Voltage

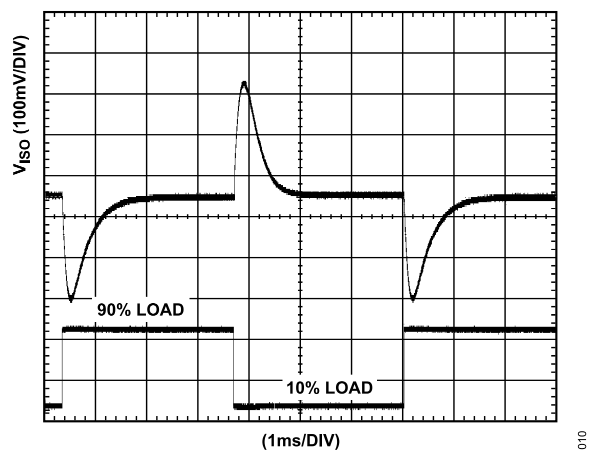

Figure 10. Typical V_{ISO} Transient Load Response, 5 V Output, 10% to 90% Load Step

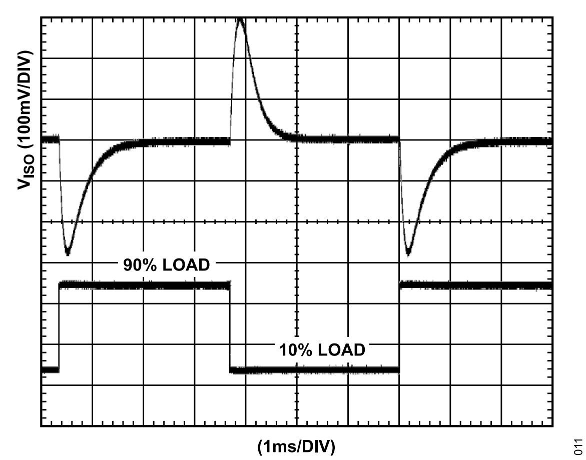

Figure 11. Typical Transient Load Response, 3 V Output, 10% to 90% Load Step

TYPICAL PERFORMANCE CHARACTERISTICS

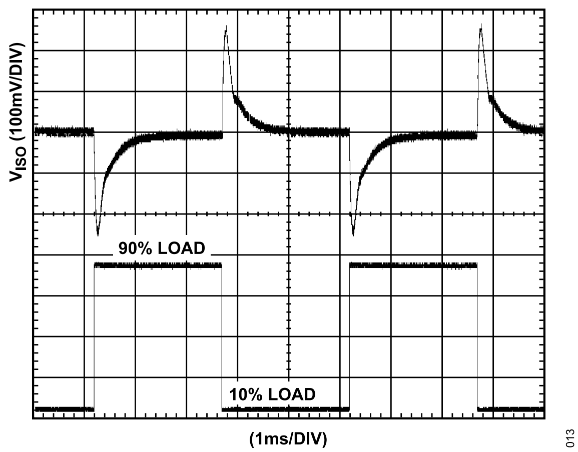

Figure 12. Typical Transient Load Response, 5 V Input, 3.3 V Output, 10% to 90% Load Step

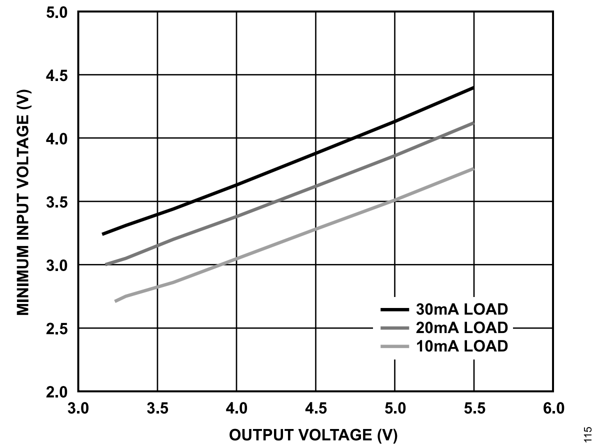

Figure 15. Relationship Between Output Voltage and Required Input Voltage, Under Load, to Maintain >80% Duty Factor in the PWM

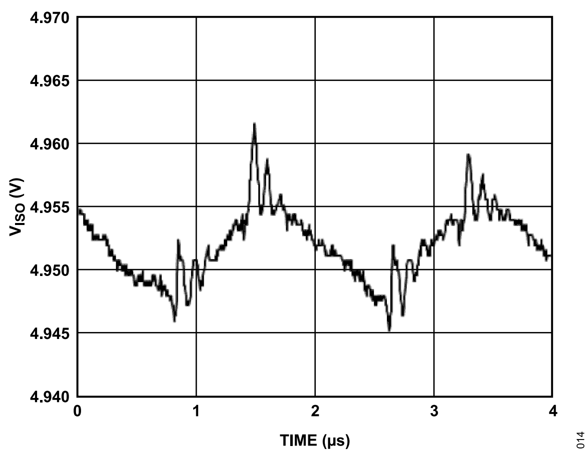

Figure 13. Typical V_{ISO} = 5 V Output Voltage Ripple at 90% Load

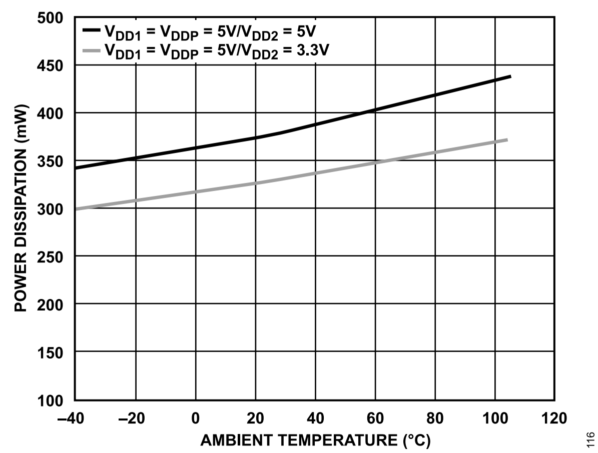

Figure 16. Power Dissipation with a 30 mA Load vs. Temperature

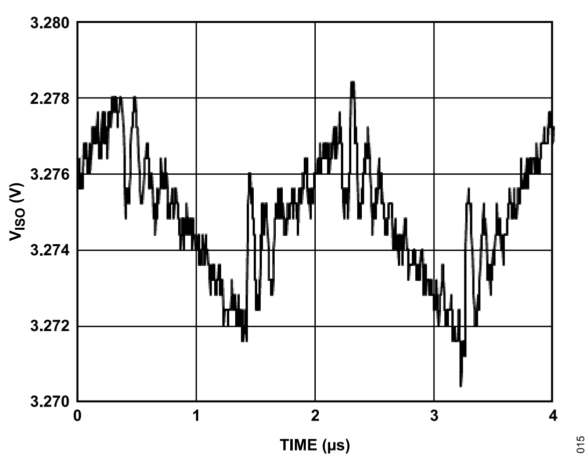

Figure 14. Typical V_{ISO} = 3.3 V Output Voltage Ripple at 90% Load

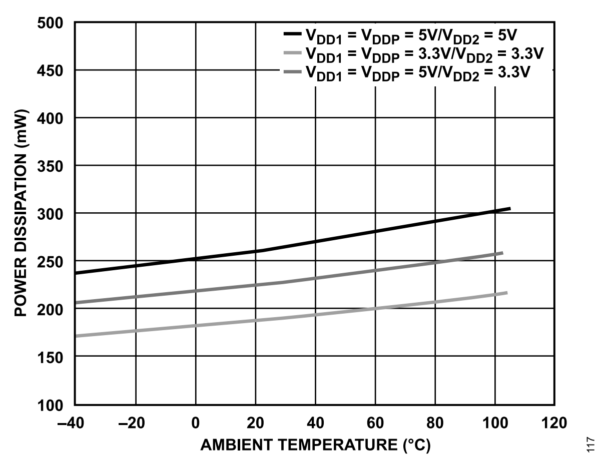

Figure 17. Power Dissipation with a 20 mA Load vs. Temperature

TYPICAL PERFORMANCE CHARACTERISTICS

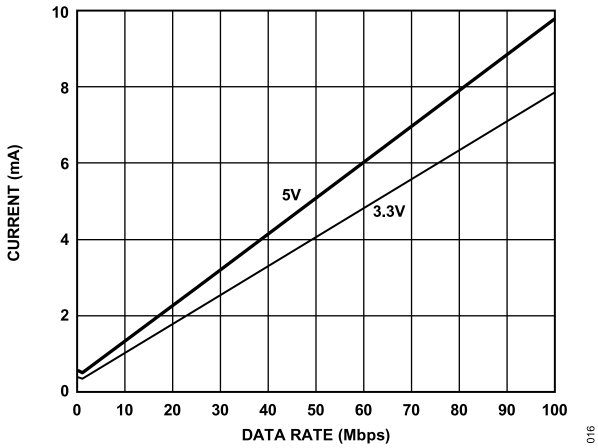

Figure 18. Typical Supply Current per Input Channel vs. Data Rate for 5 V and 3.3 V Operation (No Output Load)

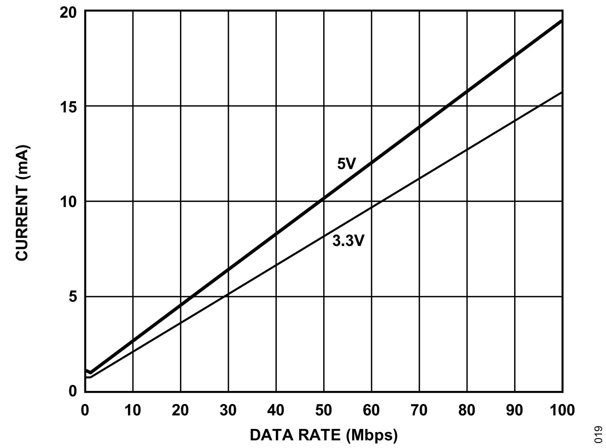

Figure 21. Typical ADuM6210 V_{DD1} or ADuM6212 V_{DD2} Supply Current vs. Data Rate for 5 V and 3.3 V Operation

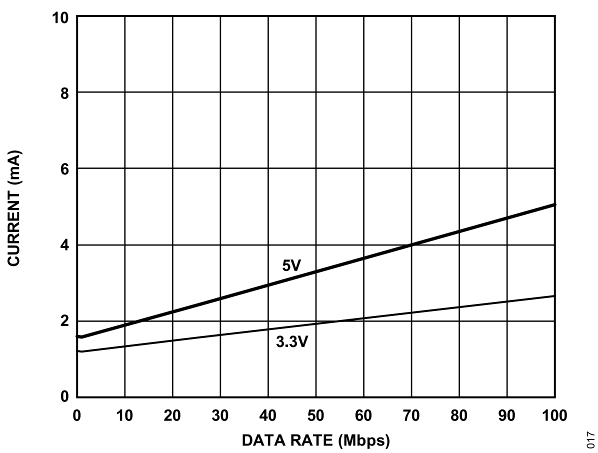

Figure 19. Typical Supply Current per Output Channel vs. Data Rate for 5 V and 3.3 V Operation (No Output Load)

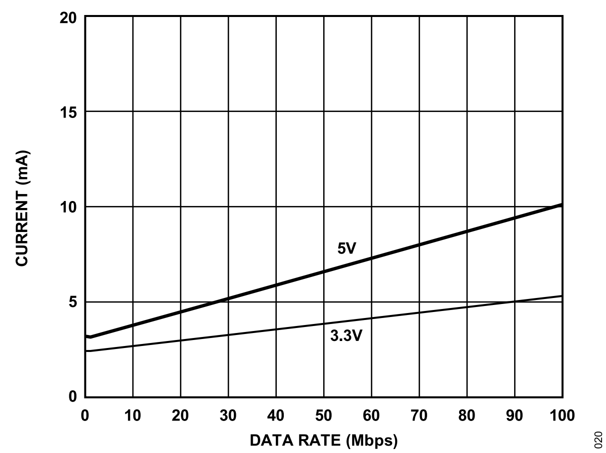

Figure 22. Typical ADuM6210 V_{DD2} or ADuM6212 V_{DD2} Supply Current vs. Data Rate for 5 V and 3.3 V Operation

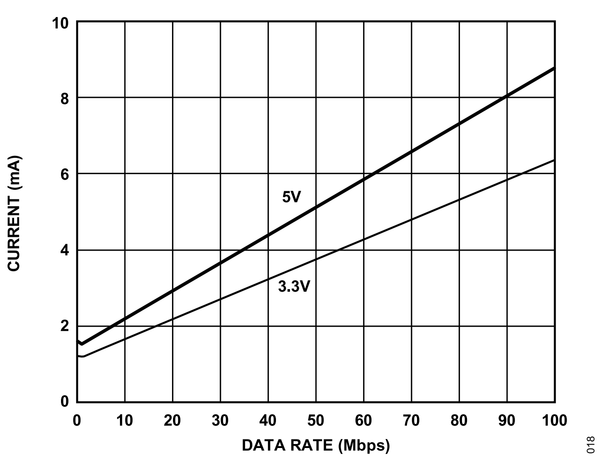

Figure 20. Typical Supply Current per Output Channel vs. Data Rate for 5 V and 3.3 V Operation (15 pF Output Load)

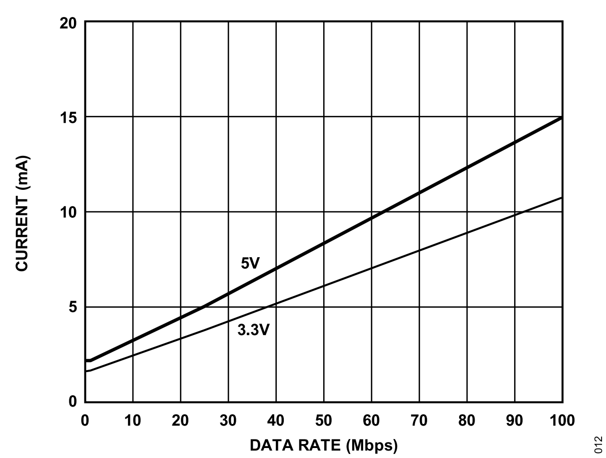

Figure 23. Typical ADuM6211 V_{DD1} or V_{DD2} Supply Current vs. Data Rate for 5 V and 3.3 V Operation

APPLICATIONS INFORMATION

The dc-to-dc converter section of the ADuM6210/ADuM6211/ADuM6212 works on principles that are common to most modern power supplies. It has a split controller architecture with isolated pulse-width modulation (PWM) feedback. V_{DDP} power is supplied to an oscillating circuit that switches current into a chip-scale air core transformer. Power transferred to the secondary side is rectified and regulated to a value between 3.135 V and 5.25 V, depending on the setpoint supplied by an external voltage divider (see Equation 1). The secondary (V_{ISO}) side controller regulates the output by creating a PWM control signal that is sent to the primary (V_{DDP}) side by a dedicated *i*Coupler data channel. The PWM modulates the oscillator circuit to control the power being sent to the secondary side. Feedback allows for significantly higher power and efficiency.

$$V_{ISO} = 1.25\ \text{V}\frac{(R1 + R2)}{R1} \quad (1)$$

where:
R1 is a resistor between V_{SEL} and GND_{ISO}.
R2 is a resistor between V_{SEL} and V_{ISO}.

Because the output voltage can be adjusted continuously, there are an infinite number of operating conditions. This data sheet addresses three discrete operating conditions in the Specifications tables. Many other combinations of input and output voltage are possible; Figure 15 depicts the supported voltage combinations at room temperature. Figure 15 was generated by fixing the V_{ISO} load and decreasing the input voltage until the PWM was at 80% duty cycle. Each of the curves represents the minimum input voltage that is required for operation under this criterion. For example, if the application requires 30 mA of output current at 5 V, the minimum input voltage at V_{DDP} is 4.25 V. Figure 15 also illustrates why the V_{DDP} = 3.3 V input and V_{ISO} = 5 V configuration is not recommended. Even at 10 mA of output current, the PWM cannot maintain less than 80% duty factor, leaving no margin to support load or temperature variations.

Typically, the ADuM6210/ADuM6211/ADuM6212 dissipates about 17% more power between room temperature and maximum temperature; therefore, the 20% PWM margin covers temperature variations.

The ADuM6210/ADuM6211/ADuM6212 implement undervoltage lockout (UVLO) with hysteresis on the primary and secondary side I/O pins as well as the V_{DDP} power input. This feature ensures that the converter does not go into oscillation due to noisy input power or slow power-on ramp rates.

PCB LAYOUT

The ADuM6210/ADuM6211/ADuM6212 digital isolators with 0.15 W *iso*Power integrated dc-to-dc converters require no external interface circuitry for the logic interfaces. Power supply bypassing with a low ESR capacitor is required, as close to the chip pads as possible. The *iso*Power inputs require several passive components to bypass the power effectively as well as set the output voltage and bypass the core voltage regulator (see Figure 24 through Figure 26).

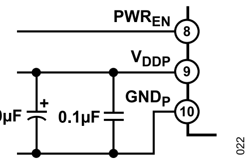

Figure 24. V_{DDP} Bias and Bypass Components

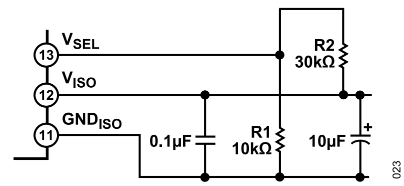

Figure 25. V_{ISO} Bias and Bypass Components

The power supply section of the ADuM6210/ADuM6211/ADuM6212 uses a 125 MHz oscillator frequency to efficiently pass power through its chip-scale transformers. Bypass capacitors are required for several operating frequencies. Noise suppression requires a low inductance, high frequency capacitor; ripple suppression and proper regulation require a large value bulk capacitor. These capacitors are most conveniently connected between Pin 9 and Pin 10 for V_{DDP} and between Pin 11 and Pin 12 for V_{ISO}. To suppress noise and reduce ripple, a parallel combination of at least two capacitors is required. The recommended capacitor values are 0.1 µF and 10 µF for V_{DD1}. The smaller capacitor must have a low ESR; for example, use of an NPO or X5R ceramic capacitor is advised. Ceramic capacitors are also recommended for the 10 µF bulk capacitance. An additional 10 nF capacitor can be added in parallel if further EMI reduction is required.

Note that the total lead length between the ends of the low ESR capacitor and the input power supply pin must not exceed 2 mm.

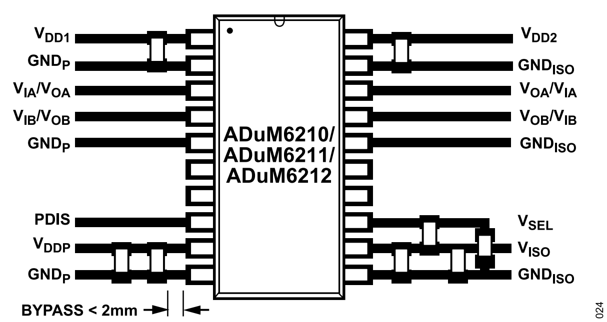

Figure 26. Recommended PCB Layout

In applications involving high common-mode transients, ensure that board coupling across the isolation barrier is minimized. Furthermore, design the board layout such that any coupling that does occur equally affects all pins on a given component side. Failure to ensure this can cause voltage differentials between pins, exceed-

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ing the absolute maximum ratings specified in Table 18, thereby leading to latch-up and/or permanent damage.

THERMAL ANALYSIS

The ADuM6210/ADuM6211/ADuM6212 consist of four internal die attached to a split lead frame with two die attach paddles. For the purposes of thermal analysis, the chip is treated as a thermal unit, with the highest junction temperature reflected in the θ_{JA} from Insulation Specifications. The value of θ_{JA} is based on measurements taken with the devices mounted on a JEDEC standard, 4-layer board with fine width traces and still air. Under normal operating conditions, the ADuM6210/ADuM6211/ADuM6212 can operate at full load across the full temperature range without derating the output current.

PROPAGATION DELAY PARAMETERS

Propagation delay is a parameter that describes the time it takes a logic signal to propagate through a component (see Figure 27). The propagation delay to a logic low output may differ from the propagation delay to a logic high.

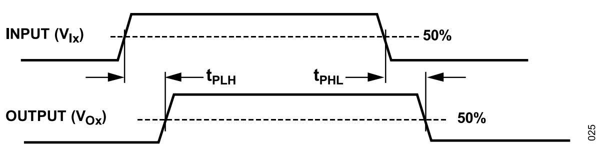

Figure 27. Propagation Delay Parameters

Pulse width distortion is the maximum difference between these two propagation delay values and is an indication of how accurately the input signal timing is preserved.

Channel-to-channel matching refers to the maximum amount the propagation delay differs between channels within a single ADuM6210/ADuM6211/ADuM6212 component.

Propagation delay skew refers to the maximum amount the propagation delay differs between multiple ADuM6210/ADuM6211/ADuM6212 devices operating under the same conditions.

EMI CONSIDERATIONS

The dc-to-dc converter section of the ADuM6210/ADuM6211/ADuM6212 components must, of necessity, operate at a very high frequency to allow efficient power transfer through the small transformers. This creates high frequency currents that can propagate in circuit board ground and power planes, causing edge and dipole radiation. Grounded enclosures are recommended for applications that use these devices. If grounded enclosures are not possible, follow good RF design practices in the layout of the PCB. See the AN-0971 Application Note for the most current PCB layout recommendations for the ADuM6210/ADuM6211/ADuM6212.

DC CORRECTNESS AND MAGNETIC FIELD IMMUNITY

Positive and negative logic transitions at the isolator input cause narrow (~1 ns) pulses to be sent to the decoder via the transformer. The decoder is bistable and is, therefore, either set or reset by the pulses, indicating input logic transitions. In the absence of logic transitions at the input for more than 1.6 µs, periodic sets of refresh pulses that are indicative of the correct input state are sent to ensure dc correctness at the output. If the decoder receives no internal pulses of more than approximately 6.4 µs, the input side is assumed to be unpowered or nonfunctional, in which case, the isolator output is forced to a default low state by the watchdog timer circuit. This situation should occur in the ADuM6210/ADuM6211/ADuM6212 only during power-up and power-down operations.

The limitation on the ADuM6210/ADuM6211/ADuM6212 magnetic field immunity is set by the condition in which induced voltage in the transformer receiving coil is sufficiently large to either falsely set or reset the decoder. The following analysis defines the conditions under which this can occur. The 3.3 V operating condition of the ADuM6210/ADuM6211/ADuM6212 is examined because it represents the most susceptible mode of operation.

The pulses at the transformer output have an amplitude of >1.5 V. The decoder has a sensing threshold of about 0.5 V, thus establishing a 0.5 V margin in which induced voltages can be tolerated. The voltage induced across the receiving coil is given by

$$V = (-d\beta/dt)\sum \pi r_n^2;\ n = 1, 2, \ldots, N \qquad (2)$$

where:
β is the magnetic flux density (gauss).
r_n is the radius of the n^{th} turn in the receiving coil (cm).
N is the number of turns in the receiving coil.

Given the geometry of the receiving coil in the ADuM6210/ADuM6211/ADuM6212 and an imposed requirement that the induced voltage be, at most, 50% of the 0.5 V margin at the decoder, a maximum allowable magnetic field is calculated as shown in Figure 28.

APPLICATIONS INFORMATION

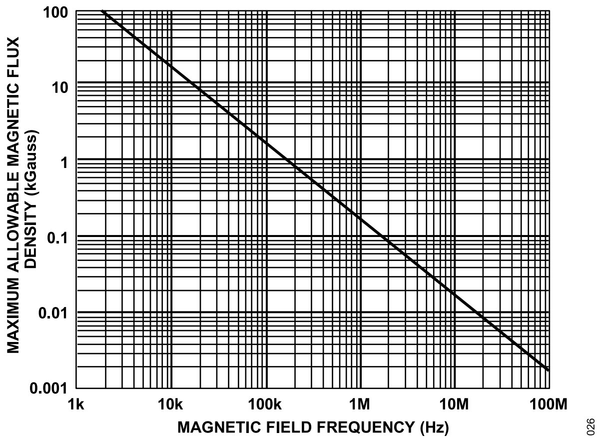

Figure 28. Maximum Allowable External Magnetic Flux Density

For example, at a magnetic field frequency of 1 MHz, the maximum allowable magnetic field of 0.2 kgauss induces a voltage of 0.25 V at the receiving coil. This is about 50% of the sensing threshold and does not cause a faulty output transition. Similarly, if such an event occurs during a transmitted pulse (and is of the worst-case polarity), it reduces the received pulse from >1.0 V to 0.75 V, which is still well above the 0.5 V sensing threshold of the decoder.

The preceding magnetic flux density values correspond to specific current magnitudes at given distances from the ADuM6210/ADuM6211/ADuM6212 transformers. Figure 29 expresses these allowable current magnitudes as a function of frequency for selected distances. As shown in Figure 29, the ADuM6210/ADuM6211/ADuM6212 are extremely immune and can be affected only by extremely large currents operated at high frequency very close to the component. For the 1 MHz example, a 0.5 kA current, placed 5 mm away from the ADuM6210/ADuM6211/ADuM6212, is required to affect component operation.

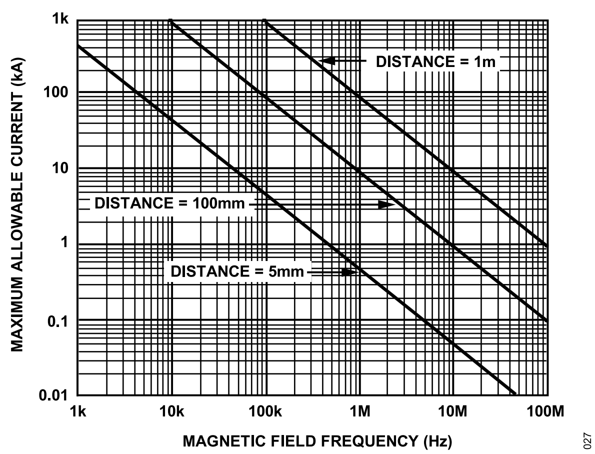

Figure 29. Maximum Allowable Current for Various Current-to-ADuM621x Spacings

Note that, in combinations of strong magnetic field and high frequency, any loops formed by PCB traces can induce error voltages that are sufficiently large to trigger the thresholds of succeeding circuitry. Exercise care in the layout of such traces to avoid this possibility.

POWER CONSUMPTION

The VDDP power supply input provides power only to the converter. Power for the data channels is provided through VDD1 and VDD2. These power supplies can be connected to VDDP and VISO, if desired; or the supplies can receive power from an independent source. The converter should be treated as a standalone supply to be utilized at the discretion of the designer.

The V_{DD1} or V_{DD2} supply current at a given channel of the ADuM6210/ADuM6211/ADuM6212 isolator is a function of the supply voltage, the data rate of the channel, and the output load of the channel.

For each input channel, the supply current is given by

$$I_{DDI} = I_{DDI(Q)} \quad f \leq 0.5\, f_r \tag{3}$$

$$I_{DDI} = I_{DDI(D)} \times (2f - f_r) + I_{DDI(Q)} \quad f > 0.5\, f_r \tag{4}$$

For each output channel, the supply current is given by

$$I_{DDO} = I_{DDO(Q)} \quad f \leq 0.5\, f_r \tag{5}$$

$$I_{DDO} = (I_{DDO(D)} + (0.5 \times 10^{-3}) \times C_L \times V_{DDO}) \times (2f - f_r) + I_{DDO(Q)} \quad f > 0.5\, f_r \tag{6}$$

where:

$I_{DDI(D)}$, $I_{DDO(D)}$ are the input and output dynamic supply currents per channel (mA/Mbps).
$I_{DDI(Q)}$, $I_{DDO(Q)}$ are the specified input and output quiescent supply currents (mA).
f is the input logic signal frequency (MHz); it is half the input data rate, expressed in units of Mbps.
f_r is the input stage refresh rate (Mbps).
C_L is the output load capacitance (pF).
V_{DDO} is the output supply voltage (V).

To calculate the total V_{DD1} and V_{DD2} supply current, the supply currents for each input and output channel corresponding to V_{DD1} and V_{DD2} are calculated and totaled. Figure 18 and Figure 19 show per-channel supply currents as a function of data rate for an unloaded output condition. Figure 20 shows the per-channel supply current as a function of data rate for a 15 pF output condition. Figure 21 through Figure 23 show the total V_{DD1} and V_{DD2} supply current as a function of data rate for ADuM6210/ADuM6211/ADuM6212 channel configurations.

INSULATION LIFETIME

All insulation structures eventually break down when subjected to voltage stress over a sufficiently long period. The rate of insulation degradation is dependent on the characteristics of the voltage waveform applied across the insulation. Analog Devices conducts an extensive set of evaluations to determine the lifetime of the insulation structure within the ADuM6210/ADuM6211/ADuM6212.

OUTLINE DIMENSIONS

Package Drawing (Option)	Package Type	Package Description
RS-20	SSOP	20-Lead Shrink Small Outline Package

For the latest package outline information and land patterns (footprints), go to Package Index.

ORDERING GUIDE

Model[1, 2]	Temperature Range	Package Description	Packing Quantity	Package Option
ADUM6210ARSZ	-40°C to +105°C	20-Lead SSOP	Tube, 66	RS-20
ADUM6210ARSZ-RL7	-40°C to +105°C	20-Lead SSOP	Reel, 500	RS-20
ADUM6210BRSZ	-40°C to +105°C	20-Lead SSOP	Tube, 66	RS-20
ADUM6210BRSZ-RL7	-40°C to +105°C	20-Lead SSOP	Reel, 500	RS-20
ADUM6210CRSZ	-40°C to +105°C	20-Lead SSOP	Tube, 66	RS-20
ADUM6210CRSZ-RL7	-40°C to +105°C	20-Lead SSOP	Reel, 500	RS-20
ADUM6211ARSZ	-40°C to +105°C	20-Lead SSOP	Tube, 66	RS-20
ADUM6211ARSZ-RL7	-40°C to +105°C	20-Lead SSOP	Reel, 500	RS-20
ADUM6211BRSZ	-40°C to +105°C	20-Lead SSOP	Tube, 66	RS-20
ADUM6211BRSZ-RL7	-40°C to +105°C	20-Lead SSOP	Reel, 500	RS-20
ADUM6211CRSZ	-40°C to +105°C	20-Lead SSOP	Tube, 66	RS-20
ADUM6211CRSZ-RL7	-40°C to +105°C	20-Lead SSOP	Reel, 500	RS-20
ADUM6212ARSZ	-40°C to +105°C	20-Lead SSOP	Tube, 66	RS-20
ADUM6212ARSZ-RL7	-40°C to +105°C	20-Lead SSOP	Reel, 500	RS-20
ADUM6212BRSZ	-40°C to +105°C	20-Lead SSOP	Tube, 66	RS-20
ADUM6212BRSZ-RL7	-40°C to +105°C	20-Lead SSOP	Reel, 500	RS-20
ADUM6212CRSZ	-40°C to +105°C	20-Lead SSOP	Tube, 66	RS-20
ADUM6212CRSZ-RL7	-40°C to +105°C	20-Lead SSOP	Reel, 500	RS-20

[1] Z = RoHS Compliant Part.

[2] The addition of an RL7 suffix designates a 7” tape and reel option.

Updated: April 25, 2024

NUMBER OF INPUTS (V_{DDP} SIDE AND V_{ISO} SIDE), MAXIMUM DATA RATE, MAXIMUM PROPAGATION DELAY, AND MAXIMUM PULSE WIDTH DISTORTION OPTIONS

Model[1]	Number of Inputs, V_{DDP} Side	Number of Inputs, V_{ISO} Side	Maximum Data Rate (Mbps)	Maximum Propagation Delay, 5 V (ns)	Maximum Pulse Width Distortion (ns)
ADUM6210ARSZ	2	0	1	75	40
ADUM6210BRSZ	2	0	25	40	3
ADUM6210CRSZ	2	0	100	15	2
ADUM6211ARSZ	1	1	1	75	40
ADUM6211BRSZ	1	1	25	40	3
ADUM6211CRSZ	1	1	100	15	2
ADUM6212ARSZ	0	2	1	75	40
ADUM6212BRSZ	0	2	25	40	3
ADUM6212CRSZ	0	2	100	15	2

[1] Z = RoHS Compliant Part.