ADuM4151/ADuM4152/ADuM4153

5 kV, 7-Channel, SPIsolator Digital Isolators for SPI

FEATURES

- Supports up to 17 MHz SPI clock speed
- 4 high speed, low propagation delay, SPI signal isolation channels
- Three 250 kbps data channels
- 20-lead SOIC_IC package with 8.3 mm creepage
- High temperature operation: 125°C
- High common-mode transient immunity: >25 kV/μs
- Safety and regulatory approvals
  - UL recognition per UL 1577
    - 5000 V rms for 1 minute
  - IEC/EN/CSA 62368-1
  - IEC/CSA 60601-1
  - IEC/CSA 61010-1
  - DIN EN IEC 60747-17 (VDE 0884-17)
    - V_{IORM} = 645 V peak

APPLICATIONS

- Industrial programmable logic controllers (PLCs)
- Sensor isolation

GENERAL DESCRIPTION

The ADuM4151/ADuM4152/ADuM4153[1] are 7-channel, SPIsolator™ digital isolators optimized for isolated serial peripheral interfaces (SPIs). Based on the Analog Devices, Inc., *i*Coupler® chip scale transformer technology, the low propagation delay in the CLK, MO/SI, MI/SO, and $\overline{SS}$ SPI bus signals supports SPI clock rates of up to 17 MHz. These channels operate with 14 ns propagation delay and 1 ns jitter to optimize timing for SPI.

The ADuM4151/ADuM4152/ADuM4153 isolators also provide three additional independent low data rate isolation channels in three different channel direction combinations. Data in the slow channels is sampled and serialized for a 250 kbps data rate with up to 2.5 μs of jitter in the low speed channels.

FUNCTIONAL BLOCK DIAGRAMS

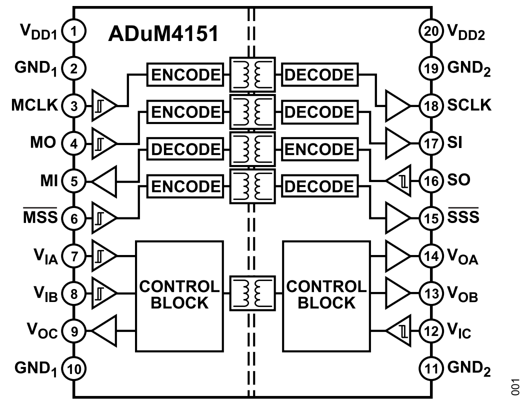

Figure 1. ADuM4151 Functional Block Diagram

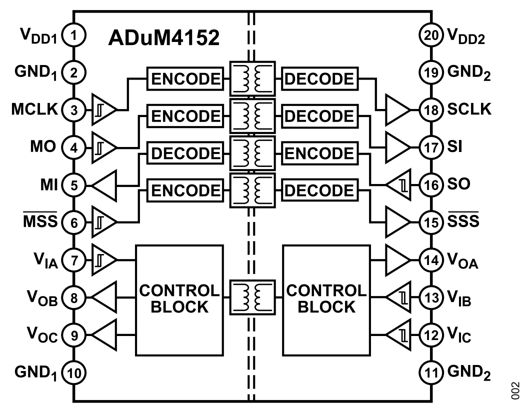

Figure 2. ADuM4152 Functional Block Diagram

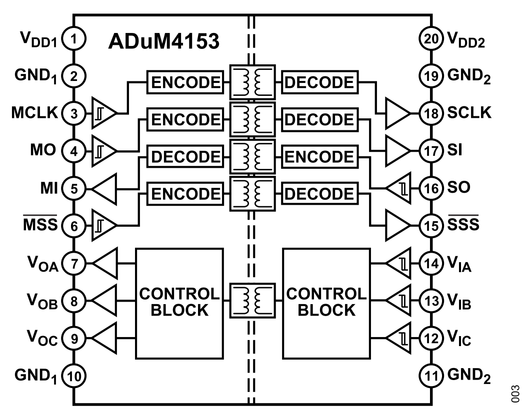

Figure 3. ADuM4153 Functional Block Diagram

[1] Protected by U.S. Patents 5,952,849; 6,873,065; 6,262,600; and 7,075,329. Other patents are pending.

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REVISION HISTORY

2/2025—Rev. C to Rev. D

Changed Master to Main and Slave to Subordinate (Throughout) 1
Changes to Features Section 1
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Changed DIN V VDE V 0884-10 (VDE V 0884-10): 2006-12 Insulation Characteristics Section to DIN EN IEC 60747-17 (VDE 0884-17) Insulation Characteristics Section 10
Changes to DIN EN IEC 60747-17 (VDE 0884-17) Insulation Characteristics Section, Table 16, and Figure 4 Caption 10
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Changes to Insulation Lifetime Section 18
Deleted Surface Tracking Section, Insulation Wear Out Section, Calculation and Use of Parameters Example Section, and Figure 19; Renumbered Sequentially 18

2/2024—Rev. B to Rev. C

Changes to Features Section 1
Changes to Functional Block Diagrams Section 1
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Updated Outline Dimensions 20
Added Number of Inputs (V_{DD1} Side and V_{DD2} Side), Maximum Data Rate, Maximum Propagation Delay, and Isolation Rating Options 20

SPECIFICATIONS

ELECTRICAL CHARACTERISTICS—5 V OPERATION

All typical specifications are at T_A = 25°C and V_{DD1} = V_{DD2} = 5 V. Minimum and maximum specifications apply over the entire recommended operation range: 4.5 V ≤ V_{DD1} ≤ 5.5 V, 4.5 V ≤ V_{DD2} ≤ 5.5 V, and −40°C ≤ T_A ≤ +125°C, unless otherwise noted. Switching specifications are tested with C_L = 15 pF and CMOS signal levels, unless otherwise noted.

Table 1. Switching Specifications

		A Grade			B Grade				
Parameter	Symbol	Min	Typ	Max	Min	Typ	Max	Unit	Test Conditions/Comments
MCLK, MO, SO									
SPI Clock Rate	SPI_{MCLK}			1			17	MHz	
Data Rate Fast (MO, SO)	DR_{FAST}			2			34	Mbps	Within PWD limit
Propagation Delay	t_{PHL}, t_{PLH}			25		12	14	ns	50% input to 50% output
Pulse Width	PW	100			12.5			ns	Within PWD limit
Pulse Width Distortion	PWD			3			2	ns	$\lvert t_{PLH} - t_{PHL}\rvert$
Codirectional Channel Matching[1]	t_{PSKCD}			3			2	ns	
Jitter, High Speed	J_{HS}		1			1		ns	
$\overline{MSS}$									
Data Rate Fast	DR_{FAST}			2			34	Mbps	Within PWD limit
Propagation Delay	t_{PHL}, t_{PLH}		21	25		21	25	ns	50% input to 50% output
Pulse Width	PW	100			12.5			ns	Within PWD limit
Pulse Width Distortion	PWD			3			3	ns	$\lvert t_{PLH} - t_{PHL}\rvert$
Setup Time[2]	$\overline{MSS}_{SETUP}$	1.5			10			ns	
Jitter, High Speed	J_{HS}		1			1		ns	
V_{IA}, V_{IB}, V_{IC}									
Data Rate Slow	DR_{SLOW}			250			250	kbps	Within PWD limit
Propagation Delay	t_{PHL}, t_{PLH}	0.1		2.6	0.1		2.6	μs	50% input to 50% output
Pulse Width	PW	4			4			μs	Within PWD limit
Jitter, Low Speed	J_{LS}			2.5			2.5	μs	
V_{Ix}[3] Minimum Input Skew[4]	$t_{VIx\ SKEW}$[3]	10			10			ns	

1 Codirectional channel matching is the absolute value of the difference in propagation delays between any two channels with inputs on the same side of the isolation barrier.

2 The $\overline{MSS}$ signal is glitch filtered in both speed grades, whereas the other fast signals are not glitch filtered in the B grade. To guarantee that $\overline{MSS}$ reaches the output ahead of another fast signal, set up $\overline{MSS}$ prior to the competing signal by different times depending on speed grade.

3 V_{Ix} = V_{IA}, V_{IB}, or V_{IC}.

4 An internal asynchronous clock not available to users samples the low speed signals. If edge sequence in codirectional channels is critical to the end application, the leading pulse must be at least 1 $t_{VIx\ SKEW}$ time ahead of a later pulse to guarantee the correct order or simultaneous arrival at the output.

Table 2. Supply Current

		1 MHz, A Grade			17 MHz, B Grade				
Device Number	Symbol	Min	Typ	Max	Min	Typ	Max	Unit	Test Conditions/Comments
ADuM4151	I_{DD1}		4.0	8.5		14.0	22	mA	C_L = 0 pF, low speed channels
	I_{DD2}		6.0	11		13.5	23	mA	C_L = 0 pF, low speed channels
ADuM4152	I_{DD1}		4.8	8.5		14.0	21.5	mA	C_L = 0 pF, low speed channels
	I_{DD2}		6.5	10.5		14.0	22.5	mA	C_L = 0 pF, low speed channels
ADuM4153	I_{DD1}		4.0	8.5		14.0	22	mA	C_L = 0 pF, low speed channels
	I_{DD2}		6.0	10.5		13.3	21	mA	C_L = 0 pF, low speed channels

SPECIFICATIONS

Table 3. For All Models[1, 2, 3]

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
DC SPECIFICATIONS						
MCLK, $\overline{\text{MSS}}$, MO, SO, V_{IA}, V_{IB}, V_{IC}						
Logic High Input Threshold	V_{IH}	$0.7 \times V_{DDx}$			V	
Logic Low Input Threshold	V_{IL}			$0.3 \times V_{DDx}$	V	
Input Hysteresis	V_{IHYST}		500		mV	
Input Current per Channel	I_I	−1	+0.01	+1	µA	$0 V \leq V_{INPUT} \leq V_{DDx}$
SCLK, $\overline{\text{SSS}}$, MI, SI, V_{OA}, V_{OB}, V_{OC}						
Logic High Output Voltages	V_{OH}	$V_{DDx} - 0.1$	5.0		V	$I_{OUTPUT} = -20$ µA, $V_{INPUT} = V_{IH}$
		$V_{DDx} - 0.4$	4.8		V	$I_{OUTPUT} = -4$ mA, $V_{INPUT} = V_{IH}$
Logic Low Output Voltages	V_{OL}		0.0	0.1	V	$I_{OUTPUT} = 20$ µA, $V_{INPUT} = V_{IL}$
			0.2	0.4	V	$I_{OUTPUT} = 4$ mA, $V_{INPUT} = V_{IL}$
V_{DD1}, V_{DD2} Undervoltage Lockout	UVLO		2.6		V	
Supply Current per High Speed Channel						
Dynamic Input Supply Current	$I_{DDI(D)}$		0.080		mA/Mbps	
Dynamic Output Supply Current	$I_{DDO(D)}$		0.046		mA/Mbps	
Supply Current for All Low Speed Channels						
Quiescent Side 1 Current	$I_{DD1(Q)}$		4.3		mA	
Quiescent Side 2 Current	$I_{DD2Q)}$		6.1		mA	
AC SPECIFICATIONS						
Output Rise/Fall Time	t_R/t_F		2.5		ns	10% to 90%
Common-Mode Transient Immunity[4]	|CM|	25	35		kV/µs	$V_{INPUT} = V_{DDx}$, $V_{CM} = 1000$ V, transient magnitude = 800 V

1 $V_{DDx} = V_{DD1}$ or V_{DD2}.

2 V_{INPUT} is the input voltage of any of the MCLK, $\overline{\text{MSS}}$, MO, SO, V_{IA}, V_{IB}, or V_{IC} pins.

3 I_{OUTPUT} is the output current of any of the SCLK, $\overline{\text{SSS}}$, MI, SI, V_{OA}, V_{OB}, or V_{OC} pins.

4 |CM| is the maximum common-mode voltage slew rate that can be sustained while maintaining output voltages within the V_{OH} and V_{OL} limits. The common-mode voltage slew rates apply to both rising and falling common-mode voltage edges.

ELECTRICAL CHARACTERISTICS—3.3 V OPERATION

All typical specifications are at $T_A = 25°C$ and $V_{DD1} = V_{DD2} = 3.3$ V. Minimum and maximum specifications apply over the entire recommended operation range: $3.0 V \leq V_{DD1} \leq 3.6 V$, $3.0 V \leq V_{DD2} \leq 3.6 V$, and $-40°C \leq T_A \leq +125°C$, unless otherwise noted. Switching specifications are tested with C_L =15 pF and CMOS signal levels, unless otherwise noted.

Table 4. Switching Specifications

		A Grade			B Grade				
Parameter	Symbol	Min	Typ	Max	Min	Typ	Max	Unit	Test Conditions/Comments
MCLK, MO, SO									
SPI Clock Rate	SPI_{MCLK}			1			12.5	MHz	
Data Rate Fast (MO, SO)	DR_{FAST}			2			34	Mbps	Within PWD limit
Propagation Delay	t_{PHL}, t_{PLH}			30			20	ns	50% input to 50% output
Pulse Width	PW	100			12.5			ns	Within PWD limit
Pulse Width Distortion	PWD			3			3	ns	$\|t_{PLH} - t_{PHL}\|$
Codirectional Channel Matching[1]	t_{PSKCD}			4			2	ns	
Jitter, High Speed	J_{HS}		1			1		ns	
$\overline{\text{MSS}}$									
Data Rate Fast	DR_{FAST}			2			34	Mbps	Within PWD limit
Propagation Delay	t_{PHL}, t_{PLH}			30			30	ns	50% input to 50% output

SPECIFICATIONS

Table 4. Switching Specifications (Continued)

		A Grade			B Grade				
Parameter	Symbol	Min	Typ	Max	Min	Typ	Max	Unit	Test Conditions/Comments
Pulse Width	PW	100			12.5			ns	Within PWD limit
Pulse Width Distortion	PWD			3			3	ns	$\lvert t_{PLH} - t_{PHL} \rvert$
Setup Time[2]	$\overline{MSS}_{SETUP}$	1.5			10			ns	
Jitter, Low Speed	J_{LS}		2.5			2.5		ns	
V_{IA}, V_{IB}, V_{IC}									
Data Rate Slow	DR_{SLOW}			250			250	kbps	Within PWD limit
Propagation Delay	t_{PHL}, t_{PLH}	0.1		2.6	0.1		2.6	µs	50% input to 50% output
Pulse Width	PW	4			4			µs	Within PWD limit
Jitter, Low Speed	J_{LS}			2.5			2.5	µs	$\lvert t_{PLH} - t_{PHL} \rvert$
V_{Ix}[3] Minimum Input Skew[4]	$t_{VIx\ SKEW}$[3]	10			10			ns	

1 Codirectional channel matching is the absolute value of the difference in propagation delays between any two channels with inputs on the same side of the isolation barrier.

2 The $\overline{MSS}$ signal is glitch filtered in both speed grades, whereas the other fast signals are not glitch filtered in the B grade. To guarantee that $\overline{MSS}$ reaches the output ahead of another fast signal, set up $\overline{MSS}$ prior to the competing signal by different times depending on speed grade.

3 $V_{Ix} = V_{IA}$, V_{IB}, or V_{IC}.

4 An internal asynchronous clock not available to users samples the low speed signals. If edge sequence in codirectional channels is critical to the end application, the leading pulse must be at least 1 $t_{VIx\ SKEW}$ time ahead of a later pulse to guarantee the correct order or simultaneous arrival at the output.

Table 5. Supply Current

		1 MHz, A Grade/B Grade			17 MHz, B Grade				
Device Number	Symbol	Min	Typ	Max	Min	Typ	Max	Unit	Test Conditions/Comments
ADuM4151	I_{DD1}		3.8	7		10.5	18	mA	C_L = 0 pF, low speed channels
	I_{DD2}		5.1	8		9.0	17	mA	C_L = 0 pF, low speed channels
ADuM4152	I_{DD1}		3.7	6.5		11.7	18	mA	C_L = 0 pF, low speed channels
	I_{DD2}		5.2	8		10.0	16	mA	C_L = 0 pF, low speed channels
ADuM4153	I_{DD1}		3.7	6.5		11.7	18	mA	C_L = 0 pF, low speed channels
	I_{DD2}		5.2	9		10.0	15	mA	C_L = 0 pF, low speed channels

Table 6. For All Models[1, 2, 3]

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
DC SPECIFICATIONS						
MCLK, $\overline{MSS}$, MO, SO, V_{IA}, V_{IB}, V_{IC}						
Logic High Input Threshold	V_{IH}	0.7 × V_{DDx}			V	
Logic Low Input Threshold	V_{IL}			0.3 × V_{DDx}	V	
Input Hysteresis	V_{IHYST}		500		mV	
Input Current per Channel	I_I	−1	+0.01	+1	µA	0 V ≤ V_{INPUT} ≤ V_{DDx}
SCLK, $\overline{SSS}$, MI, SI, V_{OA}, V_{OB}, V_{OC}						
Logic High Output Voltages	V_{OH}	V_{DDx} − 0.1	3.3		V	I_{OUTPUT} = −20 µA, $V_{INPUT} = V_{IH}$
		V_{DDx} − 0.4	3.1		V	I_{OUTPUT} = −4 mA, $V_{INPUT} = V_{IH}$
Logic Low Output Voltages	V_{OL}		0.0	0.1	V	I_{OUTPUT} = 20 µA, $V_{INPUT} = V_{IL}$
			0.2	0.4	V	I_{OUTPUT} = 4 mA, $V_{INPUT} = V_{IL}$
V_{DD1}, V_{DD2} Undervoltage Lockout	UVLO		2.6		V	
Supply Current per High Speed Channel						
Dynamic Input Supply Current	$I_{DDI(D)}$		0.086		mA/Mbps	
Dynamic Output Supply Current	$I_{DDO(D)}$		0.019		mA/Mbps	
Supply Current for All Low Speed Channels						
Quiescent Side 1 Current	$I_{DD1(Q)}$		2.9		mA	

SPECIFICATIONS

Table 6. For All Models[1, 2, 3] (Continued)

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
Quiescent Side 2 Current	$I_{DD2Q)}$		4.7		mA	
AC SPECIFICATIONS						
Output Rise/Fall Time	t_R/t_F		2.5		ns	10% to 90%
Common-Mode Transient Immunity[4]	|CM|	25	35		kV/µs	$V_{INPUT} = V_{DDx}$, V_{CM} = 1000 V, transient magnitude = 800 V

1 $V_{DDx} = V_{DD1}$ or V_{DD2}.

2 V_{INPUT} is the input voltage of any of the MCLK, $\overline{MSS}$, MO, SO, V_{IA}, V_{IB}, or V_{IC} pins.

3 I_{OUTPUT} is the output current of any of the SCLK, $\overline{SSS}$, MI, SI, V_{OA}, V_{OB}, or V_{OC} pins.

4 |CM| is the maximum common-mode voltage slew rate that can be sustained while maintaining output voltages within the V_{OH} and V_{OL} limits. The common-mode voltage slew rates apply to both rising and falling common-mode voltage edges.

ELECTRICAL CHARACTERISTICS—MIXED 5 V/3.3 V OPERATION

All typical specifications are at T_A = 25°C, V_{DD1} = 5 V, and V_{DD2} = 3.3 V. Minimum and maximum specifications apply over the entire recommended operation range: 4.5 V ≤ V_{DD1} ≤ 5.5 V, 3.0 V ≤ V_{DD2} ≤ 3.6 V, and −40°C ≤ T_A ≤ +125°C, unless otherwise noted. Switching specifications are tested with C_L =15 pF and CMOS signal levels, unless otherwise noted.

Table 7. Switching Specifications

		A Grade			B Grade				
Parameter	Symbol	Min	Typ	Max	Min	Typ	Max	Unit	Test Conditions/Comments
MCLK, MO, SO									
SPI Clock Rate	SPI_{MCLK}			1			15.6	MHz	1/(4 × t_{PHL})
Data Rate Fast (MO, SO)	DR_{FAST}			2			34	Mbps	Within PWD limit
Propagation Delay	t_{PHL}, t_{PLH}			27			16	ns	50% input to 50% output
Pulse Width	PW	100			12.5			ns	Within PWD limit
Pulse Width Distortion	PWD			3			3	ns	$\|t_{PLH} - t_{PHL}\|$
Codirectional Channel Matching[1]	t_{PSKCD}			3			2	ns	
Jitter, High Speed	J_{HS}		1			1		ns	
$\overline{MSS}$									
Data Rate Fast	DR_{FAST}			2			34	Mbps	Within PWD limit
Propagation Delay	t_{PHL}, t_{PLH}			27			26	ns	50% input to 50% output
Pulse Width	PW	100			12.5			ns	Within PWD limit
Pulse Width Distortion	PWD			3			3	ns	$\|t_{PLH} - t_{PHL}\|$
Setup Time[2]	$\overline{MSS}_{SETUP}$	1.5			10			ns	
Jitter, High Speed	J_{HS}		1			1		ns	
V_{IA}, V_{IB}, V_{IC}									
Data Rate Slow	DR_{SLOW}			250			250	kbps	Within PWD limit
Propagation Delay	t_{PHL}, t_{PLH}	0.1		2.6	0.1		2.6	µs	50% input to 50% output
Pulse Width	PW	4			4			µs	Within PWD limit
Jitter, Low Speed	J_{LS}			2.5			2.5	µs	
V_{Ix}[3] Minimum Input Skew[4]	$t_{VIx\ SKEW}$[3]	10			10			ns	

1 Codirectional channel matching is the absolute value of the difference in propagation delays between any two channels with inputs on the same side of the isolation barrier.

2 The $\overline{MSS}$ signal is glitch filtered in both speed grades, whereas the other fast signals are not glitch filtered in the B grade. To guarantee that $\overline{MSS}$ reaches the output ahead of another fast signal, set up $\overline{MSS}$ prior to the competing signal by different times depending on speed grade.

3 $V_{Ix} = V_{IA}$, V_{IB}, or V_{IC}.

4 An internal asynchronous clock not available to users samples the low speed signals. If edge sequence in codirectional channels is critical to the end application, the leading pulse must be at least 1 $t_{VIx\ SKEW}$ time ahead of a later pulse to guarantee the correct order or simultaneous arrival at the output.

SPECIFICATIONS

Table 8. Supply Current

		1 MHz, A Grade/B Grade			17 MHz, B Grade				
Device Number	Symbol	Min	Typ	Max	Min	Typ	Max	Unit	Test Conditions/Comments
ADuM4151	I_{DD1}		4.0	8.5		13.9	22	mA	C_L = 0 pF, low speed channels
	I_{DD2}		4.6	8		9.0	17	mA	C_L = 0 pF, low speed channels
ADuM4152	I_{DD1}		4.8	8.5		14.0	21.5	mA	C_L = 0 pF, low speed channels
	I_{DD2}		5.0	8		10.0	16	mA	C_L = 0 pF, low speed channels
ADuM4153	I_{DD1}		4.0	8.5		14.0	22	mA	C_L = 0 pF, low speed channels
	I_{DD2}		4.7	9		10.0	15	mA	C_L = 0 pF, low speed channels

Table 9. For All Models[1, 2, 3]

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
DC SPECIFICATIONS						
MCLK, $\overline{MSS}$, MO, SO, V_{IA}, V_{IB}, V_{IC}						
Logic High Input Threshold	V_{IH}	$0.7 \times V_{DDx}$			V	
Logic Low Input Threshold	V_{IL}			$0.3 \times V_{DDx}$	V	
Input Hysteresis	V_{IHYST}		500		mV	
Input Current per Channel	I_I	−1	+0.01	+1	µA	$0 V \leq V_{INPUT} \leq V_{DDx}$
SCLK, $\overline{SSS}$, MI, SI, V_{OA}, V_{OB}, V_{OC}						
Logic High Output Voltages	V_{OH}	$V_{DDX} - 0.1$	V_{DDX}		V	$I_{OUTPUT} = -20$ µA, $V_{INPUT} = V_{IH}$
		$V_{DDX} - 0.4$	$V_{DDX} - 2.0$		V	$I_{OUTPUT} = -4$ mA, $V_{INPUT} = V_{IH}$
Logic Low Output Voltages	V_{OL}		0.0	0.1	V	$I_{OUTPUT} = 20$ µA, $V_{INPUT} = V_{IL}$
			0.2	0.4	V	$I_{OUTPUT} = 4$ mA, $V_{INPUT} = V_{IL}$
V_{DD1}, V_{DD2} Undervoltage Lockout	UVLO		2.6		V	
Supply Current for All Low Speed Channels						
Quiescent Side 1 Current	$I_{DD1(Q)}$		4.3		mA	
Quiescent Side 2 Current	$I_{DD2Q)}$		4.7		mA	
AC SPECIFICATIONS						
Output Rise/Fall Time	t_R/t_F		2.5		ns	10% to 90%
Common-Mode Transient Immunity[4]	|CM|	25	35		kV/µs	$V_{INPUT} = V_{DDX}$, V_{CM} = 1000 V, transient magnitude = 800 V

1 $V_{DDx} = V_{DD1}$ or V_{DD2}.

2 V_{INPUT} is the input voltage of any of the MCLK, $\overline{MSS}$, MO, SO, V_{IA}, V_{IB}, or V_{IC} pins.

3 I_{OUTPUT} is the output current of any of the SCLK, $\overline{SSS}$, MI, SI, V_{OA}, V_{OB}, V_{OC} pins.

4 |CM| is the maximum common-mode voltage slew rate that can be sustained while maintaining output voltages within the V_{OH} and V_{OL} limits. The common-mode voltage slew rates apply to both rising and falling common-mode voltage edges.

ELECTRICAL CHARACTERISTICS—MIXED 3.3 V/5 V OPERATION

All typical specifications are at T_A = 25°C, V_{DD1} = 3.3 V, and V_{DD2} = 5 V. Minimum and maximum specifications apply over the entire recommended operation range: $3.0 V \leq V_{DD1} \leq 3.6 V$, $4.5 V \leq V_{DD2} \leq 5.5 V$, and $-40°C \leq T_A \leq +125°C$, unless otherwise noted. Switching specifications are tested with C_L =15 pF and CMOS signal levels, unless otherwise noted.

Table 10. Switching Specifications

		A Grade			B Grade				
Parameter	Symbol	Min	Typ	Max	Min	Typ	Max	Unit	Test Conditions/Comments
MCLK, MO, SO									
SPI Clock Rate	SPI_{MCLK}			1			15.6	MHz	
Data Rate Fast (MO, SO)	DR_{FAST}			2			34	Mbps	Within PWD limit
Propagation Delay	t_{PHL}, t_{PLH}			27			16	ns	50% input to 50% output

SPECIFICATIONS

Table 10. Switching Specifications (Continued)

Parameter	Symbol	A Grade Min	A Grade Typ	A Grade Max	B Grade Min	B Grade Typ	B Grade Max	Unit	Test Conditions/Comments
Pulse Width	PW	100			12.5			ns	Within PWD limit
Pulse Width Distortion	PWD			3			3	ns	$\lvert t_{PLH} - t_{PHL}\rvert$
Codirectional Channel Matching[1]	t_{PSKCD}			5			2	ns	
Jitter, High Speed	J_{HS}		1			1		ns	
$\overline{MSS}$									
Data Rate Fast	DR_{FAST}			2			34	Mbps	Within PWD limit
Propagation Delay	t_{PHL}, t_{PLH}			27			27	ns	50% input to 50% output
Pulse Width	PW	100			12.5			ns	Within PWD limit
Pulse Width Distortion	PWD			2			3	ns	$\lvert t_{PLH} - t_{PHL}\rvert$
Setup Time[2]	$\overline{MSS}_{SETUP}$	1.5			10			ns	
Jitter, High Speed	J_{HS}		1			1		ns	
V_{IA}, V_{IB}, V_{IC}									
Data Rate	DR_{SLOW}			250			250	kbps	Within PWD limit
Propagation Delay	t_{PHL}, t_{PLH}	0.1		2.6	0.1		2.6	μs	50% input to 50% output
Pulse Width	PW	4			4			μs	Within PWD limit
Jitter, Low Speed	J_{LS}			2.5			2.5	μs	$\lvert t_{PLH} - t_{PHL}\rvert$
V_{Ix}[3] Minimum Input Skew[4]	$t_{VIx\ SKEW}$[3]	10			10			ns	

1 Codirectional channel matching is the absolute value of the difference in propagation delays between any two channels with inputs on the same side of the isolation barrier.

2 The $\overline{MSS}$ signal is glitch filtered in both speed grades, whereas the other fast signals are not glitch filtered in the B grade. To guarantee that $\overline{MSS}$ reaches the output ahead of another fast signal, it must be set up prior to the competing signal by different times depending on speed grade.

3 $V_{Ix} = V_{IA}$, V_{IB}, or V_{IC}.

4 An internal asynchronous clock not available to users samples the low speed signals. If edge sequence in codirectional channels is critical to the end application, the leading pulse must be at least 1 $t_{VIx\ SKEW}$ time ahead of a later pulse to guarantee the correct order or simultaneous arrival at the output.

Table 11. Supply Current

Device Number	Symbol	1 MHz, A Grade/B Grade Min	1 MHz, A Grade/B Grade Typ	1 MHz, A Grade/B Grade Max	17 MHz, B Grade Min	17 MHz, B Grade Typ	17 MHz, B Grade Max	Unit	Test Conditions/Comments
ADuM4151	I_{DD1}		2.8	7		10.5	18	mA	C_L = 0 pF, low speed channels
	I_{DD2}		6.0	10.5		13.0	23	mA	C_L = 0 pF, low speed channels
ADuM4152	I_{DD1}		3.5	6.5		11.7	18	mA	C_L = 0 pF, low speed channels
	I_{DD2}		6.5	10.5		13.4	22.5	mA	C_L = 0 pF, low speed channels
ADuM4153	I_{DD1}		2.8	6.5		11.7	18	mA	C_L = 0 pF, low speed channels
	I_{DD2}		6.0	10.5		13.4	21	mA	C_L = 0 pF, low speed channels

Table 12. For All Models[1, 2, 3]

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
DC SPECIFICATIONS						
MCLK, $\overline{MSS}$, MO, SO, V_{IA}, V_{IB}, V_{IC}						
Logic High Input Threshold	V_{IH}	0.7 × V_{DDx}			V	
Logic Low Input Threshold	V_{IL}			0.3 × V_{DDx}	V	
Input Hysteresis	V_{IHYST}		500		mV	
Input Current per Channel	I_I	−1	+0.01	+1	μA	0 V ≤ V_{INPUT} ≤ V_{DDx}
SCLK, $\overline{SSS}$, MI, SI, V_{OA}, V_{OB}, V_{OC}						
Logic High Output Voltages	V_{OH}	V_{DDx} − 0.1	V_{DDX}		V	I_{OUTPUT} = −20 μA, V_{INPUT} = V_{IH}
		V_{DDx} − 0.4	V_{DDX} − 2.0		V	I_{OUTPUT} = −4 mA, V_{INPUT} = V_{IH}

SPECIFICATIONS

Table 12. For All Models[1, 2, 3] (Continued)

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
Logic Low Output Voltages	V_{OL}		0.0	0.1	V	I_{OUTPUT} = 20 µA, V_{INPUT} = V_{IL}
			0.2	0.4	V	I_{OUTPUT} = 4 mA, V_{INPUT} = V_{IL}
V_{DD1}, V_{DD2} Undervoltage Lockout	UVLO		2.6		V	
Supply Current for All Low Speed Channels						
Quiescent Side 1 Current	$I_{DD1(Q)}$		2.9		mA	
Quiescent Side 2 Current	$I_{DD2Q)}$		6.1		mA	
AC SPECIFICATIONS						
Output Rise/Fall Time	t_R/t_F		2.5		ns	10% to 90%
Common-Mode Transient Immunity[4]	|CM|	25	35		kV/µs	V_{INPUT} = V_{DDX}, V_{CM} = 1000 V, transient magnitude = 800 V

1 V_{DDx} = V_{DD1} or V_{DD2}.

2 VI_{NPUT} is the input voltage of any of the MCLK, $\overline{MSS}$, MO, SO, V_{IA}, V_{IB}, V_{IC} pins.

3 I_{OUTPUT} is the output current of any of the SCLK, $\overline{SSS}$, MI, SI, V_{OA}, V_{OB}, V_{OC} pins.

4 |CM| is the maximum common-mode voltage slew rate that can be sustained while maintaining output voltages within the V_{OH} and V_{OL} limits. The common-mode voltage slew rates apply to both rising and falling common-mode voltage edges.

PACKAGE CHARACTERISTICS

Table 13.

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
Resistance (Input to Output)[1]	R_{I-O}		10^{12}		Ω	
Capacitance (Input to Output)[1]	C_{I-O}		1.0		pF	f = 1 MHz
Input Capacitance[2]	C_I		4.0		pF	
IC Junction to Ambient Thermal Resistance	θ_{JA}		46		°C/W	Thermocouple located at center of package underside

1 The device is considered a 2-terminal device: Pin 1 through Pin 10 are shorted together, and Pin 11 through Pin 20 are shorted together.

2 Input capacitance is from any input data pin to ground.

REGULATORY INFORMATION

The ADuM4151/ADuM4152/ADuM4153 are approved by the organizations listed in Table 14. See Table 19 and the Insulation Lifetime section for the recommended maximum working voltages for specific cross isolation waveforms and insulation levels.

Table 14.

UL	CSA	VDE
UL 1577 [1]	IEC/EN/CSA 62368-1	DIN EN IEC 60747-17 (VDE 0884-17)[2]
Single Protection, 5000 V rms	Basic insulation, 870 V rms	Reinforced insulation, 645 V peak
	Reinforced insulation, 435 V rms	
	IEC/CSA 60601-1	
	Basic insulation (1 MOPP), 544 V rms	
	IEC/CSA 61010-1	
	Basic insulation, 600 V rms	
	Reinforced insulation, 300 V rms	
File E214100	File 205078	Certificate No. 40011599

1 In accordance with UL 1577, each model is proof tested by applying an insulation test voltage ≥6000 V rms for 1 second (current leakage detection limit = 10 µA).

2 In accordance with DIN EN IEC 60747-17 (VDE 0884-17), each model is proof tested by applying an insulation test voltage ≥ 1209 V peak for 1 second (partial discharge detection limit = 5 pC).

SPECIFICATIONS

INSULATION AND SAFETY RELATED SPECIFICATIONS

Table 15.

Parameter	Symbol	Value	Unit	Test Conditions/Comments
Rated Dielectric Insulation Voltage		5000	V rms	1-minute duration
Minimum External Air Gap (Clearance)[1, 2]	L(I01)	8.7	mm	Measured from input terminals to output terminals, shortest distance through air
Minimum External Tracking (Creepage)	L(I02)	8.7	mm	Measured from input terminals to output terminals, shortest distance path along body
Minimum Internal Gap (Internal Clearance)		18	μm	Insulation distance through insulation
Tracking Resistance (Comparative Tracking Index)	CTI	>400	V	DIN IEC 112/VDE 0303, Part 1
Material Group		II		Material group per IEC 60664-1

1 In accordance with IEC 62368-1/IEC 60601-1 guidelines for the measurement of creepage and clearance distances for a pollution degree of 2 and altitudes ≤2000 m.

2 Consideration must be given to pad layout to ensure the minimum required distance for clearance is maintained.

DIN EN IEC 60747-17 (VDE 0884-17) INSULATION CHARACTERISTICS

These isolators are suitable for reinforced electrical isolation only within the safety limit data. Maintenance of the safety data is ensured by protective circuits. The asterisk (*) marked on packages denotes DIN EN IEC 60747-17 (VDE 0884-17) approval.

Table 16.

Description	Test Conditions/Comments	Symbol	Characteristic	Unit
Overvoltage Category per IEC 60664-1				
For Rated Mains Voltage ≤ 150 V rms			I to IV	
For Rated Mains Voltage ≤ 300 V rms			I to III	
For Rated Mains Voltage ≤ 400 V rms			I to II	
Climatic Classification			40/105/21	
Pollution Degree per DIN VDE 0110, Table 1			2	
Maximum Repetitive Isolation Voltage		V_{IORM}	645	V peak
Maximum Working Insulation Voltage		V_{IOWM}	456	V rms
Input-to-Output Test Voltage, Method b1	$V_{IORM} \times 1.875 = V_{pd(m)}$, 100% production test, t_m = 1 sec, partial discharge < 5 pC	$V_{pd(m)}$	1209	V peak
Input-to-Output Test Voltage, Method a				
After Environmental Tests Subgroup 1	$V_{IORM} \times 1.6 = V_{pd(m)}$, t_m = 60 sec, partial discharge < 5 pC	$V_{pd(m)}$	1032	V peak
After Input and/or Safety Test Subgroup 2 and Subgroup 3	$V_{IORM} \times 1.2 = V_{pd(m)}$, t_m = 60 sec, partial dischage < 5 pC	$V_{pd(m)}$	774	V peak
Maximum Transient Isolation Voltage	$V_{TEST} = 1.2 \times V_{IOTM}$, t = 1 sec (100% production)	V_{IOTM}	6000	V peak
Maximum Impulse Voltage	Surge voltage in air, waveform per IEC 61000-4-5	V_{IMP}	6000	V peak
Maximum Surge Isolation Voltage	$V_{TEST} \geq 1.3 \times V_{IMP}$ (sample test), tested in oil, waveform per IEC 61000-4-5	V_{IOSM}	10,000	V peak
Safety Limiting Values	Maximum value allowed in the event of a failure (see Figure 4)			
Case Temperature		T_S	130	°C
Safety Total Dissipated Power		P_S	2.4	W
Insulation Resistance at T_S	V_{IO} = 500 V	R_S	$>10^9$	Ω

SPECIFICATIONS

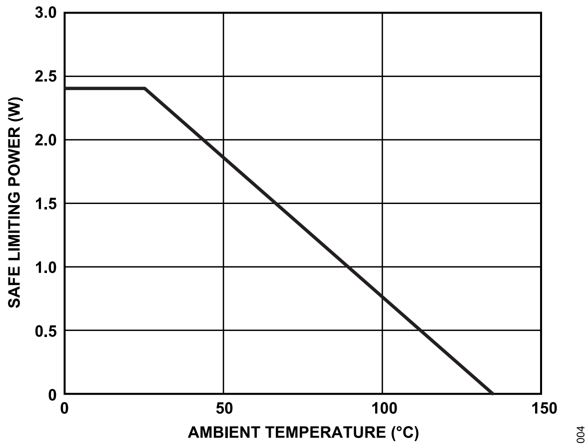


Figure 4. Thermal Derating Curve, Dependence of Safety Limiting Values with Case Temperature per DIN EN IEC 60747-17 (VDE 0884-17)

RECOMMENDED OPERATING CONDITIONS

Table 17.

Parameter	Symbol	Value
Operating Temperature Range	T_A	−40°C to +125°C
Supply Voltage Range[1]	V_{DD1}, V_{DD2}	3.0 V to 5.5 V
Input Signal Rise and Fall Times		1.0 ms

[1] See the DC Correctness and Magnetic Field Immunity section for information on the immunity to the external magnetic fields.

ABSOLUTE MAXIMUM RATINGS

T_A = 25°C, unless otherwise noted.

Table 18.

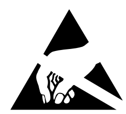
Parameter	Rating
Storage Temperature (T_{ST}) Range	−65°C to +150°C
Ambient Operating Temperature (T_A) Range	−40°C to +125°C
Supply Voltages (V_{DD1}, V_{DD2})	−0.5 V to +7.0 V
Input Voltages (V_{IA}, V_{IB}, V_{IC}, MCLK, MO, SO, $\overline{\text{MSS}}$)	−0.5 V to V_{DDx} + 0.5 V
Output Voltages (SCLK, $\overline{\text{SSS}}$, MI, SI, V_{OA}, V_{OB}, V_{OC})	−0.5 V to V_{DDx} + 0.5 V
Average Current per Output Pin[1]	−10 mA to +10 mA
Common-Mode Transients[2]	−100 kV/µs to +100 kV/µs

[1] See Figure 4 for maximum safety rated current values across temperature.

[2] Refers to common-mode transients across the insulation barrier. Common-mode transients exceeding the absolute maximum ratings may cause latch-up or permanent damage.

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

ESD CAUTION



ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

MAXIMUM CONTINUOUS WORKING VOLTAGE

Table 19. ADuM4151/ADuM4152/ADuM4153 Maximum Continuous Working Voltage

Parameter	Rating	Unit	Applicable Certification
AC Voltage			
Bipolar Waveform	645	V peak	Reinforced insulation rating per IEC 60747-17 (VDE 0884-17)[1]

[1] Maximum continuous working voltage refers to the continuous voltage magnitude imposed across the isolation barrier. See the Insulation Lifetime section for details.

PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS

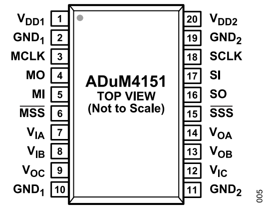


Figure 5. ADuM4151 Pin Configuration

Table 20. ADuM4151 Pin Function Descriptions

Pin No.	Mnemonic	Direction	Description
1	V_{DD1}	Power	Input Power Supply for Isolator Side 1. A bypass capacitor from V_{DD1} to GND_1 to local ground is required.
2, 10	GND_1	Return	Ground 1. Ground reference for Isolator Side 1.
3	MCLK	Input	SPI Clock from the Main Controller.
4	MO	Input	SPI Data from the Main to the Subordinate MO/SI Line.
5	MI	Output	SPI Data from the Subordinate to the Main MI/SO Line.
6	$\overline{MSS}$	Input	Subordinate Select from the Main. This signal uses an active low logic. The subordinate select pin requires a 10 ns setup time from the next clock or data edge.
7	V_{IA}	Input	Low Speed Data Input A.
8	V_{IB}	Input	Low Speed Data Input B.
9	V_{OC}	Output	Low Speed Data Output C.
11, 19	GND2	Return	Ground 2. Ground reference for Isolator Side 2.
12	V_{IC}	Input	Low Speed Data Input C.
13	V_{OB}	Output	Low Speed Data Output B.
14	V_{OA}	Output	Low Speed Data Output A.
15	$\overline{SSS}$	Output	Subordinate Select to the Subordinate. This signal uses an active low logic.
16	SO	Input	SPI Data from the Subordinate to the Main MI/SO Line.
17	SI	Output	SPI Data from the Main to the Subordinate MO/SI Line.
18	SCLK	Output	SPI Clock from the Main Controller.
20	V_{DD2}	Power	Input Power Supply for Isolator Side 2. A bypass capacitor from V_{DD2} to GND_2 to local ground is required.

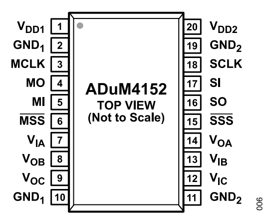


Figure 6. ADuM4152 Pin Configuration

Table 21. ADuM4152 Pin Function Descriptions

Pin No.	Mnemonic	Direction	Description
1	V_{DD1}	Power	Input Power Supply for Isolator Side 1. A bypass capacitor from V_{DD1} to GND_1 to local ground is required.
2, 10	GND_1	Return	Ground 1. Ground reference for Isolator Side 1.
3	MCLK	Input	SPI Clock from the Main Controller.
4	MO	Input	SPI Data from the Main to the Subordinate MO/SI Line.
5	MI	Output	SPI Data from the Subordinate to the Main MI/SO Line.
6	$\overline{MSS}$	Input	Subordinate Select from the Main. This signal uses an active low logic. The subordinate select pin requires a 10 ns setup time from the next clock or data edge.
7	V_{IA}	Input	Low Speed Data Input A.
8	V_{OB}	Output	Low Speed Data Output B.
9	V_{OC}	Output	Low Speed Data Output C.

PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS

Table 21. ADuM4152 Pin Function Descriptions (Continued)

Pin No.	Mnemonic	Direction	Description
11, 19	GND_2	Return	Ground 2. Ground reference for Isolator Side 2.
12	V_{IC}	Input	Low Speed Data Input C.
13	V_{IB}	Input	Low Speed Data Input B.
14	V_{OA}	Output	Low Speed Data Output A.
15	$\overline{SSS}$	Output	Subordinate Select to the Subordinate. This signal uses an active low logic.
16	SO	Input	SPI Data from the Subordinate to the Main MI/SO Line.
17	SI	Output	SPI Data from the Main to the Subordinate MO/SI Line.
18	SCLK	Output	SPI Clock from the Main Controller.
20	V_{DD2}	Power	Input Power Supply for Isolator Side 2. A bypass capacitor from V_{DD2} to GND_2 to local ground is required.

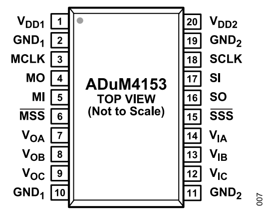


Figure 7. ADuM4153 Pin Configuration

Table 22. ADuM4153 Pin Function Descriptions

Pin No.	Mnemonic	Direction	Description
1	V_{DD1}	Power	Input Power Supply for Isolator Side 1. A bypass capacitor from V_{DD1} to GND_1 to local ground is required.
2, 10	GND_1	Return	Ground 1. Ground reference for Isolator Side 1.
3	MCLK	Input	SPI Clock from the Main Controller.
4	MO	Input	SPI Data from the Main to the Subordinate MO/SI Line
5	MI	Output	SPI Data from the Subordinate to the Main MI/SO Line.
6	$\overline{MSS}$	Input	Subordinate Select from the Main. This signal uses an active low logic. The subordinate select pin requires a 10 ns setup time from the next clock or data edge.
7	V_{OA}	Output	Low Speed Data Output A.
8	V_{OB}	Output	Low Speed Data Output B.
9	V_{OC}	Output	Low Speed Data Output C.
11, 19	GND_2	Return	Ground 1. Ground reference for Isolator Side 2.
12	V_{IC}	Input	Low Speed Data Input C.
13	V_{IB}	Input	Low Speed Data Input B.
14	V_{IA}	Input	Low Speed Data Input A.
15	$\overline{SSS}$	Output	Subordinate Select to the Subordinate. This signal uses an active low logic.
16	SO	Input	SPI Data from the Subordinate to the Main MI/SO Line.
17	SI	Output	SPI Data from the Main to the Subordinate MO/SI Line.
18	SCLK	Output	SPI Clock from the Main Controller.
20	V_{DD2}	Power	Input Power Supply for Isolator Side 2. A bypass capacitor from V_{DD2} to GND_2 to local ground is required.

Table 23. ADuM4151/ADuM4152/ADuM4153 Power-Off Default State Truth Table (Positive Logic)[1]

V_{DD1} State	V_{DD2} State	Side 1 Outputs	Side 2 Outputs	$\overline{SSS}$	Comments
Unpowered	Powered	Z	Z	Z	Outputs on an unpowered side are high impedance within one diode drop of ground
Powered	Unpowered	Z	Z	Z	Outputs on an unpowered side are high impedance within one diode drop of ground

[1] Z is high impedance.

TYPICAL PERFORMANCE CHARACTERISTICS

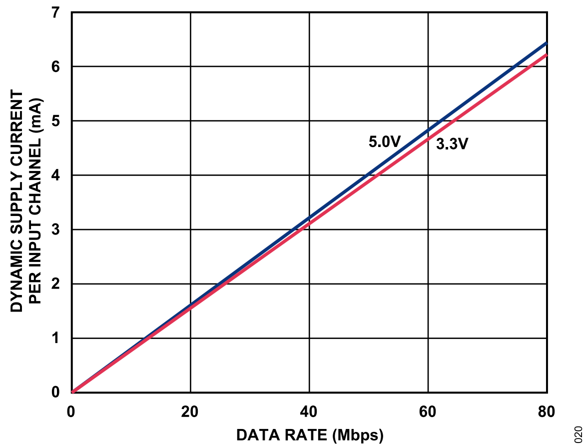


Figure 8. Typical Dynamic Supply Current per Input Channel vs. Data Rate for 5.0 V and 3.3 V Operation

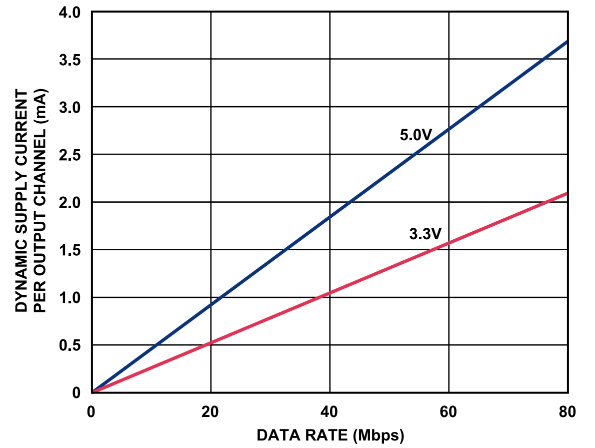


Figure 11. Typical Dynamic Supply Current per Output Channel vs. Data Rate for 5.0 V and 3.3 V Operation

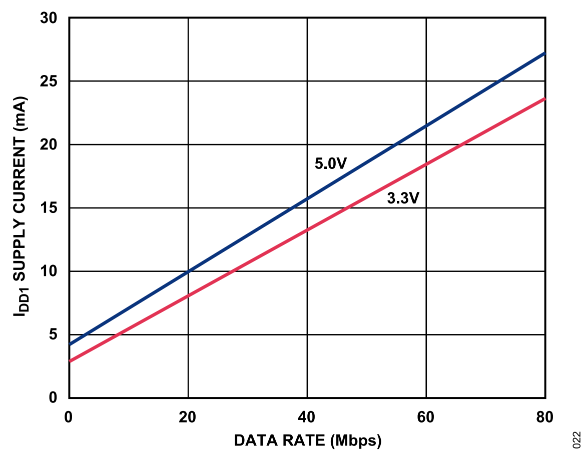


Figure 9. Typical I_{DD1} Supply Current vs. Data Rate for 5.0 V and 3.3 V Operation

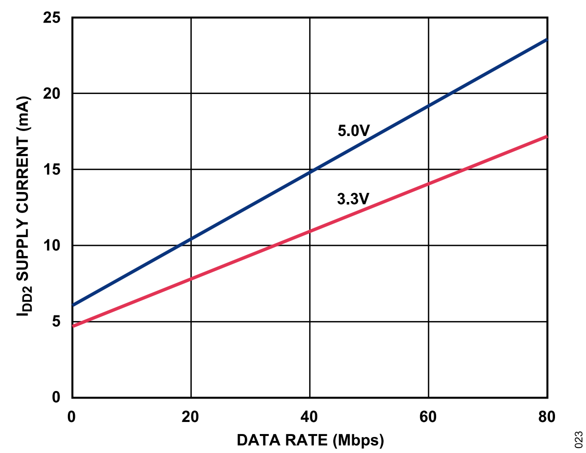


Figure 12. Typical I_{DD2} Supply Current vs. Data Rate for 5.0 V and 3.3 V Operation

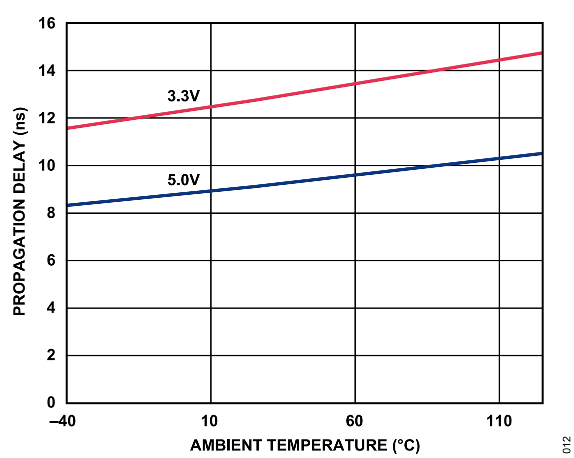


Figure 10. Typical Propagation Delay vs. Ambient Temperature for High Speed Channels Without Glitch Filter (See the High Speed Channels Section)

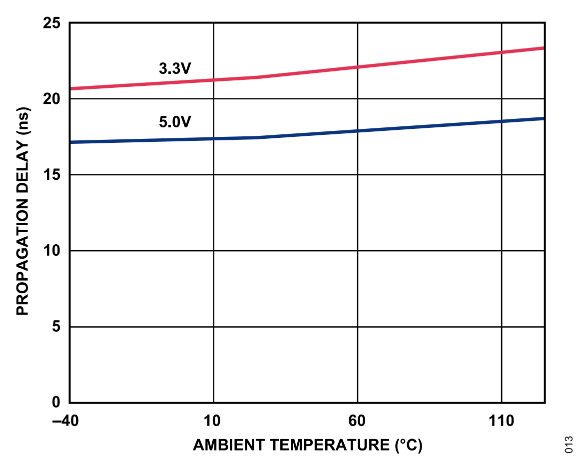


Figure 13. Typical Propagation Delay vs. Ambient Temperature for High Speed Channels with Glitch Filter (See the High Speed Channels Section)

APPLICATIONS INFORMATION

INTRODUCTION

The ADuM4151/ADuM4152/ADuM4153 are a family of devices created to optimize isolation of SPI for speed and to provide additional low speed channels for control and status monitoring functions. The isolators are based on differential signaling *i*Coupler technology for enhanced speed and noise immunity.

High Speed Channels

The ADuM4151/ADuM4152/ADuM4153 have four high speed channels. The first three channels, CLK, MI/SO, and MO/SI (the slash indicates the connection of the particular input and output channel across the isolator), are optimized for either low propagation delay in the B grade or high noise immunity in the A grade. The difference between the grades is the addition of a glitch filter to these three channels in the A grade version, which increases the propagation delay. The B grade version, with a maximum propagation delay of 14 ns, supports a maximum clock rate of 17 MHz in the standard 4-wire SPI. However, because the glitch filter is not present in the B grade version, ensure that spurious glitches of less than 10 ns are not present.

Glitches of less than 10 ns in the B grade devices can cause the missing of the second edge of the glitch. This pulse condition is then seen as a spurious data transition on the output that is corrected by a refresh or the next valid data edge. It is recommended to use the A grade devices in noisy environments.

The relationship between the SPI signal paths and the pin mnemonics of the ADuM4151/ADuM4152/ADuM4153 and the data directions is detailed in Table 24.

Table 24. Pin Mnemonics Correspondence to the SPI Signal Path Names

SPI Signal Path	Main Side 1	Data Direction	Subordinate Side 2
CLK	MCLK	→	SCLK
MO/SI	MO	→	SI
MI/SO	MI	←	SO
$\overline{\text{SS}}$	$\overline{\text{MSS}}$	→	$\overline{\text{SSS}}$

The datapaths are SPI mode agnostic. The CLK and MO/SI SPI datapaths are optimized for propagation delay and channel to channel matching. The MI/SO SPI datapath is optimized for propagation delay. The devices do not synchronize to the clock channels; therefore, there are no constraints on the clock polarity or the timing with respect to the data lines. To allow compatibility with nonstandard SPI interfaces, the MI pin is always active, and does not tristate when the subordinate select is not asserted. This precludes tying several MI lines together without adding a trisate buffer or multiplexor.

$\overline{\text{SS}}$ (subordinate select bar) is typically an active low signal. $\overline{\text{SS}}$ can have many different functions in SPI and SPI like busses. Many of these functions are edge triggered; therefore, the $\overline{\text{SS}}$ path contains a glitch filter in both the A grade and the B grade. The glitch filter prevents short pulses from propagating to the output or causing other errors in operation. The $\overline{\text{MSS}}$ signal requires a 10 ns setup time in the B grade devices prior to the first active clock edge to allow the added propagation time of the glitch filter.

Low Speed Data Channels

The low speed data channels are provided as economical isolated datapaths where timing is not critical. The dc value of all high and low speed inputs on a given side of the devices are sampled simultaneously, packetized and shifted across an isolation coil. The high speed channels are compared for dc accuracy, and the low speed data is transferred to the appropriate low speed outputs. The process is then reversed by reading the inputs on the opposite side of the devices, packetizing them and sending them back for similar processing. The dc correctness data for the high speed channels is handled internally, and the low speed data is clocked to the outputs simultaneously.

A free running internal clock regulates this bidirectional data shuttling. Because data is sampled at discrete times based on this clock, the propagation delay for a low speed channel is between 0.1 µs and 2.6 µs, depending on where the input data edge changes with respect to the internal sample clock.

Figure 14 illustrates the behavior of the low speed channels and the relationship between the codirectional channels.

- Point A: When data is sampled between the input edges of two low speed data inputs, a very narrow gap between edges is increased to the width of the output clock.
- Point B: Data edges that occur on codirectional channels between samples are sampled and simultaneously sent to the outputs, which synchronizes the data edges between the two channels at the outputs.
- Point C: Data pulses that are less than the minimum low speed pulse width may not be transmitted because they may not be sampled.

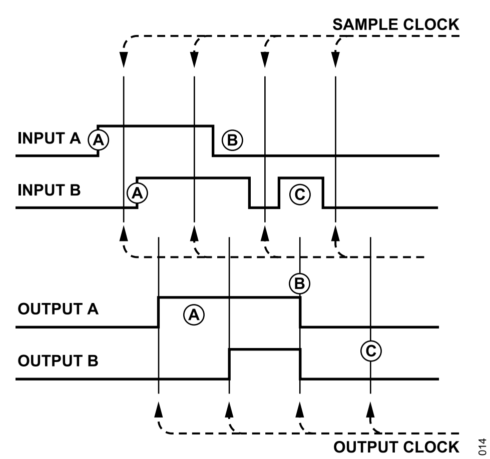


Figure 14. Slow Channel Timing

The low speed data system is carefully designed so that staggered data transitions at the inputs become either synchronized or pushed

APPLICATIONS INFORMATION

apart when they are presented at the output. Edge order is always preserved for as long as the edges are separated by at least $t_{VIx\ SKEW}$. In other words, if one edge is leading another at the input, the order of the edges is not reversed by the isolator.

PRINTED CIRCUIT BOARD (PCB) LAYOUT

The ADuM4151/ADuM4152/ADuM4153 digital isolators require no external interface circuitry for the logic interfaces. Power supply bypassing is strongly recommended at both the V_{DD1} and V_{DD2} supply pins (see Figure 15). The capacitor value must be between 0.01 µF and 0.1 µF. The total lead length between both ends of the capacitor and the input power supply pin must not exceed 20 mm.

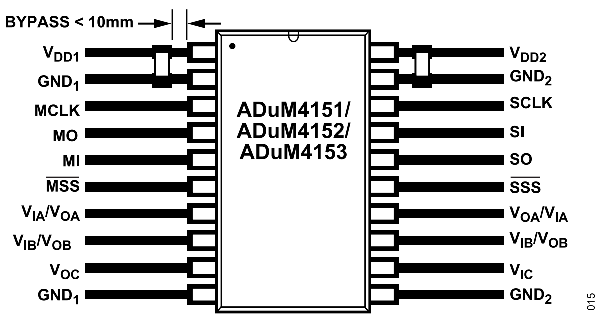


Figure 15. Recommended PCB Layout

In applications involving high common-mode transients, it is important to minimize board coupling across the isolation barrier. Furthermore, design the PCB layout so that any coupling that does occur affects all pins equally on a given component side. Failure to ensure this may cause voltage differentials between pins that exceed the absolute maximum ratings of the device, thereby leading to latch-up or permanent damage.

PROPAGATION DELAY RELATED PARAMETERS

Propagation delay is a parameter that describes the time it takes a logic signal to propagate through a component. The input to output propagation delay time for a high to low transition may differ from the propagation delay time of a low to high transition.

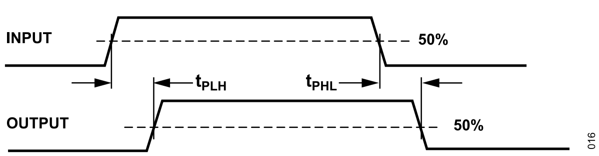


Figure 16. Propagation Delay Parameters

Pulse width distortion is the maximum difference between these two propagation delay values and an indication of how accurately the timing of the input signal is preserved.

Channel to channel matching refers to the maximum amount the propagation delay differs between channels within a single ADuM4151/ADuM4152/ADuM4153 component.

DC CORRECTNESS AND MAGNETIC FIELD IMMUNITY

Positive and negative logic transitions at the isolator input cause narrow (~1 ns) pulses to be sent via the transformer to the decoder. The decoder is bistable and is, therefore, either set or reset by the pulses indicating input logic transitions. In the absence of logic transitions at the input for more than ~1.2 µs, a periodic set of refresh pulses indicative of the correct input state are sent via the low speed channel to ensure dc correctness at the output.

If the low speed decoder receives no pulses for more than about 5 µs, the input side is assumed to be unpowered or nonfunctional, in which case, the isolator output is forced to a high-Z state by the watchdog timer circuit.

The limitation on the magnetic field immunity of the device is set by the condition in which induced voltage in the transformer receiving coil is sufficiently large to either falsely set or reset the decoder. The following analysis defines such conditions. The ADuM4151/ADuM4152/ADuM4153 were examined in a 3 V operating condition because it represents the most susceptible mode of operation for this product.

The pulses at the transformer output have an amplitude greater than 1.5 V. The decoder has a sensing threshold of about 1.0 V; thereby, establishing a 0.5 V margin in which induced voltages can be tolerated. The voltage induced across the receiving coil is given by

$$V = (-d\beta/dt)\sum \pi r_n^2;\ n = 1, 2, \ldots, N \quad (1)$$

where:
β is the magnetic flux density.
r_n is the radius of the n^{th} turn in the receiving coil.
N is the number of turns in the receiving coil.

Given the geometry of the receiving coil in the ADuM4151/ADuM4152/ADuM4153 and an imposed requirement that the induced voltage be, at most, 50% of the 0.5 V margin at the decoder, a maximum allowable magnetic field is calculated as shown in Figure 17.

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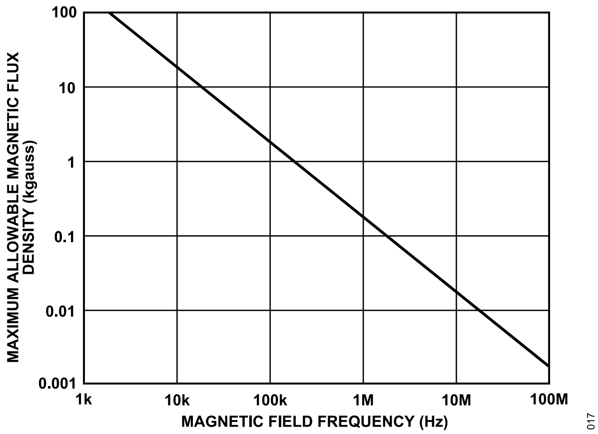

Figure 17. Maximum Allowable External Magnetic Flux Density

For example, at a magnetic field frequency of 1 MHz, the maximum allowable magnetic field of 0.5 kgauss, induces a voltage of 0.25 V at the receiving coil. This voltage is about 50% of the sensing threshold and does not cause a faulty output transition. If such an event occurs, with the worst-case polarity, during a transmitted pulse, the interference reduces the received pulse from >1.0 V to 0.75 V. This voltage is still well above the 0.5 V sensing threshold of the decoder.

The preceding magnetic flux density values correspond to specific current magnitudes at given distances away from the ADuM4151/ADuM4152/ADuM4153 transformers. Figure 18 expresses these allowable current magnitudes as a function of frequency for selected distances. The ADuM4151/ADuM4152/ADuM4153 are insensitive to external fields. Only extremely large, high frequency currents, very close to the component are a concern. For the 1 MHz example noted, placing a 1.2 kA current 5 mm away from the ADuM4151/ADuM4152/ADuM4153 affects component operation.

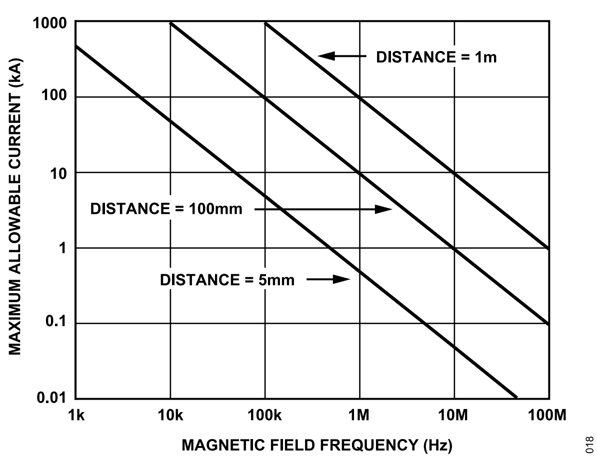

Figure 18. Maximum Allowable Current for Various Current to ADuM4151/ ADuM4152/ADuM4153 Spacings

At combinations of strong magnetic field and high frequency, any loops formed by the PCB traces may induce sufficiently large error voltages to trigger the thresholds of succeeding circuitry. Take care to avoid PCB structures that form loops.

POWER CONSUMPTION

The supply current at a given channel of the ADuM4151/ADuM4152/ADuM4153 isolators is a function of the supply voltage, the data rate of the channel, and the output load of the channel and whether it is a high or low speed channel.

The low speed channels draw a constant quiescent current caused by the internal ping-pong datapath. The operating frequency is low enough that the capacitive losses caused by the recommended capacitive load are negligible compared to the quiescent current. The explicit calculation for the data rate is eliminated for simplicity, and the quiescent current for each side of the isolator due to the low speed channels can be found in Table 3, Table 6, Table 9, and Table 12 for the particular operating voltages.

These quiescent currents add to the high speed current as is shown in the following equations for the total current for each side of the isolator. Dynamic currents are taken from Table 3 and Table 6 for the respective voltages.

For Side 1, the supply current is given by

$$I_{DD1} = I_{DDI(D)} \times (f_{MCLK} + f_{MO} + f\overline{\text{MSS}}) + f_{MI} \times (I_{DDO(D)} + ((0.5 \times 10^{-3}) \times C_{L(MI)} \times V_{DD1})) + I_{DD1(Q)} \quad (2)$$

For Side 2, the supply current is given by

$$I_{DD2} = I_{DDI(D)} \times f_{SO} + f_{SCLK} \times (I_{DDO(D)} + ((0.5 \times 10^{-3}) \times C_{L(SCLK)} \times V_{DD2})) + f_{SI} \times (I_{DDO(D)} + ((0.5 \times 10^{-3}) \times C_{L(SI)} \times V_{DD2})) + f\overline{\text{SSS}} \times (I_{DDO(D)} + ((0.5 \times 10^{-3}) \times C_{L(\overline{\text{SSS}})} \times V_{DD2})) + I_{DD2(Q)} \quad (3)$$

where:

$I_{DDI(D)}$, $I_{DDO(D)}$ are the input and output dynamic supply currents per channel (mA/Mbps).
f_x is the logic signal data rate for the specified channel (Mbps).
$C_{L(x)}$ is the load capacitance of the specified output (pF).
V_{DDx} is the supply voltage of the side being evaluated (V).
$I_{DD1(Q)}$, $I_{DD2(Q)}$ are the specified Side 1 and Side 2 quiescent supply currents (mA).

Figure 8 and Figure 11 show the typical supply current per channel as a function of data rate for an input and unloaded output. Figure 9 and Figure 12 show the total I_{DD1} and I_{DD2} supply currents as a function of data rate for the ADuM4151/ADuM4152/ADuM4153 channel configurations with all high speed channels running at the same speed and the low speed channels at idle.

INSULATION LIFETIME

All insulation structures eventually break down when subjected to voltage stress over a sufficiently long period. The rate of insulation degradation is dependent on the characteristics of the voltage waveform applied across the insulation. In addition to the testing performed by the regulatory agencies, Analog Devices carries out

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an extensive set of evaluations to determine the lifetime of the insulation structure within the ADuM4151/ADuM4152/ADuM4153.

Analog Devices performs accelerated life testing using voltage levels higher than the rated continuous working voltage. Acceleration factors for several operating conditions are determined. These factors allow calculation of the time to failure at the actual working voltage. The values shown in Table 19 summarize the maximum continuous working voltages as per IEC 60747-17. Operation at working voltages higher than the service life voltage listed leads to premature insulation failure.

OUTLINE DIMENSIONS

Package Drawing (Option)	Package Type	Package Description
RI-20-1	SOIC_IC	20-Lead Standard Small Outline Package, with Increased Creepage, Wide Body

For the latest package outline information and land patterns (footprints), go to Package Index.

Updated: January 26, 2024

ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Packing Quantity	Package Option
ADUM4151ARIZ	-40°C to +125°C	20-Lead SOIC (Increased Creepage)		RI-20-1
ADUM4151ARIZ-RL	-40°C to +125°C	20-Lead SOIC (Increased Creepage)	Reel, 1000	RI-20-1
ADUM4151BRIZ	-40°C to +125°C	20-Lead SOIC (Increased Creepage)		RI-20-1
ADUM4151BRIZ-RL	-40°C to +125°C	20-Lead SOIC (Increased Creepage)	Reel, 1000	RI-20-1
ADUM4152ARIZ	-40°C to +125°C	20-Lead SOIC (Increased Creepage)		RI-20-1
ADUM4152ARIZ-RL	-40°C to +125°C	20-Lead SOIC (Increased Creepage)	Reel, 1000	RI-20-1
ADUM4152BRIZ	-40°C to +125°C	20-Lead SOIC (Increased Creepage)		RI-20-1
ADUM4152BRIZ-RL	-40°C to +125°C	20-Lead SOIC (Increased Creepage)	Reel, 1000	RI-20-1
ADUM4153ARIZ	-40°C to +125°C	20-Lead SOIC (Increased Creepage)		RI-20-1
ADUM4153ARIZ-RL	-40°C to +125°C	20-Lead SOIC (Increased Creepage)	Reel, 1000	RI-20-1
ADUM4153BRIZ	-40°C to +125°C	20-Lead SOIC (Increased Creepage)		RI-20-1
ADUM4153BRIZ-RL	-40°C to +125°C	20-Lead SOIC (Increased Creepage)	Reel, 1000	RI-20-1

[1] Z = RoHS Compliant Part.

NUMBER OF INPUTS (V_{DD1} SIDE AND V_{DD2} SIDE), MAXIMUM DATA RATE, MAXIMUM PROPAGATION DELAY, AND ISOLATION RATING OPTIONS

Model[1]	No. of Inputs, V_{DD1} Side	No. of Inputs, V_{DD2} Side	Maximum Data Rate (MHz)	Maximum Propagation Delay, 5 V (ns)	Isolation Rating (V ac)
ADUM4151ARIZ	5	2	1	25	5000
ADUM4151ARIZ-RL	5	2	1	25	5000
ADUM4151BRIZ	5	2	17	14	5000
ADUM4151BRIZ-RL	5	2	17	14	5000
ADUM4152ARIZ	4	3	1	25	5000
ADUM4152ARIZ-RL	4	3	1	25	5000
ADUM4152BRIZ	4	3	17	14	5000
ADUM4152BRIZ-RL	4	3	17	14	5000
ADUM4153ARIZ	3	4	1	25	5000
ADUM4153ARIZ-RL	3	4	1	25	5000
ADUM4153BRIZ	3	4	17	14	5000
ADUM4153BRIZ-RL	3	4	17	14	5000

[1] Z = RoHS Compliant Part.

OUTLINE DIMENSIONS

EVALUATION BOARDS

Model[1, 2, 3]	Package Description
EVAL-ADuM3151Z	Evaluation Board

[1] Z = RoHS Compliant Part.

[2] The EVAL-ADuM3151Z uses a functionally equivalent device for evaluation. The pad layout on the EVAL-ADuM3151Z board does not support the 20-lead SOIC_IC package.

[3] To evaluate the functionality of the alternative low speed channel configurations of the ADuM4152 and the ADuM4153, the user must purchase an ADuM3152 or an ADuM3153 and replace the component on the EVAL-ADuM3151Z evaluation board.