

ADuM1440/ADuM1441/ADuM1442/ADuM1445/ ADuM1446/ADuM1447

Micropower Quad-Channel Digital Isolators

FEATURES

- ▶ Ultralow power operation
 - ▶ 3.3 V operation (typical)
 - ▶ 5.6 μA per channel quiescent current, refresh enabled
 - ▶ 0.3 μA per channel quiescent current, refresh disabled
 - ▶ 148 $\mu\text{A}/\text{Mbps}$ per channel typical dynamic current
 - ▶ 2.5 V operation (typical)
 - ▶ 3.1 μA per channel quiescent current, refresh enabled
 - ▶ 0.1 μA per channel quiescent current, refresh disabled
 - ▶ 117 $\mu\text{A}/\text{Mbps}$ per channel typical dynamic current
- ▶ Small, 16-lead QSOP and 20-Lead SSOP
- ▶ Bidirectional communication
- ▶ Up to 2 Mbps data rate (NRZ)
- ▶ High temperature operation: 125°C
- ▶ High common-mode transient immunity: >25 kV/ μs
- ▶ Safety and regulatory approvals
 - ▶ 16-Lead QSOP package
 - ▶ UL 1577 (VISO = 2500 V rms for 1 minute)
 - ▶ IEC/CSA 60950-1
 - ▶ DIN EN IEC 60747-17 (VDE 0884-17)
 - ▶ VIORM = 565 V peak
 - ▶ 20-Lead SSOP package
 - ▶ UL 1577 (VISO = 3750 V rms for 1 minute)
 - ▶ IEC/EN/CSA 62368-1
 - ▶ IEC/EN/CSA 60601-1
 - ▶ DIN EN IEC 60747-17 (VDE 0884-17)
 - ▶ VIORM = 645 V peak
- ▶ Intrinsic safety
 - ▶ UL, IECEx, CSA ATEX 2813, CSA UKEx 0518
 - ▶ II 1G Ex ia IIC Ga

APPLICATIONS

- ▶ General-purpose, low power multichannel isolation
- ▶ 1 MHz, low power peripheral interface (SPI)
- ▶ 4 mA to 20 mA loop process controls

FUNCTIONAL BLOCK DIAGRAMS

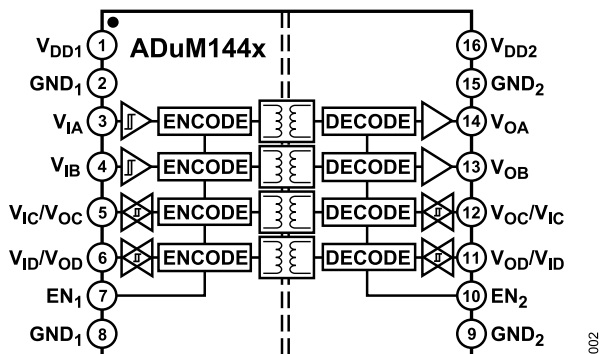


Figure 1. 16-Lead QSOP

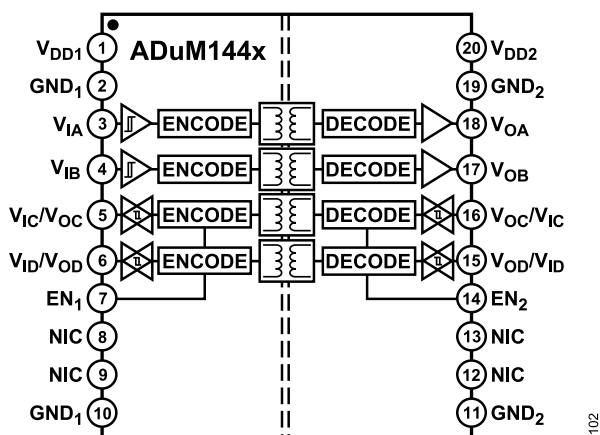


Figure 2. 20-Lead SSOP

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REVISION HISTORY

8/2025—Rev. G to Rev. H

Change to Table 17 and Figure 4 Caption.....	12
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8/2025—Rev. F to Rev. G

Changes to Features Section.....	1
Changes to Figure 1 and Figure 2 Caption.....	1
Moved General Description Section.....	3
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Changes to Regulatory Information Section and Table 12.....	9
Added Table 13; Renumbered Sequentially.....	9
Changes to Table 14.....	10
Changed DIN V VDE V 0884-10 (VDE V 0884-10):2006-12 Insulation Characteristics Section to DIN EN IEC 60747-17 (VDE 0884-17) Insulation Characteristics Section.....	10
Changes to DIN EN IEC 60747-17 (VDE 0884-17) Insulation Characteristics Section, Table 15, and Table 16.....	10
Changes to Intrinsic Safety Section.....	12
Deleted Product Conformity Certificate Section.....	12
Changes to Special Conditions for Safe Use Section, Table 17, Table 18, and Figure 4 Caption.....	12
Changes to Table 19 Title.....	13
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Deleted Table 20; Renumbered Sequentially.....	14
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Deleted Insulation Lifetime Section, Figure 34, Figure 35, and Figure 36; Renumbered Sequentially.....	23
Changes to Ordering Guide.....	24
Added Number of Inputs, V_{DD1} Side, Number of Inputs, V_{DD2} Side, Maximum Data Rate (Mbps), Default Output State, and Maximum Propagation Delay, 3.3 V (ns) Options.....	25

GENERAL DESCRIPTION

The ADuM1440/ADuM1441/ADuM1442/ADuM1445/ADuM1446/ADuM1447¹ are micropower, 4-channel digital isolators based on the Analog Devices, Inc., *iCoupler*® technology. Combining high speed, complementary metal oxide semiconductor (CMOS) and monolithic air core transformer technologies, these isolation components provide outstanding performance characteristics superior to the alternatives, such as optocoupler devices. As shown in Figure 3, in standard operating mode, when $EN_x = 0$ (internal refresh enabled), the current per channel is less than 10 μA . When $EN_x = 1$ (internal refresh disabled), the current per channel drops to less than 1 μA .

The ADuM1440/ADuM1441/ADuM1442/ADuM1445/ADuM1446/ADuM1447 family of quad 2.5 kV digital isolation devices are packaged in a small 16-lead QSOP and 20-lead SSOP, freeing almost 70% of board space compared to isolators packages in wide body SOIC packages.

The devices withstand high isolation voltages and meet regulatory requirements, such as UL and CSA standards. In addition to the space savings, the ADuM1440/ADuM1441/ADuM1442/ADuM1445/ADuM1446/ADuM1447 operate with supplies as low as 2.25 V.

Despite the low power consumption, all models of the ADuM1440/ADuM1441/ADuM1442/ADuM1445/ADuM1446/ADuM1447 provide low, pulse width distortion at <8 ns. In addition, every model has an input glitch filter to protect against extraneous noise disturbances.

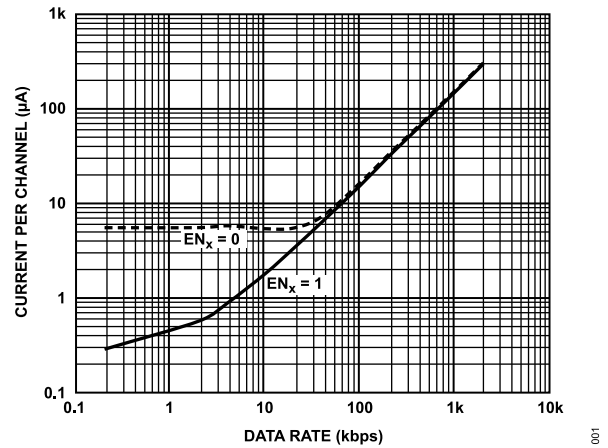


Figure 3. Typical Total Supply Current per Channel ($V_{DDX} = 3.3 \text{ V}$)

¹ Protected by U.S. Patents 5,952,849, 6,873,065, 7,075,329, 6,262,600. Other patents pending.

SPECIFICATIONS

ELECTRICAL CHARACTERISTICS—3.3 V OPERATION

All typical specifications are at $T_A = 25^\circ\text{C}$, $V_{DD1} = V_{DD2} = 3.3\text{ V}$. Minimum/maximum specifications apply over the entire recommended operating range of $3.0\text{ V} \leq V_{DD1} \leq 3.6\text{ V}$, $3.0\text{ V} \leq V_{DD2} \leq 3.6\text{ V}$, and $-40^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$, unless otherwise noted. Switching specifications are tested with $C_L = 15\text{ pF}$, and CMOS signal levels, unless otherwise noted.

Table 1.

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
SWITCHING SPECIFICATIONS						
Data Rate				2	Mbps	Within pulse-width distortion (PWD) limit
Propagation Delay	t_{PHL} , t_{PLH}		80	180	ns	50% input to 50% output
Change vs. Temperature			200		ps/°C	
Minimum Pulse Width	PW	500			ns	Within PWD limit
Pulse-Width Distortion	PWD			8	ns	$ t_{PLH} - t_{PHL} $
Propagation Delay Skew ¹	t_{PSK}			10	ns	
Channel Matching						
Codirectional	t_{PSKCD}			10	ns	
Opposing Direction	t_{PSKOD}			15	ns	

¹ t_{PSK} is the magnitude of the worst-case difference in t_{PHL} and t_{PLH} that is measured between units at the same operating temperature, supply voltages, and output load within the recommended operating conditions.

Table 2.

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
SUPPLY CURRENT						
ADuM1440/ADuM1445	I_{DD1}		732	1000	μA	2 Mbps, no load $EN_X = 0\text{ V}$, $V_{IH} = V_{DD}$, $V_{IL} = 0\text{ V}$
	I_{DD2}		492	750	μA	$EN_X = 0\text{ V}$, $V_{IH} = V_{DD}$, $V_{IL} = 0\text{ V}$
ADuM1441/ADuM1446	I_{DD1}		672	900	μA	$EN_X = 0\text{ V}$, $V_{IH} = V_{DD}$, $V_{IL} = 0\text{ V}$
	I_{DD2}		552	900	μA	$EN_X = 0\text{ V}$, $V_{IH} = V_{DD}$, $V_{IL} = 0\text{ V}$
ADuM1442/ADuM1447	I_{DD1}		612	900	μA	$EN_X = 0\text{ V}$, $V_{IH} = V_{DD}$, $V_{IL} = 0\text{ V}$
	I_{DD2}		612	900	μA	$EN_X = 0\text{ V}$, $V_{IH} = V_{DD}$, $V_{IL} = 0\text{ V}$

Table 3. For All Models

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
DC SPECIFICATIONS						
Input Threshold						

SPECIFICATIONS

Table 3. For All Models (Continued)

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
Quiescent Current						
Input Supply	$I_{DD1}(Q)$		4.8	10	μA	EN_X low
Output Supply	$I_{DDO}(Q)$		0.8	3.3	μA	EN_X low
Input (Refresh Off)	$I_{DD1}(Q)$		0.12		μA	EN_X high
Output (Refresh Off)	$I_{DDO}(Q)$		0.13		μA	EN_X high
Dynamic Supply Current						
Input	$I_{DD1}(D)$		88		$\mu A/Mbps$	
Output	$I_{DDO}(D)$		60		$\mu A/Mbps$	
AC SPECIFICATIONS						
Output Rise Time/Fall Time	t_R/t_F		2		ns	10% to 90%
Common-Mode Transient Immunity ²	$ CM $	25	40		kV/ μs	$V_{IX} = V_{DDX}$ ¹ , $V_{CM} = 1000$ V, transient magnitude = 800 V
Refresh Rate	f_r		14		kbps	

¹ $V_{DDX} = V_{DD1}$ or V_{DD2} .

² $|CM|$ is the maximum common-mode voltage slew rate that can be sustained while maintaining $V_{OUT} > 0.8 V_{DDX}$. The common-mode voltage slew rates apply to both rising and falling common-mode voltage edges.

ELECTRICAL CHARACTERISTICS—2.5 V OPERATION

All typical specifications are at $T_A = 25^\circ C$, $V_{DD1} = V_{DD2} = 2.5$ V. Minimum/maximum specifications apply over the entire recommended operating range of $2.25\text{ V} \leq V_{DD1} \leq 2.75\text{ V}$, $2.25\text{ V} \leq V_{DD2} \leq 2.75\text{ V}$, and $-40^\circ C \leq T_A \leq +125^\circ C$, unless otherwise noted. Switching specifications are tested with $C_L = 15$ pF, and CMOS signal levels, unless otherwise noted.

Table 4.

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
SWITCHING SPECIFICATIONS						
Data Rate			2		Mbps	Within PWD limit
Propagation Delay	t_{PHL}, t_{PLH}		112	180	ns	50% input to 50% output
Change vs. Temperature			280		ps/ $^\circ C$	
Pulse-Width Distortion	PWD			12	ns	$ t_{PLH} - t_{PHL} $
Minimum Pulse Width	PW	500			ns	Within PWD limit
Propagation Delay Skew ¹	t_{PSK}			10	ns	
Channel Matching						
Codirectional	t_{PSKCD}			10	ns	
Opposing Direction	t_{PSKOD}			30	ns	

¹ t_{PSK} is the magnitude of the worst-case difference in t_{PHL} or t_{PLH} that is measured between units at the same operating temperature, supply voltages, and output load within the recommended operating conditions.

ADuM1440/ADuM1441/ADuM1442/ADuM1445/ ADuM1446/ADuM1447

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SPECIFICATIONS

Table 5.

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
SUPPLY CURRENT						2 Mbps, no load
ADuM1440/ADuM1445	I_{DD1}		623	800	μA	$\text{EN}_X = 0\text{ V}$, $V_{IH} = V_{DD}$, $V_{IL} = 0\text{ V}$
	I_{DD2}		337	500	μA	$\text{EN}_X = 0\text{ V}$, $V_{IH} = V_{DD}$, $V_{IL} = 0\text{ V}$
ADuM1441/ADuM1446	I_{DD1}		552	750	μA	$\text{EN}_X = 0\text{ V}$, $V_{IH} = V_{DD}$, $V_{IL} = 0\text{ V}$
	I_{DD2}		409	750	μA	$\text{EN}_X = 0\text{ V}$, $V_{IH} = V_{DD}$, $V_{IL} = 0\text{ V}$
ADuM1442/ADuM1447	I_{DD1}		480	750	μA	$\text{EN}_X = 0\text{ V}$, $V_{IH} = V_{DD}$, $V_{IL} = 0\text{ V}$
	I_{DD2}		480	750	μA	$\text{EN}_X = 0\text{ V}$, $V_{IH} = V_{DD}$, $V_{IL} = 0\text{ V}$

Table 6. For All Models

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
DC SPECIFICATIONS						
Input Threshold						
Logic High	V_{IH}	$0.7 V_{DDX}^1$			V	
Logic Low	V_{IL}			$0.3 V_{DDX}^1$	V	
Output Voltages						
Logic High	V_{OH}	$V_{DDX}^1 - 0.1$	2.5		V	$I_{OX} = -20\text{ }\mu\text{A}$, $V_{IX} = V_{IXH}$
		$V_{DDX}^1 - 0.4$	2.35		V	$I_{OX} = -4\text{ mA}$, $V_{IX} = V_{IXH}$
Logic Low	V_{OL}		0.0	0.1	V	$I_{OX} = 20\text{ }\mu\text{A}$, $V_{IX} = V_{IXL}$
			0.1	0.4	V	$I_{OX} = 4\text{ mA}$, $V_{IX} = V_{IXL}$
Input Current per Channel	I_I	-1	+0.01	+1	μA	$0\text{ V} \leq V_{IX} \leq V_{DDX}^1$
Input Switching Thresholds						
Positive Threshold Voltage	V_{T+}		1.5		V	
Negative Going Threshold	V_{T-}		1.0		V	
Input Hysteresis	ΔV_T		0.5		V	
Undervoltage Lockout, V_{DD1} or V_{DD2}	UVLO		1.5		V	
Supply Current per Channel						
Quiescent Current						
Input Supply	$I_{DDI}(Q)$		2.6	3.3	μA	EN_X low
Output Supply	$I_{DDO}(Q)$		0.5	1.8	μA	$\text{EN}_X</$

SPECIFICATIONS

ELECTRICAL CHARACTERISTICS— $V_{DD1} = 3.3\text{ V}$, $V_{DD2} = 2.5\text{ V}$ OPERATION

All typical specifications are at $T_A = 25^\circ\text{C}$, $V_{DD1} = 3.3\text{ V}$, and $V_{DD2} = 2.5\text{ V}$. Minimum/maximum specifications apply over the entire recommended operating range of $3.0\text{ V} \leq V_{DD1} \leq 3.6\text{ V}$, $2.25\text{ V} \leq V_{DD2} \leq 2.75\text{ V}$, and $-40^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$, unless otherwise noted. Switching specifications are tested with $C_L = 15\text{ pF}$, and CMOS signal levels, unless otherwise noted.

For dc specifications and ac specifications, see [Table 3](#) for Side 1 and see [Table 6](#) for Side 2.

Table 7.

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
SWITCHING SPECIFICATIONS						
Data Rate				2	Mbps	Within PWD limit
Propagation Delay						
Side 1 to Side 2	t_{PHL}, t_{PLH}		84	180	ns	50% input to 50% output
Side 2 to Side 1	t_{PHL}, t_{PLH}		120	180	ns	50% input to 50% output
Change vs. Temperature			280		ps/ $^\circ\text{C}$	
Pulse-Width Distortion	PWD			12	ns	$ t_{PLH} - t_{PHL} $
Pulse Width	PW	500			ns	Within PWD limit
Propagation Delay Skew ¹	t_{PSK}			10	ns	
Channel Matching						
Codirectional	t_{PSKCD}			10	ns	
Opposing Direction	t_{PSKOD}			60	ns	

¹ t_{PSK} is the magnitude of the worst-case difference in t_{PHL} or t_{PLH} that is measured between units at the same operating temperature, supply voltages, and output load within the recommended operating conditions.

Table 8.

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
SUPPLY CURRENT						
ADuM1440/ADuM1445	I_{DD1}	732	1000		μA	2 Mbps, no load $EN_X = 0\text{ V}$, $V_{IH} = V_{DD}$, $V_{IL} = 0\text{ V}$
	I_{DD2}	337	750		μA	$EN_X = 0\text{ V}$, $V_{IH} = V_{DD}$, $V_{IL} = 0\text{ V}$
ADuM1441/ADuM1446	I_{DD1}	672	900		μA	$EN_X = 0\text{ V}$, $V_{IH} = V_{DD}$, $V_{IL} = 0\text{ V}$
	I_{DD2}	409	750		μA	$EN_X = 0\text{ V}$, $V_{IH} = V_{DD}$, $V_{IL} = 0\text{ V}$
ADuM1442/ADuM1447	I_{DD1}	612	900		μA	$EN_X = 0\text{ V}$, $V_{IH} = V_{DD}$, $V_{IL} = 0\text{ V}$

ADuM1440/ADuM1441/ADuM1442/ADuM1445/ ADuM1446/ADuM1447

Data Sheet

SPECIFICATIONS

Table 9. (Continued)

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
Pulse-Width Distortion	PWD			12	ns	$ t_{PLH} - t_{PHL} $
Pulse Width	PW	500			ns	Within PWD limit
Propagation Delay Skew ¹	t_{PSK}			10	ns	
Channel Matching						
Codirectional	t_{PSKCD}			10	ns	
Opposing Direction	t_{PSKOD}			60	ns	

¹ t_{PSK} is the magnitude of the worst-case difference in t_{PHL} or t_{PLH} that is measured between units at the same operating temperature, supply voltages, and output load within the recommended operating conditions.

Table 10.

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
SUPPLY CURRENT						2 Mbps, no load
ADuM1440/ADuM1445	I_{DD1}	623	1000		μA	$EN_X = 0 V, V_{IH} = V_{DD}, V_{IL} = 0 V$
	I_{DD2}	492	750		μA	$EN_X = 0 V, V_{IH} = V_{DD}, V_{IL} = 0 V$
ADuM1441/ADuM1446	I_{DD1}	552	750		μA	$EN_X = 0 V, V_{IH} = V_{DD}, V_{IL} = 0 V$
	I_{DD2}	552	900		μA	$EN_X = 0 V, V_{IH} = V_{DD}, V_{IL} = 0 V$
ADuM1442/ADuM1447	I_{DD1}	480	750		μA	$EN_X = 0 V, V_{IH} = V_{DD}, V_{IL} = 0 V$
	I_{DD2}	612	900		μA	$EN_X = 0 V, V_{IH} = V_{DD}, V_{IL} = 0 V$

PACKAGE CHARACTERISTICS

Table 11.

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
Resistance (Input-to-Output) ¹	R_{I-O}		10^{13}		Ω	
Capacitance (Input-to-Output) ¹	C_{I-O}		2		pF	$f = 1 \text{ MHz}$
Input Capacitance ²	C_I		4.0		pF	
IC Junction-to-Ambient Thermal Resistance (QSOP)	θ_{JA}		76		$^{\circ}C/W$	Thermocouple located at center of package underside
IC Junction-to-Ambient Thermal Resistance (SSOP)	θ_{JA}		50.5		$^{\circ}C/W$	Thermocouple located at center of package underside

¹ The device is considered a 2-terminal device: Pin 1 through Pin 8 are shorted together, and Pin 9 through Pin 16 are shorted together.

² Input capacitance is from any input data pin to ground.

SPECIFICATIONS

REGULATORY INFORMATION

The ADuM1440/ADuM1441/ADuM1442/ADuM1445/ADuM1446/ADuM1447 have been approved by the organizations listed below. Certifications are available at [Safety and Regulatory Certification for Digital Isolation](#). IECEx certificates of conformity are available at www.iecex.com.

Table 12. Safety Certifications for RQ-16 Package

UL	CSA	VDE	CSA/Sira
UL 1577 ¹ Single Protection, 2500 Vrms File E214100 UL 913, UL/CSA 60079-0, UL/CSA 60079-11 Class I, Division 1, Groups A, B, C and D Class I, Zone 0, AEx ia IIC File E516634	CSA IEC/CSA 60950-1 Basic Insulation, 320 Vrms File Number 205078	DIN EN IEC 60747-17 (VDE 0884-17) ² Reinforced insulation, 565 V _{PEAK} Certificate No. 40011599	IEC/EN 60079-0, IEC/EN 60079-11 II 1G Ex ia IIC Ga Certificate No. IECEx SIR 16.0091U, CSAE 23UKEX1056U, Sira 16ATEX2265U

¹ In accordance with UL 1577, each ADuM1440/ADuM1441/ADuM1442/ADuM1445/ADuM1446/ADuM1447 RQ-16 is proof tested by applying an insulation test voltage and measuring leakage during final production testing. QSOP package devices are tested at ≥3000 V rms for 1 sec with a current leakage detection limit = 5 μA. SSOP package devices are tested at ≥4500 V rms for 1 sec with a current leakage detection limit = 10 μA.

² In accordance with DIN EN IEC 60747-17 (VDE 0884-17) each ADuM1440/ADuM1441/ADuM1442/ADuM1445/ADuM1446/ADuM1447 is proof tested by applying an insulation test voltage ≥1059 V_{peak} for 1 second (partial discharge detection limit = 5 pC). The asterisk (*) marked on the component designates DIN V VDE V 0884-17 approval.

Table 13. Safety Certifications for RS-20 Package

UL	CSA	VDE	CSA/Sira
UL1577 ¹ Single Protection, 3750 Vrms File E214100 UL 913, UL/CSA 60079-0, UL/CSA 60079-11 Class I, Division 1, Groups A, B, C, and D Class I, Zone 0, AEx ia IIC File E516634	IIEC/EN/CSA 62368-1 Basic insulation, 510 Vrms Reinforced insulation, 255 Vrms IEC/CSA 60601-1 Basic insulation (1 MOPP), 250 Vrms File Number 205078	DIN EN IEC 60747-17 (VDE 0884-17) ² Reinforced insulation, 645 V _{peak} Certificate No. 40011599	IEC/EN 60079-0, IEC/EN 60079-11 II 1G Ex ia IIC Ga Certificate No. IECEx SIR 16.0091U, CSAE 23UKEX1056U, Sira 16ATEX2265U

¹ In accordance with UL 1577, each ADuM1440/ADuM1441/ADuM1442/ADuM1445/ADuM1446/ADuM1447 RS-20 is proof tested by applying an insulation test voltage ≥ 4500 V rms for 1 sec with a current leakage detection limit = 5 μA.

² In accordance with DIN EN IEC 60747-17 (VDE 0884-17) each ADuM1440/ADuM1441/ADuM1442/ADuM1445/ADuM1446/ADuM1447 is proof tested by applying an insulation test voltage ≥1209 V_{peak} for 1 second (partial discharge detection limit = 5 pC). The asterisk (*) marked on the component designates DIN V VDE V 0884-17 approval.

SPECIFICATIONS

INSULATION AND SAFETY RELATED SPECIFICATIONS

Table 14.

Parameter	Symbol	Value	Unit	Test Conditions/Comments
Rated Dielectric Insulation Voltage (RQ-16)		2500	V rms	1-minute duration
Rated Dielectric Insulation Voltage (RS-20)		3750	V rms	1-minute duration
Minimum External Tracking and Air Gap, RQ-16 (Creepage and Clearance) 1, 2	L(I02)	3.2	mm	Measured from input terminals to output terminals, shortest distance path along package body
Minimum Clearance in the Plane of the Printed Circuit Board, RQ-16 (PCB Clearance)	L(I01)	3.8	mm	Measured from input terminals to output terminals, shortest distance through air, line of sight, in the PCB mounting plane
Minimum External Tracking and Air Gap, RS-20 (Creepage and Clearance) 3, 4	L(I01)	5.1	mm	Measured from input terminals to output terminals, shortest distance path along package body
Minimum Clearance in the Plane of the Printed Circuit Board, RS-20 (PCB Clearance)	L(I02)	5.1	mm	Measured from input terminals to output terminals, shortest distance through air, line of sight, in the PCB mounting plane
Minimum Internal Gap (Internal Clearance)		18	μm	Insulation distance through insulation
Tracking Resistance (Comparative Tracking Index)	CTI	>400	V	DIN IEC 112/VDE 0303 Part 1
Material Group		II		Material Group (DIN VDE 0110, 1/89, Table 1)

¹ In accordance with IEC 60950-1 guidelines for the measurement of creepage and clearance distances for a pollution degree of 2 and altitudes ≤2000 m.

² Consideration must be given to pad layout to ensure the minimum required distance for clearance is maintained.

³ In accordance with IEC 62368-1/IEC 60601-1 guidelines for the measurement of creepage and clearance distances for a pollution degree of 2 and altitudes ≤2000 m

⁴ Consideration must be given to pad layout to ensure the minimum required distance for clearance is maintained.

DIN EN IEC 60747-17 (VDE 0884-17) INSULATION CHARACTERISTICS

These isolators are suitable for safe electrical isolation only within the safety limiting ratings. Compliance with the safety limiting ratings shall be ensured by means of suitable protective circuits. The asterisk (*) marked on packages denotes DIN EN IEC 60747-17 (VDE 0884-17) approval.

Table 15. 16-Lead QSOP (RQ-16)

Description	Test Conditions/Comments	Symbol	Characteristic	Unit
Installation Classification per DIN VDE 0110 For Rated Mains Voltage ≤ 150 V rms For Rated Mains Voltage ≤ 300 V rms			I to IV I to III	
Climatic Classification			40/125/21	
Pollution Degree per DIN VDE 0110, Table 1			2	
Maximum Repetitive Isolation Voltage		V _{IORM}	565	V _{PEAK}
Maximum Working Insulation Voltage		V _{IOWM}	400	V _{RMS}
Input-to-Output Test Voltage, Method b1	V _{IORM} × 1.875 = V _{pd(m)} , 100% production test, t _{ini} = t _m = 1 sec, partial discharge < 5 pC	V _{pd(m)}	1059	V _{PEAK}
Input-to-Output Test Voltage, Method a After Environmental Tests Subgroup 1	V _{IORM} × 1.5 = V _{pd(m)} , t _{ini} = 60 sec, t _m = 10 sec, partial discharge < 5 pC	V _{pd(m)}	904	V _{PEAK}
After Input and/or Safety Test Subgroup 2 and Subgroup 3	V _{IORM} × 1.2 = V _{pd(m)} , t _{ini} = 60 sec, t _m = 10 sec, partial discharge < 5 pC	V _{pd(m)}	678	V _{PEAK}
Maximum Transient Isolation Voltage	V _{TEST} = 1.2 × V _{IOTM} , t = 1 sec (100% production)	V _{IOTM}	4000	V _{PEAK} </

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Table 15. 16-Lead QSOP (RQ-16) (Continued)

Description	Test Conditions/Comments	Symbol	Characteristic	Unit
Case Temperature		T_S	150	°C
Total Power Dissipation at 25°C		I_{S1}	1.64	W
Insulation Resistance at T_S	$V_{IO} = 500\text{ V}$	R_S	$>10^9$	Ω

Table 16. 20-Lead SSOP (RS-20)

Description	Conditions	Symbol	Characteristic	Unit
Installation Classification per DIN VDE 0110			I to IV	
For Rated Mains Voltage $\leq 150\text{ V rms}$			I to IV	
For Rated Mains Voltage $\leq 300\text{ V rms}$			I to III	
For Rated Mains Voltage $\leq 400\text{ V rms}$			40/125/21	
Climatic Classification			2	
Pollution Degree per DIN VDE 0110, Table 1				
Maximum Repetitive Isolation Voltage		V_{IORM}	645	V_{PEAK}
Maximum Working Isolation Voltage		V_{IOWM}	456	V_{RMS}
Input-to-Output Test Voltage, Method b1	$V_{IORM} \times 1.875 = V_{pd(m)}$, 100% production test, $t_{ini} = t_m = 1\text{ sec}$, partial discharge $< 5\text{ pC}$	$V_{pd(m)}$	1209	V_{PEAK}
Input-to-Output Test Voltage, Method a				
After Environmental Tests Subgroup 1	$V_{IORM} \times 1.5 = V_{pd(m)}$, $t_{ini} = 60\text{ sec}$, $t_m = 10\text{ sec}$, partial discharge $< 5\text{ pC}$	$V_{pd(m)}$	1032	V_{PEAK}
After Input and/or Safety Test Subgroup 2 and Subgroup 3	$V_{IORM} \times 1.2 = V_{pd(m)}$, $t_{ini} = 60\text{ sec}$, $t_m = 10\text{ sec}$, partial discharge $< 5\text{ pC}$	$V_{pd(m)}$	774	V_{PEAK}
Maximum Transient Isolation Voltage	$V_{TEST} = 1.2 \times VIOTM$, $t = 1\text{ sec}$ (100% production)	V_{IOTM}	6000	V_{PEAK}
Maximum Surge-Isolation Voltage	$V_{TEST} \geq 1.3 \times VIMP$ (sample test), tested in oil, waveform per IEC 6100-4-5	V_{IOSM}	10000	V_{PEAK}
Maximum Impulse Voltage	Surge voltage in air, waveform per IEC 61000-4-5	V_{IMP}	6000	V_{PEAK}
Safety Limiting Values	Maximum value allowed in the event of a failure (see Figure 4)			
Case Temperature		T_S	150	°C
Total Power Dissipation at 25°C		I_{S1}	2.5	W
Insulation Resistance at T_S	$V_{IO} = 500\text{ V}$	R_S	$>10^9$	Ω

SPECIFICATIONS

INTRINSIC SAFETY

The ADuM1440/ADuM1441/ADuM1442/ADuM1445/ADuM1446/ADuM1447 support intrinsic safety for IS to IS and non IS to IS applications under IEC 60079-11:2023 and carry ATEX, UKEX, and IECEx certifications for IS to IS applications.

Special Conditions for Safe Use

These components are certified to comply with IEC 60079-11:2023. When one of these components is used in equipment, the component is to be fitted on a PCB inside a suitable enclosure and recertified as equipment. The creepage and clearance distances across the isolating component have been evaluated, but the distances to other circuitry remain the responsibility of the user of the certified equipment.

This assembly is an isolating component between separate intrinsically safe circuits. It is recommended that the assembly be connected to suitably certified intrinsically safe circuits considering the entity parameters in [Table 17](#).

Table 17. IS to IS Entity Parameters

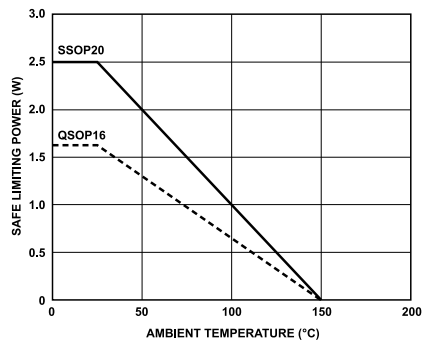
Package Type	Entity Parameters Side 1 ¹	Entity Parameters Side 2	Maximum Operating Range ²
16-Lead QSOP	$U_i = 42\text{ V}$, $I_i = 275\text{ mA}$, $P_i = 1.3\text{ W}$, $L_i = 0$, $C_i = 4\text{ pF}$	$U_i = 42\text{ V}$, $I_i = 275\text{ mA}$, $P_i = 1.3\text{ W}$, $L_i = 0$, $C_i = 4\text{ pF}$	-40°C to +85°C
16-Lead QSOP	$U_i = 42\text{ V}$, $I_i = 275\text{ mA}$, $P_i = 1.0\text{ W}$, $L_i = 0$, $C_i = 4\text{ pF}$	$U_i = 42\text{ V}$, $I_i = 275\text{ mA}$, $P_i = 1.0\text{ W}$, $L_i = 0$, $C_i = 4\text{ pF}$	-40°C to +125°C
20-Lead SSOP	$U_i = 42\text{ V}$, $I_i = 275\text{ mA}$, $P_i = 1.3\text{ W}$, $L_i = 0$, $C_i = 4\text{ pF}$	$U_i = 42\text{ V}$, $I_i = 275\text{ mA}$, $P_i = 1.3\text{ W}$, $L_i = 0$, $C_i = 4\text{ pF}$	-40°C to +85°C
20-Lead SSOP	$U_i = 42\text{ V}$, $I_i = 275\text{ mA}$, $P_i = 1.0\text{ W}$, $L_i = 0$, $C_i = 4\text{ pF}$	$U_i = 42\text{ V}$, $I_i = 275\text{ mA}$, $P_i = 1.0\text{ W}$, $L_i = 0$, $C_i = 4\text{ pF}$	-40°C to +125°C

¹ L_i is defined as input inductance, C_i is input capacitance, P_i is input power, U_i is input voltage, and I_i is input current.

² Low temperature operation limited by electrical characteristic specifications.

Table 18. Temperature Class Information

Package Type	Maximum Power Side 1 (W)	Maximum Power Side 2 (W)	Maximum Component Temperature (°C)	Ambient Temperature (°C)
16-Lead QSOP	1.3	1.3	189.8	-40°C to +85°C
16-Lead QSOP	1.0	1.0	214.3	-40°C to +125°C
20-Lead SSOP	1.3	1.3	218	-40°C to +85°C
20-Lead SSOP	1.0	1.0	200	-40°C to +125°C



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Recommended Operating Conditions

Table 19. Recommended Operating Conditions

Parameter	Symbol	Value
Operating Temperature	T_A	-40°C to +125°C
Supply Voltages ¹	V_{DD1} , V_{DD2}	2.25 V to 3.6 V
Input Signal Rise and Fall Times		1.0 ms

¹ All voltages are relative to their respective grounds. See the [DC Correctness](#) section for information on immunity to external magnetic fields.

ABSOLUTE MAXIMUM RATINGS

$T_A = 25^\circ\text{C}$, unless otherwise noted.

Table 20. Absolute Maximum Ratings

Parameter	Rating
Supply Voltages (V_{DD1} , V_{DD2})	-0.5 V to +5 V
Input Voltages (V_{IA} , V_{IB})	-0.5 V to $V_{DD1} + 0.5$ V
Output Voltages (V_{OA} , V_{OB})	-0.5 V to $V_{DD2} + 0.5$ V
Average Output Current per Pin ¹	
Side 1 (I_{O1})	-10 mA to +10 mA
Side 2 (I_{O2})	-10 mA to +10 mA
Common-Mode Transients ²	-100 kV/ μs to +100 kV/ μs
Storage Temperature (T_{ST}) Range	-65°C to +150°C
Ambient Operating Temperature(T_A) Range	-40°C to +125°C

¹ See Figure 4 for maximum safety power values for various temperatures.

² Refers to common-mode transients across the insulation barrier. Common-mode transients exceeding the absolute maximum ratings can cause latch-up or permanent damage.

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

TRUTH TABLE

Table 21. Truth Table (Positive Logic) for all Models

V_{IX} Input ^{1,2}	V_{DDI} State ³	V_{DDO} State ⁴	EN_X Input ¹	V_{OX} Output ¹	Description
H	Powered	Powered	L	H	Normal operation; data is high and refresh is enabled.
L	Powered	Powered	L	L	Normal operation; data is low and refresh is enabled.
H	Powered	Powered	H	H	Output is high, and refresh is disabled.
L	Powered	Powered	H	L ⁵	Output is low, and refresh is disabled.
L	Undervoltage	Powered	L	Default	Input undervoltage. Outputs are in the default state, high for ADuM1440, ADuM1441, and ADuM1442, and low ADuM1445, ADuM1446, and ADuM1447. Outputs return to input state within 150 μs of V_{DDI} power restoration. See the pin function descriptions (Table 22 through Table 24) for more details.
L	Undervoltage	Powered	H	Hold	Input undervoltage. Outputs are the last state before input power is shut down.
X	Powered	Undervoltage	X	Z	Output undervoltage. Output pins are in high impedance state. Outputs return to input state within 34 μs of V_{DDO} power restoration. See the pin function descriptions (Table 22 through Table 24) for more details.

¹ H = high, L = low, X = don't care, and Z = high impedance.

² V_{IX} and V_{OX} refer to the input and output signals of a given channel (A, B, C, or D).

³ V_{DDI} refers to the power supply on the input side of a given channel (A, B, C, or D).

⁴ V_{DDO} refers to the power supply on the output side of a given channel (A, B, C, or D).

⁵ Low input must follow a falling edge; otherwise, it can be in the default low state.

ESD CAUTION

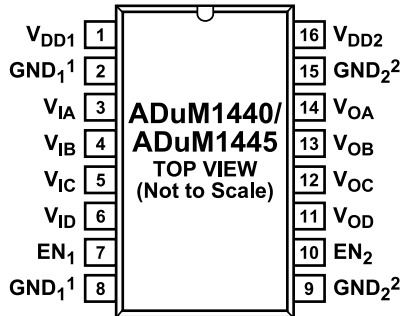


ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge

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Data Sheet

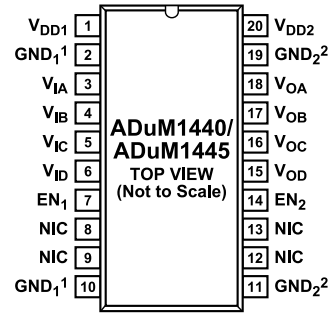
PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS



¹PIN 2 AND PIN 8 ARE INTERNALLY CONNECTED.
CONNECTING BOTH TO GND₁ IS RECOMMENDED.
²PIN 9 AND PIN 15 ARE INTERNALLY CONNECTED.
CONNECTING BOTH TO GND₂ IS RECOMMENDED.

004

Figure 5. ADuM1440/ADuM1445 QSOP Pin Configuration



NIC = NOT INTERNALLY CONNECTED.

¹PIN 2 AND PIN 10 ARE INTERNALLY CONNECTED.
CONNECTING BOTH TO GND₁ IS RECOMMENDED.
²PIN 11 AND PIN 19 ARE INTERNALLY CONNECTED.
CONNECTING BOTH TO GND₂ IS RECOMMENDED.

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Figure 6. ADuM1440/ADuM1445 SSOP Pin Configuration

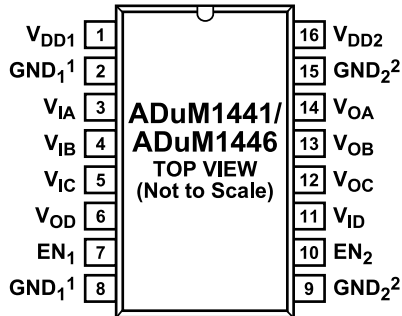
Table 22. ADuM1440/ADuM1445 Pin Function Descriptions¹

QSOP Pin No. ²	SSOP Pin No.	Mnemonic	Description
1	1	V _{DD1}	Supply Voltage for Isolator Side 1 (2.25 V to 3.6 V). Connect a ceramic bypass capacitor in the 0.01 μ F to 0.1 μ F range between V _{DD1} (Pin 1) and GND ₁ (Pin 2).
2, 8	2, 10	GND ₁	Ground 1. Ground reference for Isolator Side 1. Pin 2 and Pin 8 are internally connected, and connecting both to GND ₁ is recommended.
3	3	V _{IA}	Logic Input A.
4	4	V _{IB}	Logic Input B.
5	5	V _{IC}	Logic Input C.
6	3	V _{ID}	Logic Input D.
7	7	EN ₁	Refresh/Watchdog Enable 1. Connecting Pin 7 to GND ₁ enables input/output refresh and watchdog functionality for Side 1, supporting standard iCoupler operation. Tying Pin 7 to V _{DD1} disables refresh and watchdog functionality for lowest power operation, see the Applications Information section for a detailed description of this mode. EN ₁ and EN ₂ must be set to the same logic state.
9, 15	11, 19	GND ₂	Ground 2. Ground reference for Isolator Side 2. Pin 9 and Pin 15 are internally connected, and connecting both to GND ₂ is recommended.
10	14	EN ₂	Refresh/Watchdog Enable 2. Connecting Pin 10 to GND ₂ enables input/output refresh and watchdog functionality for Side 2, supporting standard iCoupler operation. Tying Pin 10 to V _{DD2} disables refresh and watchdog functionality for lowest power operation, see the Applications Information section for a detailed description of this mode. EN ₁ and EN ₂ must be set to the same logic state.
11	15	V _{OD}	Logic Output D.
12	16	V _{OC}	Logic Output C.
13	17	V _{OB}	Logic Output B.
14	18	V _{OA}	Logic Output A.
16	20</		

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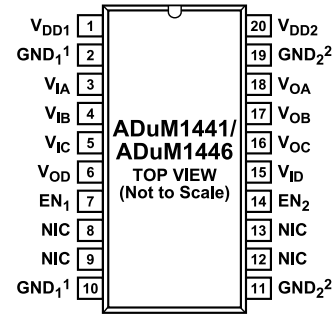
Data Sheet

PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS



¹PIN 2 AND PIN 8 ARE INTERNALLY CONNECTED.
CONNECTING BOTH TO GND₁ IS RECOMMENDED.
²PIN 9 AND PIN 15 ARE INTERNALLY CONNECTED.
CONNECTING BOTH TO GND₂ IS RECOMMENDED.

005



NIC = NOT INTERNALLY CONNECTED.

¹PIN 2 AND PIN 10 ARE INTERNALLY CONNECTED.
CONNECTING BOTH TO GND₁ IS RECOMMENDED.
²PIN 11 AND PIN 19 ARE INTERNALLY CONNECTED.
CONNECTING BOTH TO GND₂ IS RECOMMENDED.

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Figure 7. ADuM1441/ADuM1446 QSOP Pin Configuration

Figure 8. ADuM1441/ADuM1446 SSOP Pin Configuration

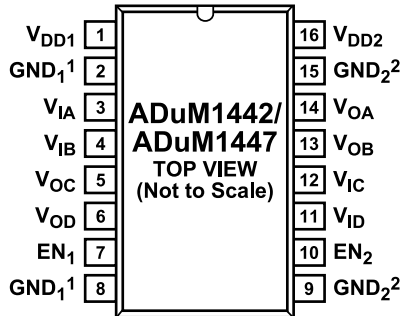
Table 23. ADuM1441/ADuM1446 Pin Function Descriptions¹

QSOP Pin No. ²	SSOP Pin No.	Mnemonic	Description
1	1	V _{DD1}	Supply Voltage for Isolator Side 1 (2.25 V to 3.6 V). Connect a ceramic bypass capacitor in the 0.01 μ F to 0.1 μ F range between V _{DD1} (Pin 1) and GND ₁ (Pin 2).
2, 8	2, 10	GND ₁	Ground 1. Ground reference for Isolator Side 1. Pin 2 and Pin 8 are internally connected, and connecting both to GND ₁ is recommended.
3	3	V _{IA}	Logic Input A.
4	4	V _{IB}	Logic Input B.
5	5	V _{IC}	Logic Input C.
6	3	V _{OD}	

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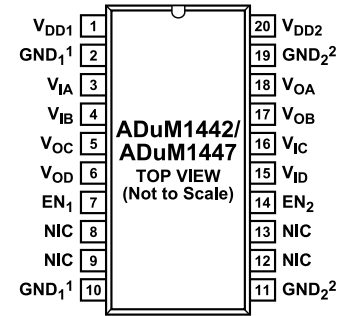
Data Sheet

PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS



¹PIN 2 AND PIN 8 ARE INTERNALLY CONNECTED.
CONNECTING BOTH TO GND₁ IS RECOMMENDED.
²PIN 9 AND PIN 15 ARE INTERNALLY CONNECTED.
CONNECTING BOTH TO GND₂ IS RECOMMENDED.

Figure 9. ADuM1442/ADuM1447 QSOP Pin Configuration



NIC = NOT INTERNALLY CONNECTED.
¹PIN 2 AND PIN 10 ARE INTERNALLY CONNECTED.
CONNECTING BOTH TO GND₁ IS RECOMMENDED.
²PIN 11 AND PIN 19 ARE INTERNALLY CONNECTED.
CONNECTING BOTH TO GND₂ IS RECOMMENDED.

Figure 10. ADuM1442/ADuM1447 SSOP Pin Configuration

Table 24. ADuM1442/ADuM1447 Pin Function Descriptions¹

QSOP Pin No. ²	SSOP Pin No.	Mnemonic	Description
1	1	V _{DD1}	Supply Voltage for Isolator Side 1 (2.25 V to 3.6 V). Connect a ceramic bypass capacitor in the 0.01 μ F to 0.1 μ F range between V _{DD1} (Pin 1) and GND ₁ (Pin 2).
2, 8	2, 10	GND ₁	Ground 1. Ground reference for Isolator Side 1. Pin 2 and Pin 8 are internally connected, and connecting both to GND ₁ is recommended.
3	3	V _{IA}	Logic Input A.
4	4	V _{IB}	Logic Input B.
5	5	V _{OC}	Logic Output C.
6	3	V _{OD}	Logic Output D.
7	7	EN ₁	Refresh/Watchdog Enable 1. Connecting Pin 7 to GND ₁ enables input/output refresh and watchdog functionality for Side 1, supporting standard iCoupler operation. Tying Pin 7 to V _{DD1} disables refresh and watchdog functionality for lowest power operation, see the Applications Information section for detailed description of this mode. EN ₁ and EN ₂ must be set to the same logic state.
9, 15	11, 19	GND ₂	Ground 2. Ground reference for Isolator Side 2. Pin 9 and Pin 15 are internally connected, and connecting both to GND ₂ is recommended.
10	14	EN ₂	Refresh/Watchdog Enable 2. Connecting Pin 10 to GND ₂ enables input/output refresh and watchdog functionality for Side 2, supporting standard iCoupler operation. Tying Pin 10 to V _{DD2} disables refresh and watchdog functionality for lowest power operation, see the Applications Information section for a detailed description of this mode. EN ₁ and EN ₂ must be set to the same logic state.
11	15	V _{ID}	Logic Input D.
12	16	V _{IC}	Logic Input C.
13	17	V _{OB}	Logic Output B.
14	18	V _{OA}	Logic Output A.
16	20	V _{DD2}	Supply Voltage for Isolator Side 2 (2.25 V to 3.6 V). Connect a ceramic bypass capacitor in the 0.01 μ F to 0.1 μ F range between V _{DD2} (Pin 16) and GND ₂ (Pin 15).
N/A	8, 9, 12, 13	NC	No Connect. Do not connect to this pin.

TYPICAL PERFORMANCE CHARACTERISTICS

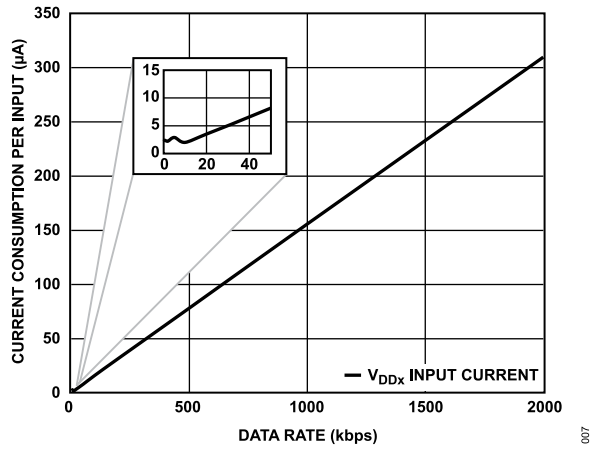


Figure 11. Current Consumption per Input vs. Data Rate for 2.5 V, $EN_x = \text{Low}$ Operation

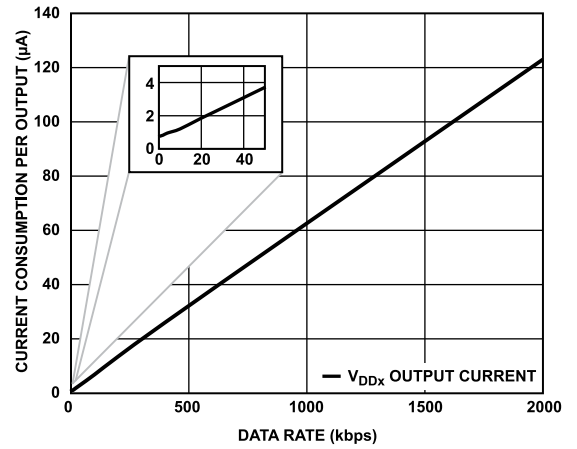


Figure 14. Current Consumption per Output vs. Data Rate for 3.3 V, $EN_x = \text{Low}$ Operation

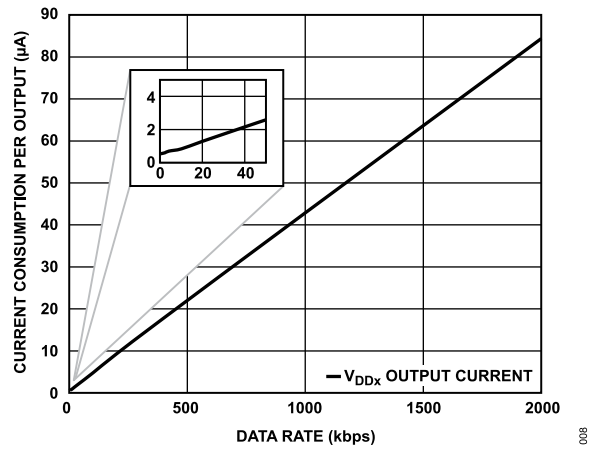


Figure 12. Current Consumption per Output vs. Data Rate for 2.5 V, $EN_x = \text{Low}$ Operation

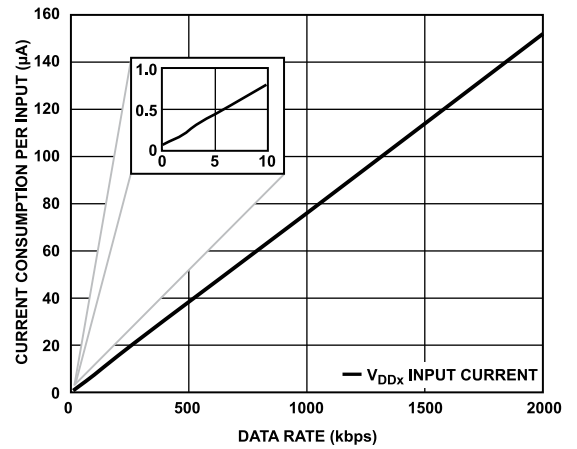


Figure 15. Current Consumption per Input vs. Data Rate for 2.5 V, $EN_x = \text{High}$ Operation

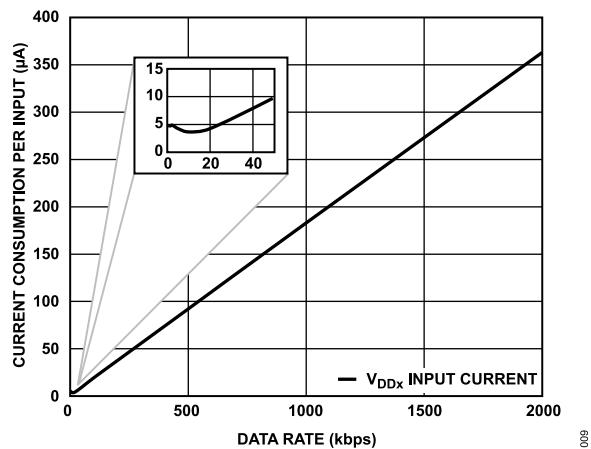


Figure 13. Current Consumption per Input vs. Data Rate for 3.3 V, $EN_x = \text{Low}$ Operation

TYPICAL PERFORMANCE CHARACTERISTICS

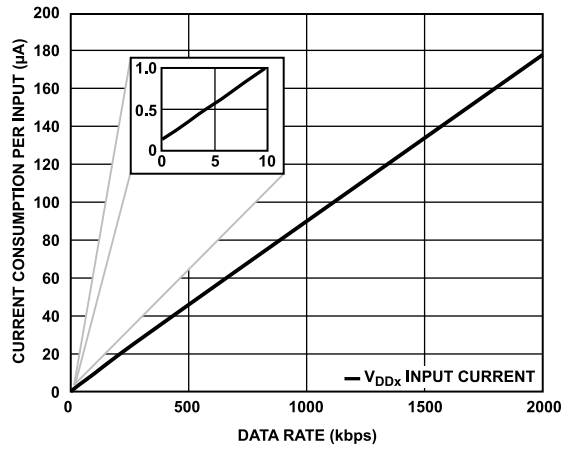


Figure 17. Current Consumption per Input vs. Data Rate for $V_{DDX} = 3.3$ V, $EN_X =$ High Operation

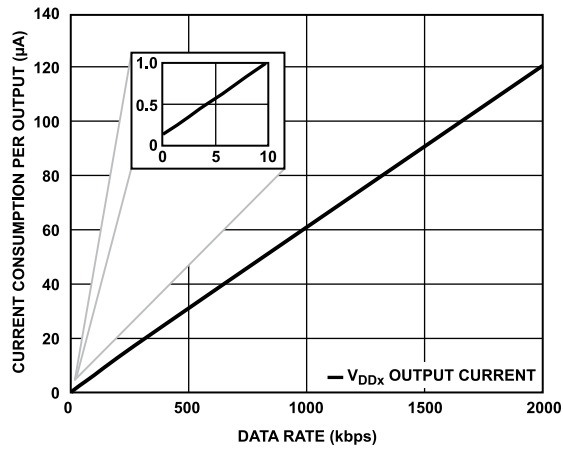


Figure 18. Current Consumption per Output vs. Data Rate for $V_{DDX} = 3.3$ V, $EN_X =$ High Operation

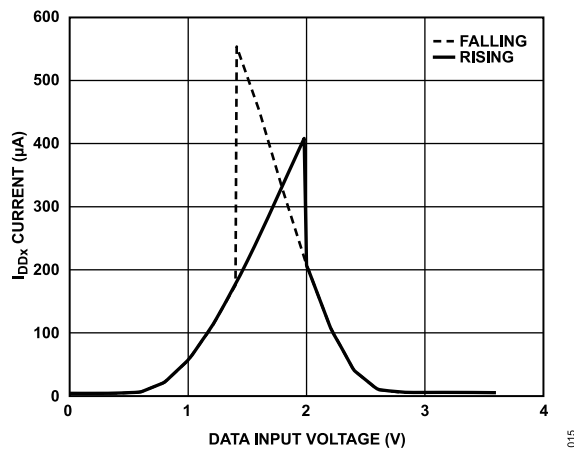


Figure 19. Typical I_{DDX} Current per Input vs. Data Input Voltage for $V_{DDX} = 3.3$ V

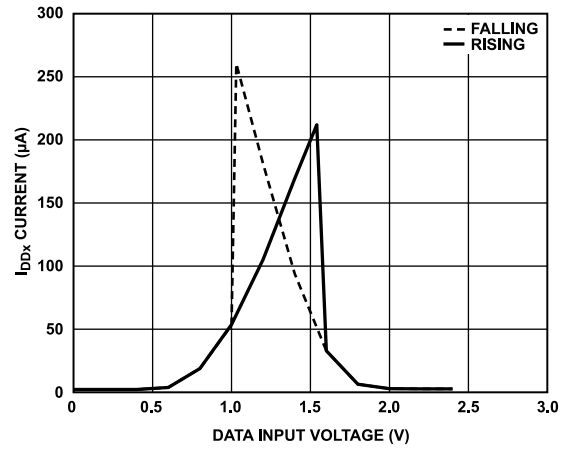


Figure 20. I_{DDX} Current per Input vs. Data Input Voltage for $V_{DDX} = 2.5$ V

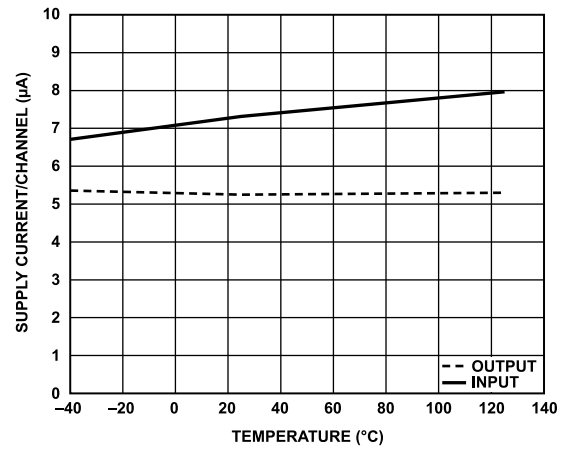


Figure 21. Typical Input and Output Supply Current per Channel vs. Temperature for $V_{DDX} = 2.5$ V, Data Rate = 100 kbps

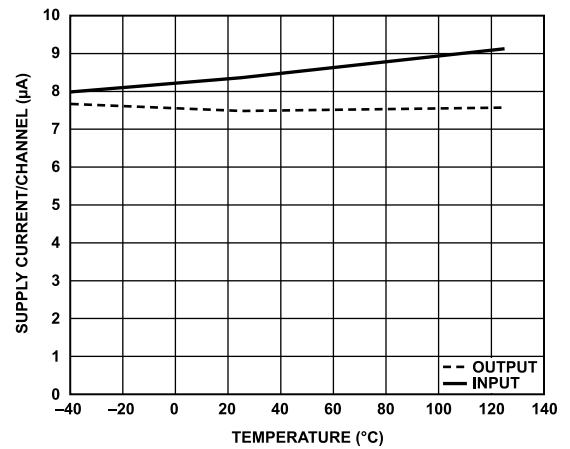


Figure 22. Typical Input and Output Supply Current per Channel vs. Temperature for $V_{DDX} = 3.3$ V, Data Rate = 100 kbps

TYPICAL PERFORMANCE CHARACTERISTICS

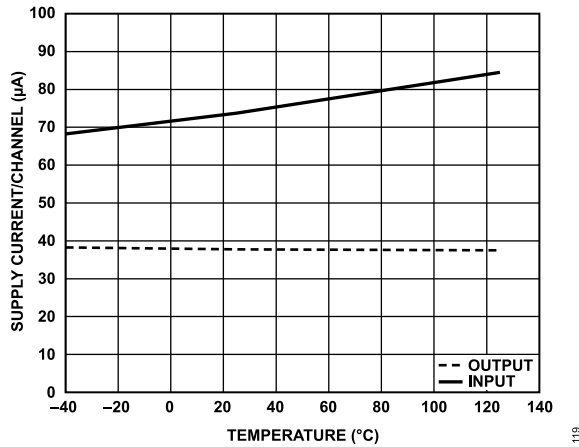


Figure 23. Typical Input and Output Supply Current per Channel vs. Temperature for $V_{DDX} = 2.5$ V, Data Rate = 1000 kbps

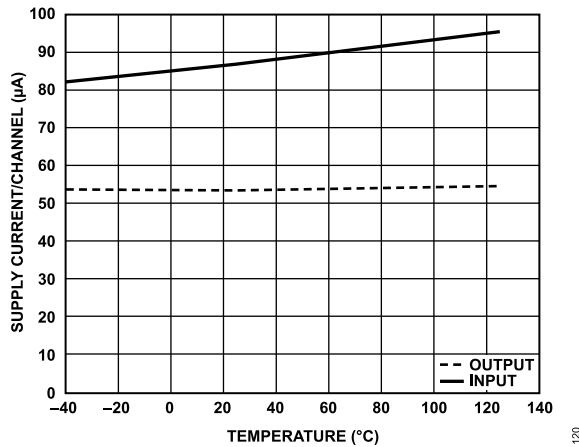


Figure 24. Typical Input and Output Supply Current per Channel vs. Temperature for $V_{DDX} = 3.3$ V, Data Rate = 1000 kbps

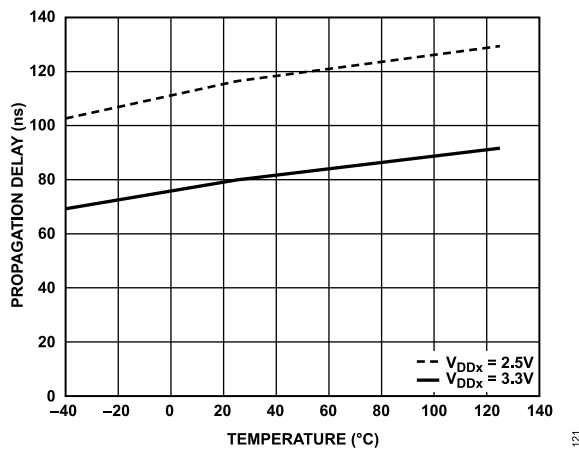


Figure 25. Typical Propagation Delay vs. Temperature for $V_{DDX} = 3.3$ V or $V_{DDX} = 2.5$ V

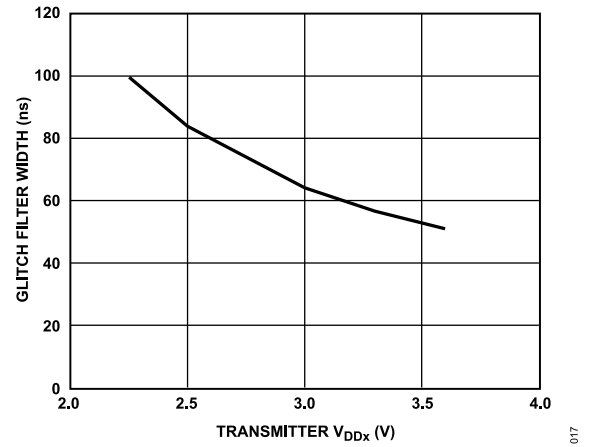
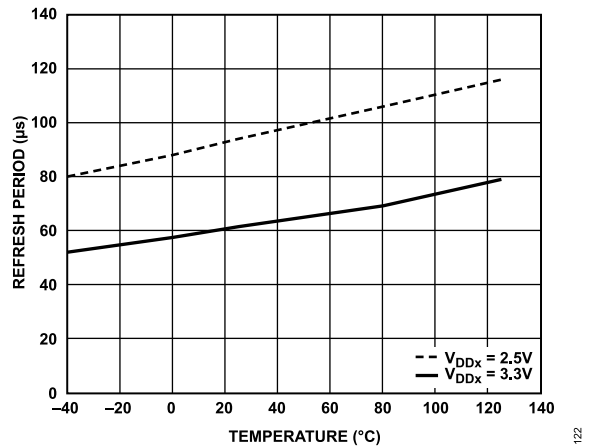


Figure 26. Typical Glitch Filter Operation Threshold



APPLICATIONS INFORMATION

PCB LAYOUT

The ADuM1440/ADuM1441/ADuM1442/ADuM1445/ADuM1446/ADuM1447 digital isolators require no external interface circuitry for the logic interfaces. Power supply bypassing is strongly recommended at both input and output supply pins: V_{DD1} and V_{DD2} (see Figure 29). Choose a capacitor value between 0.01 μF and 0.1 μF . The total lead length between both ends of the capacitor and the input power supply pin must not exceed 20 mm.

Using proper PCB design choices, the ADuM1440/ADuM1441/ADuM1442/ADuM1445/ADuM1446/ADuM1447 readily meets CISPR 22 Class A (and FCC Class A) emissions standards, as well as the more stringent CISPR 22 Class B (and FCC Class B) standards in an unshielded environment. Refer to the [AN-1109 Application Note, Recommendations for Control of Radiated Emissions with iCoupler Devices](#), for PCB-related EMI mitigation techniques, including board layout and stack-up issues.

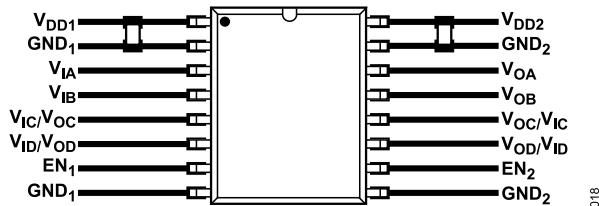


Figure 29. Recommended Printed Circuit Board Layout, QSOP

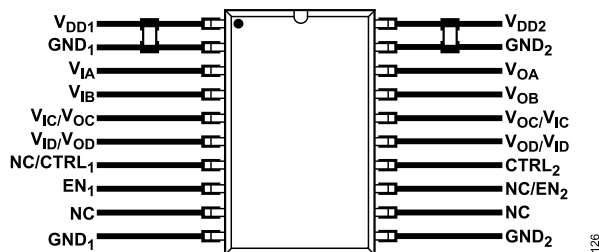


Figure 30. Recommended Printed Circuit Board Layout, SSOP

For applications involving high common-mode transients, it is important to minimize board coupling across the isolation barrier. Furthermore, design the board layout so that any coupling that does occur equally affects all pins on a given component side. Failure to ensure this can cause voltage differentials between pins exceeding the absolute maximum ratings of the device, thereby leading to latch-up or permanent damage.

PROPAGATION DELAY-RELATED PARAMETERS

These products are optimized for minimum power consumption by eliminating as many internal bias currents as possible. As a result, the timing characteristics are more sensitive to operating voltage and temperature than in standard iCoupler products. Refer

to Figure 21 through Figure 28 for the expected variation of these parameters.

Propagation delay is a parameter defined as the time it takes a logic signal to propagate through a component. The input-to-output propagation delay time for a high-to-low transition can differ from the propagation delay time of a low-to-high transition.

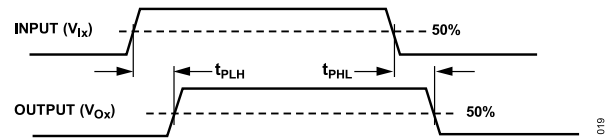


Figure 31. Propagation Delay Parameters

Pulse width distortion is the maximum difference between these two propagation delay values and an indication of how accurately the timing of the input signal is preserved.

Channel-to-channel matching is the maximum amount of time the propagation delay differs between channels within a single ADuM1440/ADuM1441/ADuM1442/ADuM1445/ADuM1446/ADuM1447 component.

Propagation delay skew is the maximum amount of time the propagation delay differs between multiple ADuM1440/ADuM1441/ADuM1442/ADuM1445/ADuM1446/ADuM1447 components operating under the same conditions.

In edge-based systems, it is critical to reject pulses that are too short to be handled by the encode and decode circuits. The ADuM1440/ADuM1441/ADuM1442/ADuM1445/ADuM1446/ADuM1447 implement a glitch filter to reject pulses less than the glitch filter operating threshold. This threshold depends on the operating voltage, as shown in Figure 26. Any pulse shorter than the glitch filter does not pass to the output. When the refresh circuit is enabled, pulses that match the glitch filter width have a small probability of being

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isolator watchdog circuit forces the output to a default state. The default state is either high as in the ADuM1440, ADuM1441, and ADuM1442 versions, or low as in the ADuM1445, ADuM1446, and ADuM1447 versions.

Low Power Operating Mode

The ADuM1440/ADuM1441/ADuM1442/ADuM1445/ADuM1446/ADuM1447 allow the refresh and watchdog functions to be disabled by pulling EN₁ and EN₂ to logic high for the lowest power consumption. These control pins must be set to the same value on each side of the component for proper operation.

In this mode, the current consumption of the chip drops to the microamp range. However, be careful when using this mode because dc correctness is no longer guaranteed at startup. For example, if the following sequence of events occurs:

1. Power is applied to Side 1
2. A high level is asserted on the V_{IA} input
3. Power is applied to Side 2

The high on V_{IA} is not automatically transferred to the Side 2 V_{OA}, and there can be a level mismatch that is not corrected until a transition occurs at V_{IA}. After power is stable on each side and a transition occurs on the input of the channel, that channel's input and output state is correctly matched. This contingency can be addressed in several ways, such as sending dummy data, or toggling refresh on for a short period to force synchronization after turn on.

Recommended Input Voltage for Low Power Operation

The ADuM1440/ADuM1441/ADuM1442/ADuM1445/ADuM1446/ADuM1447 implement Schmitt trigger input buffers so that the devices operate cleanly in low data rate or noisy environments. Schmitt triggers allow a small amount of shoot through current when their input voltage is not approximate to either V_{DDx} or GND_x levels. This is because the two transistors are both slightly on when input voltages are in the middle of the supply range. For many digital devices, this leakage is not a large portion of the total supply current and may not be noticed; however, in the ultralow power ADuM1440/ADuM1441/ADuM1442/ADuM1445/ADuM1446/ADuM1447, this leakage can be larger than the total operating current of the device and cannot be ignored.

To achieve optimum power consumption with the ADuM1440/ADuM1441/ADuM1442/ADuM1445/ADuM1446/ADuM1447, always drive the inputs as near to V_{DDx} or GND_x levels as possible. [Figure 19](#) and [Figure 20](#) illustrate the shoot through leakage of an input; therefore, whereas the logic thresholds of the input are standard CMOS levels, optimum power performance is achieved when the input logic levels are driven within 0.5 V of either V_{DDx} or GND_x levels.

MAGNETIC FIELD IMMUNITY

The magnetic field immunity of the ADuM1440/ADuM1441/ADuM1442/ADuM1445/ADuM1446/ADuM1447 is determined by the changing magnetic field, which induces a voltage in the receiving coil of the transformer large enough to either falsely set or reset the decoder. The following analysis defines the conditions under which this can occur. The 3.3 V operating condition of the ADuM1440/ADuM1441/ADuM1442/ADuM1445/ADuM1446/ADuM1447 is examined because it represents the most typical mode of operation.

The pulses at the transformer output have an amplitude greater than 1.0 V. The decoder has a sensing threshold at about 0.5 V, thus establishing a 0.5 V margin in which induced voltages can be tolerated. The voltage induced across the receiving coil is given by

$$V = (-d\beta/dt) \sum \pi r_n^2; n = 1, 2, \dots, N \quad (1)$$

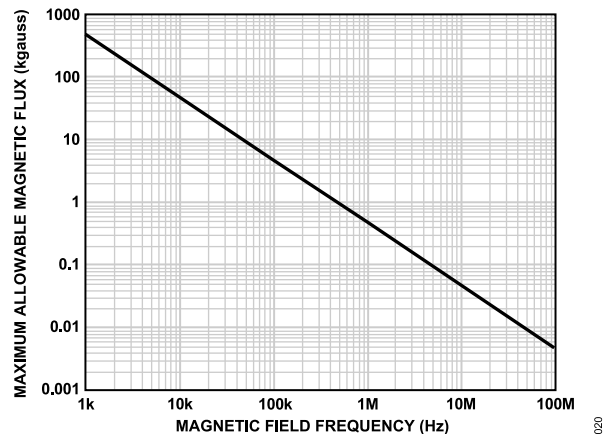
where:

β is magnetic flux density (gauss).

r_n is the radius of the nth turn in the receiving coil (cm).

N is the number of turns in the receiving coil.

Given the geometry of the receiving coil in the ADuM1440/ADuM1441/ADuM1442/ADuM1445/ADuM1446/ADuM1447 and an imposed requirement that the induced voltage be, at most, 50% of the 0.5 V margin at the decoder, a maximum allowable magnetic field at a given frequency can be calculated. The result is shown in [Figure 32](#).



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The preceding magnetic flux density values correspond to specific current magnitudes at given distances from the ADuM1440/ADuM1441/ADuM1442/ADuM1445/ADuM1446/ADuM1447 transformers. Figure 33 shows these allowable current magnitudes as a function of frequency for selected distances. As shown, the ADuM1440/ADuM1441/ADuM1442/ADuM1445/ADuM1446/ADuM1447 are extremely immune and can be affected only by extremely large currents operating at a high frequency very near to the component. For the 1 MHz example noted previously, a 1.2 kA current would have to be placed 5 mm away from the ADuM1440/ADuM1441/ADuM1442/ADuM1445/ADuM1446/ADuM1447 to affect the operation of the component.

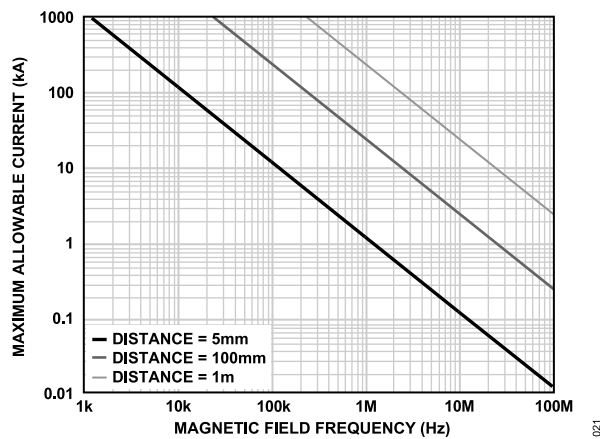


Figure 33. Maximum Allowable Current for Various Current-to-ADuM1440/ADuM1441/ADuM1442/ADuM1445/ADuM1446/ADuM1447 Spacings

Note that at combinations of strong magnetic field and high frequency, any loops formed by PCB traces can induce error voltages sufficiently large enough to trigger the thresholds of succeeding circuitry. Take care in the layout of such traces to avoid this possibility.

POWER CONSUMPTION

The supply current at a given channel of the ADuM1440/ADuM1441/ADuM1442/ADuM1445/ADuM1446/ADuM1447 isolator is a function of the supply voltage, the data rate of the channel, and the output load of the channel.

For each input channel, the supply current is given by

$$I_{DDI} = I_{DDI(Q)} f \leq 0.5 f_r$$

$$I_{DDI} = I_{DDI(D)} \times (2f - f_r) + I_{DDI(Q)} f > 0.5 f_r$$

For each output channel, the supply current is given by

$$I_{DDO} = I_{DDO(Q)} f \leq 0.5 f_r$$

$$I_{DDO} = (I_{DDO(D)} + (0.5 \times 10^{-3}) \times C_L \times V_{DDO}) \times (2f - f_r) + I_{DDO(Q)} f > 0.5 f_r$$

where:

$I_{DDI(D)}$, $I_{DDO(D)}$ are the input and output dynamic supply currents per channel (mA/Mbps).

$I_{DDI(Q)}$, $I_{DDO(Q)}$ are the specified input and output quiescent supply currents (mA).

f is the input logic signal frequency (MHz); it is half the input data rate, expressed in units of Mbps.

f_r is the input stage refresh rate (Mbps).

C_L is the output load capacitance (pF).

V_{DDO} is the output supply voltage (V).

To calculate the total V_{DD1} and V_{DD2} supply current, the supply currents for each input and output channel corresponding to V_{DD1} and V_{DD2} are calculated and totaled. Figure 11 through Figure 18 show per channel supply currents as a function of data rate for an unloaded output condition.

The ADuM1440/ADuM1441/ADuM1442/ADuM1445/ADuM1446/ADuM1447 devices are intended to operate at an ultralow current. This is achieved by operating the part at a low average data rate, either by bursting data at high speed at a low duty factor or by running low bit rates. If data is burst at high data rates, the part sits quiescent for the majority of the time, at low data rates, the power consumption approaches the quiescent power consumption. Table 25 shows the typical current for an input and output channel pair as well as the

ADuM1440/ADuM1441/ADuM1442/ADuM1445/ ADuM1446/ADuM1447

Data Sheet

OUTLINE DIMENSIONS

Package Drawing (Option)	Package Type	Package Description
RQ-16	QSOP	16-Lead Shrink Small Outline Package
RS-20	SSOP	20-Lead Shrink Small Outline Package

For the latest package outline information and land patterns (footprints), go to [Package Index](#).

ORDERING GUIDE

Model ^{1, 2}	Temperature Range	Package Description	Package Option
ADuM1440ARQZ	-40°C to +125°C	16-Lead QSOP	RQ-16
ADuM1440ARQZ-RL7	-40°C to +125°C	16-Lead QSOP	RQ-16
ADuM1441ARQZ	-40°C to +125°C	16-Lead QSOP	RQ-16
ADuM1441ARQZ-RL7	-40°C to +125°C	16-Lead QSOP	RQ-16
ADuM1442ARQZ	-40°C to +125°C	16-Lead QSOP	RQ-16
ADuM1442ARQZ-RL7	-40°C to +125°C	16-Lead QSOP	RQ-16
ADuM1445ARQZ	-40°C to +125°C	16-Lead QSOP	RQ-16
ADuM1445ARQZ-RL7	-40°C to +125°C	16-Lead QSOP	RQ-16
ADuM1446ARQZ	-40°C to +125°C	16-Lead QSOP	RQ-16
ADuM1446ARQZ-RL7	-40°C to +125°C	16-Lead QSOP	RQ-16
ADuM1447ARQZ	-40°C to +125°C	16-Lead QSOP	RQ-16
ADuM1447ARQZ-RL7	-40°C to +125°C	16-Lead QSOP	RQ-16
ADuM1440ARSZ	-40°C to +125°C	20-Lead SSOP	RS-20
ADuM1440ARSZ-RL7	-40°C to +125°C	20-Lead SSOP	RS-20
ADuM1441ARSZ	-40°C to +125°C	20-Lead SSOP	RS-20
ADuM1441ARSZ-RL7	-40°C to +125°C	20-Lead SSOP	RS-20
ADuM1442ARSZ	-40°C to +125°C	20-Lead SSOP	RS-20
ADuM1442ARSZ-RL7	-40°C to +125°C	20-Lead SSOP	RS-20
ADuM1445ARSZ	-40°C to +125°C	20-Lead SSOP	RS-20
ADuM1445ARSZ-RL7	-40°C to +125°C	20-Lead SSOP	RS-20
ADuM1446ARSZ	-40°C to +125°C	20-Lead SSOP	RS-20
ADuM1446ARSZ-RL7	-40°C to +125°C	20-Lead SSOP	RS-20
ADuM1447ARSZ	-40°C to +125°C	20-Lead SSOP	RS-20
ADuM1447ARSZ-RL7	-40°C to +125°C	20-Lead SSOP	RS-20

¹ Z = RoHS Compliant Part.

² Tape and reel is available. The addition of the -RL7 suffix indicates that the product is shipped on 7" tape and reel.

ADuM1440/ADuM1441/ADuM1442/ADuM1445/ ADuM1446/ADuM1447

Data Sheet

OUTLINE DIMENSIONS

NUMBER OF INPUTS, V_{DD1} SIDE, NUMBER OF INPUTS, V_{DD2} SIDE, MAXIMUM DATA RATE (MBPS), DEFAULT OUTPUT STATE, AND MAXIMUM PROPAGATION DELAY, 3.3 V (NS) OPTIONS

Model ¹	Number of Inputs, V_{DD2} Side	Maximum Data Rate (Mbps)	Default Output State	Maximum Propagation Delay, 3.3 V (ns)
ADuM1440ARQZ	0	2	High	180
ADuM1441ARQZ	1	2	High	180
ADuM1442ARQZ	2	2	High	180
ADuM1445ARQZ	0	2	Low	180
ADuM1446ARQZ	1	2	Low	180
ADuM1447ARQZ	2	2	Low	180
ADuM1440ARSZ	0	2	High	180
ADuM1441ARSZ	1	2	High	180
ADuM1442ARSZ	2	2	High	180
ADuM1445ARSZ	0	2	Low	180
ADuM1446ARSZ	1	2	Low	180
ADuM1447ARSZ	2	2	Low	180

¹ Z = RoHS Compliant Part.

EVALUATION BOARDS

Model ^{1, 2}	Description
EVAL-ADuM1441EBZ	Evaluation Board

¹ Z = RoHS Compliant Part.

² Tape and reel is available. The addition of the -RL7 suffix indicates that the product is shipped on 7" tape and reel.