ANALOG DEVICES

ADuM1250/ADuM1251

Hot Swappable, Dual I²C Isolators

FEATURES

- Bidirectional I²C communication
- Open-drain interfaces
- Suitable for hot swap applications
- 30 mA current sink capability
- 1000 kHz operation
- 3.0 V to 5.5 V supply/logic levels
- 8-lead, RoHS compliant SOIC package
- High temperature operation: 125°C
- Qualified for automotive applications
- Safety and regulatory approvals
  - DIN EN IEC 60747-17 (VDE 0884-17)
    - V_{IORM} = 560 V peak
  - UL 1577
    - V_{ISO} = 2500 V rms for 1 minute
  - IEC/EN/CSA 62368-1
  - IEC/CSA 61010-1
  - CQC GB4943.1

APPLICATIONS

- Isolated I²C, SMBus, or PMBus interfaces
- Multilevel I²C interfaces
- Power supplies
- Networking
- Power over Ethernet
- Hybrid electric vehicle battery management

FUNCTIONAL BLOCK DIAGRAMS

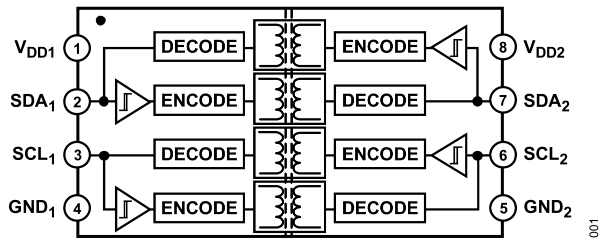

Figure 1. ADuM1250

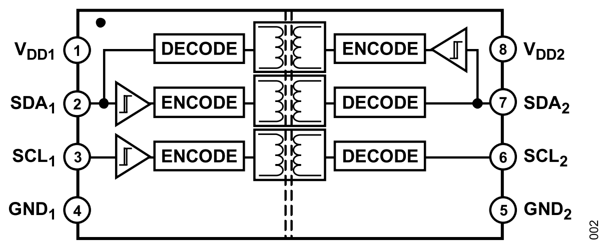

Figure 2. ADuM1251

GENERAL DESCRIPTION

The ADuM1250/ADuM1251[1] are hot swappable digital isolators with nonlatching, bidirectional communication channels that are compatible with I²C interfaces. This eliminates the need for splitting I²C signals into separate transmit and receive signals for use with standalone optocouplers.

The ADuM1250 provides two bidirectional channels, supporting a complete isolated I²C interface. The ADuM1251 provides one bidirectional channel and one unidirectional channel for applications where a bidirectional clock is not required.

Both the ADuM1250 and the ADuM1251 contain hot swap circuitry to prevent glitching data when an unpowered card is inserted onto an active bus.

These isolators are based on the *i*Coupler® chip scale transformer technology from Analog Devices, Inc. *i*Coupler is a magnetic isolation technology with functional, performance, size, and power consumption advantages as compared to optocouplers. With the ADuM1250/ADuM1251, *i*Coupler channels can be integrated with semiconductor circuitry, which enables a complete isolated I²C interface to be implemented in a small form factor.

[1] Protected by U.S. Patents 5,952,849; 6,873,065; and 7,075,329.

Rev. L

DOCUMENT FEEDBACK

TECHNICAL SUPPORT

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REVISION HISTORY

9/2025—Rev. K to Rev. L

Changes to Features Section 1
Combined Electrical Characteristics Section and DC Specifications Section into Electrical Specifications Section
Changes to Input Capacitance Parameter, Table 1 4
Changed AC Specifications Section to Timing Specifications Section 5
Deleted Package Characteristics Section and Table 3; Renumbered Sequentially 6
Deleted Insulation and Safety Related Specifications Section and Table 5 6
Changed DIN EN IEC 60747-17 (VDE 0884-17) Insulation Characteristics Section to Insulation Specifications Section 6
Changes to Insulation Specifications Section, Table 3, and Figure 3 6
Moved Regulatory Information Section and Table 4 7
Changes to Regulatory Information Section and Table 4 7
Changes to Table 5 8
Changes to Table 6 9
Added Thermal Characteristics Section and Table 7; Renumbered Sequentially 9
Added Thermal Analysis Section 14

5/2025—Rev. J to Rev. K

Changes to Features Section 1
Changes to Regulatory Information Section 7
Replaced Table 4 6
Changes to Table 5 6
Changed DIN VDE V 0884-11:2017-01 Insulation Characteristics Section to DIN EN IEC 60747-17 (VDE 0884-17) Insulation Characteristics Section 6
Changes to DIN EN IEC 60747-17 (VDE 0884-17) Insulation Characteristics Section and Table 6 6
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4/2023—Rev. I to Rev. J

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SPECIFICATIONS

ELECTRICAL SPECIFICATIONS

All voltages are relative to their respective ground. All minimum and maximum specifications apply over the entire recommended operating range, unless otherwise noted. All typical specifications are at T_A = 25°C, V_{DD1} = 3.3 V or 5 V, and V_{DD2} = 3.3 V or 5 V, unless otherwise noted.

Table 1. Electrical Characteristics

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
ADuM1250						
Input Supply Current, Side 1, 5 V	I_{DD1}		2.8	5.0	mA	V_{DD1} = 5 V
Input Supply Current, Side 2, 5 V	I_{DD2}		2.7	5.0	mA	V_{DD2} = 5 V
Input Supply Current, Side 1, 3.3 V	I_{DD1}		1.9	3.0	mA	V_{DD1} = 3.3 V
Input Supply Current, Side 2, 3.3 V	I_{DD2}		1.7	3.0	mA	V_{DD2} = 3.3 V
ADuM1251						
Input Supply Current, Side 1, 5 V	I_{DD1}		2.8	6.0	mA	V_{DD1} = 5 V
Input Supply Current, Side 2, 5 V	I_{DD2}		2.5	4.7	mA	V_{DD2} = 5 V
Input Supply Current, Side 1, 3.3 V	I_{DD1}		1.8	3.0	mA	V_{DD1} = 3.3 V
Input Supply Current, Side 2, 3.3 V	I_{DD2}		1.6	2.8	mA	V_{DD2} = 3.3 V
LEAKAGE CURRENTS	I_{SDA1}, I_{SDA2}, I_{SCL1}, I_{SCL2}		0.01	10	µA	$V_{SDA1} = V_{DD1}$, $V_{SDA2} = V_{DD2}$, $V_{SCL1} = V_{DD1}$, $V_{SCL2} = V_{DD2}$
SIDE 1 LOGIC LEVELS						
Logic Input Threshold[1]	V_{SDA1T}, V_{SCL1T}	500		700	mV	
Logic Low Output Voltages	V_{SDA1OL}, V_{SCL1OL}	600		900	mV	$I_{SDA1} = I_{SCL1}$ = 3.0 mA
		600		850	mV	$I_{SDA1} = I_{SCL1}$ = 0.5 mA
Input/Output Logic Low Level Difference[2]	ΔV_{SDA1}, ΔV_{SCL1}	50			mV	
SIDE 2 LOGIC LEVELS						
Logic Low Input Voltage	V_{SDA2IL}, V_{SCL2IL}			0.3 V_{DD2}	V	
Logic High Input Voltage	V_{SDA2IH}, V_{SCL2IH}	0.7 V_{DD2}			V	
Logic Low Output Voltage	V_{SDA2OL}, V_{SCL2OL}			400	mV	$I_{SDA2} = I_{SCL2}$ = 30 mA
INPUT CAPACITANCE	C_{IN}		4.0		pF	Pin capacitance

[1] V_{IL} < 0.5 V, V_{IH} > 0.7 V.

[2] $\Delta V_{S1} = V_{S1OL} - V_{S1T}$. This is the minimum difference between the output logic low level and the input logic threshold within a given component. This ensures that there is no possibility of the part latching up the bus to which it is connected.

SPECIFICATIONS

TIMING SPECIFICATIONS

All voltages are relative to their respective ground. All minimum and maximum specifications apply over the entire recommended operating range, unless otherwise noted. All typical specifications are at T_A = 25°C, V_{DD1} = 3.3 V or 5 V, and V_{DD2} = 3.3 V or 5 V, unless otherwise noted. Refer to Figure 5.

Table 2. Timing Characteristics

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
MAXIMUM FREQUENCY		1000			kHz	
OUTPUT FALL TIME						
5 V Operation						4.5 V ≤ V_{DD1}, V_{DD2} ≤ 5.5 V, C_{L1} = 40 pF, R1 = 1.6 kΩ, C_{L2} = 400 pF, R2 = 180 Ω
Side 1 Output (0.9 V_{DD1} to 0.9 V)	t_{f1}	13	26	120	ns	
Side 2 Output (0.9 V_{DD2} to 0.1 V_{DD2})	t_{f2}	32	52	120	ns	
3 V Operation						3.0 V ≤ V_{DD1}, V_{DD2} ≤ 3.6 V, C_{L1} = 40 pF, R1 = 1.0 kΩ, C_{L2} = 400 pF, R2 = 120 Ω
Side 1 Output (0.9 V_{DD1} to 0.9 V)	t_{f1}	13	32	120	ns	
Side 2 Output (0.9 V_{DD2} to 0.1 V_{DD2})	t_{f2}	32	61	120	ns	
PROPAGATION DELAY						
5 V Operation						4.5 ≤ V_{DD1}, V_{DD2} ≤ 5.5 V, C_{L1} = C_{L2} = 0 pF, R1 = 1.6 kΩ, R2 = 180 Ω
Side 1 to Side 2, Rising Edge[1]	t_{PLH12}		95	130	ns	
Side 1 to Side 2, Falling Edge[2]	t_{PHL12}		162	275	ns	
Side 2 to Side 1, Rising Edge[3]	t_{PLH21}		31	70	ns	
Side 2 to Side 1, Falling Edge[4]	t_{PHL21}		85	155	ns	
3 V Operation						3.0 V ≤ V_{DD1}, V_{DD2} ≤ 3.6 V, C_{L1} = C_{L2} = 0 pF, R1 = 1.0 kΩ, R2 = 120 Ω
Side 1 to Side 2, Rising Edge [1]	t_{PLH12}		82	125	ns	
Side 1 to Side 2, Falling Edge[2]	t_{PHL12}		196	340	ns	
Side 2 to Side 1, Rising Edge[3]	t_{PLH21}		32	75	ns	
Side 2 to Side 1, Falling Edge[4]	t_{PHL21}		110	210	ns	
PULSE WIDTH DISTORTION						
5 V Operation						4.5 V ≤ V_{DD1}, V_{DD2} ≤ 5.5 V, C_{L1} = C_{L2} = 0 pF, R1 = 1.6 kΩ, R2 = 180 Ω
Side 1 to Side 2, $\lvert t_{PLH12} - t_{PHL12}\rvert$	PWD_{12}		67	145	ns	
Side 2 to Side 1, $\lvert t_{PLH21} - t_{PHL21}\rvert$	PWD_{21}		54	85	ns	
3 V Operation						3.0 V ≤ V_{DD1}, V_{DD2} ≤ 3.6 V, C_{L1} = C_{L2} = 0 pF, R1 = 1.0 kΩ, R2 = 120 Ω
Side 1 to Side 2, $\lvert t_{PLH12} - t_{PHL12}\rvert$	PWD_{12}		114	215	ns	
Side 2 to Side 1, $\lvert t_{PLH21} - t_{PHL21}\rvert$	PWD_{21}		77	135	ns	
COMMON-MODE TRANSIENT IMMUNITY[5]	$\lvert CM_H\rvert$, $\lvert CM_L\rvert$	25	35		kV/μs	

[1] t_{PLH12} propagation delay is measured from the Side 1 input logic threshold to an output value of 0.7 V_{DD2}.

[2] t_{PHL12} propagation delay is measured from the Side 1 input logic threshold to an output value of 0.4 V.

[3] t_{PLH21} propagation delay is measured from the Side 2 input logic threshold to an output value of 0.7 V_{DD1}.

[4] t_{PHL21} propagation delay is measured from the Side 2 input logic threshold to an output value of 0.9 V.

[5] CM_H is the maximum common-mode voltage slew rate that can be sustained while maintaining V_O > 0.8 V_{DD2}. CM_L is the maximum common-mode voltage slew rate that can be sustained while maintaining V_O < 0.8 V. The common-mode voltage slew rates apply to both rising and falling common-mode voltage edges. The transient magnitude is the range over which the common mode is slewed.

SPECIFICATIONS

INSULATION SPECIFICATIONS

The ADuM1250/ADuM1251 are suitable for safe electrical insulation only within the safety limiting ratings. Compliance with the safety limiting ratings is ensured by means of suitable protective circuits. The asterisk (*) marking on the package denotes DIN EN IEC 60747-17 (VDE 0884-17) approval.

Table 3. ADuM1250/ADuM1251, 8-Lead Narrow-Body SOIC [SOIC_N] (R-8) Insulation Characteristics

Parameter	Symbol	Value	Unit	Test Conditions/Comments
GENERAL				
Minimum External Clearance Distance	CLR	4.0	mm	Measured from input terminals to output terminals, shortest distance through air per IEC 60664-1
Minimum External Creepage Distance	CRP	4.0	mm	Measured from input terminals to output terminals, shortest distance along body per IEC 60664-1
Distance Through Insulation	DTI	18	μm	Minimum internal
Comparative Tracking Index	CTI	>400	V	Per IEC 60112
Material Group		II		Per IEC 60664-1
Overvoltage Category per IEC 60664-1		I to IV		Rated mains voltage ≤ 150 V rms
		I to III		Rated mains voltage ≤ 300 V rms
		I to II		Rated mains voltage ≤ 400 V rms
SAFETY LIMITING VALUES				
Maximum Ambient Safety Temperature	T_S	150	°C	
Maximum Junction Temperature, Safety	$T_{JMAX,S}$	150	°C	Maximum junction temperature for isolation barrier safety
Maximum Total Power Dissipation	P_{TOT}	1.4	W	$T_A \leq 25°C$, $P_{TOT} = P_{SI} = P_{SO}$
Derating Above Ambient (T_A)		11.2	mW/°C	$T_A > 25°C$, see Figure 3
Junction-to-Air Thermal Impedance	θ_{JA}	89	°C/W	See the Thermal Characteristics section
IEC 60747-17 (REINFORCED INSULATION)				
Maximum Repetitive Peak Isolation Voltage	V_{IORM}	560	V peak	
Maximum Isolation Working Voltage	V_{IOWM}	396	V rms	AC voltage, end of life test, f = 60 Hz
		560	V peak	DC voltage
Maximum Transient Isolation Voltage	V_{IOTM}	4000	V peak	$V_{TEST} = 1.2 \times V_{IOTM}$, t = 1 s (100% production)
Maximum Impulse Voltage	V_{IMP}	4000	V peak	Surge voltage in air, waveform per IEC 61000-4-5
Maximum Surge Isolation Voltage	V_{IOSM}	10000	V peak	$V_{TEST} \geq 1.3 \times V_{IMP}$ minimum 10 kV (type test), tested in oil, waveform per IEC 61000-4-5
Apparent Charge	q_{pd}	≤5	pC	Method a (sample test), $V_{ini} = V_{IOTM}$, t_{ini} = 60 s, $V_{pd(m)} = 1.6 \times V_{IORM}$, t_m = 10 s Method b1 (100% production), $V_{ini} = 1.2 \times V_{IOTM}$, t_{ini} = 1 s, $V_{pd(m)} = 1.875 \times V_{IORM}$, t_m = 1 s
Resistance (Input to Output)[1]	R_{IO}	$>10^{12}$	Ω	T_A = 25°C, V_{TEST} = 500 V dc, t = 60 s
	R_{IO_S}	$>10^{9}$	Ω	$T_A = T_S$, V_{TEST} = 500 V dc, t = 60 s
Capacitance (Input to Output)[1]	C_{IO}	1.0	pF	f_{TEST} = 1 MHz
Climatic Category		40/105/21		A grade
		40/125/21		S, W grades
Pollution Degree		2		Per IEC 60664-1
UL 1577				
Maximum Withstanding Isolation Voltage	V_{ISO}	2500	V rms	$V_{TEST} = 1.2 \times V_{ISO}$, t = 1 s (100% production)

[1] Device measured as a 2-terminal device with Pin 1 to Pin 4 connected and Pin 5 to Pin 8 connected.

SPECIFICATIONS

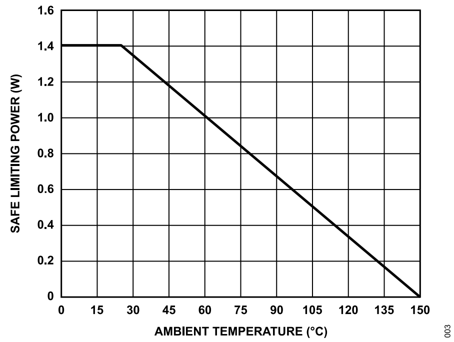


Figure 3. Thermal Derating Curve for 8-Lead Narrow-Body SOIC [SOIC_N] (R-8), Dependence of Safety Limiting Power with Ambient Temperature per IEC 60747-17

REGULATORY INFORMATION

The ADuM1250/ADuM1251 have been approved by the organizations listed in Table 4. Copies of the relevant certificates are available at Safety and Regulatory Certifications for Digital Isolation.

Table 4. ADuM1250/ADuM1251, 8-Lead Narrow-Body SOIC [SOIC_N] (R-8) Package Certifications

Regulatory Agency	Safety Standard/Rating	Certificate Number
UL	UL 1577 component recognition program: Single protection, 2500 V rms isolation voltage	File E214100
CSA[1]	CSA C22.2 No. 14-18 CSA/EN/IEC 62368-1: Basic insulation at 400 V rms Reinforced insulation at 150 V rms CSA/IEC 61010-1: Basic insulation at 300 V rms Reinforced insulation at 150 V rms	File No. 205078
VDE	IEC 60747-17: Reinforced insulation at 560 V peak	Certificate No. 40011599
CQC	GB 4943.1: Basic insulation at 400 V rms Reinforced insulation at 150 V rms	Certificate No. CQC14001108691
TÜV Süd	EN/UL 60950-1: Basic insulation at 400 V rms Reinforced insulation at 200 V rms	Certificate No. U8V 16 05 56232 017

[1] Working voltages are quoted for Pollution Degree 2, Material Group III and Overvoltage Category II except where otherwise specified. ADuM1250/ADuM1251 case material has been evaluated by CSA as Material Group II.

SPECIFICATIONS

RECOMMENDED OPERATING CONDITIONS

Table 5.

Parameter	Rating
Ambient Operating Temperature (T_A)	
A Grade	−40°C to +105°C
S, W Grades	−40°C to +125°C
Supply Voltages[1]	
V_{DD1}	3.0 V to 5.5 V
V_{DD2}	3.0 V to 5.5 V
Input/Output Signal Voltage	
V_{SDA1}, V_{SCL1}	0 V to V_{DD1}
V_{SDA2}, V_{SCL2}	0 V to V_{DD2}
Capacitive Load	
Side 1 (C_{L1})	40 pF
Side 2 (C_{L2})	400 pF
Static Output Loading	
Side 1 (I_{SDA1}, I_{SCL1})	0.5 mA to 3 mA
Side 2 (I_{SDA2}, I_{SCL2})	0.5 mA to 30 mA

[1] All voltages are relative to their respective ground. See the Magnetic Field Immunity section for information about immunity to external magnetic fields.

ABSOLUTE MAXIMUM RATINGS

Ambient temperature = 25°C, unless otherwise noted.

Table 6. Absolute Maximum Ratings

Parameter	Rating
Storage Temperature (T_{ST})	−55°C to +150°C
Ambient Operating Temperature (T_A)	
A Grade	−40°C to +105°C
S, W Grades	−40°C to +125°C
Supply Voltages	
V_{DD1} to GND_1	−0.5 V to +7.0 V
V_{DD2} to GND_2	−0.5 V to +7.0 V
Input/Output Voltage[1]	
Side 1 (V_{SDA1}, V_{SCL1})	−0.5 V to V_{DD1} + 0.5 V
Side 2 (V_{SDA2}, V_{SCL2})	−0.5 V to + 7.0 V
Average Output Current per Pin	
Side 1 (I_{O1})	±18 mA
Side 2 (I_{O2})	±100 mA
Common-Mode Transients[2]	−100 kV/µs to +100 kV/µs

1 All voltages are relative to their respective ground.

2 Refers to common-mode transients across the insulation barrier. Common-mode transients exceeding the absolute maximum rating may cause latch-up or permanent damage.

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

THERMAL CHARACTERISTICS

Thermal performance is directly linked to PCB design and operating environment. Careful attention to the PCB thermal design is required.

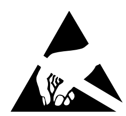
Thermal resistance and characterization parameter values specified in Table 7 are defined and calculated based on the JEDEC JESD51 standards. For more details on their definition and usage, see JEDEC JESD51-12 and the Thermal Analysis section.

Table 7. Package Thermal Data

Package Type	θ_{JA}	θ_{JB}	Ψ_{JB}	Ψ_{JT}	Unit
SOIC8_N[1]	89	71	59	2.7	°C/W

1 Thermal impedance simulated values are based on JEDEC 2S2P thermal test board with no vias and still air.

ESD CAUTION



ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

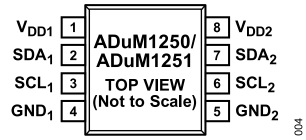


Figure 4. ADuM1250/ADuM1251 Pin Configuration

Table 8. ADuM1250 Pin Function Descriptions

Pin No.	Mnemonic	Description
1	V_{DD1}	Supply Voltage, 3.0 V to 5.5 V.
2	SDA_1	Data Input/Output, Side 1.
3	SCL_1	Clock Input/Output, Side 1.
4	GND_1	Ground 1. Ground reference for Isolator Side 1.
5	GND_2	Ground 2. Isolated ground reference for Isolator Side 2.
6	SCL_2	Clock Input/Output, Side 2.
7	SDA_2	Data Input/Output, Side 2.
8	V_{DD2}	Supply Voltage, 3.0 V to 5.5 V.

Table 9. ADuM1251 Pin Function Descriptions

Pin No.	Mnemonic	Description
1	V_{DD1}	Supply Voltage, 3.0 V to 5.5 V.
2	SDA_1	Data Input/Output, Side 1.
3	SCL_1	Clock Input, Side 1.
4	GND_1	Ground 1. Ground reference for Isolator Side 1.
5	GND_2	Ground 2. Isolated ground reference for Isolator Side 2.
6	SCL_2	Clock Output, Side 2.
7	SDA_2	Data Input/Output, Side 2.
8	V_{DD2}	Supply Voltage, 3.0 V to 5.5 V.

TEST CONDITIONS

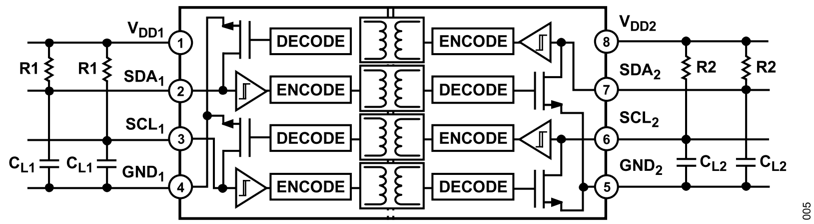


Figure 5. Timing Test Diagram

APPLICATIONS INFORMATION

FUNCTIONAL DESCRIPTION

The ADuM1250/ADuM1251 interface on each side to a bidirectional I^2C signal. Internally, the I^2C interface is split into two unidirectional channels communicating in opposing directions via a dedicated *i*Coupler isolation channel for each. One channel (the bottom channel of each channel pair shown in Figure 6) senses the voltage state of the Side 1 I^2C pin and transmits its state to its respective Side 2 I^2C pin.

Both the Side 1 and the Side 2 I^2C pins are designed to interface to an I^2C bus operating in the 3.0 V to 5.5 V range. A logic low on either pin causes the opposite pin to be pulled low enough to comply with the logic low threshold requirements of other I^2C devices on the bus. Avoidance of I^2C bus contention is ensured by an input low threshold at SDA_1 or SCL_1 guaranteed to be at least 50 mV less than the output low signal at the same pin. This prevents an output logic low at Side 1 being transmitted back to Side 2 and pulling down the I^2C bus.

Because the Side 2 logic levels/thresholds are standard I^2C values, multiple ADuM1250/ADuM1251 devices connected to a bus by their Side 2 pins can communicate with each other and with other I^2C compatible devices. A distinction is made between I^2C compatibility and I^2C compliance. I^2C compatibility refers to situations in which the logic levels of a component do not necessarily meet the requirements of the I^2C specification but still allow the component to communicate with an I^2C compliant device. I^2C compliance refers to situations in which the logic levels of a component meet the requirements of the I^2C specification.

However, because the Side 1 pin has a modified output level/ input threshold, this side of the ADuM1250/ADuM1251 can communicate only with devices that conform to the I^2C standard. In other words, Side 2 of the ADuM1250/ADuM1251 is I^2C compliant, whereas Side 1 is only I^2C compatible.

The output logic low levels are independent of the V_{DD1} and V_{DD2} voltages. The input logic low threshold at Side 1 is also independent of V_{DD1}. However, the input logic low threshold at Side 2 is designed to be at 0.3 V_{DD2}, consistent with I^2C requirements. The Side 1 and Side 2 pins have open-collector outputs whose high levels are set via pull-up resistors to their respective supply voltages.

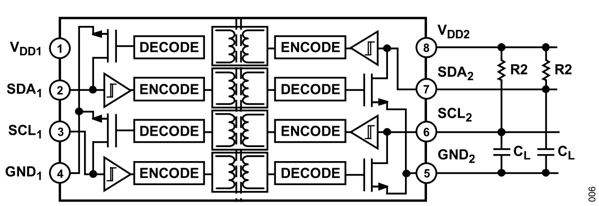


Figure 6. ADuM1250 Block Diagram

STARTUP

Both the V_{DD1} and V_{DD2} supplies have an undervoltage lockout feature to prevent the signal channels from operating unless certain criteria are met. This feature prevents input logic low signals from pulling down the I^2C bus inadvertently during power-up/power-down.

For the signal channels to be enabled, the following two criteria must be met:

- Both supplies must be at least 2.5 V.
- At least 40 μs must elapse after both supplies exceed the internal startup threshold of 2.0 V.

Until both criteria are met for both supplies, the ADuM1250/ADuM1251 outputs are pulled high, ensuring a startup that avoids any disturbances on the bus. Figure 7 and Figure 8 illustrate the supply conditions for fast and slow input supply slew rates.

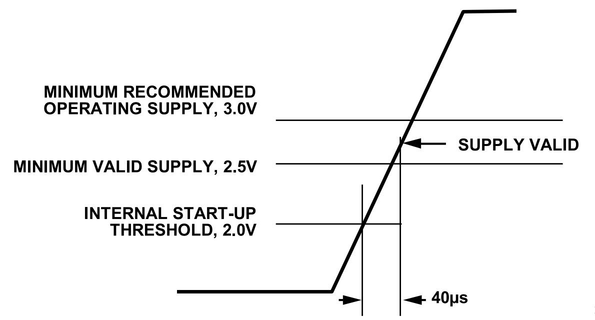


Figure 7. Start-Up Condition, Supply Slew Rate > 12.5 V/ms

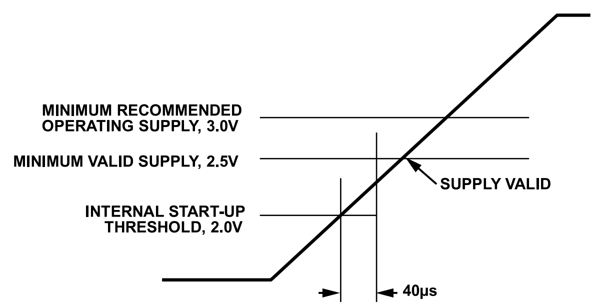


Figure 8. Start-Up Condition, Supply Slew Rate < 12.5 V/ms

TYPICAL APPLICATION DIAGRAM

Figure 9 shows a typical application circuit including the pull-up resistors required for both Side 1 and Side 2 buses. Bypass capacitors with values from 0.01 μF to 0.1 μF are required between V_{DD1} and GND_1 and between V_{DD2} and GND_2. The 200 Ω resistor shown in Figure 9 is required for latch-up immunity when hot plugging if the ambient temperature is between 105°C and 125°C, and must be placed on the side being hot plugged. Use 200 Ω for 5 V V_{DD1} and 91 Ω for 3.3 V V_{DD1}.

APPLICATIONS INFORMATION

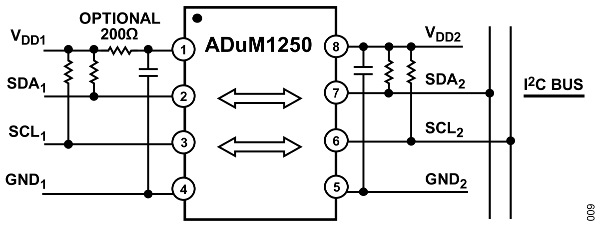


Figure 9. Typical Isolated I²C Interface Using the ADuM1250

CAPACITIVE LOAD AT LOW SPEEDS

The ADuM1250/ADuM1251 are designed for operation at speeds up to 1 Mbps. Due to the limited current available on Side 1, operation at 1 Mbps limits the capacitance that can be driven at the minimum pull-up value to 40 pF.

Most applications operate at 100 kbps in standard mode or 400 kbps in fast mode. At these lower operating speeds, the limitation on the load capacitance can be significantly relaxed. Table 10 shows the maximum capacitance at minimum pull-up values for standard and fast operating modes. If larger values for the pull up resistor are used, the maximum supported capacitance must be scaled down proportionately so that the rise time does not increase beyond the values required by the standard.

Table 10. Side 1 Maximum Load Conditions

Maximum Capacitive Load for Side 1						
Mode	**V_{DD1}**	**Data Rate (kbps)**	**t_r (ns)**	**t_f (ns)**	**R_1 (Ω)**	**C_{L1} (pF)**
Standard	5	100	1000	187	1600	484
Fast	5	400	300	172	1600	120
Standard	3.3	100	1000	270	1000	771
Fast	3.3	400	300	235	1000	188

APPLICATIONS INFORMATION

THERMAL ANALYSIS

The ADuM1250/ADuM1251 consist of two internal die attached to a split lead frame with two die attach pads. For the purposes of thermal analysis, the die are treated as a single thermal unit, with the highest junction temperature reflected in the thermal parameter values from Table 7. The thermal parameter values are based on thermal simulations with the devices mounted on a JEDEC standard, 4-layer board with fine width traces and still air.

θ_{JA} and θ_{JB} are mainly used to compare the thermal performance of the package of the device with other semiconductor packages when all test conditions listed are similar. θ_{JA} and θ_{JB} can be used for first order approximation of the junction temperature in the system environment.

If an accurate thermal measurement of the board temperature near the device under test or directly on the package top surface operating in the system environment is available along with the corresponding device power dissipation, then using Ψ_{JB} or Ψ_{JT} is a more appropriate way to estimate the junction temperature in the system environment. Use Ψ_{JB} when the temperature measurement point is on the board or Ψ_{JT} when it is on the package top. The junction temperature is estimated using the following equation:

$$T_J = \psi_{Jx} \times P_d + T_x \quad (1)$$

where:
P_d is the dissipated power.
T_x is the measured temperature at location *x* and *x* is either *B* for the PCB or *T* for the package top.

The temperature measurement point for θ_{JB} and Ψ_{JB} is between Pin 6 and Pin 7 on the outer edge of the pin footprint. The temperature measurement point for Ψ_{JT} is at the center of the top side package.

MAGNETIC FIELD IMMUNITY

The ADuM1250/ADuM1251 are extremely immune to external magnetic fields. The limitation on the magnetic field immunity of the ADuM1250/ADuM1251 is set by the condition in which induced voltage in the receiving coil of the transformer is sufficiently large to either falsely set or reset the decoder. The following analysis defines the conditions under which this may occur. The 3 V operating condition of the ADuM1250/ADuM1251 is examined because it represents the most susceptible mode of operation.

The pulses at the transformer output have an amplitude greater than 1.0 V. The decoder has a sensing threshold at approximately 0.5 V, thus establishing a 0.5 V margin in which induced voltages can be tolerated. The voltage induced across the receiving coil is given by

$$V = (-d\beta/dt) \sum \pi r_n^2;\ n = 1, 2, \ldots, N \quad (2)$$

where:
β is the magnetic flux density (gauss).
r_n is the radius of the nth turn in the receiving coil (cm).
N is the total number of turns in the receiving coil.

Given the geometry of the receiving coil in the ADuM1250 and the ADuM1251 and an imposed requirement that the induced voltage be, at most, 50% of the 0.5 V margin at the decoder, a maximum allowable magnetic field is calculated as shown in Figure 10.

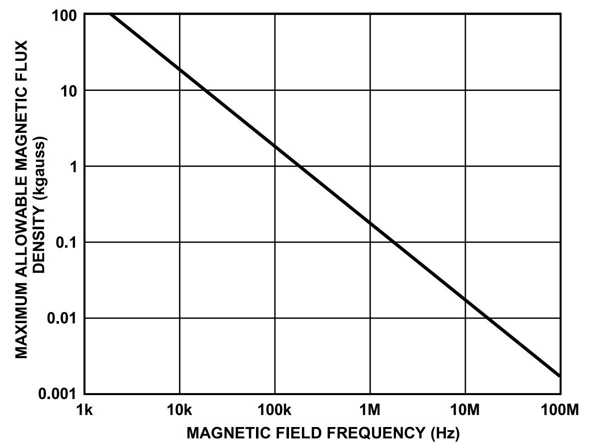


Figure 10. Maximum Allowable External Magnetic Flux Density

For example, at a magnetic field frequency of 1 MHz, the maximum allowable magnetic field of 0.2 kgauss induces a voltage of 0.25 V at the receiving coil. This voltage is approximately 50% of the sensing threshold and does not cause a faulty output transition. Similarly, if such an event occurs during a transmitted pulse (and is of the worst-case polarity), it reduces the received pulse from >1.0 V to 0.75 V, still well above the 0.5 V sensing threshold of the decoder.

The preceding magnetic flux density values correspond to specific current magnitudes at given distances away from the ADuM1250/ADuM1251 transformers. Figure 11 expresses these allowable current magnitudes as a function of frequency for selected distances. As shown in Figure 11 the ADuM1250/ADuM1251 are extremely immune and can be affected only by extremely large currents operated at high frequency very close to the component. For the 1 MHz example, a 0.5 kA current placed 5 mm away from the ADuM1250/ADuM1251 is required to affect the operation of the component.

APPLICATIONS INFORMATION

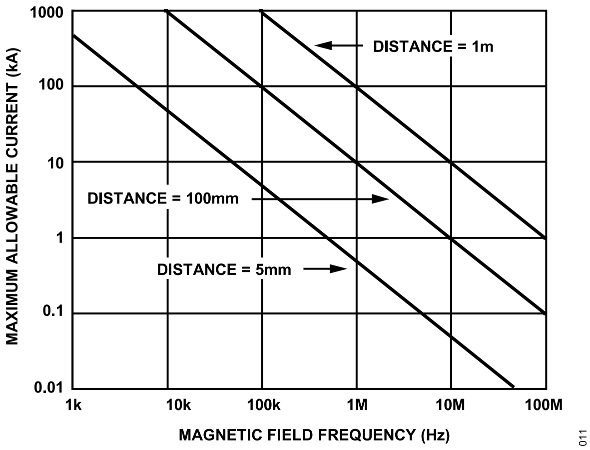


Figure 11. Maximum Allowable Current for Various Current-to-ADuM1250/ ADuM1251 Spacings

Note that at combinations of strong magnetic field and high frequency, any loops formed by PCB traces can induce error voltages sufficiently large to trigger the thresholds of succeeding circuitry. Exercise care in the layout of such traces to avoid this possibility.

OUTLINE DIMENSIONS

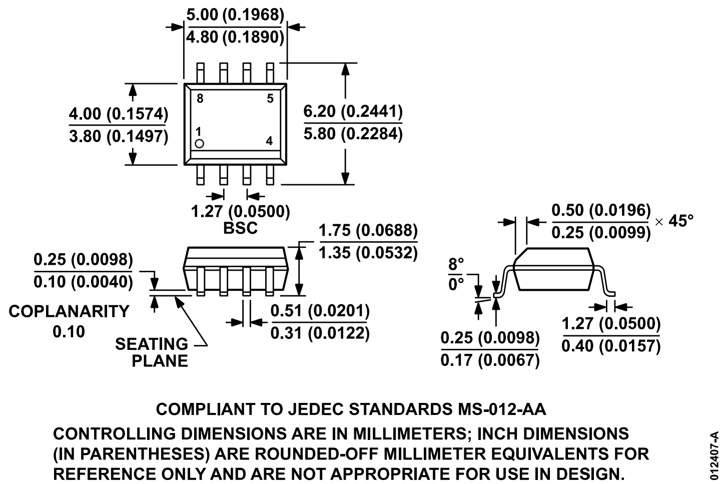


Figure 12. 8-Lead Standard Small Outline Package [SOIC_N]
Narrow Body
(R-8)
Dimensions shown in millimeters and (inches)

ORDERING GUIDE

Model[1, 2]	Temperature Range	Package Description	Packing Quantity	Package Option
ADUM1250ARZ	-40°C to +105°C	8-Lead SOIC	Tube, 98	R-8
ADUM1250ARZ-RL7	-40°C to +105°C	8-Lead SOIC	Reel, 1000	R-8
ADUM1250SRZ	-40°C to +125°C	8-Lead SOIC	Tube, 98	R-8
ADUM1250SRZ-RL7	-40°C to +125°C	8-Lead SOIC	Reel, 1000	R-8
ADUM1250WSRZ	-40°C to +125°C	8-Lead SOIC	Tube, 98	R-8
ADUM1250WSRZ-RL7	-40°C to +125°C	8-Lead SOIC	Reel, 1000	R-8
ADUM1251ARZ	-40°C to +105°C	8-Lead SOIC	Tube, 98	R-8
ADUM1251ARZ-RL7	-40°C to +105°C	8-Lead SOIC	Reel, 1000	R-8
ADUM1251WARZ	-40°C to +125°C	8-Lead SOIC	Tube, 98	R-8
ADUM1251WARZ-RL7	-40°C to +125°C	8-Lead SOIC	Reel, 1000	R-8

[1] Z = RoHS Compliant Part.

[2] W = Qualified for Automotive Applications.

EVALUATION BOARDS

Model[1]	Description
EVAL-ADuM1250EBZ	Evaluation Board

[1] EVAL-ADuM1250EBZ is RoHS compliant.

AUTOMOTIVE PRODUCTS

The ADuM1250W and ADuM1251W models are available with controlled manufacturing to support the quality and reliability requirements of automotive applications. Note that these automotive models may have specifications that differ from the commercial models; therefore, designers should review the Specifications section of this data sheet carefully. Only the automotive grade products shown are available for use in automotive applications. Contact your local Analog Devices account representative for specific product ordering information and to obtain the specific Automotive Reliability reports for these models.

I^2C refers to a communications protocol originally developed by Philips Semiconductors (now NXP Semiconductors).