

8T8R SoC with DFE, 400 MHz iBW RF Transceiver

FEATURES

- ▶ Eight differential transmitters (Tx)
- ▶ Eight differential receivers (Rx)
- ▶ Two differential observation receivers (ORx)
- ▶ Tunable range: 600 MHz to 7125 MHz
- ▶ Single-band and Multiband (N x 2T2R/4T4R) capability
- ▶ Four individual band profiles within tunable range (band profiles define bandwidth and aggregate sampling rate of a channel)
- ▶ ADRV9040BBPZ-WB supports DPD for 400 MHz iBW/OBW
- ▶ Simplifying system thermal solution
 - ▶ 13 W power consumption for all blocks enabled (use case is TDD 200 MHz instantaneous bandwidth and 200 MHz occupied bandwidth, with all blocks (DPD, CFR, and CDUC/CDDC) enabled)
 - ▶ 125°C maximum junction temperature for intermittent operation, 110°C for continuous (operating lifetime impact at >110°C can be offset by operation at <110°C based on acceleration factors)

- ▶ Fully integrated DFE (DPD, CDUC, CDDC, and CFR) engine that reduces FPGA resources and halves SERDES lane rate
 - ▶ DPD adaptation engine for power amplifier linearization
 - ▶ CDUC/CDDC—maximum eight component carriers (CCs) per each transmitter/receiver channel
 - ▶ Multistage CFR engine
- ▶ Supports DTx (micro sleep) power saving mode in downlink
- ▶ Supports JESD204B and JESD204C digital interface
- ▶ Multichip phase synchronization for all local oscillator (LO) and baseband clocks
- ▶ Dual fully integrated fractional-N RF synthesizers
- ▶ Fully integrated clock synthesizer

APPLICATIONS

- ▶ 3G/4G/5G time division duplex (TDD)/frequency division duplex (FDD) small cell, massive MIMO, and macro base stations

FUNCTIONAL BLOCK DIAGRAM

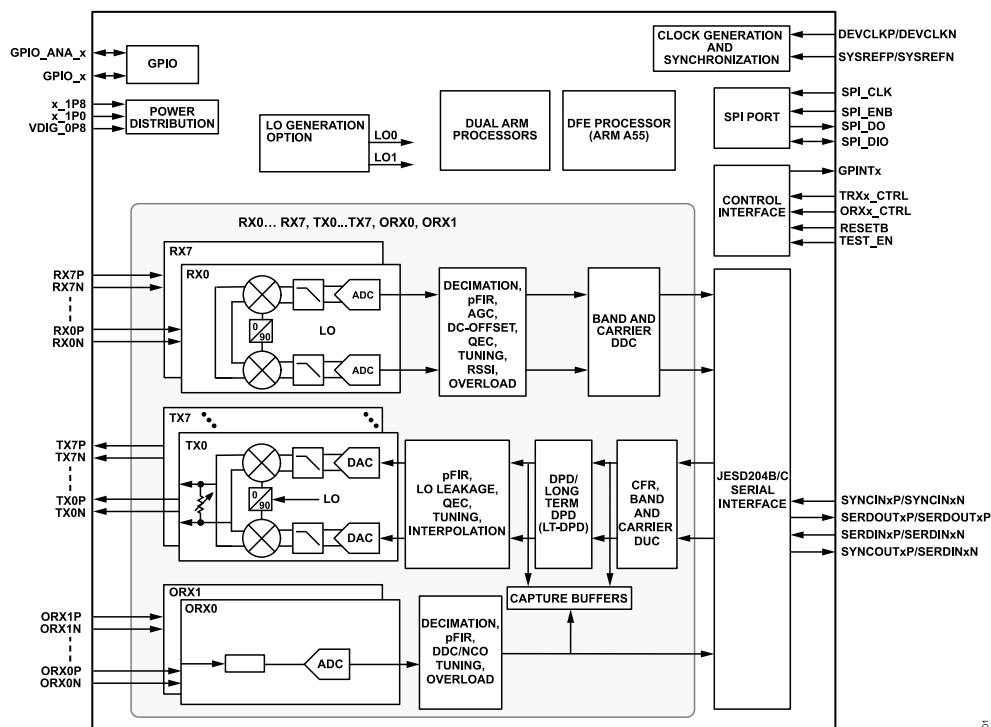


Figure 1. Functional Block Diagram

For more details on the ADRV9040, contact the local Analog Devices, Inc., sales office at radioverse@analog.com.

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