Die on Carrier, Silicon SP4T Switch, Nonreflective, 100 MHz to 45 GHz

FEATURES

- Ultrawideband frequency range: 100 MHz to 45 GHz
- Nonreflective 50 Ω design
- Low insertion loss
  - 1.4 dB at 18 GHz typical
  - 2.4 dB at 40 GHz typical
  - 3.5 dB at 45 GHz typical
- High isolation
  - 55 dB at 18 GHz typical
  - 42 dB at 40 GHz typical
  - 43 dB at 45 GHz typical
- High input linearity
  - P0.1dB: 29 dBm typical
  - IIP3: 52 dBm typical
- High power handling
  - 29 dBm through path
  - 17.5 dBm terminated path
  - 29 dBm hot switching
- No low frequency spurs
- On and off time (50% V_{CTRL} to 10% to 90% of RF_{OUT}): 20 ns
- 0.1 dB settling time (50% V_{CTRL} to 0.1 dB of final RF_{OUT}): 60 ns
- 33-pad, 2.971 mm × 3.021 mm, Bare Die [CHIP]

APPLICATIONS

- Industrial scanners
- Test instrumentation
- Cellular infrastructure mmWave 5G
- Military radios, radars, and electronic counter measures (ECMs)
- Microwave radios and very small aperture terminals (VSATs)

FUNCTIONAL BLOCK DIAGRAM

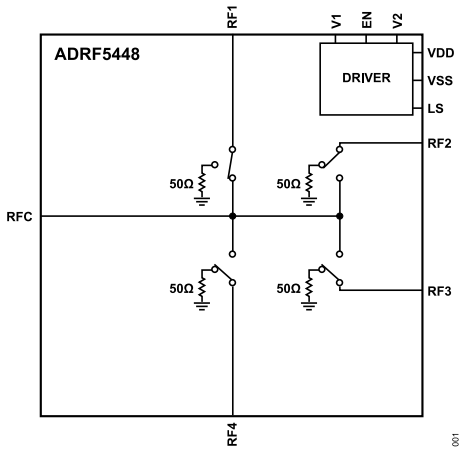


Figure 1. Functional Block Diagram

GENERAL DESCRIPTION

The ADRF5448 is a nonreflective, SP4T switch manufactured in the silicon process attached on a gallium arsenide (GaAs) carrier substrate. The substrate incorporates the bond pads for chip and wire assembly, and the bottom of the device is metalized, connected to ground.

The ADRF5448 operates from 100 MHz to 45 GHz with insertion loss less than 3.5 dB and isolation higher than 40 dB. The device has an RF input, power handling capability of 29 dBm for the through path, 17.5 dBm for the terminated path, and 29 dBm for the hot switching.

The ADRF5448 requires a positive supply (V_{DD}) of +3.3 V and a negative supply (V_{SS}) of −3.3 V. The device employs complementary metal-oxide semiconductor (CMOS)-/low-voltage transistor to transistor logic (LVTTL)-compatible controls.

The ADRF5448 is designed to match a characteristic impedance of 50 Ω and can operate from −40°C to +105°C.

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REVISION HISTORY

5/2026—Rev. 0 to Rev. A

Changes to Handling, Mounting, and Epoxy Die Attach Section ... 13
Updated Outline Dimensions ... 14

6/2024—Revision 0: Initial Version

SPECIFICATIONS

V_{DD} = +3.3 V, V_{SS} = −3.3 V, control voltage (V_{CTRL}) = 0 V or V_{DD}, T_{DIE} = 25°C, and a 50 Ω system, unless otherwise noted. RFx refers to RF1 to RF4.

Table 1. Specifications

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
FREQUENCY RANGE	f		0.1		45	GHz
INSERTION LOSS						
Between RFC and RFx (On)		100 MHz to 18 GHz		1.4		dB
		18 GHz to 26 GHz		1.7		dB
		26 GHz to 35 GHz		2.2		dB
		35 GHz to 40 GHz		2.4		dB
		40 GHz to 45 GHz		3.5		dB
ISOLATION						
Between RFC and RFx (Off)		100 MHz to 18 GHz		55		dB
		18 GHz to 26 GHz		46		dB
		26 GHz to 35 GHz		42		dB
		35 GHz to 40 GHz		40		dB
		40 GHz to 45 GHz		40		dB
Between RFC and RFx (Off)		100 MHz to 18 GHz		55		dB
		18 GHz to 26 GHz		50		dB
		26 GHz to 35 GHz		44		dB
		35 GHz to 40 GHz		42		dB
		40 GHz to 45 GHz		43		dB
RETURN LOSS						
RFC		100 MHz to 18 GHz		16		dB
		18 GHz to 26 GHz		22		dB
		26 GHz to 35 GHz		17		dB
		35 GHz to 40 GHz		18		dB
		40 GHz to 45 GHz		11		dB
RFx (On)		100 MHz to 18 GHz		20		dB
		18 GHz to 26 GHz		17		dB
		26 GHz to 35 GHz		15		dB
		35 GHz to 40 GHz		16		dB
		40 GHz to 45 GHz		11		dB
RFx (Off)		100 MHz to 18 GHz		17		dB
		18 GHz to 26 GHz		15		dB
		26 GHz to 35 GHz		13		dB
		35 GHz to 40 GHz		13		dB
		40 GHz to 45 GHz		13		dB
SWITCHING						
Rise Time and Fall Time	t_{RISE}, t_{FALL}	90% to 10% of RF output (RF_{OUT})		4		ns
On Time and Off Time	t_{ON}, t_{OFF}	50% V_{CTRL} to 10% to 90% of RF_{OUT}		20		ns
0.1 dB Settling Time		50% V_{CTRL} to 0.1 dB of final RF_{OUT}		60		ns
INPUT LINEARITY[1]						
0.1 dB Power Compression	P0.1dB	f = 0.3 GHz to 40 GHz		29		dBm
Third-Order Intercept	IIP3	Two-tone input power = 14 dBm continuous wave per tone, f = 1 GHz to 40 GHz, Δf = 1 MHz		52		dBm
SUPPLY CURRENT		VDD and VSS				
Positive Supply Current	I_{DD}			150		µA
Negative Supply Current	I_{SS}			520		µA

SPECIFICATIONS

Table 1. Specifications (Continued)

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
DIGITAL CONTROL INPUTS						
Voltage						
Low	V_{INL}		0		0.8	V
High	V_{INH}		1.2		3.45	V
Current						
Low	I_{INL}			<1		µA
High	I_{INH}	V1 and V2		<1		µA
		EN and LS		33		µA
RECOMMENDED OPERATING CONDITIONS						
Supply Voltage						
Positive	V_{DD}		3.15		3.45	V
Negative	V_{SS}		−3.45		−3.15	V
Digital Control Inputs Voltages		EN and LS	0		V_{DD}	V
RF Input Power[2, 3]		f = 0.3 GHz to 40 GHz, T_{CASE} = 85°C, life time				
Through Path		RF signal is applied to RFC or through the connected RF throw port (selected RFx)			29	dBm
Terminated Path		RF signal is applied to the unselected RFx			17.5	dBm
Hot Switching		RF signal is applied to RFC while switching between the RFx ports			29	dBm
Case Temperature	T_{CASE}		–40		+105	°C

[1] For input linearity performance over frequency, see Figure 20 to Figure 23.

[2] For power derating over frequency, see Figure 2 and Figure 3.

[3] For 105°C operation, the power handling degrades from the T_{CASE} = 85°C specification by 3 dB.

ABSOLUTE MAXIMUM RATINGS

Table 2. Absolute Maximum Ratings

Parameter	Rating
Supply Voltage	
Positive	−0.3 V to +3.6 V
Negative	−3.6 V to +0.3 V
Digital Control Input Voltage	
Voltage	−0.3 V to V_{DD} + 0.3 V
Current	3 mA
RF Input Power[1] (V_{DD} = 3.3 V, V_{SS} = −3.3 V, f = 250 MHz to 40 GHz, T_{CASE} = 85°C[2])	
Through Path	29.5 dBm
Terminated Path	18 dBm
Hot Switching	29.5 dBm
RF Power Under Unbiased Condition (V_{DD}, V_{SS} = 0 V)	10 dBm
Temperature	
Junction (T_J)	135°C
Storage	−65°C to +150°C
Reflow	260°C

1 For power derating over frequency, see Figure 2 and Figure 3.

2 For 105°C operation, the power handling degrades from the T_{CASE} = 85°C specifications by 3 dB.

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

Only one absolute maximum rating can be applied at any one time.

THERMAL RESISTANCE

Thermal performance is directly linked to printed circuit board (PCB) design and operating environment. Careful attention to PCB thermal design is required.

θ_{JC} is the junction to case bottom (channel to package bottom) thermal resistance.

Table 3. Thermal Resistance

Package Type	θ_{JC}[1]	Unit
C-33-1		
Through Path	110	°C/W
Terminated Path	900	°C/W

1 θ_{JC} is determined by simulation under the following conditions: the heat transfer is due solely to the thermal conduction from the channel through the ground pad to the PCB, and the ground pad is held constant at the operating temperature of 85°C.

POWER DERATING CURVES

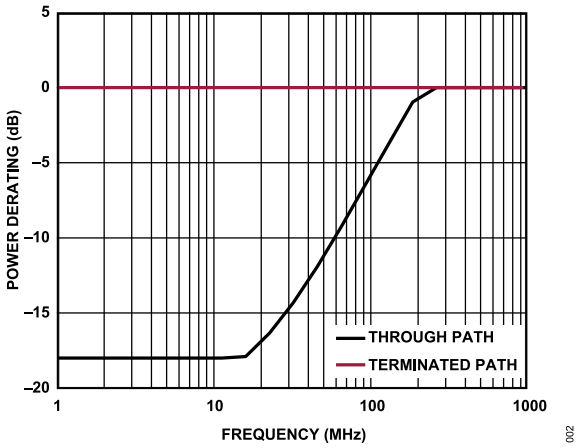


Figure 2. Power Derating vs. Frequency, Low Frequency Detail, T_{DIE} = 85°C

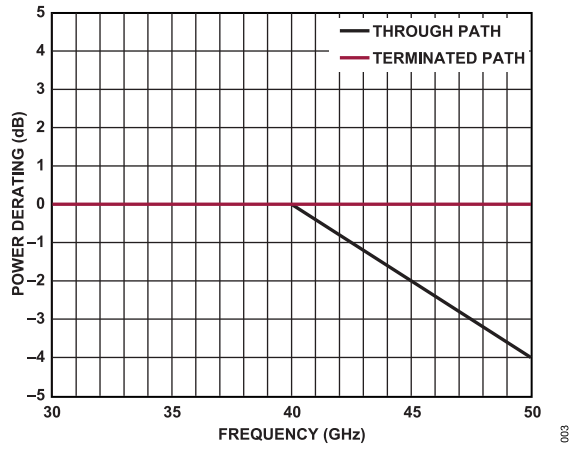


Figure 3. Power Derating vs. Frequency, High Frequency Detail, T_{DIE} = 85°C

ABSOLUTE MAXIMUM RATINGS

ELECTROSTATIC DISCHARGE (ESD) RATINGS

The following ESD information is provided for handling of ESD-sensitive devices in an ESD protected area only.

Human body model (HBM) per ANSI/ESDA/JEDEC JS-001.

ESD Ratings for ADRF5448

Table 4. ADRF5448, 33-Pad Bare Die [CHIP]

ESD Model	Withstand Threshold (V)	Class
HBM	±1000 for RF Pads	1C
	±2000 for Supply and Digital Control Pads	2

ESD CAUTION



ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

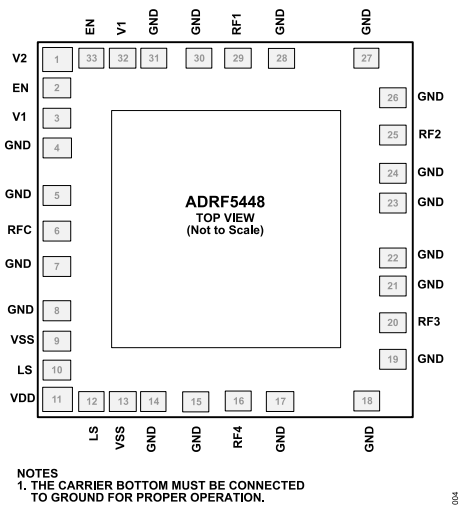


Figure 4. Pad Configuration

Table 5. Pad Function Descriptions

Pad No.	Mnemonic	Description
1	V2	Control Input 2. See Table 6 for the truth table and Figure 6 for the control interface schematic.
2, 33	EN	Enable Input. See Table 6 for the truth table and Figure 7 for the control interface schematic.
3, 32	V1	Control Input 1. See Table 6 for the truth table and Figure 6 for the control interface schematic.
4, 5, 7, 8, 14, 15, 17 to 19, 21 to 24, 26 to 28, 30, 31	GND	Ground. Bonding of these GND pads is optional. See the Applications Information section for more information.
6	RFC	RF Common Port. The RFC pin is DC-coupled to 0 V and AC matched to 50 Ω. No DC blocking capacitor is required when the RF line potential is equal to 0 V DC. See Table 6 for the truth table and Figure 5 for the interface schematic.
9, 13	VSS	Negative Supply Voltage.
10, 12	LS	Logic Select. See Table 6 for the truth table and Figure 7 for the control interface schematic.
11	VDD	Positive Supply Voltage.
16	RF4	RF Throw Port 4. The RF4 pad is DC-coupled to 0 V and AC matched to 50 Ω. No DC blocking capacitor is required when the RF line potential is equal to 0 V DC. See Table 6 for the truth table and Figure 5 for the interface schematic.
20	RF3	RF Throw Port 3. The RF3 pad is DC-coupled to 0 V and AC matched to 50 Ω. No DC blocking capacitor is required when the RF line potential is equal to 0 V DC. See Table 6 for the truth table and Figure 5 for the interface schematic.
25	RF2	RF Throw Port 2. The RF2 pad is DC-coupled to 0 V and AC matched to 50 Ω. No DC blocking capacitor is required when the RF line potential is equal to 0 V DC. See Table 6 for the truth table and Figure 5 for the interface schematic.
29	RF1	RF Throw Port 1. The RF1 pad is DC-coupled to 0 V and AC matched to 50 Ω. No DC blocking capacitor is required when the RF line potential is equal to 0 V DC. See Table 6 for the truth table and Figure 5 for the interface schematic.
	Carrier Bottom	The carrier bottom must be connected to ground for proper operation

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

INTERFACE SCHEMATICS

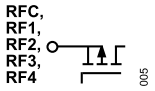


Figure 5. RF (RFC, RF1 to RF4) Interface Schematic

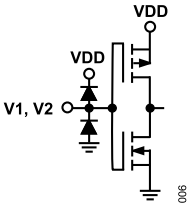


Figure 6. V1 to V2 Interface Schematic

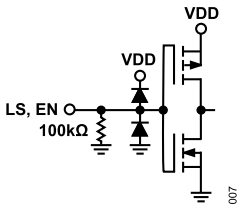


Figure 7. EN and LS Interface Schematic

TYPICAL PERFORMANCE CHARACTERISTICS

INSERTION LOSS, RETURN LOSS AND ISOLATION

V_{DD} = +3.3 V, V_{SS} = −3.3 V, V_{CTRL} = 0 V or V_{DD}, T_{DIE} = 25°C, and a 50 Ω system, unless otherwise noted.

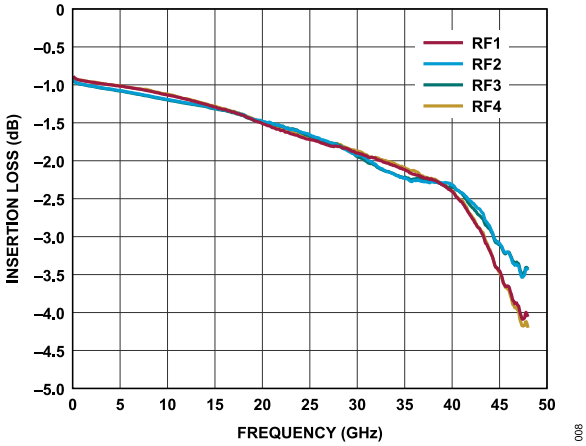


Figure 8. Insertion Loss for RFC to RFx Selected vs. Frequency

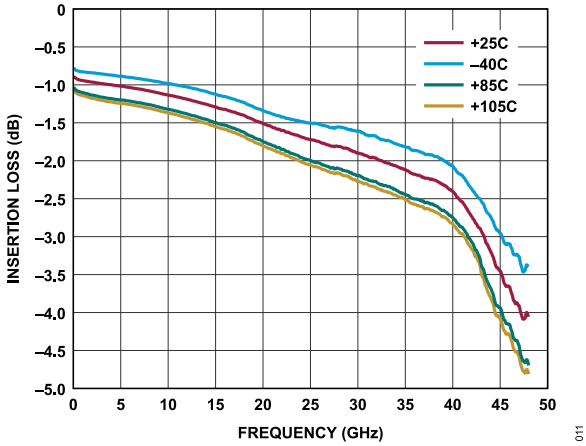


Figure 11. Insertion Loss for RFC to RF1 vs. Frequency over Temperature

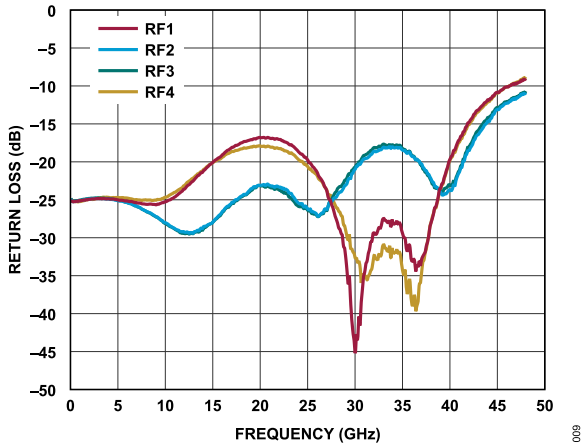


Figure 9. Return Loss for RFC when RFx Selected vs. Frequency

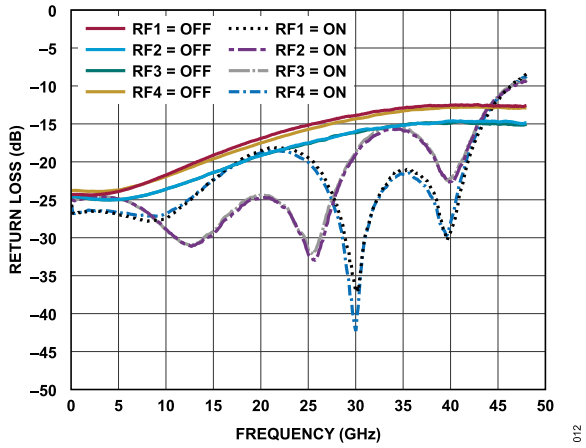


Figure 12. Return Loss for RFx Unselected and Selected

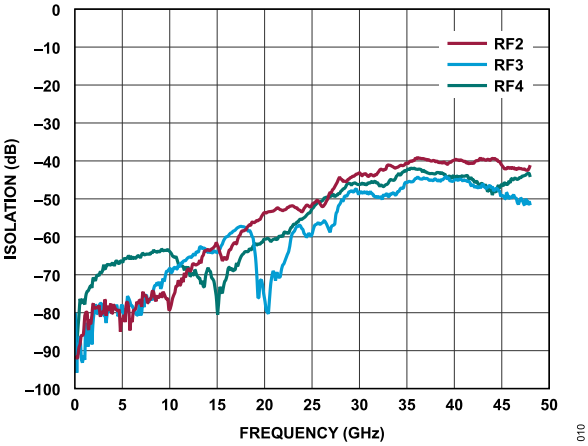


Figure 10. RFC to RF2, RF3, and RF4 Isolation vs. Frequency, RF1 Selected

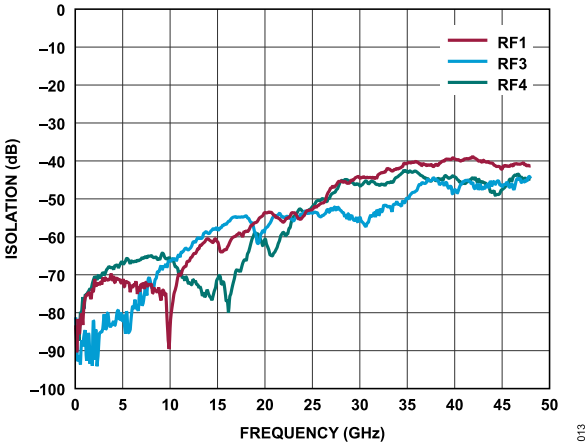


Figure 13. RFC to RF1, RF3, and RF4 Isolation vs. Frequency, RF2 Selected

TYPICAL PERFORMANCE CHARACTERISTICS

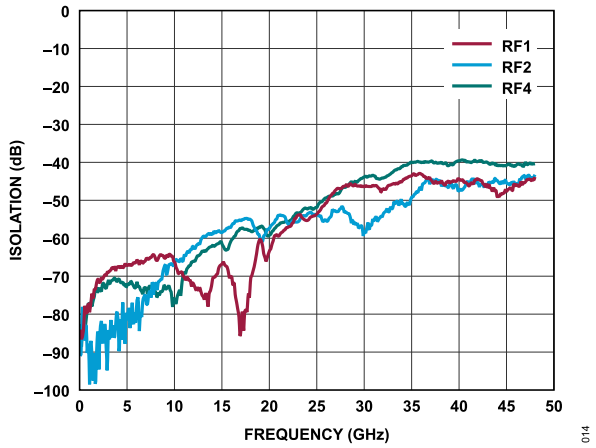


Figure 14. RFC to RF1, RF2, and RF4 Isolation vs. Frequency, RF3 Selected

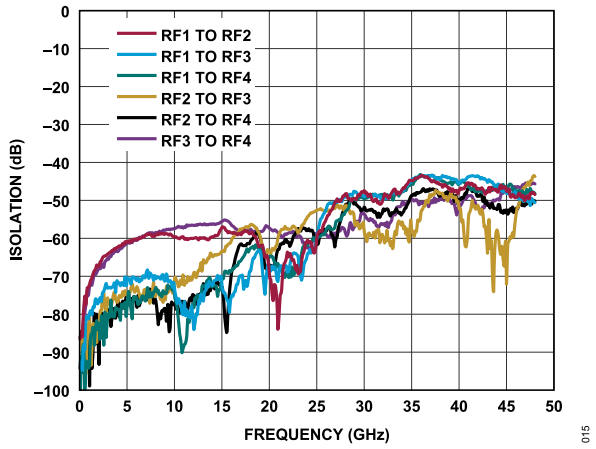


Figure 15. Channel to Channel Isolation vs. Frequency, RFC to RF1 Selected

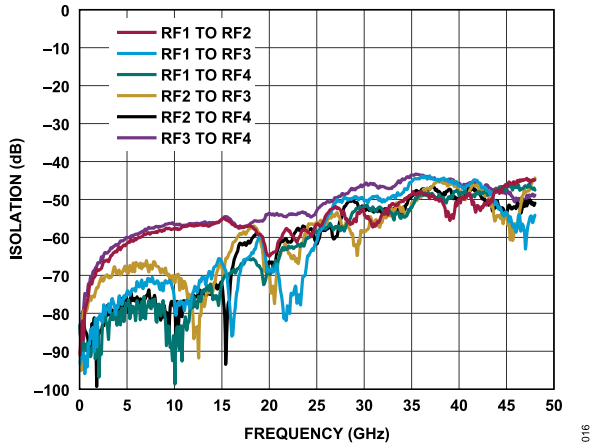


Figure 16. Channel to Channel Isolation vs. Frequency, RFC to RF3 Selected

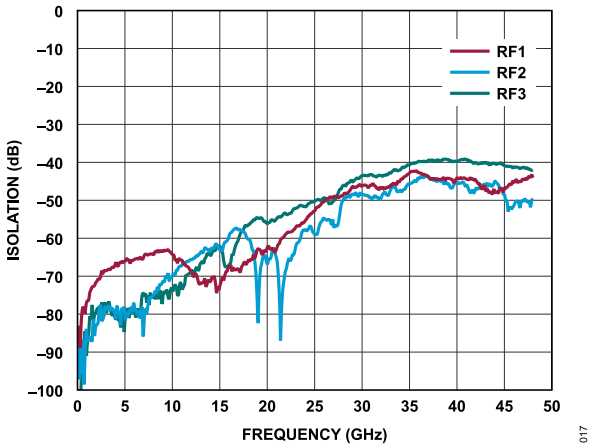


Figure 17. RFC to RF1, RF2, and RF3 Isolation vs. Frequency, RF4 Selected

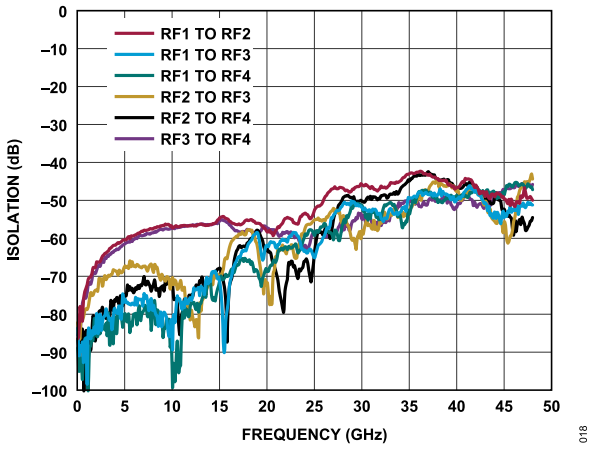


Figure 18. Channel to Channel Isolation vs. Frequency, RFC to RF2 Selected

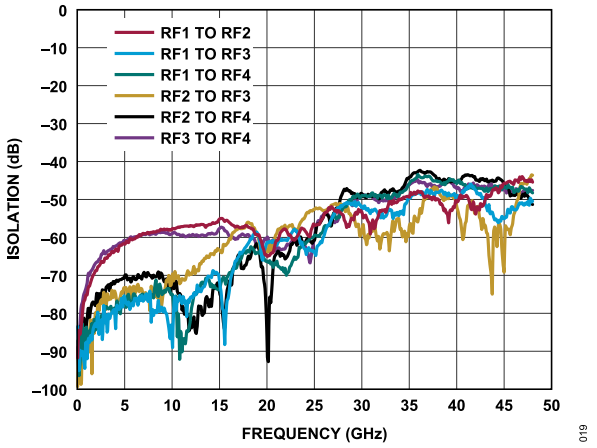


Figure 19. Channel to Channel Isolation vs. Frequency, RFC to RF4 Selected

TYPICAL PERFORMANCE CHARACTERISTICS

INPUT POWER COMPRESSION AND THIRD-ORDER INTERCEPT

V_{DD} = +3.3 V, V_{SS} = −3.3 V, V_{CTRL} = 0 V or V_{DD}, T_{DIE} = 25°C, and a 50 Ω system, unless otherwise noted.

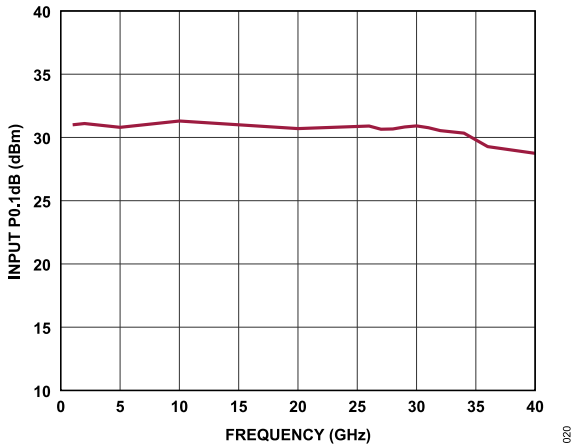


Figure 20. Input P0.1dB vs. Frequency

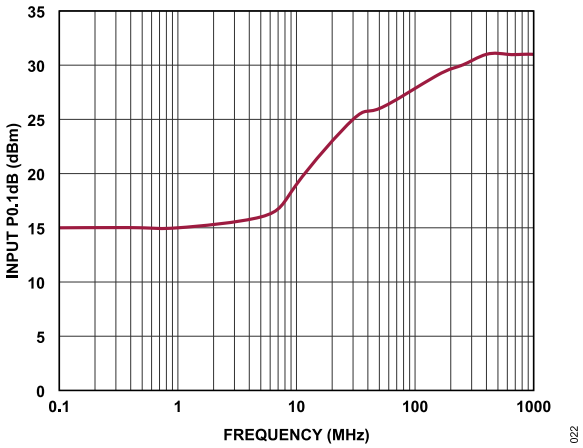


Figure 22. Input P0.1dB vs. Frequency, Low Frequency Detail

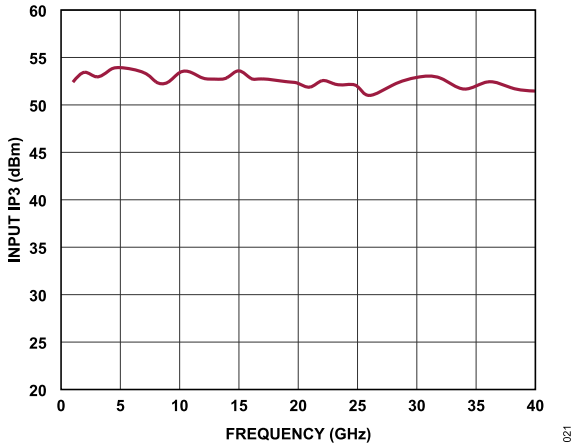


Figure 21. Input IP3 vs. Frequency

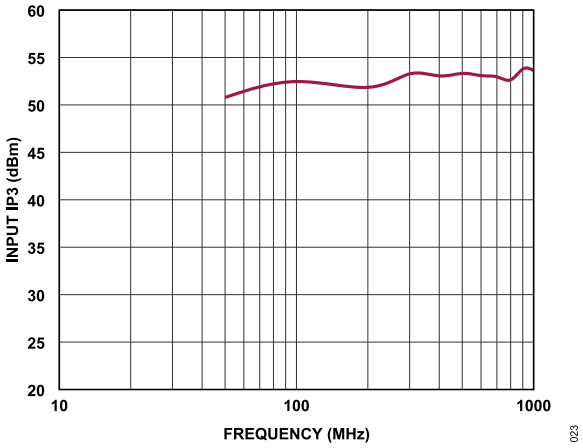


Figure 23. Input IP3 vs. Frequency, Low Frequency Detail

THEORY OF OPERATION

The ADRF5448 integrates a driver to perform the logic function internally and to provide the advantage of a simplified control interface. The driver features four digital control input pads (V1, V2, EN, and LS) that control the state of the RF paths, determining which RF port is in the insertion loss state and which RF port is in the isolation state, see Table 6.

The LS pad allows the user to define the control input logic sequence for the RF path selections. The logic level applied to the V1 and V2 pads determines which RF port is in the insertion loss state while the other three paths are in the isolation state.

When the EN pad is logic high, all four RF paths are in an isolation state regardless of the logic state of LS, V1, and V2. The RF ports are terminated to internal 50 Ω resistors, and RFC becomes reflective.

RF INPUT AND OUTPUT

All of the RF ports (RFC, RF1 to RF4) are DC-coupled to 0 V, and no DC blocking is required at the RF ports when the RF line potential is equal to 0 V.

The RF ports are internally matched to 50 Ω. Therefore, external matching networks are not required.

The insertion loss path conducts the RF signal between the RF common port and the selected RF throw port. The switch design is bidirectional with equal power handling capabilities. The RF input signal can be applied to the RF common port or the selected RF throw port. The isolation paths provide high loss between the insertion loss path and the unselected RF throw ports that are terminated to internal 50 Ω resistors.

POWER SUPPLY

The ADRF5448 requires a positive supply voltage applied to the VDD pad and a negative supply voltage applied to the VSS pad. Bypassing capacitors are recommended on the supply lines to filter high frequency noise.

The power-up sequence is as follows:

1. Connect to GND.
2. Power up V_{DD} and V_{SS}. Power up V_{SS} after V_{DD} to avoid current transients on V_{DD} during ramp up.
3. Power up the digital control inputs. The order of the digital control inputs is not important. However, powering the digital control inputs before the V_{DD} voltage supply can inadvertently forward bias and damage the internal ESD structures. To avoid this damage, use a series 1 kΩ resistor to limit the current flowing into the control pad. Use pull-up or pull-down resistors if the controller output is in a high impedance state after V_{DD} is powered up, and the control pads are not driven to a valid logic state.
4. Apply the RF signal.

The power-down sequence is the reverse order of the power-up sequence.

Table 6. Control Voltage Truth Table

Digital Control Inputs				RFx Paths			
EN	**LS**	**V1**	**V2**	**RF1 to RFC**	**RF2 to RFC**	**RF3 to RFC**	**RF4 to RFC**
Low	Low	Low	Low	Insertion loss (on)	Isolation (off)	Isolation (off)	Isolation (off)
Low	Low	High	Low	Isolation (off)	Insertion loss (on)	Isolation (off)	Isolation (off)
Low	Low	Low	High	Isolation (off)	Isolation (off)	Insertion loss (on)	Isolation (off)
Low	Low	High	High	Isolation (off)	Isolation (off)	Isolation (off)	Insertion loss (on)
Low	High	Low	Low	Isolation (off)	Isolation (off)	Isolation (off)	Insertion loss (on)
Low	High	High	Low	Isolation (off)	Isolation (off)	Insertion loss (on)	Isolation (off)
Low	High	Low	High	Isolation (off)	Insertion loss (on)	Isolation (off)	Isolation (off)
Low	High	High	High	Insertion loss (on)	Isolation (off)	Isolation (off)	Isolation (off)
High	Low or high	Low or high	Low or high	Isolation (off)	Isolation (off)	Isolation (off)	Isolation (off)

APPLICATIONS INFORMATION

DIE ASSEMBLY

An assembly diagram of the ADRF5448 is shown in Figure 24.

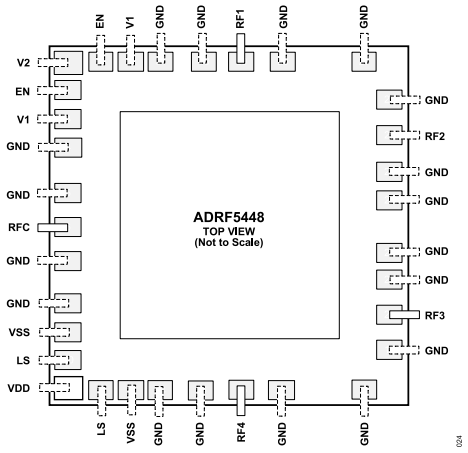


Figure 24. Die Assembly Diagram

The ADRF5448 is designed to have the optimum RF input and output impedance match with 3 mil × 0.5 mil gold ribbon wire and 3 mil loop height typical. The bonding diagrams are shown in Figure 25 and Figure 26. Alternatively, using multiple wire bonds with equivalent inductance yields similar performance. For RF routing from the device, coplanar wave guide or microstrip transmission lines can be used. No impedance matching is required on the transmission line pad because the device is designed to match internally to the recommended ribbon bond. A spacing of 3 mils from the RF transmission line to the device edge is recommended for optimum performance.

DC pads can be connected using standard 1 mil diameter wire by keeping the wire lengths as short as possible to minimize the parasitic inductance. The DC pads are large enough to accommodate ribbon bonds, if preferred.

All bonds must be thermosonically bonded at a nominal stage temperature of 150°C, and a minimum amount of ultrasonic energy must be applied to achieve reliable bonds.

The ADRF5448 is metalized on the backside, and the ground connection can be done by attaching the device directly to the RF ground plane using a conductive epoxy. In this case, connecting the ground pads is optional; however, still recommended to ensure a solid ground connection.

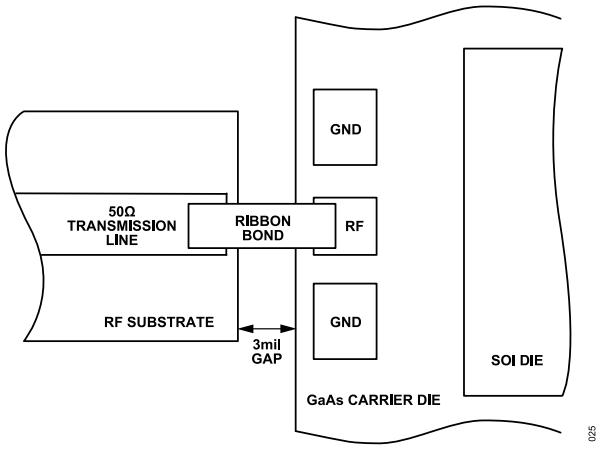


Figure 25. Bonding Diagram Top View

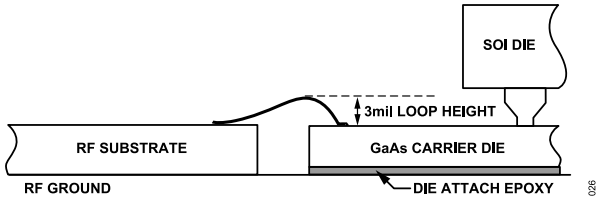


Figure 26. Bonding Diagram Side View

HANDLING, MOUNTING, AND EPOXY DIE ATTACH

Keep devices in ESD protective sealed bags for shipment, and store all bare die in a dry nitrogen environment.

For manual picking, it is a common practice to use a pair of tweezers for GaAs devices. However, for die on carrier devices, the use of a vacuum tool is recommended to avoid any damage on the device substrate. Handle these devices in a clean environment, and do not attempt to clean devices using liquid cleaning systems.

To attach the die with epoxy, apply an amount of epoxy to the mounting surface so that a thin epoxy fillet is observed around the perimeter of the chip after it is placed into position. Set epoxy cure temperatures per the recommendations of the manufacturer and the maximum ratings of the device to minimize accumulated mechanical stress after assembly.

Since both dies are attached with solder joints, users must follow best practices for the thermomechanical design of their module assemblies. The temperature expansion coefficient of the substrate material must match the thermal expansion coefficient of the GaAs and silicon (Si) die. Do not allow warpage or other mechanical deformation on the substrate. Set the die attach process and the epoxy cure temperatures to lower the accumulated stress after assembly.

OUTLINE DIMENSIONS

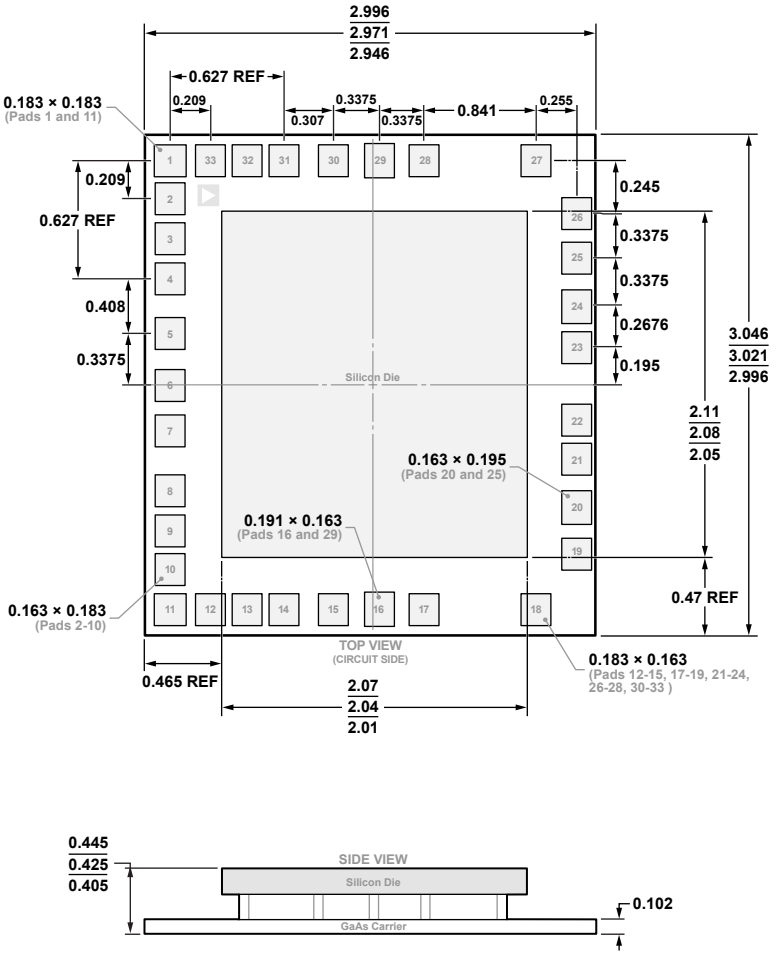


Figure 27. 33-Pad Bare Die [CHIP]
(C-33-1)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Package Option
ADRF5448BCZ	−40°C to +105°C	33-Pad Bare Die [CHIP]	C-33-1
ADRF5448BCZ-GP	−40°C to +105°C	33-Pad Bare Die [CHIP]	C-33-1
ADRF5448BCZ-SX	−40°C to +105°C	33-Pad Bare Die [CHIP]	C-33-1

[1] Z = RoHS Compliant Part.

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