Die on Carrier, Silicon SPDT Switch, Nonreflective, 100 MHz to 55 GHz

FEATURES

- Ultrawideband frequency range: 100 MHz to 55 GHz
- Nonreflective design
- Low insertion loss
  - 1.3 dB typical to 18 GHz
  - 1.9 dB typical to 40 GHz
  - 2.5 dB typical to 50 GHz
  - 3.6 dB typical to 55 GHz
- High isolation
  - 43 dB typical to 40 GHz
  - 38 dB typical to 55 GHz
- High input linearity
  - 0.1 dB power compression (P0.1dB): 31 dBm
  - Third-order intercept (IP3): 53 dBm
- High power handling at T_{CASE} = 85°C
  - 30 dBm through path
  - 24 dBm terminated path
  - 30 dBm hot switching
- RF settling time (0.1 dB final RF output): 30 ns
- No low-frequency spurious signals
- All-off state control
- Positive control interface: CMOS-/LVTTL-compatible
- 15-pad, 3.021 mm × 2.305 mm bare die [CHIP]

APPLICATIONS

- Test and instrumentation
- Cellular infrastructure: 5G millimeterwave (mmW)
- Military radios, radars, and electronic countermeasures (ECMs)
- Microwave radios and very small aperture terminals (VSATs)
- Industrial scanners

FUNCTIONAL BLOCK DIAGRAM

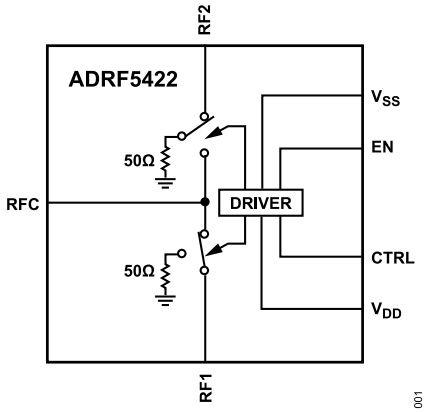


Figure 1. Functional Block Diagram

GENERAL DESCRIPTION

The ADRF5422 is a nonreflective, SPDT switch manufactured in the silicon process attached on a gallium arsenide (GaAs) carrier substrate. The substrate incorporates the bond pads for chip and wire assembly. The bottom of the device is metalized and connected to ground.

This device operates from 100 MHz to 55 GHz with a typical insertion loss of 3.6 dB and isolation of 38 dB at 55 GHz. The ADRF5422 has an RF input power handling capability of 30 dBm for the through path, 24 dBm for the terminated path, and 30 dBm for the hot switching.

The ADRF5422 requires a positive supply of +3.3 V and a negative supply of −3.3 V. The device employs complementary metal-oxide semiconductor (CMOS)-/low voltage transistor to transistor logic (LVTTL)-compatible controls.

The ADRF5422 can operate with a single positive supply voltage (V_{DD}) applied while the negative supply voltage (V_{SS}) is connected to ground. In this operating condition, the small signal performance is maintained while the switching characteristics, linearity, and power handling performance is derated. For more details, see Table 2.

The ADRF5422 is designed to match a characteristic impedance of 50 Ω and can operate from −40°C to +105°C.

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REVISION HISTORY

5/2026—Rev. 0 to Rev. A

Changes to Handling, Mounting, and Epoxy Die Attach Section ... 12

7/2024—Revision 0: Initial Version

SPECIFICATIONS

V_{DD} = 3.3 V, V_{SS} = −3.3 V, V_{CTRL} and V_{EN} = 0 V or V_{DD}, T_{CASE} = 25°C, and 50 Ω system, unless otherwise noted. RFx refers to RF1 or RF2.

Table 1. Electrical Specifications

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
FREQUENCY RANGE	f		0.1		55	GHz
INSERTION LOSS						
Between RFC and RFx (On)		100 MHz to 18 GHz		1.3		dB
		18 GHz to 26 GHz		1.5		dB
		26 GHz to 40 GHz		1.9		dB
		40 GHz to 50 GHz		2.5		dB
		50 GHz to 55 GHz		3.6		dB
RETURN LOSS						
RFC		100 MHz to 26 GHz		20		dB
		26 GHz to 50 GHz		15		dB
		50 GHz to 55 GHz		11		dB
RFx (On)		100 MHz to 26 GHz		20		dB
		26 GHz to 40 GHz		15		dB
		40 GHz to 50 GHz		13		dB
		50 GHz to 55 GHz		10		dB
RFx (Off)		100 MHz to 40 GHz		20		dB
		40 GHz to 50 GHz		10		dB
		50 GHz to 55 GHz		8		dB
ISOLATION						
Between RFC and RFx (Off)		100 MHz to 26 GHz		58		dB
		26 GHz to 40 GHz		43		dB
		40 GHz to 50 GHz		42		dB
		50 GHz to 55 GHz		38		dB
Between RF1 and RF2		100 MHz to 18 GHz		57		dB
		18 GHz to 26 GHz		50		dB
		26 GHz to 40 GHz		43		dB
		40 GHz to 50 GHz		40		dB
		50 GHz to 55 GHz		40		dB
SWITCHING CHARACTERISTICS						
Rise Time and Fall Time	t_{RISE} and t_{FALL}	10% to 90% of RF output (RF_{OUT})		3		ns
On Time and Off Time	t_{ON} and t_{OFF}	50% V_{CTRL} to 90% of RF_{OUT}		20		ns
0.1 dB RF Settling Time		50% V_{CTRL} to 0.1 dB of final RF_{OUT}		30		ns
INPUT LINEARITY[1]		f = 100 MHz to 40 GHz				
0.1 dB Power Compression	P0.1dB			31		dBm
Input Third-Order Intercept	IIP3	Two-tone input power = 14 dBm each tone and Δf = 1 MHz		53		dBm
SUPPLY CURRENT		V_{DD} and V_{SS} pads				
Positive Supply Current	I_{DD}			140		µA
Negative Supply Current	I_{SS}			510		µA
DIGITAL CONTROL INPUTS						
Voltage						
Low	V_{INL}		0		0.8	V
High	V_{INH}		1.2		3.3	V
Current						
Low	I_{INL}			<1		µA
High	I_{INH}	CTRL		<1		µA

SPECIFICATIONS

Table 1. Electrical Specifications (Continued)

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
		EN		33		µA
RECOMMENDED OPERATING CONDITONS						
Positive Supply Voltage	V_{DD}		3.15		3.45	V
Negative Supply Voltage	V_{SS}		−3.45		−3.15	V
Digital Control Input Voltage	V_{CTRL}		0		V_{DD}	V
RF Input Power[2, 3]	P_{IN}	f = 250 MHz to 40 GHz and T_{CASE} = 85°C				
Through Path		RF signal is applied to the RFC or through connected RF1 and RF2			30	dBm
Terminated Path		RF signal is applied to unselected RF1 or unselected RF2			24	dBm
Hot Switching		RF signal is applied to the RFC while switching between RF1 and RF2			30	dBm
Case Temperature	T_{CASE}		−40		+105	°C

1 For input linearity performance over frequency, see Figure 2 and Figure 3.

2 For power derating over frequency, see Figure 2 and Figure 3.

3 For 105°C operation, the power handling degrades from the T_{CASE} = 85°C specification by 3 dB.

SINGLE-SUPPLY OPERATION

V_{DD} = 3.3 V, V_{SS} = 0 V, V_{CTRL} and V_{EN} = 0 V or V_{DD}, T_{CASE} = 25°C, and 50 Ω system, unless otherwise noted.

Table 2. Single-Supply Operation Specifications

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
FREQUENCY RANGE	f		0.1		55	GHz
SWITCHING CHARACTERISTICS						
Rise Time and Fall Time	t_{RISE} and t_{FALL}	10% to 90% of RF_{OUT}		22		ns
On Time and Off Time	t_{ON} and t_{OFF}	50% V_{CTRL} to 90% of RF_{OUT}		65		ns
0.1 dB RF Settling Time		50% V_{CTRL} to 0.1 dB of final RF_{OUT}		90		ns
INPUT LINEARITY		f = 250 MHz to 40 GHz				
0.1 dB Power Compression	P0.1dB			17		dBm
Input Third-Order Intercept	IIP3	Two-tone input power = 0 dBm each tone and Δf = 1 MHz		44		dBm
RECOMMENDED OPERATING CONDITONS						
RF Input Power[1, 2]	P_{IN}	f = 250 MHz to 40 GHz and T_{CASE} = 85°C				
Through Path		RF signal is applied to the RFC or through connected RF1 and RF2			17	dBm
Terminated Path		RF signal is applied to unselected RF1 or unselected RF2			12	dBm
Hot Switching		RF signal is applied to the RFC while switching between RF1 and RF2			17	dBm

1 For power derating over frequency, see Figure 2 and Figure 3 .

2 For 105°C operation, the power handling degrades from the T_{CASE} = 85°C specification by 3 dB.

ABSOLUTE MAXIMUM RATINGS

For recommended operating conditions, see Table 1 and Table 2.

Table 3. Absolute Maximum Ratings

Parameter	Rating
Supply Voltage	
Positive	−0.3 V to +3.6 V
Negative	−3.6 V to +0.3 V
Digital Control Input Voltage	
Voltage	−0.3 V to V_{DD} + 0.3 V
Current	3 mA
RF Input Power, Dual Supply[1] (V_{DD} = 3.3 V, V_{SS} = −3.3 V, f = 250 MHz to 40 GHz, and T_{CASE} = 85°C)	
Through Path	31 dBm
Terminated Path	25 dBm
Hot Switching	31 dBm
RF Input Power, Single Supply (V_{DD} = 3.3 V, V_{SS} = 0 V, f = 250 MHz to 40 GHz, and T_{CASE} = 85°C)	
Through Path	18 dBm
Terminated Path	13 dBm
Hot Switching	18 dBm
RF Power Under Unbiased Condition (V_{DD} and V_{SS} = 0 V)	18 dBm
Temperature	
T_J	135°C
Storage	−65°C to +150°C
Reflow	260°C

[1] For power derating over frequency, see Figure 2 and Figure 3.

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

THERMAL RESISTANCE

Thermal performance is directly linked to printed circuit board (PCB) design and operating environment. Careful attention to PCB thermal design is required.

θ_{JC} is the junction to case bottom (channel to package bottom) thermal resistance.

Table 4. Thermal Resistance

Package Type	θ_{JC}[1]	Unit
C-15-2		
Through Path	135	°C/W
Terminated Path	200	°C/W

[1] θ_{JC} is determined by simulation under the following conditions: the heat transfer is due solely to the thermal conduction from the channel through the ground pad to the PCB, and the ground pad is held constant at the operating temperature of 85°C.

POWER DERATING CURVES

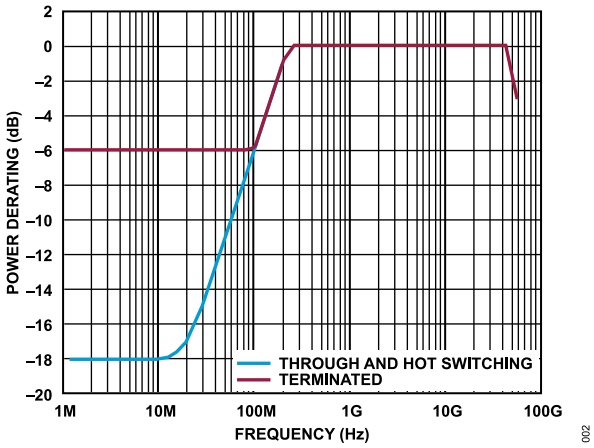


Figure 2. Power Derating vs. Frequency, Low Frequency Detail and Die Temperature (T_{DIE}) = 85°C

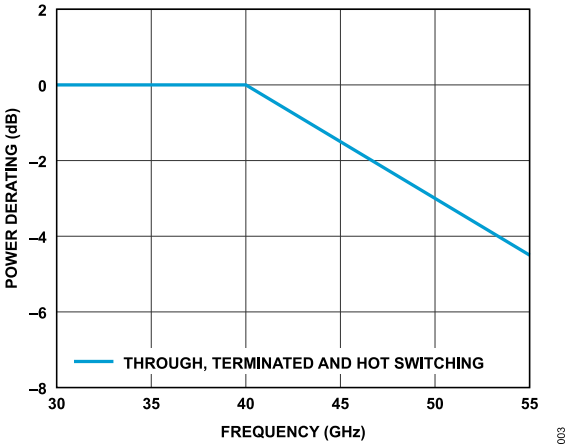


Figure 3. Power Derating vs. Frequency, High Frequency Detail and T_{DIE} = 85°C

ABSOLUTE MAXIMUM RATINGS

ELECTROSTATIC DISCHARGE (ESD) RATINGS

The following ESD information is provided for handling of ESD-sensitive devices in an ESD protected area only.

Human body model (HBM) per ANSI/ESDA/JEDEC JS-001.

ESD Ratings for ADRF5422

Table 5. ADRF5422, 15-Pad Bare Die [CHIP]

ESD Model	Withstand Threshold (V)	Class
HBM	±1250 for RF pads	1C
	±2000 for supply and control pads	2

ESD CAUTION



ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

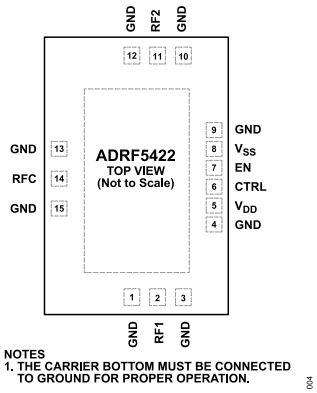


Figure 4. Pad Configuration

Table 6. Pad Function Descriptions

Pad Number	Mnemonic	Description
1, 3, 4, 9, 10, 12, 13, 15	GND	Ground. Bonding of these GND pads is optional. See the Applications Information section.
14	RFC	RF Common Port. The RFC pad is DC-coupled to 0 V and AC matched to 50 Ω. No DC blocking capacitor is required when the RF line potential is equal to 0 V DC. For the interface schematic, see Figure 5.
2	RF1	RF Throw Port 1. The RF1 pad is DC-coupled to 0 V and AC matched to 50 Ω. No DC blocking capacitor is required when the RF line potential is equal to 0 V DC. For the interface schematic, see Figure 5.
5	V_{DD}	Positive Supply Voltage. For the interface schematic, see Figure 6.
6	CTRL	Control Input Voltage. For the interface schematic, see Figure 8.
7	EN	Enable Input Voltage. For the interface schematic, see Figure 9.
8	V_{SS}	Negative Supply Voltage. For the interface schematic, see Figure 7.
11	RF2	RF Throw Port 2. The RF2 pad is DC-coupled to 0 V and AC matched to 50 Ω. No DC blocking capacitor is required when the RF line potential is equal to 0 V DC. For the interface schematic, see Figure 5.
	Carrier Bottom	Exposed Pad. The exposed pad must be connected to the RF and DC ground of the PCB.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

INTERFACE SCHEMATICS

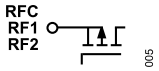


Figure 5. RF Pads (RFC, RF1, and RF2) Interface Schematic

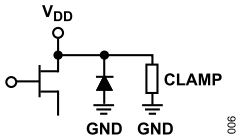


Figure 6. V_{DD} Pad Interface Schematic

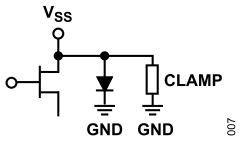


Figure 7. V_{SS} Pad Interface Schematic

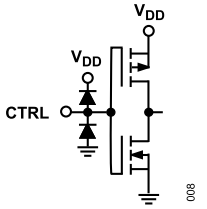


Figure 8. CTRL Pad Interface Schematic

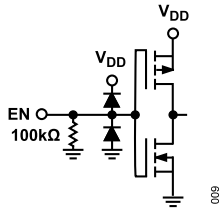


Figure 9. EN Pad Interface Schematic

TYPICAL PERFORMANCE CHARACTERISTICS

INSERTION LOSS, RETURN LOSS, AND ISOLATION

V_{DD} = +3.3 V, V_{SS} = −3.3 V, control voltages = 0 V or V_{DD}, T_{DIE} = 25°C, and a 50 Ω system, unless otherwise noted.

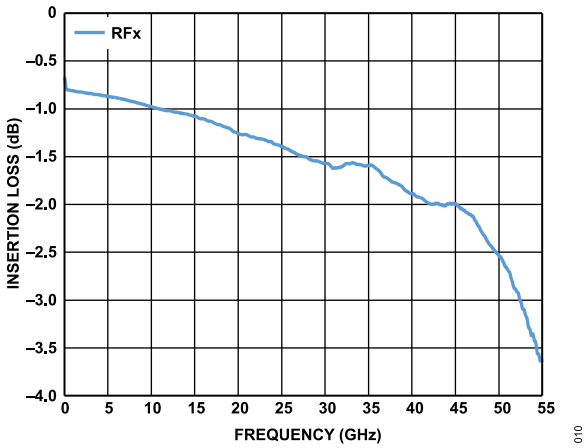


Figure 10. Insertion Loss vs. Frequency at Room Temperature for RFx

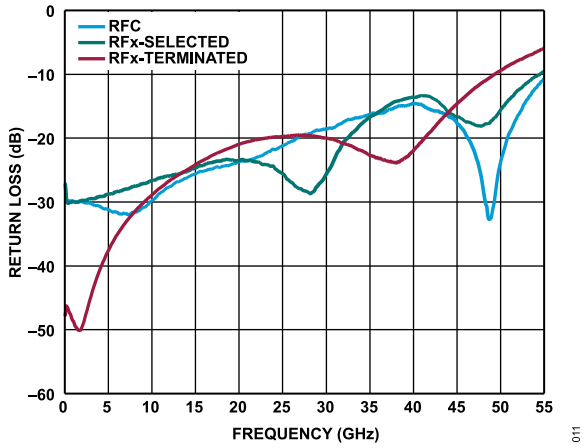


Figure 11. Return Loss vs. Frequency

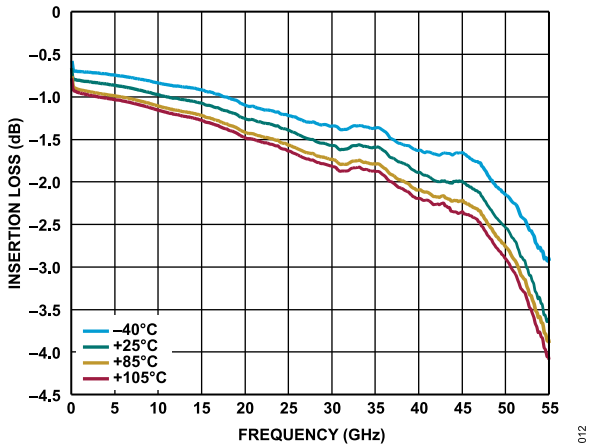


Figure 12. Insertion Loss vs. Frequency over Temperature

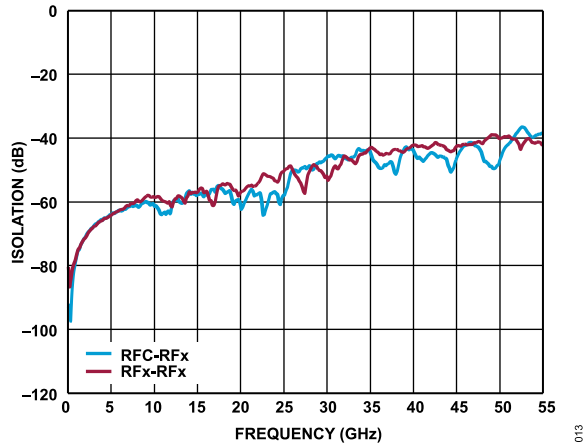


Figure 13. Isolation vs. Frequency

TYPICAL PERFORMANCE CHARACTERISTICS

INPUT POWER COMPRESSION AND THIRD-ORDER INTERCEPT

V_{DD} = +3.3 V, V_{SS} = −3.3 V, control voltages = 0 V or V_{DD}, T_{DIE} = 25°C, and a 50 Ω system, unless otherwise noted.

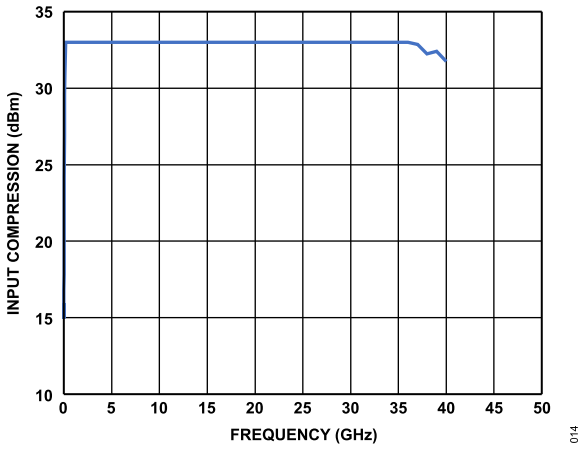


Figure 14. Input P0.1dB vs. Frequency

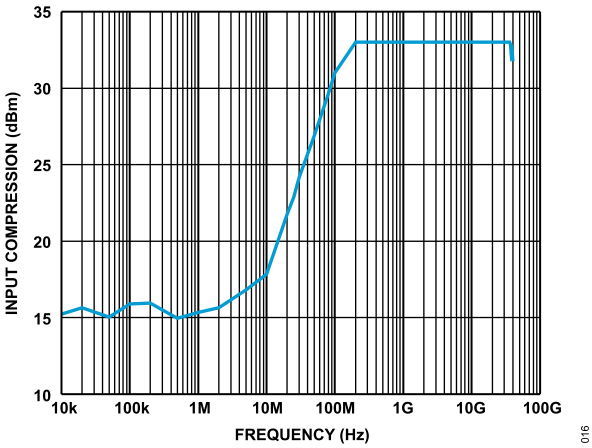


Figure 16. Input P0.1dB vs. Frequency, Low Frequency Detail

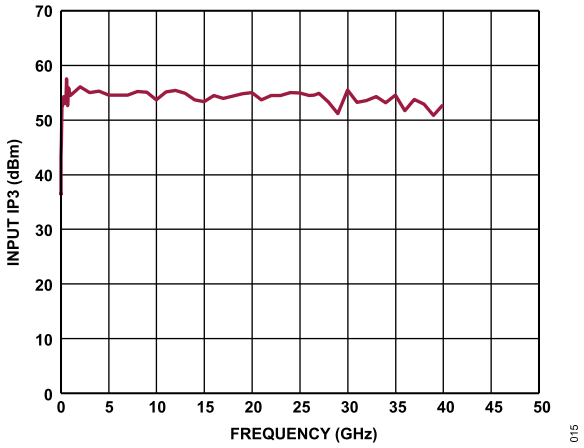


Figure 15. Input IP3 vs. Frequency

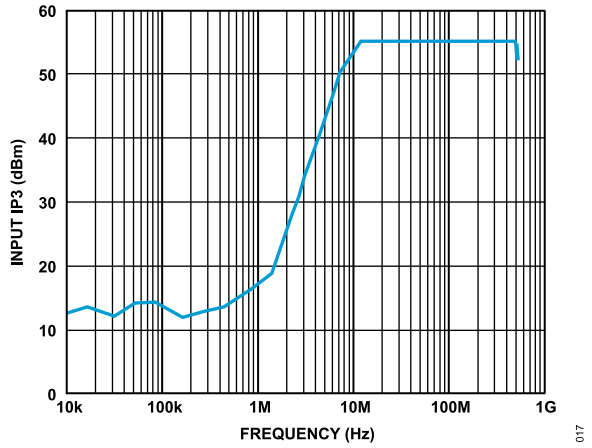


Figure 17. Input IP3 vs. Frequency, Low Frequency Detail

THEORY OF OPERATION

The ADRF5422 integrates a driver to perform logic function internally and to provide the advantage of a simplified control interface. The driver features two digital control input pads (CTRL and EN), see Table 7. The CTRL pad determines which RF port is in insertion loss state and which RF port is in isolation state. When the EN pad is logic high, the switch is in an all-off state regardless of the logic state of the CTRL pad. Both the RF1 to RFC path and the RF2 to RFC path are in an isolation state. The RF1 and RF2 ports are terminated to internal 50 Ω resistors, and the RFC port becomes reflective.

POWER SUPPLY

The ADRF5422 requires a positive supply voltage applied to the V_{DD} pad and a negative supply voltage applied to the V_{SS} pad. Bypassing capacitors are recommended on the supply lines to filter high frequency noise.

The power-up sequence is as follows:

1. Connect GND.
2. Power up the V_{DD} and V_{SS} voltages. Power up V_{SS} after V_{DD} to avoid current transients on V_{DD} during ramp up.
3. Power up the digital control inputs. The order of the digital control inputs is not important. However, powering the digital control inputs before the V_{DD} voltage supply can inadvertently forward bias and damage the internal ESD structures. To avoid this damage, use a series 1 kΩ resistor to limit the current flowing into the control pad. Use pull-up or pull-down resistors if the controller output is in a high impedance state after the V_{DD} voltage is powered up and the control pads are not driven to a valid logic state.
4. Apply RF signal.

The power-down sequence is the reverse order of the power-up sequence.

Single-Supply Operation

The ADRF5422 can operate with a single positive supply voltage applied to the V_{DD}, and the V_{SS} pad is connected to ground. However, some performance differences occur in switching characteristics and large signal. For more details, see Table 2.

RF INPUT AND OUTPUT

All of the RF ports (RFC, RF1, and RF2) are DC-coupled to 0 V, and no DC blocking is required at the RF ports when the RF line potential is equal to 0 V.

The RF ports are internally matched to 50 Ω. Therefore, external matching networks are not required.

The insertion loss path conducts the RF signal between the selected RF throw port and the RF common port. The isolation path provides high loss between the insertion loss path and the unselected RF throw port that is terminated to an internal 50 Ω resistor.

The switch design is bidirectional with equal power handling capabilities. The RF input signal can be applied to the RFC port or the selected RF throw port.

Table 7. Control Voltage Truth Table

Digital Control Inputs		RF Paths	
EN	**CTRL**	**RF1 to RFC**	**RF2 to RFC**
Low	Low	Isolation (off)	Insertion loss (on)
Low	High	Insertion loss (on)	Isolation (off)
High	Low	Isolation (off)	Isolation (off)
High	High	Isolation (off)	Isolation (off)

APPLICATIONS INFORMATION

DIE ASSEMBLY

An assembly diagram of the ADRF5422 is shown in Figure 18.

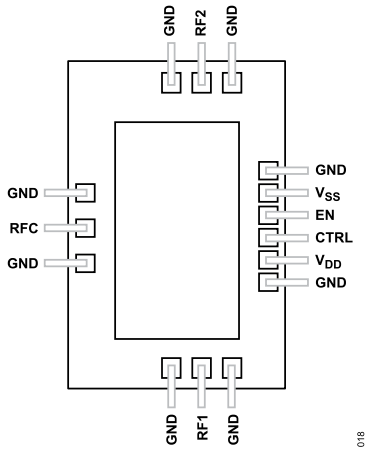


Figure 18. Die Assembly Diagram

The ADRF5422 is designed to have the optimum RF input and output impedance match with 3 mil × 0.5 mil gold ribbon wire and 3 mil loop height typical. The bonding diagrams are shown in Figure 19 and Figure 20. Alternatively, using multiple wire bonds with equivalent inductance yields similar performance. For RF routing from the device, coplanar wave guide or microstrip transmission lines can be used. No impedance matching is required on the transmission line pad because the device is designed to match internally to the recommended ribbon bond. A spacing of 3 mils from the RF transmission line to the device edge is recommended for optimum performance.

DC pads can be connected using standard 1 mil diameter wire by keeping the wire lengths as short as possible to minimize the parasitic inductance. The DC pads are large enough to accommodate ribbon bonds, if preferred.

All bonds must be thermosonically bonded at a nominal stage temperature of 150°C, and a minimum amount of ultrasonic energy must be applied to achieve reliable bonds.

The device is metalized on the backside, and the ground connection can be done by attaching the device directly to the RF ground plane using a conductive epoxy. In this case, connecting the ground pads is optional but still recommended to ensure a solid ground connection.

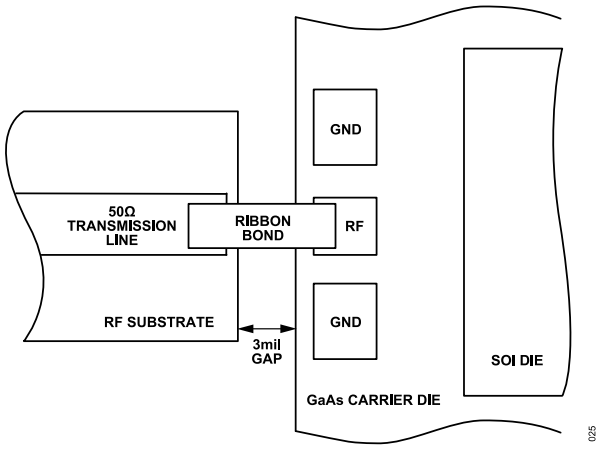


Figure 19. Bonding Diagram Top View

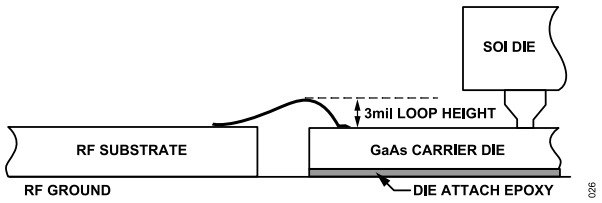


Figure 20. Bonding Diagram Side View

HANDLING, MOUNTING, AND EPOXY DIE ATTACH

Keep devices in ESD protective sealed bags for shipment, and store all bare die in a dry nitrogen environment.

For manual picking, it is a common practice to use a pair of tweezers for GaAs devices. However, for die on carrier devices, the use of a vacuum tool is recommended to avoid any damage on the device substrate. Handle these devices in a clean environment, and do not attempt to clean devices using liquid cleaning systems.

To attach the die with epoxy, apply an amount of epoxy to the mounting surface so that a thin epoxy fillet is observed around the perimeter of the chip after it is placed into position. Set epoxy cure temperatures per the recommendations of the manufacturer and the maximum ratings of the device to minimize accumulated mechanical stress after assembly.

Since both dies are attached with solder joints, users must follow best practices for the thermomechanical design of their module assemblies. The temperature expansion coefficient of the substrate material must match the thermal expansion coefficient of the GaAs and silicon (Si) die. Do not allow warpage or other mechanical deformation on the substrate. Set the die attach process and the epoxy cure temperatures to lower the accumulated stress after assembly.

OUTLINE DIMENSIONS

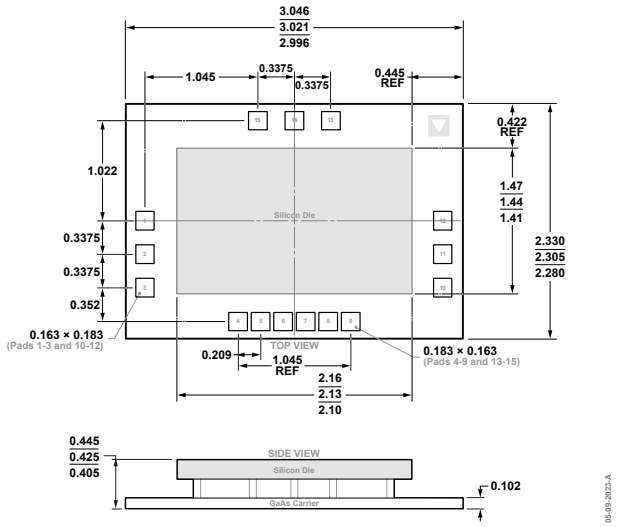


Figure 21. 15-Pad Bare Die [CHIP]
(C-15-2)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Package Option
ADRF5422BCZ	−40°C to +105°C	15-Pad Bare Die [CHIP]	C-15-2
ADRF5422BCZ-GP	−40°C to +105°C	15-Pad Bare Die [CHIP]	C-15-2
ADRF5422BCZ-SX	−40°C to +105°C	15-Pad Bare Die [CHIP]	C-15-2

[1] Z = RoHS Compliant Part.

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