Flip-Chip, Silicon SPDT Switch, 1GHz to 90GHz

FEATURES

- Frequency range: 1GHz to 90GHz
- Low insertion loss
  - 1.2dB typical to 40GHz
  - 1.7dB typical to 67GHz
  - 3.0dB typical to 90GHz
- High Isolation
  - 42dB typical up to 40GHz
  - 40dB typical up to 67GHz
  - 30dB typical up to 90GHz
- High input linearity
  - P0.1dB: 24dBm typical
  - IP3: 45dBm typical
- High RF input power handling
  - Through path: 24dBm maximum
  - Hot switching: 21dBm maximum
- No low frequency spurs
- CMOS- and LVTTL-compatible
- Fast switching on time and off time (50% V_{CTRL} to 90% of RF output): 15ns
- RF settling time, 0.1dB (50% V_{CTRL} to 0.1dB of final RF output): 35ns
- Single-supply operation capability (V_{DD} = 3.3V and V_{SS} = 0V)
- 30-ball, 1.56mm × 2.04mm, bumped, bare die sales

APPLICATIONS

- Test and instrumentation
- Cellular infrastructure: 5G mmWave
- Military radios, radars, electronic counter measures (ECMs)
- Microwave radios and very small aperture terminals (VSATs)

FUNCTIONAL BLOCK DIAGRAM

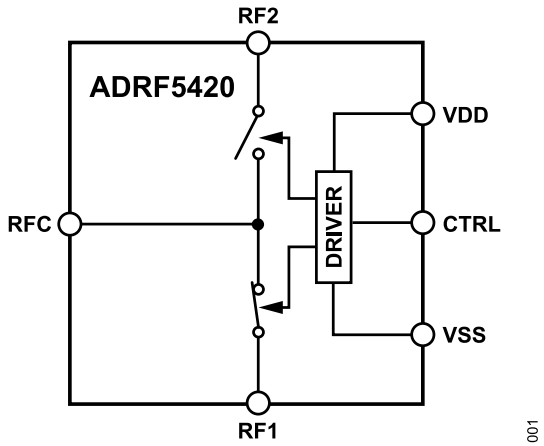

Figure 1. Functional Block Diagram

GENERAL DESCRIPTION

The ADRF5420 is a reflective, SPDT switch manufactured in the silicon process. This switch operates from 1GHz to 90GHz with better than 3.0dB of insertion loss and 30dB of isolation. The ADRF5420 has an RF input power handling capability of 24dBm for the through path and 21dBm for hot switching.

The ADRF5420 draws a current of 130µA on the positive supply of +3.3V and 490µA on negative supply of −3.3V. The device employs complementary metal-oxide semiconductor (CMOS)-/low voltage transistor to transistor logic (LVTTL)-compatible controls.

The ADRF5420 can also operate with a single positive supply voltage (V_{DD}) applied while the negative supply voltage (V_{SS}) is tied to ground. The small signal performance is maintained while the switching characteristics, linearity, and power handling performance is derated. See Table 2 for more details.

The ADRF5420 RF ports are designed to match a characteristic impedance of 50Ω. The ADRF5420 is a 30-ball, 1.56mm × 2.04mm, bumped bare die sales and can operate between −40°C to +105°C.

One Analog Way, Wilmington, MA 01887-2356, U.S.A.

TABLE OF CONTENTS

REVISION HISTORY

1/2026—Revision 0: Initial Version

SPECIFICATIONS

ELECTRICAL SPECIFICATIONS

V_{DD} = +3.3V, V_{SS} = −3.3V, control voltage (V_{CTRL}) = 0V or V_{DD}, and case temperature (T_{CASE}) = 25°C for 50Ω system, unless otherwise noted.

Table 1. Electrical Specifications

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
FREQUENCY RANGE	f		1		90	GHz
INSERTION LOSS						
Between RFC and RF1 and RF2 (On)		100MHz to 18GHz		0.9		dB
		18GHz to 40GHz		1.2		dB
		40GHz to 55GHz		1.5		dB
		55GHz to 67GHz		1.7		dB
		67GHz to 90GHz		3.0		dB
RETURN LOSS						
RFC and RF1 and RF2 (On)		100MHz to 18GHz		18		dB
		18GHz to 40GHz		16		dB
		40GHz to 55GHz		15		dB
		55GHz to 67GHz		15		dB
		67GHz to 90GHz		10		dB
ISOLATION						
Between RFC and RF1/RF2		100MHz to 18GHz		47		dB
		18GHz to 40GHz		40		dB
		40GHz to 55GHz		40		dB
		55GHz to 67GHz		40		dB
		67GHz to 90GHz		30		dB
Between RF1 and RF2		100MHz to 18GHz		49		dB
		18GHz to 40GHz		42		dB
		40GHz to 55GHz		43		dB
		55GHz to 67GHz		40		dB
		67GHz to 90GHz		30		dB
SWITCHING CHARACTERISTICS						
Rise and Fall Time	t_{RISE}, t_{FALL}	10% to 90% of RF output		5		ns
On and Off Time	t_{ON}, t_{OFF}	50% V_{CTRL} to 90% of RF output		15		ns
RF Settling Time						
0.1dB		50% V_{CTRL} to 0.1dB of final RF output		35		ns
INPUT LINEARITY[1]		1GHz to 67GHz				
0.1dB Power Compression	P0.1dB			24		dBm
Third-Order Intercept	IP3	Two-tone input power = 14dBm each tone, Δf = 1MHz		45		dBm
SUPPLY CURRENT		VDD and VSS pins				
Positive Supply Current	I_{DD}			130		µA
Negative Supply Current	I_{SS}			490		µA
DIGITAL CONTROL INPUTS		CTRL pin				
Voltage						
Low	V_{INL}		0		0.8	V
High	V_{INH}		1.2		3.3	V
Current						
Low and High	I_{INL}, I_{INH}			<1		µA

SPECIFICATIONS

Table 1. Electrical Specifications (Continued)

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
RECOMMENDED OPERATING CONDITONS						
Supply Voltage						
Positive	V_{DD}		3.15		3.45	V
Negative	V_{SS}		−3.45		−3.15	V
Digital Control Voltage	V_{CTRL}		0		V_{DD}	V
RF Input Power[2]	P_{IN}	f = 3GHz to 70GHz, T_{CASE} = 85°C[3]				
Through Path		RF signal is applied to RFC or through connected RF1 and RF2			24	dBm
Hot Switching		RF signal is present at RFC while switching between RF1 and RF2			21	dBm
Case Temperature	T_{CASE}		−40		+105	°C

1 For input linearity performance over frequency, see Figure 13 to Figure 16.

2 For power derating over frequency, see Figure 2 and Figure 3.

3 For 105°C operation, the power handling degrades from the T_{CASE} = 85°C specification by 3dB.

SINGLE-SUPPLY OPERATION

V_{DD} = 3.3 V, V_{SS} = 0V, V_{CTRL} = 0V or V_{DD}, and T_{CASE} = 25°C for 50Ω system, unless otherwise noted.

Table 2. Single-Supply Operation Specifications

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
FREQUENCY RANGE	f		1		90	GHz
SWITCHING CHARACTERISTICS						
Rise and Fall Time	t_{RISE}, t_{FALL}	10% to 90% of RF output		20		ns
On and Off Time	t_{ON}, t_{OFF}	50% V_{CTRL} to 90% of RF output		38		ns
0.1dB RF Settling Time		50% V_{CTRL} to 0.1dB of final RF output		42		ns
INPUT LINEARITY		f = 1GHz to 67GHz				
0.1dB Power Compression	P0.1dB			14		dBm
Input Third-Order Intercept	IIP3	Two-tone input power = 0dBm each tone, Δf = 1MHz		41		dBm
RECOMMENDED OPERATING CONDITONS						
RF Input Power[1]	P_{IN}	f = 3GHz to 70GHz, T_{CASE} = 85°C[2]				
Through Path		RF signal is applied to the RFC or through connected RF1 and RF2			14	dBm
Hot Switching		RF signal is applied to the RFC while switching between RF1 and RF2			11	dBm

1 For power derating over frequency, see Figure 2 and Figure 3.

2 For 105°C operation, the power handling degrades from the T_{CASE} = 85°C specification by 1dB.

ABSOLUTE MAXIMUM RATINGS

For the recommended operating conditions, see Table 1.

Table 3. Absolute Maximum Ratings

Parameter	Rating
Positive Supply Voltage	−0.3V to +3.6V
Negative Supply Voltage	−3.6V to +0.3V
Digital Control Input[1]	
Voltage	−0.3V to V_{DD} + 0.3V
Current	3mA
RF Input Power, Dual Supply[2] (V_{DD} = +3.3V, V_{SS} = −3.3V, f = 3GHz to 70GHz, T_{CASE} = 85°C[3])	
Through Path	25dBm
Hot Switching	22dBm
RF Input Power, Single Supply (V_{DD} = 3.3V, V_{SS} = 0V, f = 3GHz to 70GHz, T_{CASE} = 85°C[3])	
Through Path	15dBm
Hot Switching (RFC)	12dBm
RF Input Power Under Unbiased Condition (V_{DD} and V_{SS} = 0V)	15dBm
Temperature	
Junction, T_J	135°C
Storage Range	−65°C to +150°C
Reflow	260°C

1 Overvoltages at the digital control input are clamped by internal diodes. Current must be limited to the maximum rating given.

2 For power derating over frequency, see Figure 2 and Figure 3.

3 For 105°C operation, the power handling degrades from the T_{CASE} = 85°C specification by 3 dB for dual supply and 1dB for single supply.

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

Only one absolute maximum rating can be applied at any one time.

THERMAL RESISTANCE

Thermal performance is directly linked to printed circuit board (PCB) design and operating environment. Careful attention to PCB thermal design is required.

θ_{JC} is the junction to case bottom (channel to package bottom) thermal resistance.

Table 4. Thermal Resistance

Package Type	θ_{JC}[1]	Unit
CD-30-3, Through Path	537	°C/W

1 θ_{JC} was determined by simulation under the following conditions: the heat transfer is due solely to the thermal conduction from the channel through the ground pad to the PCB, and the ground pad is held constant at the operating temperature of 85°C.

POWER DERATING CURVES

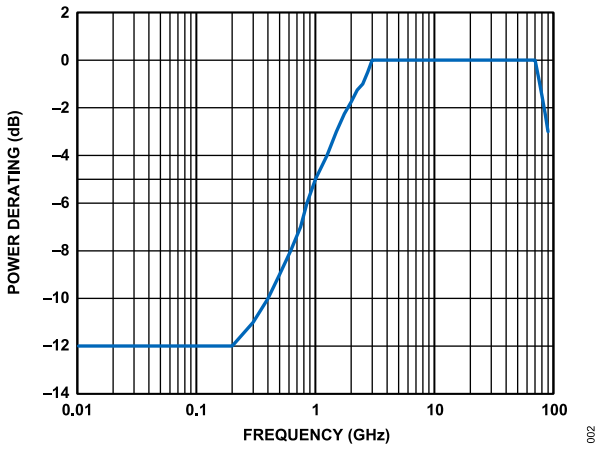

Figure 2. Power Derating vs. Frequency, Low Frequency Detail, T_{CASE} = 85°C

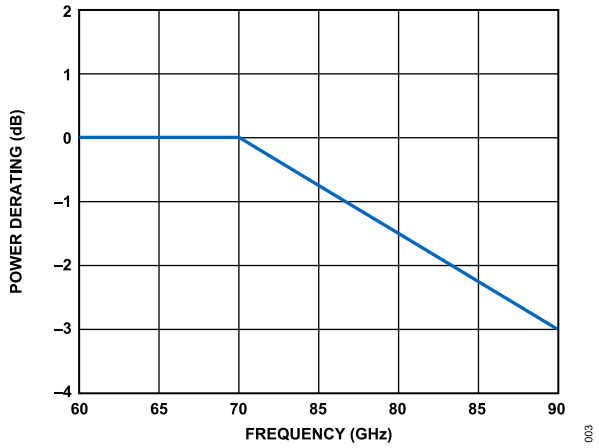

Figure 3. Power Derating vs. Frequency, High Frequency Detail, T_{CASE} = 85°C

ELECTROSTATIC DISCHARGE (ESD) RATINGS

The following ESD information is provided for handling of ESD-sensitive devices in an ESD-protected area only.

Human body model (HBM) per ANSI/ESDA/JEDEC JS-001.

ESD Ratings for the ADRF5420

Table 5. ADRF5420, 30-Ball BUMPED_CHIP

ESD Model	Withstand Threshold (V)
HBM	±500 for the RF pins ±2000 for the supply and digital control pins

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

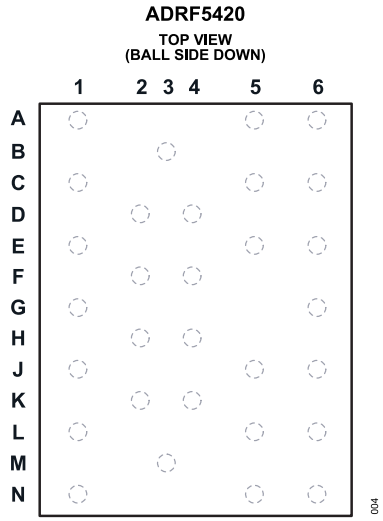

Figure 4. Pin Configuration (Top View—Ball Side Down)

Table 6. Pin Function Descriptions

Ball No.	Mnemonic	X Coordinate (mm)	Y Coordinate (mm)	Description
A1	GND	−0.575	+0.9	Ground.
A5	GND	+0.275	+0.9	Ground.
A6	GND	+0.575	+0.9	Ground.
B3	RF2	−0.15	+0.75	RF Port 2. The RF2 pin is DC-coupled and biased to 0V and AC matched to 50Ω. No DC blocking capacitor is necessary when the RF line potential is equal to 0V. See Figure 5 for the interface schematic.
C1	GND	−0.575	+0.6	Ground.
C5	GND	+0.275	+0.6	Ground.
C6	GND	+0.575	+0.6	Ground.
D2	GND	−0.275	+0.45	Ground.
D4	GND	−0.025	+0.45	Ground.
E1	GND	−0.575	+0.3	Ground.
E5	GND	+0.275	+0.3	Ground.
E6	VSS	+0.575	+0.3	Negative Supply Voltage. See Figure 8 for the interface schematic.
F2	GND	−0.275	+0.15	Ground.
F4	GND	−0.025	+0.15	Ground.
G1	RFC	−0.575	0	RF Common Port. The RFC pin is DC-coupled and biased to 0V and AC matched to 50Ω. No DC blocking capacitor is necessary when the RF line potential is equal to 0V. See Figure 5 for the interface schematic.
G6	CTRL	+0.575	0	Control Input Voltage. See for the Figure 6 interface schematic.
H2	GND	−0.275	−0.15	Ground.
H4	GND	−0.025	−0.15	Ground.
J1	GND	−0.575	−0.3	Ground.
J5	GND	+0.275	−0.3	Ground.
J6	VDD	+0.575	−0.3	Positive Supply Voltage. See Figure 7 for the interface schematic.
K2	GND	−0.275	−0.45	Ground.
K4	GND	−0.025	−0.45	Ground.
L1	GND	−0.575	−0.6	Ground.
L5	GND	+0.275	−0.6	Ground.
L6	GND	+0.575	−0.6	Ground.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

Table 6. Pin Function Descriptions (Continued)

Ball No.	Mnemonic	X Coordinate (mm)	Y Coordinate (mm)	Description
M3	RF1	−0.15	−0.75	RF Port 1. The RF1 pin is DC-coupled and biased to 0V and AC matched to 50Ω. No DC blocking capacitor is necessary when the RF line potential is equal to 0V. See Figure 5 for the interface schematic.
N1	GND	−0.575	−0.9	Ground.
N5	GND	+0.275	−0.9	Ground.
N6	GND	+0.575	−0.9	Ground.

INTERFACE SCHEMATICS

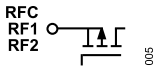

Figure 5. RFC, RF1, and RF2 Interface Schematic

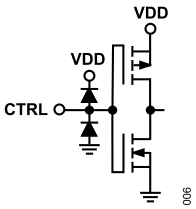

Figure 6. CTRL Interface Schematic

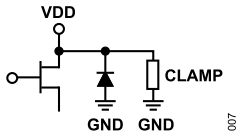

Figure 7. VDD Interface Schematic

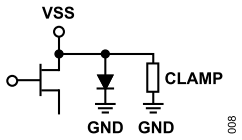

Figure 8. VSS Interface Schematic

TYPICAL PERFORMANCE CHARACTERISTICS

INSERTION LOSS, RETURN LOSS, AND ISOLATION

V_{DD} = 3.3V, V_{SS} = −3.3V, V_{CTRL} = 0V or V_{DD}, and T_{CASE} = 25°C for a 50Ω system, unless otherwise noted. Insertion loss, return loss and isolation are measured on a probe board using ground-signal-ground (GSG) probes close to the RFx pins.

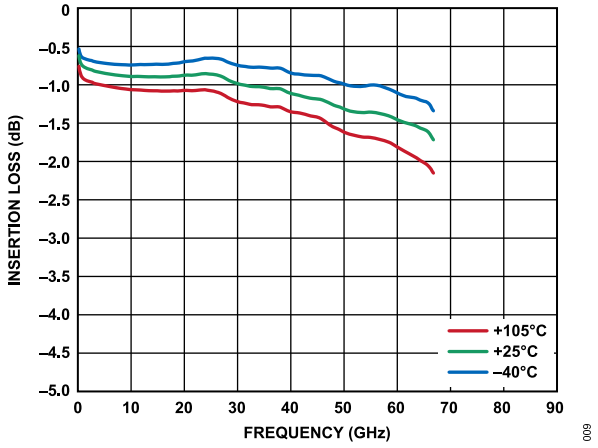

Figure 9. Insertion Loss vs. Frequency over Temperature (Setup Limitation Is 67GHz)

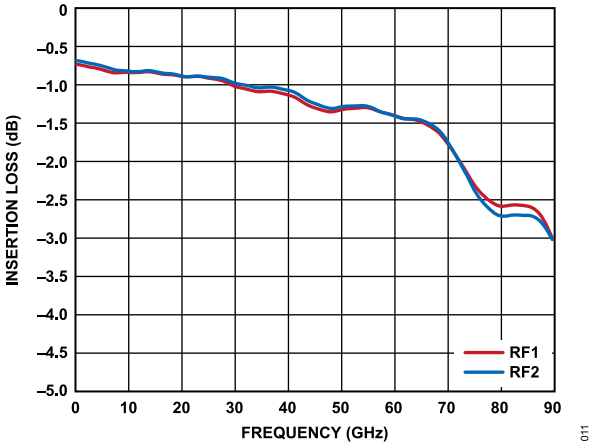

Figure 11. Insertion Loss vs. Frequency

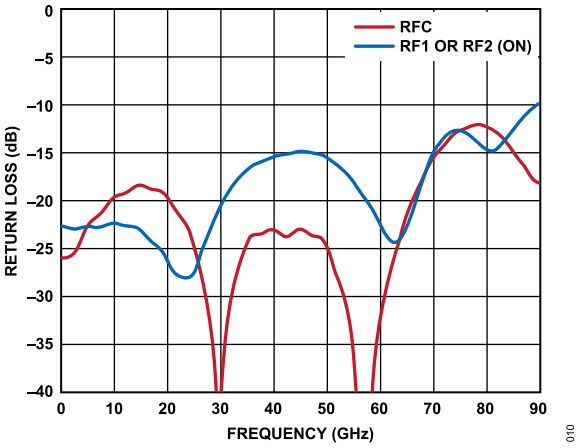

Figure 10. Return Loss vs. Frequency

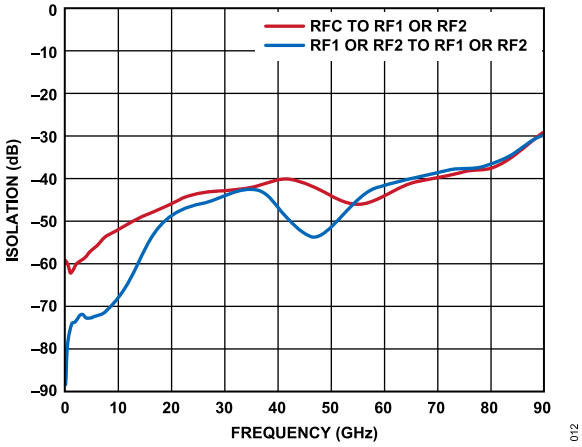

Figure 12. Isolation vs. Frequency

TYPICAL PERFORMANCE CHARACTERISTICS

INPUT POWER COMPRESSION AND THIRD-ORDER INTERCEPT

V_{DD} = +3.3V, V_{SS} = −3.3V, V_{CTRL} = 0V or V_{DD}, and T_{CASE} = 25°C for a 50Ω system, unless otherwise noted. The large signal performance parameters are measured on a connectorized board.

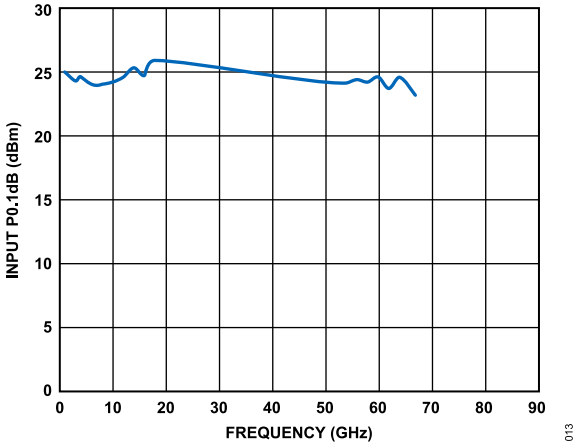

Figure 13. Input P0.1dB vs. Frequency

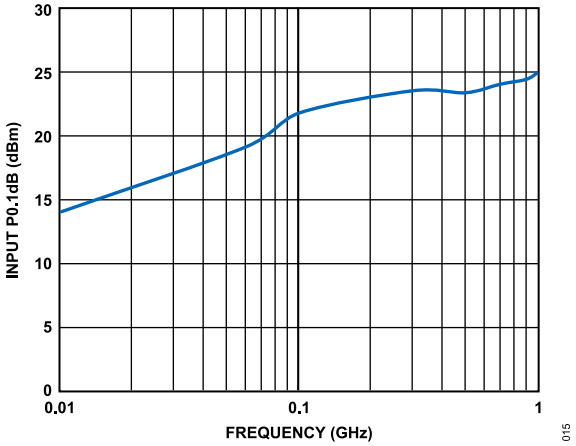

Figure 15. Input P0.1dB vs. Frequency (Low Frequency Detail)

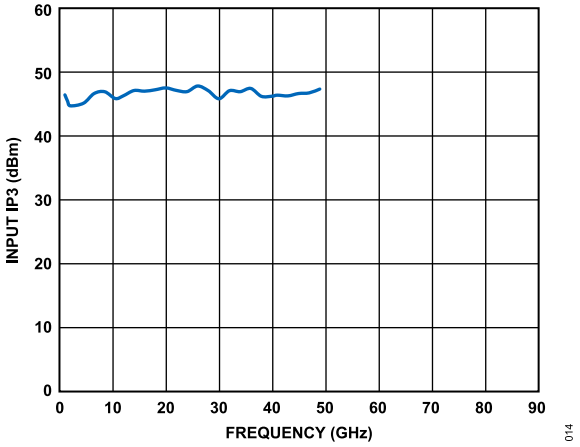

Figure 14. Input IP3 vs. Frequency

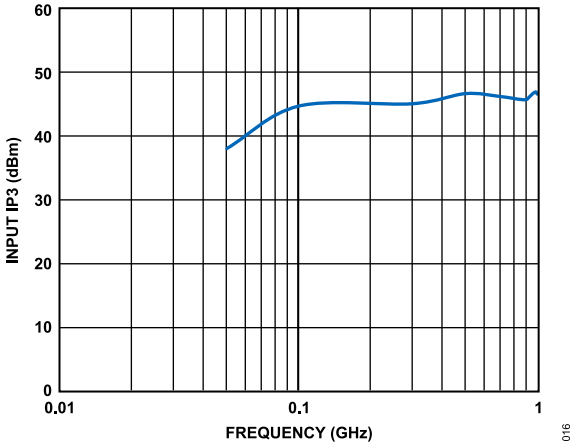

Figure 16. Input IP3 vs. Frequency (Low Frequency Detail)

THEORY OF OPERATION

The ADRF5420 integrates a driver to perform logic functions internally and provides the user with the advantage of a simplified CMOS-compatible and LVTTL-compatible control interface. This driver features a single digital control input pin, CTRL. The logic level applied to the CTRL pin determines which RF port is in the insertion loss state and in the isolation state (see Table 7).

RF INPUT AND OUTPUT

The RF ports (RFC, RF1, and RF2) are DC-coupled to 0 V, and no DC-blocking is required at the RF ports when the RF line potential is equal to 0 V. The RF ports are internally matched to 50 Ω.

The ADRF5420 is bidirectional with equal power-handling capabilities. The RF input signal can be applied to the RFC port or the selected RF throw port.

The insertion loss path conducts the RF signal between the selected RF throw port and the RF common port. The isolation paths provide high loss between the insertion loss path and the unselected RF throw port. The unselected RF port of the ADRF5420 is reflective.

The power handling of the ADRF5420 derates with frequencies less than 3 GHz and more than 70GHz. See Figure 2 and Figure 3 for derating of the RF power towards lower and higher frequencies.

POWER SUPPLY

The ADRF5420 requires a positive supply voltage applied to the VDD pin and a negative supply voltage applied to the VSS pin. Bypassing capacitors are recommended on the supply lines to filter high frequency noise.

The ideal power-up sequence is as follows:

1. Connect GND.
2. Power up VDD and VSS. Power up VSS after VDD to avoid current transients on VDD during ramp up.
3. Apply the digital control input. Powering the digital control input before the VDD supply can inadvertently forward bias and damage the internal ESD protection structures. To avoid this damage, use a series 1kΩ resistor to limit the current flowing into the CTRL pin. Use pull-up or pull-down resistors if the controller is in a high impedance state after VDD is powered up and the CTRL pin is not driven to a valid logic state.
4. Apply an RF input signal.

The ideal power-down sequence is the reverse order of the power-up sequence.

Table 7. Control Voltage Truth Table

	RF Path	
Digital Control Input (V_{CTRL})	**RF1 to RFC**	**RF2 to RFC**
Low	Isolation (off)	Insertion loss (on)
High	Insertion loss (on)	Isolation (off)

APPLICATIONS INFORMATION

The ADRF5420 has two power supply pins (VDD and VSS) and one control pin (CTRL). Figure 17 shows the external components and connections for the supply pin. The VDD, VSS, and CTRL pins are decoupled with a 100pF multilayer ceramic capacitor. The device pinout allows the placement of the decoupling capacitors close to the device. No other external components are needed for bias and operation, except DC blocking capacitors on the RF pins when the RF lines are biased at a voltage different than 0V. Refer to the Pin Configuration and Function Descriptions section for further details.

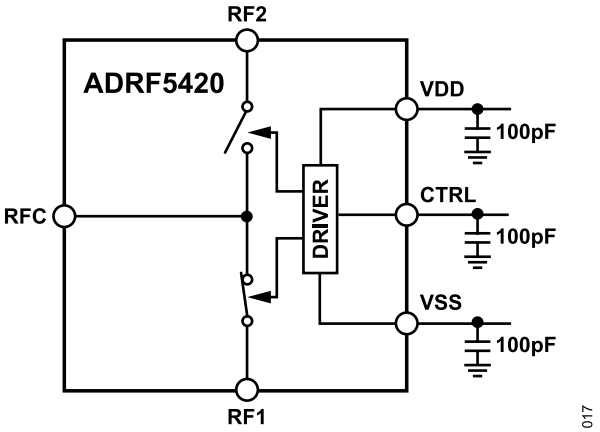

Figure 17. Recommended Schematic

APPLICATIONS INFORMATION

RECOMMENDATIONS FOR PCB DESIGN

The RF ports are matched to 50Ω internally, and the pinout is designed to mate a coplanar waveguide (CPWG) with 50Ω characteristic impedance on the PCB. Figure 18 shows the referenced CPWG design for a 150µm thick Megtron6 2×1080 R-5775G dielectric material. The RF trace with 300µm width and 300µm gap is used for 42µm finished copper thickness.

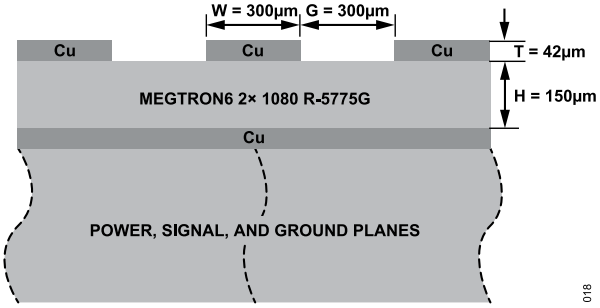

Figure 18. Probe Board Stackup

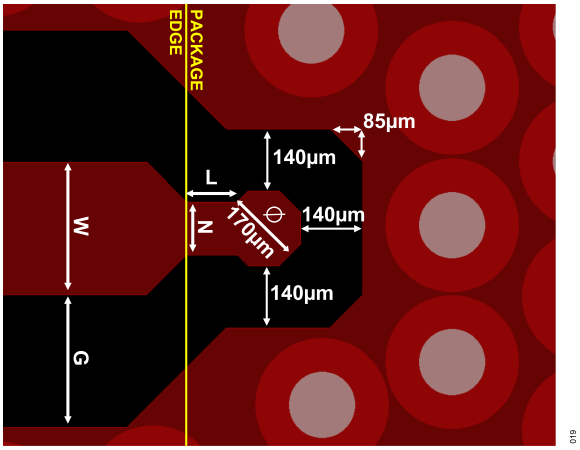

Figure 19. Recommended RF Pin Transitions

Figure 19 shows the recommended layout from the device RF pins to the 50Ω CPWG. Signal pads have a 170µm diameter extended with a neck for broadband tuning and tapered to RF trace with a 45° angle. The optimized RF pin transitions for broadband performance is given for different stackups in Table 8. For further recomenndations on alternate PCB stackups with different dielectric thickness and CPWG design, contact Analog Devices, Inc., Analog Devices Support.

Table 8. Recommended RFx Pin Transitions for Different Stackups

RF Stackup Height and Dielectric		RF Trace Dimensions		ADRF5420	Transition Dimensions	
H (µm)	Er	W (µm)	G (µm)	Mnemonics	N (µm)	L (µm)
85	3.02	180	250	RFC	100	190
				RF1, RF2	100	215
100	3.34	200	225	RFC	120	190
				RF1, RF2	120	165
115	3.40	225	250	RFC	120	140
				RF1, RF2	120	165
125	3.00	250	225	RFC	120	90
				RF1, RF2	120	165
150[1]	3.40	300	300	RFC	120	90
				RF1, RF2	120	165
175	3.16	360	245	RFC	120	90
				RF1, RF2	120	165
190	3.00	425	225	RFC	170	90
				RF1, RF2	170	165
200	3.55	425	275	RFC	170	90
				RF1, RF2	170	165

[1] Design reference and generic footprint.

APPLICATIONS INFORMATION

DIE ASSEMBLY

The ADRF5420 complies with the standard RoHS reflow assembly process and can be assembled together with other surface-mounted technology (SMT) components in the same reflow cycle. The PCB must incorporate fiduicials close to the device to get the best pick and place accuracy.

The top copper layer of the PCB is designed for optimum RF performance, and the solder mask and paste mask layers are designed for optimum assembly yield. The ground pads are drawn as solder mask defined. The signal pads are drawn as pad defined. The same solder mask and paste mask design is used for both pads. Alternatively, the ADRF5420 can be assembled without applying a solder paste on the PCB. If no solder paste is applied, the device must be dipped into flux prior to placement on the PCB.

Reflow Assembly with Solder Paste

Solder mask openings of 175µm in a square shape are recommended for the signal and RF pads, and solder mask openings of 150µm in a square shape are recommended for the GND pads. Solder mask thickness must not exceed 50µm. Paste mask is drawn circular with a 150µm diameter. Using a stencil with 2mil thickness and no aperture reduction yields the optimum paste mask print. The device does not need any flux dipping during the pick and place process.

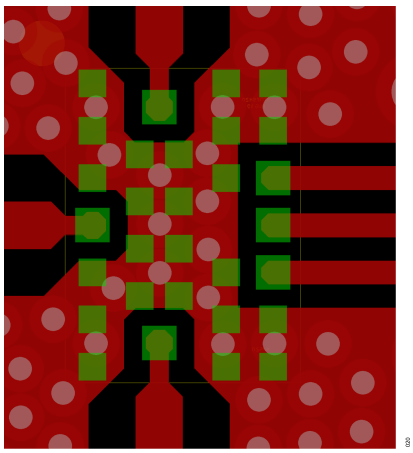

Figure 20. Recommended Footprint for Solder Paste

Reflow Assembly with Flux Dipping

Solder mask openings in a circular shape and 130µm in diameter are recommended. Solder mask thickness must not exceed 50µm. Solder paste is not applied. The device is dipped into flux prior to placement on the board.

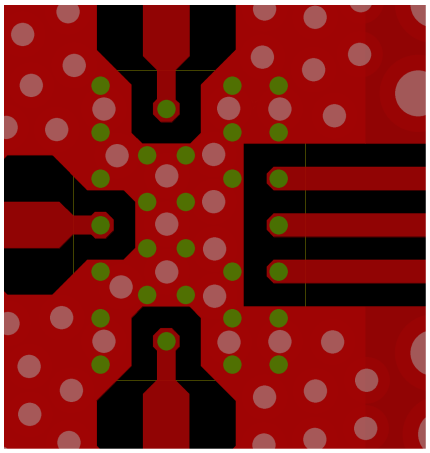

Figure 21. Recommended Footprint for Flux Dip Assembly

Assembly Durability

The device is a bumped die. The bump composition is copper (Cu) pillar with a plated tin (Sn) and silver (Ag) solder-cap, which forms the device interconnect to PCB when it is attached with reflow. The integrity of the interconnect structures and solder joints are compromised by the accumulated stress over temperature due to a mismatch of the thermomechanical properties of the different materials in the complete assembly of the user hardware. The ADRF5420 fulfills the JEDEC JED47L requirements under the JESD22-A104 Condition J (0-100C) for 2300 temperature cycles while mounted on a 0.75mm thick laminate PCB, which is assembled using solder paste reflow and without any underfill material applied. Users must qualify their hardware for the environmental conditions aligned with their end-use requirements because differences in PCB properties and design, varied number of temperature cycles, soak and dwell times, and changes in temperature range, can affect thermomechanical results. Note that using a proper underfill adhesive significantly improves the integrity of the device assembly by reducing the stress exposed to the interconnect structures and solder joints.

OUTLINE DIMENSIONS

Package Drawing Option	Package Type	Package Description
CD-30-3	BUMPED_CHIP	38-Ball Bumped Bare Die Sales

For the latest package outline information and land patterns (footprints), go to Package Index.

ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Packaging Quantity	Package Option
ADRF5420BCDZ	−40°C to +105°C	30-Ball Bumped Bare Die Sales [BUMPED_CHIP]	Cut-Tape, 1 to 500	CD-30-3
ADRF5420BCDZ-R7	−40°C to +105°C	30-Ball Bumped Bare Die Sales [BUMPED_CHIP]	Reel, 500	CD-30-3

[1] Z = RoHS-Compliant Part.