High Isolation, Silicon SP4T, Nonreflective Switch, 0.1GHz to 13GHz

FEATURES

- Frequency range: 100MHz to 13GHz
- Nonreflective, 50Ω design
- Low insertion loss
  - 1.3dB to 7GHz typical
  - 1.6dB to 13GHz typical
- High isolation
  - 46dB to 7GHz typical
  - 40dB to 13GHz typical
- High power handling (average)
  - 34dBm through path
  - 24dBm terminated path
  - 32dBm hot switching (RFC)
- High input linearity
  - P0.1dB: 34.5dBm typical
  - IP3: 61dBm typical
- Fast RF settling time 0.1dB: 230ns
- Single positive supply: 3.3V to 5V
- CMOS-/LVTTL-compatible
- 20-lead, 3mm × 3mm, LFCSP

APPLICATIONS

- Cellular infrastructure
- Wireless infrastructure
- Military radios, radars, and electronic counter measures (ECMs)
- Microwave radios and very small aperture terminals (VSATs)
- Test instrumentation

FUNCTIONAL BLOCK DIAGRAM

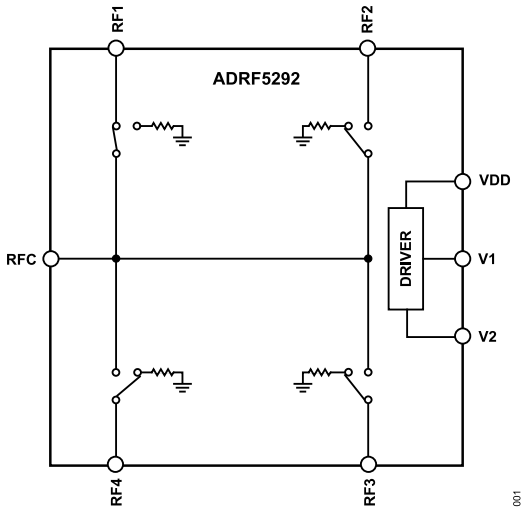


Figure 1. Functional Block Diagram

GENERAL DESCRIPTION

The ADRF5292 is a high isolation, nonreflective, 0.1GHz to 13GHz, silicon SP4T switch in the silicon process.

The ADRF5292 operates from 0.1GHz to 13GHz with an insertion loss lower than 1.6dB and an isolation higher than 40dB at 13GHz. The ADRF5292 has a nonreflective design, and the RF ports are internally terminated to 50Ω. The device has an input power handling capability of 34dBm (average) for through path, 24dBm (average) for terminated path, and 32dBm (average) hot switching at the RFC pin.

The ADRF5292 requires a single-supply voltage (V_{DD}) of 3.3V to 5V. The ADRF5292 employs 1.8V complementary metal-oxide semiconductor (CMOS)-compatible and 3.3V low-voltage transistor logic (LVTTL)-compatible controls.

The ADRF5292 comes in a 20-lead, 3mm × 3mm, LFCSP and can operate from −40°C to +125°C.

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REVISION HISTORY

12/2025—Rev. 0 to Rev. A

Changes to Ordering Guide 15

10/2025—Revision 0: Initial Version

SPECIFICATIONS

Positive supply voltage (V_{DD}) = 5V, Control Voltage 1 (V_1) and Control Voltage 2 (V_2) = 0V or 5V, and T_{CASE} = 25°C, with a 50Ω system, unless otherwise noted. RFx refers to RF1 to RF4.

Table 1. Electrical Characteristics for V_{DD} = 5V

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
FREQUENCY RANGE	f		0.1		13	GHz
INSERTION LOSS						
Between RFC and RFx (On)		0.1GHz to 2GHz		1.0		dB
		2GHz to 7GHz		1.3		dB
		7GHz to 13GHz		1.6		dB
RETURN LOSS						
RFC (On State)		0.1GHz to 13GHz		<20		dB
RFx (On State)		0.1GHz to 7GHz		<20		dB
		7GHz to 13GHz		17		dB
RFx (Terminated State)		0.4GHz to 13GHz		<20		dB
ISOLATION						
Between RFC and RFx		0.1GHz to 2GHz		55		dB
		2GHz to 7GHz		46		dB
		7GHz to 13GHz		40		dB
Between RFx and RFx		0.1GHz to 2GHz		55		dB
		2GHz to 7GHz		45		dB
		7GHz to 13GHz		40		dB
SWITCHING CHARACTERISTICS						
Rise Time and Fall Time	t_{RISE}, t_{FALL}	10% to 90% of RF output (RF_{OUT})		40		ns
On Tine and Off Time	t_{ON}, t_{OFF}	50% V_{CTRL} to 90% of RF_{OUT}		130		ns
RF Settling Time, 0.1dB	$t_{SETTLING}$	50% V_{CTRL} to 0.1dB of final RF_{OUT}		230		ns
INPUT LINEARITY[1]		0.4GHz to 10GHz				
0.1dB Power Compression	P0.1dB	V_{DD} = 5V		34.5		dBm
Third-Order Intercept	IP3	Two- tone input power = 14dBm each tone, Δf = 1MHz		61		dBm
SUPPLY CURRENT	I_{DD}	V_{DD} = 5V		480		µA
DIGITAL CONTROL INPUTS		V1 and V2 pins				
Voltage		V_{DD} = 5V				
Low	V_{INL}		0		0.8	V
High	V_{INH}		1.07		5	V
Current						
Low	I_{INL}	V_1 and V_2 = 0V, V_{DD} = 5V		<1		µA
High	I_{INH}	V_1 = 5V, V_{DD} = 5V		63		µA
		V_2 = 5V, V_{DD} = 5V		63		µA
RECOMMENDED OPERATING CONDITONS						
Supply Voltage	V_{DD}		4.75	5	5.25	V
RF Input Power [2]	P_{IN}	f = 100MHz to 10GHz, T_{CASE} = 85°C[3, 4]				
Through Path		RF signal is applied to RFC or through the connected RF throw port (selected RFx)				
Average					34	dBm
Peak[5]					34	dBm
Terminated Path		RF signal is applied to the unselected RFx port				
Average					24	dBm
Peak					29	dBm

SPECIFICATIONS

Table 1. Electrical Characteristics for V_{DD} = 5V (Continued)

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
Hot Switching (RFC)		RF signal is applied to RFC while switching between RFx ports				
Average					32	dBm
Peak					32	dBm
Hot Switching (RFx)		RF signal is applied to RFx port while switching				
Average					24	dBm
Peak					29	dBm
Case Temperature	T_{CASE}		−40		+125	°C

[1] For input linearity performance over frequency, see Figure 22 to Figure 25.

[2] For power derating over frequency, see the Power Derating Curves section.

[3] For 105°C operation, the average power handling degrades 3dB, and the peak power handling degrades 1dB from the T_{CASE} = 85°C specifications.

[4] For 125°C operation, the average power handling degrades 16dB, and the peak power handling degrades 4dB from the T_{CASE} = 85°C specifications.

[5] Peak has a ≤100 ns pulse duration and 5% duty cycle.

V_{DD} = 3.3V, V_1 and V_2 = 0V or 3.3V, and T_{CASE} = 25°C, with a 50Ω system, unless otherwise noted. RFx refers to RF1 to RF4.

Table 2. Electrical Characteristics for V_{DD} = 3.3V

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
FREQUENCY RANGE	f		0.1		13	GHz
INSERTION LOSS						
Between RFC and RFx (On)		0.1GHz to 2GHz		1.1		dB
		2GHz to 7GHz		1.3		dB
		7GHz to 13GHz		1.7		dB
RETURN LOSS						
RFC (On State)		0.1GHz to 13GHz		<20		dB
RFx (On State)		0.1GHz to 7GHz		<20		dB
		7GHz to 13GHz		17		dB
RFx (Terminated State)		0.4GHz to 13GHz		<20		dB
ISOLATION						
Between RFC and RFx (Off)		0.1GHz to 2GHz		55		dB
		2GHz to 7GHz		44		dB
		7GHz to 13GHz		40		dB
Between RFx and RFx		0.1GHz to 2GHz		55		dB
		2GHz to 7GHz		45		dB
		7GHz to 13GHz		40		dB
SWITCHING CHARACTERISTICS						
Rise Time and Fall Time	t_{RISE}, t_{FALL}	10% to 90% of RF_{OUT}		70		ns
On Time and Off Time	t_{ON}, t_{OFF}	50% V_{CTRL} to 90% of RF_{OUT}		160		ns
RF Settling Time	$t_{SETTLING}$	50% V_{CTRL} to 0.1 dB of final RF_{OUT}		250		ns
INPUT LINEARITY[1]		400MHz to 10GHz				
0.1dB Power Compression	P0.1dB	V_{DD} = 3.3V		32		dBm
Third-Order Intercept	IP3	Two-tone input power = 14dBm each tone, Δf = 1MHz		58		dBm
SUPPLY CURRENT	I_{DD}	V_{DD} = 3.3V		350		µA
DIGITAL CONTROL INPUTS		V1 and V2 pins				
Voltage		V_{DD} = 3.3V				
Low	V_{INL}		0		0.8	V
High	V_{INH}		1.07		3.3	V

SPECIFICATIONS

Table 2. Electrical Characteristics for V_{DD} = 3.3V (Continued)

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
Current						
Low	I_{INL}	V_1 and V_2 = 0V, V_{DD} = 3.3V		<1		µA
High	I_{INH}	V_1 = 5V, V_{DD} = 3.3V		11		µA
		V_2 = 5V, V_{DD} = 3.3V		11		µA
RECOMMENDED OPERATING CONDITONS						
Supply Voltage	V_{DD}		3.15	3.3	3.45	V
RF Input Power [2]	P_{IN}	f = 100MHz to 10GHz, T_{CASE} = 85°C[3, 4]				
Through Path		RF signal is applied to RFC or through connected RF throw port (selected RFx)				
Average					32	dBm
Peak[5]					32	dBm
Terminated Path		RF signal is applied to the unselected RFx port				
Average					23	dBm
Peak					28	dBm
Hot Switching (RFC)		RF signal is applied to RFC while switching between RFx ports				
Average					30	dBm
Peak					30	dBm
Hot Switching (RFx)		RF signal is applied to RFx port while switching				
Average					23	dBm
Peak					28	dBm
Case Temperature	T_{CASE}		−40		+125	°C

1 For input linearity performance over frequency, see Figure 22 to Figure 25.

2 For power derating over frequency, see the Power Derating Curves section.

3 For 105°C operation, the average power handling degrades 3dB, and the peak power handling degrades 1dB from the T_{CASE} = 85°C specifications.

4 For 125°C operation, the average power handling degrades 16dB, and the peak power handling degrades 4dB from the T_{CASE} = 85°C specifications.

5 Peak has a ≤100 ns pulse duration and 5% duty cycle.

ABSOLUTE MAXIMUM RATINGS

For recommended operating conditions, see Table 1 and Table 2.

Table 3. Absolute Maximum Ratings

Parameter	Rating
Supply Voltage	−0.3V to +5.8V
Digital Control Inputs[1]	
Voltage	−0.5V to V_{DD} + 0.3V
Current	3mA
RF Input Power (V_{DD} = 5V)[2, 3, 4]	
Through Path	
Average	35dBm
Peak[5]	35dBm
Terminated Path	
Average	25dBm
Peak	30dBm
Hot Switching (RFC)	
Average	31dBm
Peak	31dBm
Hot Switching (RFx)	
Average	25dBm
Peak	30dBm
RF Input Power (V_{DD} = 3.3V)	
Through Path	
Average	33dBm
Peak	33dBm
Terminated Path	
Average	24dBm
Peak	29dBm
Hot Switching (RFC)	
Average	31dBm
Peak	31dBm
Hot Switching (RFx)	
Average	24dBm
Peak	29dBm
RF Power Under Unbiased Condition (V_{DD} = 0V)	18dBm
Temperature	
Junction (T_j)	135°C
Storage	−65°C to +150°C
Reflow	260°C

1 Overvoltages at the digital control inputs are clamped by internal diodes. Current must be limited to the maximum rating given.

2 For power derating over frequency, see Figure 2 and Figure 3.

3 For 105°C operation, the average power handling degrades 3dB, and the peak power handling degrades 1dB from the T_{CASE} = 85°C specifications.

4 For 125°C operation, the average power handling degrades 16dB, and the peak power handling degrades 4dB from the T_{CASE} = 85°C specifications.

5 Peak has a ≤100 ns pulse duration and 5% duty cycle.

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

Only one absolute maximum rating can be applied at any one time.

THERMAL RESISTANCE

Thermal performance is directly linked to printed circuit board (PCB) design and operating environment. Careful attention to PCB thermal design is required.

θ_{JC} is the junction to case bottom (channel to package bottom) thermal resistance.

Table 4. Thermal Resistance

Package Type	θ_{JC}	Unit
CR-20-2		
Through Path	62	°C/W
Terminated Path	200	°C/W

POWER DERATING CURVES

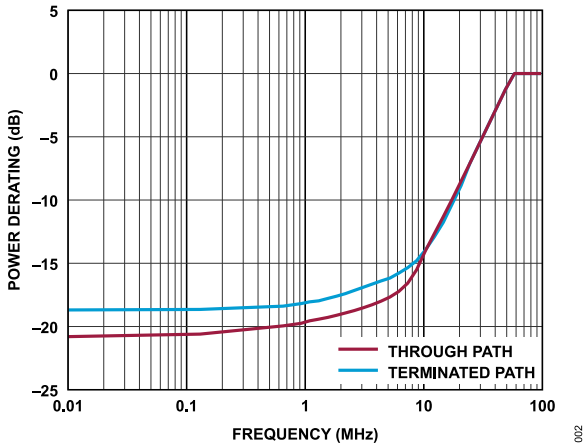


Figure 2. Power Derating vs. Frequency, Low Frequency Detail, T_{CASE} = 85°C

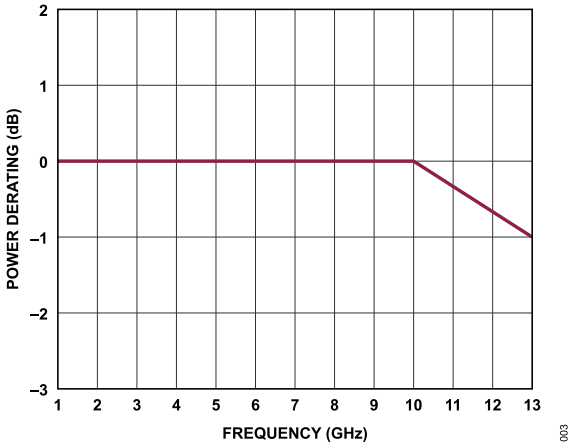


Figure 3. Power Derating vs. Frequency, High Frequency Detail, T_{CASE} = 85°C

ABSOLUTE MAXIMUM RATINGS

ELECTROSTATIC DISCHARGE (ESD) RATINGS

The following ESD information is provided for handling of ESD-sensitive devices in an ESD protected area only.

Human body model (HBM) per ANSI/ESDA/JEDEC JS-001.

Charged device model (CDM) ratings are per ANSI/ESDA/JEDEC JS-002.

ESD Ratings for the ADRF5292

Table 5. ADRF5292, 20-Lead LFCSP_RT

ESD Model	Withstand Threshold (V)	Class
HBM		
RFC and RFx Pins	±500	1B
Supply and Control Pins	±2000	2
CDM	±500	C2A

ESD CAUTION



ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

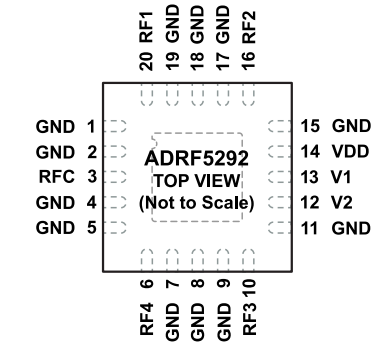


Figure 4. Pin Configuration

Table 6. Pin Function Descriptions

Pin No.	Mnemonic	Description
1, 2, 4, 5, 7, 8, 9, 11, 15, 17, 18, 19	GND	Grounds. The package bottom has an exposed metal pad that must connect to the PCB RF ground.
3	RFC	RF Common Port. The RFC pin is DC-coupled and matched to 50Ω. A DC blocking capacitor is required on this pin. See Figure 5 for the interface schematic.
6	RF4	RF Throw Port 4. The RF4 pin is DC-coupled and matched to 50Ω. A DC blocking capacitor is required on this pin. See Figure 5 for the interface schematic.
10	RF3	RF Throw Port 3. The RF3 pin is DC-coupled and matched to 50Ω. A DC blocking capacitor is required on this pin. See Figure 5 for the interface schematic.
12	V2	Control Input 2. See Figure 6 for the interface schematic.
13	V1	Control Input 1. See Figure 6 for the interface schematic.
14	VDD	Supply Voltage Pin. See Figure 7 for the interface schematic.
16	RF2	RF Throw Port 2. The RF2 pin is DC-coupled and matched to 50Ω. A DC blocking capacitor is required on this pin. See Figure 5 for the interface schematic.
20	RF1	RF Throw Port 1. The RF1 pin is DC-coupled and matched to 50Ω. A DC blocking capacitor is required on this pin. See Figure 5 for the interface schematic.
	EPAD	Exposed Pad. Exposed pad must be connected to RF and DC ground.

INTERFACE SCHEMATICS

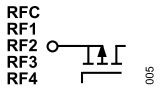


Figure 5. RFC, RF1, RF2, RF3, and RF4 Interface Schematic

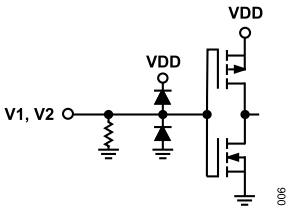


Figure 6. V1, V2 Interface Schematic

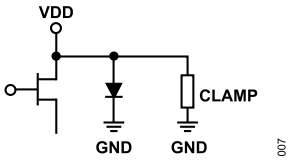


Figure 7. VDD Interface Schematic

TYPICAL PERFORMANCE CHARACTERISTICS

INSERTION LOSS, ISOLATION, AND RETURN LOSS

V_{DD} = 3.3V or 5V, V_1 and V_2 = 0V or VDD, and T_{CASE} = 25°C, with a 50 Ω system, unless otherwise noted. RFx refers to RF1 to RF4.

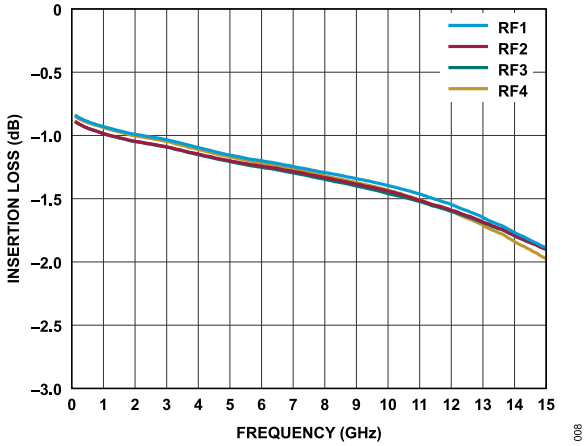


Figure 8. Insertion Loss vs. Frequency, (V_{DD} = 5V)

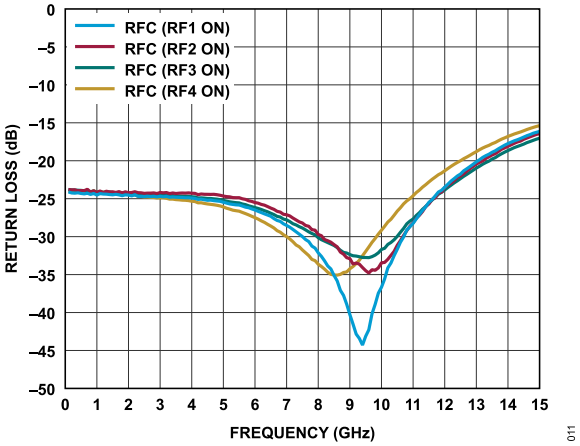


Figure 11. Return Loss for RFC vs. Frequency (V_{DD} = 3.3V to 5V)

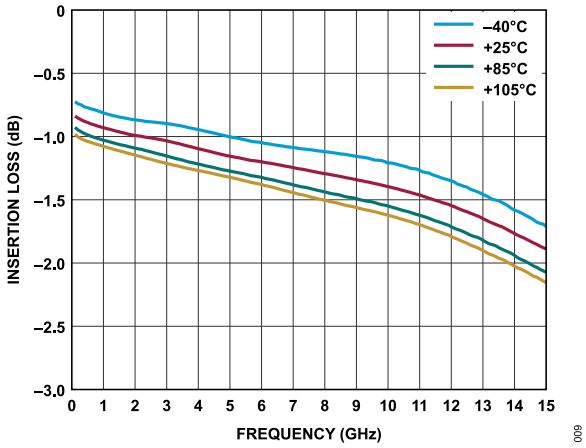


Figure 9. Insertion Loss vs. Frequency over Temperature (V_{DD} = 5V, RF1 Selected)

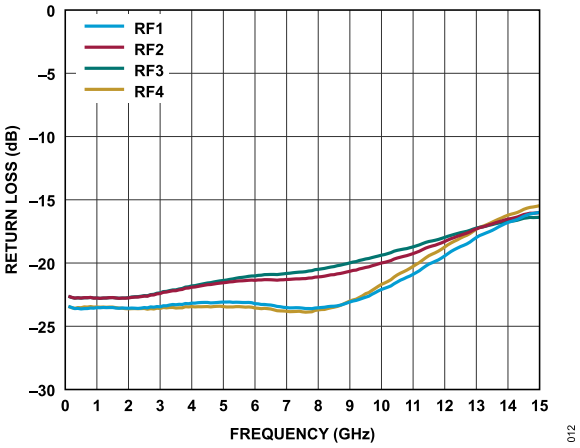


Figure 12. Return Loss for Selected RFx vs. Frequency (V_{DD} = 3.3V to 5V)

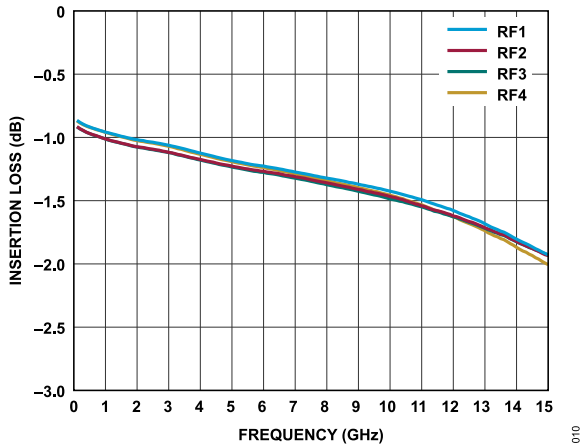


Figure 10. Insertion Loss vs. Frequency, (V_{DD} = 3.3V)

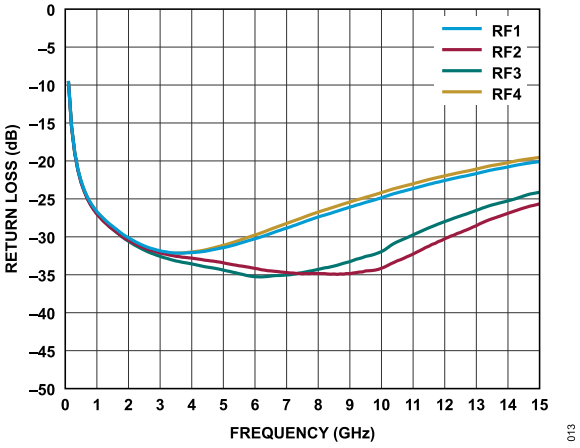


Figure 13. Return Loss for Unselected RFx vs. Frequency (V_{DD} = 3.3V to 5V)

TYPICAL PERFORMANCE CHARACTERISTICS

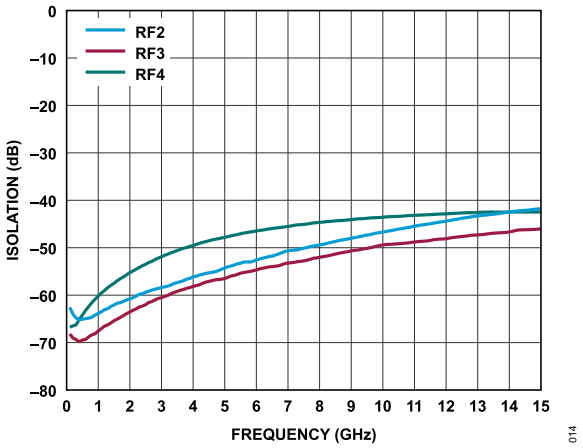


Figure 14. Isolation for RFC to RFx Off vs. Frequency, RFC to RF1 Path Selected (V_{DD} = 3.3V to 5V)

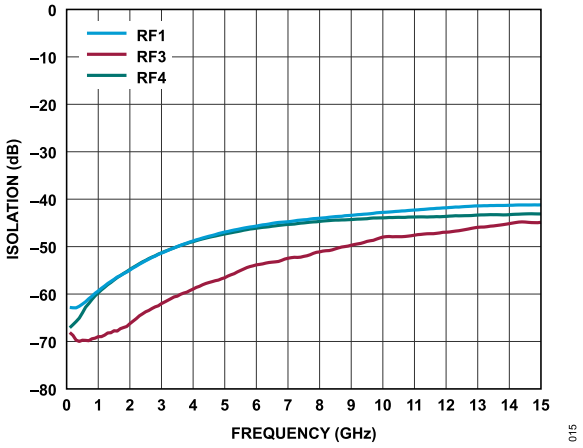


Figure 15. Isolation for RFC to RFx Off vs. Frequency, RFC to RF2 Path Selected (V_{DD} = 3.3V to 5V)

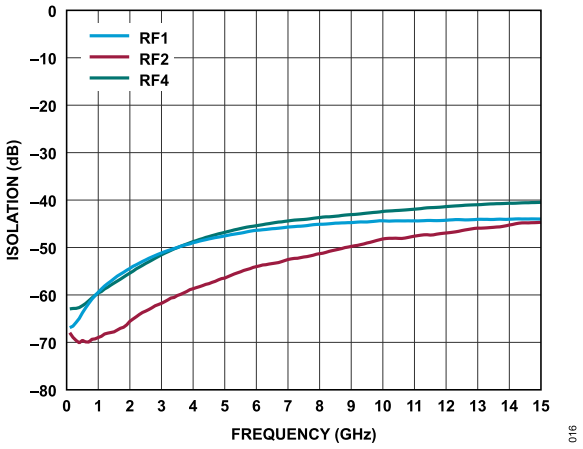


Figure 16. Isolation for RFC to RFx Off vs. Frequency, RFC to RF3 Path Selected (V_{DD} = 3.3V to 5V)

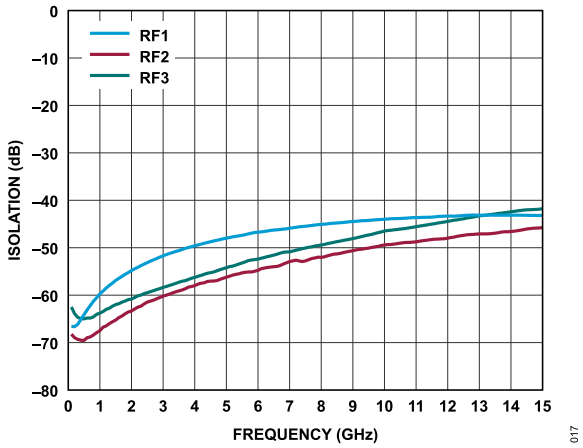


Figure 17. Isolation for RFC to RFx Off vs. Frequency, RFC to RF4 Path Selected (V_{DD} = 3.3V to 5V)

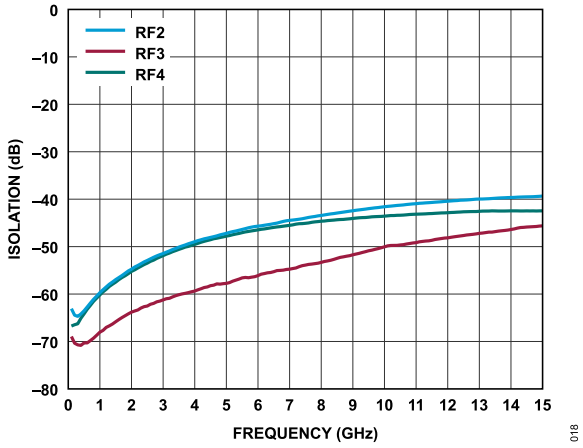


Figure 18. Channel to Channel Isolation vs. Frequency, RFC to RF1 Path Selected (V_{DD} = 3.3V to 5V)

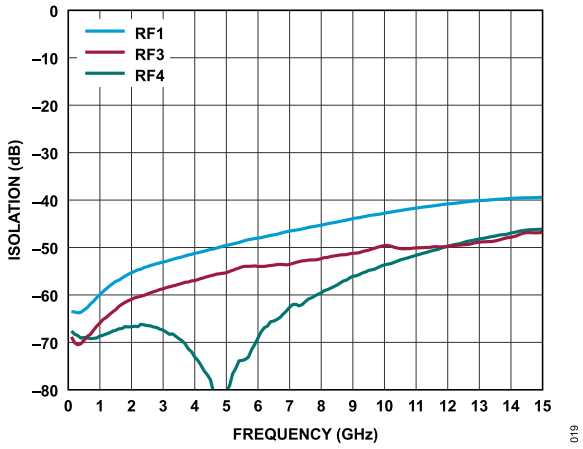


Figure 19. Channel to Channel Isolation vs. Frequency, RFC to RF2 Path Selected (V_{DD} = 3.3V to 5V)

TYPICAL PERFORMANCE CHARACTERISTICS

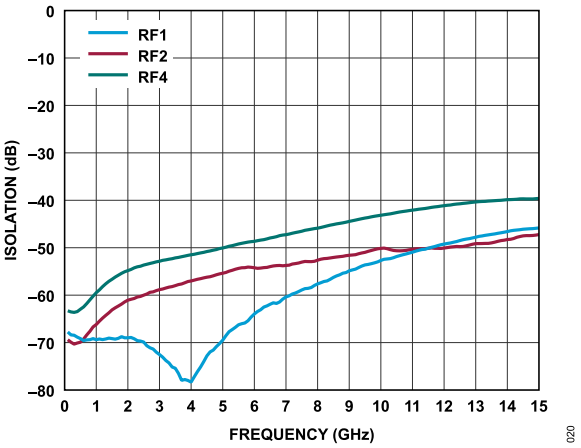


Figure 20. Channel to Channel Isolation vs. Frequency, RFC to RF3 Path Selected (V_{DD} = 3.3V to 5V)

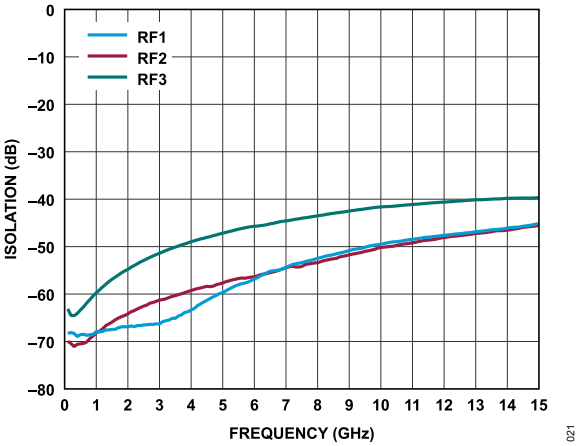


Figure 21. Channel to Channel Isolation vs. Frequency, RFC to RF4 Path Selected (V_{DD} = 3.3V to 5V)

TYPICAL PERFORMANCE CHARACTERISTICS

INPUT POWER COMPRESSION AND THIRD-ORDER INTERCEPT

V_{DD} = 3.3V or 5V, V_1 and V_2 = 0V or VDD, and T_{CASE} = 25°C, with a 50 Ω system, unless otherwise noted. RFx refers to RF1 to RF4.

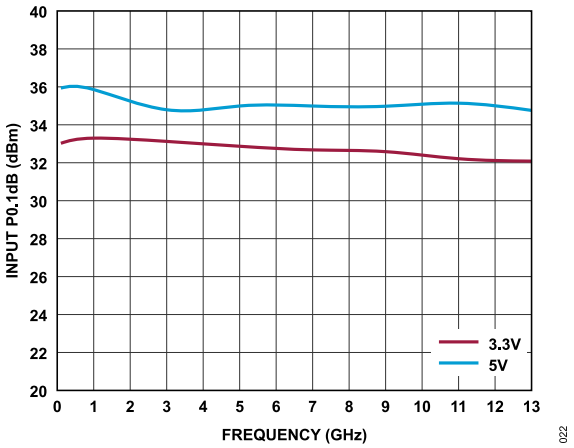


Figure 22. Input P0.1dB vs. Frequency

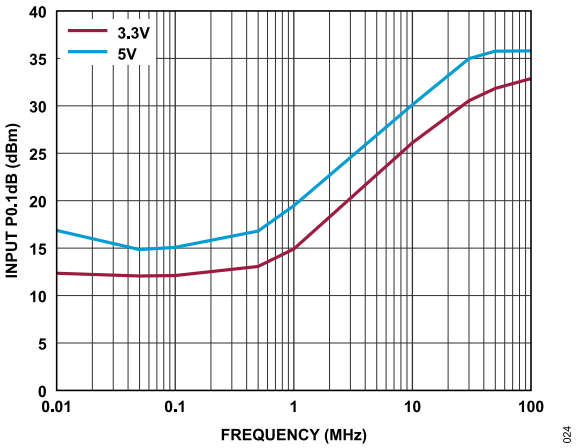


Figure 24. Input P0.1dB vs. Frequency (Low Frequency Detail)

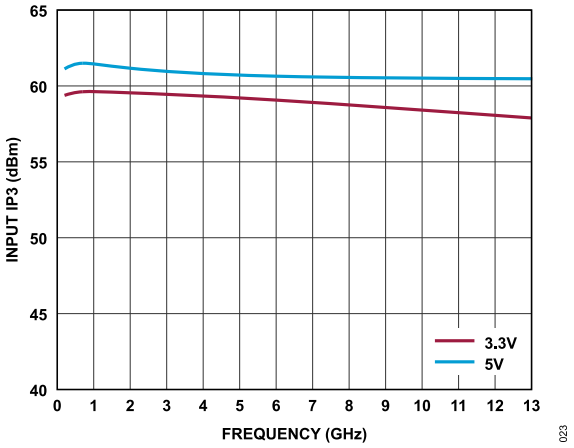


Figure 23. Input IP3 vs. Frequency

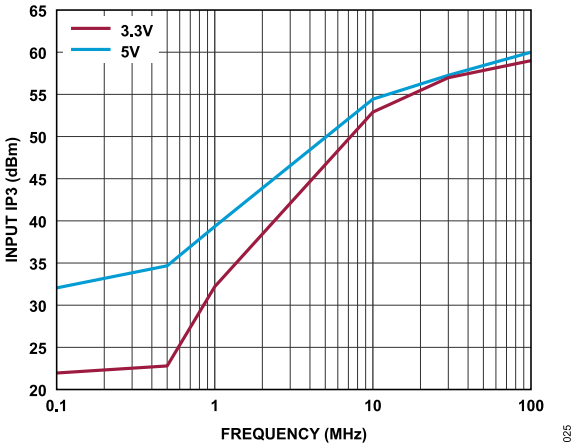


Figure 25. Input IP3 vs. Frequency (Low Frequency Detail)

THEORY OF OPERATION

The ADRF5292 integrates a driver to perform logic functions internally and to provide the advantage of a simplified CMOS-/LVTTL-compatible control interface. There are two digital control input pins (V1 and V2) that determine which RF port is in the insertion loss state and which RF port is in the isolation state. See Table 7 for the control voltage truth table.

Table 7. Control Voltage Truth Table

V1	V2	RFC to RF1	RFC to RF2	RFC to RF3	RFC to RF4
Low	Low	On	Off	Off	Off
High	Low	Off	On	Off	Off
Low	High	Off	Off	On	Off
High	High	Off	Off	Off	On

RF INPUT AND OUTPUT

The RF pins (RFC and RF1 to RF4) are DC-coupled, and DC blocking capacitors are required on the RF lines. The RF ports are internally matched to 50Ω. Therefore, external matching networks are not required.

The insertion loss path conducts the RF signal between the selected RF throw port and the RF common port. The isolation path provides high loss between the insertion loss path and the unselected RF throw port that is terminated to an internal 50Ω resistor.

The ADRF5292 is bidirectional with equal power handling capabilities. The RF input signal can be applied to the RFC port or the selected RF throw port.

POWER SUPPLY

The ADRF5292 requires a positive supply on the VDD pin. Bypassing capacitors are recommended on the supply lines to minimize RF coupling.

The power-up sequence is as follows:

1. Connect to GND.
2. Power up VDD.
3. Apply the digital control inputs. The relative order of the logic control inputs is not important. Powering the digital control inputs before VDD can inadvertently forward bias and damage ESD protection structures. To avoid this damage, use a series 1kΩ resistor to limit the current flowing into the digital control pins. Use pull-up or pull-down resistors if the controller is in a high impedance state after VDD is powered up and the control pins are not driven to a valid logic state.
4. Apply an RF input signal.

The ideal power-down sequence is the reverse order of the power-up sequence.

APPLICATIONS INFORMATION

The ADRF5292 has one power supply pin (VDD) and two digital control pins (V1 and V2). Figure 26 shows the external components and connections for the supply pin. The VDD pin is decoupled with a 100pF multilayer ceramic capacitor. The ADRF5292 pinout allows the placement of the decoupling capacitors close to the device. No other external components are needed for bias and operation, except DC blocking capacitors on the RF pins (RFC and RF1 to RF4). Wideband capable DC blocking capacitors are recommended for best performance.

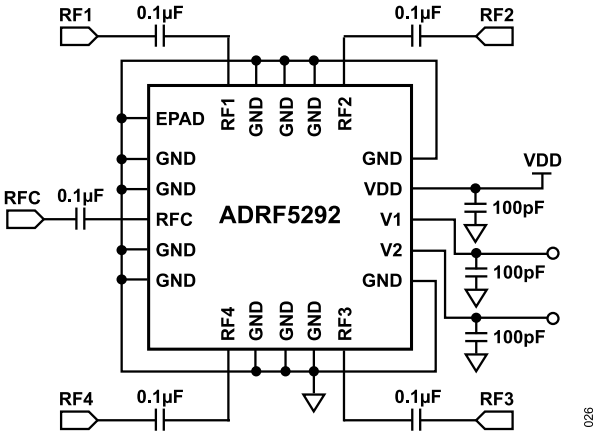


Figure 26. Recommended Schematic

RECOMMENDATIONS FOR PRINTED CIRCUIT BOARD DESIGN

The RF ports are matched to 50Ω internally, and the pinout is designed to mate a coplanar waveguide (CPWG) with a 50Ω characteristic impedance on the PCB. Figure 27 shows the referenced CPWG RF trace design for an RF substrate with 10mil thick Rogers RO4350B dielectric material. The RF trace with an 18mil width and 13mil clearance is recommended for 2.8mil finished copper thickness.

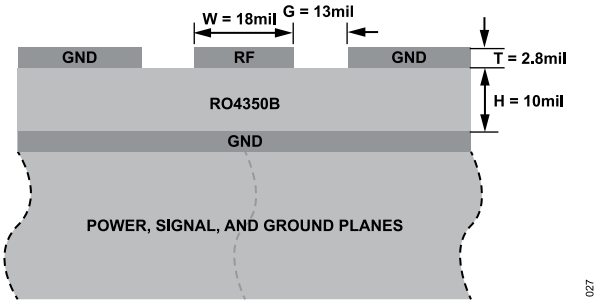


Figure 27. ADRF5292-EVALZ Stack-Up

Figure 28 shows the routing of the RF traces, supply, and control signals from the ADRF5292. The ground planes are connected with densely filled through vias for optimal RF and thermal performance. The primary thermal path for the ADRF5292 is the bottom side.

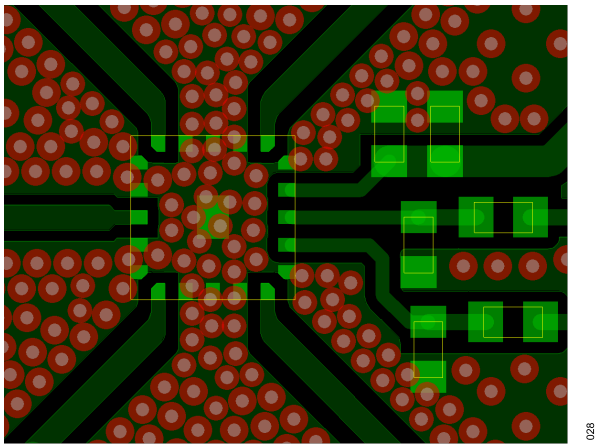


Figure 28. PCB Routings

Figure 29 shows the recommended layout from the RF pins (RFC and RF1 to RF4) of the ADRF5292 to the 50Ω CPWG on the referenced stack-up. PCB pads are drawn 1:1 to the device pads. The ground pads are drawn soldermask defined, and the signal pads are drawn as pad defined. The RF trace from the PCB pad is extended with the same width for a 5mil and tapered to the RF trace. The paste mask is designed to match the pads of the ADRF5292 without any aperture reduction. The paste mask is divided into multiple openings for the paddle.

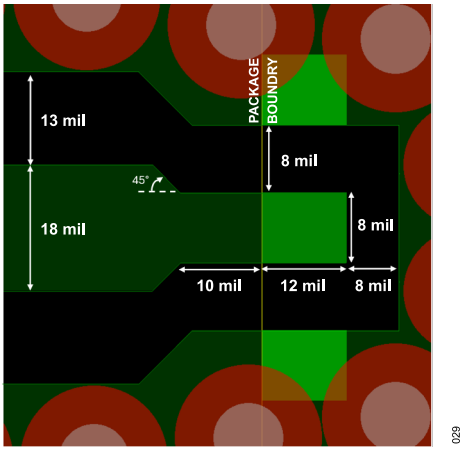


Figure 29. Recommended RF Pin Transition

For alternate PCB stack-ups with different dielectric thickness and CPWG design, contact Analog Devices, Inc., Technical Support Center for further recommendations.

OUTLINE DIMENSIONS

Package Drawing Option	Package Type	Package Description
CR-20-2	LFCSP_RT	20-Lead Lead Frame Chip Scale, Routable

For the latest package outline information and land patterns (footprints), go to Package Index.

ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Package Quantity	Package Option
ADRF5292BCRZN	−40°C to +125°C	20-Lead Lead Frame Chip Scale, Routable [LFCSP_RT]	Cut-Tape, 1500	CR-20-2
ADRF5292BCRZN-RL7	−40°C to +125°C	20-Lead Lead Frame Chip Scale, Routable [LFCSP_RT]	Reel, 1500	CR-20-2
ADRF5292BCRZN-RL	−40°C to +125°C	20-Lead Lead Frame Chip Scale, Routable [LFCSP_RT]	Reel, 5000	CR-20-2

[1] Z = RoHS-Compliant Part.

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