1600W, Nonisolated Quarter-Brick DC-DC Power Module

ADPM12160

Product Features

- Electrical
  - 40V to 60V Input Voltage Range
  - 12V/12.5V Fully Regulated Output Voltage
  - Thermal Design Power up to 1600W
  - Peak Power up to 2400W
  - Peak Efficiency up to 98% at Half Load
  - Fully Protected: OTP, Input UVLO and OVLO, Input OCP, Output OVP, Output OCP, and SCP
  - No Minimum Load Required
  - Fast Load-Transient Response with Coupled Inductor
  - Optional Logic for Remote ON/OFF (REM)
  - PMBus™ Configuration
  - Event Data Recorder (Black Box)
  - Parallel Operation with Active Current Sharing
  - Nonisolated
- Mechanical
  - Industry-Standard Quarter-Brick Footprint: 58.4mm × 36.8mm × 15.1mm (2.30in × 1.45in × 0.59in)
  - Optional Pin Length: 2.79mm, 3.70mm, or 4.32mm
- Safety and Certificates
  - IEC/UL/EN/CSA 62368-1
  - Compliance with RoHS EU Directive 2011/65/EU and (EU)2015/863
  - ISO 9001, TL 9000, ISO 14001, ISO 45001 Certified Manufacturing Facility

Key Applications

- Distributed Power Architectures
- Wireless Networks
- Access and Optical Network Equipment
- Enterprise Networks
- Latest-Generation ICs (DSP, FPGA, and ASIC) and Microprocessor-Powered Applications



General Description

The ADPM12160 is a high-power, quarter-brick DC-DC converter that provides up to 98% efficiency at half load.

The ADPM12160 is a nonisolated converter that delivers a fully regulated 12V/12.5V output with a continuous power level of 1600W and a peak power capability of up to 2400W for limited time.

***Ordering Information* appears at the end of the data sheet.**

Rev 2; 4/26

© 2026 Analog Devices, Inc. All rights reserved. Trademarks and registered trademarks are the property of their respective owners.

Absolute Maximum Ratings

IN to GND (when V_{IN} > V_{IN}, OVLO, module enters into input OVLO) ..... -0.5V to +75V

Operating Ambient Temperature (T_A)..... -40°C to +85°C

Storage Temperature ..... -55°C to +125°C

Operating Humidity (noncondensing)..... +85RH (%)

Storage Humidity (noncondensing) ..... +85RH (%)

Operating Altitude ..... 0 to +3000m

Storage Altitude ..... 0 to +3000m

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Electrical Characteristics

(V_{IN} = 40V to 60V, T_A = +25°C, C_{IN}, EXT = 200µF, C_{OUT}, EXT = 1500µF (550µF MLCC, OS-CON for others), resistive load, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
INPUT CHARACTERISTICS							
Operating Input Voltage	V_{IN}			40	54	60	V
Input Current	I_{IN}	V_{IN} = 40V to 60V, no load			160		mA
		V_{IN} = 40V, full load				45	A
		V_{IN} = 54V, disabled by REM			10		mA
Input Reflected Ripple Current	$I_{IN, RIPPLE}$	(see *Figure 1*)				300	mA, pk-pk
Recommended External Input Capacitance	$C_{IN, EXT}$			200			µF
REMOTE CONTROL CHARACTERISTICS							
REM Logic Threshold	V_{REM}	Logic high		2.4		20	V
		Logic low				0.8	
REM Current	I_{REM}	V_{REM} = 0V				0.3	mA
Leakage Current		Logic high, V_{REM} = 20V			30		µA
REM Voltage when Floating	$V_{REM_FLOATING}$				3		V
OUTPUT CHARACTERISTICS							
Output Voltage Set Point	$V_{OUT, SET}$	V_{IN} = 54V, I_{OUT} = 0A	ADPM12160CMLZxx	11.88	12	12.12	V
			ADPM12160CMLZxxA	12.35	12.5	12.65	
		Over V_{IN}, I_{OUT} range	ADPM12160CMLZxx	11.64		12.36	
			ADPM12160CMLZxxA	12.10		12.90	
Output Current Range	I_{OUT}	V_{IN} = 40V to 60V	ADPM12160CMLZxx	0		133.3	A
			ADPM12160CMLZxxA	0		128.0	
Peak Current Duration		I_{OUT} up to 200A				150	ms
Line Regulation		V_{IN} = 40V to 60V, I_{OUT} = 0A			60		mV
Load Regulation		V_{IN} = 54V, I_{OUT} = 0A to $I_{OUT, MAX}$			120		mV
Temperature Coefficient		T_A = -40°C to +85°C				200	ppm/°C
External Output Capacitance	$C_{OUT, EXT}$	No less than 550µF for ceramic, oscon for others		1500		30000	µF

(V_{IN} = 40V to 60V, T_A = +25°C, $C_{IN, EXT}$ = 200µF, $C_{OUT, EXT}$ = 1500µF (550µF MLCC, OS-CON for others), resistive load, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Dynamic Response	$\Delta V_{OUT, OVERSHOOT}$	75% ~ 50% of $I_{OUT, MAX}$ load step, di/dt = 1A/µs			250		mV
	$\Delta V_{OUT, UNDERSHOOT}$	50% ~ 75% of $I_{OUT, MAX}$ load step, di/dt = 1A/µs			250		mV
	Settling time	$C_{OUT, EXT}$ = 1500µF, di/dt = 1A/µs	Within 1% nominal V_{OUT}			200	µs
Ripple and Noise		$I_{OUT} = I_{OUT, MAX}$, $C_{OUT, EXT}$ = 1500µF + 10µF tantalum + 1µF ceramic	5Hz to 20MHz bandwidth		120		mV, pk-pk
			5Hz to 20MHz bandwidth		10	50	mV, RMS
Turn-On Delay Time	$t_{ON, DELAY}$	Time from instant at which V_{IN} = 40V, from REM assertion to V_{OUT} = 10% of $V_{OUT, SET}$			300		ms
Turn-On Rise Time	t_{RISE}	Time for V_{OUT} to rise from 10% to 90% of $V_{OUT, SET}$			45		ms
Current Sharing Accuracy		30% ~ 100% load	Four modules in parallel operation (Note 2)	-10		+10	%
Power-Good Signal	V_{PGOOD}			0		3.6	V
PROTECTION CHARACTERISTICS							
Input Undervoltage Lockout	$V_{IN, UVLO}$	V_{IN} rising		37	38	39	V
		V_{IN} falling		36	37	38	V
Input Overvoltage Lockout	$V_{IN, OVLO}$	Latch off (Note 1)			66		V
Output Overvoltage Lockout	$V_{OUT, OVLO}$	Latch off (Note 1)	ADPM12160CMLZxx		13.5		V
			ADPM12160CMLZxxA		14.0		V
Output Overcurrent Protection	I_{OCP}	Latch off (Note 1)	(Note 3)		275		A
Output Short-Circuit Protection		Latch off (Note 1)					
Overtemperature Protection	T_{OTP}	Retry (Note 1), PMBus report temperature			122		°C
GENERAL SPECIFICATIONS							
Efficiency	η	V_{IN} = 40V, half load			98.0		%
		V_{IN} = 54V, half load			97.8		%
		V_{IN} = 54V, full load			97.5		%
Switching Frequency	f_{SW}	V_{IN} = 54V, full load	Fixed frequency		180		kHz
FIT		10^9/MTBF			182		
MTBF		Telcordia SR-332, Issue 4, 2016, T_A = +40°C			5.5×10^6		hours
Weight					100		g
PMBUS							
CLK, DATA Input Logic Threshold	V_{IL}	Logic low				0.8	V
	V_{IH}	Logic high		2.1		3.6	V

(V_{IN} = 40V to 60V, T_A = +25°C, $C_{IN, EXT}$ = 200µF, $C_{OUT, EXT}$ = 1500µF (550µF MLCC, OS-CON for others), resistive load, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Output Logic Low	V_{OL}	Sinking current = 4mA	CLK, DATA, and ALERT pins			0.4	V
Leakage Current		CLK, DATA, and ALERT pins; logic output high		-5		+5	µA
Input Capacitance		CLK, DATA, and ALERT pins; inside the module			50		pF
CLK Frequency	f_{CLK}				100		kHz
Input Voltage Reporting Accuracy				-2		+2	V
Output Voltage Reporting Accuracy				-0.25		+0.25	V
Output Current Reporting Accuracy		< 30% load		-3		+3	A
		30% ~ 100% load		-6		+6	%
Temperature Reporting Range		(Note 4)		-40		+125	°C
Temperature Reporting Accuracy				-5		+5	°C

Note 1: The fault response is programmable with the options of retry, latch off, and ignore. See the *MFR_FAULT_RESPONSE (D9h)* section for more details.

Note 2: Current sharing accuracy is guaranteed by design and characterization only.

Note 3: OCP is a typical characterized value, and it is not production tested. The actual trip point level depends on operating conditions, including voltage, load, and temperature.

Note 4: Temperature reporting guaranteed accuracy up to +125°C.
Reporting may saturate or extend slightly beyond this range, but accuracy is not guaranteed above +125°C.
Temperature reporting range and temperature reporting accuracy are not production tested and are guaranteed by design.

Note 5: Safety: Compliant with IEC 62368-1, UL 62368-1, EN 62368-1, and CSA 62368-1.

Note 6: Vibration: IEC 60068-2-6, 10Hz to 500Hz sweep, 0.75mm excursion, 10g acceleration, 10min in each three perpendicular directions.

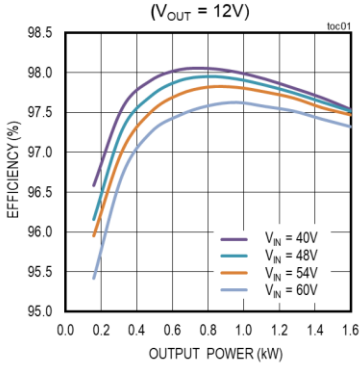
Note 7: Transportation: ETS 300019-1-2.

Note 8: Shock: IEC 60068-2-27, 200g acceleration, duration 3ms, six drops in each three perpendicular directions.

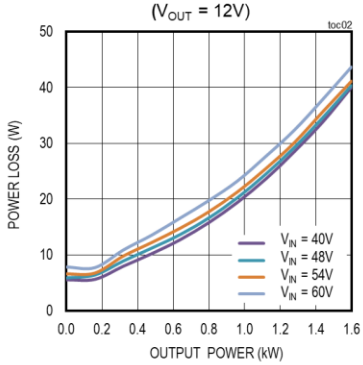
Typical Operating Characteristics

(T_A = +25°C, V_{IN} = 54V, V_{OUT} = 12V, unless otherwise noted.)

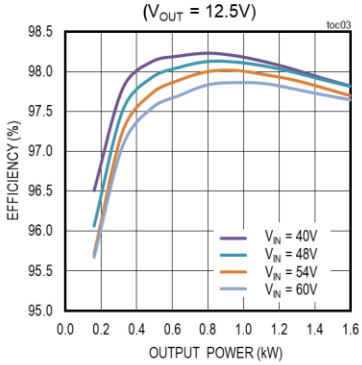
EFFICIENCY vs. OUTPUT POWER (V_{OUT} = 12V)



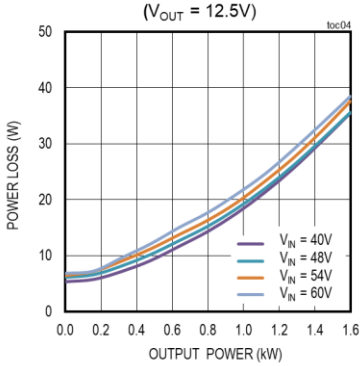
POWER LOSS vs. OUTPUT POWER (V_{OUT} = 12V)



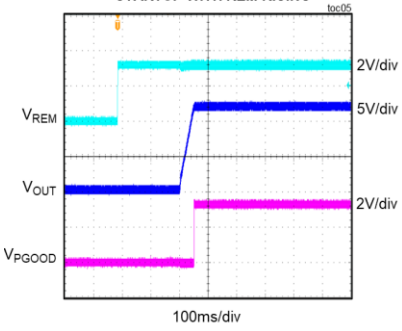
EFFICIENCY vs. OUTPUT POWER (V_{OUT} = 12.5V)



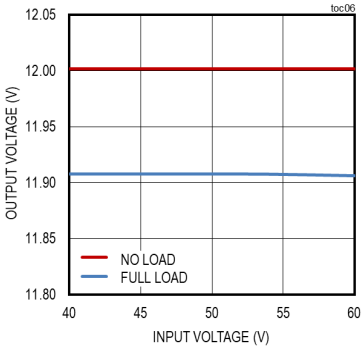
POWER LOSS vs. OUTPUT POWER (V_{OUT} = 12.5V)



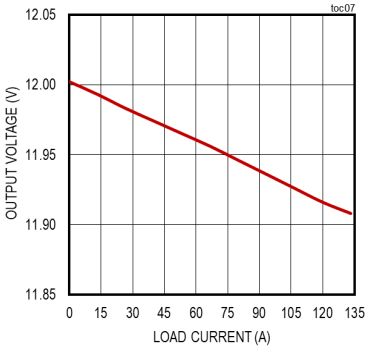
STARTUP WITH REM RISING



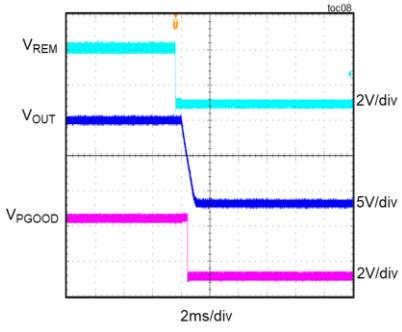
LINE REGULATION



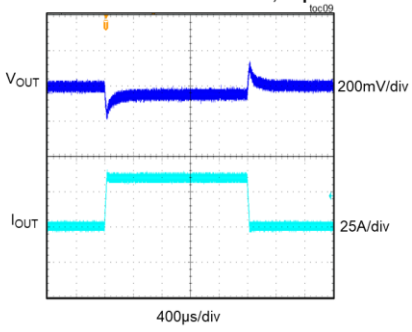
LOAD REGULATION



SHUTDOWN WITH REM FALLING

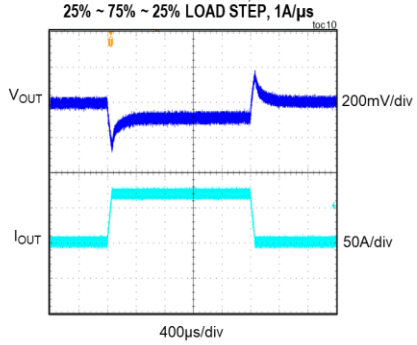


LOAD TRANSIENT WITH $C_{OUT, EXT}$ = 1.5mF
50% ~ 75% ~ 50% LOAD STEP, 1A/µs

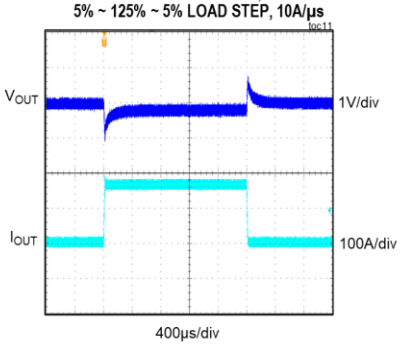


(T_A = +25°C, V_{IN} = 54V, V_{OUT} = 12V, unless otherwise noted.)

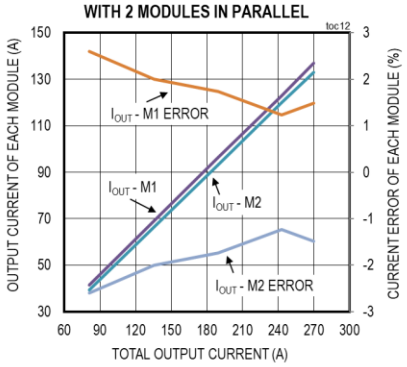
LOAD TRANSIENT WITH $C_{OUT, EXT}$ = 1.5mF
25% ~ 75% ~ 25% LOAD STEP, 1A/µs



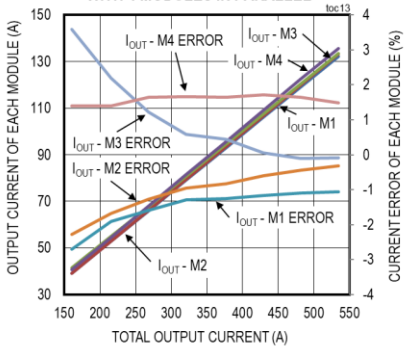
LOAD TRANSIENT WITH $C_{OUT, EXT}$ = 1.5mF
5% ~ 125% ~ 5% LOAD STEP, 10A/µs



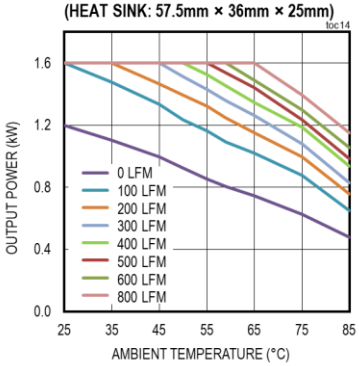
ACTIVE CURRENT SHARING
WITH 2 MODULES IN parallel



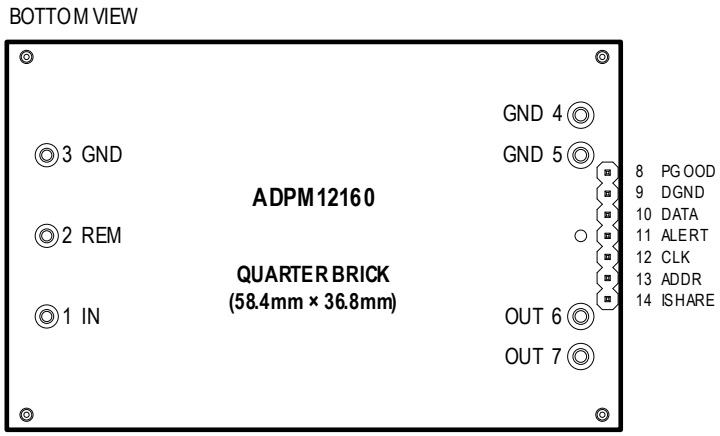
ACTIVE CURRENT SHARING
WITH 4 MODULES IN PARALLEL



THERMAL DERATING
(HEAT SINK: 57.5mm × 36mm × 25mm)



Pin Configurations



Pin Descriptions

PIN	NAME	FUNCTION
1	IN	Positive Input
2	REM	Remote ON/OFF Control. With active-high modules, pull it high or leave it open to enable the output of the module. Pull it low to disable the output. With active-low modules, pull it high or leave it open to disable the output of the module. Pull it low to enable the output.
3, 4, 5	GND	Power Ground
6, 7	OUT	Positive Output
8	PGOOD	Power-Good Output. Internally pulled up to 3.3V bias through a 10kΩ resistor with ADPM12160CMLZxx. Requires externally pulled up resistor with ADPM12160CMLZxxA.
9	DGND	Digital Ground. Internally connected to GND through a single point.
10	DATA	PMBus Data. Internally pulled up to 3.3V bias through a 10kΩ resistor with ADPM12160CMLZxx. Requires externally pulled up resistor with ADPM12160CMLZxxA.
11	ALERT	PMBus Alert. Internally pulled up to 3.3V bias through a 10kΩ resistor with ADPM12160CMLZxx. Requires externally pulled up resistor with ADPM12160CMLZxxA.
12	CLK	PMBus Clock. Internally pulled up to 3.3V bias through a 10kΩ resistor with ADPM12160CMLZxx. Requires externally pulled up resistor with ADPM12160CMLZxxA.
13	ADDR	PMBus Address Configuration. Connect a resistor from the ADDR pin to DGND to select the proper module address.
14	ISHARE	Active Current Sharing. For standalone operation, leave this pin open. For parallel operation, tie the ISHARE pin of each module together. Do not leave this pin open.

Applications Information

Test Configurations

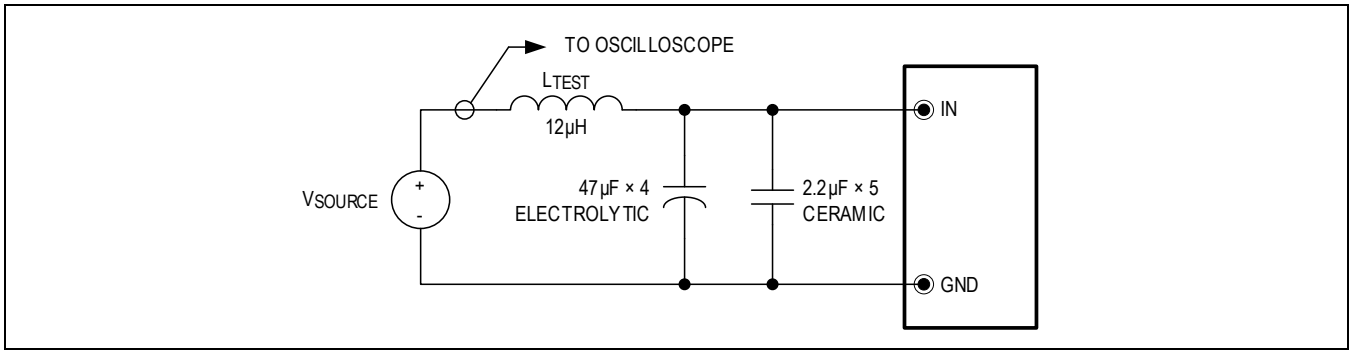


Figure 1. Input Reflected Ripple Current Test Setup

Note: Measure the input-reflected ripple current with a simulated source inductance of 12µH. The measurement points for the input-reflected ripple current are shown in *Figure 1*.

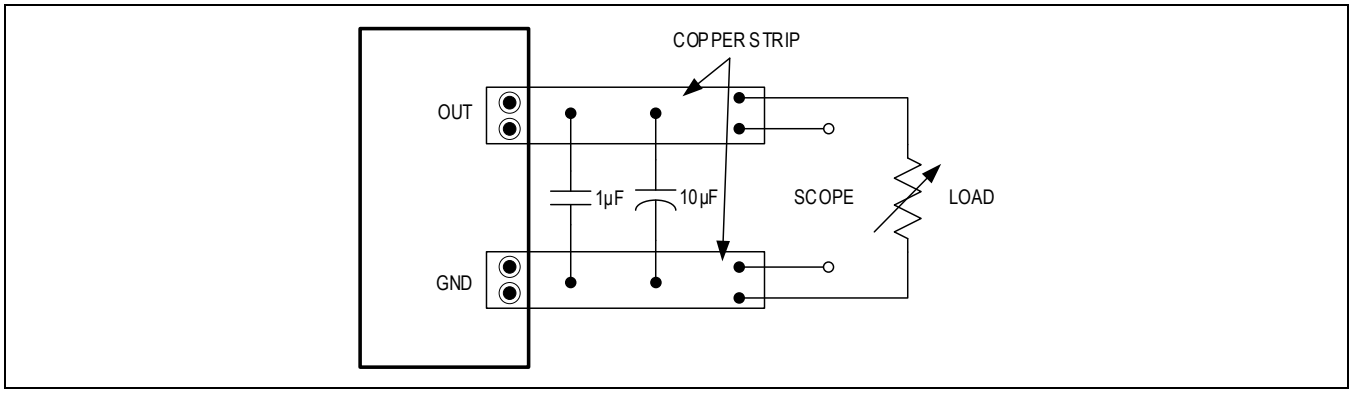


Figure 2. Output Ripple and Noise Test Setup

Note: Scope measurements should be made using a BNC socket with a 1µF ceramic capacitor and a 10µF tantalum capacitor. Position the oscilloscope probe between 51mm and 76mm (2in and 3in) from the module.

Input Filtering

The power module should be connected to a low AC-impedance input source. High inductive source impedances can affect the stability of the power module. For the test configuration in *Figure 1*, having four 47µF electrolytic capacitors and five 2.2µF ceramic capacitors in parallel mounted close to the power module helps ensure stability of the module.

Safety Considerations

For safety-agency approval of the system in which the power module is used, the power module must be installed in compliance with the spacing and separation requirements of the end-use safety agency standard (i.e., CAN/CSA-C22.2, and also in compliance with UL 62368-1, CAN/CSA C22.2 No. 62368-1-14, EN 62368-1, and IEC 62368-1.

Power-Good Output (PGOOD)

The ADPM12160CMLZxx module provides a PGOOD signal, which is internally pulled up to 3.3V, to indicate that the output voltage is within the normal output voltage range of the power module. The ADPM12160CMLZxxA module provides a power-good (PGOOD) signal, which is open-drain output, to indicate that the output voltage is within the normal output voltage range of the power module. PGOOD is pulled low if any fault condition such as overtemperature, overcurrent, or loss of regulation occurs that would result in the output voltage going outside the normal voltage range.

Remote ON/OFF Control (REM)

The REM pin is used to turn the power module ON or OFF through a system signal. Its logic is optional with different variants.

For the active-high module, pull the REM pin high or leave it open to enable the output; pull the REM pin low to disable its output.

For the active-low module, pull the REM pin high or leave it open to disable the output; pull the REM pin low to enable its output.

Output Current Protection

To provide protection in an output-overload fault condition, the module is equipped with internal current-protection circuitry. When the output current is above the overcurrent fault limit, the module shuts down immediately and enters into latched mode by default.

Output Voltage Protection

The output overvoltage protection consists of circuitry that monitors the voltage on the output terminals. When the output voltage is above the overvoltage fault limit, the module shuts down immediately, and enters into latched mode by default.

Overtemperature Protection

The overtemperature protection consists of circuitry that provides protection from thermal damage. When the temperature sensor detects a temperature above its OTP threshold, the module shuts down immediately and restarts after the temperature is within specification.

Parallel Operation ACS (Active Current Sharing, ISHARE)

Better current-sharing performance can be achieved with the ACS feature enabled. The advantages of the ACS as compared with normal dynamic load share (DLS) are that it utilizes a dedicate current share bus (ISHARE) to balance the load between the paralleled modules, and each module in the bus trims its regulated output up or down continuously in order to output the same current seen from the current share bus. The ACS feature cancels out the current-share error caused by the module's output voltage deviation, temperature deviation, and layout asymmetry.

By connecting the IN pins, OUT pins, and ISHARE pins of the parallel modules together, current sharing can be achieved automatically.

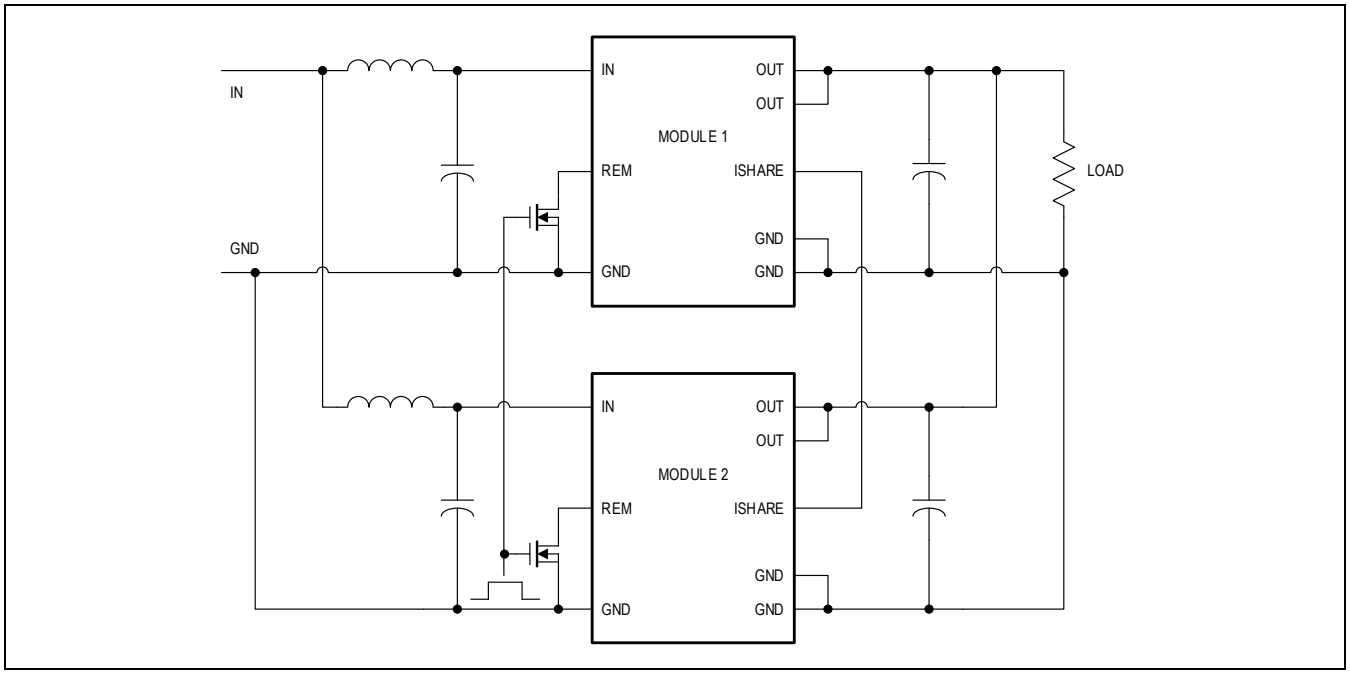


Figure 3. Active Current-Sharing Diagram with Two Modules

Use the following design rules for better accuracy and normal operation:

- The inputs of the modules must be connected to the same voltage source.
- When multiple modules are connected in parallel, ensure that the input loop and output loop of each module are as symmetrical as possible.

- The ISHARE of each parallel module must be connected with the shortest wires.
- The REM pin of the modules in parallel must be connected together.
- More than 1V/ms dv/dt of input voltage rise is helpful.
- The total output current share during startup must be less than 30A.
- The total current share of the parallel module must be less than 95% of the rated output current.

EMC Considerations

Figure 4 shows a suggested configuration to meet the conducted emission limits of EN55032 Class A.

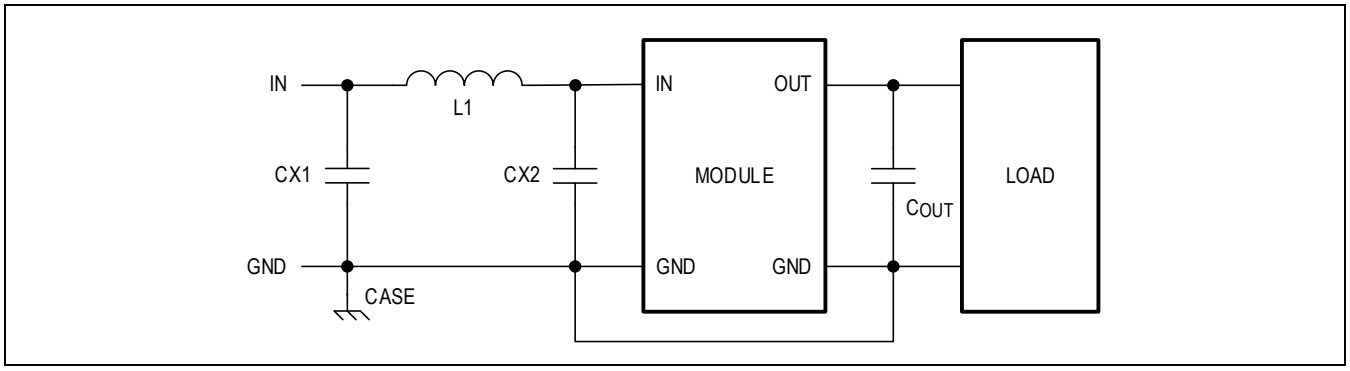


Figure 4. EMC Testing Typical Application Circuit

Table 1. Recommended Parameters for EMC Filter

COMPONENT	SPECIFICATIONS
CX1	47µF/100V ×2 (electrolytic capacitor) + 0.1µF ×3 (MLCC) + 2.2µF ×2 (MLCC)
CX2	47µF/100V ×4 (electrolytic capacitor)
C_{OUT}	1500µF
L1	0.22µH

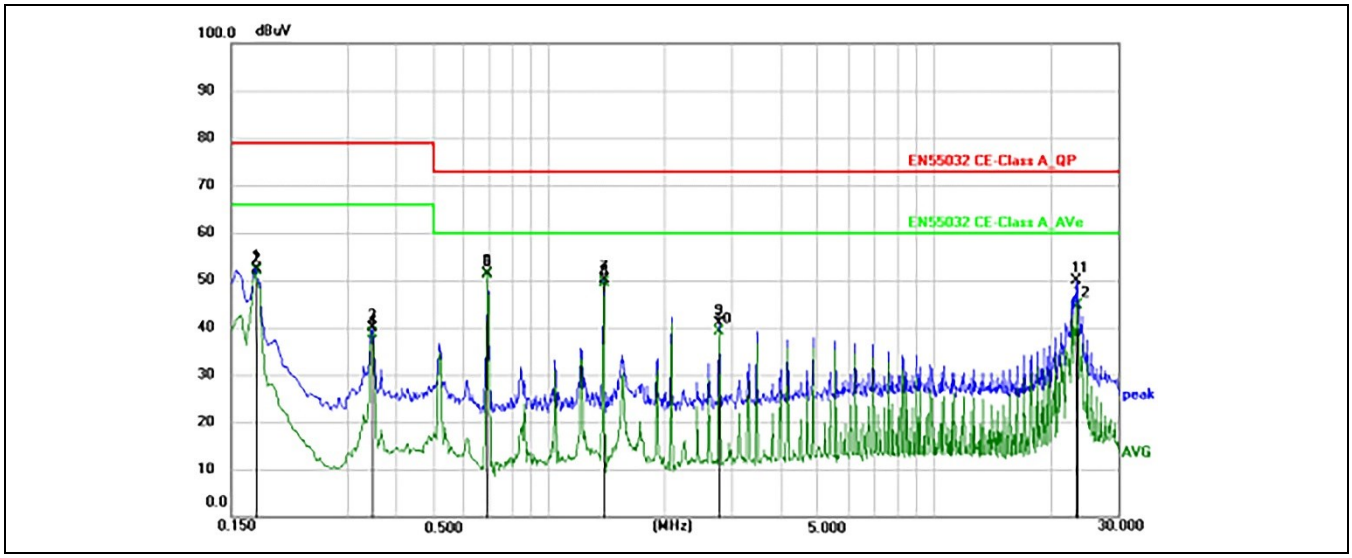


Figure 5. EMC Test Result (V_{IN} = 54V, V_{OUT} =12V, I_{OUT} = 133.3A)

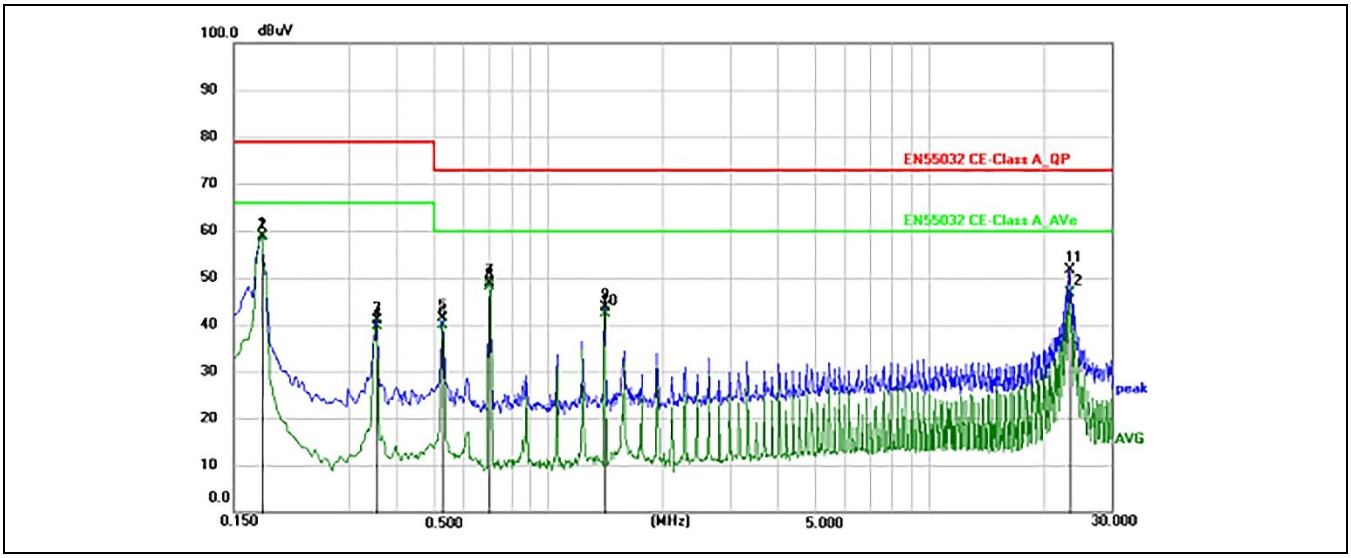
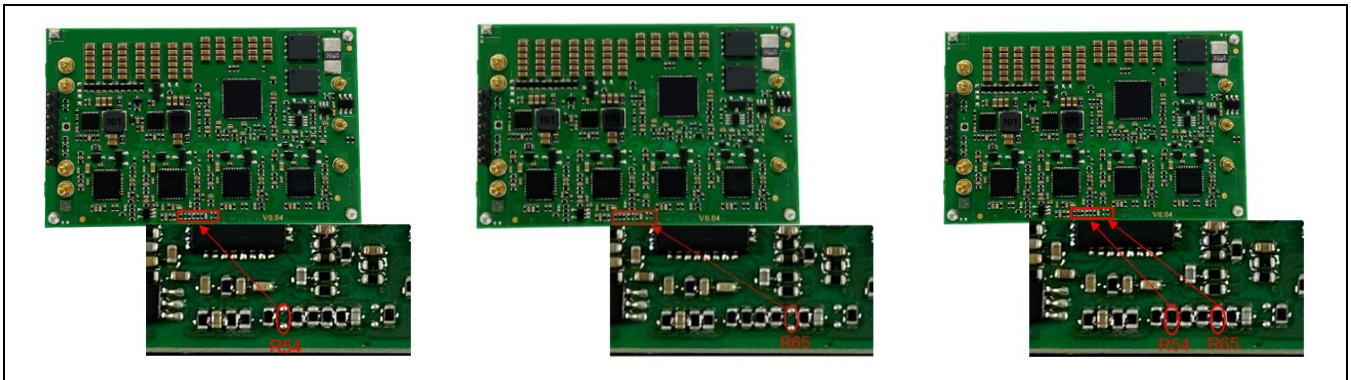


Figure 6. EMC Test Result (V_{IN} = 54V, V_{OUT} = 12.5V, I_{OUT} = 128.0A)

Appearance of the Output Voltage Calibration Resistor Position

During power module manufacturing, in order to ensure that the output voltage is within the range indicated in the specification, the output voltage must be calibrated by adjusting the resistors. Therefore, the power module may be configured in three ways as shown in *Figure 6*, all of which are typical qualified products, and the output voltage has been calibrated within the qualified range.



(a) R54 is not installed. *(b) R65 is not installed.* *(c) R54 and R65 are installed.*

Figure 7. Configuration of the Calibration Resistors

Digital Feature Descriptions

PMBus Interface Capability

The module is equipped with a digital PMBus interface to allow the module to be configured and communicate with system controllers.

The module supports a subset of the commands defined in the PMBus Power System Management Protocol Specification Part II – Command Language Revision 1.1. For detailed specifications and the complete list of PMBus commands, refer to Part II of the PMBus specification available at www.PMBus.org. The supported PMBus commands and the corresponding module behaviors are described in this document.

The module supports the group command where a host can write different data to multiple modules on the same serial bus with one long continuous data stream. All of the modules addressed during this transaction wait for the host to issue a STOP command before beginning to respond to the group command.

The module contains nonvolatile memory that is used for configuration setting and fault logging.

SMBALERT Interface Capability

The module also supports the SMBALERT response protocol. The SMBALERT response protocol is a mechanism through which the module can alert the host that it has an active status or alarm condition through pulling the ALERT pin low.

If the ALERT output is enabled (ALERT bit, bit[13] = 1 in MFR_MODE) when a fault occurs, the module pulls the ALERT pin low, and then waits for the host to send an Alert Response Address (ARA). When the ARA is received and the module is asserting ALERT, the module acknowledges (ACKs) it and then attempts to place its fixed target device address on the bus by arbitrating the bus, since another module could also try to respond to the ARA. The rules of arbitration state that the lowest address module wins. If the module wins the arbitration, it deasserts ALERT. If the module loses arbitration, it keeps ALERT asserted and waits for the host to once again send the ARA.

PMBus Addressing

The module has flexible addressing capability. Connect a resistor (E96 series, ±1%) between the ADDR pin and DGND pin to select the PMBus address.

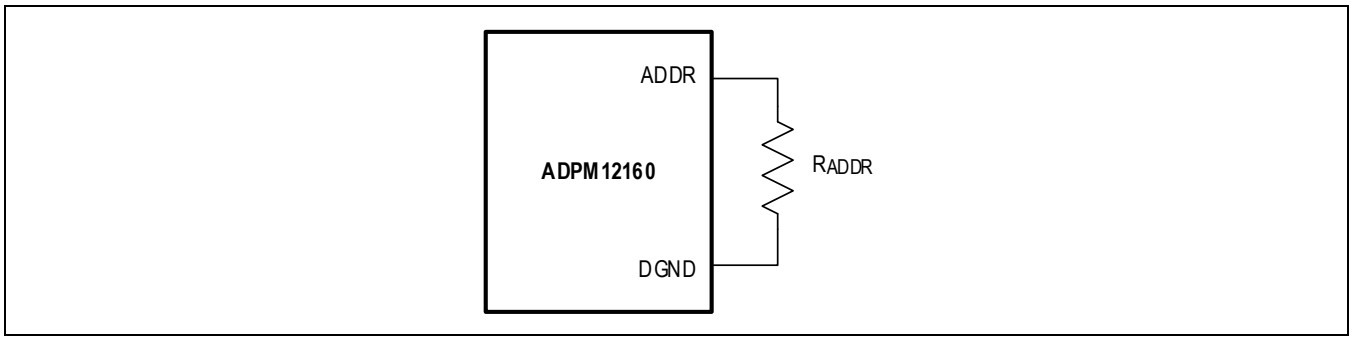


Figure 8. PMBus Address Select

Table 2. PMBus Address

R_{ADDR} (±1%)	7-BIT ADDRESS	R_{ADDR} (±1%)	7-BIT ADDRESS	R_{ADDR} (±1%)	7-BIT ADDRESS
10kΩ	96d (60h)	45.3kΩ	101d (65h)	130kΩ	106d (6Ah)
15kΩ	97d (61h)	56.2kΩ	102d (66h)	156kΩ	107d (6Bh)
21kΩ	98d (62h)	69.8kΩ	103d (67h)	191kΩ	108d (6Ch)
28kΩ	99d (63h)	88.7kΩ	104d (68h)	232kΩ	109d (6Dh)
35.7kΩ	100d (64h)	107kΩ	105d (69h)		

The module responds to receiving its fixed target device address by asserting an ACK on the bus. The module does not respond to a general call address; it only responds when it receives its fixed target device address or the alert response address.

PMBus Data Format

Voltage data for commanding or reading the output voltage or related parameters (such as the overvoltage threshold) are presented in DIRECT format. DIRECT format data is a 2-byte, two's complement binary value. DIRECT format data can be used with any command that sends or reads a parametric value. The DIRECT format uses an equation and defined coefficients to calculate the desired values. *Table 3* lists the coefficients used by the module.

Table 3. PMBus Command Code Coefficients

PARAMETER	COMMANDS	UNITS	RESOLUTION	MAXIMUM	m	b	R
Voltage	VOUT_MARGIN_HIGH VOUT_MARGIN_LOW VOUT_OV_FAULT_LIMIT VOUT_OV_WARN_LIMIT VOUT_UV_WARN_LIMIT VOUT_UV_FAULT_LIMIT POWER_GOOD_ON POWER_GOOD_OFF READ_VOUT MFR_VOUT_PEAK MFR_VOUT_MIN	mV	8	262136	0.125	0	0
Current	IOUT_OC_FAULT_LIMIT IOUT_OC_WARN_LIMIT READ_IOUT MFR_IOUT_PEAK MFR_IOUT_AVG	A	0.04	1310.68	0.25	0	2
Temperature	OT_FAULT_LIMIT OT_WARN_LIMIT READ_TEMPERATURE_1 READ_TEMPERATURE_PEAK	°C	0.01	327.67	1	0	2
Timing	TON_DELAY, TOFF_DELAY TON_MAX_FAULT_LIMIT MFR_FAULT_RETRY	ms	0.2	6553.4	5	0	0

Note: *To reliably process fault-retry during simultaneous fault events on multiple channels, it is recommended to set MFR_FAULT_RETRY ≥ 1s.*

Interpreting Received DIRECT Format Values

The host system uses the following equation to convert the value received from the module into a reading of volts, degrees Celsius, or other units as appropriate:

$$X = (1/m) \times (Y \times 10^{-R} - b)$$

where X is the calculated real-word value in the appropriate units (V, °C, or other units); m is the slope coefficient; Y is the 2-byte, two's complement integer received from the module; b is the offset; and R is the exponent.

Sending a DIRECT Format Value

To send a value, the host must use the following equation to solve for Y:

$$Y = (mX + b) \times 10^{R}$$

where Y is the 2-byte, two's complement integer to be sent to the module; m is the slope coefficient; X is the real-word value in units such as volts, to be converted for transmission; b is the offset; and R is the exponent.

Password Protection

The module can be password protected by using the LOCK bit in the MFR_MODE command. Once the module is locked, only certain PMBus commands can be accessed with the serial port. See *Table 4* for a complete list of PMBus commands. Commands that have password protection return all ones (FFh), with the proper number of data bytes, when read. When the module is locked, only the PAGE, OPERATION, CLEAR_FAULTS, and MFR_SERIAL commands can be written; all other written commands are ignored. When MFR_SERIAL is written and the upper 4 bytes match the internally flash-stored value, the module unlocks and remains unlocked until the LOCK bit in MFR_MODE is activated once again. The LOCK status bit in STATUS_MFR_SPECIFIC is always available to indicate whether the module is locked or unlocked.

SMBus Timeout

During an active SMBus communication sequence, if the CLK signal is held low for greater than the timeout duration (nominally 27ms), the module terminates the sequence and resets the serial bus. It takes no other action. No status bits are set.

PMBus Command

The supported PMBus commands are listed in *Table 4*.

Table 4. PMBus Command Codes

CODE	COMMAND NAME	TYPE	PAGE (Note 1)				NO. OF BYTES	FLASH STORED/ LOCKED (Note 2)	DEFAULT VALUE (Note 2)
			0-11	12-15	16-20	255			
00h	PAGE	R/W byte	R/W	R/W	R/W	R/W	1	N/N	00h
01h	OPERATION	R/W byte	R/W	—	—	W	1	N/N	00h
02h	ON_OFF_CONFIG	R/W byte	R/W	R/W	R/W	R/W	1	Y/Y	(Note 3)
03h	CLEAR_FAULTS	Send byte	W	W	W	W	0	N/N	—
10h	WRITE_PROTECT	R/W byte	R/W	R/W	R/W	R/W	1	N/Y	00h
11h	STORE_DEFAULT_ALL	Send byte	W	W	W	W	0	N/Y	—
12h	RESTORE_DEFAULT_ALL	Send byte	W	W	W	W	0	N/Y	—
19h	CAPABILITY	Read byte	R	R	R	R	1	N/N	20h
20h	VOUT_MODE	Read byte	R	R	R	R	1	FIXED/N	40h
25h	VOUT_MARGIN_HIGH	R/W word	R/W	—	—	—	2	Y/Y	0000h (Note 4)
26h	VOUT_MARGIN_LOW	R/W word	R/W	—	—	—	2	Y/Y	0000h (Note 4)
40h	VOUT_OV_FAULT_LIMIT	R/W word	R/W	R/W	—	—	2	Y/Y	See *Table 6*
42h	VOUT_OV_WARN_LIMIT	R/W word	R/W	R/W	—	—	2	Y/Y	See *Table 6*
43h	VOUT_UV_WARN_LIMIT	R/W word	R/W	R/W	—	—	2	Y/Y	See *Table 6*
44h	VOUT_UV_FAULT_LIMIT	R/W word	R/W	R/W	—	—	2	Y/Y	See *Table 6*
46h	IOUT_OC_FAULT_LIMIT	R/W word	R/W	R/W	—	—	2	Y/Y	See *Table 6*
4Ah	IOUT_OC_WARN_LIMIT	R/W word	R/W	R/W	—	—	2	Y/Y	See *Table 6*
4Fh	OT_FAULT_LIMIT	R/W word	—	—	R/W	—	2	Y/Y	2FA8h (Note 5)
51h	OT_WARN_LIMIT	R/W word	—	—	R/W	—	2	Y/Y	2AF8h (Note 5)
5Eh	POWER_GOOD_ON	R/W word	R/W	R/W	—	—	2	Y/Y	See *Table 6*
5Fh	POWER_GOOD_OFF	R/W word	R/W	R/W	—	—	2	Y/Y	See *Table 6*
60h	TON_DELAY	R/W word	R/W	—	—	—	2	Y/Y	See *Table 6*
62h	TON_MAX_FAULT_LIMIT	R/W word	R/W	—	—	—	2	Y/Y	01F4h (Note 4)
64h	TOFF_DELAY	R/W word	R/W	—	—	—	2	Y/Y	See *Table 6*
79h	STATUS_WORD	Read word	R	R	R	R	2	N/N	0000h
7Ah	STATUS_VOUT	Read byte	R	R	—	—	1	N/N	00h
7Bh	STATUS_IOUT	Read byte	R	R	—	—	1	N/N	00h
7Ch	STATUS_INPUT	Read byte	R	R	—	—	1	N/N	00h
7Dh	STATUS_TEMPERATURE	Read byte	—	—	R	—	1	N/N	00h
7Eh	STATUS_CML	Read byte	R	R	R	R	1	N/N	00h

CODE	COMMAND NAME	TYPE	PAGE (Note 1)				NO. OF BYTES	FLASH STORED/ LOCKED (Note 2)	DEFAULT VALUE (Note 2)
			0-11	12-15	16-20	255			
80h	STATUS_MFR_SPECIFIC	Read byte	R	—	—	R	1	N/N	00h
88h	READ_VIN	Read word	R	R	—	—	2	N/N	0000h
89h	READ_IIN	Read word	R	R	—	—	2	N/N	0000h
8Bh	READ_VOUT	Read word	R	R	—	—	2	N/N	0000h
8Ch	READ_IOUT	Read word	R	R	—	—	2	N/N	0000h
8Dh	READ_TEMPERATURE_1	Read word	—	—	R	—	2	N/N	0000h
98h	PMBUS_REVISION	Read byte	R	R	R	R	1	FIXED/N	11h
99h	MFR_ID	Read byte	R	R	R	R	1	FIXED/N	4Dh
9Ah	MFR_MODEL	Read byte	R	R	R	R	1	FIXED/N	59h
9Bh	MFR_REVISION	Read word	R	R	R	R	2	FIXED/N	3236h
9Ch	MFR_LOCATION	R/W 64	R/W	R/W	R/W	R/W	8	Y/Y	3130313031303130h (Note 7)
9Eh	MFR_SERIAL	R/W 64	R/W	R/W	R/W	R/W	8	Y/Y	—
D1h	MFR_MODE	R/W word	R/W	R/W	R/W	R/W	2	Y/Y	0022h
D4h	MFR_VOUT_PEAK	R/W word	R/W	R/W	—	—	2	N/Y	0000h
D5h	MFR_IOUT_PEAK	R/W word	R/W	R/W	—	—	2	N/Y	0000h
D6h	MFR_TEMPERATURE_PEAK	R/W word	—	—	R/W	—	2	N/Y	8000h
D7h	MFR_VOUT_MIN	R/W word	R/W	R/W	—	—	2	N/Y	7FFFh
D8h	MFR_NV_LOG_CONFIG	R/W word	R/W	R/W	R/W	R/W	2	Y/Y	0200h
D9h	MFR_FAULT_RESPONSE	R/W 32	R/W	R/W	—	—	4	Y/Y	See *Table 6*
DAh	MFR_FAULT_RETRY	R/W word	R/W	R/W	R/W	R/W	2	Y/Y	1388h
DCh	MFR_NV_FAULT_LOG	Read 32	R	R	R	R	255	Y/Y	(Note 6)
DDh	MFR_TIME_COUNT	R/W 32	R/W	R/W	R/W	R/W	4	N/Y	(Note 8)
DFh	MFR_MARGIN_CONFIG	R/W word	R/W	—	—	—	2	Y/Y	403Eh (Note 4)
E2h	MFR_IOUT_AVG	R/W word	R	R	—	—	2	N/Y	0000h
ECh	MFR_CONFIG_VERSION	R/W word	—	—	—	R/W	2	N/N	0000h
EEh	MFR_STORE_ALL	Write byte	W	W	W	W	1	N/Y	—
EFh	MFR_RESTORE_ALL	Write byte	W	W	W	W	1	N/Y	—
F2h	MFR_WP_CONTROL	R/W byte	R/W	R/W	R/W	R/W	1	N/N	00h
FCh	MFR_STORE_SINGLE	R/W word	R/W	R/W	R/W	R/W	2	N/Y	0000h
FEh	MFR_CRC	R/W word	R/W	R/W	R/W	R/W	2	N/Y	(Note 9)

Note 1: *Common commands are shaded; access through any page results in the same response.*

Note 2: *The value shown in the **Default Value** column is the value when shipped from the factory, which are automatically loaded upon power-on reset.*

*In the **Flash Stored/Locked** column, the "N" on the left indicates that this parameter is not stored in flash memory when the STORE_DEFAULT_ALL or MFR_STORE_ALL command is executed; The "Y" on the left indicates that the currently loaded value in this parameter is stored in flash memory when the STORE_DEFAULT_ALL or*

*MFR_STORE_ALL command is executed and is automatically loaded upon power-on reset; "FIXED" in the **Flash Stored** column means that the value is fixed at the factory and cannot be changed. The right-side Y/N indicates that when the module is locked, only the commands listed with "N" can be accessed. All other commands are ignored if written and return FFh if read. Only the PAGE, CLEAR_FAULTS, OPERATION, and MFR_SERIAL commands can be written to.*

The module unlocks if the upper 4 bytes of MFR_SERIAL match the data written to the module.

Note 3: *14h for REM active-low modules, 16h for REM active-high modules.*

Note 4: *When PAGE = 02h for output voltage configuration.*

Note 5: *When PAGE = 12h (18d) for temperature configuration.*

Note 6: *The factory-set default value for the complete block of the MFR_NV_FAULT_LOG is FFh.*

Note 7: *The factory-set default value for this 8-byte block is 3130313031303130h (ADPM12160CMLZCL).The register includes the information of output voltage/output power/REM logic/manufacturer location/software version. Please contact local technical support for the register value with different models.*

Note 8: *The factory-set default value for this 4-byte block is 00000040h.*

Note 9: *ADPM12160CMLZxx: 237Dh for REM active-low modules, D2C5h for REM active-high modules.*

ADPM12160CMLZxxA: 1812h for REM active-low modules, E95Bh for REM active-high modules.

PAGE (00h)

The ADPM12160 module monitors the input voltage, input current, output voltage, output current and the board temperature. All of the monitoring and control is accomplished using one PMBus address.

Send the PAGE command with data 2–10, 14, or 18 (decimal) to select which voltage or current or temperature is affected before processing associated PMBus commands. Not all commands are supported within each page. If an unsupported command is received, the CML status bit is set. Some commands are common, which means that any selected page has the same effect on and the same response from the module. See *Table 5* for PAGE commands.

Set the PAGE to 255 when the following PMBus commands should apply to all pages at the same time. There are only a few commands (OPERATION, CLEAR_FAULTS) where this function has a real application.

Table 5. PAGE (00h) Commands

PAGE	ASSOCIATED CONTROL
0, 1, 15	Internal used. Do NOT change any values in these pages.
2	Output voltage monitoring and control.
3	PGOOD output delay control.
4	Output current control.
5	Phase 1 current monitoring and control.
6	Phase 2 current monitoring and control.
7	Phase 3 current monitoring and control.
8	Phase 4 current monitoring and control.
9	Input voltage monitoring and control.
10	Input current monitoring and control.
11–13, 16, 17, 19, 20	Not used.
14	Accurate output current monitoring, READ_IOUT (8Ch) command only.
18	PCB board temperature monitoring and control.
21–254	Reserved.

PAGE	ASSOCIATED CONTROL
255	Applies to all pages.

Table 6. Default Values for Voltage/Current Setting

CODE	COMMAND NAME	DEFAULT VALUE WITHIN PAGE								
		2 (V_{OUT})	3 (PGOOD)	4 (I_{OUT})	5 ($I_{PH}1$)	6 ($I_{PH}2$)	7 ($I_{PH}3$)	8 ($I_{PH}4$)	9 (V_{IN})	10 (I_{IN})
40h	VOUT_OV_FAULT_LIMIT (ADPM12160CMLZxx)	0698h	—	—	—	—	—	—	203Ah	—
	VOUT_OV_FAULT_LIMIT (ADPM12160CMLZxxA)	06D6h	—	—	—	—	—	—	203Ah	—
42h	VOUT_OV_WARN_LIMIT (ADPM12160CMLZxx)	0659h	—	—	—	—	—	—	1FBDh	—
	VOUT_OV_WARN_LIMIT (ADPM12160CMLZxxA)	0698h	—	—	—	—	—	—	1FBDh	—
43h	VOUT_UV_WARN_LIMIT	0426h	—	—	—	—	—	—	128Eh	—
44h	VOUT_UV_FAULT_LIMIT	03E8h	—	—	—	—	—	—	11DFh	—
46h	IOUT_OC_FAULT_LIMIT	—	—	1AF4h	0A32h	0A32h	0A32h	0A32h	—	07B0h
4Ah	IOUT_OC_WARN_LIMIT	—	—	1AF4h	0A32h	0A32h	0A32h	0A32h	—	07B0h
5Eh	POWER_GOOD_ON (ADPM12160CMLZxx)	—	0546h	—	—	—	—	—	—	—
	POWER_GOOD_ON (ADPM12160CMLZxxA)	—	057Eh	—	—	—	—	—	—	—
5Fh	POWER_GOOD_OFF (ADPM12160CMLZxx)	—	0520h	—	—	—	—	—	—	—
	POWER_GOOD_OFF (ADPM12160CMLZxxA)	—	0559h	—	—	—	—	—	—	—
60h	TON_DELAY	0424h	0000h	—	—	—	—	—	—	—
64h	TOFF_DELAY	0000h	0000h	—	—	—	—	—	—	—
D9h	MFR_FAULT_RESPONSE	0101C 009h	—	0101C 001h	0101C 001h	0101C 001h	0101C 001h	0101C 001h	0101C 009h	0101C 082h

OPERATION (01h)

The OPERATION command is used to turn the module on and off in conjunction with the REM input pin. The OPERATION command is also used to cause the module to set the output voltage to the upper or lower margin voltages. The module stays in the commanded operating mode until a subsequent OPERATION command or a change in the state of the REM pin (if enabled) instructs the module to change to another state.

The valid OPERATION command byte values are shown in *Table 7*.

Table 7. OPERATION (01h) Command Byte

COMMAND BYTE	OUTPUT ON/OFF		OUTPUT MARGIN STATE (PAGE = 2)
	BIT 3 OF ON_OFF_CONFIG = 1	BIT 3 OF ON_OFF_CONFIG = 0	
00h	Immediate off	No effect	—
40h	Soft-off with delay		—
80h	On		Margin off
94h	On		Margin low (ignore all faults)

98h	On		Margin low (act on any fault)
A4h	On		Margin high (ignore all faults)
A8h	On		Margin high (act on any fault)

The OPERATION command controls how the module responds when commanded to change the output. When the command byte is 00h, the module immediately turns off and ignores any programmed turn-off delay. When the command byte is set to 40h, the output powers down according to the programmed turn-off delay.

In most cases, for power-on and power-off control, the OPERATION command should be sent when PAGE is set to 255.

For output-margining control, the OPERATION command can be used with the PAGE = 2. In *Table 7*, "act on any fault" means that if any warning or fault on the output is detected when the output is margined, the module treats this as a warning or fault and responds as programmed. "Ignore all faults" means that all warnings and faults on output are ignored. To begin the margining function, the output must exceed its POWER_GOOD_ON value.

ON_OFF_CONFIG (02h)

The ON_OFF_CONFIG command configures the combination of the REM input and PMBus OPERATION commands needed to turn the module on and off. This indicates how the module is commanded when power is applied. The ON_OFF_CONFIG message content is described in *Table 8*. The host should not modify ON_OFF_CONFIG while the output is active.

Table 8. ON_OFF_CONFIG (02h) Command Byte

BIT	PURPOSE	VALUE	MEANING
7:6	Reserved.	N/A	Always returns 00.
5	OPERATION command and REM pin and/or select.	0	OPERATION command is ANDed with REM pin if both are enabled.
		1	OPERATION command is ORed with REM pin if both are enabled.
4	Turn on the module when input is present or use the REM pin/OPERATION command.	0	Turns on the module when input is present, regardless of the REM pin.
		1	Uses the REM pin (if enabled) and/or OPERATION command (Note 1).
3	OPERATION command enable.	0	On/off portion of the OPERATION command disabled.
		1	OPERATION command enabled.
2	REM pin enable.	0	REM pin disabled.
		1	REM pin enabled.
1	REM pin polarity.	0	REM active low.
		1	REM active high.
0	REM pin turn-off action.	0	Uses the programmed turn-off delay (soft-off).
		1	Turns off the module immediately.

Note 1: *Unless bit 5 is set (if both bits 3:2 are set), both the REM pin and OPERATION command are required to turn the module on, and either can turn the module off.*

CLEAR_FAULTS (03h)

The CLEAR_FAULTS command is used to clear any latched fault or warning bits in the status registers that have been set and also unconditionally deasserts the ALERT output. This command clears all bits simultaneously. The CLEAR_FAULTS command does not cause a power supply that has latched off for a fault condition to restart. If a fault is still present after the CLEAR_FAULTS command is executed, the fault status bit is immediately set again, but ALERT is not reasserted. ALERT is only asserted again when a new fault or warning is detected that occurs after the CLEAR_FAULTS command is executed. This command is write-only. There is no data byte for this command.

WRITE_PROTECT (10h)

The WRITE_PROTECT command is used to provide protection against accidental changes to the module's operating memory. All supported commands can have their parameters read, regardless of the WRITE_PROTECT settings.

No fault or error is generated if the host attempts to write to a protected area.

The WRITE_PROTECT message content is described in *Table 9*.

Table 9. WRITE_PROTECT (10h) Command Byte

COMMAND BYTE	MEANING
80h	Disables all writes except the WRITE_PROTECT command.
40h	Disables all writes except the WRITE_PROTECT, OPERATION, and PAGE commands.
20h	Disables all writes except the WRITE_PROTECT, OPERATION, PAGE, and ON_OFF_CONFIG commands.
00h	Enables writes for all commands (default).

Configuration Data Management

The module stores configuration data in both nonvolatile flash memory and volatile RAM. The PMBus engine manages the module configuration data. See *Figure 8*.

The flash memory has three separate arrays for configuration parameters, whereas the RAM only has a single array. When a PMBus command is written to the module, it is always written to the RAM. When the module is shipped from the factory, the MAIN and BACKUP flash memory arrays are identical and are configured as shown in *Table 4* and *Table 6*. The SINGLE array is empty.

There is a set of five PMBus commands that can be used to transfer data between the flash and RAM arrays. These commands are described in *Table 10*.

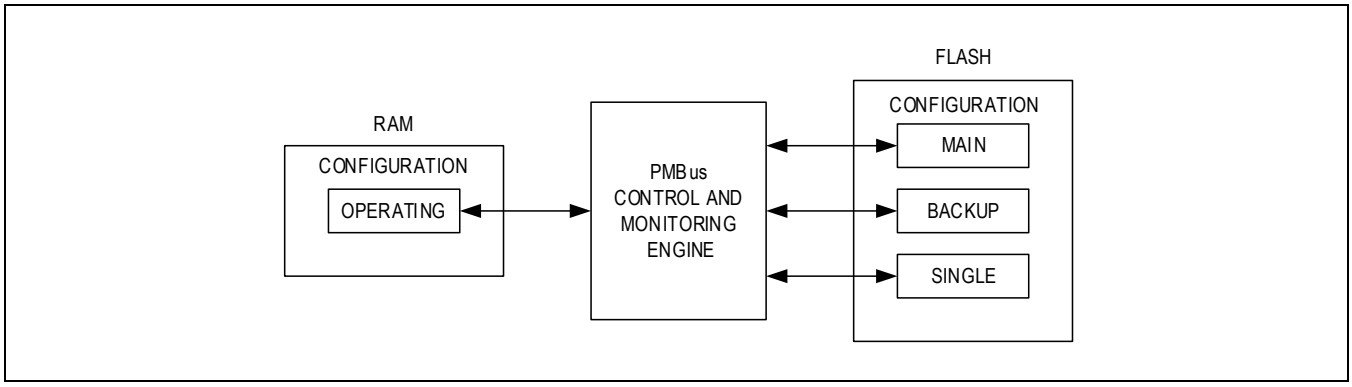


Figure 9. Configuration Data Management

Table 10. Memory Transfer PMBus Commands

PMBus COMMAND		RESULTING MEMORY TRANSFER
STORE_DEFAULT_ALL		Copies RAM OPERATING to the flash MAIN.
RESTORE_DEFAULT_ALL		Copies the flash MAIN to RAM OPERATING.
MFR_STORE_ALL	CODE = 00h	Copies RAM OPERATING to the flash MAIN.
	CODE = 01h	Copies RAM OPERATING to the flash BACKUP.
MFR_RESTORE_ALL	CODE = 00h	Copies the flash MAIN to RAM OPERATING.
	CODE = 01h	Copies the flash BACKUP to RAM OPERATING.
MFR_STORE_SINGLE		Copies RAM OPERATING (single parameter) to the flash SINGLE.

STORE_DEFAULT_ALL (11h)

The STORE_DEFAULT_ALL command instructs the module to copy RAM OPERATING to the flash MAIN memory. Not all of the information is stored. Only configuration data is stored, not any status or operational data. If an error occurs

during the transfer, ALERT asserts if enabled and the CML bit in STATUS_WORD is set to 1. No bits are set in STATUS_CML. This command is write-only. There is no data byte for this command.

When the STORE_DEFAULT_ALL command is invoked, the module is unresponsive to PMBus commands and does not monitor power supplies while transferring the configuration. The time required to complete this task is 80ms (typ). The MFR_STORE_SINGLE command allows a single command to be stored in much less time, 310µs.

RESTORE_DEFAULT_ALL (12h)

The RESTORE_DEFAULT_ALL command instructs the module to copy the flash MAIN memory to RAM OPERATING. The RESTORE_DEFAULT_ALL command should only be executed when the module is not operating. This command is write-only. There is no data byte for this command. When RESTORE_DEFAULT_ALL is issued, the data is checked for validity before being transferred. If the MAIN array is corrupt, the module sets bit 1 of STATUS_CML and loads the BACKUP copy. If the BACKUP copy is corrupt, then the module sets bit 2 of STATUS_CML and remains in a disabled state. To resolve the data corruption, the configuration data must be written to RAM OPERATING and STORE_DEFAULT_ALL must be issued, followed by a power reset.

Upon a module power-on reset, this command is automatically executed by the module without PMBus action required.

MFR_STORE_ALL (EEh)

The MFR_STORE_ALL command instructs the module to copy RAM OPERATING to either the flash MAIN memory array (CODE = 00h) or the flash BACKUP memory array (CODE = 01h). This command is write-only. There is 1 data byte for this command, which is the CODE. The CODE is either 00h to instruct the module to copy into the MAIN array, or 01h to copy into the BACKUP array. All other CODE values are ignored. Not all information is stored. Only configuration data is stored, not any status or operational data. If an error occurs during the transfer, ALERT asserts if enabled and the CML bit in STATUS_WORD is set to 1. No bits are set in STATUS_CML. Note that if the CODE is 00h, then this command operates the same as STORE_DEFAULT_ALL.

When the MFR_STORE_ALL command is invoked, the module is unresponsive to PMBus commands and does not monitor power supplies while transferring the configuration. The time required to complete this task is 80ms.

MFR_RESTORE_ALL (EFh)

The MFR_RESTORE_ALL command instructs the module to copy either the flash MAIN memory array (CODE = 00h) or the flash BACKUP memory array (CODE = 01h) to RAM OPERATING. This command is write-only. There is 1 data byte for this command, which is the CODE. The CODE is either 00h to instruct the module to copy from the MAIN array or 01h to copy from the BACKUP array. All other CODE values are ignored. Note that if the CODE is 00h, then this command operates the same as RESTORE_DEFAULT_ALL.

The MFR_RESTORE_ALL command should only be executed when the module is not operating. When MFR_RESTORE_ALL is issued, the data is checked for validity before being transferred. If the MAIN array is corrupt, the module sets bit 1 of STATUS_CML. If the BACKUP array is corrupt, then the module sets bit 2 of STATUS_CML. No other action is taken. To resolve the data corruption, the configuration data must be written to RAM OPERATING and STORE_DEFAULT_ALL or MFR_STORE_ALL must be issued.

MFR_STORE_SINGLE (FCh)

MFR_STORE_SINGLE is a read/write word command that instructs the module to transfer a single configuration parameter from RAM OPERATING to the flash SINGLE memory array. The MFR_STORE_SINGLE command allows a single command to be stored in 310µs.

The upper byte contains the PAGE and the lower byte contains the PMBus command that should be stored. When read, this command reports the last single PAGE/command written to flash. This command can be used while the module is operating. If an error occurs during the transfer, ALERT asserts if enabled and the CML bit in STATUS_WORD is set to 1. No bits are set in STATUS_CML. The MFR_STORE_SINGLE command should only be invoked a maximum of 85 times before a power cycle occurs, or the RESTORE_DEFAULT_ALL command is invoked. Once the MFR_STORE_SINGLE command is invoked, the STORE_DEFAULT_ALL and MFR_STORE_ALL commands should not be used until a power cycle occurs, or the RESTORE_DEFAULT_ALL command is invoked. Also, MFR_STORE_SINGLE should not be used for commands that are not stored in flash. See *Table 4* for a list of commands that are stored in flash.

MFR_CRC (FEh)

MFR_CRC is a read/write word command that instructs the module to report the calculated 16-bit CRC value of either the RAM OPERATING or the flash MAIN or BACKUP memory arrays. A CRC value for the flash SINGLE array is not available. Only one 16-bit CRC is reported with each read of MFR_CRC. The CRC value to be reported is determined by the most previous written CODE value, as shown in *Table 11*. For example, if MFR_CRC is first written with a CODE of 0001h, then the next read of MFR_CRC reports the CRC for the flash BACKUP array. If no CODE value is written, MFR_CRC returns FFFFh when read. See *Table 11*.

Table 11. MFR_CRC (FEh) Command Byte

MFR_CRC CODE VALUE	MEMORY ARRAY CRC VALUE TO BE REPORTED ON NEXT READ OF MFR_CRC
0000h	Flash MAIN
0001h	Flash BACKUP
0002h	RAM OPERATING

Upon reset, the module runs an internal algorithm to check the integrity of the key nonvolatile memory. If the CRC check fails, the module does not power up.

CAPABILITY (19h)

The CAPABILITY command is used to determine some key capabilities of the module. The CAPABILITY command is read-only. The message content is described in *Table 12*.

Table 12. CAPABILITY (19h) Command Byte

BIT	NAME	MEANING
7	Packet-error checking	0 = PEC not supported.
6:5	PMBus speed	01 = Maximum supported bus speed is 400kHz.
4	ALERT	1 = Supports an ALERT output (ALERT is enabled in MFR_MODE). 0 = Does not support an ALERT output (ALERT is disabled in MFR_MODE).
3:0	Reserved	Always returns 0000.

VOUT_MODE (20h)

The VOUT_MODE command is used to report the data format of the module. The module uses the DIRECT format for all of the voltage-related commands. The value returned is 40h, indicating the DIRECT data format. This command is read-only. If a host attempts to write this command, the CML status bit is asserted. See *Table 3* for the m, b, and R values for the various commands.

VOUT_MARGIN_HIGH (25h)

The VOUT_MARGIN_HIGH command sets the voltage to the target margin high voltage when the OPERATION command is set to margin high. If the module is already operating at margin high, changing VOUT_MARGIN_HIGH has no effect on the output voltage. The module only adjusts the output to the new VOUT_MARGIN_HIGH voltage after receiving a new margin-high OPERATION command. The 2 data bytes are in DIRECT format. If the module cannot successfully close-loop margin the output, the module keeps attempting to margin the voltage and does the following:

1) Sets the MARGIN bit in STATUS_WORD.
2) Sets the MARGIN_FAULT bit in STATUS_MFR_SPECIFIC (PAGE 2).
3) Notifies the host through ALERT assertion (if enabled in MFR_MODE).

VOUT_MARGIN_LOW (26h)

The VOUT_MARGIN_LOW command sets the voltage to the target margin low voltage when the OPERATION command is set to margin low. If the module is already operating at margin low, changing VOUT_MARGIN_LOW has no effect on the output voltage. The module only adjusts the output to the new VOUT_MARGIN_LOW voltage after receiving a new margin-low OPERATION command. The 2 data bytes are in DIRECT format. If the module cannot successfully close-loop margin the output, the module keeps attempting to margin the supply and does the following:

1) Sets the MARGIN bit in STATUS_WORD.
2) Sets the MARGIN_FAULT bit in STATUS_MFR_SPECIFIC (PAGE 2).
3) Notifies the host through the ALERT assertion (if enabled in MFR_MODE).

VOUT_OV_FAULT_LIMIT (40h)

The VOUT_OV_FAULT_LIMIT command sets the value of the voltage that causes an overvoltage fault. The monitored voltage must drop by at least 2% below the limit before the fault is allowed to clear. The 2 data bytes are in DIRECT format. In response to the VOUT_OV_FAULT_LIMIT being exceeded, the module does the following:

1) Sets the VOUT_OV bit and the VOUT bit in STATUS_WORD.
2) Sets the VOUT_OV_FAULT bit in STATUS_VOUT.
3) Responds as specified in the MFR_FAULT_RESPONSE.
4) Notifies the host through the ALERT assertion (if enabled in MFR_MODE).

When PAGE = 2, the VOUT_OV_FAULT_LIMIT command sets the OV threshold of the output voltage. Its maximum threshold is clamped to 14.5V by the hardware circuit; the VOUT_OV_FAULT_LIMIT should then be set lower than 14.5V to ensure that the command works properly.

When PAGE = 9, the VOUT_OV_FAULT_LIMIT command sets the OV threshold of the input voltage.

VOUT_OV_WARN_LIMIT (42h)

The VOUT_OV_WARN_LIMIT command sets the value of the voltage that causes a voltage high warning. The monitored voltage must drop by at least 2% below the limit before the warning is allowed to clear. This value is typically less than the overvoltage threshold in VOUT_OV_FAULT_LIMIT. The 2 data bytes are in DIRECT format. In response to the VOUT_OV_WARN_LIMIT being exceeded, the module does the following:

1) Sets the VOUT bit in STATUS_WORD.
2) Sets the VOUT_OV_WARN bit in STATUS_VOUT.
3) Notifies the host using the ALERT assertion (if enabled in MFR_MODE).

VOUT_UV_WARN_LIMIT (43h)

The VOUT_UV_WARN_LIMIT command sets the value of the voltage that causes a voltage low warning. The monitored voltage must increase by at least 2% above the limit before the warning is allowed to clear. This value is typically greater than the undervoltage-fault threshold in VOUT_UV_FAULT_LIMIT. This warning is masked until the voltage reaches the programmed POWER_GOOD_ON for the first time and during turn-off when the power supply is disabled. VOUT_UV_WARN_LIMIT should be set to a value greater than 100mV. The 2 data bytes are in DIRECT format. In response to violation of the VOUT_UV_WARN_LIMIT, the module does the following:

1) Sets the VOUT bit in STATUS_WORD.
2) Sets the VOUT_UV_WARN bit in STATUS_VOUT.
3) Notifies the host using the ALERT assertion (if enabled in MFR_MODE).

VOUT_UV_FAULT_LIMIT (44h)

The VOUT_UV_FAULT_LIMIT command sets the value of the voltage that causes an undervoltage fault. The monitored voltage must increase by at least 2% above the limit before the fault is allowed to clear. This fault is masked until the voltage reaches the programmed POWER_GOOD_ON for the first time and during turn-off when the power supply is disabled. VOUT_UV_FAULT_LIMIT should be set to a value greater than 100mV. The 2 data bytes are in DIRECT format. In response to violation of the VOUT_UV_FAULT_LIMIT, the module does the following:

1) Sets the VOUT bit in STATUS_WORD.
2) Sets the VOUT_UV_FAULT bit in STATUS_VOUT.
3) Responds as specified in MFR_FAULT_RESPONSE.
4) Notifies the host using the ALERT assertion (if enabled in MFR_MODE).

The minimum input voltage UV rising threshold is set to 38.4V (typ) by hardware circuit; the value of VOUT_UV_FAULT_LIMIT (when PAGE = 9) should then be set higher than it to ensure the command works properly.

IOUT_OC_FAULT_LIMIT (46h)

The IOUT_OC_FAULT_LIMIT command sets the value of the current that causes an overcurrent fault. The monitored current must decrease by at least 5% below the limit before the fault is allowed to clear. This fault is masked until the current is below this limit for the first time. The 2 data bytes are in DIRECT format. In response to violation of the IOUT_OC_FAULT_LIMIT, the module does the following:

1) Sets the IOUT bit in STATUS_WORD.
2) Sets the IOUT_OC_FAULT bit in STATUS_IOUT.
3) Responds as specified in the MFR_FAULT_RESPONSE.
4) Notifies the host using the ALERT assertion (if enabled in MFR_MODE).

IOUT_OC_WARN_LIMIT (4Ah)

The IOUT_OC_WARN_LIMIT command sets the value of the current that causes an overcurrent warning. The monitored current must decrease by at least 5% below the limit before the warning is allowed to clear. This value is typically less than the overcurrent-fault threshold in IOUT_OC_FAULT_LIMIT. The 2 data bytes are in DIRECT format. In response to violation of the IOUT_OC_WARN_LIMIT, the module does the following:

1) Sets the IOUT bit in STATUS_WORD.
2) Sets the IOUT_OC_WARN bit in STATUS_IOUT.
3) Notifies the host using the ALERT assertion (if enabled in MFR_MODE).

OT_FAULT_LIMIT (4Fh)

The OT_FAULT_LIMIT command sets the temperature, in degrees Celsius, at which an overtemperature fault is detected. The temperature must drop by at least 4°C below the limit before the fault is allowed to clear. The 2 data bytes are in DIRECT format. In response to the OT_FAULT_LIMIT being exceeded, the module does the following:

1) Sets the TEMPERATURE bit in STATUS_WORD.
2) Sets the OT_FAULT bit in STATUS_TEMPERATURE register.
3) Responds as specified in the MFR_FAULT_RESPONSE.
4) Notifies the host using the ALERT assertion (if enabled in MFR_MODE).

OT_WARN_LIMIT (51h)

The OT_WARN_LIMIT command sets the temperature, in degrees Celsius, at which an overtemperature warning is detected. The temperature must drop by at least 4°C below the limit before the warning is allowed to clear. The 2 data bytes are in DIRECT format. In response to the OT_WARN_LIMIT being exceeded, the module does the following:

1) Sets the TEMPERATURE bit in STATUS_WORD.
2) Sets the OT_WARN bit in STATUS_TEMPERATURE register.
3) Notifies the host using the ALERT assertion (if enabled in MFR_MODE).

POWER_GOOD_ON (5Eh)

The POWER_GOOD_ON command sets the value of the output voltage that it must exceed to assert the PGOOD pin. The POWER_GOOD_ON threshold is also used to determine if TON_MAX_FAULT_LIMIT is exceeded. The POWER_GOOD_ON level should always be set higher than the POWER_GOOD_OFF level. The 2 data bytes are in DIRECT format.

POWER_GOOD_ON should be set higher than VOUT_UV_FAULT_LIMIT and VOUT_UV_WARN_LIMIT because their functionality does not become active until the output voltage rises above the POWER_GOOD_ON threshold.

POWER_GOOD_OFF (5Fh)

The POWER_GOOD_OFF command sets the value of the output voltage that causes the PGOOD pin to deassert after it has been asserted. The POWER_GOOD_OFF level should always be set lower than the POWER_GOOD_ON level. The 2 data bytes are in DIRECT format.

When the V_{OUT} voltage falls from greater than the POWER_GOOD_ON value to less than the POWER_GOOD_OFF value, the module does the following:

1) Deassert the PGOOD pin.
2) Sets the POWER_GOOD# bit in STATUS_WORD.
3) Sets the POWER_GOOD# bit in STATUS_MFR_SPECIFIC register (PAGE 2).

Note: If the POWER_GOOD_ON value is configured to be lower than the POWER_GOOD_OFF value, the module sets the POWER_GOOD_OFF value to be equal to the POWER_GOOD_ON value. Conversely, if the POWER_GOOD_OFF value is configured to be higher than the POWER_GOOD_ON value, the module sets the POWER_GOOD_ON value to be equal to the POWER_GOOD_OFF value.

TON_DELAY (60h)

When PAGE = 2, the TON_DELAY sets the time, in milliseconds, from the REM assertion to the beginning of V_{OUT} rising. Considering the required initialization time for internal circuits, DO NOT set TON_DELAY less than 215ms when the module works in standalone mode. When in parallel operation to support high power output, DO NOT change this TON_DELAY value to ensure all modules start up simultaneously.

When PAGE = 3, the TON_DELAY sets the delay time before PGOOD pin is asserted.

The 2 data bytes are in DIRECT format.

TOFF_DELAY (64h)

When PAGE = 2, the TOFF_DELAY sets the time, in milliseconds, before V_{OUT} drops when REM is deasserted. Considering the internal holdup time of the bias circuits, TOFF_DELAY should be set less than 1ms. The TOFF_DELAY value is ignored if the OPERATION commands to turn off immediately.

When PAGE = 3, the TOFF_DELAY sets the delay time before PGOOD pin is deasserted.

The 2 data bytes are in DIRECT format.

TON_MAX_FAULT_LIMIT (62h)

The TON_MAX_FAULT_LIMIT sets an upper time limit, in milliseconds, from when V_{OUT} starts rising until it crosses the POWER_GOOD_ON threshold. The 2 data bytes are in DIRECT format. If the value is zero, then the limit is disabled. In response to the TON_MAX_FAULT_LIMIT being exceeded, the module does the following:

1) Sets the VOUT bit in STATUS_WORD.
2) Sets the TON_MAX_FAULT bit in STATUS_VOUT.
3) Responds as specified in MFR_FAULT_RESPONSE.
4) Notifies the host using the ALERT assertion (if enabled in MFR_MODE).

STATUS_WORD (79h)

The STATUS_WORD command returns 2 bytes of information with a summary of the reason for a fault.

Table 13. STATUS_WORD (79h)

BIT	NAME	MEANING
15	VOUT	A voltage fault or warning, or TON_MAX_FAULT_LIMIT has occurred.
14	IOUT	An overcurrent fault or warning has occurred.
13	0	Always returns 0.
12	MFR	A bit in STATUS_MFR_SPECIFIC (PAGE = 255) has been set.
11	POWER_GOOD#	Voltage has fallen from POWER_GOOD_ON to less than POWER_GOOD_OFF (logical OR of all the POWER_GOOD# bits in STATUS_MFR_SPECIFIC).
10:9	0	Always returns 00.
8	MARGIN	A margining fault has occurred.
7	0	Always returns 0.
6	SYS_OFF	Set when output is off (logical OR of all the OFF bits in STATUS_MFR_SPECIFIC).
5	VOUT_OV	An overvoltage fault has occurred.
4	IOUT_OC	An overcurrent fault has occurred.
3	0	Always returns 0.
2	TEMPERATURE	A temperature fault or warning has occurred.
1	CML	A communication, memory, or logic fault has occurred.
0	0	Always returns 0.

Note: *The setting of the SYS_OFF and POWER_GOOD# bits do not assert the ALERT signal.*

STATUS_VOUT (7Ah)

The STATUS_VOUT command returns 1 byte of information with contents, as described in *Table 14*. All of the bits in STATUS_VOUT are latched. When cleared, the bits are set again if the condition persists, or in the case of TON_MAX_FAULT, when the event occurs again.

Table 14. STATUS_VOUT (7Ah)

BIT	NAME	MEANING	LATCHED
7	VOUT_OV_FAULT	V_{OUT} overvoltage fault.	Yes
6	VOUT_OV_WARN	V_{OUT} overvoltage warning.	Yes
5	VOUT_UV_WARN	V_{OUT} undervoltage warning.	Yes
4	VOUT_UV_FAULT	V_{OUT} undervoltage fault.	Yes
3	0	Always returns 0.	—
2	TON_MAX_FAULT	TON_MAX_FAULT_LIMIT fault.	Yes
1:0	0	Always returns 00.	—

STATUS_IOUT (7Bh)

The STATUS_IOUT command returns 1 byte of information with contents, as described in *Table 15*. All the bits in STATUS_IOUT are latched. When cleared, the bits are set again if the condition persists.

Table 15. STATUS_IOUT (7Bh)

BIT	NAME	MEANING	LATCHED
7	IOUT_OC_FAULT	I_{OUT} overcurrent fault.	Yes
6	0	Always returns 0.	—
5	IOUT_OC_WARN	I_{OUT} overcurrent warning.	Yes
4:0	0	Always returns 00000.	—

STATUS_INPUT (7Ch)

The STATUS_INPUT command returns 1 byte of information with contents, as described in *Table 16*. All of the bits, except bit 3 in STATUS_INPUT, are latched. When cleared, the bits are set again if the condition persists.

Table 16. STATUS_INPUT (7Ch)

BIT	NAME	MEANING	LATCHED
7	VIN_OV_FAULT	V_{IN} overvoltage fault.	Yes
6	VIN_OV_WARN	V_{IN} overvoltage warning.	Yes
5	VIN_UV_WARN	V_{IN} undervoltage warning.	Yes
4	VIN_UV_FAULT	V_{IN} undervoltage fault.	Yes
3	UNIT_OFF	Module is off for insufficient input voltage*.	No
2	IIN_OC_FAULT	I_{IN} overcurrent fault.	Yes
1	IIN_OV_WARN	I_{IN} overcurrent warning.	Yes
0	0	Always returns 0.	—

**Either the input voltage has never exceeded the input turn-on threshold or, if the module did start, the input voltage decreased below the turn-off threshold.*

STATUS_TEMPERATURE (7Dh)

The STATUS_TEMPERATURE command returns 1 byte of information with contents, as described in *Table 17*. All of the bits in STATUS_VOUT are latched. When cleared, the bits are set again if the condition persists.

Table 17. STATUS_TEMPERATURE (7Dh)

BIT	NAME	MEANING	LATCHED
7	OT_FAULT	Overtemperature fault.	Yes
6	OT_WARN	Overtemperature warning.	Yes
5:0	0	Always returns 000000.	—

STATUS_CML (7Eh)

The STATUS_CML command returns 1 byte of information with contents, as described in *Table 18*. The COMM_FAULT, DATA_FAULT, MAIN_FAULT, and BACKUP_FAULT bits are latched. When cleared, the bits are set again when the event occurs again. The FAULT_LOG_FULL bit reflects the current real-time state of the fault log.

Table 18. STATUS_CML (7Eh)

BIT	NAME	MEANING	LATCHED
7	COMM_FAULT	An invalid or unsupported command has been received.	Yes
6	DATA_WARN	An invalid or unsupported data has been received.	Yes
5:3	0	Always returns 000.	—
2	BACKUP_FAULT	Flash BACKUP memory array is corrupt.	Yes
1	MAIN_FAULT	Flash MAIN memory array is corrupt.	Yes
0	FAULT_LOG_FULL	MFR_NV_FAULT_LOG is full and needs to be cleared.	No

Note: *When the NV fault log overwrite is enabled (NV_LOG_OVERWRITE = 1 in MFR_MODE), FAULT_LOG_FULL is set when the fault log is full, but clears when the fault log is overwritten since two fault logs are cleared before each overwrite; setting of the BACKUP_FAULT and MAIN_FAULT bits does not assert the ALERT signal.*

STATUS_MFR_SPECIFIC (80h)

The STATUS_MFR_SPECIFIC message content varies based on the select PAGE and is described in *Table 19* and *Table 20*.

Table 19. STATUS_MFR_SPECIFIC (80h) (for PAGES 0–11)

BIT	NAME	MEANING	LATCHED
7	—	Internal used.	No
6:4	0	Always returns 000.	—
3	MARGIN_FAULT	This bit is set if the module cannot properly close-loop margin the voltage.	Yes
2	POWER_GOOD#	This bit is set when the voltage has fallen from POWER_GOOD_ON to less than POWER_GOOD_OFF. On module reset, this bit is set until the voltage is greater than POWER_GOOD_ON.	No
1:0	0	Always returns 00.	—

Table 20. STATUS_MFR_SPECIFIC (80h) (for PAGE 255)

BIT	NAME	MEANING	LATCHED
7	LOCK	Set when the module is password protected. Setting this bit does not assert the ALERT signal.	No
6:4	—	Internal used.	Yes
3	REM	Set each time the REM input is deasserted. (ON_OFF_CONFIG must be configured to use the REM pin for this status bit to function.)	Yes
2:0	0	Always returns 000.	—

READ_VIN (88h)

The READ_VIN command returns the actual measured input voltage when PAGE = 9.

READ_VIN is measured and updated every 5ms. The 2 data bytes are in DIRECT format.

READ_IIN (89h)

The READ_IIN command returns the latest measured input current when PAGE = 10.

READ_IIN is measured and updated every 5ms. The 2 data bytes are in DIRECT format.

READ_VOUT (8Bh)

The READ_VOUT command returns the actual measured output voltage when PAGE = 2.

READ_VOUT is measured and updated every 5ms. The 2 data bytes are in DIRECT format.

READ_IOUT (8Ch)

The READ_IOUT command returns the latest output current when PAGE = 14 and the latest measured phase current when PAGE = 5, 6, 7, or 8.

READ_IOUT is measured and updated every 5ms. The 2 data bytes are in DIRECT format.

READ_TEMPERATURE_1 (8Dh)

The READ_TEMPERATURE_1 command returns the measured PCB board temperature when PAGE = 18.

READ_TEMPERATURE_1 is measured and updated every one second. The 2 data bytes are in DIRECT format.

PMBUS_REVISION (98h)

The PMBUS_REVISION command returns the revision of the PMBus specification to which the module is compliant. The command has 1 data byte. Bits 7:4 indicate the revision of the PMBus specification Part I to which the module is compliant. Bits 3:0 indicate the revision of the PMBus specification Part II to which the module is compliant. This command is read-only. The PMBUS_REVISION value returned is always 11h, which indicates that the module is compliant with Part I, Rev 1.1 and Part II, Rev 1.1.

MFR_SERIAL (9Eh)

The MFR_SERIAL command loads the module with text (ISO/IEC 8859-1) characters that uniquely identify the module. The maximum number of characters is 8. This data is written to internal flash using the STORE_DEFAULT_ALL command. The upper 4 bytes of MFR_SERIAL are used to unlock a module that has been password protected. The lower 4 bytes of MFR_SERIAL are not used to unlock a module, and they can be set to any value.

MFR_MODE (D1h)

The MFR_MODE command is used to configure the module to support manufacturer-specific commands. The MFR_MODE command should not be changed while the module is operating. The MFR_MODE command is described in *Table 21*.

Table 21. MFR_MODE (D1h)

BIT	NAME	MEANING
15:14	0	Always returns 00.
13	ALERT	0 = ALERT output disabled (the module does not respond to ARA). 1 = ALERT output enabled (the module does respond to ARA).
12	0	Always returns 0.
11	SOFT_RESET	This bit must be set, then cleared and set again within 8ms for a soft reset to occur.
10	LOCK	This bit must be set, then cleared and set again within 8ms for the module to become password protected. This bit is cleared when the password is unlocked. The module should only be locked and then unlocked a maximum of 256 times before a power cycle occurs.
9:8	0	Always returns 00.
7:0	—	Internal use. Default value: 22h.

MFR_VOUT_PEAK (D4h)

The MFR_VOUT_PEAK command returns the maximum actual measured output voltage when PAGE = 2, or the maximum actual measured input voltage when PAGE = 9. To reset this value to 0, write to this command with a data value of 0. Any values written to this command are used as a comparison for future peak updates. The 2 data bytes are in DIRECT format.

MFR_IOUT_PEAK (D5h)

The MFR_IOUT_PEAK command returns the maximum actual measured output current when PAGE = 4, or the maximum actual measured input current when PAGE = 10, or the maximum actual measured phase current when PAGE = 5, 6, 7, or 8. To reset this value to 0, write to this command with a data value of 0. Any values written to this command are used as a comparison for future peak updates. The 2 data bytes are in DIRECT format.

MFR_TEMPERATURE_PEAK (D6h)

The MFR_TEMPERATURE_PEAK command returns the maximum measured PCB board temperature when PAGE = 18. To reset this value to its lowest value, write to this command with a data value of 8000h. Any other values written by this command are used as a comparison for future peak updates. The 2 data bytes are in DIRECT format.

MFR_VOUT_MIN (D7h)

The MFR_VOUT_MIN command returns the minimum actual measured output voltage when PAGE = 2, or the minimum actual measured input voltage when PAGE = 9. To reset this value, write to this command with a data value of 7FFFh. Any values written to this command are used as a comparison for future minimum updates. The 2 data bytes are in DIRECT format.

MFR_IOUT_AVG (E2h)

The MFR_IOUT_AVG command returns the calculated average output current when PAGE = 4, or the calculated average input current when PAGE = 10, or the calculated average phase current when PAGE = 5, 6, 7, or 8. Writes to this command are ignored. The 2 data bytes are in DIRECT format.

MFR_NV_LOG_CONFIG (D8h)

The MFR_NV_LOG_CONFIG command is used to configure the operation of the nonvolatile fault logging in the module. The MFR_NV_LOG_CONFIG command is described in *Table 22*.

Table 22. MFR_NV_LOG_CONFIG (D8h)

BIT	NAME	MEANING		
15	FORCE_NV_FAULT_LOG	Setting this bit to a 1, forces the module to log data into the nonvolatile fault log. Once set, the module clears this bit when the action is completed. Host must set again for subsequent action. If an error occurs during this action, the module sets the CML bit in STATUS_WORD; no bits are set in STATUS_CML.		
14	CLEAR_NV_FAULT_LOG	Setting this bit to a 1, forces the module to clear the nonvolatile fault log by writing FFh to all byte locations. Once set, the module clears this bit when the action is completed. Host must set again for subsequent action. If an error occurs during this action, the module sets the CML bit in STATUS_WORD; no bits are set in STATUS_CML. While clearing the fault log, monitoring is stopped and commands should not be sent to the PMBus port.		
13:11	0	Always returns 000.		
10	NV_LOG_T0_CONFIG	This bit determines the source of the data written into the T0 location of each page when a nonvolatile fault log is written: 0 = Log the last regular collection interval ADC reading. 1 = Read the latest ADC value before logging.		
9	NV_LOG_OVERWRITE	0 = Do not overwrite the NV fault log. 1 = Overwrite the NV fault log once it is full. The module clears 2 fault logs at a time when overwrite is enabled.		
8:7	NV_LOG_DEPTH	These bits determine the depth of the NV fault log:		
			ADC RESULT COLLECTION INTERVAL	**NV FAULT LOG DEPTH**
		00	5ms	15ms
		01	20ms	60ms
		10	80ms	240ms
		11	160ms	480ms
6:0	—	Internal use. Default value: 00h.		

MFR_FAULT_RESPONSE (D9h)

The MFR_FAULT_RESPONSE command specifies the response to each fault or warning condition supported by the module. In response to a fault/warning, the module always reports the fault/warning in the appropriate status register and asserts the ALERT output (if enabled in MFR_MODE). A CML fault cannot cause any module action other than setting the status bit and asserting the ALERT output. The MFR_FAULT_RESPONSE command is described in *Table 23*.

When a fault is configured to latch off, the output turns off either immediately or after the TOFF_DELAY as configured or commanded, then remains off until the power is toggled using the OPERATION command or REM pin as configured in the ON_OFF_CONFIG command or the module is power cycled.

When a fault is configured to retry, the output turns off either immediately or after the TOFF_DELAY as configured or commanded, then remains off, until the time in MFR_FAULT_RETRY expires and then restarts.

Before output is enabled, the module checks for overvoltage, overcurrent, and overtemperature faults. Undervoltage faults are detected only when the output turns on and fails to reach the power-good level, and the TON_MAX_FAULT_LIMIT is exceeded.

If bit 15 of MFR_FAULT_RESPONSE is set, faults are logged into the on-board nonvolatile fault log unless the response for the associated fault is configured to take no action (FAULT_LIMIT_RESPONSE = 00). To keep from needlessly filling the fault log with excessive data, the following rules are applied when subsequent faults occur. When overvoltage fault occurs, subsequent overvoltage faults are not written to the fault log until either the CLEAR_FAULTS command is issued or a module reset occurs. The same rule applies to overcurrent, undervoltage, overtemperature, and sequencing faults.

Table 23. MFR_FAULT_RESPONSE (D9h)

BIT	NAME	MEANING	
31:16	—	Internal use. Default value: 0101h.	
15	NV_LOG	0 = Do not log the fault into MFR_NV_FAULT_LOG. 1 = Log the fault into MFR_NV_FAULT_LOG.	
14	—	Internal use. Default value: 1.	
13:12	FILTER	Continuous excursion time before a fault or warning is declared and action is taken:	
		00	Immediate
		01	2ms
		10	3ms
		11	4ms
11:8	—	Internal use. Default value: 0000.	
7:6	OT_FAULT_LIMIT_RESPONSE (when PAGE = 18)	Bits [7:6], [5:4], [3:2], [1:0]	Fault response
5:4	TON_MAX_FAULT_LIMIT _RESPONSE (when PAGE = 2)	11	Sets the corresponding fault bit in the appropriate status register (Note 1). Logs fault into MFR_NV_FAULT_LOG if NV_LOG = 1. Continues operation.
3:2	VOUT_UV_FAULT_LIMIT _RESPONSE (when PAGE = 2, 9)	10 (Retry)	Shuts down the output. Sets the corresponding fault bit in the appropriate status register (Note 1). Logs fault into MFR_NV_FAULT_LOG if NV_LOG = 1. Waits for the time configured in MFR_FAULT_RETRY and restarts.
1:0	VOUT_OV_FAULT_LIMIT _RESPONSE (when PAGE = 2, 9)	01 (Latch off)	Latches off the output. Sets the corresponding fault bit in the appropriate status register (Note 1). Logs fault into MFR_NV_FAULT_LOG if NV_LOG = 1.
	IOUT_OC_FAULT_LIMIT _RESPONSE (when PAGE = 4, 5, 6, 7, 8, 10)	00	Sets the corresponding fault bit in the appropriate status register (Note 1). Continues operation without any action.

Note 1: *ALERT is asserted if enabled when a new status bit is set. A status bit is latched when a particular fault occurs that causes a fault response.*

MFR_FAULT_RETRY (DAh)

The MFR_FAULT_RETRY command sets the delay time between a shutdown due to a fault event and its restarting if the fault response is configured to retry. This command value is used for all fault responses.

The 2 data bytes are in DIRECT format.

MFR_NV_FAULT_LOG (DCh)

Data from each of the 15 nonvolatile fault logs is constituted (in nonvolatile memory) as a block of 255 bytes. Executing the MFR_NV_FAULT_LOG command using the Read 32 SMBus protocol, each block of 255 bytes can be read back from the module in packets of 4 bytes. Alternatively, the MFR_NV_FAULT_LOG can also be executed to read back a block of 255 bytes by using the Block Read SMBus protocol except that the module does not report the Byte Count during read back.

The MFR_NV_FAULT_LOG command must be executed 15 times to dump the complete nonvolatile fault log. If the returned fault log is all FFs (except bytes 0 and 1), this indicates that this fault log has not been written by the module. As the module is operating, it is reading the latest operating conditions for voltage, current, and temperature and updating the status registers. All of this information is stored in on-board RAM. When a fault is detected (if so enabled in MFR_FAULT_RESPONSE), the module automatically logs this information to one of the 15 nonvolatile fault logs. After 15 faults have been written, bit 0 of STATUS_CML is set and the module can be configured (with the NV_LOG_OVERWRITE bit in MFR_NV_LOG_CONFIG) to either stop writing additional fault logs or write over the oldest data. The host can clear the fault log by setting the CLEAR_NV_FAULT_LOG bit in MFR_NV_LOG_CONFIG.

There is a FAULT_LOG_COUNT (16-bit counter) at the beginning of each fault log that indicates which fault log is the latest. This counter rolls over should more than 65,535 faults be logged. This counter is not cleared when the CLEAR_NV_FAULT_LOG bit in MFR_NV_LOG_CONFIG is toggled. The 255 bytes returned by the MFR_NV_FAULT_LOG command are described in *Table 24*.

If an error occurs while the module is attempting to write to or clear the MFR_NV_FAULT_LOG, the module sets the CML bit in STATUS_WORD (no bits are set in STATUS_CML) and ALERT is asserted (if enabled in MFR_MODE).

Table 24. MFR_NV_FAULT_LOG (DCh)

BYTE	PARAMETER	BYTE	PARAMETER
0	00h/FAULT_LOG_INDEX	128	READ_VOUT/READ_IOUT T1 PAGE 9
2	FAULT_LOG_COUNT	130	READ_VOUT/READ_IOUT T2 PAGE 9
4	MFR_TIME_COUNT (LSW)	132	READ_VOUT/READ_IOUT T0 PAGE 10
6	MFR_TIME_COUNT (HSW)	134	READ_VOUT/READ_IOUT T1 PAGE 10
8	0000h	136	READ_VOUT/READ_IOUT T2 PAGE 10
10	STATUS_CML/00h	138	READ_VOUT/READ_IOUT T0 PAGE 11
12	STATUS_WORD	140	READ_VOUT/READ_IOUT T1 PAGE 11
14	STATUS_VOUT/STATUS_IOUT PAGES 0/1	142	READ_VOUT/READ_IOUT T2 PAGE 11
16	STATUS_VOUT/STATUS_IOUT PAGES 2/3	144	READ_VOUT/READ_IOUT T0 PAGE 12
18	STATUS_VOUT/STATUS_IOUT PAGES 4/5	146	READ_VOUT/READ_IOUT T1 PAGE 12
20	STATUS_VOUT/STATUS_IOUT PAGES 6/7	148	READ_VOUT/READ_IOUT T2 PAGE 12
22	STATUS_VOUT/STATUS_IOUT PAGES 8/9	150	READ_VOUT/READ_IOUT T0 PAGE 13
24	STATUS_VOUT/STATUS_IOUT PAGES 10/11	152	READ_VOUT/READ_IOUT T1 PAGE 13
26	STATUS_VOUT/STATUS_IOUT PAGES 12/13	154	READ_VOUT/READ_IOUT T2 PAGE 13
28	STATUS_VOUT/STATUS_IOUT PAGES 14/15	156	READ_VOUT/READ_IOUT T0 PAGE 14
30	STATUS_MFR_SPECIFIC PAGES 0/1	158	READ_VOUT/READ_IOUT T1 PAGE 14
32	STATUS_MFR_SPECIFIC PAGES 2/3	160	READ_VOUT/READ_IOUT T2 PAGE 14
34	STATUS_MFR_SPECIFIC PAGES 4/5	162	READ_VOUT/READ_IOUT T0 PAGE 15
36	STATUS_MFR_SPECIFIC PAGES 6/7	164	READ_VOUT/READ_IOUT T1 PAGE 15
38	STATUS_MFR_SPECIFIC PAGES 8/9	166	READ_VOUT/READ_IOUT T2 PAGE 15
40	STATUS_MFR_SPECIFIC PAGES 10/11	168	MFR_VOUT_PEAK/MFR_IOUT_PEAK PAGE 0
42	STATUS_MFR_SPECIFIC PAGES 12/13	170	MFR_VOUT_PEAK/MFR_IOUT_PEAK PAGE 1
44	STATUS_MFR_SPECIFIC PAGES 14/15	172	MFR_VOUT_PEAK/MFR_IOUT_PEAK PAGE 2
46	STATUS_MFR_SPECIFIC PAGE 255/00h	174	MFR_VOUT_PEAK/MFR_IOUT_PEAK PAGE 3

BYTE	PARAMETER	BYTE	PARAMETER
48	STATUS_TEMPERATURE PAGES 16/17	176	MFR_VOUT_PEAK/MFR_IOUT_PEAK PAGE 4
50	STATUS_TEMPERATURE PAGES 18/19	178	MFR_VOUT_PEAK/MFR_IOUT_PEAK PAGE 5
52	STATUS_TEMPERATURE PAGE 20/00h	180	MFR_VOUT_PEAK/MFR_IOUT_PEAK PAGE 6
54	CURRENT_CHANNELS (Note 4)	182	MFR_VOUT_PEAK/MFR_IOUT_PEAK PAGE 7
56	STATUS_INPUT PAGES 0/1	184	MFR_VOUT_PEAK/MFR_IOUT_PEAK PAGE 8
58	STATUS_INPUT PAGES 2/3	186	MFR_VOUT_PEAK/MFR_IOUT_PEAK PAGE 9
60	STATUS_INPUT PAGES 4/5	188	MFR_VOUT_PEAK/MFR_IOUT_PEAK PAGE 10
62	STATUS_INPUT PAGES 6/7	190	MFR_VOUT_PEAK/MFR_IOUT_PEAK PAGE 11
64	STATUS_INPUT PAGES 8/9	192	MFR_VOUT_PEAK/MFR_IOUT_PEAK PAGE 12
66	STATUS_INPUT PAGES 10/11	194	MFR_VOUT_PEAK/MFR_IOUT_PEAK PAGE 13
68	STATUS_INPUT PAGES 12/13	196	MFR_VOUT_PEAK/MFR_IOUT_PEAK PAGE 14
70	STATUS_INPUT PAGES 14/15	198	MFR_VOUT_PEAK/MFR_IOUT_PEAK PAGE 15
72	READ_VOUT/READ_IOUT T0 PAGE 0 (Notes 2, 3)	200	MFR_VOUT_MIN PAGE 0
74	READ_VOUT/READ_IOUT T1 PAGE 0 (Notes 2, 3)	202	MFR_VOUT_MIN PAGE 1
76	READ_VOUT/READ_IOUT T2 PAGE 0 (Notes 2, 3)	204	MFR_VOUT_MIN PAGE 2
78	READ_VOUT/READ_IOUT T0 PAGE 1	206	MFR_VOUT_MIN PAGE 3
80	READ_VOUT/READ_IOUT T1 PAGE 1	208	MFR_VOUT_MIN PAGE 4
82	READ_VOUT/READ_IOUT T2 PAGE 1	210	MFR_VOUT_MIN PAGE 5
84	READ_VOUT/READ_IOUT T0 PAGE 2	212	MFR_VOUT_MIN PAGE 6
86	READ_VOUT/READ_IOUT T1 PAGE 2	214	MFR_VOUT_MIN PAGE 7
88	READ_VOUT/READ_IOUT T2 PAGE 2	216	MFR_VOUT_MIN PAGE 8
90	READ_VOUT/READ_IOUT T0 PAGE 3	218	MFR_VOUT_MIN PAGE 9
92	READ_VOUT/READ_IOUT T1 PAGE 3	220	MFR_VOUT_MIN PAGE 10
94	READ_VOUT/READ_IOUT T2 PAGE 3	222	MFR_VOUT_MIN PAGE 11
96	READ_VOUT/READ_IOUT T0 PAGE 4	224	MFR_VOUT_MIN PAGE 12
98	READ_VOUT/READ_IOUT T1 PAGE 4	226	MFR_VOUT_MIN PAGE 13
100	READ_VOUT/READ_IOUT T2 PAGE 4	228	MFR_VOUT_MIN PAGE 14
102	READ_VOUT/READ_IOUT T0 PAGE 5	230	MFR_VOUT_MIN PAGE 15
104	READ_VOUT/READ_IOUT T1 PAGE 5	232	READ_TEMPERATURE_1 PAGE 16
106	READ_VOUT/READ_IOUT T2 PAGE 5	234	READ_TEMPERATURE_1 PAGE 17
108	READ_VOUT/READ_IOUT T0 PAGE 6	236	READ_TEMPERATURE_1 PAGE 19
110	READ_VOUT/READ_IOUT T1 PAGE 6	238	READ_TEMPERATURE_1 PAGE 19
112	READ_VOUT/READ_IOUT T2 PAGE 6	240	READ_TEMPERATURE_1 PAGE 20
114	READ_VOUT/READ_IOUT T0 PAGE 7	242	MFR_TEMPERATURE_PEAK PAGE 16
116	READ_VOUT/READ_IOUT T1 PAGE 7	244	MFR_TEMPERATURE_PEAK PAGE 17
118	READ_VOUT/READ_IOUT T2 PAGE 7	246	MFR_TEMPERATURE_PEAK PAGE 18
120	READ_VOUT/READ_IOUT T0 PAGE 8	248	MFR_TEMPERATURE_PEAK PAGE 19
122	READ_VOUT/READ_IOUT T1 PAGE 8	250	MFR_TEMPERATURE_PEAK PAGE 20
124	READ_VOUT/READ_IOUT T2 PAGE 8	252	0000h
126	READ_VOUT/READ_IOUT T0 PAGE 9	254	LOG_VALID (Note 1)

Note 1: *LOG_VALID is set to DDh if the fault log contains valid data.*

Note 2: *For READ_VOUT, READ_IOUT, T2 is the oldest reading and T0 is the newest reading.*

Note 3: *STATUS_VOUT/STATUS_IOUT and READ_VOUT/READ_IOUT depend on whether the rail (or PAGE) is configured to monitor voltage or current, see* Table 5.

Note 4: *CURRENT_CHANNELS is a bitmask (0 = voltage/1 = current) indicating which channels (or PAGES) are enabled for current measurement, see* Table 5.

MFR_TIME_COUNT (DDh)

The MFR_TIME_COUNT command returns the current value of a real-time counter that increments every 5ms, 20ms, 80ms, or 160ms depending on the configuration of the NV_LOG_DEPTH bits in MFR_NV_LOG_CONFIG. This counter is useful in determining the time between multiple faults. The counter is a 32-bit value that rolls over. The count is reset to zero upon module power cycle, or a soft-reset. MFR_TIME_COUNT can be preset to any value and starts counting up from the preset value.

MFR_MARGIN_CONFIG (DFh)

The module uses an internal PWM signal to implement the MARGIN function. And the MFR_MARGIN_CONFIG (DFh) command is used to configure this PWM signal to margin the output voltage. The MFR_MARGIN_CONFIG command is described in *Table 25*.

Table 25. MFR_MARGIN_CONFIG (DCh)

BIT	NAME	MEANING
15	SLOPE	DAC and PWM setting to resulting voltage relationship: 0 = Negative slope, increasing PWM duty cycle results in a lower voltage. 1 = Positive slope, increasing PWM duty cycle results in a higher voltage.
14	OPEN_LOOP	0 = Normal closed-loop margining. 1 = PWM duty cycle or DAC value set constantly to the DC_DAC value when margining invoked.
13:8	0	Always returns 000000.
7:0	DC_DAC	This 8-bit value has two purposes (default value: 3Eh): With PWM margining, it is used as the initial PWM duty cycle when the module begins to margin a power supply either up or down. When bit 14 is set, this value is used to set the PWM duty cycle.

The margin function works only when output voltage is higher than its programmed POWER_GOOD_ON level.

When OPERATION is set to one of the margin states, margining is initiated, and the module margins the output voltage. The module averages four samples of V_{OUT} for a total time of 20ms. If the measured V_{OUT} and the target (set by either VOUT_MARGIN_HIGH or VOUT_MARGIN_LOW) differ, the PWM duty cycle is adjusted by one step. The direction of the duty-cycle adjustment is determined by the SLOPE bit in MFR_MARGIN_CONFIG, and a negative slope must be used here.

When the OPERATION command deactivates margining, and the margining has been running with the “Ignore All Faults” condition, the module does not begin monitoring for faults for 100ms after the “Margin Off” input is received to allow time for the output voltage to return to a normal condition.

Margining Faults

The module detects two possible margining faults. First, if the initial PWM duty cycle causes V_{OUT} to exceed the target value (either high or low, depending on whether the module has been instructed to margin high or low, respectively), this creates a fault. Second, if the target value cannot be reached when the PWM duty cycle reaches zero or full scale, this also creates a fault. If either margining fault occurs, the module continues attempting to margin the output and does the following:

1) Sets the MARGIN bit in STATUS_WORD.
2) Sets the MARGIN_FAULT bit in STATUS_MFR_SPECIFIC (PAGE 2).
3) Notifies the host through ALERT assertion (if enabled in MFR_MODE).

DC_DAC Value

When bit 14 of MFR_MARGIN_CONFIG is set, adjusting the value of DC_DAC could adjust the output voltage by the formula:

DC_DAC = 626.4 – 47.23 × V_{OUT_TARGET} (for ADPM12160CMLZxx)

DC_DAC = 740.8 – 54.54 × V_{OUT_TARGET} (for ADPM12160CMLZxxA)

where V_{OUT_TARGET} is the target output voltage in volts, and DC_DAC is the value of bit[7:0] of MFR_MARGIN_CONFIG in decimal.

MFR_CONFIG_VERSION (ECh)

The MFR_CONFIG_VERSION command returns the user-defined configuration file version that is loaded in the module. This command is read-and-write.

MFR_WP_CONTROL (F2h)

The MFR_WP_CONTROL command provides write protection to the module, which prevents the configuration file from being modified. The provided write protection features double security, which means users must write a certain value to MFR_WP_CONTROL first, then recycle the power to disable the write protection. Doing so with only one step or reserved sequence will not be able to disable the write protection of the module. The write protection feature of the module is disabled by default, and it can be enabled by writing any value other than 9Ch to the command.

Outline Dimensions

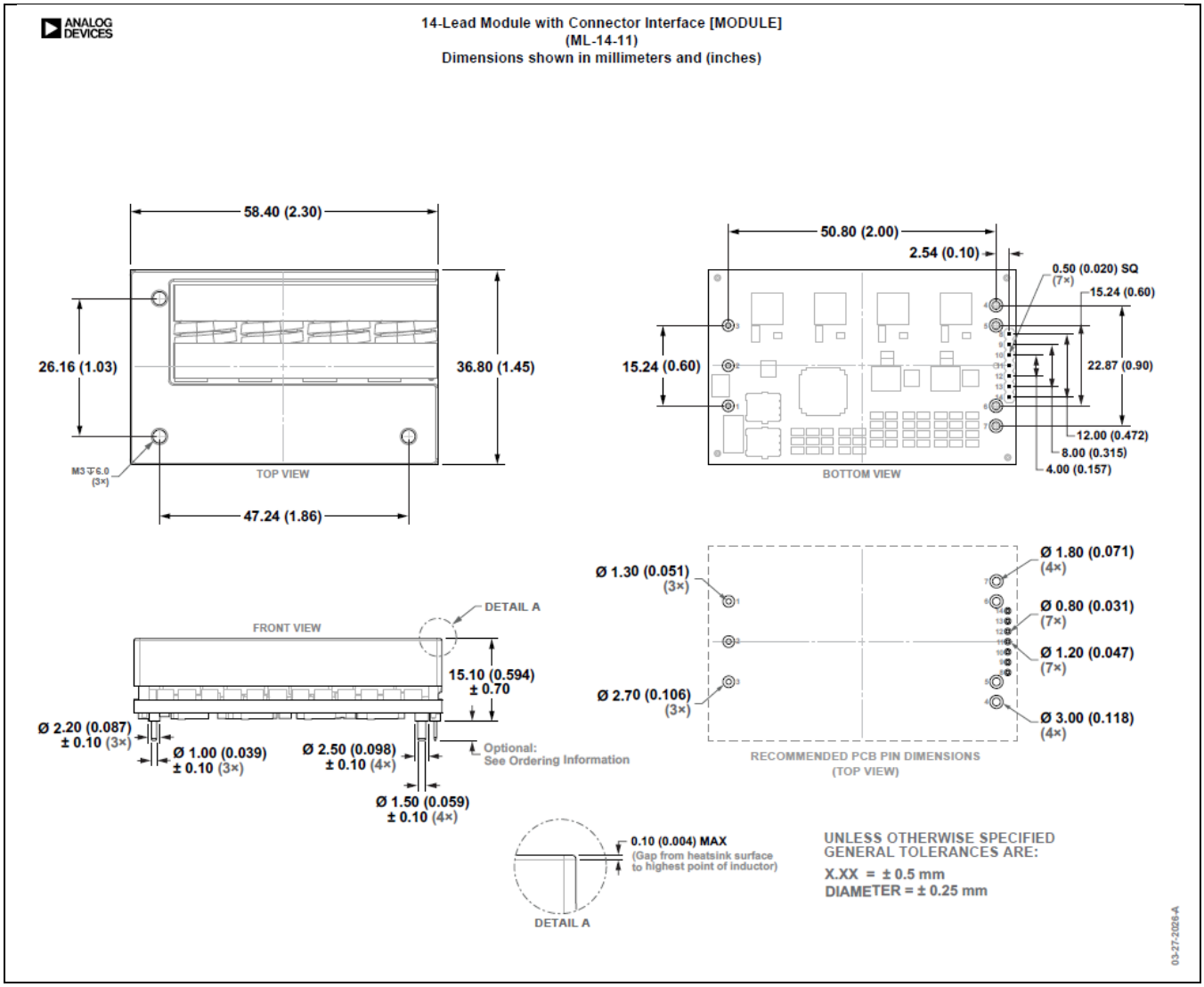


Figure 10. Outline Diagram

Soldering Information

Through-Hole Soldering

The hole-mounted product is intended for plated through-hole mounting by wave or manual soldering. Reflow soldering is discouraged for through-hole-mounted power modules, as the associated difficulties can compromise reliability.

Maximum preheat rate of 3°C/s and temperature of +150°C (max) is suggested. When soldering by hand, care should be taken to avoid direct contact between the hot soldering iron tip and the pins for more than a few seconds in order to prevent overheating.

A no-clean (NC) flux is recommended to avoid entrapment of cleaning fluids in cavities inside of the DC-DC power module. The residues may affect long-time reliability and isolation voltage.

Lead-Free (Pb-Free) Solder Processes

For Pb-free solder processes, a pin temperature (T_{PIN}) in excess of the solder melting temperature (T_L, +217°C to +221°C for Sn/Ag/Cu solder alloys) for more than 30 seconds and a peak temperature of +240°C on all solder joints are recommended to ensure a reliable solder joint.

For Pb-free solder processes, the ADPM12160 is qualified for MSL 3 according to IPC/JEDEC standard J-STD-020C.

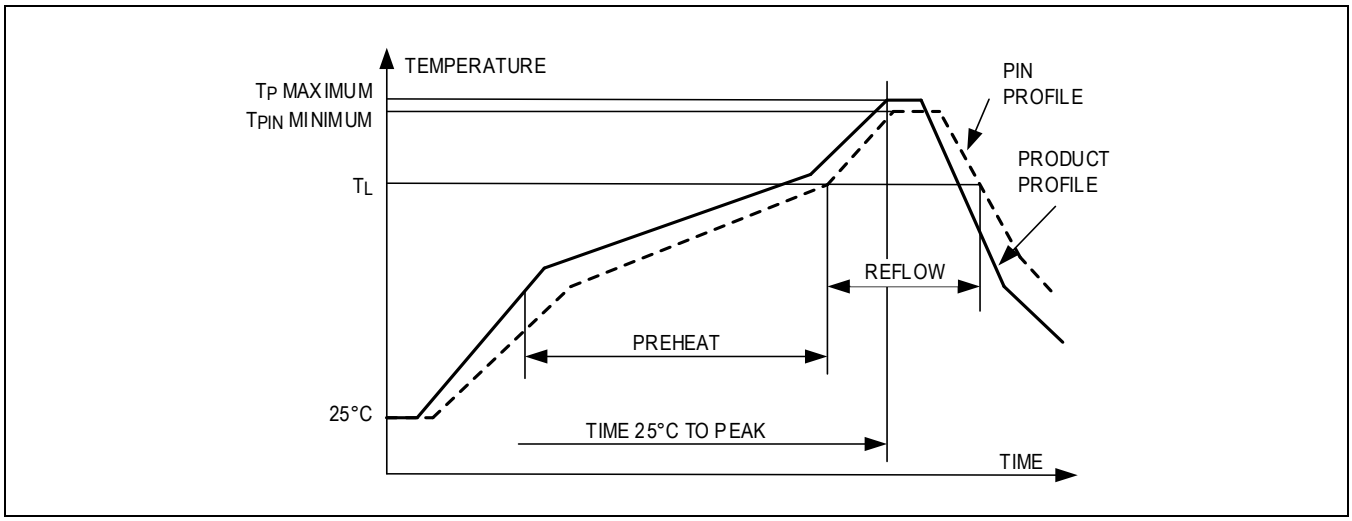


Figure 11. Recommended Reflow Profile

Table 26. Reflow Process Specifications

REFLOW PROCESS SPECIFICATIONS		Pb-FREE
Average ramp-up rate (T_P)		3°C/s, max
Typical solder melting (liquidus) temperature	T_L	+221°C
Minimum reflow time above T_L		30s ~ 90s
Minimum pin temperature (measured on the power module pins)	T_{PIN}	+235°C
Peak product temperature	T_{PEAK}	+240°C
Average ramp-down rate (T_P)		6°C/s, max
Maximum time 25°C to peak		8min

Ordering Information

PART NUMBER	PIN LENGTH	V_{OUT}	REM LOGIC	PACKAGE DESCRIPTION	TEMP RANGE
ADPM12160CMLZBH	2.79mm	12V	Active high	Quarter brick, 58.4mm × 36.8mm × 15.1mm	-40°C to +85°C
ADPM12160CMLZCH	3.70mm				
ADPM12160CMLZDH	4.32mm				
ADPM12160CMLZBL	2.79mm	12V	Active low		
ADPM12160CMLZCL	3.70mm				
ADPM12160CMLZDL	4.32mm				
ADPM12160CMLZBHA	2.79mm	12.5V	Active high	Quarter brick, 58.4mm × 36.8mm × 15.1mm	-40°C to +85°C
ADPM12160CMLZCHA	3.70mm				
ADPM12160CMLZDHA	4.32mm				
ADPM12160CMLZBLA	2.79mm	12.5V	Active low		
ADPM12160CMLZCLA	3.70mm				
ADPM12160CMLZDLA	4.32mm				

All products are halogen-free and MSL 3 qualified.

Packing Details

The products are supplied as standard in the antistatic tray, shown in *Figure 11*.

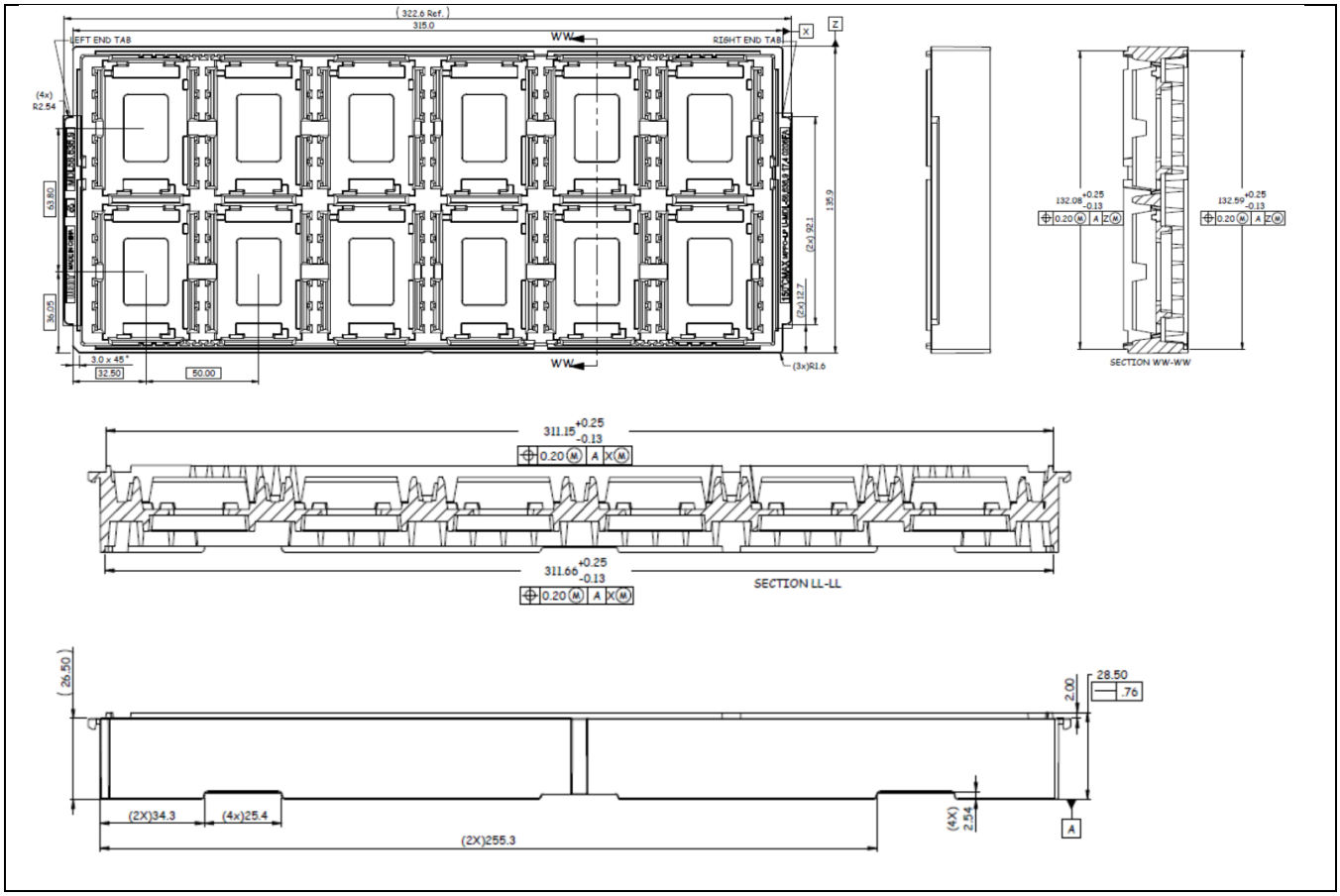


Figure 12. Packaging Tray Diagram

Table 27. Tray Specification

Material	CF, antistatic
Surface Resistance	$10^6\Omega \sim 10^{11}\Omega$
Tray Capacity	12 products/tray
Box Capacity	36 products, 3 full trays/box

Revision History

REVISION MUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	10/25	Initial release	–
1	3/26	Added ADPM12160CMLZxxA information: Updated Product Features and General Description sections Updated EC table Added Notes 2, 3, and 4 to the Electrical Characteristics table Added TOC 03 and TOC 04 Updated Pin Descriptions table Updated Power-Good Output (PGOOD) section Updated Notes for Table 4 Updated Table 6 Updated DC_DAC Value section Updated Outline Dimensions Updated Ordering Information table	 1 2,3 4 5 7 8 16 17 34 35 37
2	4/26	Updated Electrical Characteristics notes Updated Table 4 Updated Table 6	3, 4 14–16 17

Information furnished by Analog Devices is believed to be accurate and reliable. However, no responsibility is assumed by Analog Devices for its use, nor for any infringements of patents or other rights of third parties that may result from its use. Specifications subject to change without notice. No license is granted by implication or otherwise under any patent or patent rights of Analog Devices. Trademarks and registered trademarks are the property of their respective owners. All Analog Devices products contained herein are subject to release and availability.