Data Sheet

ADPL42010A

20V, 1A, Fast Transient Response LDO Regulator

FEATURES

- **Optimized for Fast Transient Response**
- **Output Current: 1A**
- **Dropout Voltage: 400mV**
- **Noise: 70µV_{RMS} (10Hz to 100kHz)**
- **1mA Quiescent Current**
- No Protection Diodes Needed
- Fixed Output Voltages: 1.5V, 1.8V, 2.5V, 3.3V
- Adjustable Output from 1.21V to 20V
- <1µA Quiescent Current in Shutdown
- Stable with 10µF Output Capacitor (see the *Applications Information* section)
- Stable with Ceramic Capacitors (see the *Applications Information* section)
- Reverse Battery Protection
- No Reverse Current
- Thermal Limiting
- 3-Lead SOT-223 and 8-Lead SO Packages

APPLICATIONS

- 3.3V to 2.5V Logic Power Supplies
- Post Regulator for Switching Supplies

GENERAL DESCRIPTION

The ADPL42010A is a low dropout regulator optimized for fast transient response. The device is capable of supplying 1A of output current with a dropout voltage of 400mV. Operating quiescent current is 1mA, dropping to <1µA in shutdown.

Output voltage range is from 1.21V to 20V. The ADPL42010A regulator is stable with output capacitors as low as 10µF. Internal protection circuitry includes reverse battery protection, current limiting, thermal limiting and reverse current protection. The ADPL42010A is available in fixed output voltages of 1.5V, 1.8V, 2.5V, 3.3V, and as an adjustable device with a 1.21V reference voltage. The ADPL42010A regulator is available in 3-lead SOT-223 and 8-lead SO packages.

TYPICAL APPLICATION CIRCUIT

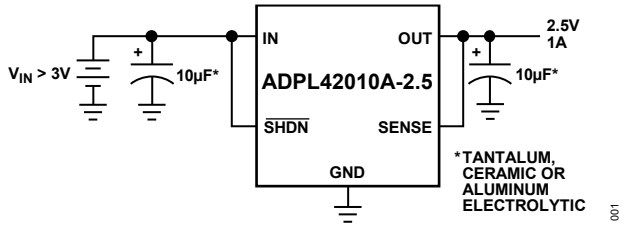


Figure 1. ADPL42010A with Fixed Output Voltage, 2.5V

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SPECIFICATIONS

Table 1. Electrical Characteristics

(The specifications apply over the full-operating temperature range, unless specified otherwise. (1))

PARAMETER	CONDITIONS	COMMENTS	MIN	TYP	MAX	UNITS
Minimum Input Voltage (2, 3)	I_{LOAD} = 0.5A	T_A = 25°C		1.9		V
	I_{LOAD} = 1A			2.1	2.5	V
Regulated Output Voltage (4)	ADPL42010A-1.5 V_{IN} = 2.21V, I_{LOAD} = 1mA	T_A = 25°C	1.477	1.500	1.523	V
	ADPL42010A-1.5 2.5V < V_{IN} < 20V, 1mA < I_{LOAD} < 1A		1.447	1.500	1.545	V
	ADPL42010A-1.8 V_{IN} = 2.3V, I_{LOAD} = 1mA	T_A = 25°C	1.773	1.800	1.827	V
	ADPL42010A-1.8 2.8V < V_{IN} < 20V, 1mA < I_{LOAD} < 1A		1.737	1.800	1.854	V
	ADPL42010A-2.5 V_{IN} = 3V, I_{LOAD} = 1mA	T_A = 25°C	2.462	2.500	2.538	V
	ADPL42010A-2.5 3.5V < V_{IN} < 20V, 1mA < I_{LOAD} < 1A		2.412	2.500	2.575	V
	ADPL42010A-3.3 V_{IN} = 3.8V, I_{LOAD} = 1mA	T_A = 25°C	3.250	3.300	3.350	V
	ADPL42010A-3.3 4.3V < V_{IN} < 20V, 1mA < I_{LOAD} < 1A		3.200	3.300	3.400	V
ADJ Pin Voltage (2, 4)	ADPL42010A V_{IN} = 2.21V, I_{LOAD} = 1mA	T_A = 25°C	1.192	1.210	1.228	V
	ADPL42010A 2.5V < V_{IN} < 20V, 1mA < I_{LOAD} < 1A		1.174	1.210	1.246	V
Line Regulation	ADPL42010A-1.5 ΔV_{IN} = 2.21V to 20V, I_{LOAD} = 1mA			2.0	6	mV
	ADPL42010A-1.8 ΔV_{IN} = 2.3V to 20V, I_{LOAD} = 1mA			2.5	7	mV

(The specifications apply over the full-operating temperature range, unless specified otherwise. (1))

PARAMETER	CONDITIONS	COMMENTS	MIN	TYP	MAX	UNITS
	ADPL42010A-2.5 ΔV_{IN} = 3V to 20V, I_{LOAD} = 1mA			3.0	10	mV
	ADPL42010A-3.3 ΔV_{IN} = 3.8V to 20V, I_{LOAD} = 1mA			3.5	10	mV
	ADPL42010A (2) ΔV_{IN} = 2.21V to 20V, I_{LOAD} = 1mA			1.5	5	mV
Load Regulation	ADPL42010A-1.5 V_{IN} = 2.5V, ΔI_{LOAD} = 1mA to 1A	T_A = 25°C		2	9	mV
					18	mV
	ADPL42010A-1.8 V_{IN} = 2.8V, ΔI_{LOAD} = 1mA to 1A	T_A = 25°C		2	10	mV
					20	mV
	ADPL42010A-2.5 V_{IN} = 3.5V, ΔI_{LOAD} = 1mA to 1A	T_A = 25°C		2.5	15	mV
					30	mV
	ADPL42010A-3.3 V_{IN} = 4.3V, ΔI_{LOAD} = 1mA to 1A	T_A = 25°C		3	20	mV
					35	mV
	ADPL42010A (2) V_{IN} = 2.5V, ΔI_{LOAD} = 1mA to 1A	T_A = 25°C		2	8	mV
					15	mV
Dropout Voltage $V_{IN} = V_{OUT(NOMINAL)}$ (3, 5, 6)	I_{LOAD} = 1mA	T_A = 25°C		0.02	0.06	V
					0.10	V
	I_{LOAD} = 1A	T_A = 25°C		0.4	0.55	V
					0.65	V
GND Pin Current $V_{IN} = V_{OUT(NOMINAL)}$ + 1V (5, 7)	I_{LOAD} = 0mA			1.0	1.5	mA
	I_{LOAD} = 1A			80	120	mA
Output Voltage Noise	C_{OUT} = 10µF, I_{LOAD} = 1A, BW = 10Hz to 100kHz	T_A = 25°C		70		µVRMS
ADJ Pin Bias Current (2, 8)		T_A = 25°C		3	10	µA
Shutdown Pin Threshold	V_{OUT} = Off to On			0.90	2	V
	V_{OUT} = On to Off		0.25	0.75		V
$\overline{SHDN}$ Pin Current (9)	$V_{\overline{SHDN}}$ = 0V	T_A = 25°C		0.01	1	µA

(The specifications apply over the full-operating temperature range, unless specified otherwise. ([1]))

PARAMETER	CONDITIONS	COMMENTS	MIN	TYP	MAX	UNITS
	$V_{\overline{SHDN}}$ = 20V	T_A = 25°C		3	30	µA
Quiescent Current in Shutdown	V_{IN} = 6V, $V_{\overline{SHDN}}$ = 0V	T_A = 25°C		0.01	1	µA
Ripple Rejection	$V_{IN} - V_{OUT}$ = 1.5V (Avg), V_{RIPPLE} = 0.5V_{Pk-Pk}, f_{RIPPLE} = 120Hz, I_{LOAD} = 0.75A	T_A = 25°C		55		dB
Current Limit	V_{IN} = 7V, V_{OUT} = 0V	T_A = 25°C		2		A
	V_{IN} = $V_{OUT(NOMINAL)}$ + 1V, ΔV_{OUT} = –0.1V		1.6			A
Input Reverse Leakage Current ([10])	S8 Package V_{IN} = –20V, V_{OUT} = 0				1	mA
	ST Package V_{IN} = –20V, V_{OUT} = 0				2	mA
Reverse Output Current ([11])	ADPL42010A-1.5 V_{OUT} = 1.5V, V_{IN} < 1.5V	T_A = 25°C		600	1200	µA
	ADPL42010A-1.8 V_{OUT} = 1.8V, V_{IN} < 1.8V	T_A = 25°C		600	1200	µA
	ADPL42010A-2.5 V_{OUT} = 2.5V, V_{IN} < 2.5V	T_A = 25°C		600	1200	µA
	ADPL42010A-3.3 V_{OUT} = 3.3V, V_{IN} < 3.3V	T_A = 25°C		600	1200	µA
	ADPL42010A ([2]) V_{OUT} = 1.21V, V_{IN} < 1.21V	T_A = 25°C		300	600	µA

1 The ADPL42010A is tested and specified under pulse load conditions such that $T_J \approx T_A$. The ADPL42010AB is 100% tested at T_A = 25°C. Performance at –40°C and +125°C is assured by design, characterization and correlation with statistical process controls.

2 The ADPL42010A (adjustable version) is tested and specified for these conditions with the ADJ pin connected to the OUT pin.

3 For the ADPL42010A, ADPL42010A-1.5, and ADPL42010A-1.8 dropout voltage is limited by the minimum input voltage specification under some output voltage/load conditions.

4 Operating conditions are limited by maximum junction temperature. The regulated output voltage specification does not apply for all possible combinations of input voltage and output current. When operating at maximum input voltage, the output current range must be limited. When operating at maximum output current, the input voltage range must be limited.

5 To satisfy requirements for minimum input voltage, the ADPL42010A (adjustable version) is tested and specified for these conditions with an external resistor divider (two 4.12kΩ resistors) for an output voltage of 2.4V. The external resistor divider adds a 300µA DC load on the output.

6 Dropout voltage is the minimum input to output voltage differential needed to maintain regulation at a specified output current. In dropout, the output voltage is equal to $V_{IN} - V_{DROPOUT}$.

7 GND pin current is tested with $V_{IN} = V_{OUT(NOMINAL)} + 1V$ and a current source load. The GND pin current decreases at higher input voltages.

8 ADJ pin bias current flows into the ADJ pin.

9 $\overline{SHDN}$ pin current flows into the $\overline{SHDN}$ pin.

10 For the ST package, the input reverse leakage current increases due to the additional reverse leakage current for the $\overline{SHDN}$ pin, which is connected internally to the IN pin.

11 Reverse output current is tested with the IN pin grounded and the OUT pin forced to the rated output voltage. This current flows into the OUT pin and out the GND pin.

ABSOLUTE MAXIMUM RATINGS

T_A = 25°C, unless otherwise specified.

Table 2. Absolute Maximum Ratings

PARAMETER	RATING
IN Pin Voltage	±20V
OUT Pin Voltage	±20V
Input to Output Differential Voltage ([1])	±20V
SENSE Pin Voltage	±20V
ADJ Pin Voltage	±7V
$\overline{SHDN}$ Pin Voltage	±20V
Output Short-Circuit Duration	Indefinite
Temperature	
Operating Junction Range (ADPL42010AB) ([2])	–40°C to +125°C
Storage Range	–65°C to +150°C
Lead (Soldering, 10sec)	300°C

1 Absolute maximum input to output differential voltage can not be achieved with all combinations of rated IN pin and OUT pin voltages. With the IN pin at 20V, the OUT pin may not be pulled below 0V. The total measured voltage from IN to OUT can not exceed ±20V.

2 The ADPL42010A is tested and specified under pulse load conditions such that $T_J \approx T_A$. The ADPL42010AB is 100% tested at T_A = 25°C. Performance at –40°C and +125°C is assured by design, characterization, and correlation with statistical process controls.

Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

Thermal Data

Absolute maximum ratings apply individually only, not in combination. The ADPL42010A can be damaged when the junction temperature limits are exceeded. Monitoring ambient temperature does not guarantee that T_J is within the specified temperature limits. The junction temperature of the device is dependent on the ambient temperature, the power dissipation (P_D) of the device, and the junction-to-ambient thermal resistance of the package (θ_{JA}).

Maximum T_J is calculated from the T_A and P_D using the following formula:

$$T_J = T_A + (P_D \times \theta_A) \qquad (1)$$

Thermal Resistance

θ_{JA} and θ_{JC} are specified in *Figure 2* and *Figure 3*. θ_{JA} measurements are taken in still air on a 1/16” FR-4 board with 1oz copper.

ESD Caution

	**ESD (electrostatic discharge) sensitive device.** Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS

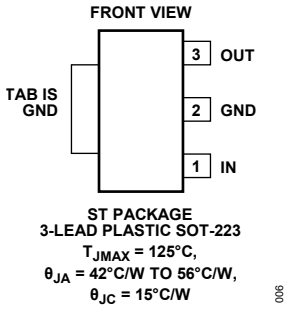


Figure 2. 3-Lead SOT-223 Pin Configuration

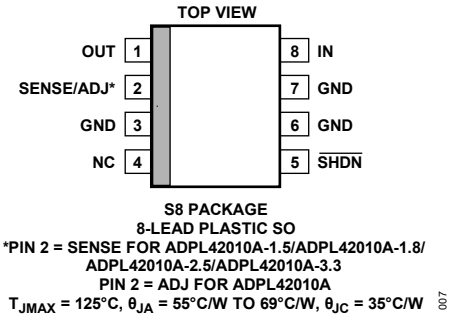
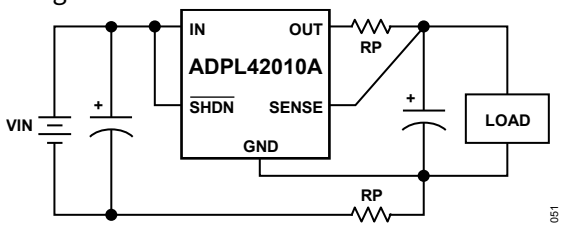


Figure 3. 8-Lead SO Pin Configuration

Pin Descriptions

Table 3. Pin Descriptions

PIN		NAME	DESCRIPTION
3-Lead SOT-223	8-Lead SO		
3	1	OUT	Regulator Outpu Pin. The output supplies power to the load. A minimum output capacitor of 10µF is required to prevent oscillations. Larger output capacitors are required for applications with large transient loads to limit peak voltage transients. For more details on output capacitance and reverse output characteristics, see the *Applications Information* section.
	2	SENSE/ADJ	Sense Pin. For fixed voltage versions of the ADPL42010A (ADPL42010A-1.5/ADPL42010A-1.8/ADPL42010A-2.5/ADPL42010A-3.3), the SENSE pin is the input to the error amplifier. Optimum regulation is obtained at the point where the SENSE pin is connected to the OUT pin of the regulator. In critical applications, small voltage drops are caused by the resistance (R_P) of PC traces between the regulator and the load. These may be eliminated by connecting the SENSE pin to the output at the load, as shown in *Figure 4*. Note that the voltage drop across the external PC traces add to the dropout voltage

PIN		NAME	DESCRIPTION
3-Lead SOT-223	8-Lead SO		
			of the regulator. The SENSE pin bias current is 600µA at the nominal rated output voltage. The SENSE pin can be pulled below ground (as in a dual supply system where the regulator load is returned to a negative supply) and still allow the device to start and operate. Adjust Pin. For the adjustable ADPL42010A, the ADJ pin is the input to the error amplifier. This pin is internally clamped to ±7V. It has a bias current of 3µA which flows into the pin. The ADJ pin voltage is 1.21V referenced to ground and the output voltage range is 1.21V to 20V.  ***Figure 4. Kelvin Sense Connection***
2	3, 6, 7	GND	Regulator Ground Pin. To ensure proper elecrical and thermal performance, connect all GND pins of the package to the ground.
	4	NC	No Connect. Not connected internally.
	5	$\overline{\text{SHDN}}$	Shutdown Pin. The $\overline{\text{SHDN}}$ pin is used to put the ADPL42010A regulators into a low-power shutdown state. The output is off when the $\overline{\text{SHDN}}$ pin is pulled low. The $\overline{\text{SHDN}}$ pin can be driven either by 5V logic or open-collector logic with a pull-up resistor. The pull-up resistor is required to supply the pull-up current of the opencollector gate, normally several microamperes, and the $\overline{\text{SHDN}}$ pin current, typically 3µA. If unused, the $\overline{\text{SHDN}}$ pin must be connected to V_{IN}. The device is in the low-power shutdown state if the $\overline{\text{SHDN}}$ pin is not connected.
1	8	IN	Regulator Supply Input Pin. Power is supplied to the device through the IN pin. A bypass capacitor is required on this pin if the device is more than 6inches away from the main input filter capacitor. In general, the output impedance of a battery rises with frequency, so it is advisable to include a bypass capacitor in battery-powered circuits. A bypass capacitor in the range of 1µF to 10µF is sufficient. The ADPL42010A regulators are designed to withstand reverse voltages on the IN pin with respect to ground and the OUT pin. In the case of a reverse input, which can happen if a battery is plugged in backwards, the device acts as if there is a diode in series with its input. There is no reverse current flow into the regulator and no

PIN		NAME	DESCRIPTION
3-Lead SOT-223	8-Lead SO		
			reverse voltage appears at the load. The device protects both itself and the load.

TYPICAL PERFORMANCE CHARACTERISTICS

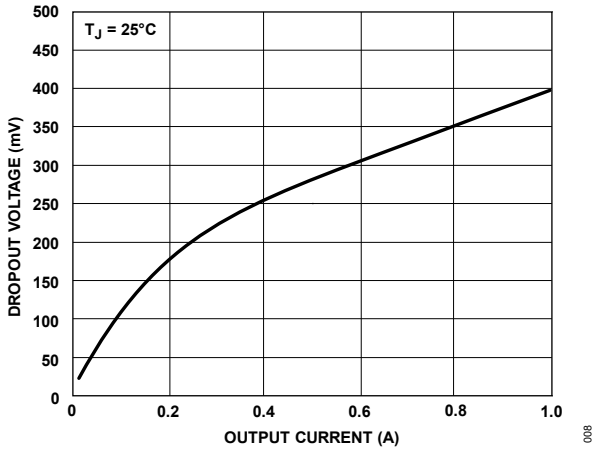


Figure 5. Typical Dropout Voltage

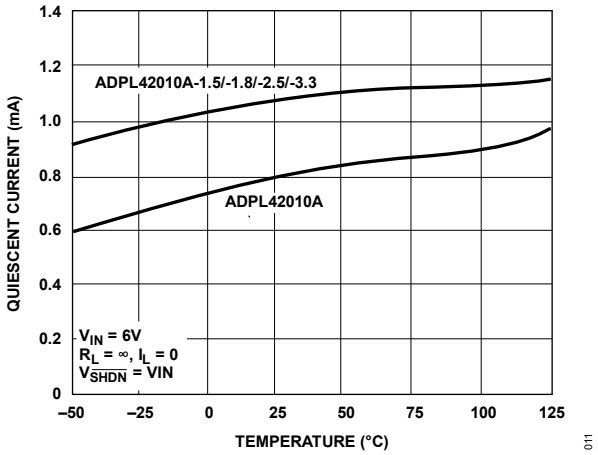


Figure 6. Quiescent Current

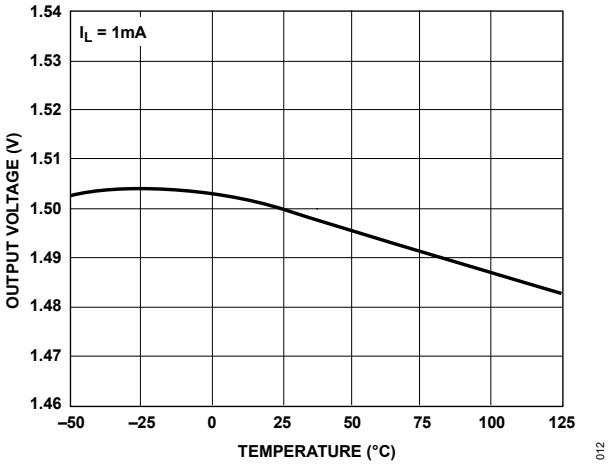


Figure 7. ADPL42010A-1.5 Output Voltage

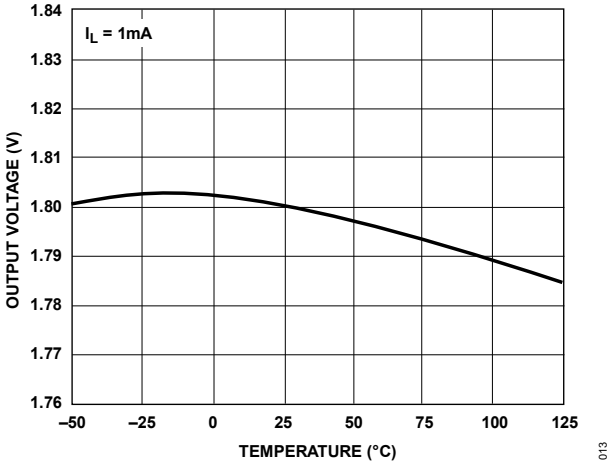


Figure 8. ADPL42010A-1.8 Output Voltage

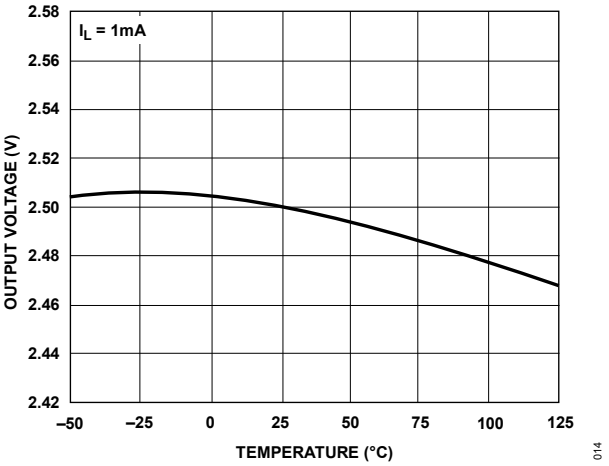


Figure 9. ADPL42010A-2.5 Output Voltage

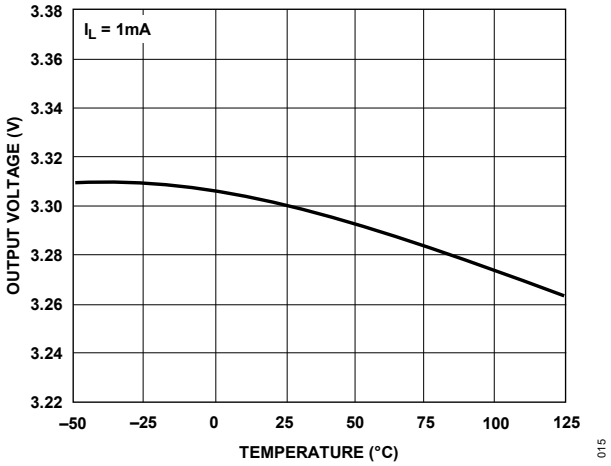


Figure 10. ADPL42010A-3.3 Output Voltage

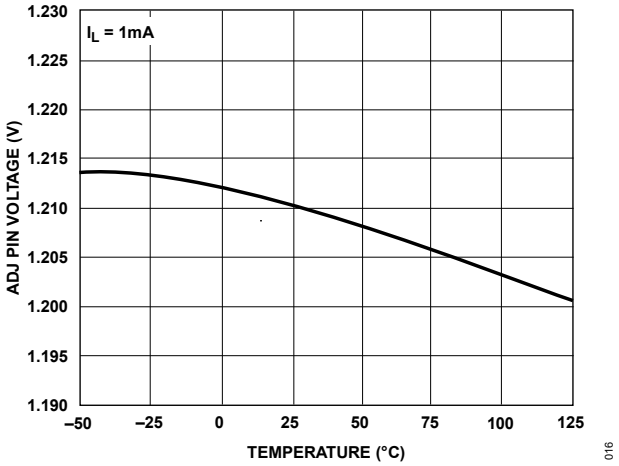


Figure 11. ADPL42010A ADJ Pin Voltage

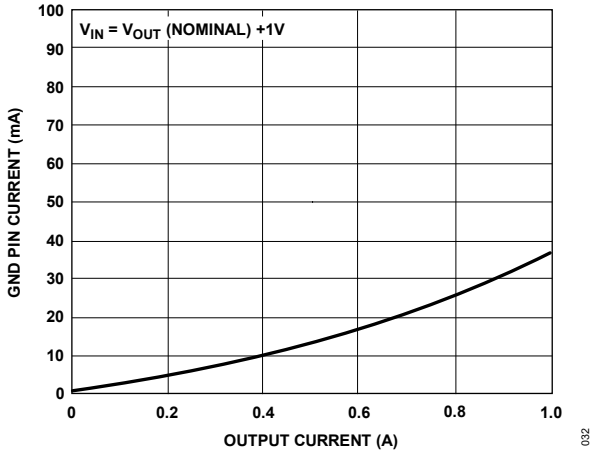


Figure 12. GND Pin Current vs. I_{LOAD}

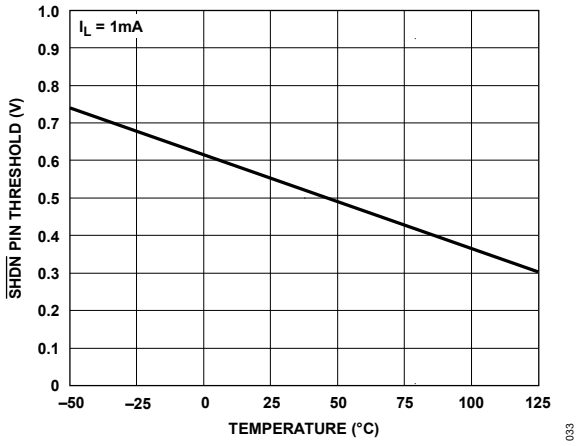


Figure 13. $\overline{SHDN}$ Pin Threshold (On-to-Off)

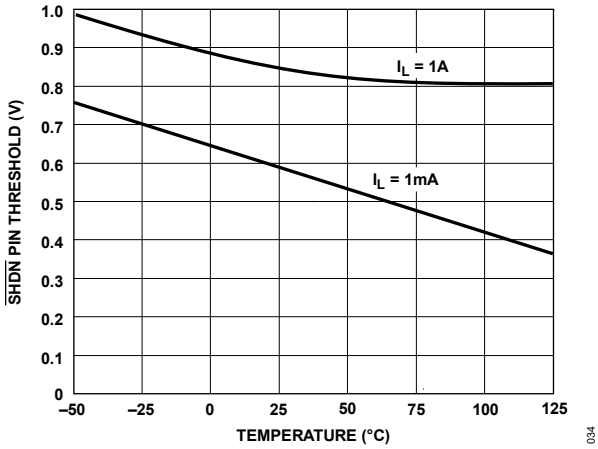


Figure 14. $\overline{SHDN}$ Pin Threshold (Off-to-On)

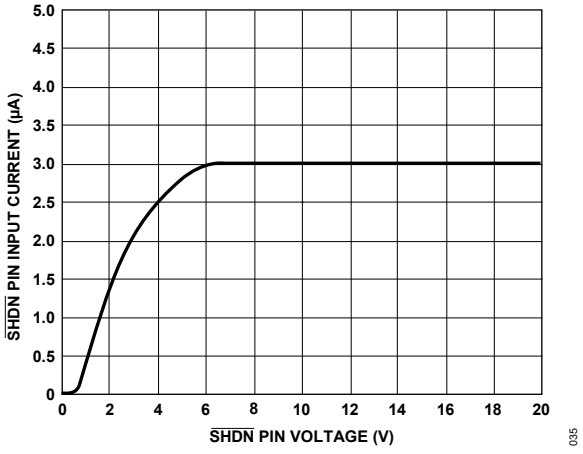


Figure 15. $\overline{SHDN}$ Pin Input Current

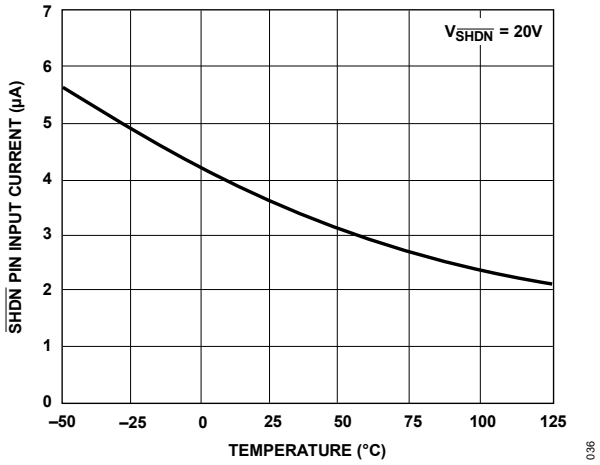


Figure 16. $\overline{SHDN}$ Pin Input Current

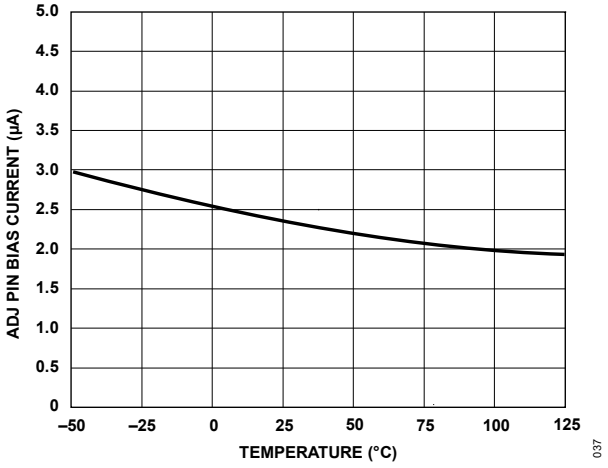


Figure 17. ADJ Pin Bias Current

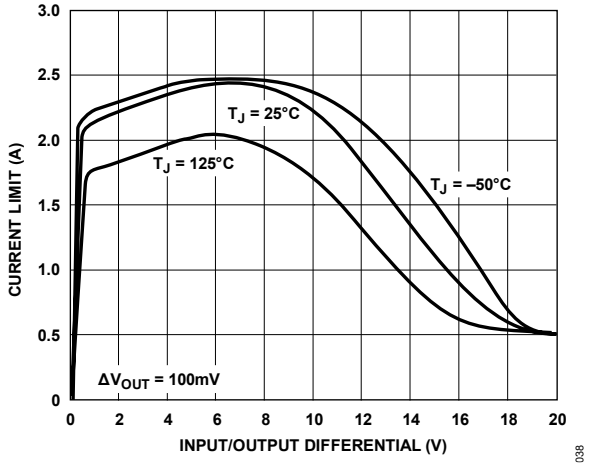


Figure 18. Current Limit vs. Input/Output Differential at Various Temperature

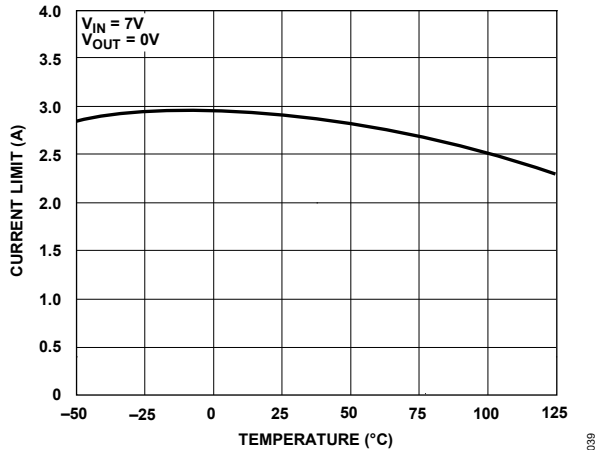


Figure 19. Current Limit vs. Temperature

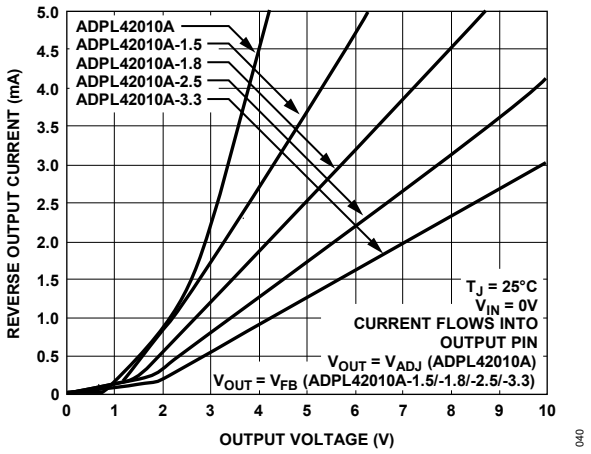


Figure 20. Reverse Output Current

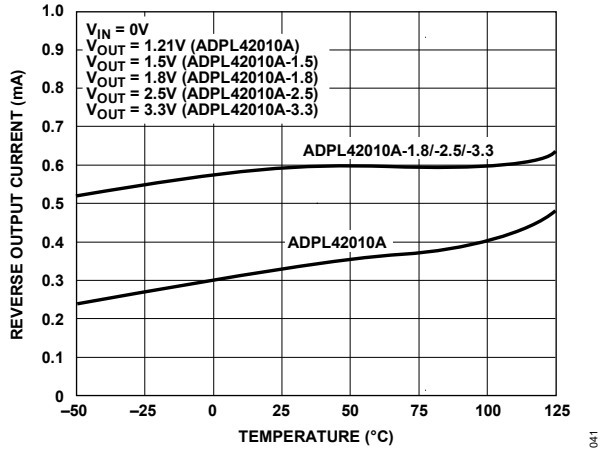


Figure 21. Reverse Output Current

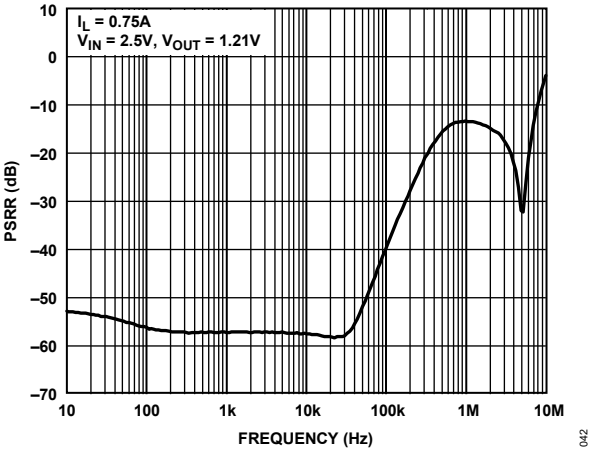


Figure 22. Power-Supply Rejection Ratio (PSRR) vs. Frequency

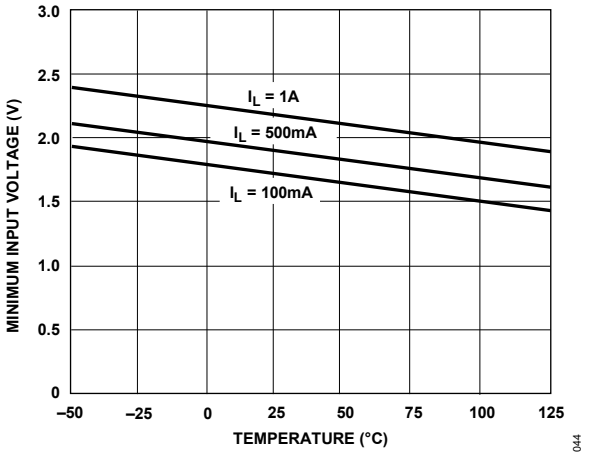


Figure 23. ADPL42010A Minimum Input Voltage

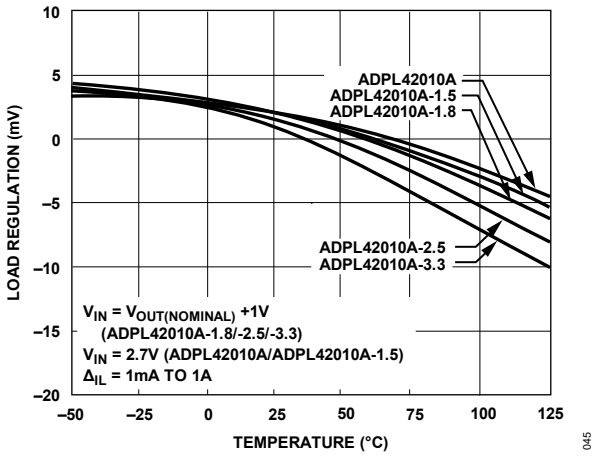


Figure 24. Load Regulation

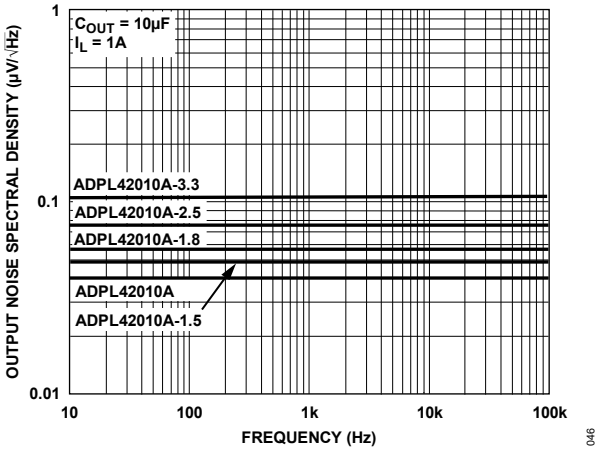


Figure 25. Output Noise Spectral Density

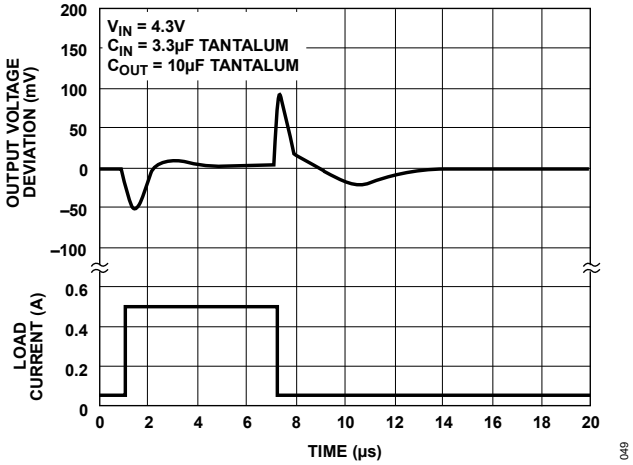


Figure 26. ADPL42010A-3.3 Transient Response

APPLICATIONS INFORMATION

The ADPL42010A series are 1A low dropout regulators optimized for fast transient response. The devices are capable of supplying 1A at a dropout voltage of 400mV. The low operating quiescent current (1mA) drops to less than 1µA in shutdown. In addition to the low quiescent current, the ADPL42010A regulators incorporate several protection features, which make them ideal for use in battery-powered systems. The devices are protected against both reverse input and reverse output voltages. In battery backup applications where the output can be held up by a backup battery when the input is pulled to ground, the ADPL42010A acts as it has a diode in series with its output and prevents reverse current flow. Additionally, in dual supply applications where the regulator load is returned to a negative supply, the output can be pulled below ground by as much as 20V and still allow the device to start and operate.

Adjustable Operation

The adjustable version of the ADPL42010A has an output voltage range of 1.21V to 20V. The output voltage is set by the ratio of two external resistors, as shown in *Figure 27*. The device serves the output to maintain the voltage at the ADJ pin at 1.21V referenced to ground. The current in R1 is then equal to 1.21V/R1 and the current in R2 is the current in R1 plus the ADJ pin bias current. The ADJ pin bias current, 3µA at 25°C, flows through R2 into the ADJ pin. The output voltage can be calculated using the formula in *Figure 27*. The value of R1 should be less than 4.17k to minimize errors in the output voltage caused by the ADJ pin bias current. Note that in shutdown, the output is turned off and the divider current is zero.

The adjustable device is tested and specified with the ADJ pin connected to the OUT pin for an output voltage of 1.21V. Specifications for output voltages greater than 1.21V are proportional to the ratio of the required output voltage to 1.21V: V_{OUT}/1.21V. For example, load regulation for an output current change of 1mA to 1A is –3mV typical at V_{OUT} = 1.21V. At V_{OUT} = 5V, load regulation is:

$$(5V/1.21V) \times (-3mV) = -12.4mV$$

Output Capacitors and Stability

The ADPL42010A regulator is a feedback circuit. Similar to any feedback circuit, frequency compensation is needed to make it stable. For the ADPL42010A, the frequency compensation is both internal and external due to the output capacitor. The size of the output capacitor, the type of the output capacitor, and the ESR of the particular output capacitor all affect the stability.

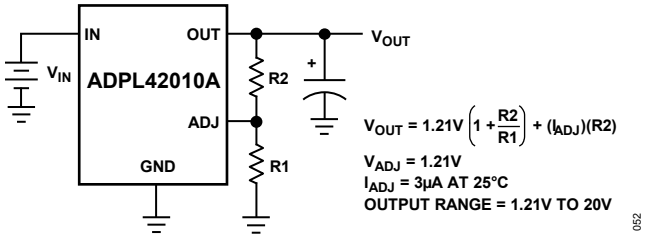


Figure 27. Adjustable Operation

In addition to stability, the output capacitor also affects the high frequency transient response. The regulator loop has a finite bandwidth. For the high-frequency transient loads, recovery from a transient is a combination of the output capacitor and the bandwidth of the regulator. The ADPL42010A is designed to be easy to use and accept a wide variety of output capacitors. However, the frequency compensation is affected by the output capacitor and optimum frequency stability may require some ESR, especially with ceramic capacitors.

For ease of use, low ESR polytantalum capacitors (POSCAP) are a good choice for both the transient response and stability of the regulator. These capacitors have intrinsic ESR that improves the stability. Ceramic capacitors have extremely low ESR, and while they are a good choice in many cases, placing a small series resistance element sometimes achieves optimum stability and minimize ringing. In all cases, a minimum of 10µF is required while the maximum 3Ω ESR is allowed.

The place where ESR is most helpful with ceramics is at low output voltages. At low output voltages, below 2.5V, some ESR prevents oscillation when ceramic output capacitors are used. Also, some ESR allows a smaller capacitor value to be used. When small signal ringing occurs with ceramics due to insufficient ESR, adding ESR or increasing the capacitor value improves the stability and reduces the ringing. *Table 4* gives the minimum values of ESR to prevent oscillation during load transient testing. Additional ESR or capacitance are necessary for adequate margin.

Table 4. Capacitor Minimum ESR

V_{OUT}	10µF	22µF	47µF	100µF
1.2V	20mΩ	15mΩ	10mΩ	5mΩ
1.5V	20mΩ	15mΩ	10mΩ	5mΩ
1.8V	15mΩ	10mΩ	10mΩ	5mΩ
2.5V	5mΩ	5mΩ	5mΩ	5mΩ
3.3V	0mΩ	0mΩ	0mΩ	5mΩ
≥5V	0mΩ	0mΩ	0mΩ	0mΩ

Figure 28 to *Figure 30* show the effect of ESR on the transient response of the regulator. These scope captures show the transient response for the ADPL42010A at a worst-case condition when the output voltage is 1.2V. As *Table 4* shows, higher output voltages require proportionally less ESR and output capacitance for stability. The output load conditions are the same for *Figure 28* to *Figure 30*. In all cases, there is a DC load of 500mA. The load steps up to 1A at the first transition and steps back to 500mA at the second transition. Load transient testing on actual hardware is a good way to ensure circuit stability, especially if the output voltage is 5V or less or the output network is inductive due to filtering or lead length.

In *Figure 28*, a minimum ESR of 50mΩ is required for adequate stability when C_{OUT} is 10µF. In *Figure 29*, a minimum ESR of 10mΩ is required for adequate stability when C_{OUT} is 100µF. Capacitors with added ESR can be combined with low ESR ceramic capacitors to achieve both good high frequency bypassing and fast settling time. *Figure 30* shows the improvement in transient response that can be seen when a parallel combination of a 10µF ceramic and a 100µF capacitor in series with 40mΩ are used.

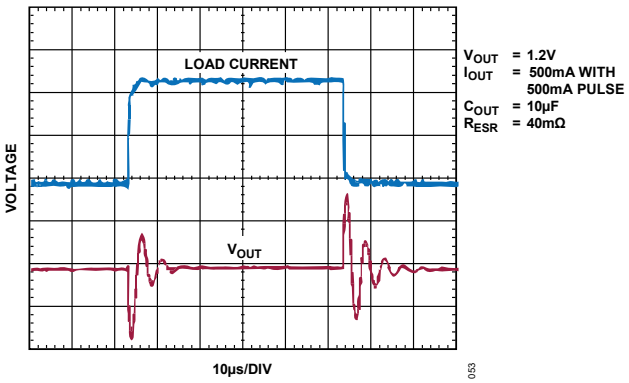


Figure 28. Transient Response at 1.2V_{OUT} with 10µF C_{OUT} and 40mΩ R_{ESR}

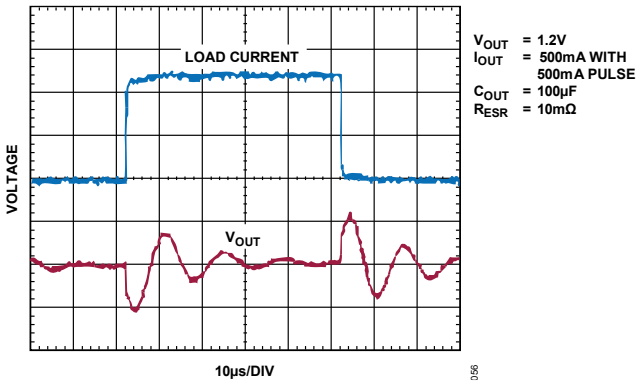


Figure 29. Transient Response at 1.2V_{OUT} with 100µF C_{OUT} and 10mΩ R_{ESR}

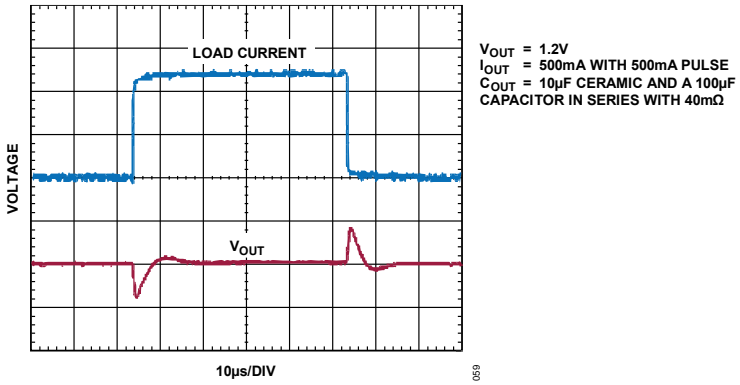


Figure 30. Effect of ESR on Transient Response of the Regulator

Tantalum and Polytantalum Capacitors

There is a variety of tantalum capacitor types available, with a wide range of ESR specifications. Older types have ESR specifications in the hundreds of mΩ to several Ohms. Some newer types of polytantalum with multi-electrodes have maximum ESR specifications as low as 5mΩ. In general the lower the ESR specification, the larger the size and the higher the price. Polytantalum capacitors have better surge capability than older types and generally lower ESR. Some types such as the Sanyo TPE and TPB series have ESR specifications in the 20mΩ to 50mΩ range, which provide near optimum transient response.

Aluminum Electrolytic Capacitors

Aluminum electrolytic capacitors can also be used with the ADPL42010A. These capacitors can also be used in conjunction with ceramic capacitors. These tend to be the cheapest and lowest performance type of capacitors. The user must take care while selecting these capacitors as some types can have ESR which can easily exceed the 3Ω maximum value.

Ceramic Capacitors

Extra consideration must be given to the use of ceramic capacitors. Ceramic capacitors are manufactured with a variety of dielectrics, each with different behavior over temperature and applied voltage. The most common dielectrics used are Z5U, Y5V, X5R, and X7R. The Z5U and Y5V dielectrics are good for providing high capacitances in a small package, but exhibit strong voltage and temperature coefficients, as shown in *Figure 31* and *Figure 32*. When

used with a 5V regulator, a 10µF Y5V capacitor can exhibit an effective value as low as 1µF to 2µF over the operating temperature range. The X5R and X7R dielectrics result in more stable characteristics and are more suitable for use as the output capacitor. The X7R type has better stability across temperature, while the X5R is less expensive and is available in higher values.

Voltage and temperature coefficients are not the only sources of problems. Some ceramic capacitors have a piezoelectric response. A piezoelectric device generates voltage across its terminals due to mechanical stress, similar to the way a piezoelectric accelerometer or microphone works. For a ceramic capacitor, the stress can be induced by vibrations in the system or thermal transients.

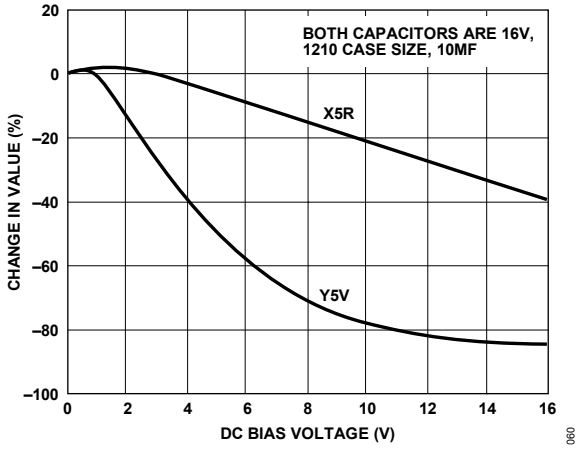


Figure 31. Ceramic Capacitor DC Bias Characteristics

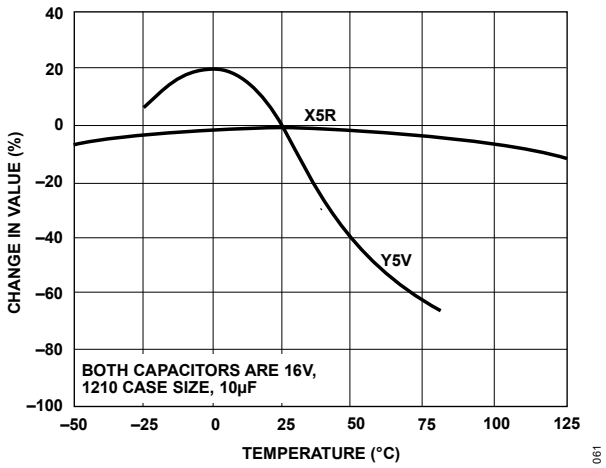


Figure 32. Ceramic Capacitor Temperature Characteristics

Free Resistance with PC Traces

The resistance values shown in *Table 5* can easily be made by putting an actual resistor in series with the capacitor, or by using a small section of PC trace in series with the output capacitor. The wide range of non-critical ESR makes it easy to use PC trace. The trace width should be sized to handle the RMS ripple current associated with the load. The output capacitor only sources or sinks current for a few microseconds during fast output current transitions. There is no DC current in the output capacitor. Worst case ripple current occurs if the output load is a high frequency (>100kHz) square wave with a high peak value and fast edges (<1µs). Measured RMS value for this case is 0.5 times

the peak-to-peak current change. Slower edges or lower frequency significantly reduces the RMS ripple current in the capacitor.

Table 5. PC Trace Resistors

	10mΩ	20mΩ	30mΩ
0.5oz CU	Width: 0.011in (0.28mm) Length: 0.102in (2.6mm)	Width: 0.011in (0.28mm) Length: 0.204in (5.2mm)	Width: 0.011in (0.28mm) Length: 0.307in (7.8mm)
1.0oz CU	Width: 0.006in (0.15mm) Length: 0.110in (2.8mm)	Width: 0.006in (0.15mm) Length: 0.220in (5.6mm)	Width: 0.006in (0.15mm) Length: 0.330in (8.4mm)
2.0oz CU	Width: 0.006in (0.15mm) Length: 0.224in (5.7mm)	Width: 0.006in (0.15mm) Length: 0.450in (11.4mm)	Width: 0.006in (0.15mm) Length: 0.670in (17mm)

This resistor should be made using one of the inner layers of the PC board which are well defined. The resistivity is determined primarily by the sheet resistance of the copper laminate with no additional plating steps. *Table 5* gives some sizes for 0.75A RMS current for various copper thicknesses. For more details on resistors made from PC traces, refer to the *Appendix A* of the Application Note 69*: LT1575 UltraFast Linear Controller Makes Fast Transient Response Power Supplies*.

Overload Recovery

Similar to many IC power regulators, the ADPL42010A-X has a safe operating area (SOA) protection. The SOA protection decreases the current limit as input-to-output voltage increases and keeps the power transistor inside a safe operating region for all values of input-to-output voltage. The protection is designed to provide some output current at all values of input-to-output voltage up to the device breakdown. When power is first turned on, as the input voltage rises, the output follows the input, which allows the regulator to start up into very heavy loads. During the start-up, as the input voltage is rising, the input-to-output voltage differential is small, which allows the regulator to supply large output currents. With a high input voltage, a problem can occur wherein removal of an output short does not allow the output voltage to recover. Other regulators, such as the *LT1085*, also exhibit this phenomenon, so it is not unique to the ADPL42010A-X.

The problem occurs with a heavy output load when the input voltage is high and the output voltage is low. Common situations are immediately after the removal of a short-circuit or when the $\overline{\text{SHDN}}$ pin is pulled high after the input voltage has already been turned on. The load line for such a load may intersect the output current curve at two points. If this happens, there are two stable output operating points for the regulator. With this double intersection, the input power supply may need to be cycled down to zero and brought up again to make the output recover.

Output Voltage Noise

The ADPL42010A regulators have been designed to provide low output voltage noise over the 10Hz to 100kHz bandwidth while operating at full load. Output voltage noise is typically 70nV/√Hz over this frequency bandwidth for the ADPL42010A (adjustable version). For higher output voltages (generated by using a resistor divider), the output voltage noise gains up accordingly. This results in RMS noise over the 10Hz to 100kHz bandwidth of 22µVRMS for the ADPL42010A increasing to 83µVRMS for the ADPL42010A-3.3.

Higher values of output voltage noise may be measured when care is not exercised with regard to circuit layout and testing. Crosstalk from nearby traces can induce unwanted noise onto the output of the ADPL42010A-X. Power supply ripple rejection must also be considered, the ADPL42010A regulators do not have unlimited power supply rejection and pass a small portion of the input noise through to the output.

Protection Features

The ADPL42010A incorporates several protection features, which makes it ideal for use in battery-powered circuits. In addition to the normal protection features associated with monolithic regulators, such as current limiting and thermal limiting, the devices are protected against reverse input voltages, reverse output voltages, and reverse voltages from output to input.

Current limit protection and thermal overload protection are intended to protect the device against current overload conditions at the output of the device. For normal operation, the junction temperature should not exceed 125°C.

The input of the device withstands reverse voltages of 20V. Current flow into the device is limited to less than 1mA (typically less than 100µA) and no negative voltage appears at the output. The device protects both itself and the load. This provides protection against batteries that can be plugged in backward.

The output of the ADPL42010A can be pulled below ground without damaging the device. If the input is left open circuit or grounded, the output can be pulled below ground by 20V. For fixed voltage versions, the output acts as a large resistor, typically 5k or higher, limiting current flow to typically less than 600µA. For adjustable versions, the output acts as an open circuit, no current flows out of the pin. If the input is powered by a voltage source, the output sources the short-circuit current of the device and protects itself by thermal limiting. In this case, grounding the $\overline{\text{SHDN}}$ pin turns off the device and stop the output from sourcing the short-circuit current.

The ADJ pin of the adjustable device can be pulled above or below ground by as much as 7V without damaging the device. If the input is left open circuit or grounded, the ADJ pin acts as an open circuit when pulled below ground and as a large resistor (typically 5k) in series with a diode when pulled above ground.

In situations where the ADJ pin is connected to a resistor divider that pulls the ADJ pin above its 7V clamp voltage if the output is pulled high, the ADJ pin input current must be limited to less than 5mA. For example, a resistor divider is used to provide a regulated 1.5V output from the 1.21V reference when the output is forced to 20V. The top resistor of the resistor divider must be chosen to limit the current into the ADJ pin to less than 5mA when the ADJ pin is at 7V. The 13V difference between OUT and ADJ pins divided by the 5mA maximum current into the ADJ pin yields a minimum top resistor value of 2.6k.

In circuits where a backup battery is required, several different input/output conditions can occur. The output voltage may be held up while the input is either pulled to ground, pulled to some intermediate voltage, or is left open circuit. Current flow back into the output follows the curve, as shown in *Figure 33*.

When the IN pin of the ADPL42010A is forced below the OUT pin or the OUT pin is pulled above the IN pin, input current typically drops to less than 2µA. This can happen if the input of the device is connected to a discharged (low voltage) battery and the output is held up by either a backup battery or a second regulator circuit. The state of the $\overline{\text{SHDN}}$ pin have no effect on the reverse output current when the output is pulled above the input.

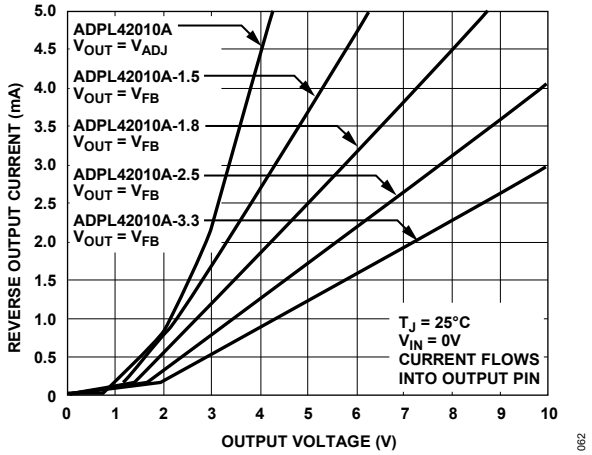


Figure 33. Reverse Output Current

Thermal Considerations

The power handling capability of the device is limited by the maximum rated junction temperature (125°C). The power dissipated by the device is made up of two components:

1. Output current multiplied by the input/output voltage differential: $(I_{OUT}) \times (V_{IN} - V_{OUT})$.

2. And GND pin current multiplied by the input voltage: $(I_{GND}) \times (V_{IN})$.

For the GND pin current, see *Figure 12*. Power dissipation is equal to the sum of the two components listed above.

The ADPL42010A has an internal thermal limiting designed to protect the device during overload conditions. For continuous normal conditions, the maximum junction temperature rating of 125°C must not be exceeded.

PRINTED CIRCUIT BOARD (PCB) LAYOUT CONSIDERATIONS

It is important to give careful consideration to all sources of thermal resistance from junction-to-ambient when designing the PCB layout for the ADPL42010A. Additional heat sources mounted nearby must also be considered. Heat dissipation from the package can be improved by increasing the amount of copper directly attached to the pins and exposed pad of the ADPL42010A. Thermal vias may be used to connect the exposed pad to copper on the opposite side of the PCB. However, a point of diminishing returns is eventually reached, beyond which an increase in the copper size does not yield significant heat dissipation benefits.

It is also important for electrical performance to give careful consideration to component placement and ground layer placement when designing the PCB layout for the ADPL42010A. Place the input capacitor as close as possible to the VIN and GND pins. Place the output capacitor as close as possible to the VOUT and GND pins. Place the input and output capacitors on the same side of the PCB as the ADPL42010A with their ground terminals close to each other. The input capacitor, output capacitor, and ADPL42010A grounds all connect on one side of the device, while grounds for control signals connect to the ADPL42010A on the other side of the device. Utilize an unbroken ground plane on the PCB layer that is adjacent to the top or bottom PCB layer with the ADPL42010A. *Figure 34* shows a recommended layout that delivers the full performance of the regulator.

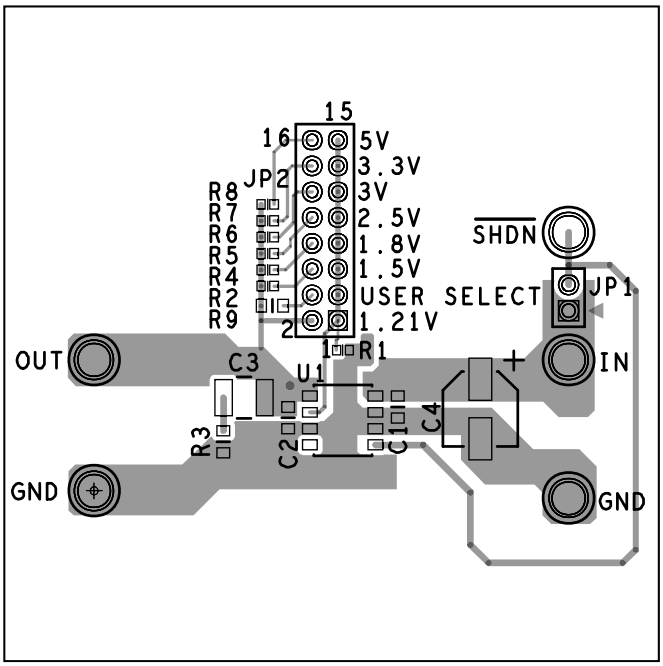


Figure 34. ADPL42010A Example PCB Layout

OUTLINE DIMENSIONS

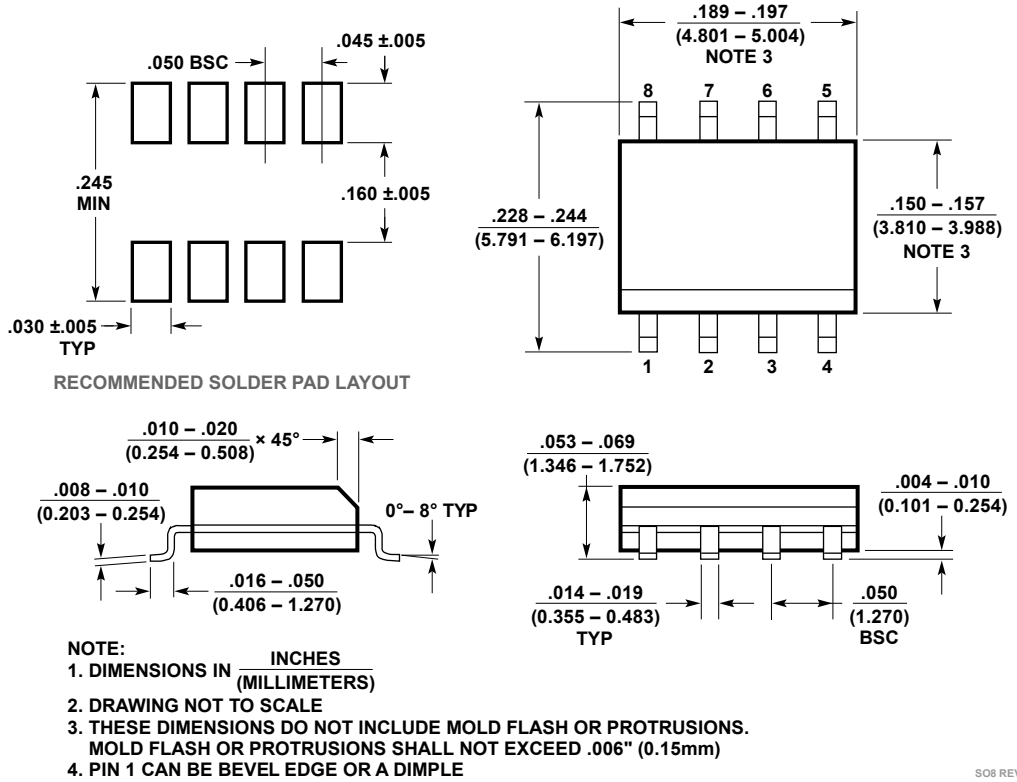


Figure 35. S8 Package
8-Lead Plastic Small Outline (Narrow .150inch)
(Reference LTC DWG # 05-08-1610 Rev G)

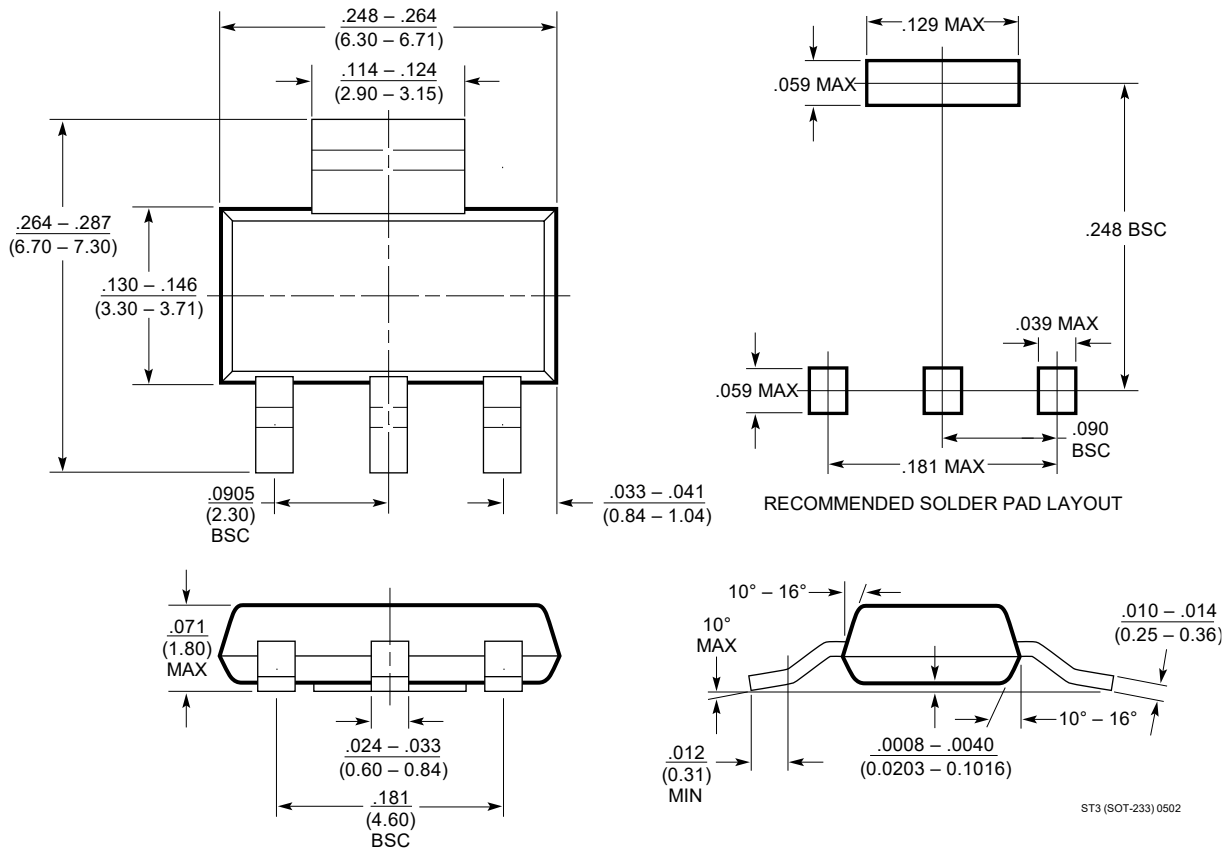


Figure 36. ST Package
3-Lead Plastic SOT-223
(Reference LTC DWG # 05-08-1630)

ORDERING GUIDE

Table 6. Ordering Guide

MODEL[1, 2]	TEMPERATURE RANGE	PACKAGE DESCRIPTION	PACKAGE OPTION
ADPL42010ABKZZ-2.5	–40°C to +125°C	3-Lead Plastic SOT-223	05-08-1630
ADPL42010ABKZZ-2.5-RL	–40°C to +125°C	3-Lead Plastic SOT-223	05-08-1630
ADPL42010ABKZZ-3.3	–40°C to +125°C	3-Lead Plastic SOT-223	05-08-1630
ADPL42010ABKZZ-3.3-RL	–40°C to +125°C	3-Lead Plastic SOT-223	05-08-1630
ADPL42010ABRCZ	–40°C to +125°C	8-Lead Plastic SO	05-08-1610
ADPL42010ABRCZ-RL	–40°C to +125°C	8-Lead Plastic SO	05-08-1610
ADPL42010ABRCZ-1.5	–40°C to +125°C	8-Lead Plastic SO	05-08-1610
ADPL42010ABRCZ-1.5-RL	–40°C to +125°C	8-Lead Plastic SO	05-08-1610
ADPL42010ABRCZ-1.8	–40°C to +125°C	8-Lead Plastic SO	05-08-1610
ADPL42010ABRCZ-1.8-RL	–40°C to +125°C	8-Lead Plastic SO	05-08-1610
ADPL42010ABRCZ-2.5	–40°C to +125°C	8-Lead Plastic SO	05-08-1610
ADPL42010ABRCZ-2.5-RL	–40°C to +125°C	8-Lead Plastic SO	05-08-1610
ADPL42010ABRCZ-3.3	–40°C to +125°C	8-Lead Plastic SO	05-08-1610
ADPL42010ABRCZ-3.3-RL	–40°C to +125°C	8-Lead Plastic SO	05-08-1610

[1]Z = RoHS Compliant Part.

[2]RL = Tape and Reel.

Table 7. Output Voltage Options

MODEL[1, 2]	OUTPUT VOLTAGE (V)
ADPL42010ABRCZ	Adjustable (1.21)
ADPL42010ABRCZ-1.5, ADPL42010ABRCZ-1.5-RL	1.5
ADPL42010ABRCZ-1.8, ADPL42010ABRCZ-1.8-RL	1.8
ADPL42010ABRCZ-2.5, ADPL42010ABKZZ-2.5, ADPL42010ABRCZ-2.5-RL, ADPL42010ABKZZ-2.5-RL	2.5
ADPL42010ABRCZ-3.3, ADPL42010ABKZZ-3.3, ADPL42010ABKZZ-3.3-RL, ADPL42010ABRCZ-3.3-RL	3.3

[1]Z = RoHS Compliant Part.

[2]RL = Tape and Reel.

Table 8. Evaluation Boards

MODEL[1, 2]	PACKAGE DESCRIPTION
EVAL-ADPL42010AZ	8-Lead SO Package Evaluation Board

[1]Z = RoHS Compliant Part

[2]The evaluation board is preconfigured with an adjustable ADPL42010A.

REVISION HISTORY

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	12/25	Initial release	—
A	9/26	Updated Figures 28–30.	18

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