

# DC to 31 GHz, GaAs, pHEMT, 2 W Power Amplifier

## FEATURES

- Wideband, internally-matched, RF power amplifier
- DC-coupled input and output
- Integrated RF power detector
- Integrated temperature sensor
- Gain: 12.5 dB typical at 2 GHz to 16 GHz
- OP1dB: 33 dBm typical at 2 GHz to 16 GHz
- $P_{SAT}$ : 34 dBm typical at 2 GHz to 16 GHz
- OIP3: 45 dBm typical at 2 GHz to 16 GHz
- 32-Lead, 5.00 mm  $\times$  5.00 mm, LFCSP\_CAV package

## APPLICATIONS

- ▶ Electronic warfare
- ▶ Radar
- ▶ Test and measurement equipment

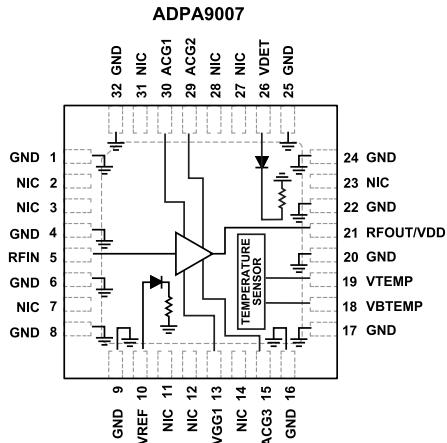
## GENERAL DESCRIPTION

The ADPA9007 is a 2 W, RF power amplifier that operates from DC to 31 GHz. The RF input and output are internally-matched and DC-coupled. The ADPA9007 includes an integrated temperature-compensated RF power detector and an integrated temperature sensor.

The ADPA9007 amplifier provides a gain of 12.5 dB, an output power for 1 dB compression (OP1dB) of 33 dBm, and an output third-order intercept (OIP3) of 45 dBm from 2 GHz to 16 GHz. The amplifier operates from a typical supply voltage of 15 V and has a 500 mA typical quiescent bias current, which is adjustable.

The ADPA9007 is fabricated on a gallium arsenide (GaAs), pseudomorphic high electron mobility transistor (pHEMT) process. The amplifier is housed in an RoHS-compliant, 32-Lead, 5 mm × 5 mm, lead frame chip scale package, premolded cavity [[LFCSP\\_CAV](#)] and is specified for operation from -40°C to +85°C.

## FUNCTIONAL BLOCK DIAGRAM



**Figure 1. Functional Block Diagram**

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**REVISION HISTORY****6/2025—Rev. 0 to Rev. A**

Change to Title.....	1
Added 28 GHz to 31 GHz Frequency Range Section and Table 6; Renumbered Sequentially.....	5
Changes to Typical Performance Characteristics Section.....	9

**12/2023—Revision 0: Initial Version**

## SPECIFICATIONS

## 0.05 GHZ TO 2 GHZ FREQUENCY RANGE

$T_{CASE} = 25^\circ\text{C}$ , supply voltage ( $V_{DD} = 15\text{ V}$ ), and quiescent drain current ( $I_{DQ} = 500\text{ mA}$ ), unless otherwise noted. Adjust the gate voltage ( $V_{GG1}$ ) from  $-1.5\text{ V}$  to  $0\text{ V}$  to achieve  $I_{DQ} = 500\text{ mA}$  typical.

Table 1. 0.05 GHz to 2 GHz Frequency Range

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
FREQUENCY RANGE		0.05	2		GHz
GAIN		11	13		dB
Flatness			$\pm 1.05$		dB
Variation over Temperature			0.02		$\text{dB}/^\circ\text{C}$
NOISE FIGURE		10			dB
RETURN LOSS					
Input		14			dB
Output		15			dB
OUTPUT					
OP1dB		29	31		dBm
Saturated Output Power ( $P_{SAT}$ )			34		dBm
OIP3	Output power ( $P_{OUT}$ ) per tone = $16\text{ dBm}$ with $1\text{ MHz}$ tone spacing		43		dBm
OIP2	$P_{OUT}$ per tone = $16\text{ dBm}$ with $1\text{ MHz}$ tone spacing		48		dBm
SUPPLY					
$I_{DQ}$	Adjust $V_{GG1}$ to achieve $I_{DQ} = 500\text{ mA}$ typical		500		mA
$V_{DD}$		10	15		V

## 2 GHZ TO 16 GHZ FREQUENCY RANGE

$T_{CASE} = 25^\circ\text{C}$ ,  $V_{DD} = 15\text{ V}$ , and  $I_{DQ} = 500\text{ mA}$ , unless otherwise noted. Adjust  $V_{GG1}$  from  $-1.5\text{ V}$  to  $0\text{ V}$  to achieve  $I_{DQ} = 500\text{ mA}$  typical.

Table 2. 2 GHz to 16 GHz Frequency Range

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
FREQUENCY RANGE		2	16		GHz
GAIN		10.5	12.5		dB
Flatness			$\pm 0.26$		dB
Variation over Temperature			0.016		$\text{dB}/^\circ\text{C}$
NOISE FIGURE		4			dB
RETURN LOSS					
Input		13			dB
Output		15			dB
OUTPUT					
OP1dB		31	33		dBm
$P_{SAT}$			34		dBm
OIP3	$P_{OUT}$ per tone = $16\text{ dBm}$ with $1\text{ MHz}$ tone spacing		45		dBm
OIP2	$P_{OUT}$ per tone = $16\text{ dBm}$ with $1\text{ MHz}$ tone spacing		45		dBm
SUPPLY					
$I_{DQ}$	Adjust $V_{GG1}$ to achieve $I_{DQ} = 500\text{ mA}$ typical		500		mA
$V_{DD}$		10	15		V

## SPECIFICATIONS

## 16 GHZ TO 20 GHZ FREQUENCY RANGE

$T_{CASE} = 25^\circ\text{C}$ ,  $V_{DD} = 15 \text{ V}$ , and  $I_{DQ} = 500 \text{ mA}$ , unless otherwise noted. Adjust  $V_{GG1}$  from  $-1.5 \text{ V}$  to  $0 \text{ V}$  to achieve  $I_{DQ} = 500 \text{ mA}$  typical.

Table 3. 16 GHz to 20 GHz Frequency Range

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
FREQUENCY RANGE		16	20		GHz
GAIN		10.5	12.5		dB
Flatness		$\pm 0.1$			dB
Variation over Temperature		0.002			$\text{dB}/^\circ\text{C}$
NOISE FIGURE		3.5			dB
RETURN LOSS					
Input		14			dB
Output		17			dB
OUTPUT					
OP1dB		29	31		dBm
$P_{SAT}$			33.5		dBm
OIP3	$P_{OUT}$ per tone = 16 dBm with 1 MHz tone spacing		43		dBm
OIP2	$P_{OUT}$ per tone = 16 dBm with 1 MHz tone spacing		45		dBm
SUPPLY					
$I_{DQ}$	Adjust $V_{GG1}$ to achieve $I_{DQ} = 500 \text{ mA}$ typical		500		mA
$V_{DD}$		10	15		V

## 20 GHZ TO 24 GHZ FREQUENCY RANGE

$T_{CASE} = 25^\circ\text{C}$ ,  $V_{DD} = 15 \text{ V}$ , and  $I_{DQ} = 500 \text{ mA}$ , unless otherwise noted. Adjust the  $V_{GG1}$  from  $-1.5 \text{ V}$  to  $0 \text{ V}$  to achieve  $I_{DQ} = 500 \text{ mA}$  typical

Table 4. 20 GHz to 24 GHz Frequency Range

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
FREQUENCY RANGE		20	24		GHz
GAIN		12.5			dB
Flatness		$\pm 0.008$			dB
Variation over Temperature					$\text{dB}/^\circ\text{C}$
NOISE FIGURE		4			dB
RETURN LOSS					
Input		12			dB
Output		13			dB
OUTPUT					
OP1dB		29			dBm
$P_{SAT}$		32			dBm
OIP3	$P_{OUT}$ per tone = 16 dBm with 1 MHz spacing		43		dBm
SUPPLY					
$I_{DQ}$	Adjust $V_{GG1}$ to achieve $I_{DQ} = 500 \text{ mA}$ typical		500		mA
$V_{DD}$		10	15		V

**SPECIFICATIONS****24 GHZ TO 28 GHZ FREQUENCY RANGE**

$T_{CASE} = 25^\circ\text{C}$ ,  $V_{DD} = 15 \text{ V}$ , and  $I_{DQ} = 500 \text{ mA}$ , unless otherwise noted. Adjust the  $V_{GG1}$  from  $-1.5 \text{ V}$  to  $0 \text{ V}$  to achieve  $I_{DQ} = 500 \text{ mA}$  typical.

**Table 5. 24 GHz to 28 GHz Frequency Range**

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
FREQUENCY RANGE		24		28	GHz
GAIN			12		dB
Flatness			$\pm 1.05$		dB
Variation over Temperature			0.017		
NOISE FIGURE		4.5			dB
RETURN LOSS					
Input			13		dB
Output			14		dB
OUTPUT					
OP1dB			27		dBm
$P_{SAT}$			31		dBm
OIP3	$P_{OUT}$ per tone = 16 dBm with 1 MHz tone spacing		39		dBm
SUPPLY					
$I_{DQ}$	Adjust $V_{GG1}$ to achieve $I_{DQ} = 500 \text{ mA}$ typical		500		mA
$V_{DD}$		10		15	V

**28 GHZ TO 31 GHZ FREQUENCY RANGE**

$T_{CASE} = 25^\circ\text{C}$ ,  $V_{DD} = 15 \text{ V}$ , and  $I_{DQ} = 500 \text{ mA}$ , unless otherwise noted. Adjust the  $V_{GG1}$  from  $-1.5 \text{ V}$  to  $0 \text{ V}$  to achieve  $I_{DQ} = 500 \text{ mA}$  typical.

**Table 6. 28 GHz to 31 GHz Frequency Range**

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
FREQUENCY RANGE		28		31	GHz
GAIN			10		dB
Flatness			$\pm 1$		dB
Variation over Temperature			0.017		
NOISE FIGURE		7			dB
RETURN LOSS					
Input			8		dB
Output			6.5		dB
OUTPUT					
OP1dB			23		dBm
$P_{SAT}$			27		dBm
OIP3	$P_{OUT}$ per tone = 16 dBm with 1 MHz tone spacing		35		dBm
SUPPLY					
$I_{DQ}$	Adjust $V_{GG1}$ to achieve $I_{DQ} = 500 \text{ mA}$ typical		500		mA
$V_{DD}$		10		15	V

## ABSOLUTE MAXIMUM RATINGS

Table 7. Absolute Maximum Ratings

Parameter	Rating
$V_{DD}$	16.0 V
$V_{GG1}$	-2.0 V to 0 V
RF Input Power (RFIN)	29 dBm
Continuous Power Dissipation ( $P_{DISS}$ ), $T_{CASE} = 85^\circ\text{C}$ (Derate 135 mW/ $^\circ\text{C}$ above $85^\circ\text{C}$ )	12.2 W
Temperature	
Maximum Channel	175°C
Quiescent Channel ( $T_{CASE} = 85^\circ\text{C}$ , $V_{DD} = 15$ V), $I_{DQ} = 500$ mA, and Input Power ( $P_{IN}$ ) = Off	140.5°C
Storage Range	-65°C to +150°C
Operating Range	-40°C to +85°C

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

## THERMAL RESISTANCE

Thermal performance is directly linked to printed circuit board (PCB) design and operating environment. Careful attention to PCB thermal design is required.

$\theta_{JC}$  is the junction-to-case thermal resistance (channel to exposed metal ground pad on the underside of the device).

Table 8. Thermal Resistance

Package Type	$\theta_{JC}$ <sup>1</sup>	Unit
CG-32-2	7.4	°C/W

<sup>1</sup>  $\theta_{JC}$  was determined by simulation under the following conditions: the heat transfer is due solely to thermal conduction from the channel through the ground pad to the PCB. The ground pad is held constant at 85°C operating temperature.

## ELECTROSTATIC DISCHARGE (ESD) RATINGS

The following ESD information is provided for handling of ESD-sensitive devices in an ESD-protected area only.

Human Body Model (HBM) per ANSI/ESDA/JEDEC JS-001.

## ESD Ratings for ADPA9007

Table 9. ADPA9007, 32-Lead LFCSP\_CAV

ESD Model	Withstand Threshold (V)	Class
HBM	±250	1A

## ESD CAUTION



**ESD (electrostatic discharge) sensitive device.** Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

## PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

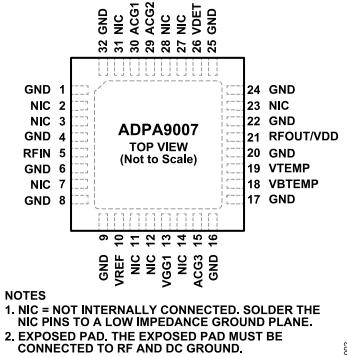


Figure 2. Pin Configuration

Table 10. Pin Function Descriptions

Pin No.	Mnemonic	Description
1, 4, 6, 8, 9, 16, 17, 20, 22, 24, 25, 32	GND	Ground. The GND pins must be connected to the RF and the DC ground. See <a href="#">Figure 3</a> for the interface schematic.
2, 3, 7, 11, 12, 14, 23, 27, 28, 31	NIC	Not Internally Connected. The NIC pins are not connected internally. However, all data shown is measured with the NIC pins connected to RF and DC ground externally.
5	RFIN	RF Input of the Amplifier. The RFIN pin is DC-coupled and matched to $50\ \Omega$ . See <a href="#">Figure 4</a> for the interface schematic.
10	VREF	Reference Diode Voltage for the Temperature Compensation of the VDET RF Output Power Measurements. The VREF pin voltage ( $V_{REF}$ ) requires the application of a DC bias voltage through an external series resistor. See <a href="#">Figure 5</a> for the interface schematic.
13	VGG1	Gate Control for the Amplifier. Attach bypass capacitors per the <a href="#">Applications Information</a> section. See the <a href="#">Power-Up Sequence</a> and <a href="#">Power-Down Sequence</a> for additional information. See <a href="#">Figure 6</a> for the interface schematic.
15	ACG3	Low Frequency Termination. Attach bypass capacitors per the <a href="#">Applications Information</a> section. See <a href="#">Figure 4</a> for the interface schematic.
18	VBTTEMP	Temperature Sensor Bias. Bias pin for biasing the integrated temperature sensor. See <a href="#">Figure 7</a> for the interface schematic.
19	VTTEMP	Integrated Temperature Sensor output. See <a href="#">Figure 7</a> for the interface schematic.
21	RFOUT/VDD	RF Output of the Amplifier. Connect the RFOUT/VDD pin to the DC bias ( $V_{DD}$ ) network to provide drain current ( $I_{DD}$ ). See <a href="#">Applications Information</a> section. See <a href="#">Figure 8</a> for the interface schematic.
26	VDET	Detector Diode Voltage to Measure the RF Output Power. Detection by the VDET pin requires the application of a DC bias voltage through an external series resistor. Used in combination with the VREF pin, the difference detector voltage ( $V_{REF} - V_{DET}$ ) is a temperature compensated DC voltage proportional to the RF output power. See <a href="#">Figure 8</a> for the interface schematic.
29	ACG2	Low Frequency Termination. Attach bypass capacitors per the <a href="#">Applications Information</a> section. See <a href="#">Figure 8</a> for the interface schematic.
30	ACG1	Low Frequency Termination. Attach bypass capacitor per the <a href="#">Applications Information</a> section. See <a href="#">Figure 8</a> for the interface schematic.
	EPAD	Exposed Pad. The exposed pad must be connected to the RF and the DC ground.

## PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

## INTERFACE SCHEMATICS



Figure 3. GND Interface Schematic

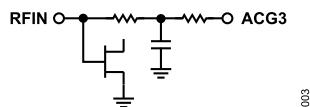


Figure 4. RFIN and ACG3 Interface Schematic

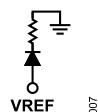


Figure 5. VREF Interface Schematic

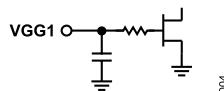


Figure 6. VGG1 Interface Schematic



Figure 7. VTEMP and VBTEMP Interface Schematic

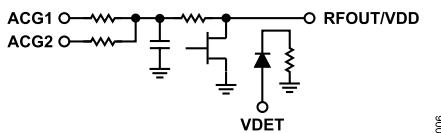


Figure 8. ACG1, ACG2, RFOUT/VDD, and VDET Interface Schematic

## TYPICAL PERFORMANCE CHARACTERISTICS

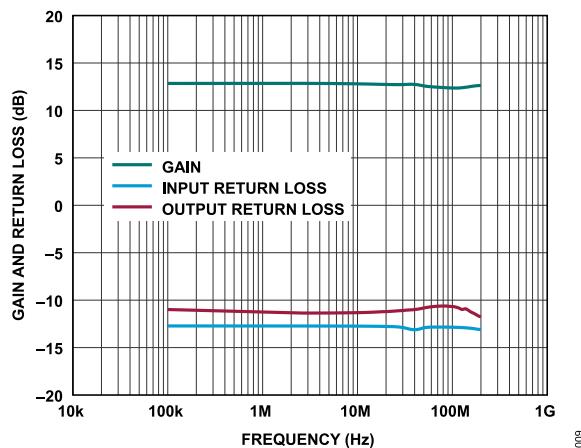


Figure 9. Gain and Return Loss vs. Frequency, 100 kHz to 200 MHz,  
 $V_{DD} = 15 \text{ V}$ ,  $I_{DQ} = 500 \text{ mA}$

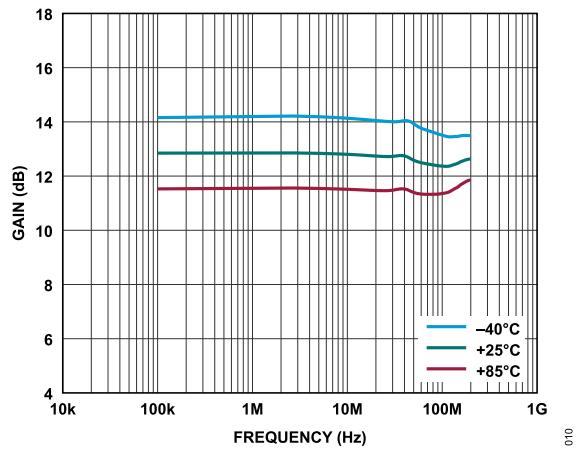


Figure 10. Gain vs. Frequency for Various Temperatures, 100 kHz to 200 MHz,  
 $V_{DD} = 15 \text{ V}$ ,  $I_{DQ} = 500 \text{ mA}$

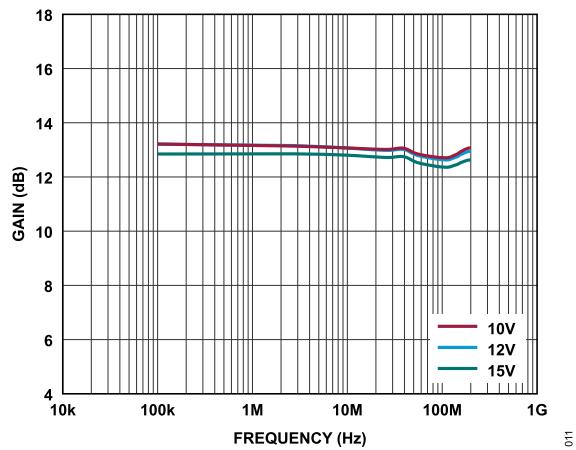


Figure 11. Gain vs. Frequency for Various  $V_{DD}$  Values, 100 kHz to 200 MHz,  
 $I_{DQ} = 500 \text{ mA}$

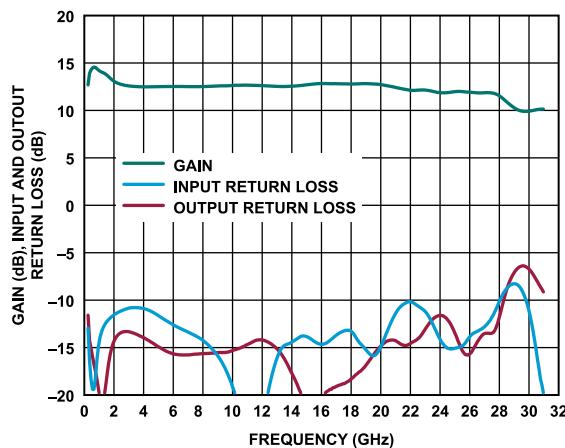


Figure 12. Gain and Return Loss vs. Frequency, 200 MHz to 31 GHz,  
 $V_{DD} = 15 \text{ V}$ ,  $I_{DQ} = 500 \text{ mA}$

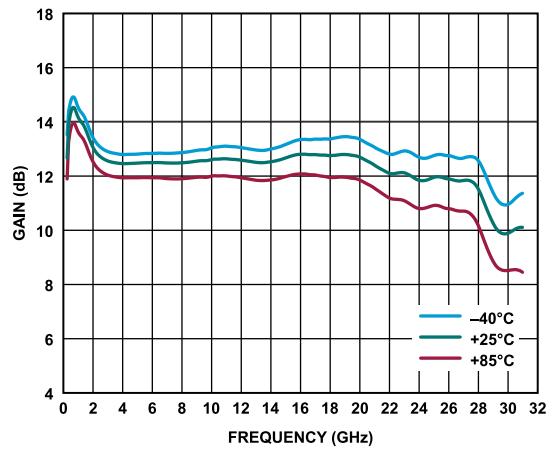


Figure 13. Gain vs. Frequency for Various Temperatures, 200 MHz to 31 GHz,  
 $V_{DD} = 15 \text{ V}$ ,  $I_{DQ} = 500 \text{ mA}$

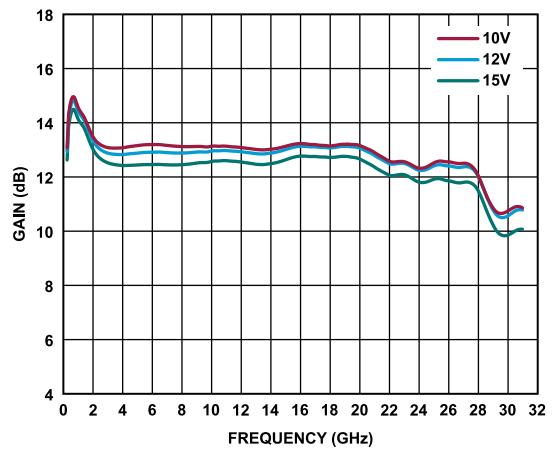


Figure 14. Gain vs. Frequency for Various  $V_{DD}$  Values, 200 MHz to 31 GHz,  
 $I_{DQ} = 500 \text{ mA}$

## TYPICAL PERFORMANCE CHARACTERISTICS

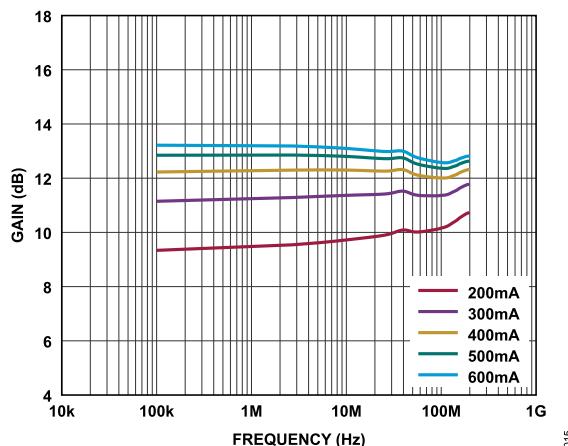


Figure 15. Gain vs. Frequency for Various  $I_{DQ}$  Values, 100 kHz to 200 MHz,  
 $V_{DD} = 15$  V

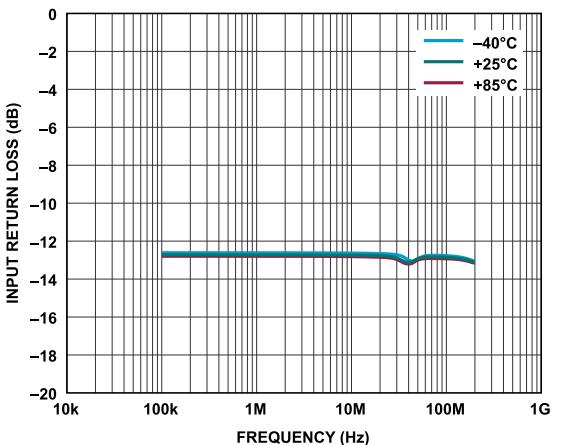


Figure 16. Input Return Loss vs. Frequency for Various Temperatures,  
 $100$  kHz to  $200$  MHz,  $V_{DD} = 15$  V,  $I_{DQ} = 500$  mA

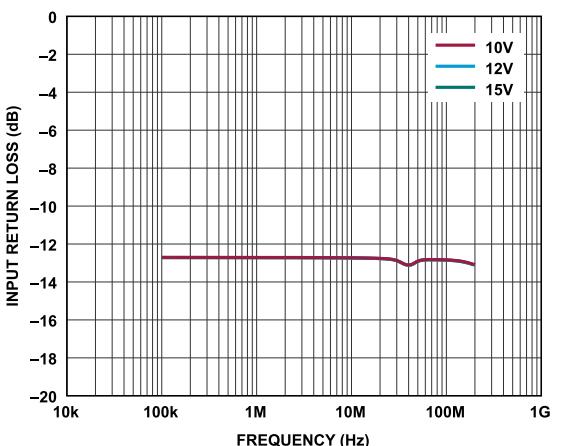


Figure 17. Input Return Loss vs. Frequency for Various  $V_{DD}$  Values,  
 $100$  kHz to  $200$  MHz,  $I_{DQ} = 500$  mA

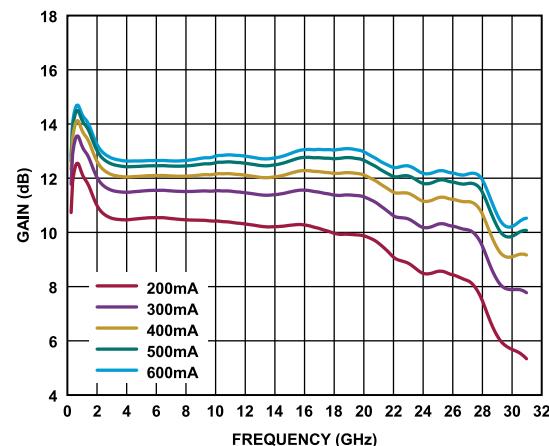


Figure 18. Gain vs. Frequency for Various  $I_{DQ}$  Values, 200 MHz to 31 GHz,  
 $V_{DD} = 15$  V

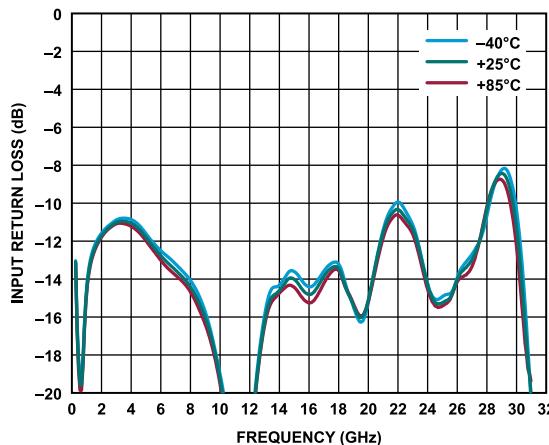


Figure 19. Input Return Loss vs. Frequency for Various Temperatures,  
 $200$  MHz to  $31$  GHz,  $V_{DD} = 15$  V,  $I_{DQ} = 500$  mA

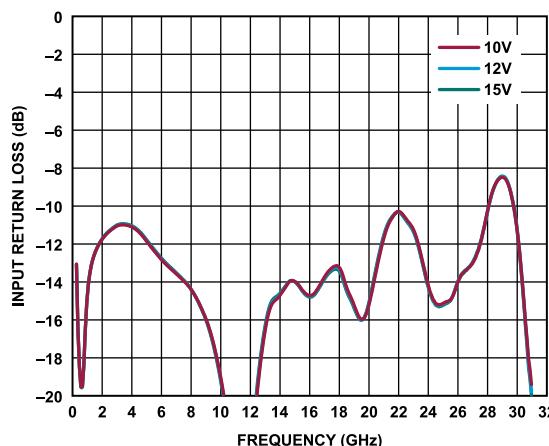


Figure 20. Input Return Loss vs. Frequency for Various  $V_{DD}$  Values,  
 $200$  MHz to  $31$  GHz,  $I_{DQ} = 500$  mA

## TYPICAL PERFORMANCE CHARACTERISTICS

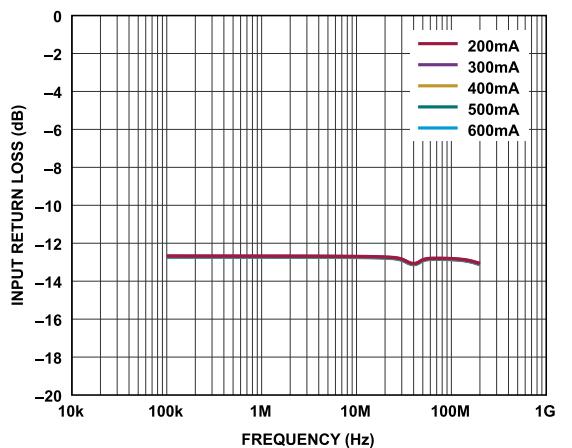


Figure 21. Input Return Loss vs. Frequency for Various  $I_{DQ}$  Values,  
100 kHz to 200 MHz,  $V_{DD} = 15$  V

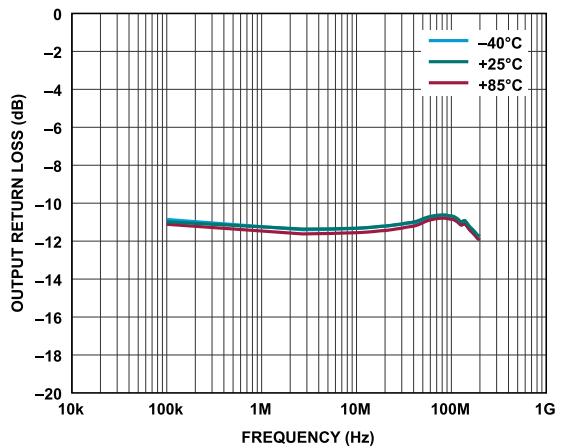


Figure 22. Output Return Loss vs. Frequency for Various Temperatures,  
100 kHz to 200 MHz,  $V_{DD} = 15$  V,  $I_{DQ} = 500$  mA

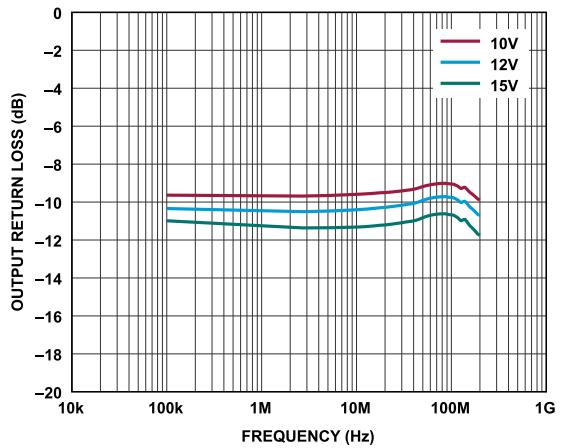


Figure 23. Output Return Loss vs. Frequency for Various  $V_{DD}$  Values,  
100 kHz to 200 MHz,  $I_{DQ} = 500$  mA

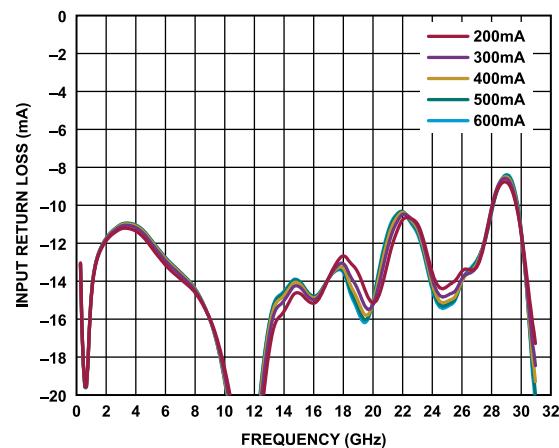


Figure 24. Input Return Loss vs. Frequency for Various  $I_{DQ}$  Values,  
200 MHz to 31 GHz,  $V_{DD} = 15$  V

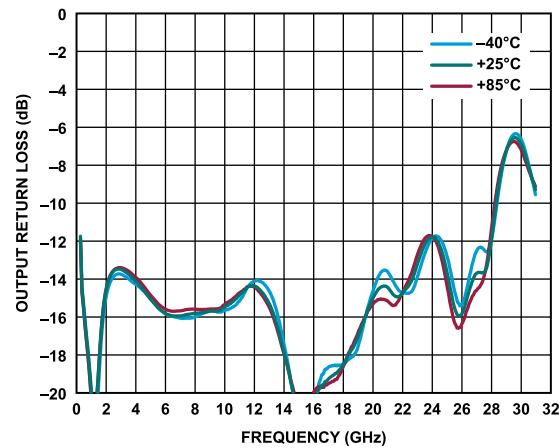


Figure 25. Output Return Loss vs. Frequency for Various Temperatures,  
200 MHz to 31 GHz,  $V_{DD} = 15$  V,  $I_{DQ} = 500$  mA

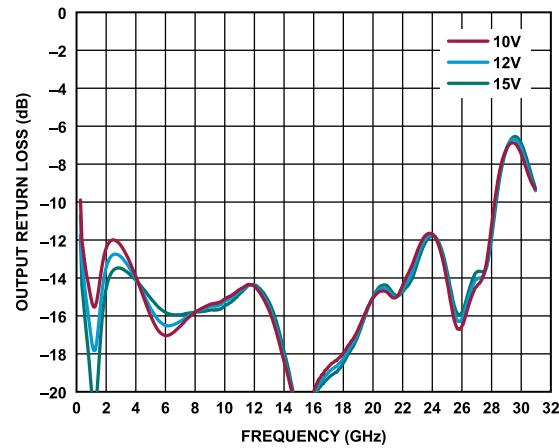


Figure 26. Output Return Loss vs. Frequency for Various  $V_{DD}$  Values,  
200 MHz to 31 GHz,  $I_{DQ} = 500$  mA

## TYPICAL PERFORMANCE CHARACTERISTICS

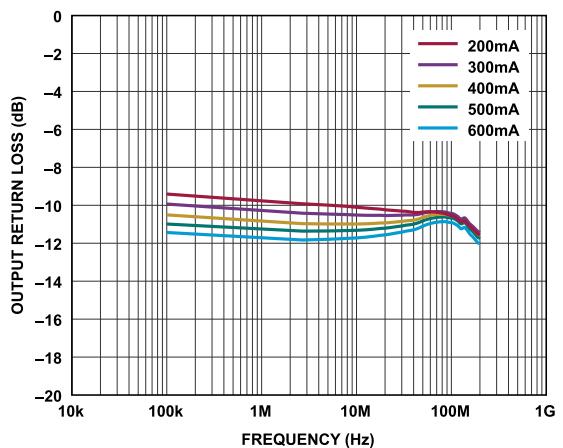


Figure 27. Output Return Loss vs. Frequency for Various  $I_{DQ}$  Values,  
100 kHz to 200 MHz,  $V_{DD} = 15$  V

027

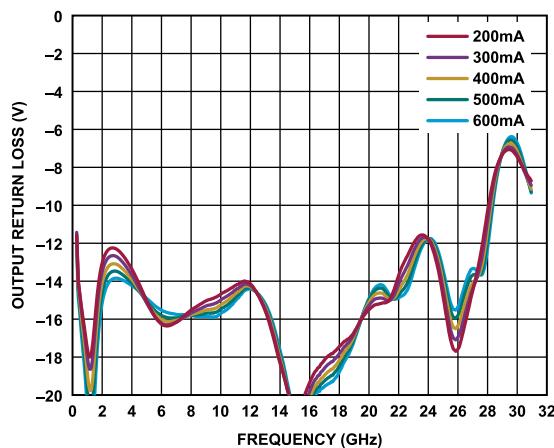
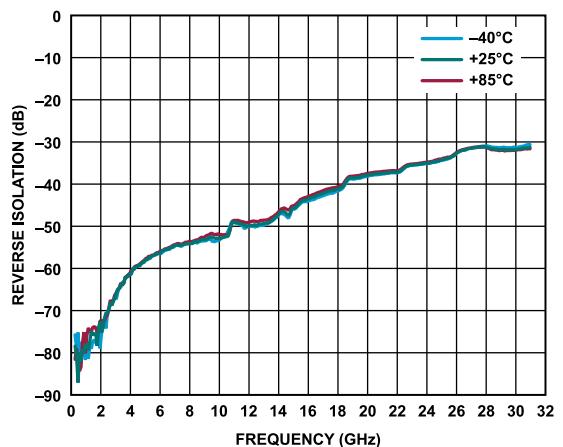


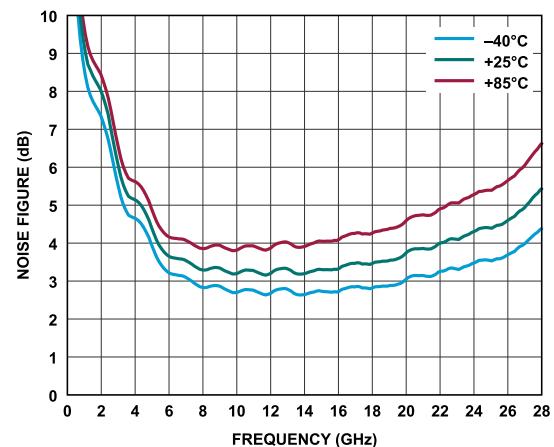
Figure 30. Output Return Loss vs. Frequency for Various  $I_{DQ}$  Values,  
200 MHz to 31 GHz,  $V_{DD} = 15$  V

030



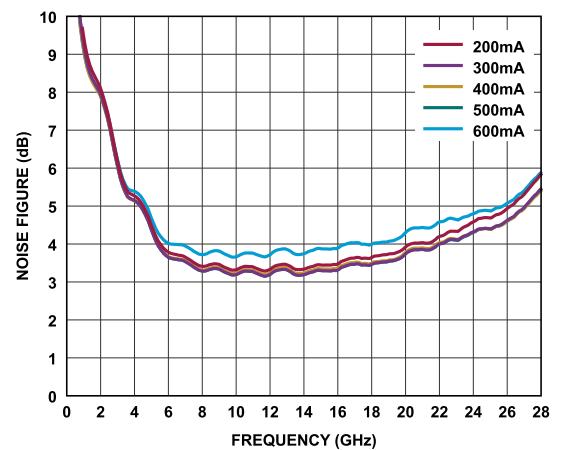
028

Figure 28. Reverse Isolation vs. Frequency for Various Temperatures,  
 $V_{DD} = 15$  V,  $I_{DQ} = 500$  mA



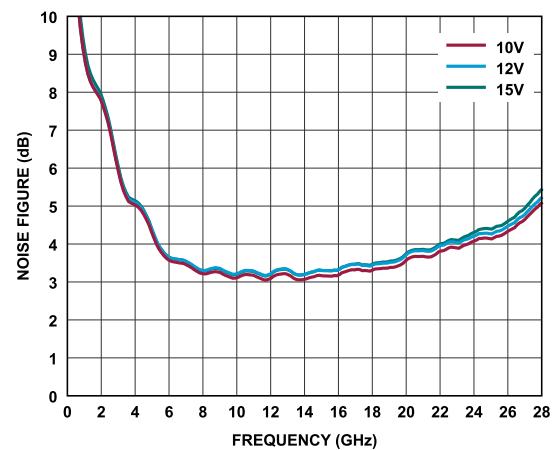
031

Figure 31. Noise Figure vs. Frequency for Various Temperatures,  $V_{DD} = 15$  V,  
 $I_{DQ} = 500$  mA



029

Figure 29. Noise Figure vs. Frequency for Various  $I_{DQ}$  Values,  $V_{DD} = 15$  V



032

Figure 32. Noise Figure vs. Frequency for Various  $V_{DD}$  Values,  $I_{DQ} = 500$  mA

## TYPICAL PERFORMANCE CHARACTERISTICS

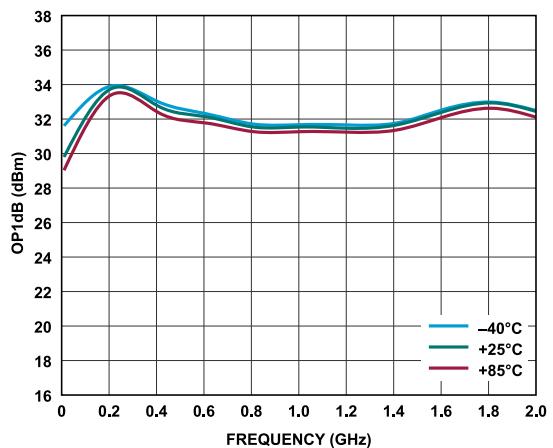


Figure 33.  $OP1dB$  vs. Frequency for Various Temperatures, 10 MHz to 2 GHz,  
 $V_{DD} = 15$  V,  $I_{DQ} = 500$  mA

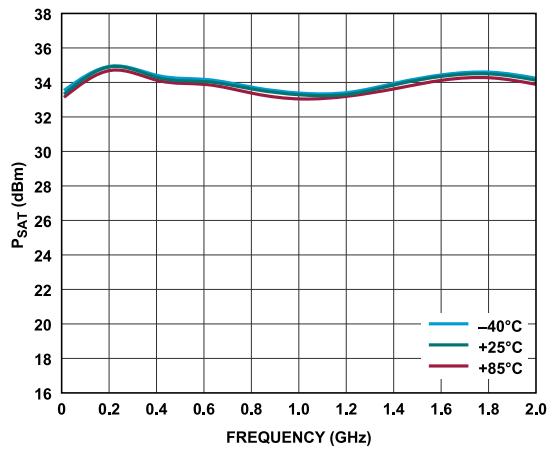


Figure 34.  $P_{SAT}$  vs. Frequency for Various Temperatures, 10 MHz to 2 GHz,  
 $V_{DD} = 15$  V,  $I_{DQ} = 500$  mA

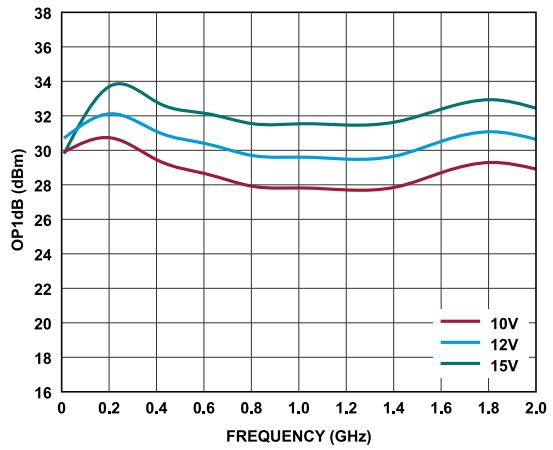


Figure 35.  $OP1dB$  vs. Frequency for Various  $V_{DD}$  Values, 10 MHz to 2 GHz,  
 $I_{DQ} = 500$  mA

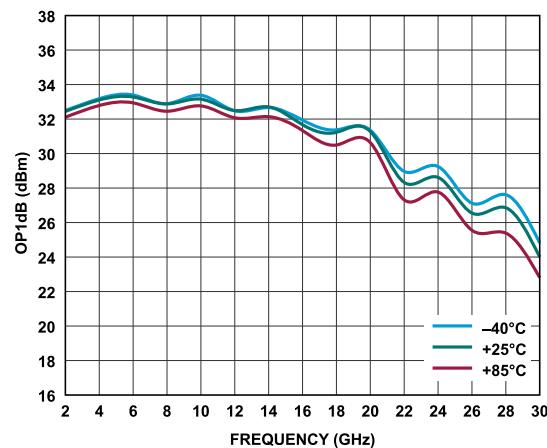


Figure 36.  $OP1dB$  vs. Frequency for Various Temperatures, 2 GHz to 28 GHz,  
 $V_{DD} = 15$  V,  $I_{DQ} = 500$  mA

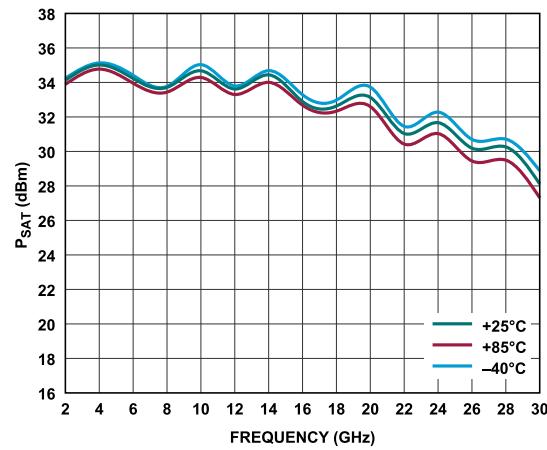


Figure 37.  $P_{SAT}$  vs. Frequency for Various Temperatures, 2 GHz to 28 GHz,  
 $V_{DD} = 15$  V,  $I_{DQ} = 500$  mA

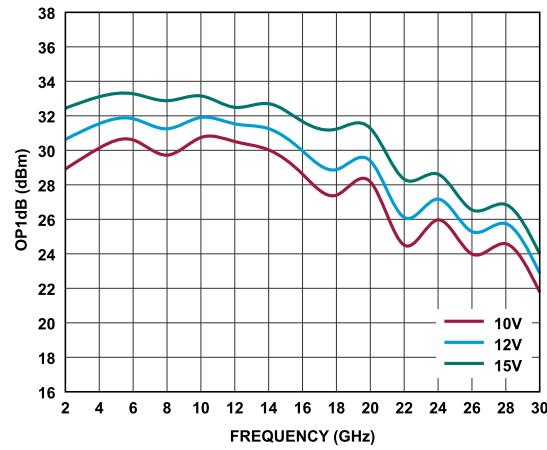
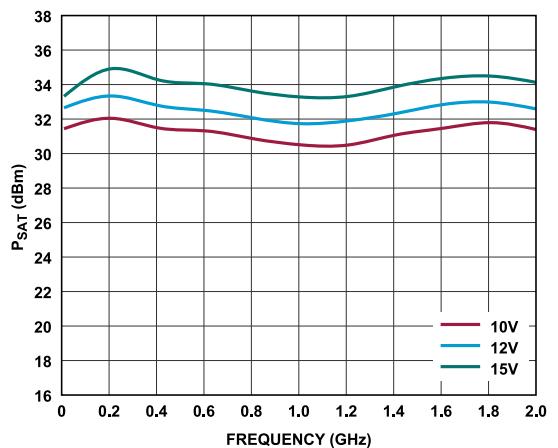
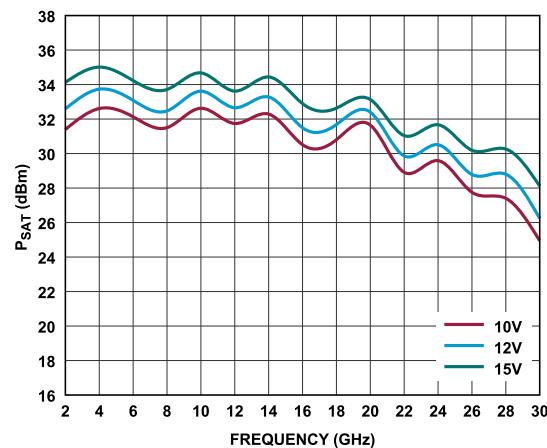


Figure 38.  $OP1dB$  vs. Frequency for Various  $V_{DD}$  Values, 2 GHz to 28 GHz,  
 $I_{DQ} = 500$  mA

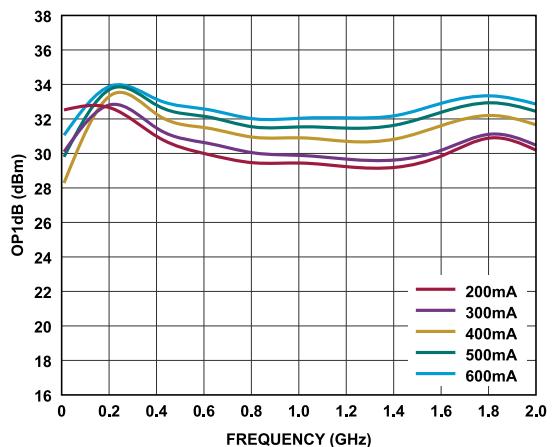
## TYPICAL PERFORMANCE CHARACTERISTICS



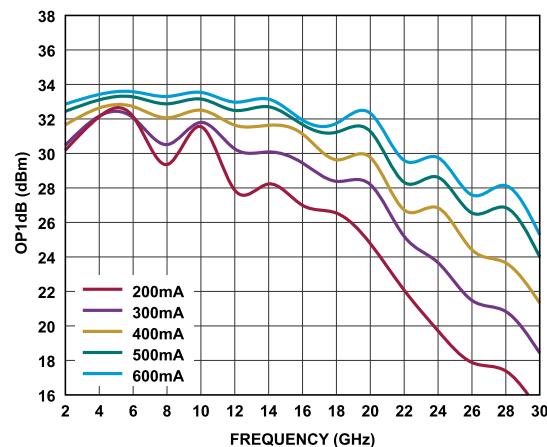
039



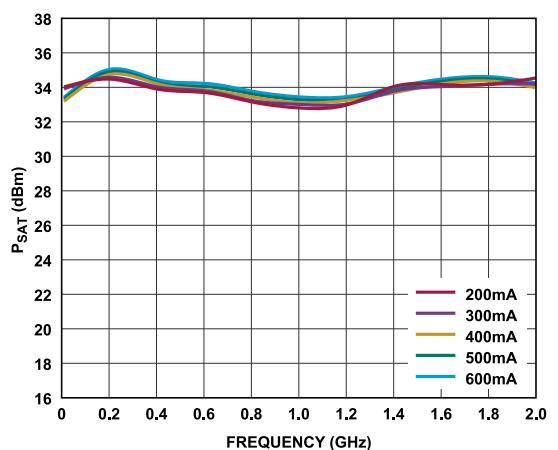
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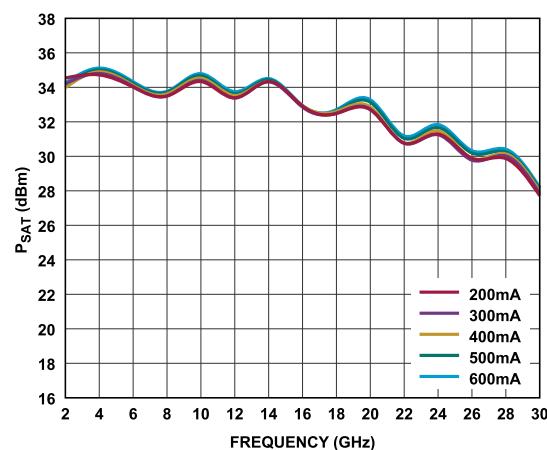
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043



041



044

## TYPICAL PERFORMANCE CHARACTERISTICS

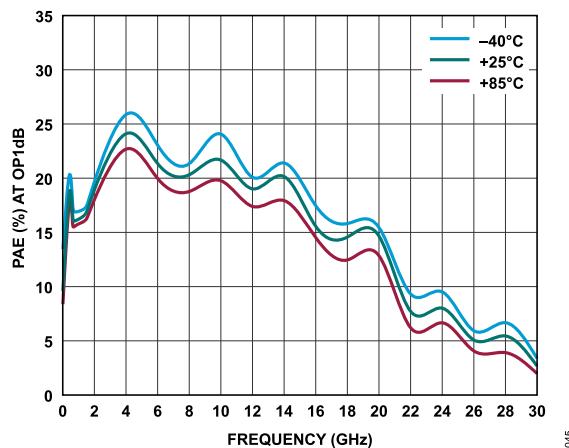


Figure 45. Power-Added Efficiency (PAE) at OP1dB vs. Frequency for Various Temperatures,  $V_{DD} = 15$  V,  $I_{DQ} = 500$  mA

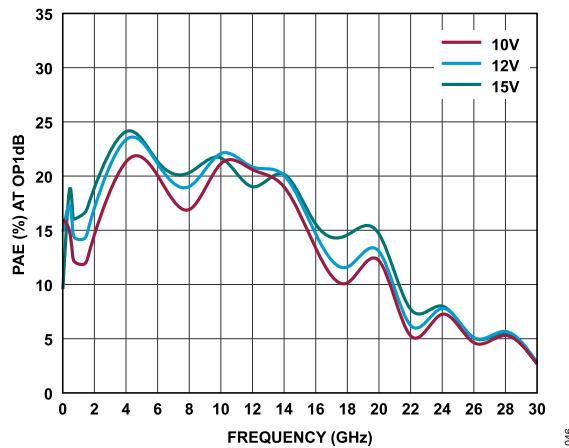


Figure 46. PAE at OP1dB vs. Frequency for Various  $V_{DD}$  Values,  $I_{DQ} = 500$  mA

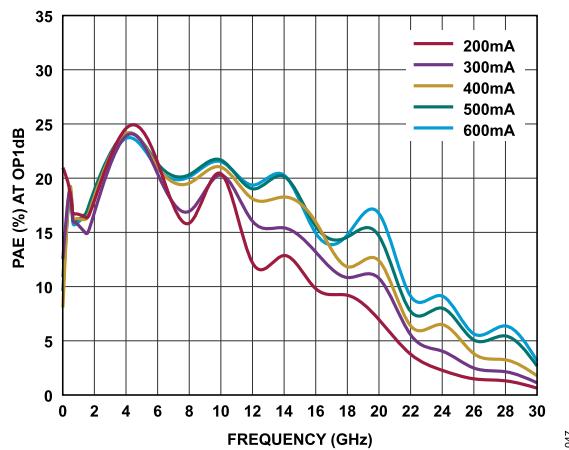


Figure 47. PAE at OP1dB vs. Frequency for Various  $I_{DQ}$  Values,  $V_{DD} = 15$  V

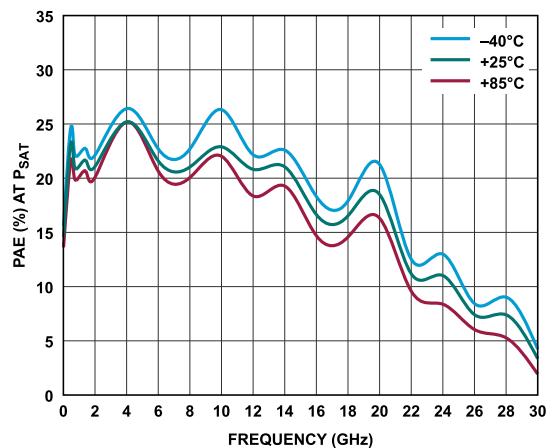


Figure 48. PAE at  $P_{SAT}$  vs. Frequency for Various Temperatures,  $V_{DD} = 15$  V,  $I_{DQ} = 500$  mA

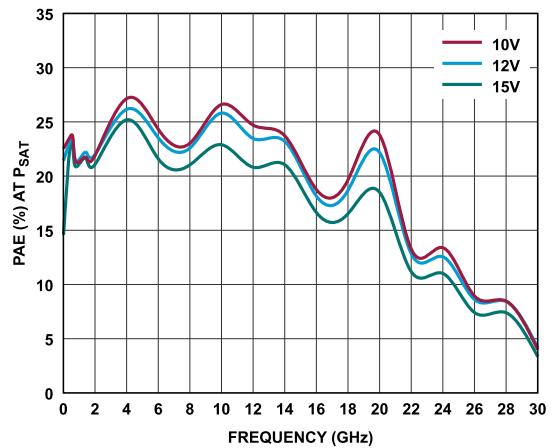


Figure 49. PAE at  $P_{SAT}$  vs. Frequency for Various  $V_{DD}$  Values,  $I_{DQ} = 500$  mA

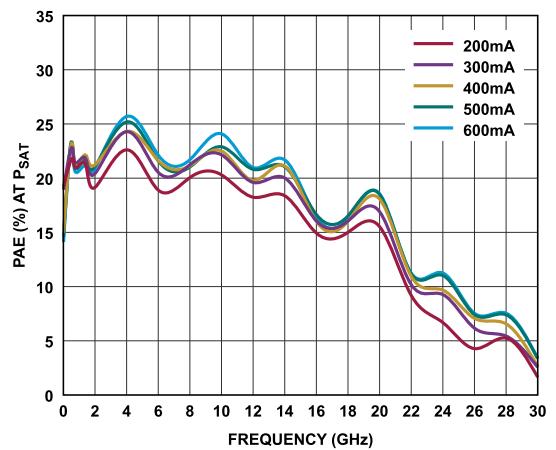
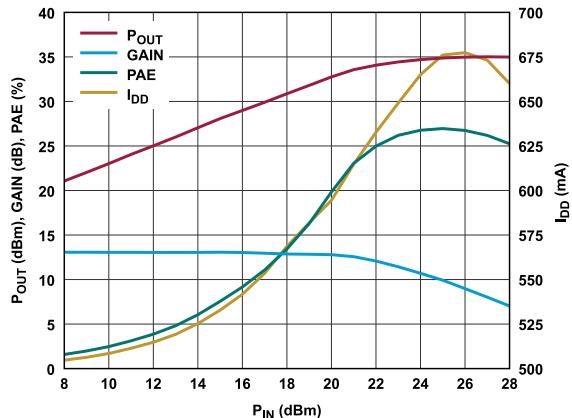
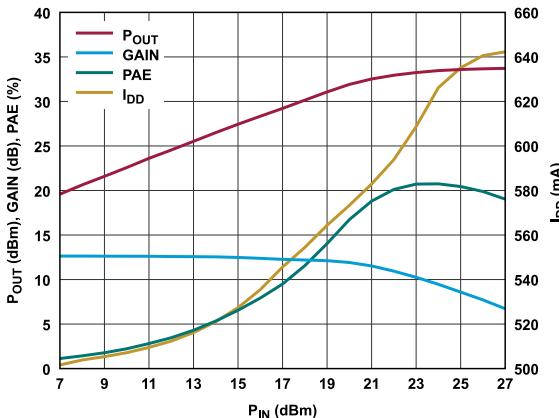


Figure 50. PAE at  $P_{SAT}$  vs. Frequency for Various  $I_{DQ}$  Values,  $V_{DD} = 15$  V

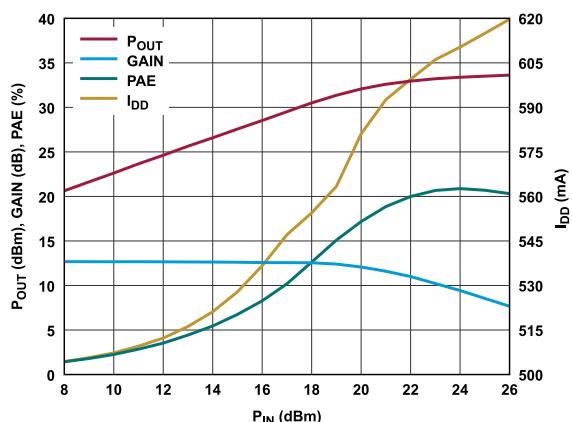
## TYPICAL PERFORMANCE CHARACTERISTICS



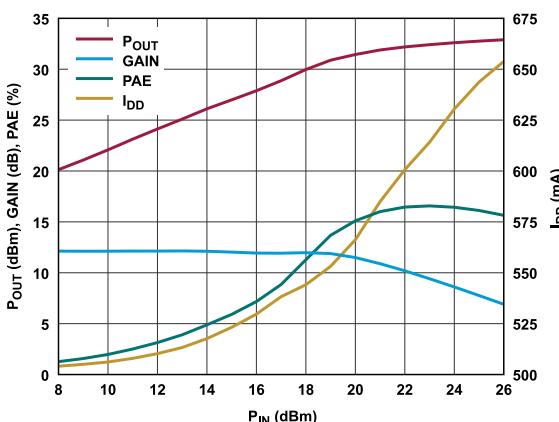
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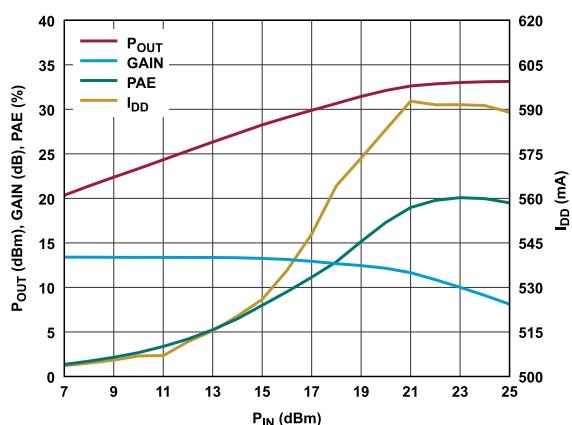
054



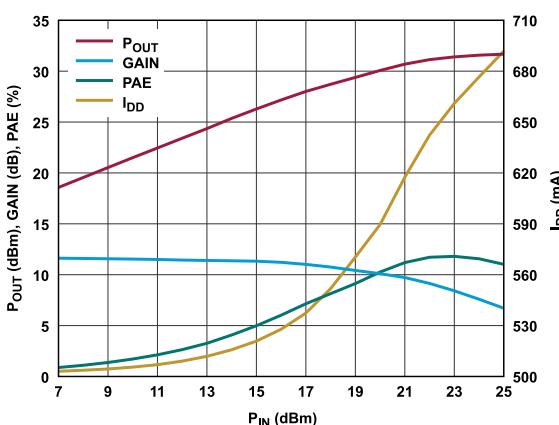
052



054



053



056

## TYPICAL PERFORMANCE CHARACTERISTICS

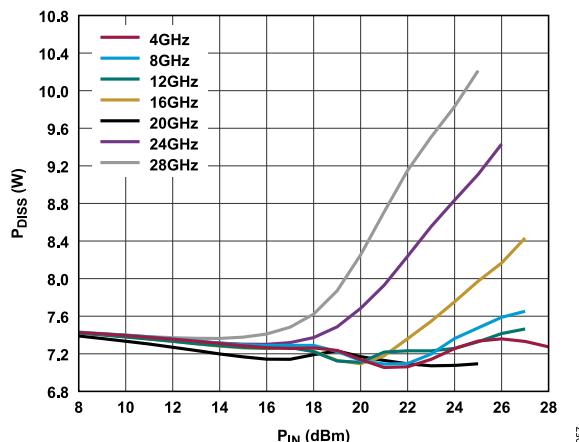


Figure 57.  $P_{DISS}$  vs.  $P_{IN}$  for Various Frequencies at  $T_A = 85^\circ\text{C}$ ,  $V_{DD} = 15\text{ V}$ ,  $I_{DQ} = 500\text{ mA}$

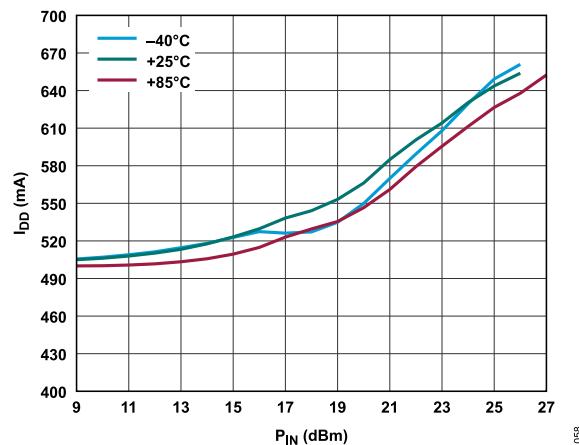


Figure 58.  $I_{DD}$  vs.  $P_{IN}$  for Various Temperatures, 16 GHz,  $V_{DD} = 15\text{ V}$ ,  $I_{DQ} = 500\text{ mA}$

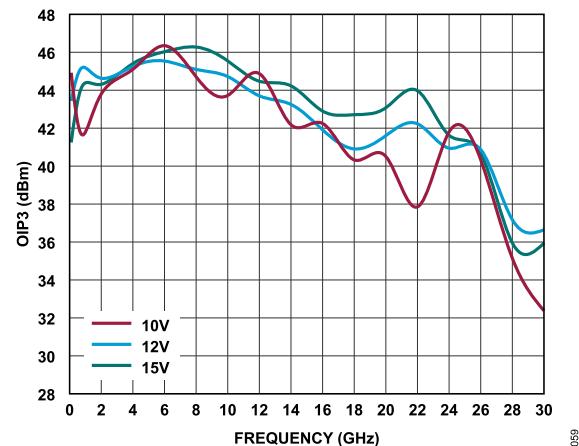


Figure 59. OIP3 vs. Frequency for Various  $V_{DD}$  Values,  $P_{OUT}$  per Tone = 16 dBm,  $I_{DQ} = 500\text{ mA}$

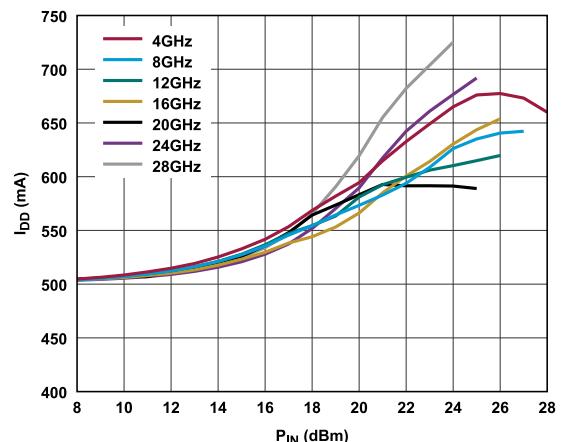


Figure 60.  $I_{DD}$  vs.  $P_{IN}$  for Various Frequencies,  $V_{DD} = 15\text{ V}$ ,  $I_{DQ} = 500\text{ mA}$

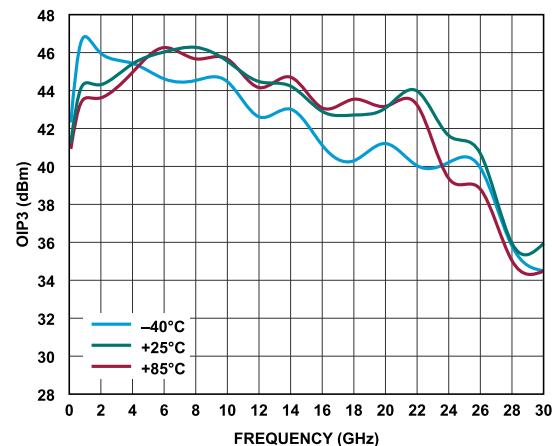


Figure 61. OIP3 vs. Frequency for Various Temperatures,  $P_{OUT}$  per Tone = 16 dBm,  $V_{DD} = 15\text{ V}$ ,  $I_{DQ} = 500\text{ mA}$

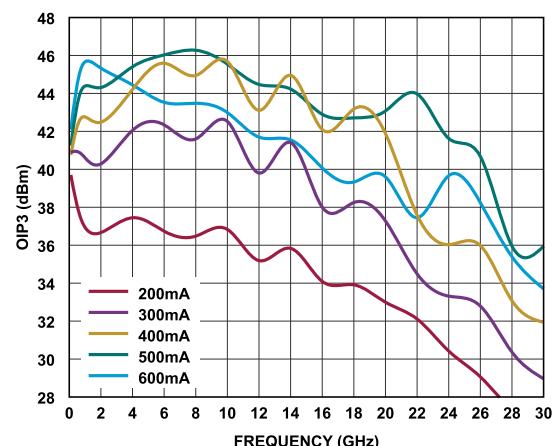


Figure 62. OIP3 vs. Frequency for Various  $I_{DQ}$  Values,  $P_{OUT}$  per Tone = 16 dBm,  $V_{DD} = 15\text{ V}$

## TYPICAL PERFORMANCE CHARACTERISTICS

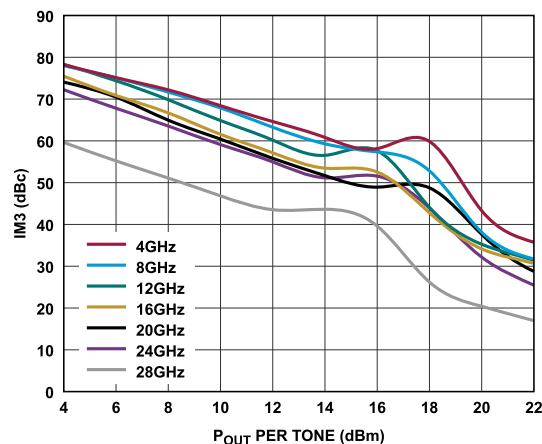


Figure 63. Third-Order Intermodulation Distortion (IM3) vs.  $P_{OUT}$  per Tone for Various Frequencies,  $V_{DD} = 10$  V,  $I_{DQ} = 500$  mA

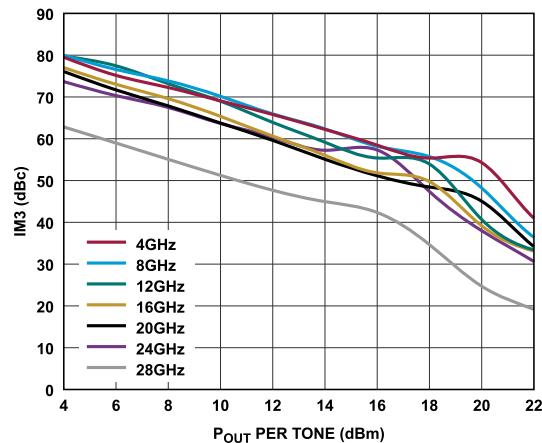


Figure 64. IM3 vs.  $P_{OUT}$  per Tone for Various Frequencies,  $V_{DD} = 12$  V,  $I_{DQ} = 500$  mA

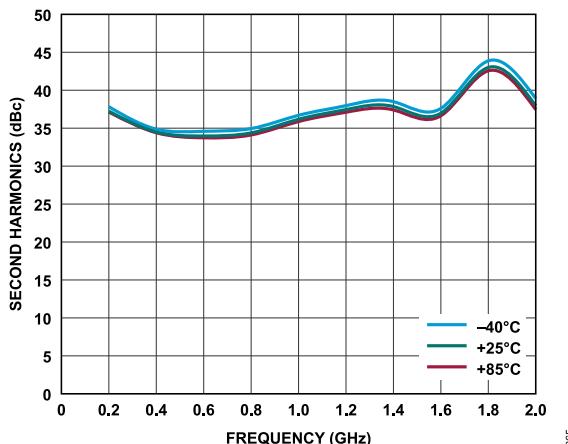


Figure 65. Low Frequency Second Harmonics vs. Frequency for Various Temperatures,  $V_{DD} = 15$  V,  $I_{DQ} = 500$  mA,  $P_{OUT} = 16$  dBm

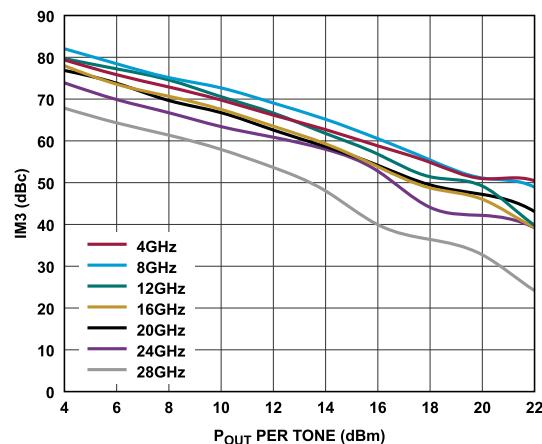


Figure 66. IM3 vs.  $P_{OUT}$  per Tone for Various Frequencies,  $V_{DD} = 15$  V,  $I_{DQ} = 500$  mA

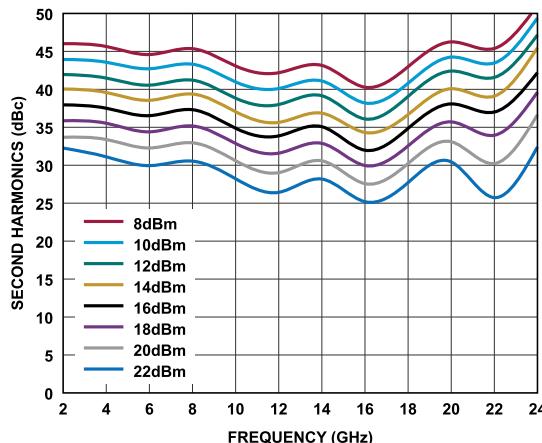


Figure 67. Second Harmonics vs. Frequency for Various  $P_{OUT}$  Values,  $V_{DD} = 15$  V,  $I_{DQ} = 500$  mA

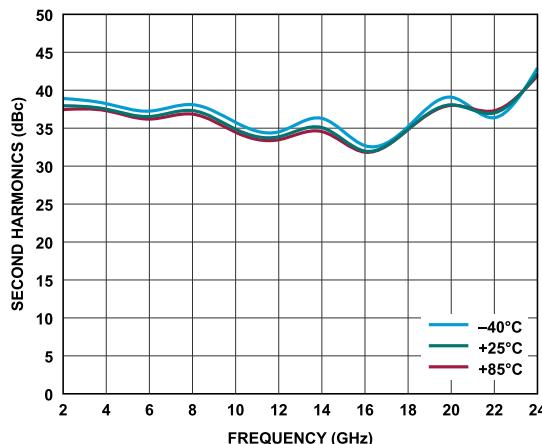


Figure 68. Second Harmonics vs. Frequency for Various Temperatures,  $V_{DD} = 15$  V,  $I_{DQ} = 500$  mA,  $P_{OUT} = 16$  dBm

## TYPICAL PERFORMANCE CHARACTERISTICS

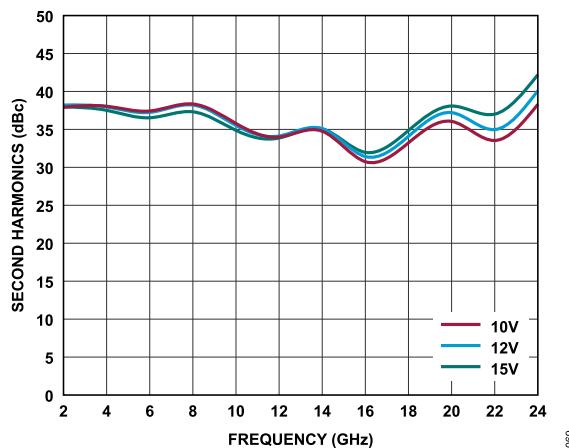


Figure 69. Second Harmonics vs. Frequency for Various  $V_{DD}$  Values,  
 $I_{DQ} = 500 \text{ mA}$ ,  $P_{OUT} = 16 \text{ dBm}$

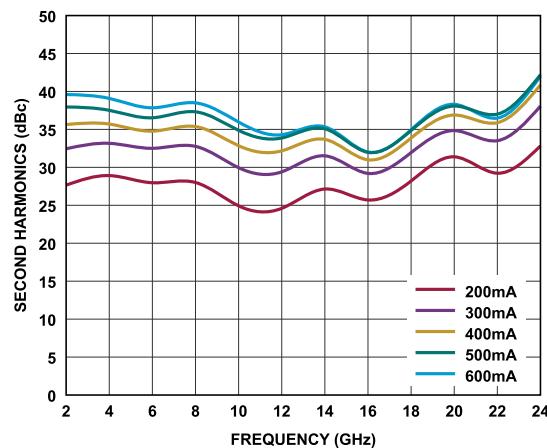


Figure 72. Second Harmonics vs. Frequency for Various  $I_{DQ}$  Values,  
 $V_{DD} = 15 \text{ V}$ ,  $P_{OUT} = 16 \text{ dBm}$

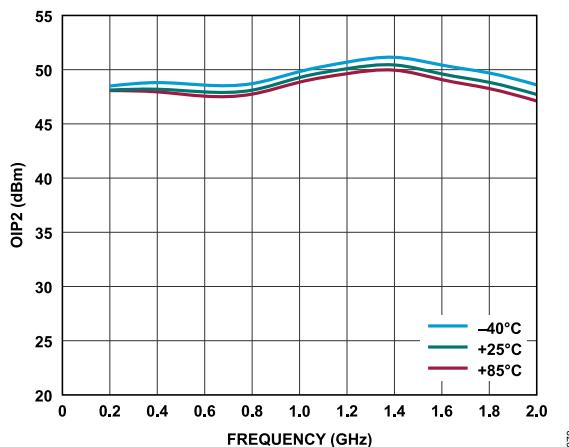


Figure 70. Low Frequency OIP2 vs. Frequency for Various Temperatures,  
 $V_{DD} = 15 \text{ V}$ ,  $I_{DQ} = 500 \text{ mA}$ ,  $P_{OUT} = 16 \text{ dBm}$

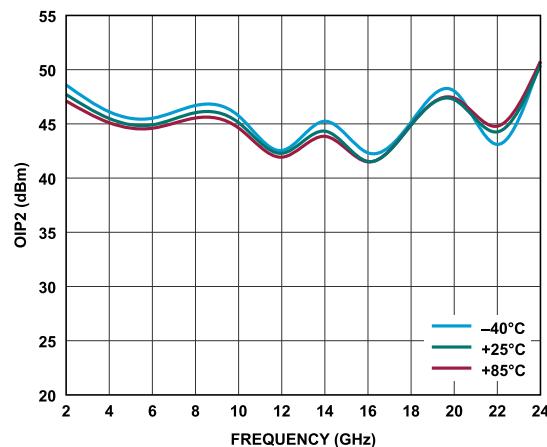


Figure 73. OIP2 vs. Frequency for Various Temperatures,  $V_{DD} = 15 \text{ V}$ ,  
 $I_{DQ} = 500 \text{ mA}$ ,  $P_{OUT} = 16 \text{ dBm}$

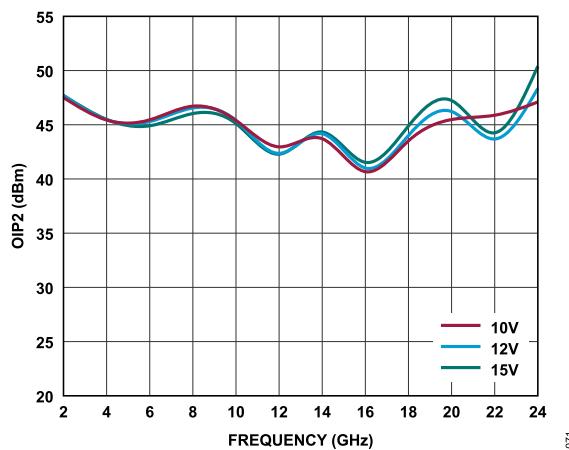


Figure 71. OIP2 vs. Frequency for Various  $V_{DD}$  Values,  $I_{DQ} = 500 \text{ mA}$ ,  
 $P_{OUT} = 16 \text{ dBm}$

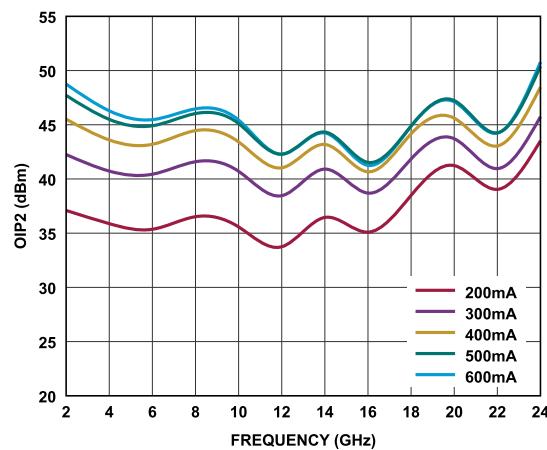
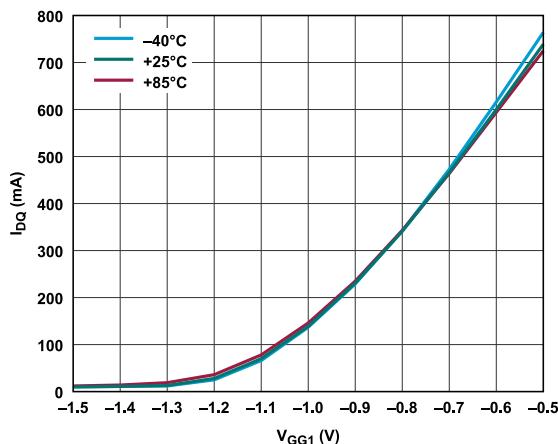
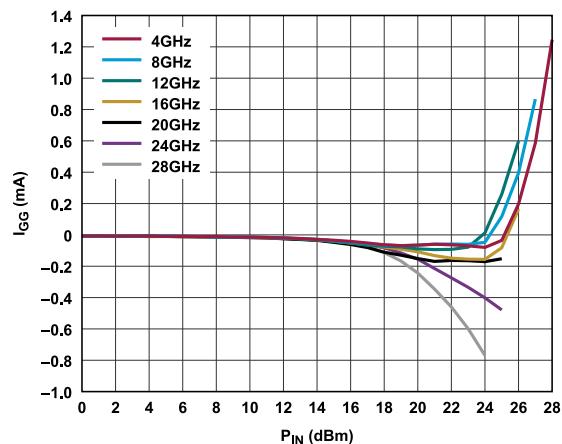
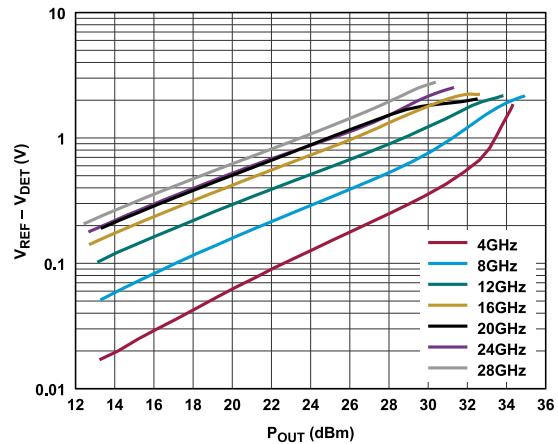
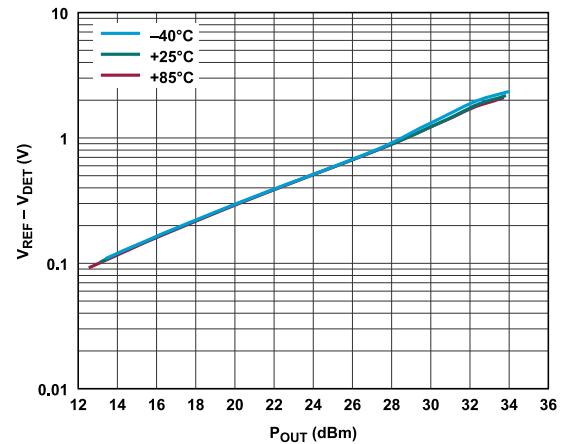
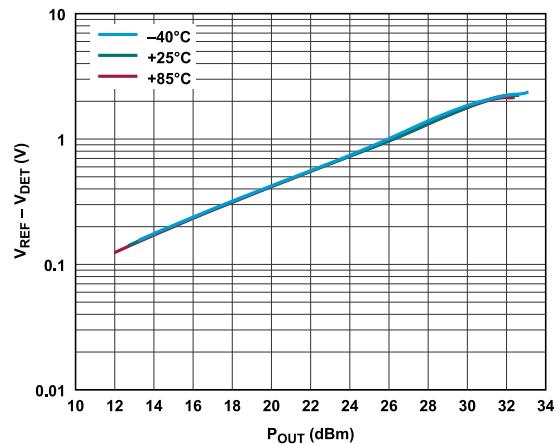
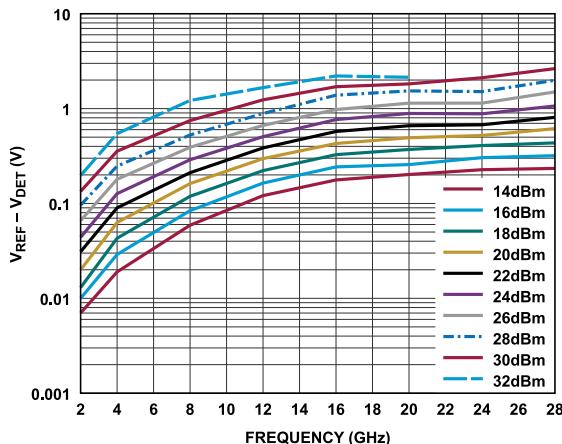


Figure 74. OIP2 vs. Frequency for Various  $I_{DQ}$  Values,  $V_{DD} = 15 \text{ V}$ ,  
 $P_{OUT} = 16 \text{ dBm}$

## TYPICAL PERFORMANCE CHARACTERISTICS

Figure 75.  $I_{DQ}$  vs.  $V_{GG1}$  for Various Temperatures,  $V_{DD} = 15$  VFigure 78.  $I_{GG}$  vs.  $P_{IN}$  for Various Frequencies,  $V_{DD} = 15$  VFigure 76. Detector Voltage ( $V_{REF} - V_{DET}$ ) vs.  $P_{OUT}$  for Various FrequenciesFigure 79.  $V_{REF} - V_{DET}$  vs.  $P_{OUT}$  for Various Temperatures at 12 GHzFigure 77.  $V_{REF} - V_{DET}$  vs.  $P_{OUT}$  for Various Temperatures at 16 GHzFigure 80.  $V_{REF} - V_{DET}$  vs. Frequency for Various  $P_{OUT}$  Values

## TYPICAL PERFORMANCE CHARACTERISTICS

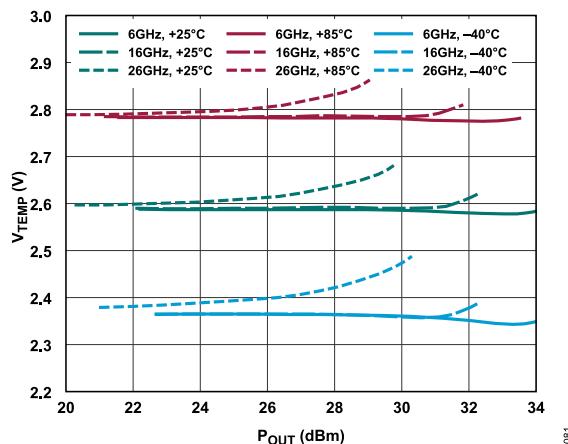


Figure 81. Temperature Sensor Voltage ( $V_{TEMP}$ ) vs.  $P_{OUT}$  for Various Frequencies and Temperatures,  $V_{DD} = 15$  V,  $I_{DQ} = 500$  mA

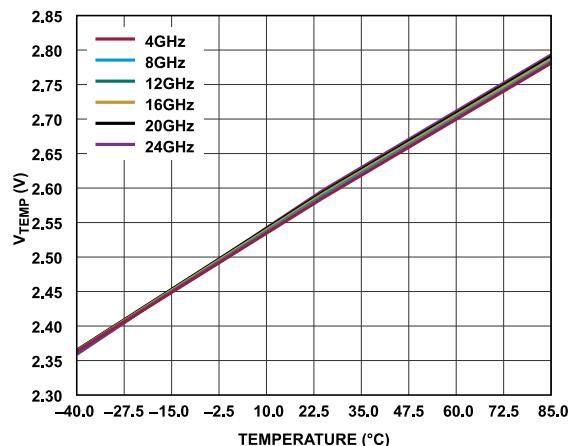


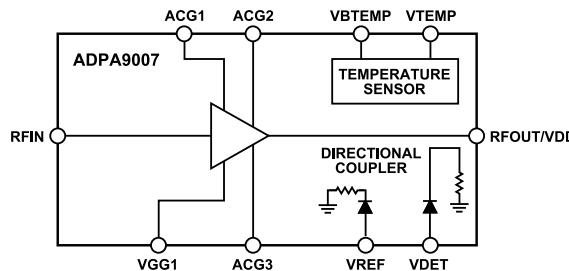
Figure 82.  $V_{TEMP}$  vs. Temperature for Various Frequencies,  $P_{OUT} = 28$  dBm,  $V_{DD} = 15$  V,  $I_{DQ} = 500$  mA

## THEORY OF OPERATION

The ADPA9007 is a broadband distributed GaAs, pHEMT, medium power amplifier. The simplified block diagram is shown in [Figure 83](#). The drain current is set by the negative voltage applied to the VGG1 pin. The gate pin, VGG1, is driven by a negative voltage in the  $-1.5$  V to  $0$  V range. For an  $I_{DQ}$  of  $500$  mA, a gate bias voltage of  $-0.7$  V is typically required. The drain bias voltage is applied through the RFOUT/VDD pin via a broadband bias tee or external bias network.

A portion of the RF output signal is directionally coupled to a diode for detection of the RF output power. When the diode is DC biased, the diode rectifies the RF power and makes the RF power available for measurement as DC voltage at the VDET pin. To allow temperature compensation of the VDET pin, an identical circuit (minus the RF coupled power) is available via the VREF pin. Taking the difference of  $V_{REF} - V_{DET}$  provides a temperature compensated signal that is proportional to the RF output power.

The ADPA9007 contains an integrated temperature sensor. The temperature sensor that is biased using the VBTEMP pin and a voltage that is proportional to the device temperature is available on VTEMP pin.



*Figure 83. ADPA9007 Architecture*

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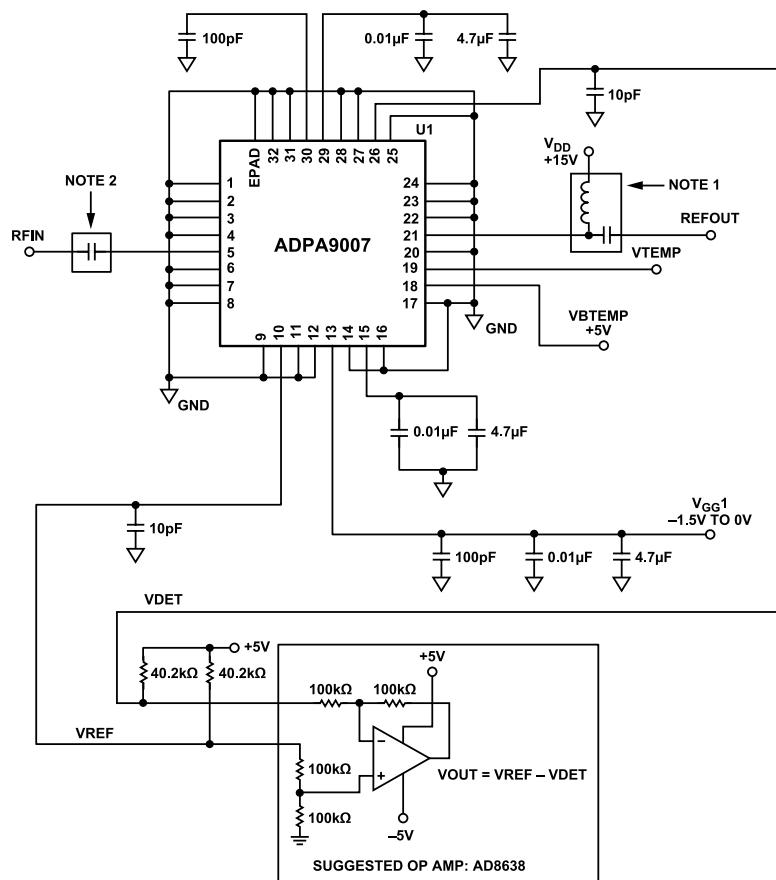
## APPLICATIONS INFORMATION

Figure 84 shows the basic connections for operating the ADPA9007. The RFIN and the RFOUT/VDD pins require external AC-coupling capacitors. The drain bias is applied through a bias tee on the RFOUT/VDD pin. The nominal drain bias is 15 V. The negative gate current is applied to the VGG1 pin. A V<sub>GG1</sub> of approximately  $-0.7$  V sets the drain current to 500 mA.

The VDET and VREF pins are connected to 5 V through 40.2 k $\Omega$  biasing resistors to bias internal circuits. Figure 84 shows an option-

al op amp differential amplifier circuit that can be used to subtract V<sub>DET</sub> from V<sub>REF</sub>, yielding a temperature-compensated voltage that is proportional to the RF output power.

The configuration shown in Figure 84 was used to characterize the device with the exception of the op-amp circuit. VDET and VREF were measured at their respective pins with just the two 40.2 k $\Omega$  biasing resistors attached.



## NOTES

1. DRAIN BIAS, (V<sub>DD</sub>), MUST BE APPLIED THROUGH A BROADBAND BIAS TEE OR EXTERNAL BIAS NETWORK.
2. EXTERNAL DC BLOCK REQUIRED AT RF INPUT.

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Figure 84. Basic Connections

**APPLICATIONS INFORMATION****POWER-UP SEQUENCING**

The following power-up sequencing is recommended:

1. Connect GND to ground.
2. Set  $V_{GG1}$  to -1.5 V.
3. Set RFOUT/VDD to 15 V.
4. Increase  $V_{GG1}$  to achieve an  $I_{DQ} = 500$  mA.
5. Apply the RF signal.

If the desired gate voltage is known, set the  $V_{GG1}$  directly in Step 2 and skip Step 4.

**POWER-DOWN SEQUENCING**

The following power-down sequencing is recommended.

1. Turn off the RF signal.
2. Decrease  $V_{GG1}$  to -1.5 V to achieve an  $I_{DQ} = 0$  mA.
3. Decrease  $V_{DD}$  to 0 V.
4. Increase  $V_{GG1}$  to 0 V.

## BIASING THE ADPA9007 WITH THE HMC980LP4E

The [HMC980LP4E](#) is an active bias controller that is designed to meet the bias requirements of depletion mode amplifiers such as the ADPA9007. The controller provides constant drain current biasing over temperature, device to device variation, and it properly sequences gate and drain voltages to ensure the safe operation of the amplifier. The HMC980LP4E also offers self-protection in the event of a short circuit. An internal charge pump generates the negative voltage that is needed on the gate of the ADPA9007, and there is an option to use an external negative voltage source. The HMC980LP4E is also available in die form as the [HMC980-Die](#).

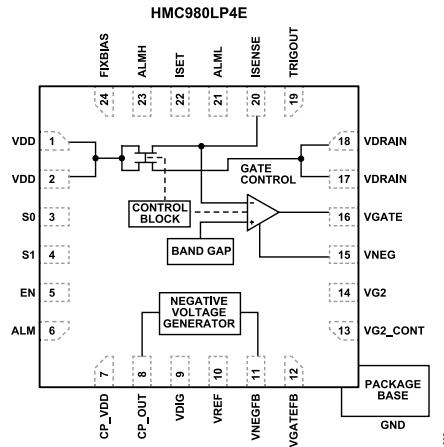


Figure 85. HMC980LP4E Active Bias Control

## APPLICATION CIRCUIT SETUP

Figure 86 shows an application circuit using the HMC980LP4E to control the ADPA9007. When using an external negative supply for VNEG, see the application circuit shown in Figure 87.

In the application circuit shown in Figure 86, the ADPA9007 drain voltage ( $V_{DRAIN}$ ) and drain current ( $I_{DRAIN}$ ) are set by the following equations:

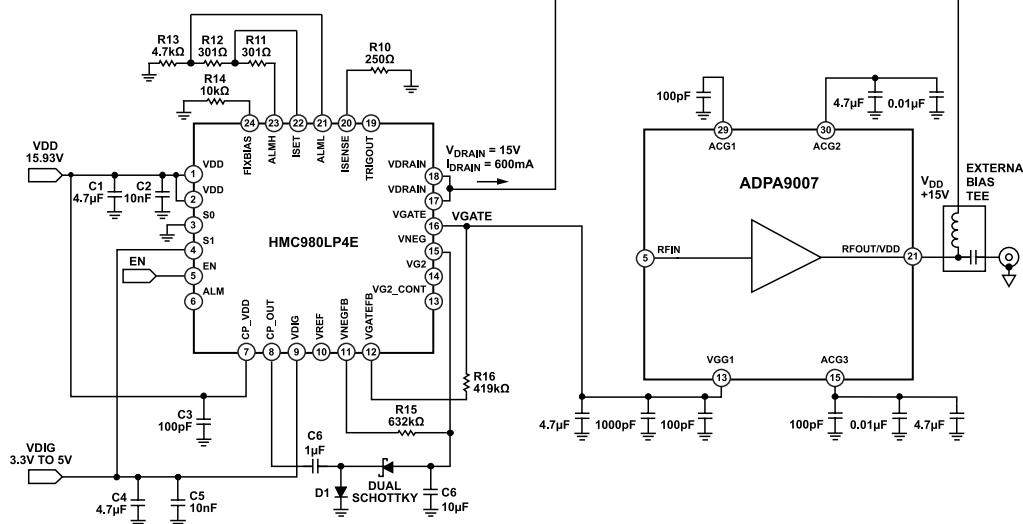


Figure 86. Application Circuit Using the HMC980LP4E with the ADPA9007 (Internal Negative Voltage Source)

$$V_{DD} = V_{DRAIN} + (I_{DRAIN} \times 1.55 \Omega) \quad (1)$$

$$V_{DD} = 15 V + (0.6 A \times 1.55 \Omega) = 15.93 V \quad (2)$$

where:

The  $V_{DD}$  and  $V_{DRAIN}$  values are in volts.

The  $I_{DRAIN}$  value is in amperes.

$$R10 = (150 \Omega \times A) / (I_{DRAIN}) \quad (3)$$

$$R10 = (150 \Omega \times A) / (0.6 A) = 250 \Omega \quad (4)$$

where:

The  $R10$  is in ohms.

The  $I_{DRAIN}$  is in amperes.

To achieve a certain large signal output power, sufficient drain current must be available to the device. The required drain current can be estimated from the curves shown in [Figure 51](#) to [Figure 56](#).

As an example, for 16 GHz at  $I_{DQ} = 500$  mA in constant gate voltage mode, [Figure 55](#) shows that the  $IDD$  ramps up to approximately 600 mA at  $P1dB$ . In order to obtain similar  $P1dB$  performance in constant drain current mode, the constant drain current must thus be set higher than 500 mA, so that 600 mA is available to the device. This can be seen in [Figure 95](#). If the constant drain current were to instead be set to 500 mA, then 600 mA would not be available to the device at large signal, resulting in a lower  $P1dB$ .

## LIMITING VGATE FOR THE ADPA9007 V<sub>GG1</sub>

When using the HMC980LP4E to control the ADPA9007, the minimum gate voltage should be set to approximately -1.5 V. To set the minimum voltages, set the R15 and R16 resistors to the values shown in [Figure 86](#) and [Figure 87](#). Refer to the [AN-1363: Meeting Biasing Requirements of Externally Biased RF/Microwave Amplifiers with Active Bias Controllers](#) application note for more information and calculations for the R15 and R16 resistors.

## BIASING THE ADPA9007 WITH THE HMC980LP4E

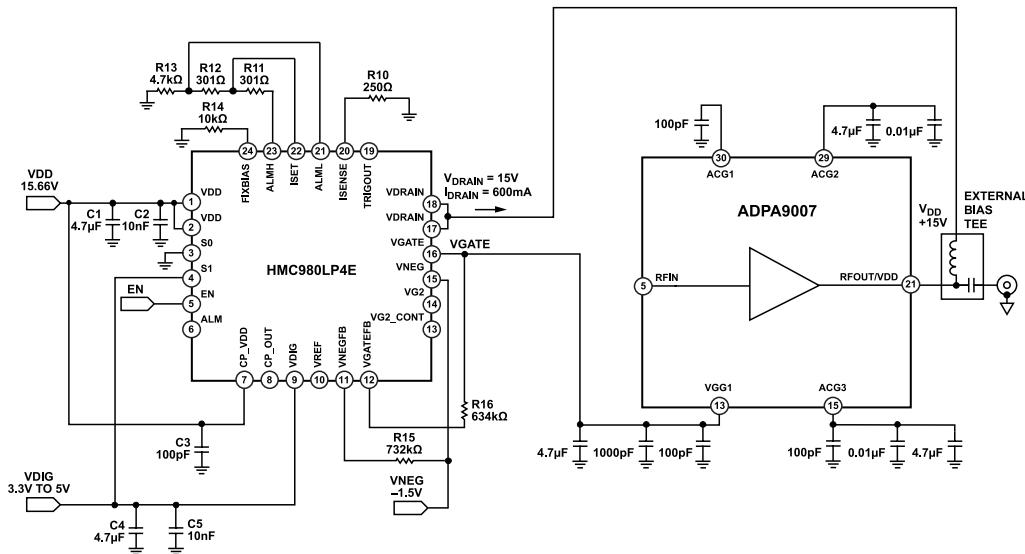


Figure 87. Application Circuit Using the HMC980LP4E with the ADPA9007 (External Negative Voltage Source)

## HMC980LP4E BIAS SEQUENCE

The DC supply sequence described in this section is required to prevent damage to the [HMC980LP4E](#) when using the device to control the ADPA9007.

## Power-Up Sequence

The power-up sequence for the HMC980LP4E is as follows:

1. Set the **VDIG** pin = 3.3 V.
2. Set the **S0** pin = 3.3 V.
3. Set the **VDD** pin = 15.51 V.
4. Set the **VNEG** pin = -1.5 V (this step is unnecessary if using an internally generated voltage).
5. Set the **EN** pin = 3.3 V (the transition from 0 V to 3.3 V turns on the **VGATE** pin and the **VDRAIN** pin).

## Power-Down Sequence

The power-down sequence for the HMC980LP4E is as follows:

1. Set the EN pin = 0 V (the transition from 3.3 V to 0 V turns off the VDRAIN pins and the VGATE pin).
2. Set the VNEG pin = 0 V (this step is unnecessary if using an internally generated voltage).
3. Set the VDD pin = 0 V.
4. Set the S0 pin = 0 V.
5. Set the VDIG pin = 0 V.

After the HMC980LP4E bias control circuit is set up, toggle the bias to the ADPA9007 on or off by applying 3.3 V or 0 V, respectively, to the EN pin. At the EN pin = +3.3 V, the VGATE pin drops to -1.5 V, and the VDRAIN pins turn on at +15 V. The VGATE pin then rises until  $I_{DRAIN} = 600$  mA, and the closed control loop regulates

$I_{DRAIN}$  at 600 mA. When the EN pin = 0 V, the VGATE pin is set to -1.5 V, and the VDRAIN pins are set to 0 V.

## CONSTANT DRAIN CURRENT BIASING VS. CONSTANT GATE VOLTAGE BIASING

The **HMC980LP4E** uses closed-loop feedback to continuously adjust the VGATE pin to maintain a constant drain current bias over DC supply variation, temperature, and device-to-device variation. In addition, constant drain current biasing is the optimum method to reduce time in calibration procedures and to maintain consistent performance over time.

To increase the OP1dB performance for the constant drain current bias, increase the set-point current as shown in [Figure 89](#). The limit of increasing set-point current under the constant drain current operation is set by the thermal limitations found in [Table 7](#) with the maximum power-dissipation specification. As the  $I_{DD}$  increases, the power dissipation increases, but the actual OP1dB does not continue to increase indefinitely. Therefore, when using constant drain current biasing, take the relationship between the power dissipation and the OP1dB performance into consideration.

## BIASING THE ADPA9007 WITH THE HMC980LP4E

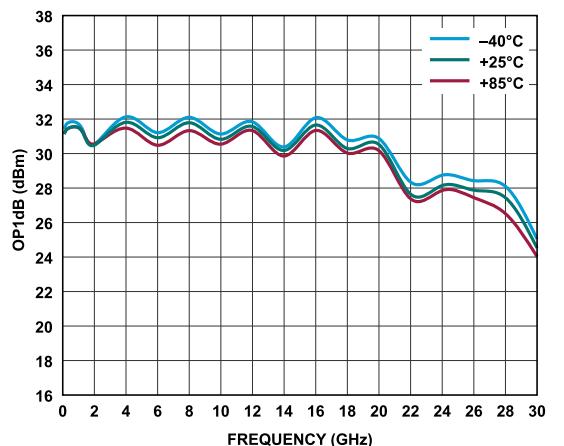


Figure 88.  $OP_{1dB}$  vs. Frequency for Various Temperatures,  $V_{DD} = 15$  V, Data Measured with Constant  $I_{DD} = 600$  mA

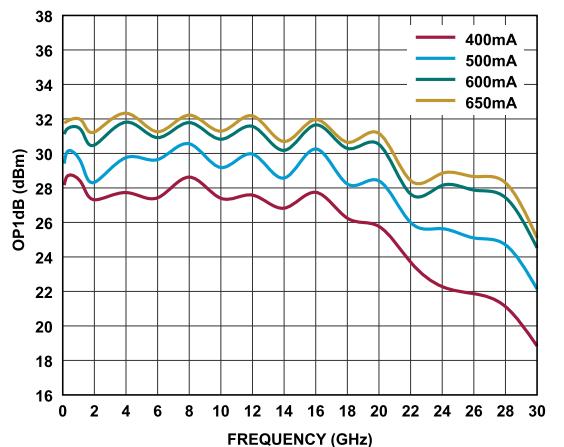


Figure 89.  $OP_{1dB}$  vs. Frequency for Various Set-Point Drain Currents, Constant Current Mode,  $V_{DD} = 15$  V

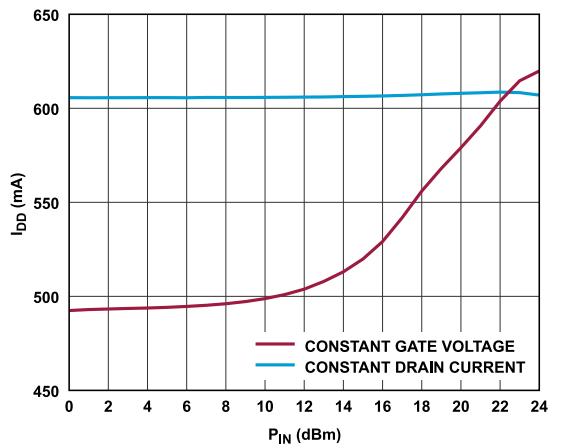


Figure 90.  $I_{DD}$  vs.  $P_{IN}$ ,  $V_{DD} = 15$  V, Frequency = 16 GHz, Constant  $I_{DRAIN}$  Set Point = 600 mA and Constant  $V_{GG1}$  ( $I_{DQ} = 500$  mA)

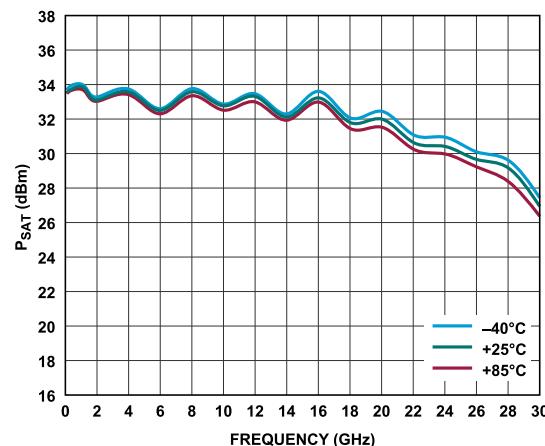


Figure 91.  $P_{SAT}$  vs. Frequency for Various Temperatures,  $V_{DD} = 15$  V, Data Measured with Constant  $I_{DD} = 600$  mA

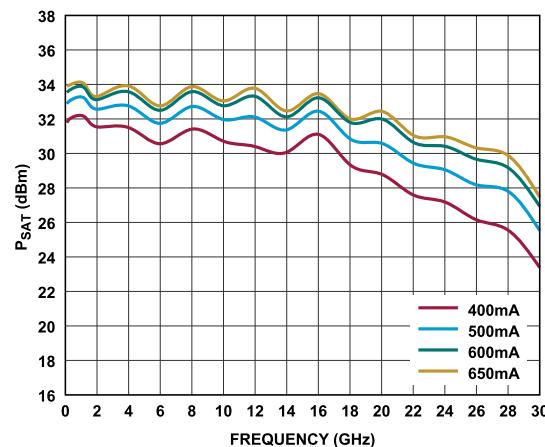


Figure 92.  $P_{SAT}$  vs. Frequency for Various Set-Point Drain Currents, Constant Current Mode,  $V_{DD} = 15$  V

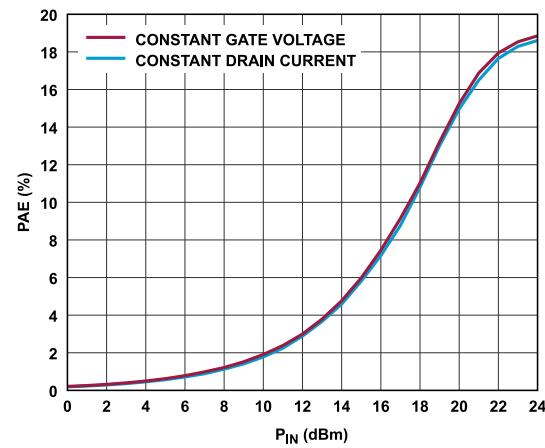


Figure 93. PAE vs.  $P_{IN}$ ,  $V_{DD} = 15$  V, Frequency = 16 GHz, Constant  $I_{DRAIN}$  Set Point = 600 mA and Constant  $V_{GG1}$  ( $I_{DQ} = 500$  mA)

## BIASING THE ADPA9007 WITH THE HMC980LP4E

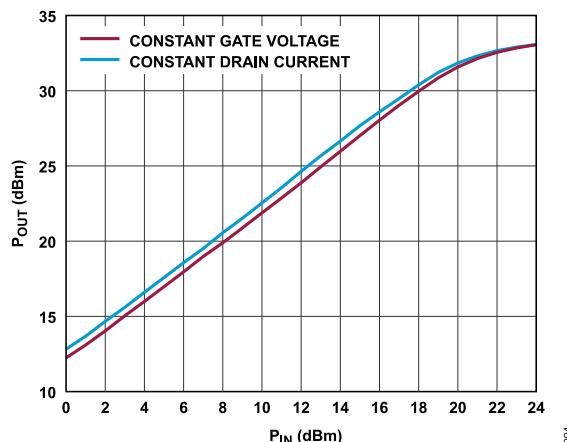


Figure 94.  $P_{OUT}$  vs.  $P_{IN}$ ,  $V_{DD} = 15$  V, Frequency = 16 GHz, Constant  $I_{DRAIN}$  Set Point = 600 mA and Constant  $V_{GG1}$  ( $I_{DQ} = 500$  mA)

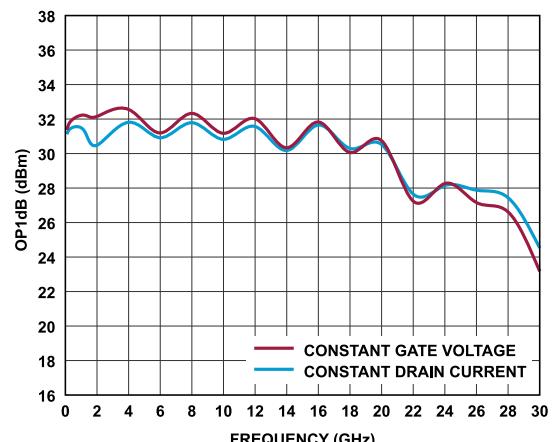


Figure 95. OP1dB vs. Frequency,  $V_{DD} = 15$  V, Constant  $I_{DRAIN}$  Set Point = 600 mA and Constant  $V_{GG1}$  ( $I_{DQ} = 500$  mA)

**OUTLINE DIMENSIONS**

Package Drawing (Option)	Package Type	Package Description
CG-32-2	LFCSP_CAV	32-Lead Lead Frame Chip Scale Package, Premolded Cavity

For the latest package outline information and land patterns (footprints), go to [Package Index](#).

**ORDERING GUIDE**

Model <sup>1</sup>	Temperature Range	Package Description	Packing Quantity	Package Option
ADPA9007ACGZN	-40°C to +85°C	32-Lead LFCSP (5 mm × 5 mm w/ EP)	Reel, 100	CG-32-2
ADPA9007ACGZN-R7	-40°C to +85°C	32-Lead LFCSP (5 mm × 5 mm w/ EP)	Reel, 1000	CG-32-2

<sup>1</sup> Z = RoHS Compliant Part.

Updated: August 11, 2023

**EVALUATION BOARDS**

Model <sup>1</sup>	Description
ADPA9007-EVALZ	Evaluation Board

<sup>1</sup> Z = RoHS Compliant Part.