1GHz to 22GHz, 15W, GaN Power Amplifier

FEATURES

- Frequency range: 1GHz to 22GHz
- 50Ω matched input and output
- Power gain: 14dB typical from 8GHz to 16GHz
- P_{OUT}: 42dBm typical from 8GHz to 16GHz
- PAE: 25% typical from 8GHz to 16GHz
- S21: 20.5dB typical from 8GHz to 16GHz
- OIP3: 44dBm typical from 8GHz to 16GHz
- Integrated RF power detector
- V_{DD}: 28V
- I_{DQ}: 600mA

APPLICATIONS

- Electronic warfare
- Test and measurement equipment

FUNCTIONAL BLOCK DIAGRAM

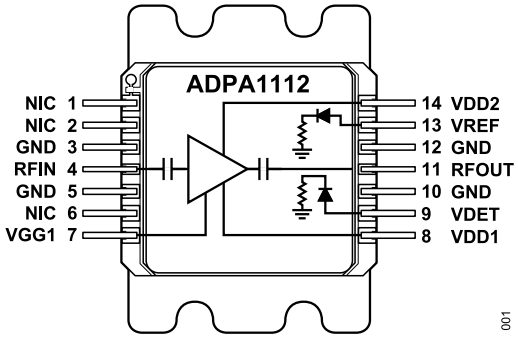

Figure 1. Functional Block Diagram

GENERAL DESCRIPTION

The ADPA1112 is a 1GHz to 22GHz wideband power amplifier with a saturated output power (P_{OUT}) of 42dBm, power added efficiency (PAE) of 25%, and a power gain of 14dB typical from 8GHz to 16GHz at input power (P_{IN}) of 28.0dBm. The RF input and RF output are internally matched and AC-coupled. A drain bias voltage (V_{DD}) of 28V is applied to the VDD1 and VDD2 pins, which have integrated bias inductors. The drain current is set by applying a negative voltage to the VGG1 pin. A temperature-compensated RF detector is integrated allowing monitoring of the RF output power.

The ADPA1112 is fabricated on a gallium nitride (GaN) process and is specified for operation from −40°C to +85°C.

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REVISION HISTORY

6/2025—Revision 0: Initial Version

ELECTRICAL SPECIFICATIONS

1GHz TO 2GHz FREQUENCY RANGE

T_{CASE} = 25°C, VDD1 drain bias voltage (V_{DD1}) and VDD2 drain bias voltage (V_{DD2}) = 28V, target quiescent current (I_{DQ}) = 600mA, and frequency range = 1GHz to 2GHz, unless otherwise stated.

Table 1. 1GHz to 2GHz Frequency Range

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
FREQUENCY RANGE	1		2	GHz	
GAIN					
Small Signal Gain (S21)		23.0		dB	
Gain Flatness		±1.34		dB	
Gain Variation over Temperature		0.03		dB/°C	
RETURN LOSS					
Input (S11)		10		dB	
Output (S22)		7.5		dB	
POWER					P_{IN} = 28.0dBm
P_{OUT}		41.5		dBm	
Gain		13.5		dB	
Power Added Efficiency (PAE)		36		%	
Output Third-Order Intercept (OIP3)		46		dBm	P_{OUT} per tone = 32.0dBm with 1MHz spacing
Output Second-Order Intercept (OIP2)		45		dBm	P_{OUT} per tone = 32.0dBm with 1MHz spacing
SUPPLY					
V_{DD}		28	30	V	
I_{DQ}		600		mA	Adjust the gate control voltage (V_{GG1}) between −3V and −1V to achieve an I_{DQ} = 600mA typical

2GHz TO 8GHz FREQUENCY RANGE

T_{CASE} = 25°C, V_{DD1} = V_{DD2} = 28V, I_{DQ} = 600mA, and frequency range = 2GHz to 8GHz, unless otherwise stated.

Table 2. 2GHz to 8GHz Frequency Range

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
FREQUENCY RANGE	2		8	GHz	
GAIN					
S21	17	21.0		dB	
Gain Flatness		±1.12		dB	
Gain Variation over Temperature		0.03		dB/°C	
RETURN LOSS					
S11		14		dB	
S22		10		dB	
POWER					P_{IN} = 28.0dBm
P_{OUT}	39.5	41.5		dBm	
Gain	11.5	13.5		dB	
PAE		26		%	
OIP3		45		dBm	P_{OUT} per tone = 32.0dBm with 1MHz spacing
OIP2		52		dBm	P_{OUT} per tone = 32.0dBm with 1MHz spacing
SUPPLY					
V_{DD}		28	30	V	
I_{DQ}		600		mA	Adjust V_{GG1} between −3V and −1V to achieve an I_{DQ} = 600mA typical

ELECTRICAL SPECIFICATIONS

8GHz TO 16GHz FREQUENCY RANGE

T_{CASE} = 25°C, V_{DD1} = V_{DD2} = 28V, I_{DQ} = 600mA, and frequency range = 8GHz to 16GHz, unless otherwise stated.

Table 3. 8GHz to 16GHz Frequency Range

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
FREQUENCY RANGE	8		16	GHz	
GAIN					
S21	16.5	20.5		dB	
Gain Flatness		±0.3		dB	
Gain Variation over Temperature		0.03		dB/°C	
RETURN LOSS					
S11		14		dB	
S22		14		dB	
POWER					P_{IN} = 28.0dBm
P_{OUT}	40	42		dBm	
Gain	12	14		dB	
PAE		25		%	
OIP3		44		dBm	P_{OUT} per tone = 32.0dBm with 1MHz spacing
OIP2		58		dBm	P_{OUT} per tone = 32.0dBm with 1MHz spacing
SUPPLY					
V_{DD}		28	30	V	
I_{DQ}		600		mA	Adjust V_{GG1} between −3V and −1V to achieve an I_{DQ} = 600mA typical

16GHz TO 18GHz FREQUENCY RANGE

T_{CASE} = 25°C, V_{DD1} = V_{DD2} = 28V, I_{DQ} = 600mA, and frequency range = 16GHz to 18GHz, unless otherwise stated.

Table 4. 16GHz to 18GHz Frequency Range

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
FREQUENCY RANGE	16		18	GHz	
GAIN					
S21	16.0	20.0		dB	
Gain Flatness		±0.3		dB	
Gain Variation over Temperature		0.03		dB/°C	
RETURN LOSS					
S11		14		dB	
S22		10		dB	
POWER					P_{IN} = 28.0dBm
P_{OUT}	40.0	42.0		dBm	
Gain	12	14		dB	
PAE		24		%	
OIP3		44.5		dBm	P_{OUT} per tone = 32.0dBm with 1MHz spacing
OIP2		53		dBm	P_{OUT} per tone = 32.0dBm with 1MHz spacing
SUPPLY					
V_{DD}		28	30	V	
I_{DQ}		600		mA	Adjust V_{GG1} between −3V and −1V to achieve an I_{DQ} = 600mA typical

ELECTRICAL SPECIFICATIONS

18GHz TO 20GHz FREQUENCY RANGE

T_{CASE} = 25°C, V_{DD1} and V_{DD2} = 28V, I_{DQ} = 600mA, and frequency range = 18GHz to 20GHz, unless otherwise stated

Table 5. 18GHz to 20GHz Frequency Range

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
FREQUENCY RANGE	18		20	GHz	
GAIN					
S21	16.5	20.5		dB	
Gain Flatness		±0.6		dB	
Gain Variation over Temperature		0.03		dB/°C	
RETURN LOSS					
S11		14		dB	
S22		10		dB	
POWER					P_{IN} = 28.0dBm
P_{OUT}	38.5	41		dBm	
Gain	10.5	13		dB	
PAE		20		%	
OIP3		44		dBm	P_{OUT} per tone = 32.0dBm with 1MHz spacing
OIP2		57		dBm	P_{OUT} per tone = 32.0dBm with 1MHz spacing
SUPPLY					
V_{DD}		28	30	V	
I_{DQ}		600		mA	Adjust V_{GG1} between −3V and −1V to achieve an I_{DQ} = 600mA typical

20GHz TO 22GHz FREQUENCY RANGE

T_{CASE} = 25°C, V_{DD1} and V_{DD2} = 28V, I_{DQ} = 600mA, and frequency range = 20GHz to 22GHz, unless otherwise stated

Table 6. 20GHz to 22GHz Frequency Range

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
FREQUENCY RANGE	20		22	GHz	
GAIN					
S21		19.0		dB	
Gain Flatness		±1.2		dB	
Gain Variation over Temperature		0.03		dB/°C	
RETURN LOSS					
S11		9		dB	
S22		10		dB	
POWER					P_{IN} = 28.0dBm
P_{OUT}		40.0		dBm	
Gain		12.0		dB	
PAE		16		%	
OIP3		44		dBm	P_{OUT} per tone = 32.0dBm with 1MHz spacing
OIP2		58		dBm	P_{OUT} per tone = 32.0dBm with 1MHz spacing
SUPPLY					
V_{DD}		28	30	V	
I_{DQ}		600		mA	Adjust V_{GG1} between −3V and −1V to achieve an I_{DQ} = 600mA typical

ABSOLUTE MAXIMUM RATINGS

Table 7. Absolute Maximum Ratings

Parameter	Rating
Bias Voltage	
Drain (V_{DD1} and V_{DD2})	35V
Gate (V_{GG1})	−8.0V DC to 0V DC
Bias Current	
Gate Current (I_{GG1}) at 85°C	7.2mA (see Figure 51)
RF Input Power (RFIN)	33 dBm
Continuous Power Dissipation (P_{DISS}), T_{CASE} = 85°C, Derate 407mW/°C Above 85°C	56.9W
Temperature	
Nominal Peak Channel, T_{CASE} = 85°C, P_{IN} = 28dBm, P_{DISS} = 50.0W at 20GHz	208.0°C
Storage Range	−55°C to +150°C
Operating Range	−40°C to +85°C
Maximum Channel	225°C

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

THERMAL RESISTANCE

Thermal performance is directly linked to printed circuit board (PCB) design and operating environment. Careful attention to PCB thermal design is required.

θ_{JC} is the channel to case thermal resistance where the case is the bottom of the package base.

Table 8. Thermal Resistance

Package Type	θ_{JC}[1]	Unit
EJ-14-1	2.46	°C/W

[1] θ_{JC} was determined by simulation under the following conditions: the heat transfer is due solely to thermal conduction from the channel through the package base to the heatsink. The bottom of the package base is held constant at the operating temperature of 85°C.

ELECTROSTATIC DISCHARGE (ESD) RATINGS

The following ESD information is provided for handling of ESD sensitive devices in an ESD protected area only.

Human body model (HBM) per ANSI/ESDA/JEDEC JS-001.

ESD Ratings for ADPA1112

Table 9. ADPA1112, 14-Lead LDCC

ESD Model	Withstand Threshold (V)	Class
HBM	±500	1B

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

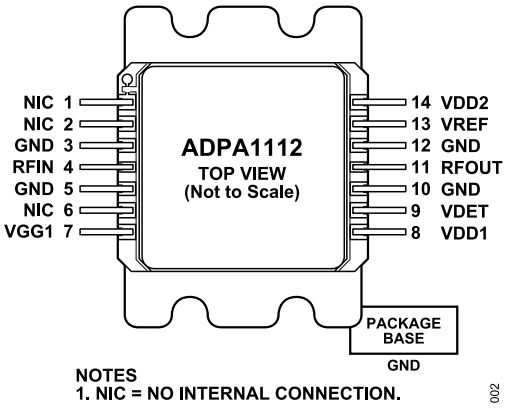

Figure 2. Pin Configuration

Table 10. Pin Function Descriptions

Pin No.	Mnemonic	Description
1, 2, 6	NIC	No Internal Connection. The NIC pins are not connected internally. For normal operation, connect the NIC pins to ground.
3, 5, 10, 12	GND	Ground. The GND pins must be connected to the RF and the DC ground. See Figure 3 for the interface schematic.
4	RFIN	RF Input. The RFIN pin is AC-coupled and matched to 50Ω. See Figure 4 for the interface schematic.
7	VGG1	Gate Bias for the First and Second Gain Stages. Adjust the negative voltage on the VGG1 pin to set I_{DQ} to the desired level. See Figure 8 for the interface schematic.
8	VDD1	Drain Bias for the First Gain Stage. Capacitively bypass as shown in the typical application circuit (see Figure 59). See Figure 7 for the interface schematic.
9	VDET	Detector Diode to Measure the RF Output Power. Used in combination with the VREF pin. The difference in voltage (VREF voltage (V_{REF}) − VDET voltage (V_{DET})) is a temperature compensated DC voltage that is proportional to the RF P_{OUT}. Connect a 40.2kΩ resistor between the VDET pin and 5V to provide the DC bias. See Figure 5 for the interface schematic.
11	RFOUT	RF Output. The RFOUT pin is AC-coupled and matched to 50Ω. See Figure 5 for the interface schematic.
13	VREF	Reference Diode for Temperature Compensation of the VDET RF P_{OUT} Measurements. Connect a 40.2kΩ resistor between the VREF pin and 5V to provide DC bias. See Figure 6 for the interface schematic.
14	VDD2	Drain Bias for the Second Gain Stage. Capacitively bypass as shown in the typical application circuit (see Figure 59). See Figure 5 for the interface schematic.
Package Base	GND	The package base must be connected to the RF and the DC ground. See Figure 3 for the interface schematic.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

INTERFACE SCHEMATICS

Figure 3. GND Interface Schematic

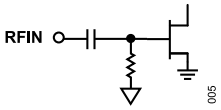

Figure 4. RFIN Interface Schematic

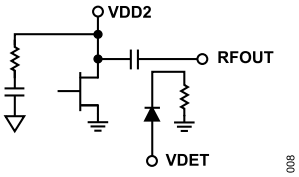

Figure 5. VDD2, VDET, and RFOUT Interface Schematic

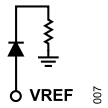

Figure 6. VREF Interface Schematic

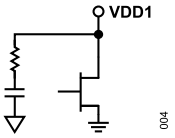

Figure 7. VDD1 Interface Schematic

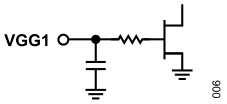

Figure 8. VGG1 interface Schematic

TYPICAL PERFORMANCE CHARACTERISTICS

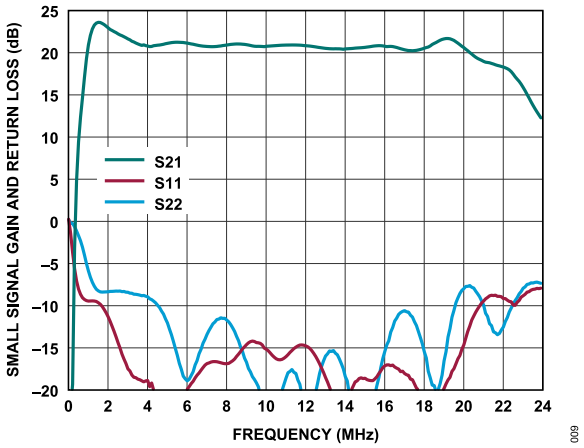

Figure 9. Small Signal Gain and Return Loss vs. Frequency, V_{DD} = 28V, I_{DQ} = 600mA

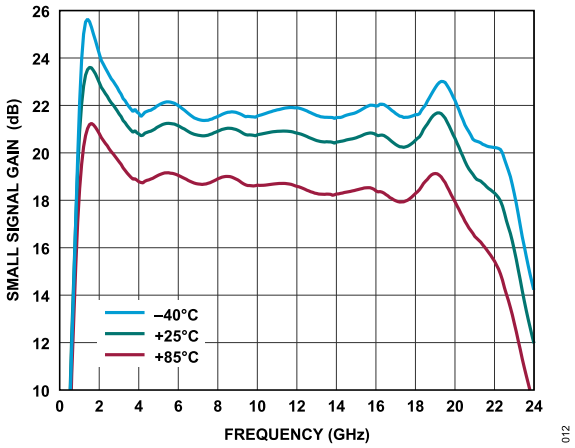

Figure 12. Small Signal Gain vs. Frequency for Various Temperatures, V_{DD} = 28V, I_{DQ} = 600mA

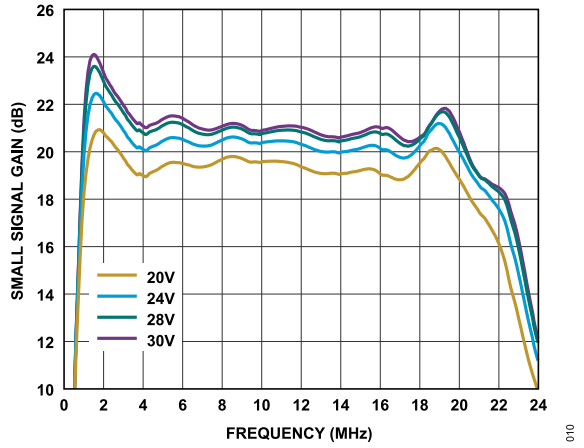

Figure 10. Small Signal Gain vs. Frequency for Various Supply Voltages, I_{DQ} = 600mA

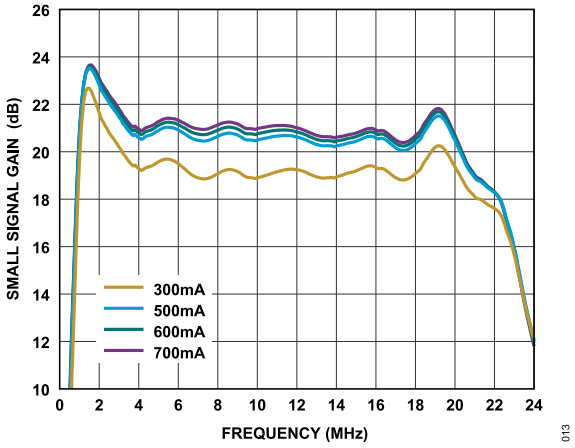

Figure 13. Small Signal Gain vs. Frequency for Various Supply Currents, V_{DD} = 28V

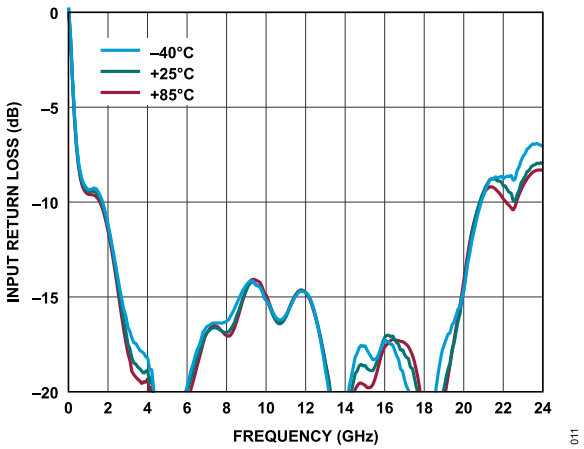

Figure 11. Input Return Loss vs. Frequency for Various Temperatures, V_{DD} = 28V, I_{DQ} = 600mA

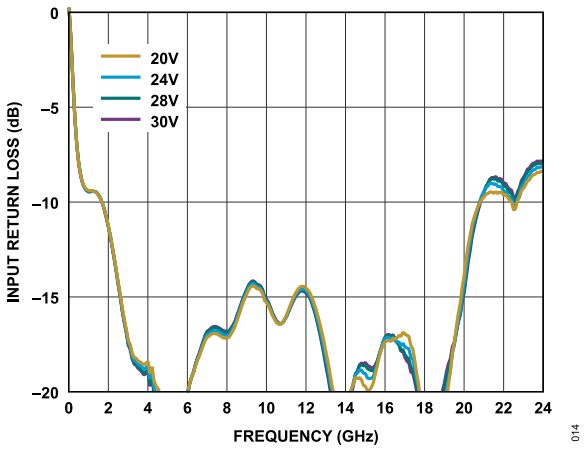

Figure 14. Input Return Loss vs. Frequency for Various Supply Voltages, I_{DQ} = 600mA

TYPICAL PERFORMANCE CHARACTERISTICS

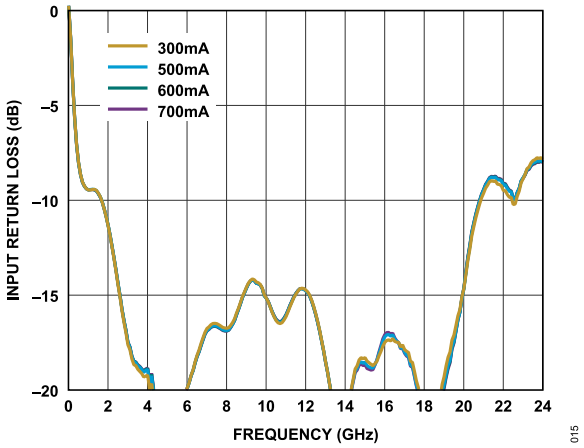

Figure 15. Input Return Loss vs. Frequency for Various Supply Currents, V_{DD} = 28V

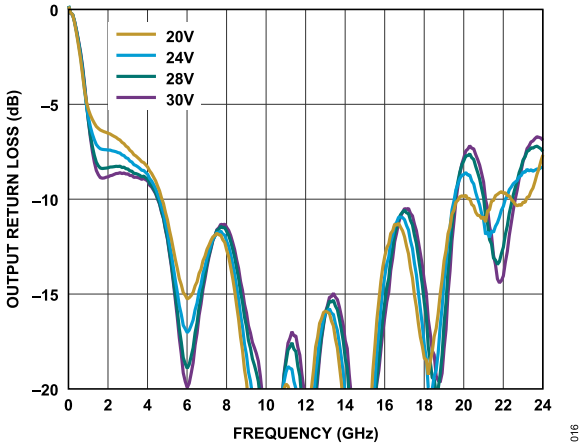

Figure 16. Output Return Loss vs. Frequency for Various Supply Voltages, I_{DQ} = 600mA

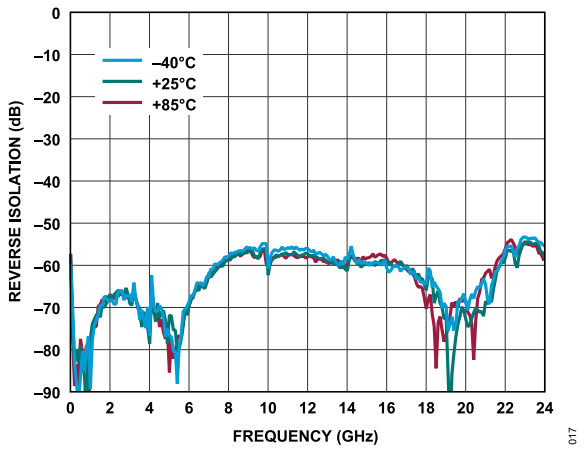

Figure 17. Reverse Isolation vs. Frequency for Various Temperatures, V_{DD} = 28V, I_{DQ} = 600mA

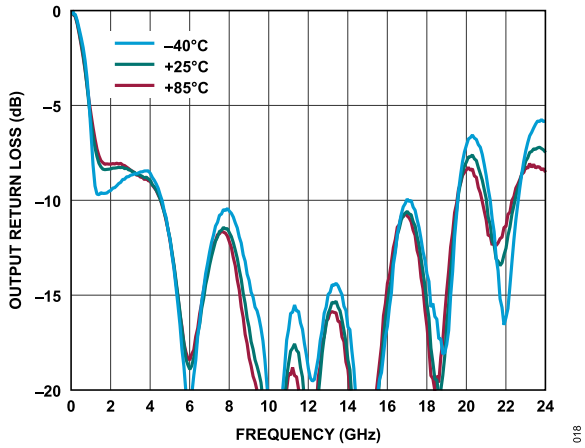

Figure 18. Output Return Loss vs. Frequency for Various Temperatures, V_{DD} = 28V, I_{DQ} = 600mA

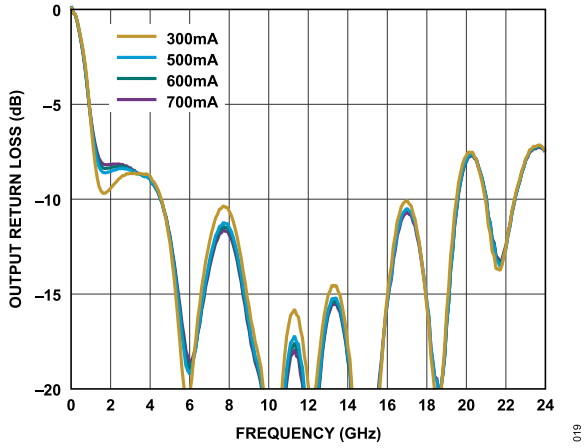

Figure 19. Output Return Loss vs. Frequency for Various Supply Currents, V_{DD} = 28V

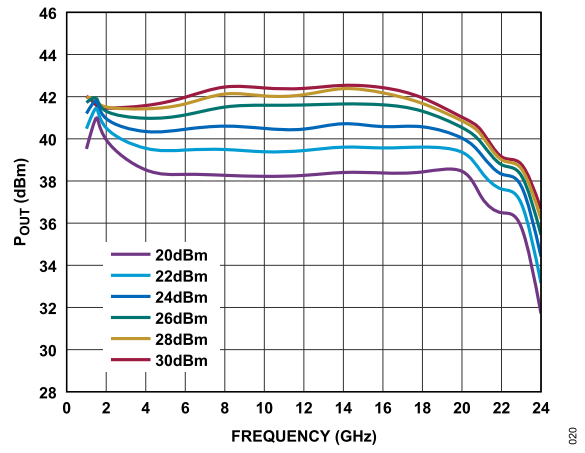

Figure 20. P_{OUT} vs. Frequency for Various P_{IN} Levels, V_{DD} = 28V, I_{DQ} = 600mA

TYPICAL PERFORMANCE CHARACTERISTICS

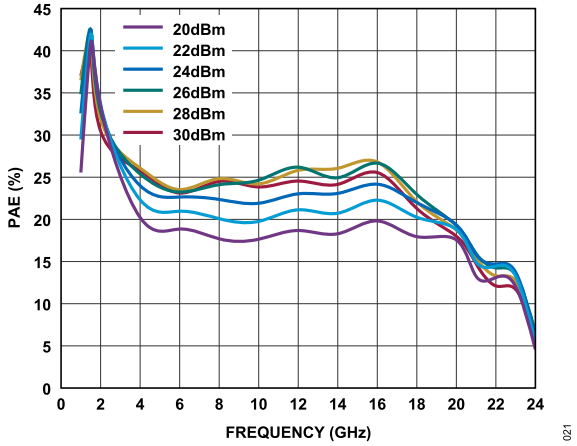

Figure 21. PAE vs. Frequency for Various P_{IN} Levels, V_{DD} = 28V, I_{DQ} = 600mA

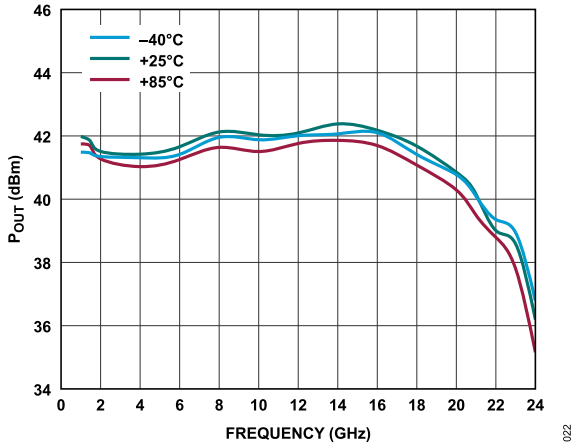

Figure 22. P_{OUT} vs. Frequency at Various Temperatures for P_{IN} = 28dBm, V_{DD} = 28V, I_{DQ} = 600mA

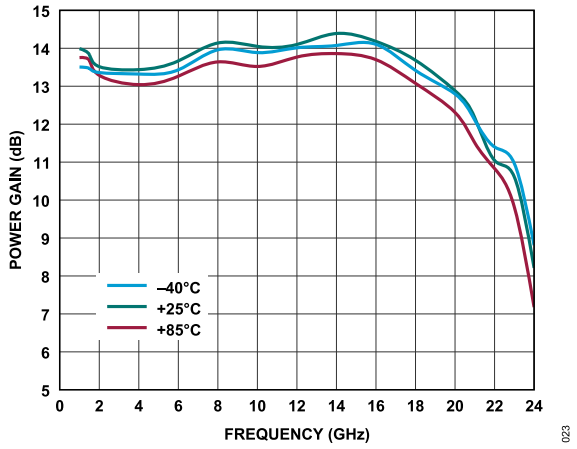

Figure 23. Power Gain vs. Frequency at Various Temperatures for P_{IN} = 28dBm, V_{DD} = 28V, I_{DQ} = 600mA

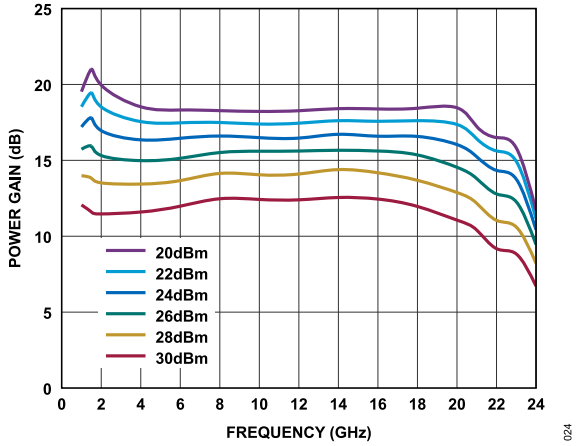

Figure 24. Power Gain vs. Frequency for Various P_{IN} Levels, V_{DD} = 28V, I_{DQ} = 600mA

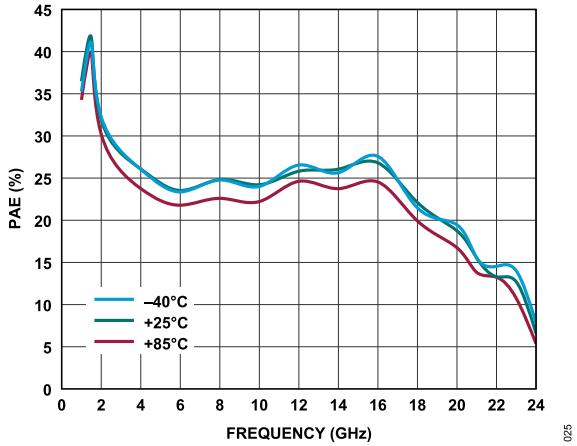

Figure 25. PAE vs. Frequency at Various Temperatures for P_{IN} = 28dBm, V_{DD} = 28V, I_{DQ} = 600mA

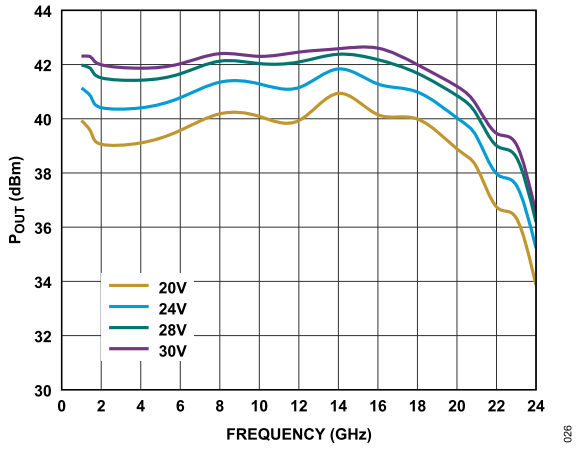

Figure 26. P_{OUT} vs. Frequency for Various Supply Voltages at P_{IN} = 28dBm, I_{DQ} = 600mA

TYPICAL PERFORMANCE CHARACTERISTICS

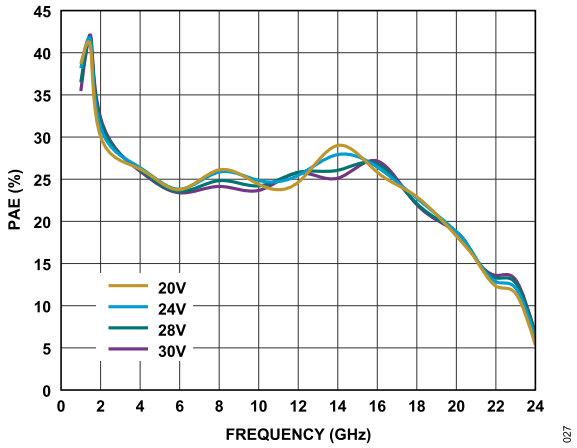

Figure 27. PAE vs. Frequency for Various Supply Voltages at P_{IN} = 28dBm, I_{DQ} = 600mA

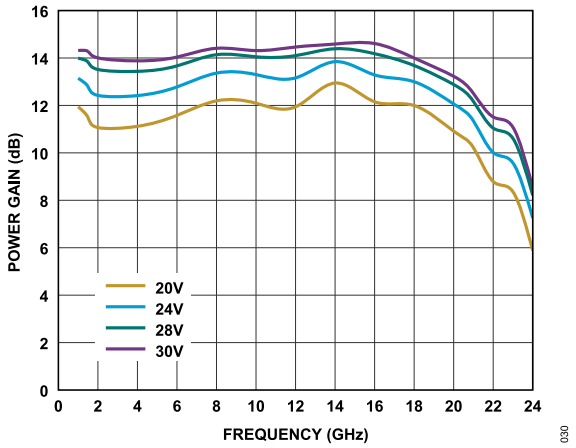

Figure 30. Power Gain vs. Frequency for Various Supply Voltages at P_{IN} = 28dBm I_{DQ} = 600mA

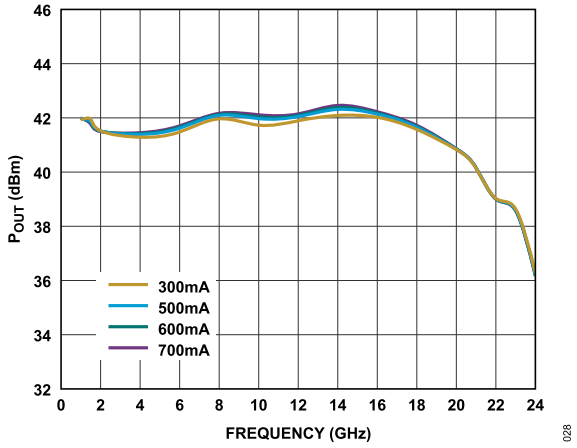

Figure 28. P_{OUT} vs. Frequency for Various Supply Currents at P_{IN} = 28dBm, V_{DD} = 28V

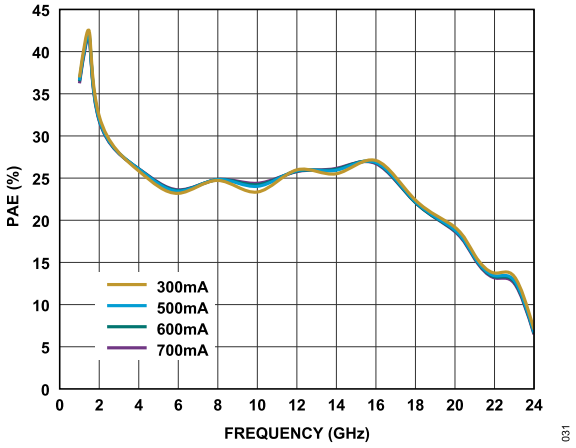

Figure 31. PAE vs. Frequency for Various Supply Currents at P_{IN} = 28dBm, V_{DD} = 28V

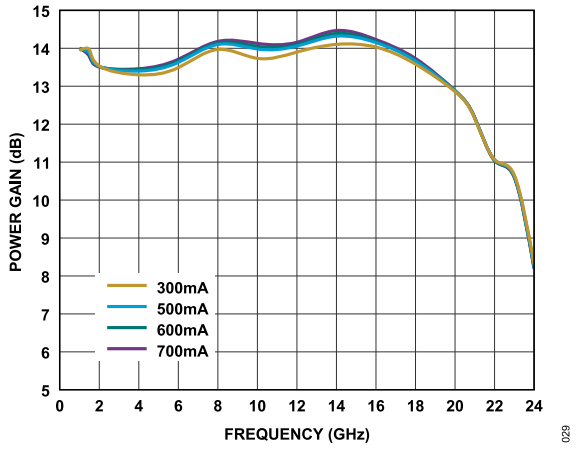

Figure 29. Power Gain vs. Frequency for Various Supply Currents at P_{IN} = 28dBm, V_{DD} = 28V

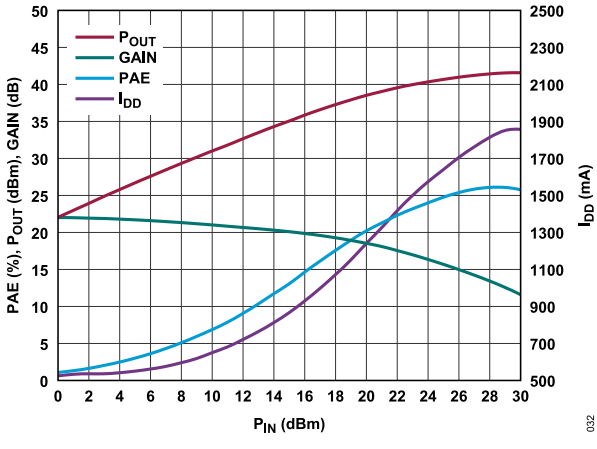

Figure 32. PAE, P_{OUT}, Gain, and Supply Current (I_{DD}) vs. P_{IN} at 4GHz, V_{DD} = 28V, I_{DQ} = 600mA

TYPICAL PERFORMANCE CHARACTERISTICS

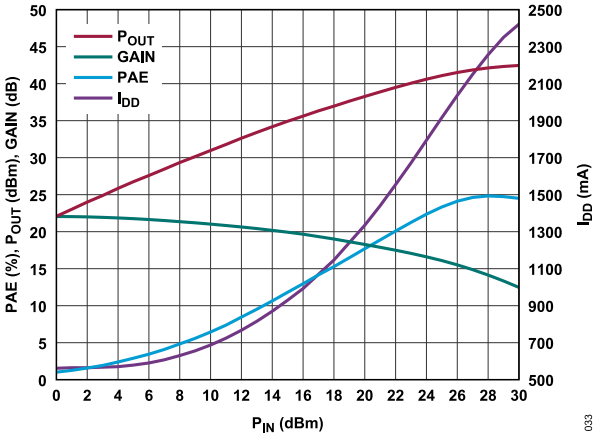

Figure 33. PAE, P_{OUT}, Gain, and I_{DD} vs. P_{IN} at 8GHz, V_{DD} = 28V, I_{DQ} = 600mA

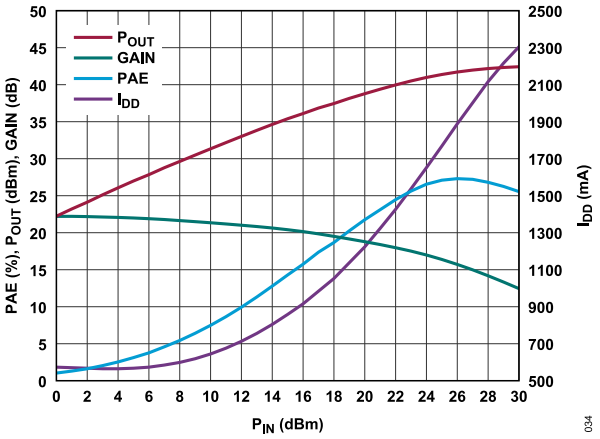

Figure 34. PAE, P_{OUT}, Gain, and I_{DD} vs. P_{IN} at 16GHz, V_{DD} = 28V, I_{DQ} = 600mA

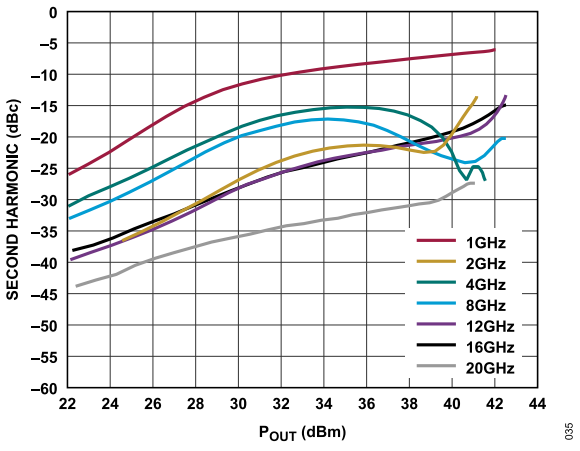

Figure 35. Second Harmonic vs. P_{OUT} for Various Frequencies, V_{DD} = 28V, I_{DQ} = 600mA

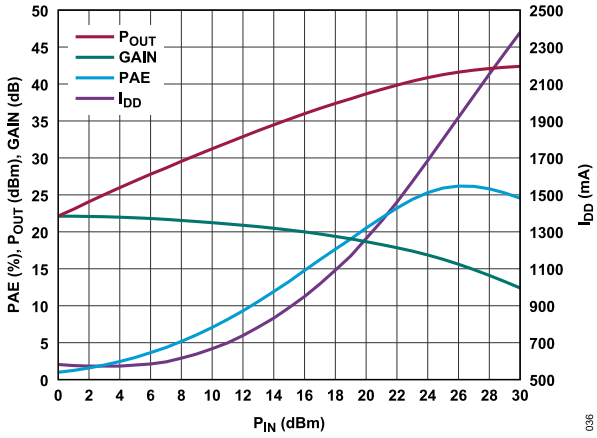

Figure 36. PAE, P_{OUT}, Gain, and I_{DD} vs. P_{IN} at 12GHz, V_{DD} = 28V, I_{DQ} = 600mA

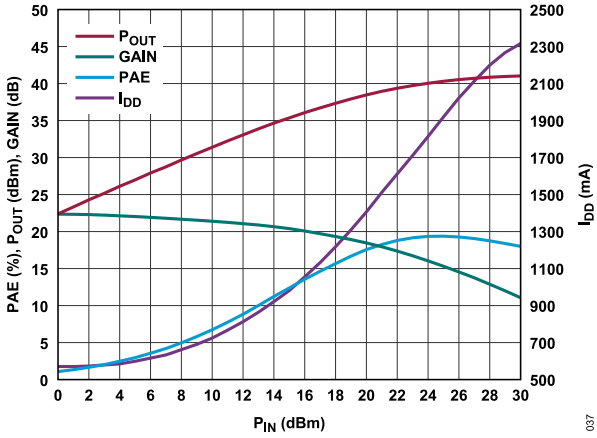

Figure 37. PAE, P_{OUT}, Gain, and I_{DD} vs. P_{IN} at 20GHz, V_{DD} = 28V, I_{DQ} = 600mA

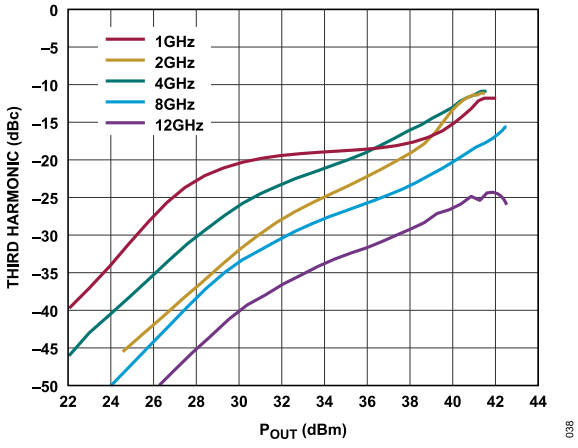

Figure 38. Third Harmonic vs. P_{OUT} for Various Frequencies, V_{DD} = 28V, I_{DQ} = 600mA

TYPICAL PERFORMANCE CHARACTERISTICS

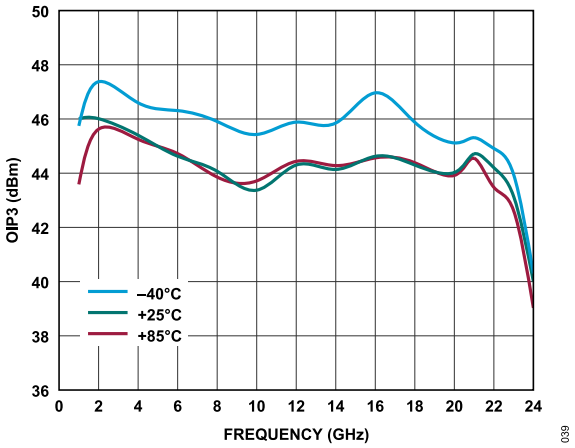

Figure 39. OIP3 vs. Frequency for Various Temperatures at P_{OUT} per Tone = 32dBm, V_{DD} = 28V, I_{DQ} = 600mA

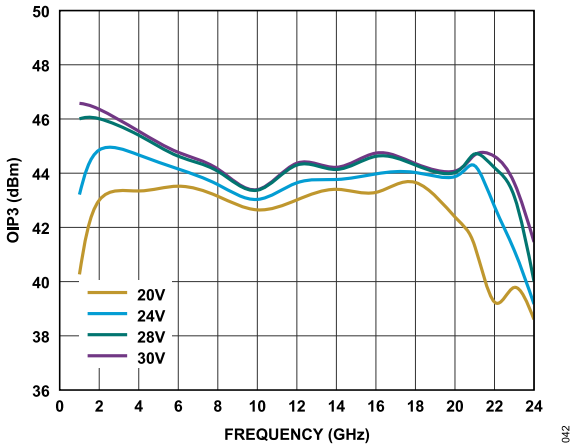

Figure 42. OIP3 vs. Frequency for Various Supply Voltages at P_{OUT} per Tone = 32dBm, I_{DQ} = 600mA

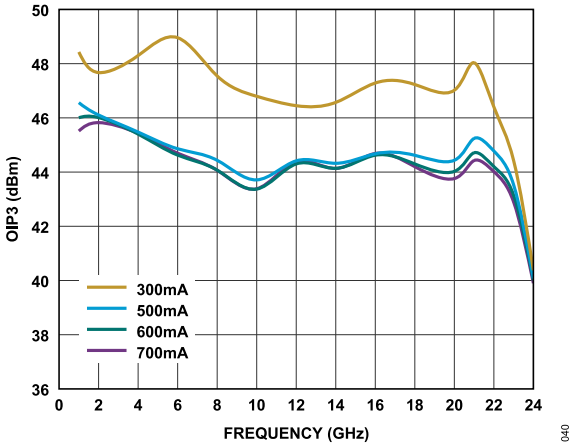

Figure 40. OIP3 vs. Frequency for Various Supply Currents at P_{OUT} per Tone = 32dBm, V_{DD} = 28V, I_{DQ} = 600mA

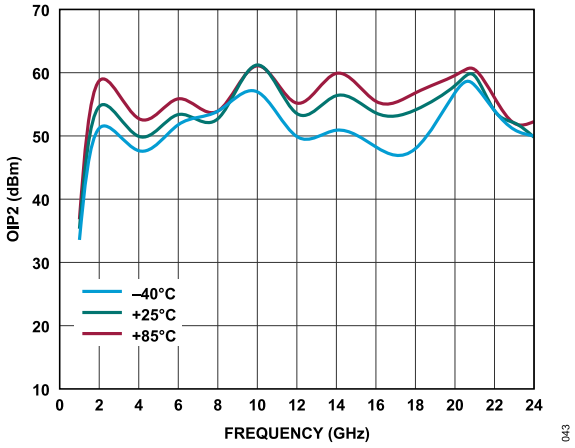

Figure 43. OIP2 vs. Frequency for Various Temperatures at P_{OUT} per Tone = 32dBm V_{DD} = 28V, I_{DQ} = 600mA

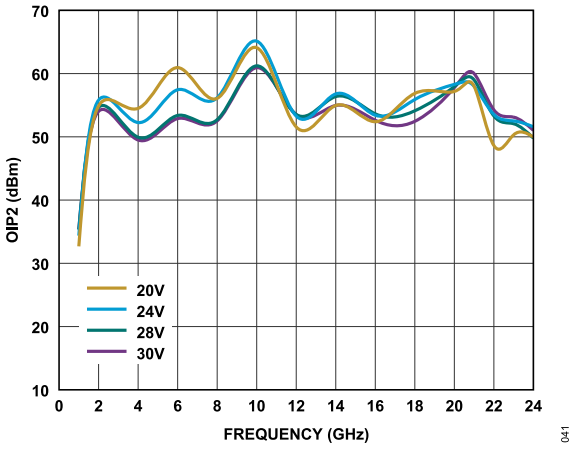

Figure 41. OIP2 vs. Frequency for Various Supply Voltages at P_{OUT} per Tone = 32dBm I_{DQ} = 600mA

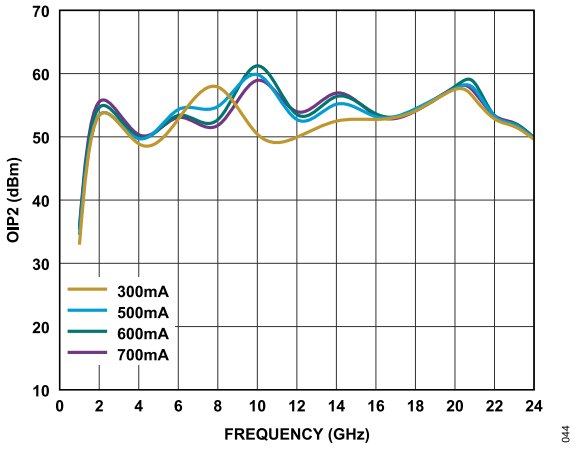

Figure 44. OIP2 vs. Frequency for Various Supply Currents at P_{OUT} per Tone = 32dBm V_{DD} = 28V

TYPICAL PERFORMANCE CHARACTERISTICS

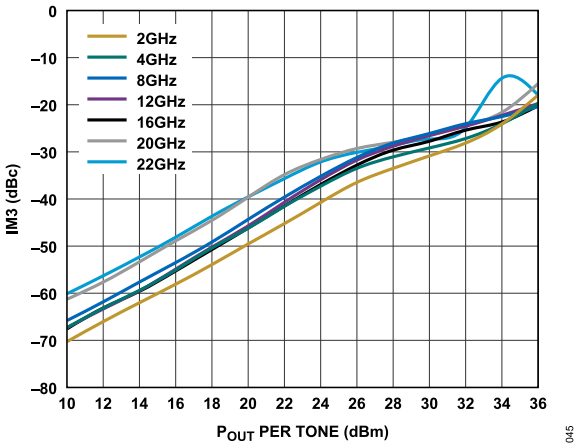

Figure 45. IM3 vs. P_{OUT} per Tone for Various Frequencies, V_{DD} = 28V, I_{DQ} = 600mA

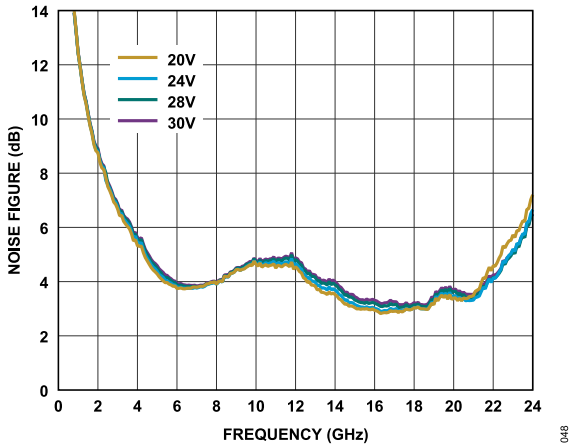

Figure 48. Noise Figure vs. Frequency for Various Supply Voltages, I_{DQ} = 600mA

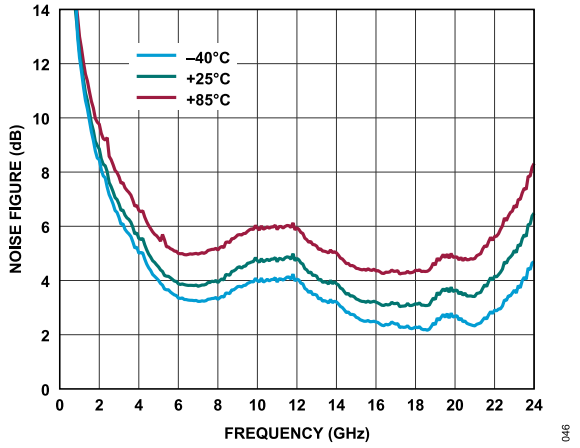

Figure 46. Noise Figure vs. Frequency for Various Temperatures, V_{DD} = 28V, I_{DQ} = 600mA

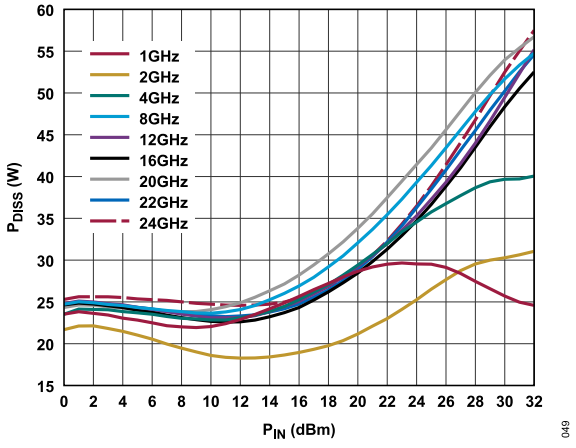

Figure 49. P_{DISS} vs. P_{IN} for Various Frequencies at T_{CASE} = 85°C, V_{DD} = 28V, I_{DQ} = 600mA

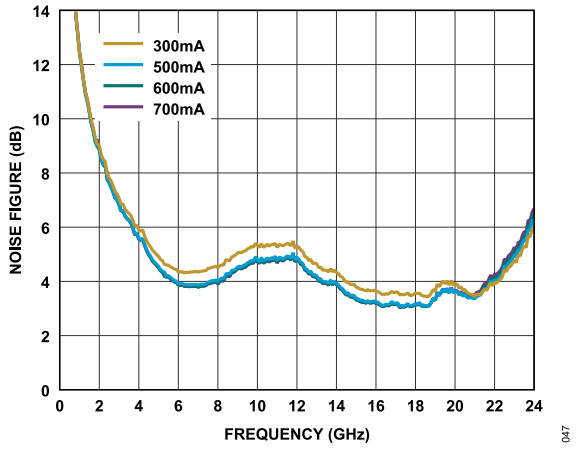

Figure 47. Noise Figure vs. Frequency for Various Supply Currents, V_{DD} = 28V

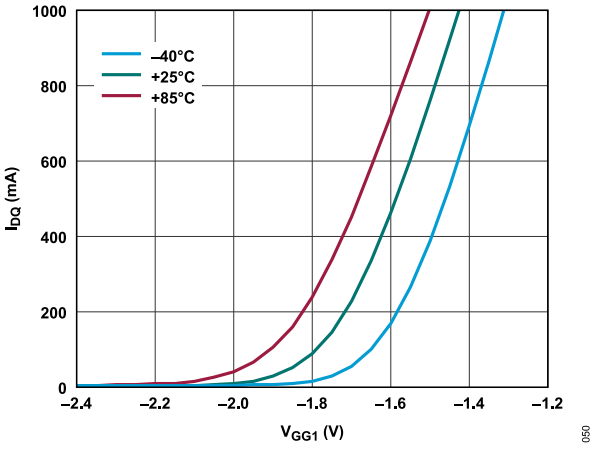

Figure 50. I_{DQ} vs. V_{GG1} for Various Temperatures, V_{DD} = 28V

TYPICAL PERFORMANCE CHARACTERISTICS

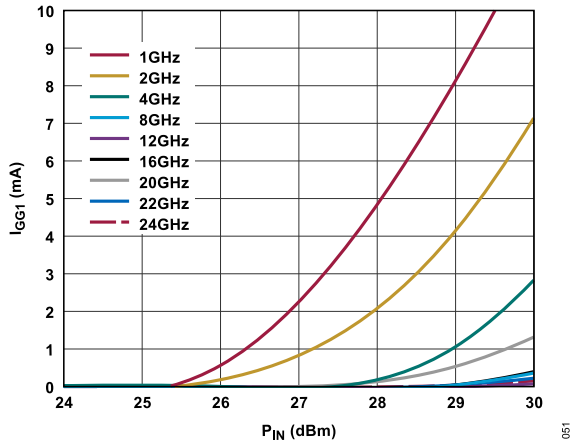

Figure 51. I_{GG1} vs. P_{IN} for Various Frequencies at T_{CASE} = 85°C, V_{DD} = 28V, I_{DQ} = 600mA

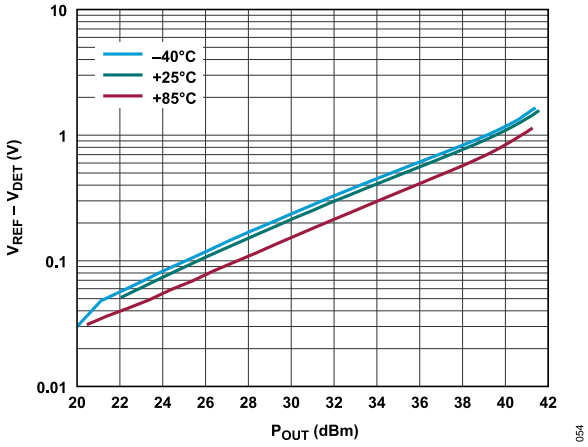

Figure 54. V_{REF} – V_{DET} vs. P_{OUT} for Various Temperature at 4GHz, V_{DD} = 28V, I_{DQ} = 600mA

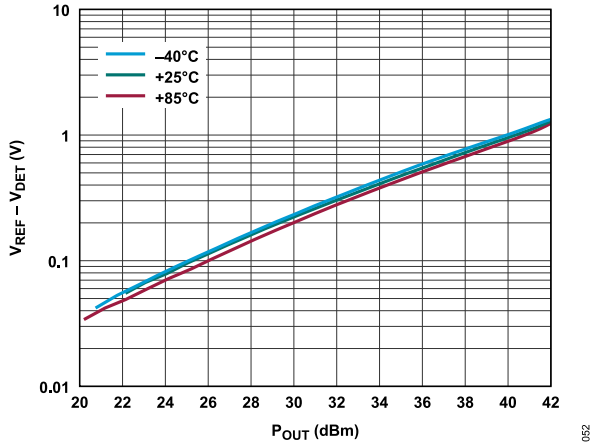

Figure 52. V_{REF} – V_{DET} vs. P_{OUT} for Various Temperature at 12GHz, V_{DD} = 28V, I_{DQ} = 600mA

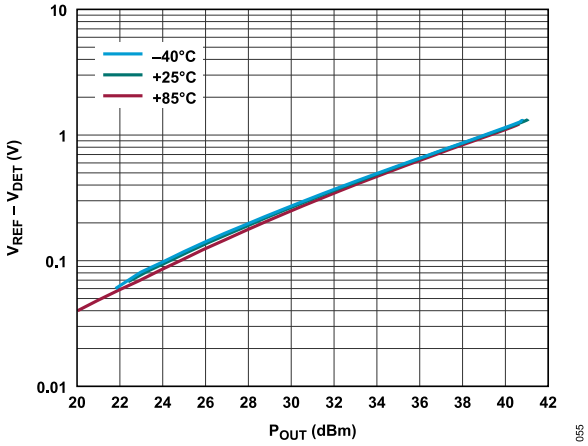

Figure 55. V_{REF} – V_{DET} vs. P_{OUT} for Various Temperature at 20GHz, V_{DD} = 28V, I_{DQ} = 600mA

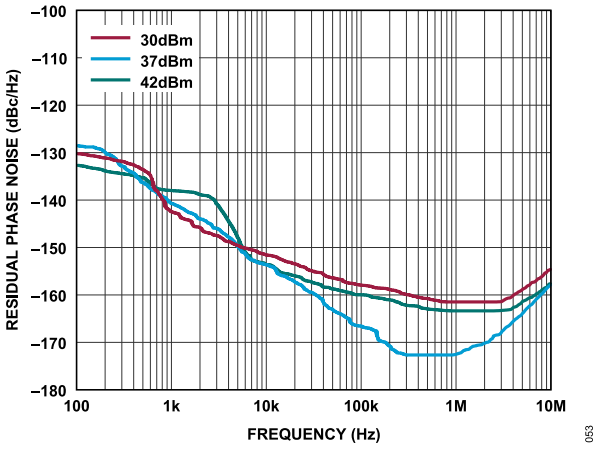

Figure 53. Residual Phase Noise vs. Frequency for Various P_{OUT} Levels at 2GHz, V_{DD} = 28V, I_{DQ} = 600mA

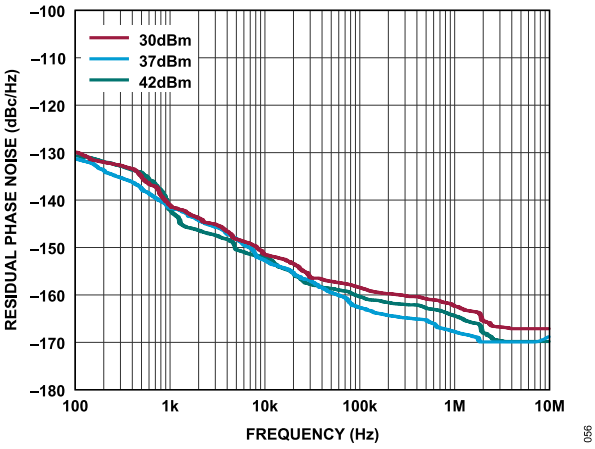

Figure 56. Residual Phase Noise vs. Frequency for Various P_{OUT} Levels at 10GHz, V_{DD} = 28V, I_{DQ} = 600mA

TYPICAL PERFORMANCE CHARACTERISTICS

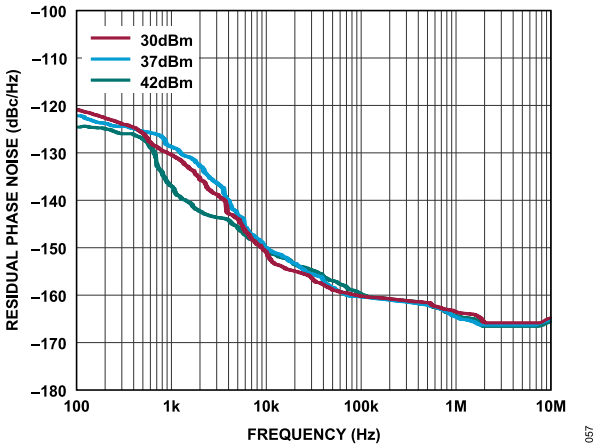

Figure 57. Residual Phase Noise vs. Frequency for Various P_{OUT} Levels at 16GHz, V_{DD} = 28V, I_{DQ} = 600mA

THEORY OF OPERATION

The ADPA1112 is a GaN power amplifier with cascaded gain stages that are biased by a positive drain supply (V_{DD1} and V_{DD2}) and an externally applied negative gate voltage (V_{GG1}). A nominal 28V is applied to the first and second stage drains (VDD1 and VDD2) and a negative voltage is applied to VGG1 to set the total I_{DQ} to 600mA nominal.

When biased as described, the ADPA1112 operates in Class AB, resulting in the maximum PAE at saturation. The ADPA1112 features integrated RF chokes for each drain plus on-chip DC blocking of the RFIN and RFOUT ports.

A portion of the RF output signal is directionally coupled to a diode for detection of the RF P_{OUT}. When the diode is DC biased, the diode rectifies the coupled RF power and makes it available for measurement as a DC voltage at VDET. To allow temperature compensation of VDET, an identical and symmetrically located circuit without the coupled RF power is available through VREF. Taking the difference of V_{REF} − V_{DET} provides a temperature-compensated signal that is proportional to the RF output.

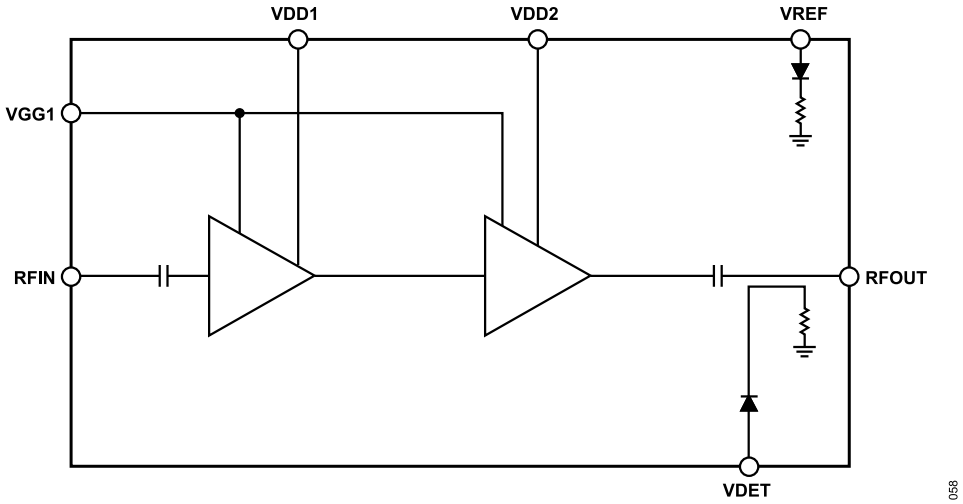

Figure 58. Basic Block Diagram

APPLICATIONS INFORMATION

BASIC CONNECTIONS

The basic connections to operate the ADPA1112 are shown in Figure 59. Decouple the VDD1, VDD2, and VGG1 pins as shown in Figure 59. The gate voltage for all stages (−3.0 V to −1.0 V for biased operation and −4.0 V for pinch off) is applied to the VGG1 pin. A V_{DD} of 28 V nominal is applied to the VDD1 and VDD2 pins. Pin 1, Pin 2, and Pin 6 are designated as NIC pins. Although these NIC pins are not internally connected, the NIC pins were all connected to ground during the characterization of the device.

To turn on the ADPA1112, take the following steps:

1. Connect the power supply grounds to GND.
2. Set V_{GG1} to −4V.
3. Set V_{DD1} and V_{DD2} to 28V.
4. Adjust V_{GG1} more positive to achieve an I_{DQ} of 600mA, approximately −2V.
5. Apply to the RF signal.

To turn off the ADPA1112, take the following steps:

1. Turn off the RF signal.
2. Set V_{GG1} to −4V to achieve an I_{DQ} of 0mA.
3. Set the voltage on V_{DD1} and V_{DD2} to 0V.
4. Increase V_{GG1} to 0V.

SOLDERING AND ASSEMBLY CONSIDERATIONS

The ADPA1112 is a nonhermetic air cavity device. The body of the package normally sits within a cutout in the PCB that allows direct access to a heatsink beneath the PCB. To facilitate good thermal and electrical conduction to the heatsink, a shim of electrically and thermally conductive material, such as Heat-Spring indium from Indium Corporation, can be used. (Alternatively, electrically and thermally conductive paste or grease can be used). The shim is placed between the heatsink and the bottom of the package base. Then, the package can be attached to the heatsink using screws (typically). Once attached with the screw hardware, the pins must be flush with the PCB, which allows the leads to be soldered to the PCB pads.

TYPICAL APPLICATION CIRCUIT

Figure 59 shows the typical application circuit.

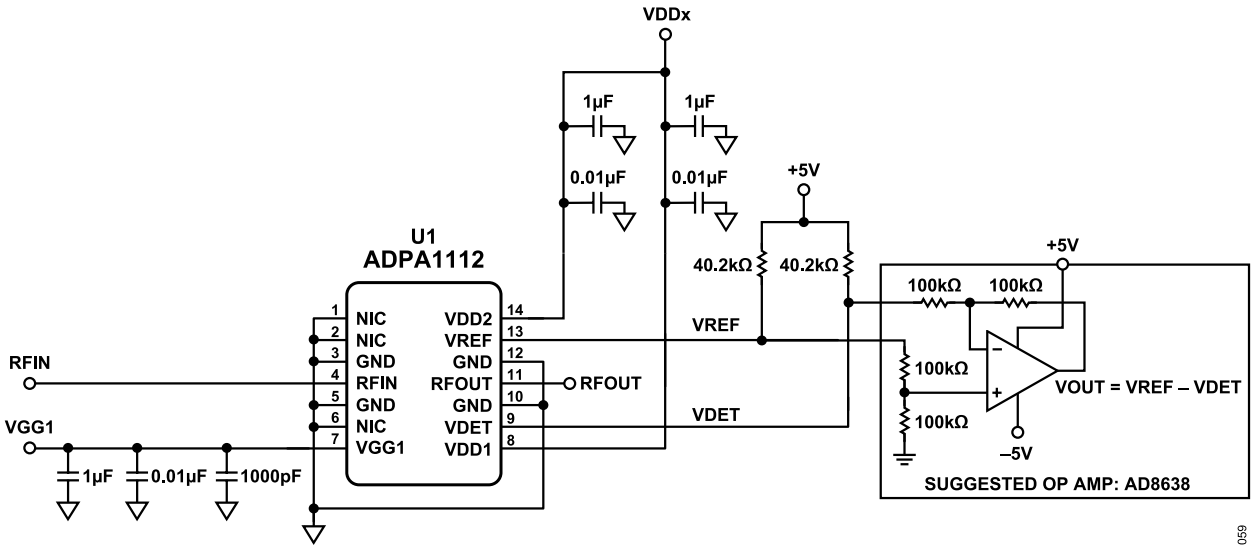

Figure 59. Typical Application Circuit

OUTLINE DIMENSIONS

Package Drawing Option	Package Type	Package Description
EJ-14-1	LDCC	14-Lead Ceramic Leaded Chip Carrier Package

For the latest package outline information and land patterns (footprints), go to Package Index.

ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Packing Quantity	Package Option
ADPA1112AEJZ	−40°C to +85°C	14-Lead Ceramic Leaded Chip Carrier [LDCC]	Tray, 1	EJ-14-1
ADPA1112AEJZ-50	−40°C to +85°C	14-Lead Ceramic Leaded Chip Carrier [LDCC]	Tray, 50	EJ-14-1

[1] Z = RoHS Compliant Part.

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