Data Sheet

ADMV1355

17.7GHz to 55GHz, Wideband, Microwave Upconverter

FEATURES

- Wideband RF output frequency range: 17.7GHz to 55GHz
- Integrated RF chain features
  - Tunable sideband rejection filters
  - Gain control DSAs
- Integrated LO chain features
  - Input frequency range: 8.85GHz to 27.5GHz
  - Internal 2× multiplier
  - Tunable LO harmonic rejection filter
  - I/Q phase correction
- Three frequency translation modes
  - Baseband I/Q differential input: DC to 12GHz
  - IF hybrid input: 8GHz to 12GHz
  - Complex IF input: 1GHz to 12GHz
- Programmable features
  - Sideband rejection optimization
  - LO carrier feedthrough calibration
- Simple SPI: 3-wire or 4-wire
- General-purpose logic outputs for integration with other chips in a system
- LUT logic inputs for fast frequency hopping applications
- 120-ball, 6mm × 6.5mm, CSP_BGA package

APPLICATIONS

- Satellite payload[1] and ground stations (SATCOM)
- Wideband radar and electronic warfare systems (EW)
- Instrumentation and automatic test equipment (ATE)
- Millimeter-wave 5G and 6G testers

[1]*For information regarding commercial space low (CSL) or commercial space high (CSH) qualified versions of the ADMV1355, contact space@analog.com.*

GENERAL DESCRIPTION

The ADMV1355 is a highly integrated microwave upconverter optimized for wideband radio designs operating in the 17.7GHz to 55GHz RF range. Provides a compact alternative to traditional multichip solutions, significantly reducing system size, weight, and power consumption.

The integrated local oscillator (LO) signal chain accepts LO input signals in the 8.85GHz to 27.5GHz range. In the LO signal chain, there are internal amplifiers, a 2× frequency multiplier, programmable harmonic-reject filter, and phase-adjust circuitry that generates the necessary 17.7GHz to 55GHz signal to drive the inphase/quadrature (I/Q) mixer.

The ADMV1355 offers three frequency translation mixer modes: IF hybrid input, complex IF input, and baseband I/Q differential input. The IF hybrid input mode utilizes one intermediate frequency (IF) input signal in the 8GHz to 12GHz range, which then passes through an on-chip 90° IF hybrid. The IF hybrid coupler produces the necessary quadrature signals for the mixer. The complex IF input mode utilizes two quadrature IF input signals in the 1GHz to 12GHz range. The baseband I/Q differential input mode utilizes differential baseband I/Q input signals from DC to 12GHz.

Immediately following the mixer are two, switch-selectable RF output driver signal chains. The low band signal chain operates from 17.7GHz to 34GHz, and the high band signal chain operates from 30GHz to 55GHz. Each signal chain has multiple stages of signal level control and harmonic filtering.

The RF output, LO input, and IF input pins are all single-ended and matched to 50Ω impedance, and the differential baseband I/Q input pins are matched to a 100Ω differential impedance. Note that no external matching circuitry is required.

Integrated gain and frequency look-up tables (LUTs) are provided and can be addressed through the serial peripheral interface (SPI) or directly using the ADD_Fx and ADD_Gx ball connections to allow fast switching for frequency hopping applications.

Incorporated within the ADMV1355 is a simple SPI that can operate in either a 3-wire or 4-wire implementation. The SPI allows programming all on-chip adjustable functions, such as gain control, LO feedthrough adjustment, sideband rejection optimization, tunable filters, general-purpose logic outputs, and LUTs.

The ADMV1355 upconverter is offered in a 120-ball CSP_BGA package that supports heat sinking either from the top of the package or through the bottom of the printed circuit board (PCB). Either method of heat sinking has similar thermal performance and is acceptable to efficiently control the T_C. The ADMV1355 operates over the −40°C to +95°C temperature range.

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REVISION HISTORY

10/2026—Rev. 0 to Rev. A

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4/2026—Revision 0: Initial Version

FUNCTIONAL BLOCK DIAGRAM

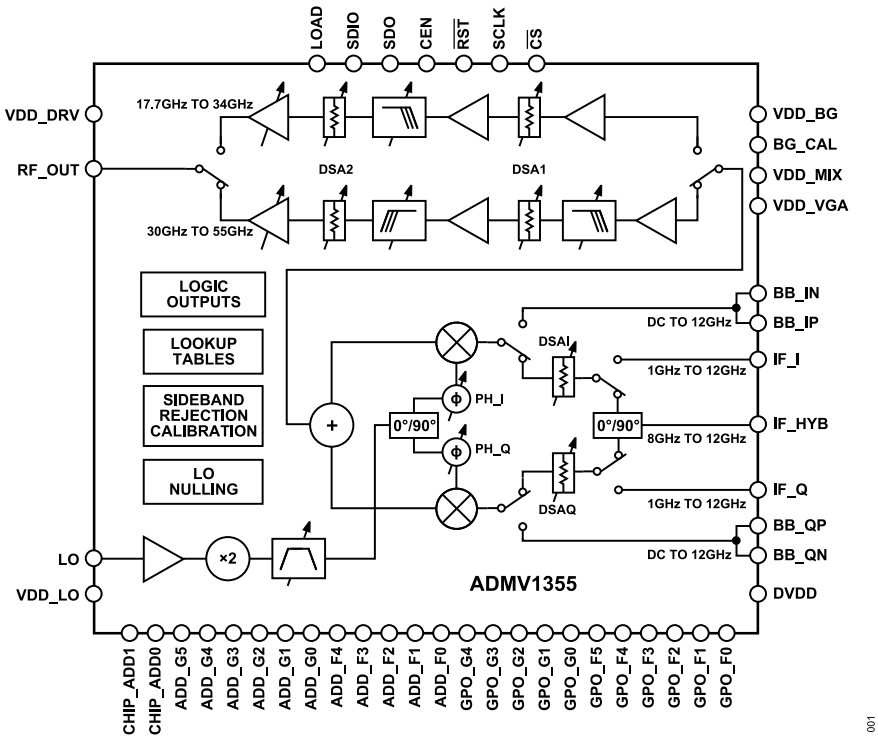


Figure 1. Functional Block Diagram

SPECIFICATIONS

T_C = 25°C, VDD_DRV = 3V, all other supply voltages = 1.8V, and LO power (P_{LO}) = −5 dBm, unless otherwise noted.

Table 1. Specifications

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
FREQUENCY RANGES					
RF Output (f_{RF})					
Low Band Signal Chain		17.7		34	GHz
High Band Signal Chain		30		55	GHz
LO Input (f_{LO})		8.85		27.5	GHz
2× LO Multiplier (2× f_{LO})		17.7		55	GHz
IF Hybrid Input		8		12	GHz
Complex IF Input		1		12	GHz
High Frequency Mode		3		12	GHz
Low Frequency Mode		1		4	GHz
Baseband I/Q Differential Input		DC		12	GHz
LO AMPLITUDE RANGE					
f_{LO} < 25GHz		−7		−3	dBm
f_{LO} ≥ 25GHz		−3		0	dBm
OPERATING TEMPERATURE RANGE		−40		+95	°C
DIGITAL STEP ATTENUATOR (DSA) PERFORMANCE					
Full Attenuation Range	DSA1 and DSA2		30		dB
Attenuation Step Size	DSA1 and DSA2		1		dB
Step Error	DSA1, RF high band		±0.3		dB
	DSA2, RF high band		± 0.4		dB
	DSA1, RF low band		± 0.5		dB
	DSA2, RF low band		±0.5		dB
SIDEBAND REJECTION CONTROL					
LO Phase Adjustment			±20		Degrees
LO Phase Step			0.6		Degrees
IF Amplitude Step Size			0.1		dB
BASEBAND INPUT COMMON-MODE VOLTAGE (V_{ICM})	Externally generated	0		1.55	V
RETURN LOSS					
IF Hybrid Input	50Ω single-ended		−17		dB
Complex IF Input	50Ω single-ended				
High Frequency Mode			−7		dB
Low Frequency Mode			−8		dB
LO Input	50Ω single-ended		−8		dB
RF_OUT Output	50Ω single-ended				
Low Band	17GHz to 34GHz		−10		dB
High Band	30GHz to 55GHz		−8		dB
LOGIC INPUTS					
Input High Voltage (V_{INH})		1.2		1.8	V
Input Low Voltage (V_{INL})			0	0.63	V
High and Low Input Current (I_{INH}/I_{INL})			100		µA
Input Capacitance (C_{IN})			0.4		pF
LOGIC OUTPUTS					
Output High Voltage (V_{OH})	Output high current (I_{OH}) = 8mA	1.35			V
Output Low Voltage (V_{OL})	Output low current (I_{OL}) = 8mA			0.45	V
Minimum Hysteresis Window			160		mV

SPECIFICATIONS

Table 1. Specifications (Continued)

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
POWER SUPPLIES					
DVDD		1.6	1.8	2	V
VDD_BG		1.6	1.8	2	V
VDD_LO		1.6	1.8	2	V
VDD_MIX		1.6	1.8	2	V
VDD_VGA		1.6	1.8	2	V
VDD_DRV		2.85	3	3.3	V
Supply Current					
1.8V Supplies	CEN high and RF Band 0		516		mA
	CEN high and RF Band 1		600		mA
	CEN low		48		mA
3V Supply	CEN high and RF Band 0		84		mA
	CEN high and RF Band 1		84		mA
	CEN low		2		mA

SPECIFICATIONS

IF HYBRID MODE

IF_HYB Input, High Band

T_C = 25°C, VDD_DRV = 3V, all other supply voltages = 1.8V, IF power (P_{IF}) = −20dBm, LO power (P_{LO}) = −5dBm, IF frequency (f_{IF}) = 8GHz, upper sideband, maximum gain, RF low-pass filter (LPF) setting = 0x00 (highest cutoff), and RF high-pass filter (HPF) setting = 0x3F (lowest cutoff), unless otherwise noted.

Table 2. IF_HYB Input, High Band

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
IF HYBRID MODE, HIGH BAND					
Conversion Gain			16		dB
Single Sideband Noise Figure			21		dB
Output 1dB Compression (P1dB)			16		dBm
Output Third-Order Intercept (IP3)	100MHz tone spacing		25		dBm
Sideband Rejection	No RF filtering applied				
	Uncalibrated		−30		dBc
	Calibrated		−40		dBc

IF_HYB Input, Low Band

T_C = 25°C, VDD_DRV = 3V, all other supply voltages = 1.8V, P_{IF} = −20dBm, P_{LO} = −5dBm, f_{IF} = 8GHz, lower sideband, maximum gain, and RF LPF setting = 0x00 (highest cutoff), unless otherwise noted.

Table 3. IF_HYB Input, Low Band

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
IF HYBRID MODE, LOW BAND					
Conversion Gain			19		dB
Single Sideband Noise Figure			23		dB
Output P1dB			19		dBm
Output IP3	100MHz tone spacing		26		dBm
Sideband Rejection	No RF filtering applied				
	Uncalibrated		−20		dBc
	Calibrated		−45		dBc

SPECIFICATIONS

COMPLEX IF MODE

IF_x Inputs, High Band

T_C = 25°C, VDD_DRV = 3V, all other supply voltages = 1.8V, P_{IF} = −21dBm, P_{LO} = −5dBm, f_{IF} = 1GHz, upper sideband, maximum gain, RF LPF setting = 0x00 (highest cutoff), and RF HPF setting = 0x3F (lowest cutoff). Measurements were performed using external 90° hybrid, with losses de-embedded, unless otherwise noted.

Table 4. IF_I and IF_Q Inputs, High Band

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
COMPLEX IF MODE, HIGH BAND					
Conversion Gain			18		dB
Single Sideband Noise Figure	<52GHz		16		dB
Output P1dB			17		dBm
Output IP3	100MHz tone spacing		25		dBm
Sideband Rejection	No RF filtering applied				
	Low frequency mode, uncalibrated		−30		dBc
	Low frequency mode, calibrated		−50		dBc
	High frequency mode, uncalibrated		−35		dBc
	High frequency mode, calibrated		−45		dBc

IF_x Inputs, Low Band

T_C = 25°C, VDD_DRV = 3V, all other supply voltages = 1.8V, P_{IF} = −21dBm, P_{LO} = −5dBm, f_{IF} = 1GHz, lower sideband, maximum gain, and RF LPF setting = 0x00 (highest cutoff). Measurements were performed using external 90° hybrid, with losses de-embedded, unless otherwise noted.

Table 5. IF_I and IF_Q Inputs, Low Band

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
COMPLEX IF MODE, LOW BAND					
Conversion Gain			23		dB
Single Sideband Noise Figure			18.5		dB
Output P1dB			19		dBm
Output IP3	100MHz tone spacing		27		dBm
Sideband Rejection	No RF filtering applied				
	Low frequency mode, uncalibrated		−25		dBc
	Low frequency mode, calibrated		−35		dBc
	High frequency mode, uncalibrated		−25		dBc
	High frequency mode, calibrated		−40		dBc

SPECIFICATIONS

I/Q BASEBAND MODE

BB_Ix and BB_Qx Inputs, High Band

T_C = 25°C, VDD_DRV = 3V, all other supply voltages = 1.8V, baseband power (P_{BB}) = −20dBm, P_{LO} = 0dBm, baseband frequency (f_{BB}) = 100MHz, upper sideband, maximum gain, RF LPF setting = 0x00 (highest cutoff), RF HPF setting = 0x3F (lowest cutoff), and V_{ICM} = 1V. Measurements were performed with the baseband ports driven externally, with losses de-embedded, unless otherwise noted.

Table 6. BBB_IP, BB_IN, BB_QP, and BB_QN Inputs, High Band

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
I/Q BASEBAND MODE, HIGH BAND					
Conversion Gain			26		dB
Noise Figure, Single Sideband			13		dB
Output P1dB			16		dBm
Ouput IP3	100MHz tone spacing		25		dBm
Sideband Rejection	No RF filtering applied				
	Uncalibrated		−20		dBc
	Calibrated with internal phase correction only		−35		dBc
	Calibrated using the AD9084 Apollo external digital-to-analog converters (DACs) with amplitude and phase correction		−60		dBc
Baseband Quadrature Imbalance	Using Apollo external DACs				
Amplitude			±0.9		dB
Phase			±16		Degrees

BB_Ix and BB_Qx Inputs, Low Band

T_C = 25°C, VDD_DRV = 3V, all other supply voltages = 1.8V, P_{BB} = −20dBm, P_{LO} = 0dBm, f_{BB} = 100MHz, lower sideband, maximum gain, RF LPF setting = 0x00 (highest cutoff), and V_{ICM} = 1V. Measurements were performed with the baseband ports driven externally, with losses de-embedded, unless otherwise noted.

Table 7. BB_IP, BB_IN, BB_QP, and BB_QN Inputs, Low Band

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
I/Q BASEBAND MODE, LOW BAND					
Conversion Gain			26		dB
Output P1dB			20		dBm
Output IP3	100MHz tone spacing		26		dBm
Sideband Rejection	No RF filtering applied				
	Uncalibrated		−30		dBc
	Calibrated		−35		dBc
Baseband Quadrature Imbalance	Using Apollo external DACs				
Amplitude			±0.9		dB
Phase			±16		Degrees

SPECIFICATIONS

TIMING SPECIFICATIONS

See the Timing Diagrams Overview section, the Power-Up and Apply the Digital Inputs section, the Initialization SPI Instructions section, the Chip Enable and Operation section, the Chip Disable and Reset section, and the Chip Disable and Power-Down section for additional information.

Table 8. Timing Specifications

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
t_1	1		100	ms	Power supplies 10% to 90% rise time.
t_2	10			ns	Power supplies 90% level to valid digital input time ($t_{DIGITAL}$). Do not set any logic input levels high prior to $t_{DIGITAL}$. The $\overline{RST}$ and $\overline{CS}$ can go high together after t_2 has transpired. If CHIP_ADD0 and CHIP_ADD1 are to be set externally, then set them to the desired logic levels after t_2 and prior to any SPI instructions.
t_3	10			ns	$\overline{RST}$ rising edge to $\overline{CS}$ falling edge (first SPI instruction after reset). Waiting t_3 ensures that the digital logic has reset to the default values.
t_4	5			ns	$\overline{CS}$ falling edge to $\overline{SCLK}$ rising edge setup time.
t_5	10			ns	SCLK cycle time (write).
t_5	20			ns	SCLK cycle time (read).
t_6	2.5			ns	SCLK high time.
t_7	2.5			ns	SCLK low time.
t_8	3			ns	SDI data setup time.
t_9	2			ns	SDI data hold time.
t_{10}	5			ns	SCLK rising edge to $\overline{CS}$ hold time.
t_{11}	5			ns	Minimum $\overline{CS}$ high time for latching in data (for multiple SPI transactions).
t_{12}	5			ns	$\overline{CS}$ rising edge to next SCLK rising edge ignore.
t_{13}		4		ns	SCLK falling edge to SDO valid (load capacitance (C_L) = 10pF).
t_{14}		5		ns	SDO rise and fall time (C_L = 10pF).
t_{15}		4		ns	$\overline{CS}$ rising edge to SDO tristate (C_L = 10pF).
t_{16}	10			ns	Time from final initialization SPI instruction to entering the operational time ($t_{OPERATIONAL}$). Set CEN to logic high at this time.
t_{17}	5			ns	$\overline{CS}$ rising edge to LOAD pin first rising edge time for loading filter contents.
t_{18}	10			ns	LOAD pin high time for loading the filter and DSA contents.
t_{19}	10			ns	LOAD pin low time for preparing to load the DSA offsets.
t_{20}	10			ns	LOAD pin high time for loading the DSA offsets.
t_{21}	0			ns	$\overline{CS}$ falling edge to LOAD pin falling edge time. Both can be set low at the same time after a load operation has been completed (after t_{18} or t_{20}) and another SPI instruction is desired.
t_{22}	10			ns	Time from the last SPI instruction when the chip is operational ($t_{CONTINUE}$) to the disable time ($t_{DISABLE}$). After t_{22} has transpired, set CEN to logic low to disable the chip.
t_{23}	3			µs	CEN falling edge to $\overline{RST}$ falling edge. Waiting t_{23} ensures that the RF portions of the chip have been allowed to power down prior to chip reset.
t_{24}	10			ns	$\overline{RST}$ low time to perform reset.
t_{25}	3			µs	CEN falling edge to the power-down time ($t_{POWER-DOWN}$). Waiting t_{25} ensures that the RF portions of the chip have been allowed to power down prior to shutting down the chip power.
t_{26}			10	µs	Logic inputs fall time. The logic inputs and power supplies can be turned off at the same time.
t_{27}	1		100	ms	Power supplies 90% to 10% fall time.

ABSOLUTE MAXIMUM RATINGS

Table 9. Absolute Maximum Ratings

Parameter	Rating
Supply Voltage	
3V Supply	3.3V
1.8V Supply	2V
Digital Input and Output Voltages	
1.8V Supply	2V
LO Input Power	2dBm
RF Input Power[1]	
IF_HYB, IF_I, and IF_Q Pins	7dBm
BB_IP, BB_IN, BB_QP, and BB_QN Pins	5dBm
Continuous RF Input Power	
For 10 Year Reliability	
IF Hybrid Mode and Complex IF Mode	
DSA1 ≤ 10	−10dBm + DSA1 Value
DSA1 > 10	0dBm
I/Q Baseband Mode	
DSA1 ≤ 10	−17dBm + DSA1 Value
DSA1 > 10	−7dBm
Continuous RF Output Power	
For 10 Year Reliability	
DSA1 ≤ 10 and, DSA2 = 0	5dBm
DSA1 > 10 and DSA2 > 0	5dBm, additional attenuation
Survivability RF Input Power	
2 Hours Over Lifetime	
IF Hybrid Mode and Complex IF Mode	
DSA1 ≤ 10	3dBm + DSA1 Value
DSA1 > 1	13dBm
I/Q Baseband Mode	
DSA1 ≤ 10	−4dBm + DSA1 Value
DSA1 > 10	6dBm
Survivability RF Output Power	
2 Hours Over Lifetime	
DSA1 ≤ 10 and DSA2 = 0	18dBm
DSA1 > 10 and DSA2 > 0	18dBm, additional attenuation
Temperature	
Maximum Junction (T_J)	125°C
Maximum Storage Range	−65°C to +150°C
Operating T_C Range	−40°C to +95°C
Maximum Power Dissipation	1.3W
Moisture Sensitivity Level (MSL) Rating[2]	MSL3

[1] The RF input power rating assumes a peak to average ratio of 10dB.

[2] Based on IPC/JEDEC J-STD-20 MSL classifications.

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

THERMAL RESISTANCE

Thermal performance is directly linked to the PCB design and operating environment. Careful attention to PCB thermal design is required.

θ_{JC_TOP} is thermal resistance, junction to case (°C/W).

Only use θ_{JC_TOP} to compare the thermal performance of different packages when all test conditions listed are similar to JEDEC specifications. Otherwise, use Ψ_{JT} and Ψ_{JB} to calculate the device junction temperature using the following equations:

$$T_J = (P \times \Psi_{JT}) + T_{TOP}$$

where:
P is the total power dissipation in the chip (W).
Ψ_{JT} is the junction to top thermal characterization number.
T_{TOP} is the package top temperature (°C), and it is measured at the top center of the package.

$$T_J = (P \times \Psi_{JB}) + T_{BOARD}$$

where:
P is the total power dissipation in the chip (W).
Ψ_{JB} is the junction to board thermal characterization number.
T_{BOARD} is the board temperature measured on the midpoint of the longest side of the package, no more than 1mm from the edge of the package body (°C).

As stated in JEDEC51-12, only use the previous equations when no heatsink or a heat spreader is present. When a heatsink or heat spreader is added, use θ_{JC_TOP} to estimate or calculate the junction temperature.

Table 10 details the temperature rise from case to junction (T_{RISE_JC}) based on a power map that was based on a JEDEC (JESD51-2) board, as opposed to a JEDEC standard of uniform power dissipation across the ADMV1355 package. T_{RISE_JC} applies to all conditions of operation and results in a higher calculated junction temperature. However, T_{RISE_JC} results in a more accurate calculation of the junction temperature on a JEDEC board with the ADMV1355.

To calculate $T_{C, MAX}$, use the following equations and see Figure 2:

$$T_{C, MAX} = T_{J, MAX} - T_{RISE_JC} - P \times \theta_{JC_BOT} \quad (1)$$

If the bottom side is applied to the PCB bottom surface, use the following equation:

$$T_{BOARD} = T_{BASE_PLATE} + P \times \theta_{BOARD} + P \times \theta_{TIM} \quad (2)$$

where:
$T_{C, MAX}$ is the maximum board temperature measured on the mid-point of the longest side of the package no more than 1 mm from the edge of the package body (°C).
$T_{J, MAX}$ is the maximum junction temperature (°C) in Table 9.
T_{RISE_JC} is the highest temperature rise (°C) from case to junction in Table 10.
P is the total power dissipation in the chip (W).

ABSOLUTE MAXIMUM RATINGS

θ_{JC_BOT} is the junction to bottom case thermal resistance (°C/W) in Table 11.
T_{BOARD} is the board temperature measured on the midpoint of the longest side of the package no more than 1 mm from the edge of the package body (°C).
T_{BASE_PLATE} is the temperature of the base plate of the heatsink.
θ_{BOARD} is the thermal resistance (°C/W) of the board.
θ_{TIM} is the thermal resistance (°C/W) of the TIM.

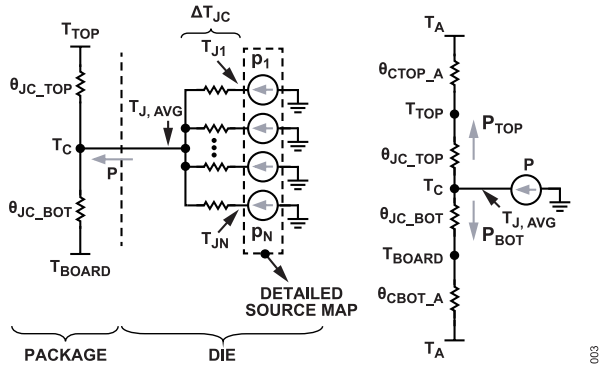


Figure 2. Circuit Level Description of Power Map (Left) and Uniform Power Dissipation Methods (Right)

Table 10. Temperature Rise Based on a Power Map

Package Type[1]	T_{RISE_JC}	Unit
BC-120-4	25	°C

[1] See JEDEC Standard JESD51-2 for additional information on optimizing the thermal impedance.

The thermal resistance of the ADMV1355 assuming the JEDEC standard of uniform power dissipation based on a JEDEC (JESD51-2) board is shown in Table 11. Thermal resistance based on a uniform power dissipation is useful when comparing the performance of the ADMV1355 to other similar ICs.

Table 11. Thermal Resistance Based on Uniform Power Dissipation

Package Type	θ_{JC_BOT}[1]	θ_{JC_TOP}[1]	Ψ_{JT}	Ψ_{JB}	θ_{JA}	Unit
BC-120-4	2.5	3.2	0.1	8.2	28.1	°C/W

[1] See JEDEC Standard JESD51-2 for additional information on optimizing the thermal impedance.

ELECTROSTATIC DISCHARGE (ESD) RATINGS

The following ESD information is provided for handling of ESD-sensitive devices in an ESD protected area only.

Human body model (HBM) per ANSI/ESDA/JEDEC JS-001.

Field induced charged device model (FICDM) per ANSI/ESDA/JEDEC JS-002.

ESD Ratings for ADMV1355

Table 12. ADMV1355, 120-Ball CSP_BGA

ESD Model	Withstand Threshold (V)	Class
HBM	1000	1C
FICDM	250	C1

ESD CAUTION



ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

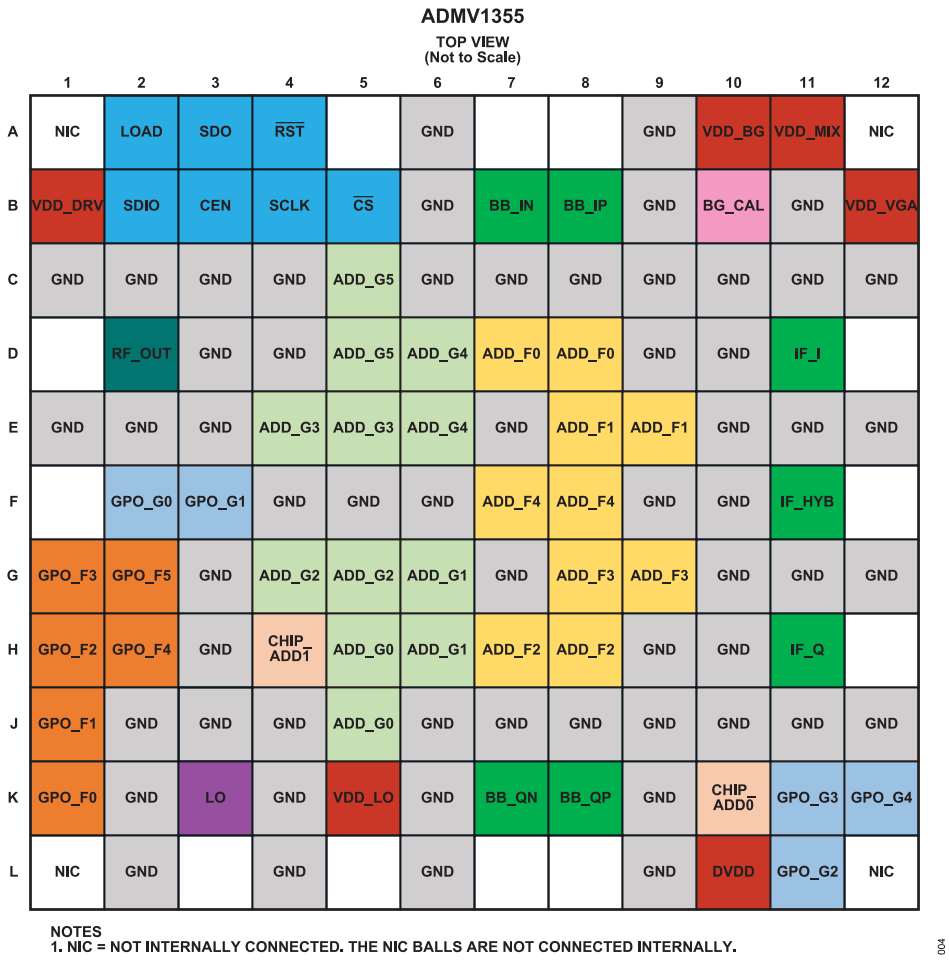


Figure 3. Pin Configuration

Table 13. Pin Function Descriptions

Pin No.	Mnemonic	Description
A1, A12, L1, L12	NIC	Not Internally Connected. The NIC balls are not connected internally.
A2	LOAD	Load Synchronous Toggle. Active high, 1.8V logic. When the LOAD feature is enabled, transitioning the LOAD ball from a logic low to logic high causes content in the filter and gain registers to be sent to the working registers. Return the LOAD ball to logic low when the loading operation completes, see Figure 181 for more information. No internal pull-up or pull-down resistance. Tie LOAD to the logic output from a microcontroller or field-programmable gate array (FPGA); do not float. If LOAD feature is not used, ground this ball.
A3	SDO	SPI Data Output. Active high, 1.8V logic. For 4-wire SPI implementations, SPI data is read using the SDO ball. If SDO is not used, float this ball.
A4	$\overline{\text{RST}}$	Chip Reset. Active low, 1.8V logic.
A6, A9, B6, B9, B11, C1 to C4, C6 to C12, D3, D4, D9, D10, E1 to E3, E7, E10 to E12, F4 to F6, F9, F10, G3, G7, G10 to G12, H3, H9, H10, J2 to J4, J6 to J12, K2, K4, K6, K9, L2, L4, L6, L9	GND	Ground. Tie all ground balls together to a low impedance plane on the PCB.
A10	VDD_BG	Band-Gap Reference Supply Voltage, 1.8V. Place 0.01µF and 1µF decoupling capacitors close to VDD_BG.
A11	VDD_MIX	Mixer Supply Voltage, 1.8V. Place 0.01µF and 1µF decoupling capacitors close to VDD_MIX.
B1	VDD_DRV	RF Output Driver Supply, 3V. Place 0.01µF and 1µF decoupling capacitors close to VDD_DRV.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

Table 13. Pin Function Descriptions (Continued)

Pin No.	Mnemonic	Description
B2	SDIO	SPI Data Input and Output. Active high, 1.8V logic. For 3-wire SPI implementation, SDIO is bidirectional. For 4-wire SPI implementation, SDIO is only used for data input.
B3	CEN	Chip Enable. Active high, 1.8V logic. No internal pull-up or pull-down resistance. Tie CEN to the logic output from a microcontroller, FPGA, or power sequencer; do not float. The CEN pin must be held low until all supply voltages have been turned on and $\overline{RST}$ has been set high.
B4	SCLK	SPI Clock Input. Active high, 1.8V logic. During SPI write transactions, data is sampled on the rising edge of SCLK. During SPI read transactions, output data changes at the falling edge of SCLK.
B5	$\overline{CS}$	SPI Chip Select. Active low, 1.8V logic. Bring $\overline{CS}$ low to begin the SPI transaction, see Figure 180 and Figure 181 for more information.
B7, B8	BB_IN, BB_IP	Differential Baseband I Inputs. The inputs are internally DC-coupled with a 100Ω differential output impedance. The common-mode input voltage (V_{ICM}) range is from 0V to 1.55V. When operating in IF mode, BB_IN and BB_IP can float.
B10	BG_CAL	Band-Gap Reference Calibration. BG_CAL is used for factory and debug purposes. This ball can be left floating or be tied to a 3.48kΩ, 1%, resistor. Do not ground this ball.
B12	VDD_VGA	RF Signal Chain Supply, 1.8V. Place 0.01µF and 1µF decoupling capacitors close to VDD_VGA.
C5, D5	ADD_G5	Gain LUT Address Bit 5. Active high, 1.8V logic. No internal pull-up or pull-down resistance. Tie ADD_G5 to the logic output from a microcontroller or FPGA; do not float. If ADD_G5 is not used to set the LUT address pointer, ground this ball.
D2	RF_OUT	RF Output. This ball is DC-coupled and matched to 50Ω. Do not apply an external voltage to RF_OUT. If required, place a DC-blocking capacitor in-series with RF_OUT and ensure that any capacitor parasitic attributes are acceptable for the required operating frequency range.
D6, E6	ADD_G4	Gain LUT Address Bit 4. Active high, 1.8V logic. No internal pull-up or pull-down resistance. Tie ADD_G4 to the logic output from a microcontroller or FPGA; do not float. If ADD_G4 is not used to set the LUT address pointer, ground this ball.
D7, D8	ADD_F0	Frequency LUT Address Bit 0. Active high, 1.8V logic. No internal pull-up or pull-down resistance. Tie ADD_F0 to the logic output from a microcontroller or FPGA; do not float. If ADD_F0 is not used to set the LUT address pointer, ground this ball.
D11, H11	IF_I, IF_Q	Complex IF Inputs. Each input is DC-coupled and matched to 50Ω. Do not apply an external voltage to IF_I or IF_Q. If required, place a DC-blocking capacitor in series and ensure that any capacitor parasitic attributes are acceptable for the required operating frequency range.
E4, E5	ADD_G3	Gain LUT Address Bit 3. Active high, 1.8V logic. No internal pull-up or pull-down resistance. Tie ADD_G3 to the logic output from a microcontroller or FPGA; do not float. If ADD_G3 is not used to set the LUT address pointer, ground this ball.
E8, E9	ADD_F1	Frequency LUT Address Bit 1. Active high, 1.8V logic. No internal pull-up or pull-down resistance. Tie ADD_F1 to the logic output from a microcontroller or FPGA; do not float. If ADD_F1 is not used to set the LUT address pointer, ground this ball.
F2	GPO_G0	General-Purpose Digital Output Pin Gain 0. Active high, 1.8V logic. This ball can be left floating. Do not ground this ball.
F3	GPO_G1	General-Purpose Digital Output Pin Gain 1. Active high, 1.8V logic. This ball can be left floating. Do not ground this ball.
F7, F8	ADD_F4	Frequency LUT Address Bit 4. Active high, 1.8V logic. No internal pull-up or pull-down resistance. Tie ADD_F4 to the logic output from a microcontroller or FPGA; do not float. If ADD_F4 is not used to set the LUT address pointer, ground this ball.
F11	IF_HYB	IF Hybrid Input. This ball is DC-coupled and matched to 50Ω. Do not apply an external voltage to IF_HYB. If required, place a DC-blocking capacitor in series with IF_HYB and ensure that any capacitor parasitic attributes are acceptable for the required operating frequency range.
G1	GPO_F3	General-Purpose Digital Output Pin Filter 3. Active high, 1.8V logic. This ball can be left floating. Do not ground this ball.
G2	GPO_F5	General-Purpose Digital Output Pin Filter 5. Active high, 1.8V logic. This ball can be left floating. Do not ground this ball.
G4, G5	ADD_G2	Gain LUT Address Bit 2. Active high, 1.8V logic. No internal pull-up or pull-down resistance. Tie ADD_G2 to the logic output from a microcontroller or FPGA; do not float. If ADD_G2 is not used to set the LUT address pointer, ground this ball.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

Table 13. Pin Function Descriptions (Continued)

Pin No.	Mnemonic	Description
G6, H6	ADD_G1	Gain LUT Address Bit 1. Active high, 1.8V logic. No internal pull-up or pull-down resistance. Tie ADD_G1 to the logic output from a microcontroller or FPGA; do not float. If ADD_G1 is not used to set the LUT address pointer, ground this ball.
G8, G9	ADD_F3	Frequency LUT Address Bit 3. Active high, 1.8V logic. No internal pull-up or pull-down resistance. Tie ADD_F3 to the logic output from a microcontroller or FPGA; do not float. If ADD_F3 is not used to set the LUT address pointer, ground this ball.
H1	GPO_F2	General-Purpose Digital Output Pin Filter 2. Active high, 1.8V logic. This ball can be left floating. Do not ground this ball.
H2	GPO_F4	General-Purpose Digital Output Pin Filter 4. Active high, 1.8V logic. This ball can be left floating. Do not ground this ball.
H4	CHIP_ADD1	Chip Address Bit 1. Active high, 1.8V logic. CHIP_ADD1 is internally pulled high through 15kΩ. This ball can be dynamically set by logic output from a microcontroller or FPGA. For fixed addressing implementations, set this ball high by leaving it floating and set this ball low by grounding it. For single-chip implementations, always ground this ball.
H5, J5	ADD_G0	Gain LUT Address Bit 0. Active high, 1.8V logic. No internal pull-up or pull-down resistance. Tie ADD_G0 to the logic output from a microcontroller or FPGA; do not float. If ADD_G0 is not used to set the LUT address pointer, ground this ball.
H7, H8	ADD_F2	Frequency LUT Address Bit 2. Active high, 1.8V logic. No internal pull-up or pull-down resistance. Tie ADD_F2 to the logic output from a microcontroller or FPGA; do not float. If ADD_F2 is not used to set the LUT address pointer, ground this ball.
J1	GPO_F1	General-Purpose Digital Output Pin Filter 1. Active high, 1.8V logic. This ball can be left floating. Do not ground this ball.
K1	GPO_F0	General-Purpose Digital Output Pin Filter 0. Active high, 1.8V logic. This ball can be left floating. Do not ground this ball.
K3	LO	LO Input. This ball is DC-coupled and matched to 50Ω. Do not apply an external voltage to LO. If required, place a DC-blocking capacitor in series with LO and ensure that any capacitor parasitic attributes are acceptable for the required operating frequency range.
K5	VDD_LO	Local Oscillator Supply, 1.8 V. Place 0.01µF and 1µF decoupling capacitors close to VDD_LO.
K7, K8	BB_QN, BB_QP	Differential Baseband Q Inputs. The inputs are internally DC-coupled with a 100Ω differential output impedance. The V_{ICM} range is from 0V to 1.55V. When operating in IF mode, BB_QN and BB_QP can float.
K10	CHIP_ADD0	Chip Address Bit 0. Active high, 1.8V logic. CHIP_ADD0 is internally pulled high through 15kΩ. This ball can be dynamically set by the logic output from a microcontroller or FPGA. For fixed addressing implementations, set this ball high by leaving it floating and set this ball low by grounding it. For single-chip implementations, always ground this ball.
K11	GPO_G3	General-Purpose Digital Output Pin Gain 3. Active high, 1.8V logic. This ball can be left floating. Do not ground this ball.
K12	GPO_G4	General-Purpose Digital Output Pin Gain 4. Active high, 1.8V logic. This ball can be left floating. Do not ground this ball.
L10	DVDD	Digital Supply Voltage, 1.8V. Place 0.01µF and 1µF decoupling capacitors close to DVDD.
L11	GPO_G2	General-Purpose Digital Output Pin Gain 2. Active high, 1.8V logic. This ball can be left floating. Do not ground this ball.

TYPICAL PERFORMANCE CHARACTERISTICS

IF HYBRID MODE, IF_HYB, HIGH BAND

All measurements use IF_HYB as an input with the RF high-band settings. VDD_DRV = 3V, all other supply voltages = 1.8V, and T_C = 25°C, unless otherwise noted.

All measurements taken with P_{IF} = −20dBm, P_{LO} = −5dBm, f_{IF} = 8GHz, upper sideband, maximum gain, RF LPF setting = 0x00 (highest cutoff), RF HPF setting = 0x3F (lowest cutoff), and LO tunable filter wideband high settings (see Table 18), unless otherwise noted. Trace and connector losses are de-embeded to the RF pins (see the IF_HYB input pin and RF_OUT output pin in Figure 3).

Conversion Gain

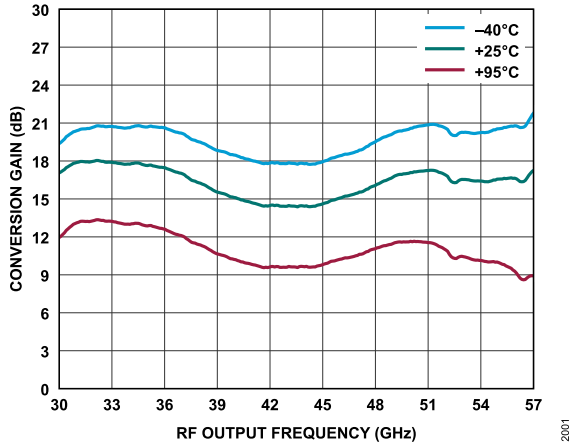


Figure 4. Conversion Gain vs. RF Output Frequency at Various Temperatures

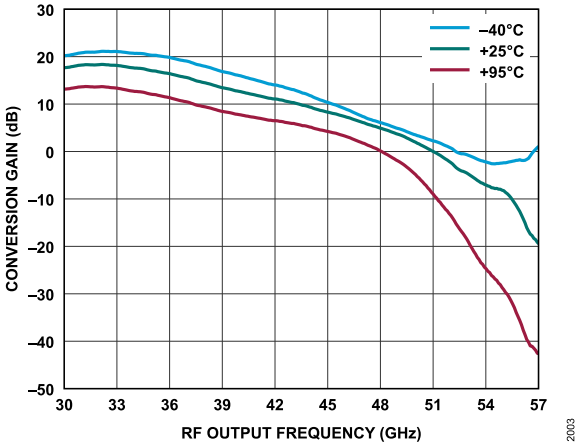


Figure 6. Conversion Gain vs. RF Output Frequency at Various Temperatures, LO Filter Wideband Low Setting

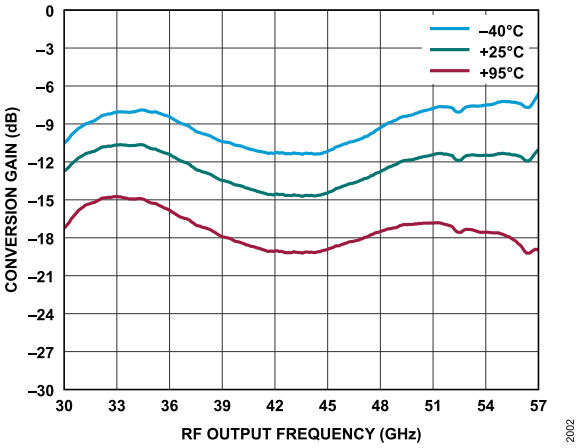


Figure 5. Conversion Gain vs. RF Output Frequency at Various Temperatures, Minimum Gain

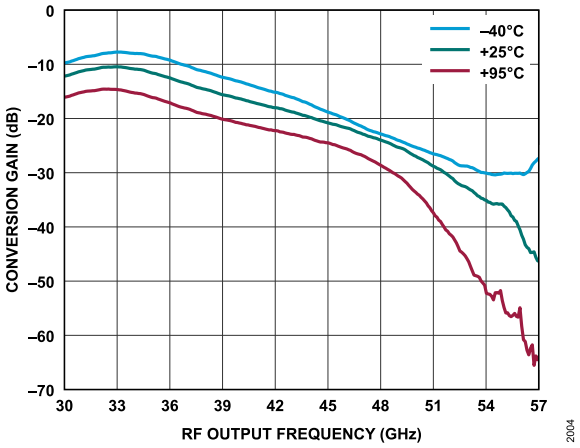


Figure 7. Conversion Gain vs. RF Output Frequency at Various Temperatures, LO Filter Wideband Low Setting, Minimum Gain

TYPICAL PERFORMANCE CHARACTERISTICS

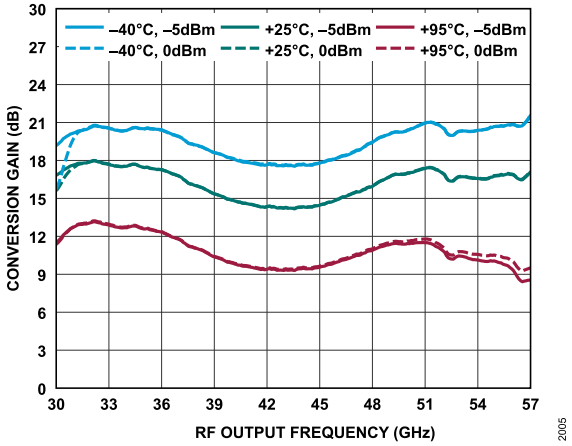


Figure 8. Conversion Gain vs. RF Output Frequency at Various Temperatures and LO Powers

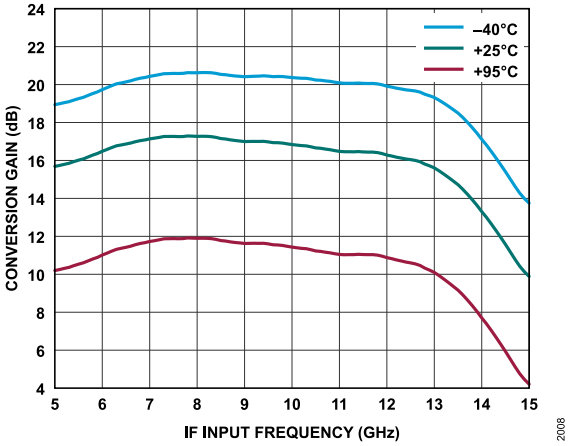


Figure 11. Conversion Gain vs. IF Input Frequency at Various Temperatures

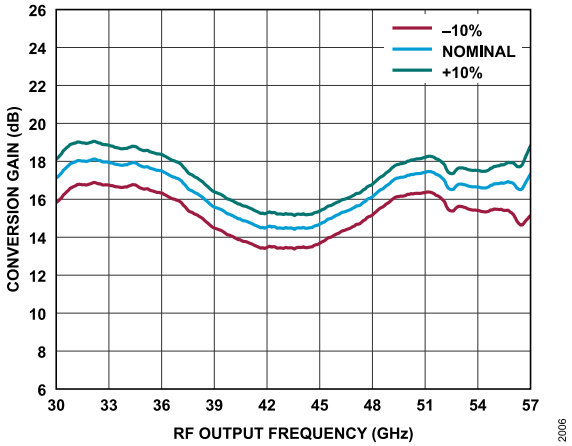


Figure 9. Conversion Gain vs. RF Output Frequency at Various Supply Voltages

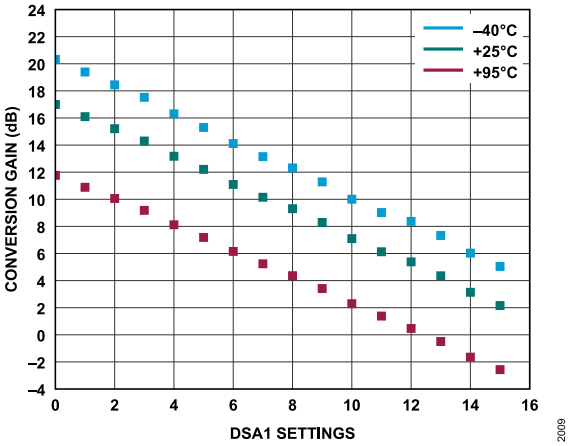


Figure 12. Conversion Gain vs. DSA1 Settings at Various Temperatures, Single f_{RF} = 49GHz

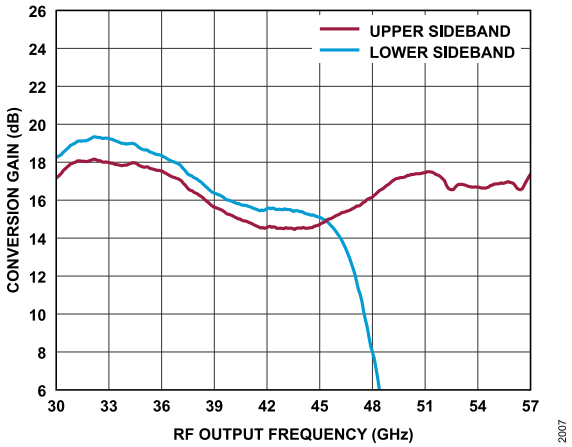


Figure 10. Conversion Gain vs. RF Output Frequency, Upper Sideband and Lower Sideband

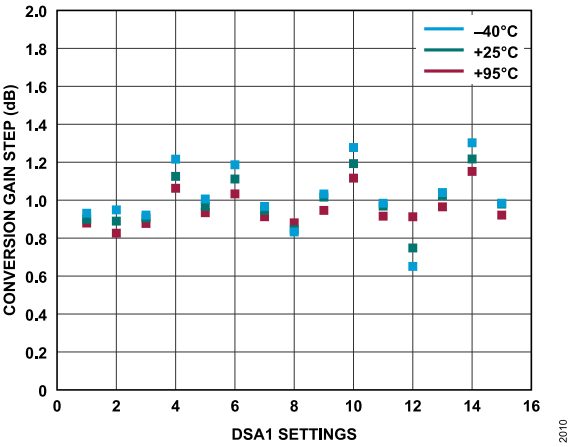


Figure 13. Conversion Gain Step vs. DSA1 Settings at Various Temperatures, Single f_{RF} = 49GHz

TYPICAL PERFORMANCE CHARACTERISTICS

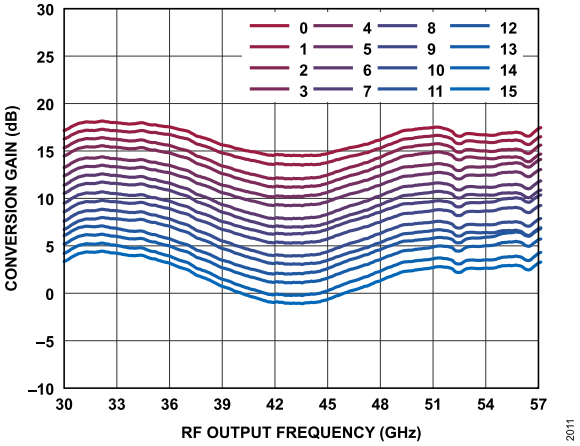


Figure 14. Conversion Gain vs. RF Output Frequency at Various DSA1 Settings

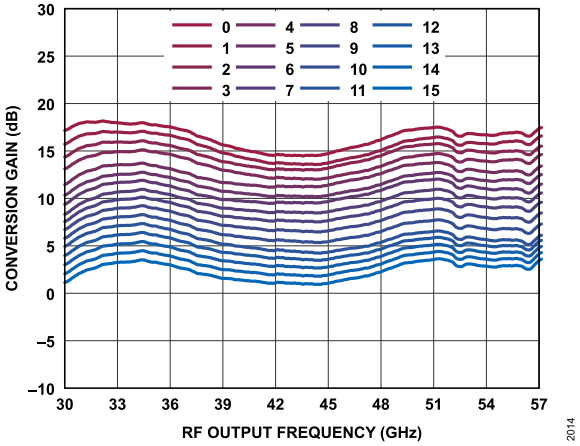


Figure 17. Conversion Gain vs. RF Output Frequency at Various DSA2 Settings

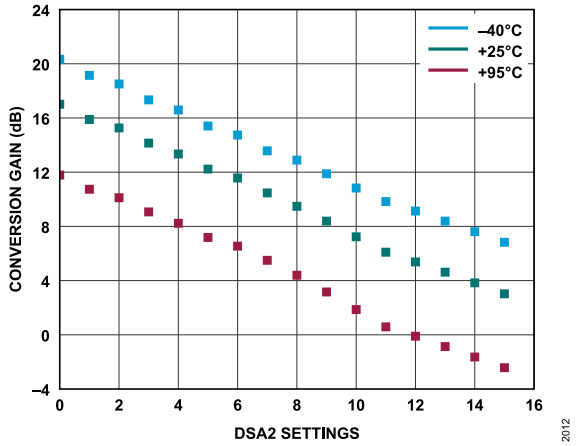


Figure 15. Conversion Gain vs. DSA2 Settings at Various Temperatures, Single f_{RF} = 49GHz

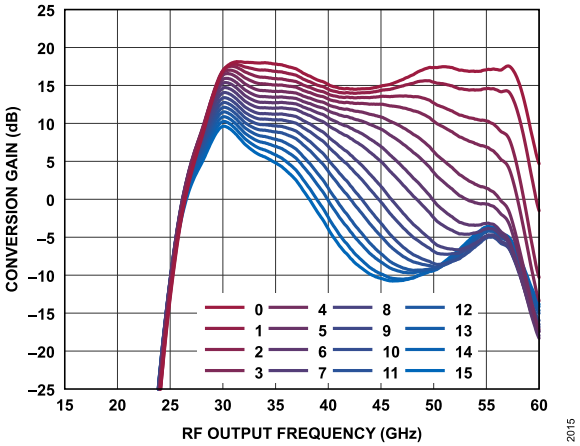


Figure 18. Conversion Gain vs. RF Output Frequency at Various RF Low-Pass Filter Settings

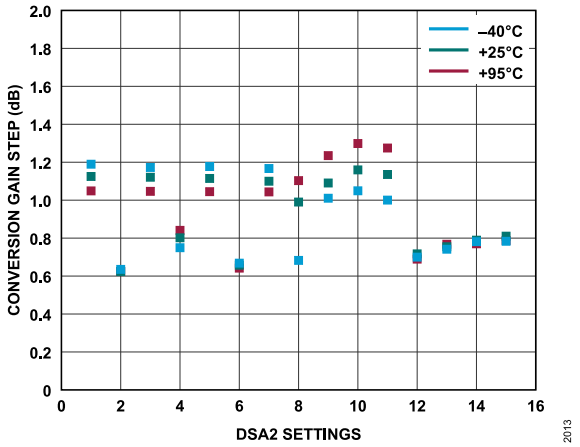


Figure 16. Conversion Gain Step vs. DSA2 Settings at Various Temperatures, Single f_{RF} = 49GHz

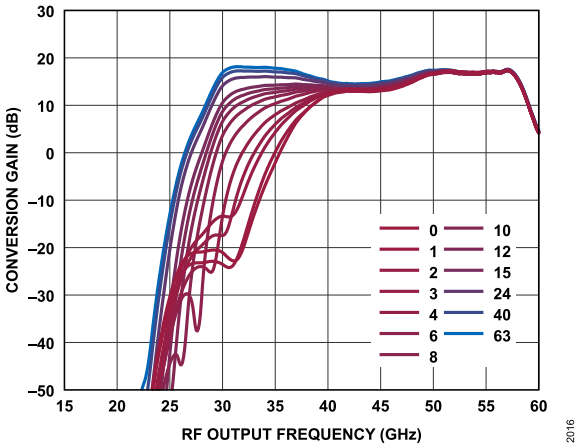


Figure 19. Conversion Gain vs. RF Output Frequency at Various RF High-Pass Filter Settings

TYPICAL PERFORMANCE CHARACTERISTICS

Output IP3

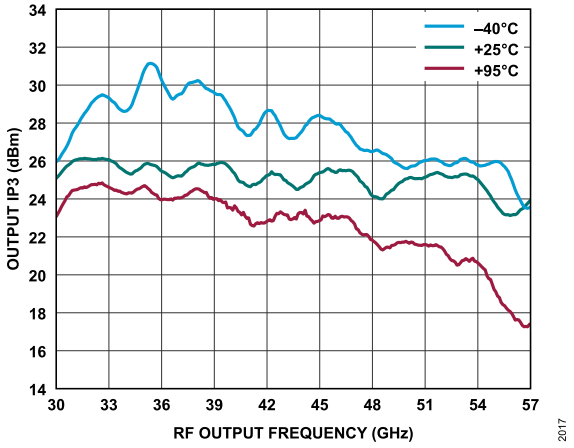


Figure 20. Output IP3 vs. RF Output Frequency at Various Temperatures

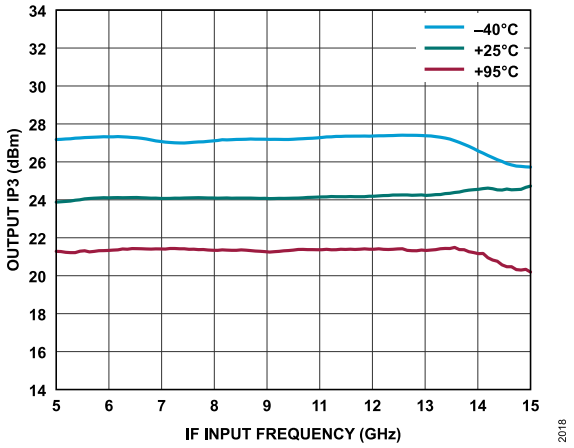


Figure 21. Output IP3 vs. IF Input Frequency at Various Temperatures

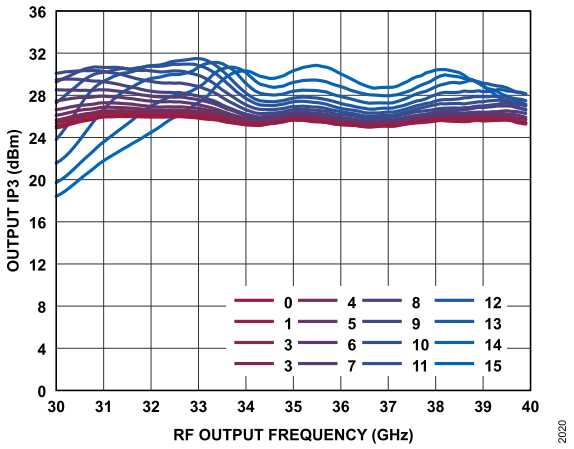


Figure 22. Output IP3 vs. RF Output Frequency, 30GHz to 40GHz at Various DSA1 Settings

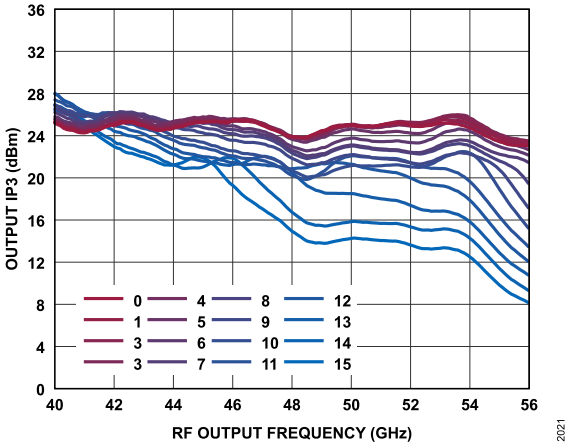


Figure 23. Output IP3 vs. RF Output Frequency, 40GHz to 56GHz at Various DSA1 Settings

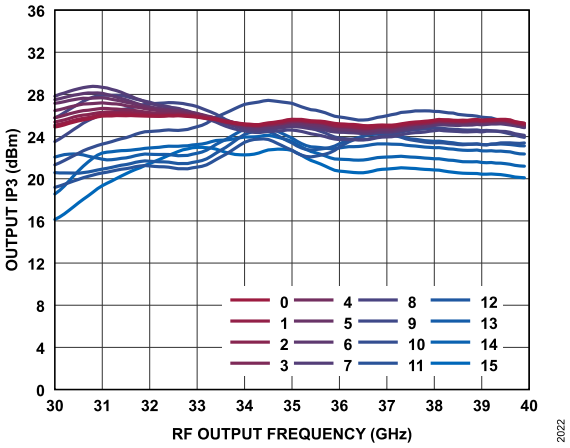


Figure 24. Output IP3 vs. RF Output Frequency, 30GHz to 40GHz at Various DSA2 Settings

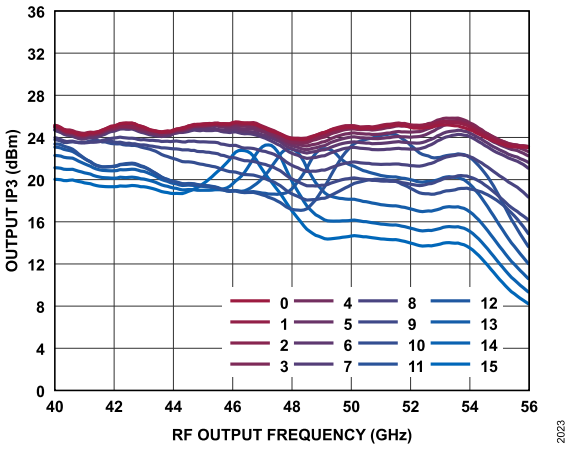


Figure 25. Output IP3 vs. RF Output Frequency, 40GHz to 56GHz at Various DSA2 Settings

TYPICAL PERFORMANCE CHARACTERISTICS

Noise Figure

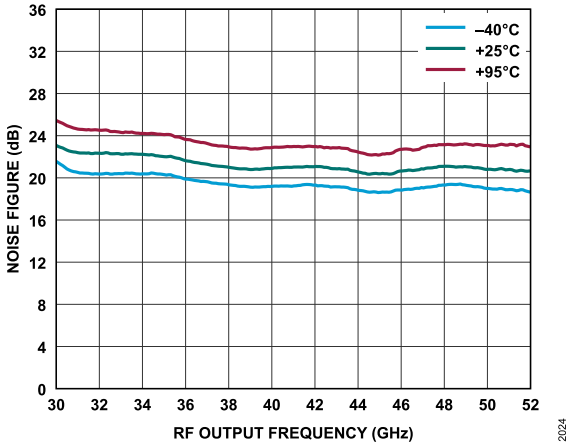


Figure 26. Noise Figure vs. RF Output Frequency at Various Temperatures

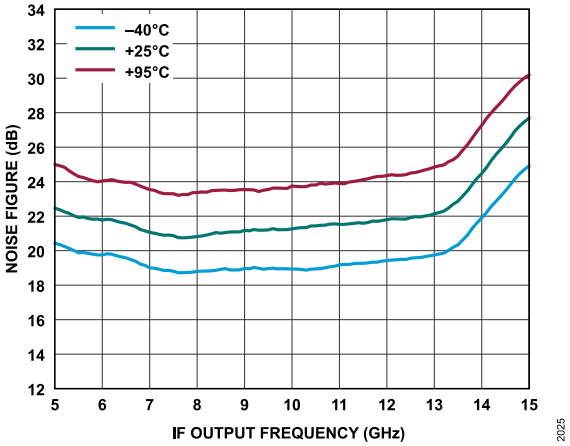


Figure 27. Noise Figure vs. IF Input Frequency at Various Temperatures

TYPICAL PERFORMANCE CHARACTERISTICS

Output P1dB

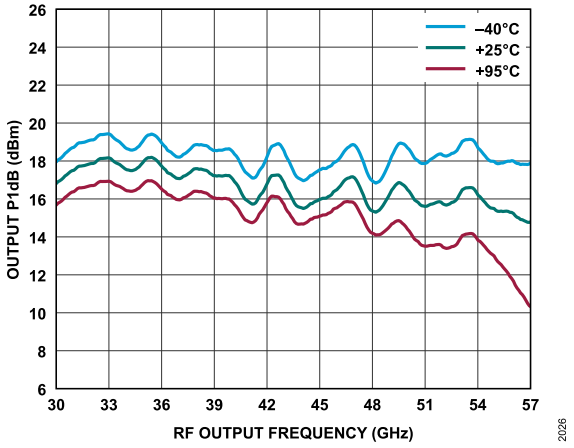


Figure 28. Output P1dB vs. RF Output Frequency at Various Temperatures

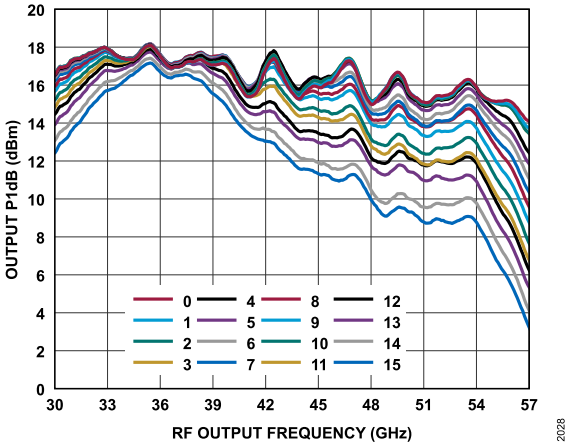


Figure 30. Output P1dB vs. RF Output Frequency at Various DSA1 Settings

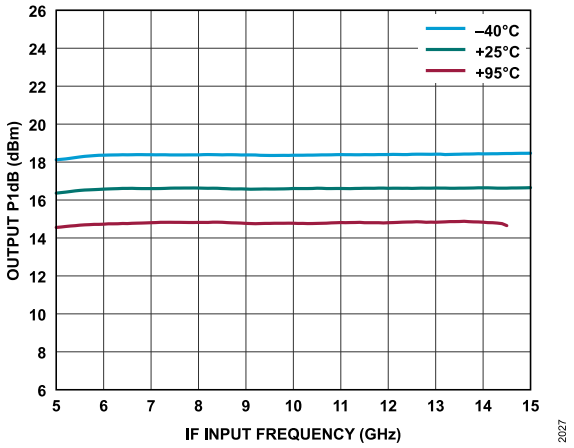


Figure 29. Output P1dB vs. IF Input Frequency at Various Temperatures

TYPICAL PERFORMANCE CHARACTERISTICS

Sideband Rejection

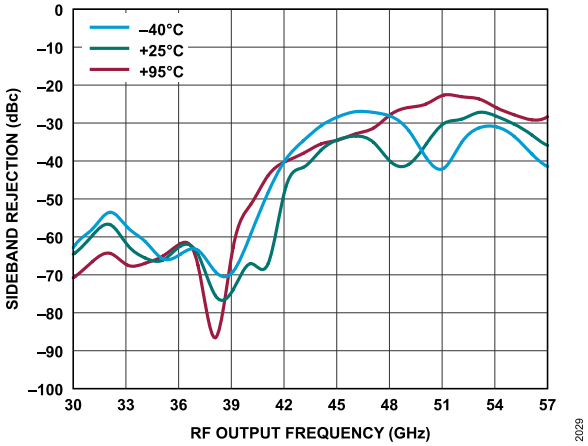


Figure 31. Sideband Rejection vs. RF Output Frequency at Various Temperatures With No Calibration and No RF Filters Applied

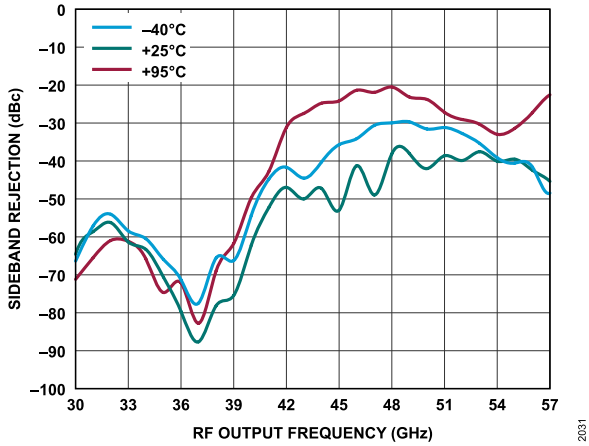


Figure 33. Sideband Rejection vs. RF Output Frequency at Various Temperatures with Optimization at 25°C and No RF Filters Applied

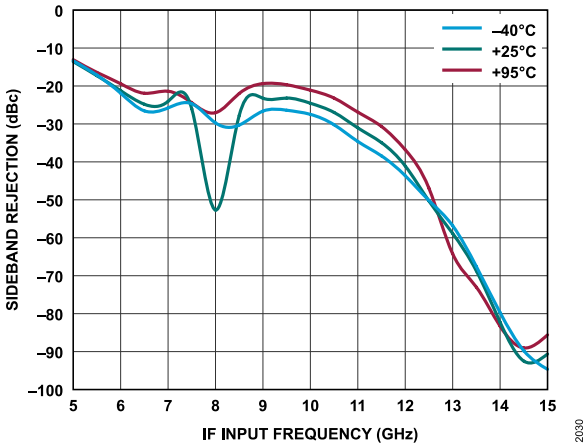


Figure 32. Sideband Rejection vs. IF Input Frequency at Various Temperatures With No Calibration and No RF Filters Applied

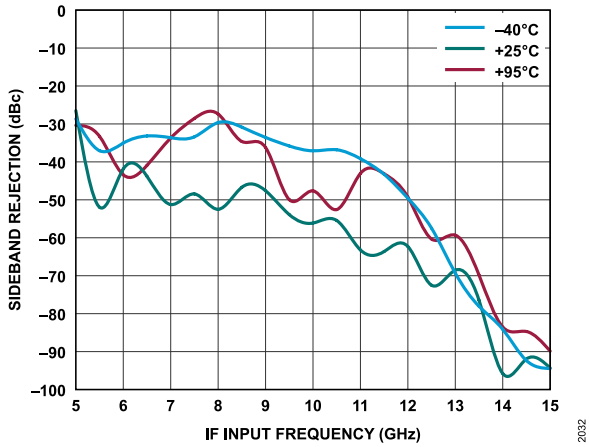


Figure 34. Sideband Rejection vs. IF Input Frequency at Various Temperatures with Optimization at 25°C and No RF Filters Applied

TYPICAL PERFORMANCE CHARACTERISTICS

Spurs

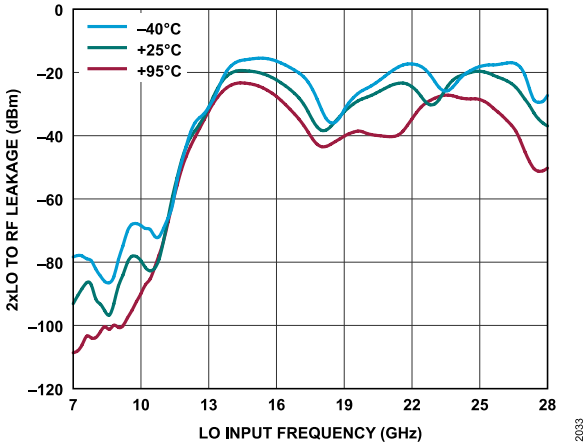


Figure 35. 2× LO to RF Leakage vs. LO Input Frequency at Various Temperatures With No Calibration and No RF Filters Applied

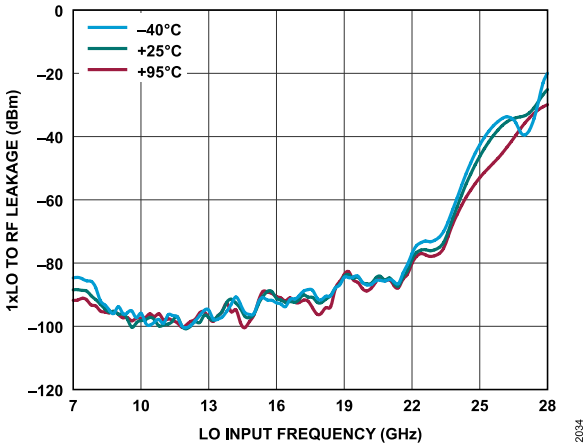


Figure 36. 1× LO to RF Leakage vs. LO Input Frequency at Various Temperatures With No Calibration and No RF Filters Applied

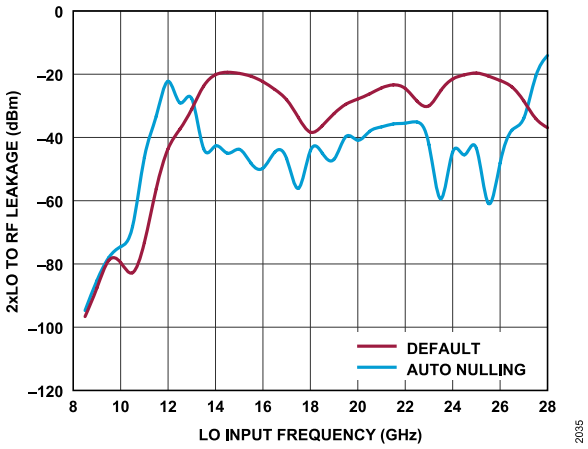


Figure 37. 2× LO to RF Leakage vs. LO Input Frequency at 25°C With and Without Auto LO Nulling Calibration and No RF Filters Applied

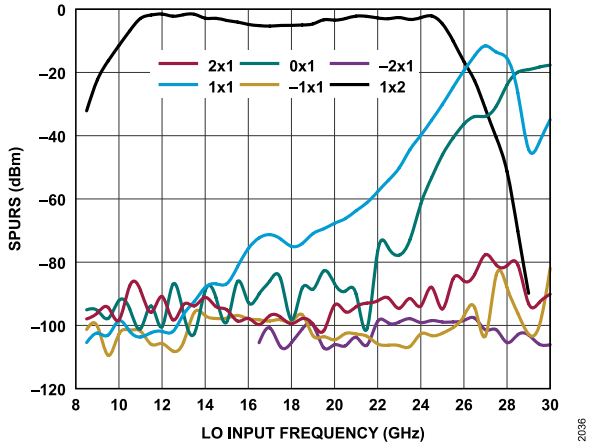


Figure 38. (IF × m) + 1× LO Spurs to RF Leakage vs. LO Input Frequency with No RF Filters Applied

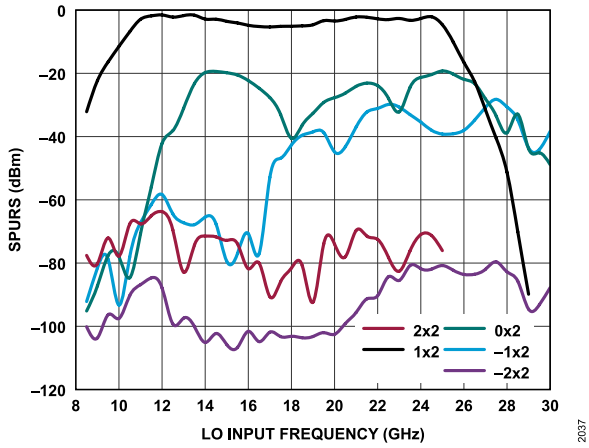


Figure 39. (IF × m) + 2× LO Spurs to RF Leakage vs. LO Input Frequency with No RF Filters Applied

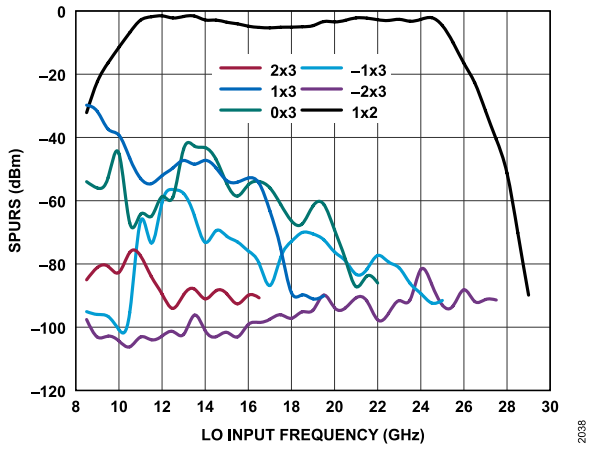


Figure 40. (IF × m) + 3× LO Spurs to RF Leakage vs. LO Input Frequency with No RF Filters Applied

TYPICAL PERFORMANCE CHARACTERISTICS

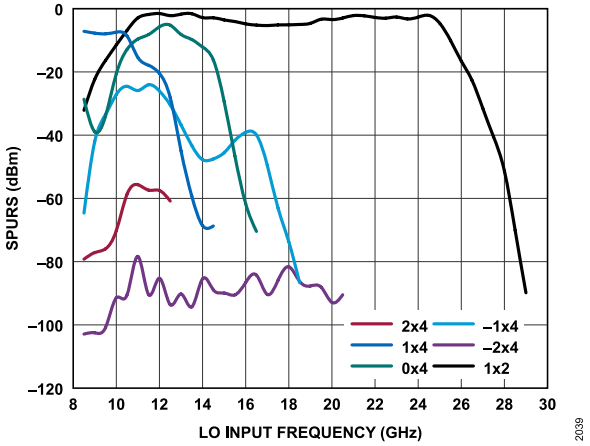


Figure 41. (IF × m) + 4× LO Spurs to RF Leakage vs. LO Input Frequency with No RF Filters Applied

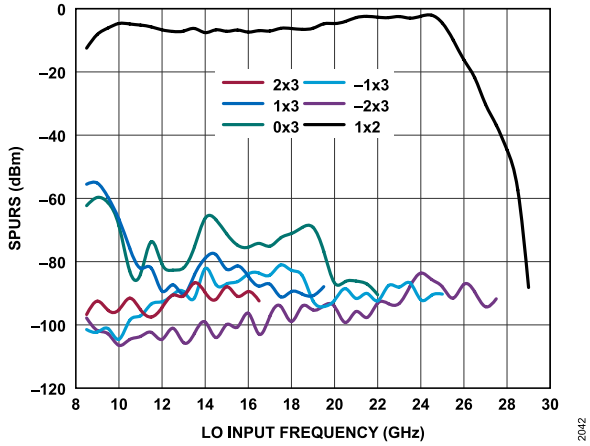


Figure 44. (IF x m) + 3× LO Spurs to RF Leakage vs. LO Input Frequency with LO and RF Filter Settings Adjusted with Sweeping Frequency

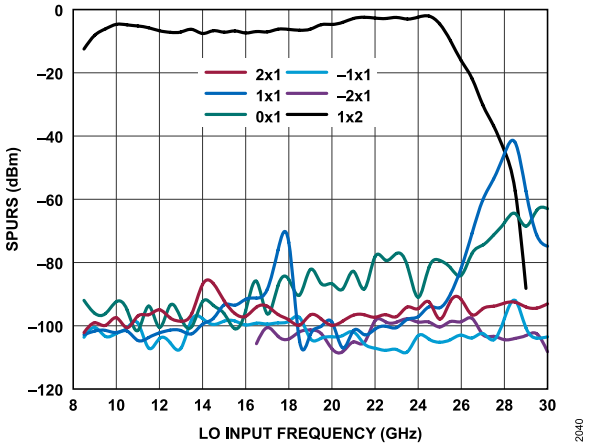


Figure 42. (IF × m) + 1× LO Spurs to RF Leakage vs. LO Input Frequency with LO and RF Filter Settings Adjusted with Sweeping Frequency

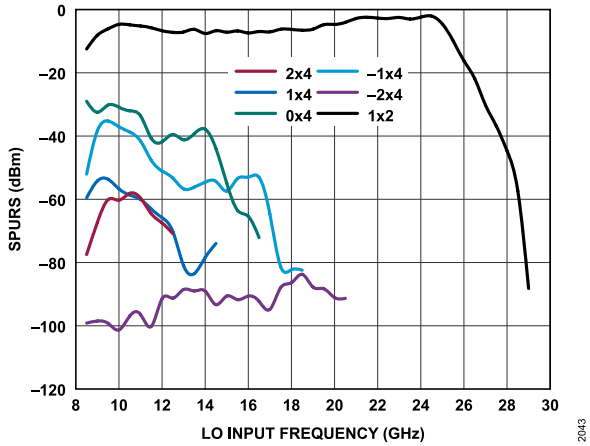


Figure 45. (IF × m) + 4× LO Spurs to RF Leakage vs. LO Input Frequency and LO with RF Filter Settings Adjusted with Sweeping Frequency

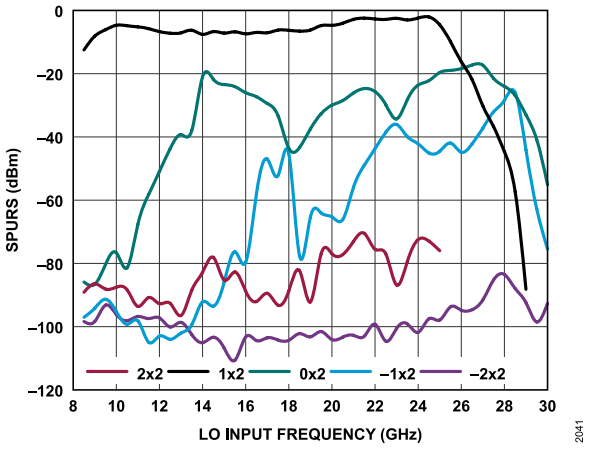


Figure 43. (IF × m) + 2× LO Spurs to RF Leakage vs. LO Input Frequency with LO and RF Filter Settings Adjusted with Sweeping Frequency

TYPICAL PERFORMANCE CHARACTERISTICS

IF HYBRID MODE, IF_HYB, LOW BAND

All measurements use IF_HYB as an input with the RF low-band settings. VDD_DRV = 3V, all other supply voltages = 1.8V, and T_C = 25°C, unless otherwise noted.

All measurements taken with P_{IF} = −20dBm, P_{LO} = −5dBm, f_{IF} = 8GHz, lower sideband, maximum gain, RF LPF setting = 0x00 (highest cutoff), and LO tunable filter wideband high settings, unless otherwise noted. Trace and connector losses are de-embeded to the RF pins (see the IF_HYB input pin and RF_OUT output pin in Figure 3).

Conversion Gain

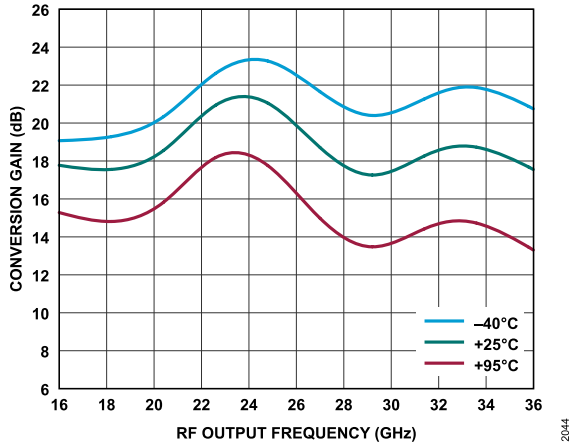


Figure 46. Conversion Gain vs. RF Output Frequency at Various Temperatures

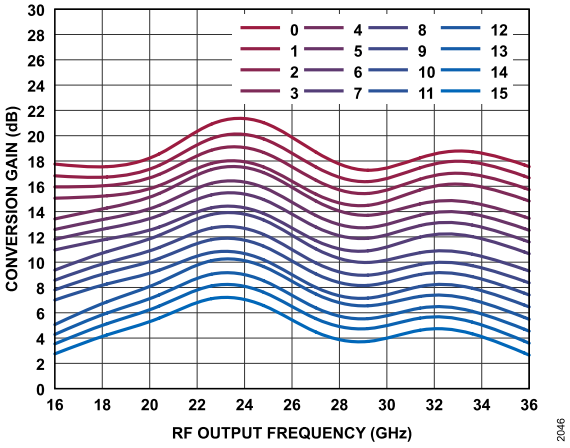


Figure 48. Conversion Gain vs. RF Output Frequency at Various DSA1 Settings

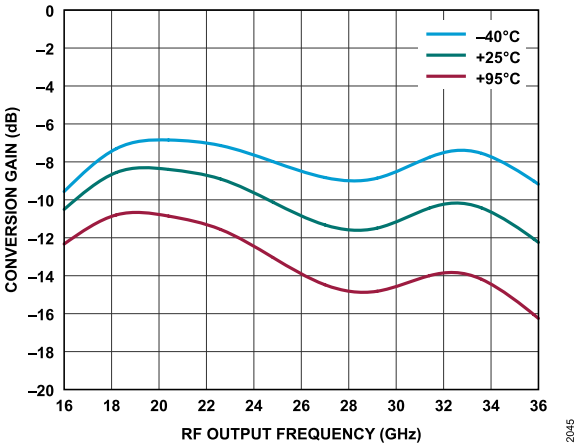


Figure 47. Conversion Gain vs. RF Output Frequency at Various Temperatures, Minimum Gain

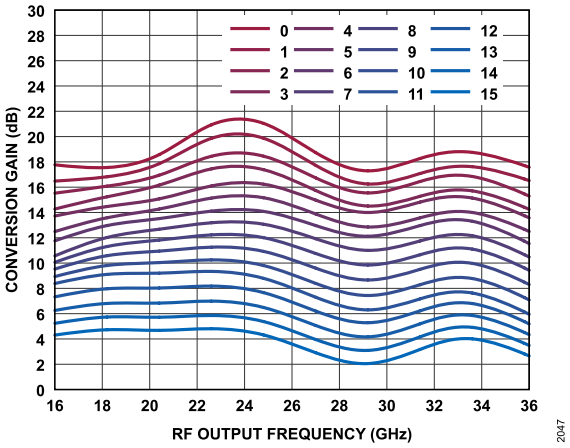


Figure 49. Conversion Gain vs. RF Output Frequency at Various DSA2 Settings

TYPICAL PERFORMANCE CHARACTERISTICS

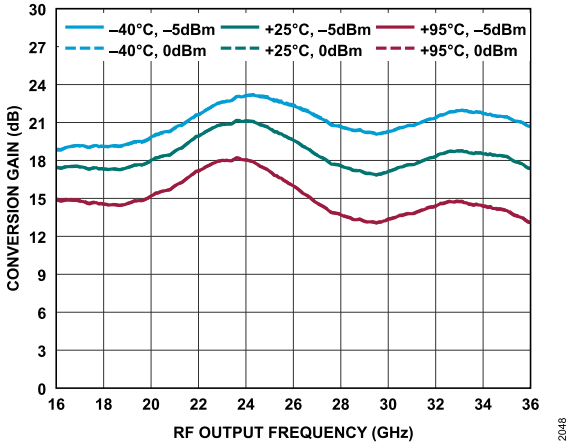


Figure 50. Conversion Gain vs. RF Output Frequency at Temperatures and LO Powers

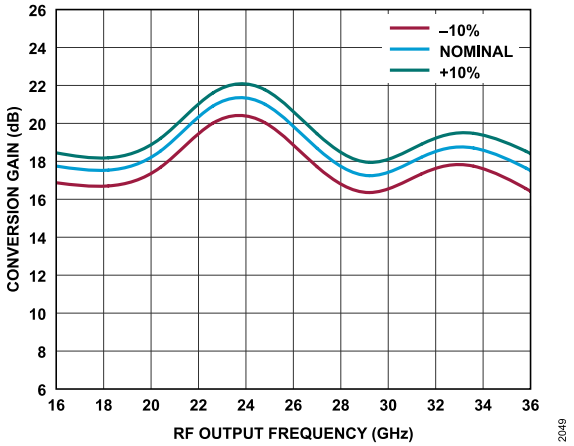


Figure 51. Conversion Gain vs. RF Output Frequency at Various Supply Voltages

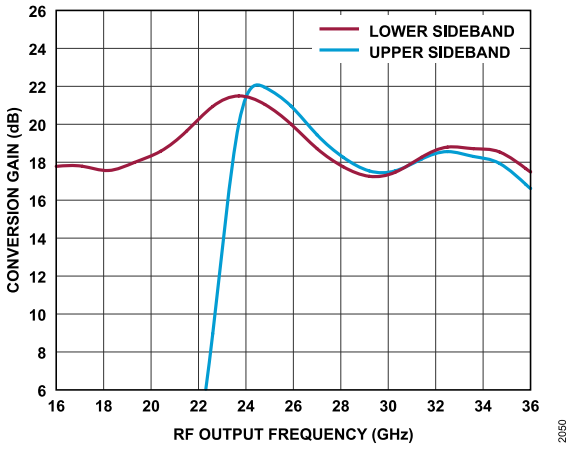


Figure 52. Conversion Gain vs. RF Output Frequency, Upper Sideband and Lower Sideband

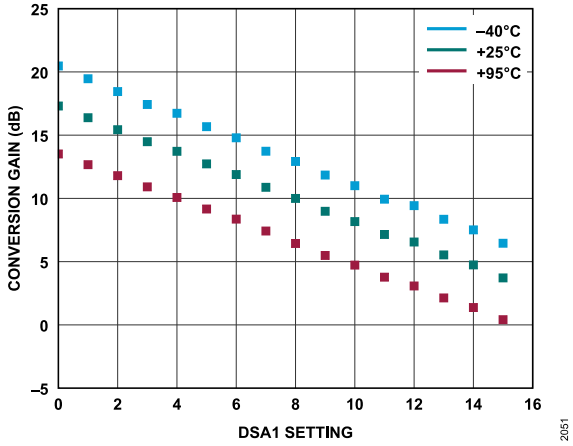


Figure 53. Conversion Gain vs. DSA1 Settings at Various Temperatures, Single f_{RF} = 29GHz

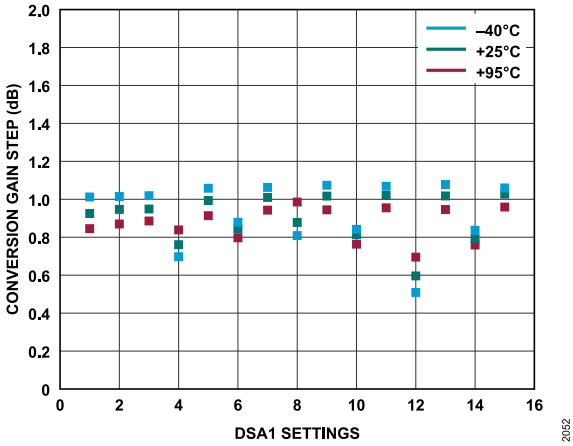


Figure 54. Conversion Gain Step vs. DSA1 Settings at Various Temperatures, Single f_{RF} = 29GHz

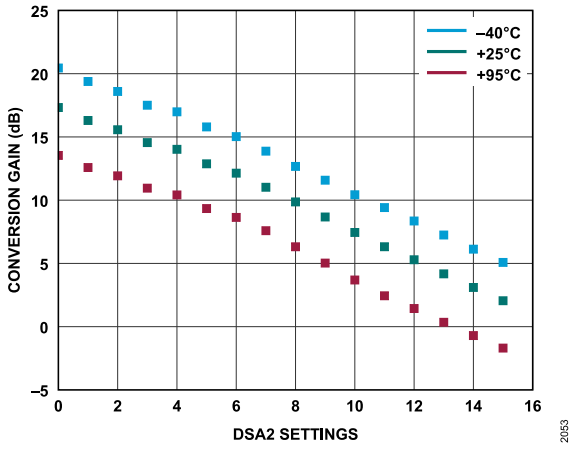


Figure 55. Conversion Gain vs. DSA2 Settings at Various Temperatures, Single f_{RF} = 29GHz

TYPICAL PERFORMANCE CHARACTERISTICS

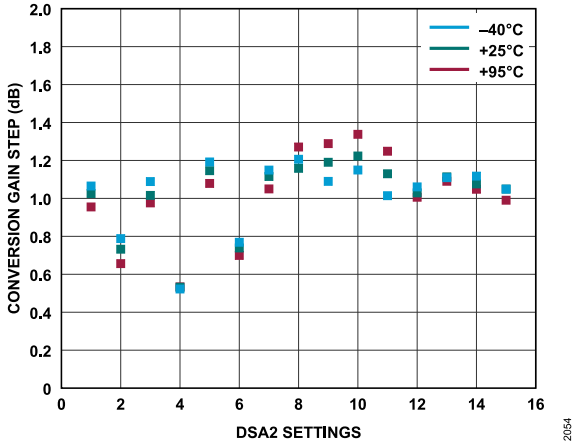


Figure 56. Conversion Gain Step vs. DSA2 Settings at Various Temperatures, Single f_{RF} = 29GHz

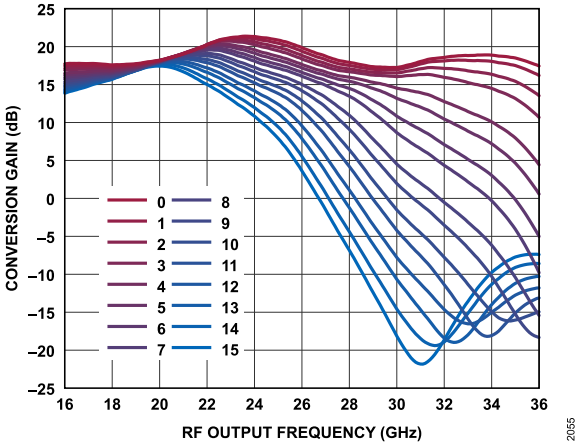


Figure 57. Conversion Gain vs. RF Output Frequency at Various RF LPF Settings

TYPICAL PERFORMANCE CHARACTERISTICS

Output IP3

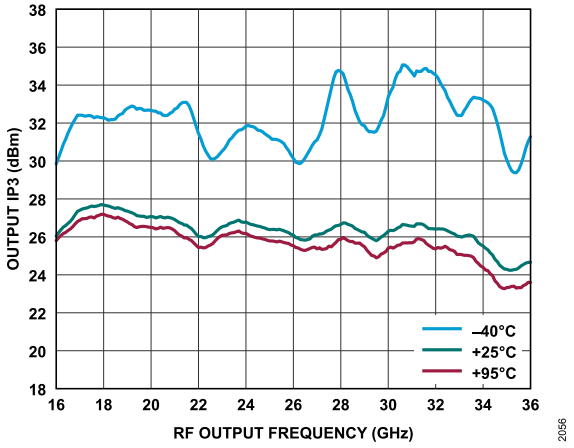


Figure 58. Output IP3 vs. RF Output Frequency at Various Temperatures

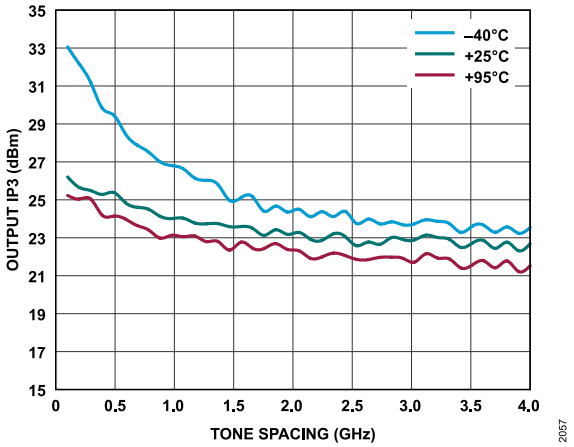


Figure 59. Output IP3 vs. Tone Spacing at Various Temperatures

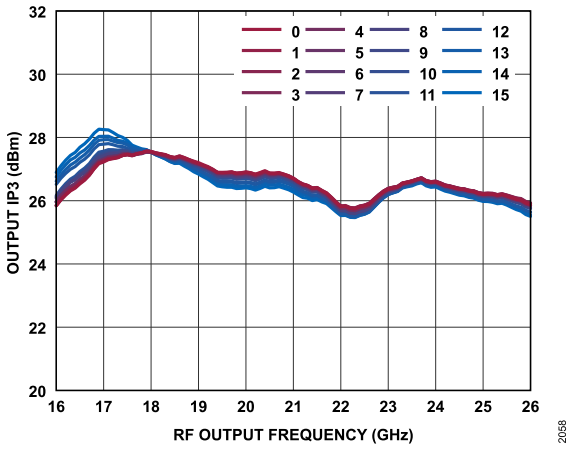


Figure 60. Output IP3 vs. RF Output Frequency from 16GHz to 26GHz at Various DSA1 Settings

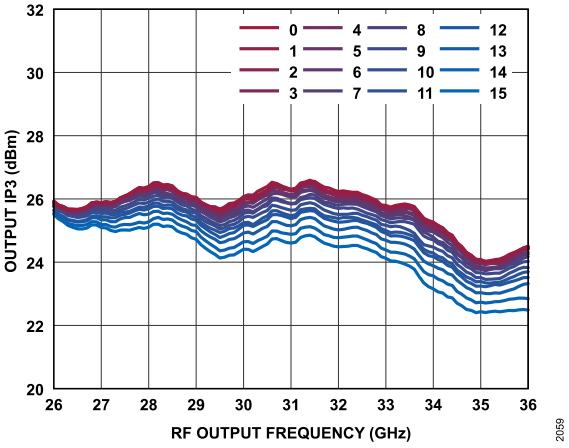


Figure 61. Output IP3 vs. RF Output Frequency from 26GHz to 36GHz at Various DSA1 Settings

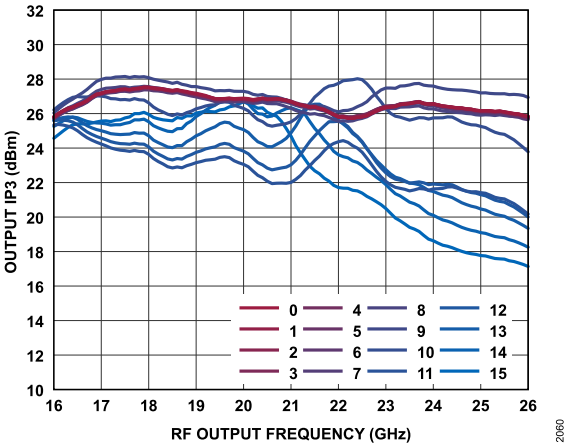


Figure 62. Output IP3 vs. RF Output Frequency from 16GHz to 36GHz at Various DSA2 Settings

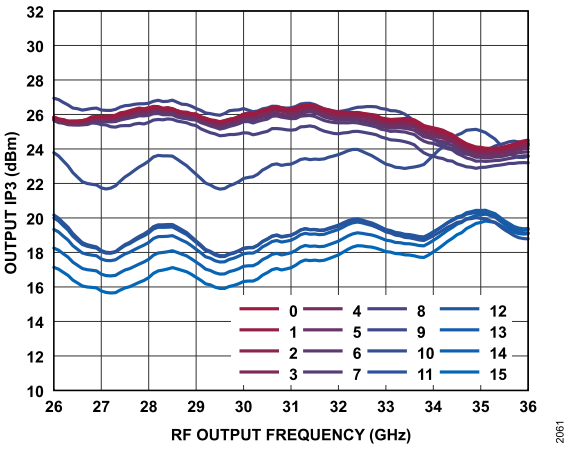


Figure 63. Output IP3 vs. RF Output Frequency from 26GHz to 36GHz at Various DSA2 Settings

TYPICAL PERFORMANCE CHARACTERISTICS

Noise Figure

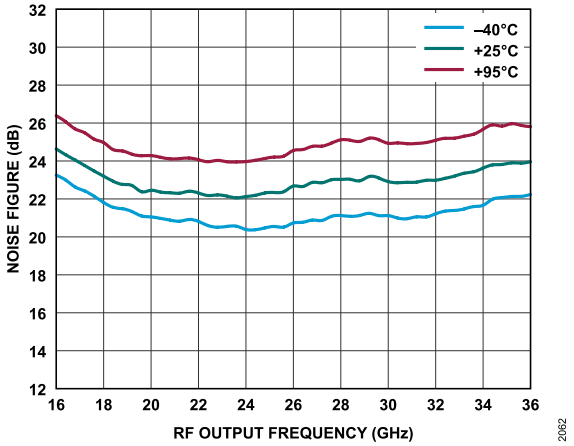


Figure 64. Noise Figure vs. RF Output Frequency at Various Temperatures

TYPICAL PERFORMANCE CHARACTERISTICS

Output P1dB

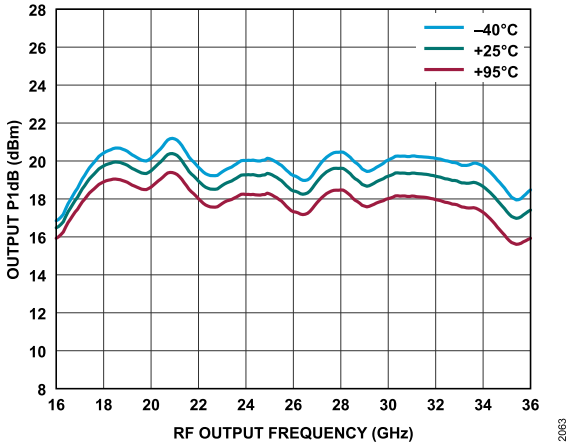


Figure 65. Output P1dB vs. RF Output Frequency at Various Temperatures

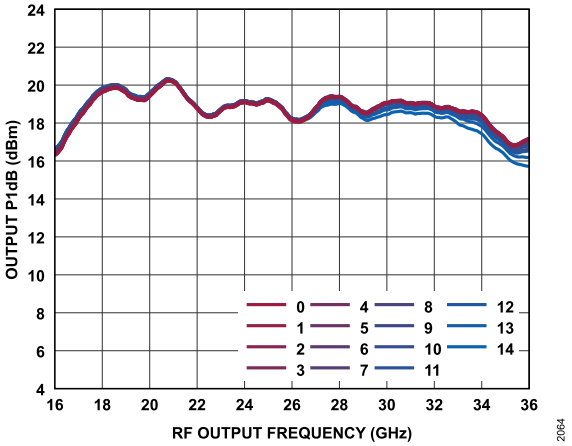


Figure 66. Output P1dB vs. RF Output Frequency at Various DSA1 Settings

TYPICAL PERFORMANCE CHARACTERISTICS

Sideband Rejection

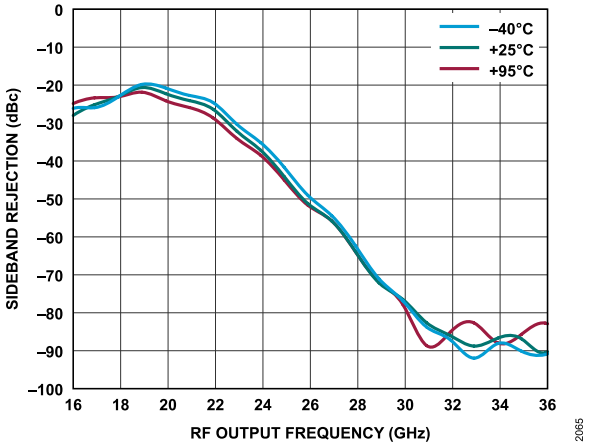


Figure 67. Sideband Rejection vs. RF Output Frequency at Various Temperatures with No Calibration and No RF Filters Applied

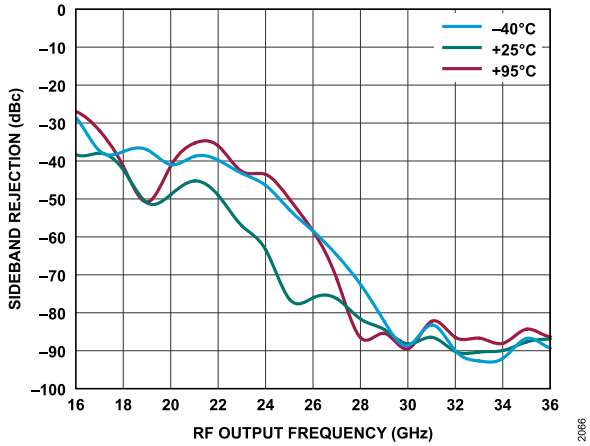


Figure 68. Sideband Rejection vs. RF Output Frequency at Various Temperatures with Optimization at 25°C and No RF Filters Applied

TYPICAL PERFORMANCE CHARACTERISTICS

Spurs

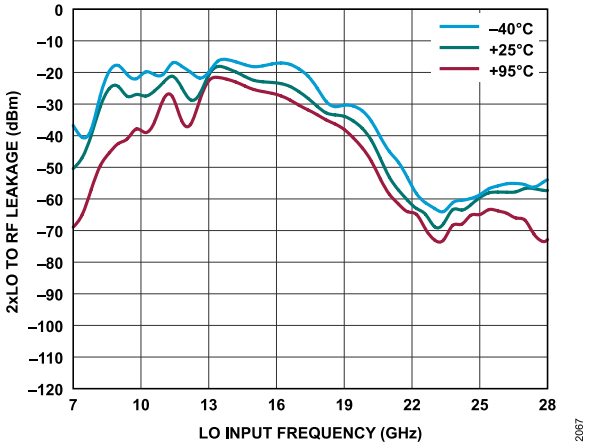


Figure 69. 2×LO to RF Leakage vs. LO Input Frequency at Various Temperatures with No Calibration and No RF Filters Applied

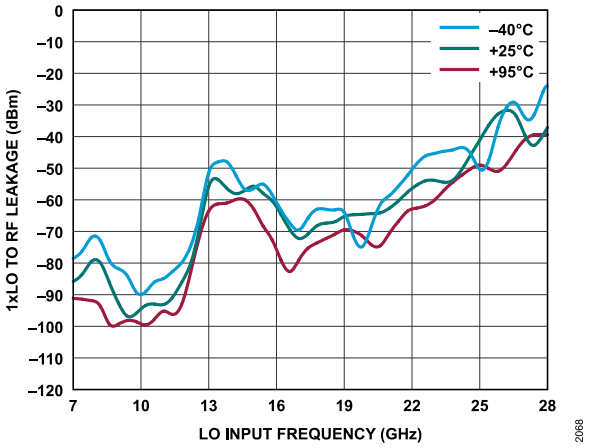


Figure 70. 1×LO to RF Leakage vs. LO Input Frequency at Various Temperatures with No Calibration and No RF Filters Applied

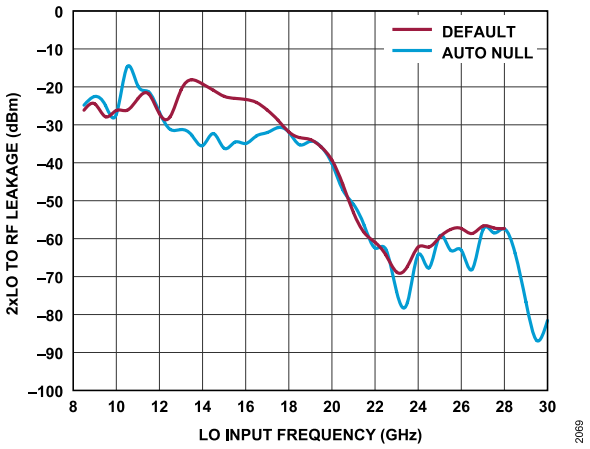


Figure 71. 2×LO to RF Leakage vs. LO Input Frequency at 25°C, With and Without Auto LO Nulling Calibration and No RF Filters Applied

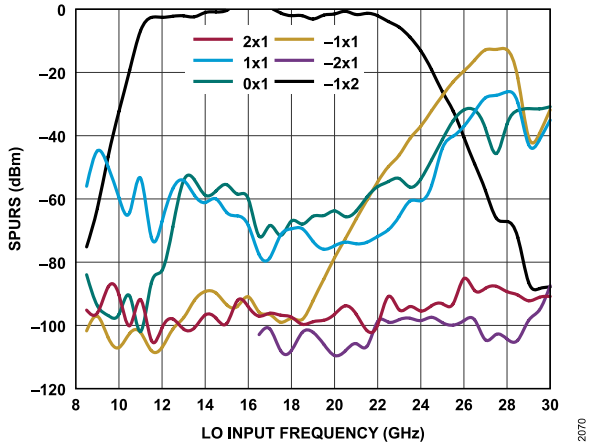


Figure 72. (IF × m) + 1× LO Spurs to RF Leakage vs. LO Input Frequency with No RF Filters Applied

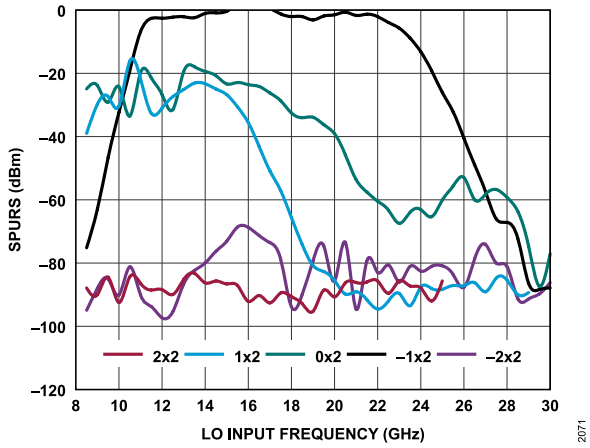


Figure 73. (IF × m) + 2× LO Spurs to RF Leakage vs. LO Input Frequency with No RF Filters Applied

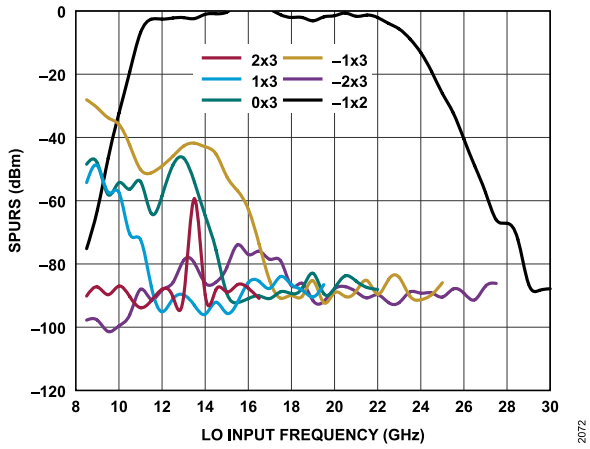


Figure 74. (IF × m) + 3× LO Spurs to RF Leakage vs. LO Input Frequency with No RF Filters Applied

TYPICAL PERFORMANCE CHARACTERISTICS

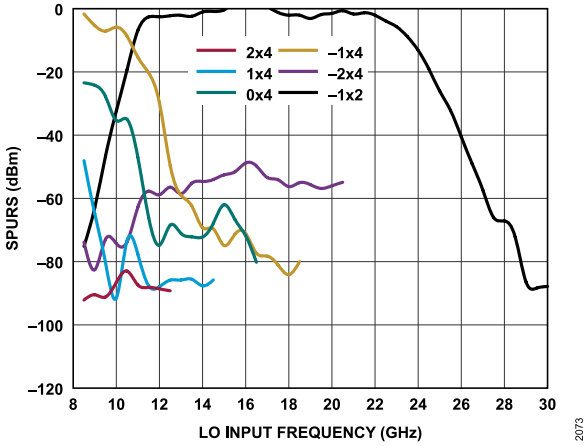


Figure 75. (IF × m) + 4× LO Spurs to RF Leakage vs. LO Input Frequency with No RF Filters Applied

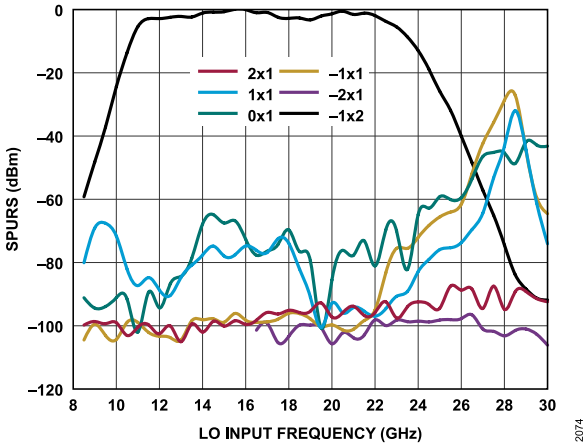


Figure 76. (IF × m) + 1× LO Spurs to RF Leakage vs. LO Input Frequency with LO and RF Filter Settings Adjusted with Sweeping Frequency

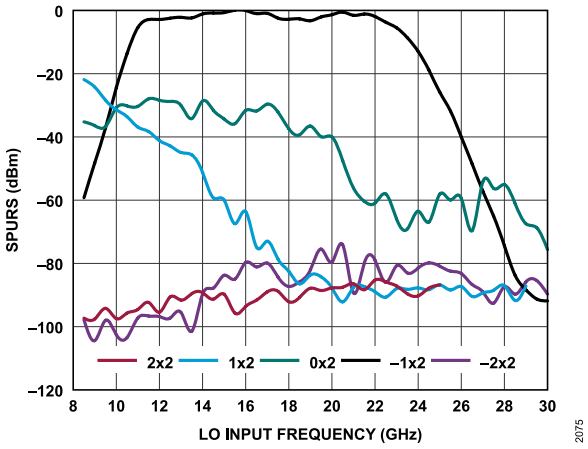


Figure 77. (IF × m) + 2× LO Spurs to RF Leakage vs. LO Input Frequency with LO and RF Filter Settings Adjusted with Sweeping Frequency

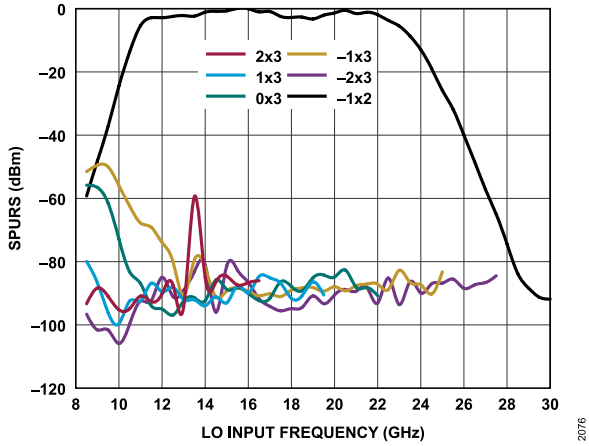


Figure 78. (IF × m) + 3× LO Spurs to RF Leakage vs. LO Input Frequency with LO and RF Filter Settings Adjusted with Sweeping Frequency

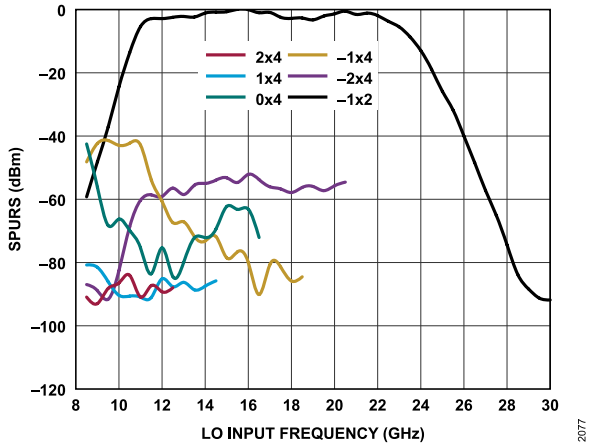


Figure 79. (IF × m) + 4× LO Spurs to RF Leakage vs. LO Input Frequency with LO and RF Filter Settings Adjusted with Sweeping Frequency

TYPICAL PERFORMANCE CHARACTERISTICS

COMPLEX IF MODE, IF_X, HIGH BAND

All measurements use IF_I and IF_Q as inputs and RF_OUT as an output with the RF high-band settings. VDD_DRV = 3V, all other supply voltages = 1.8V, and T_C = 25°C, unless otherwise noted.

All measurements taken with P_{IF} = −21dBm, P_{LO} = −5dBm, f_{IF} = 1GHz, f_{RF} = 49GHz, f_{LO} = 48GHz (upper sideband), maximum gain, RF LPF setting = 0x00 (highest cutoff), RF HPF setting = 0x3F (lowest cutoff), and LO tunable filter wideband high settings, unless otherwise noted. Trace and connector losses are de-embeded to the RF pins (see the IF_I and IF_Q input pins and RF_OUT output pin in Figure 3).

Conversion Gain

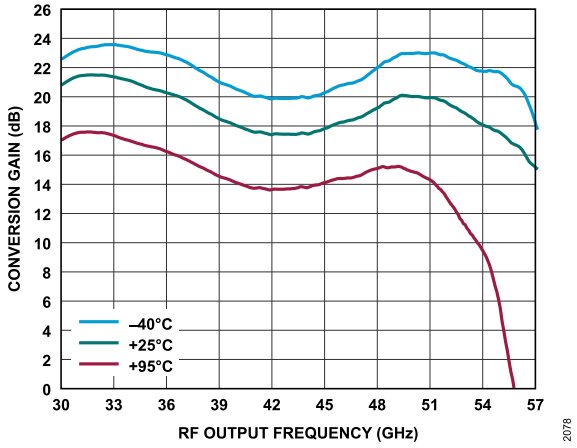


Figure 80. Conversion Gain vs. RF Output Frequency at Various Temperatures

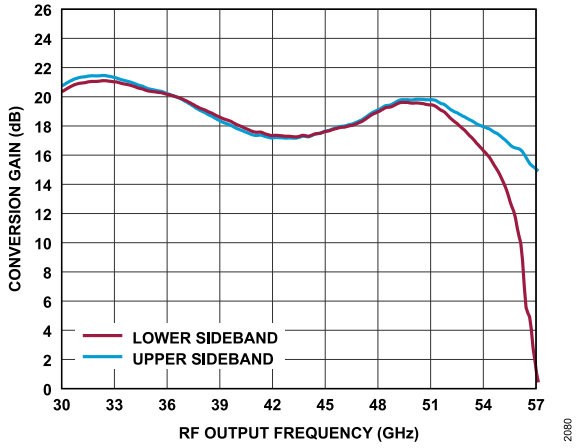


Figure 82. Conversion Gain vs. RF Output Frequency, Upper Sideband and Lower Sideband

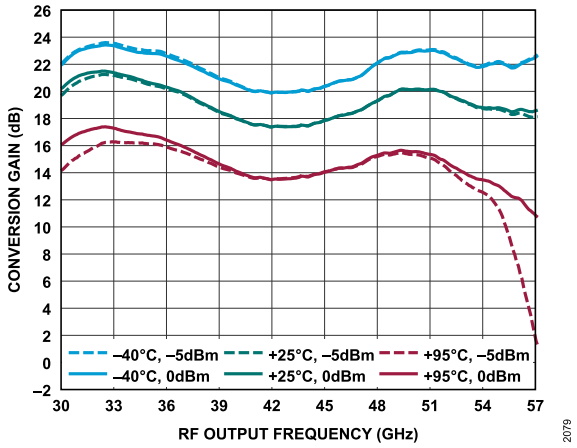


Figure 81. Conversion Gain vs. RF Output Frequency at Various Temperatures and LO Powers

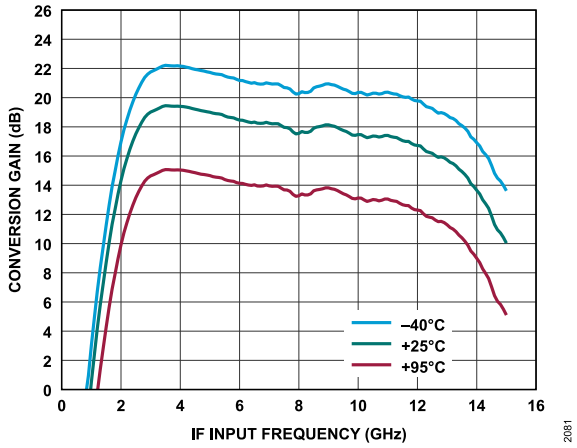


Figure 83. Conversion Gain vs. IF Input Frequency at Various Temperatures, High Frequency Complex IF Mode

TYPICAL PERFORMANCE CHARACTERISTICS

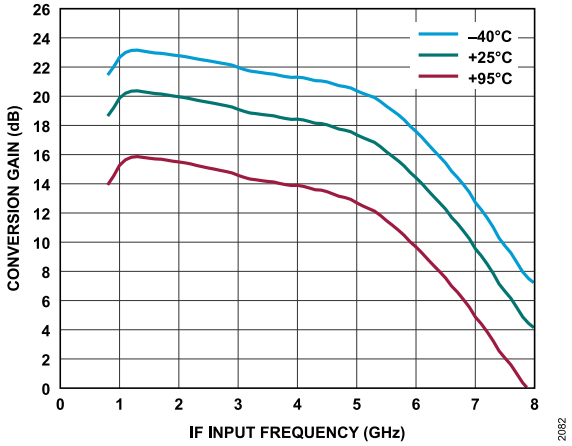


Figure 84. Conversion Gain vs. IF Input Frequency at Various Temperatures, Low Frequency Complex IF Mode

TYPICAL PERFORMANCE CHARACTERISTICS

Output IP3

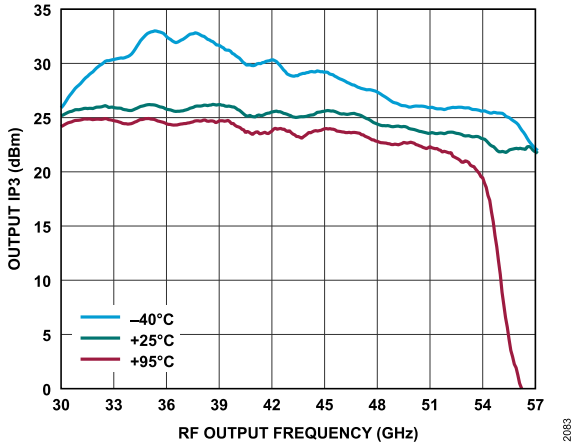


Figure 85. Output IP3 vs. RF Output Frequency at Various Temperatures

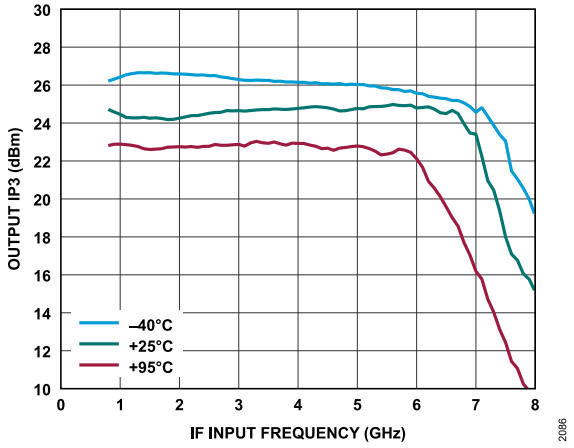


Figure 88. Output IP3 vs. IF Input Frequency at Various Temperatures, Low Frequency Complex IF Mode

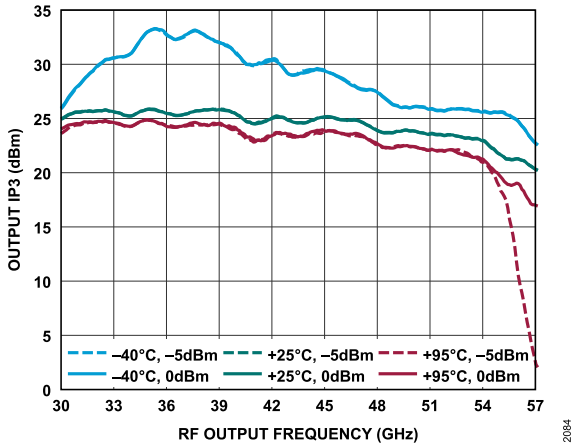


Figure 86. Output IP3 vs. RF Output Frequency at Various Temperatures for Various Temperatures and LO Powers

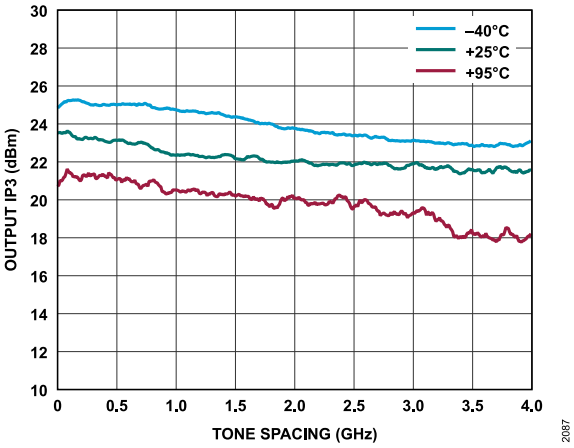


Figure 89. Output IP3 vs. Tone Spacing at Various Temperatures

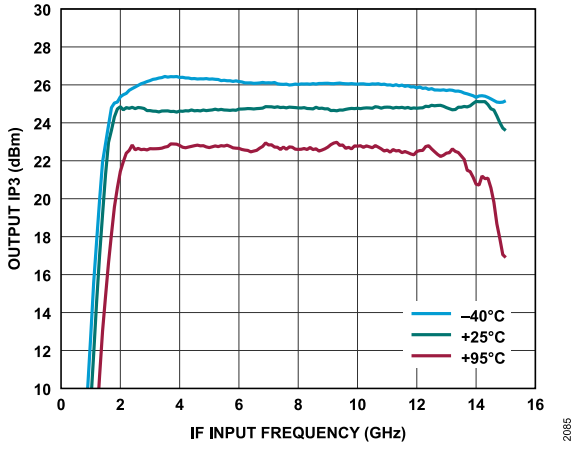


Figure 87. Output IP3 vs. IF Input Frequency at Various Temperatures, High Frequency Complex IF Mode

TYPICAL PERFORMANCE CHARACTERISTICS

Noise Figure

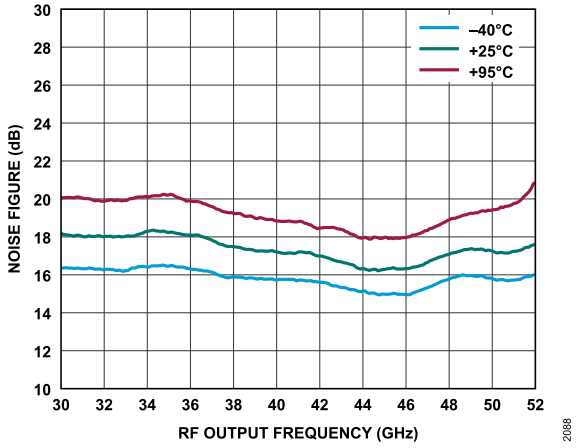


Figure 90. Noise Figure vs. RF Output Frequency at Various Temperatures

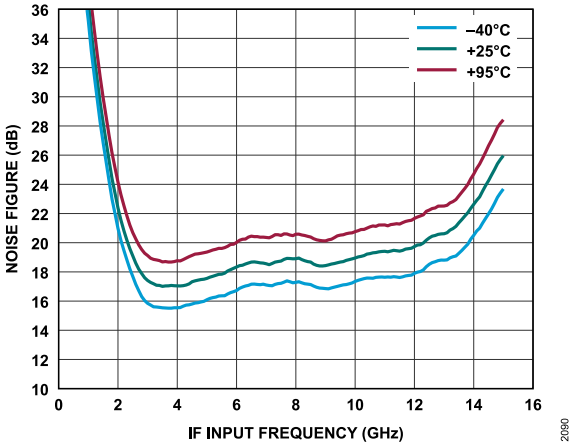


Figure 92. Noise Figure vs. IF Input Frequency at Various Temperatures, High Frequency Complex IF Mode

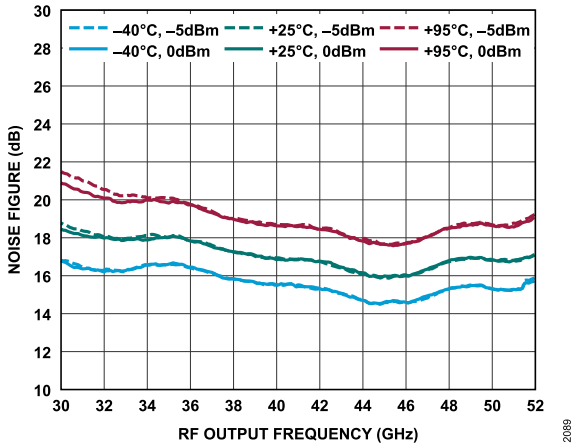


Figure 91. Noise Figure vs. RF Output Frequency at Various Temperatures and LO Powers

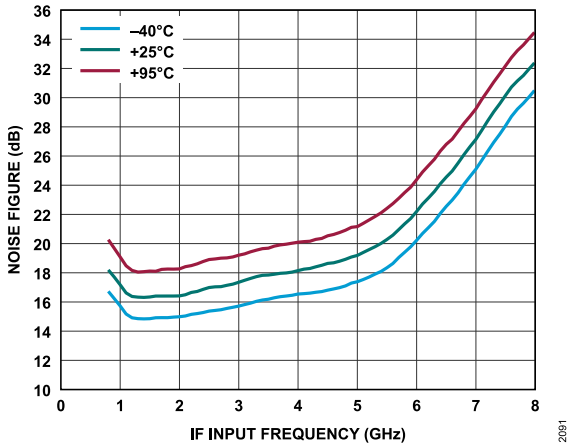


Figure 93. Noise Figure vs. IF Input Frequency at Various Temperatures, Low Frequency Complex IF Mode

TYPICAL PERFORMANCE CHARACTERISTICS

Output P1dB

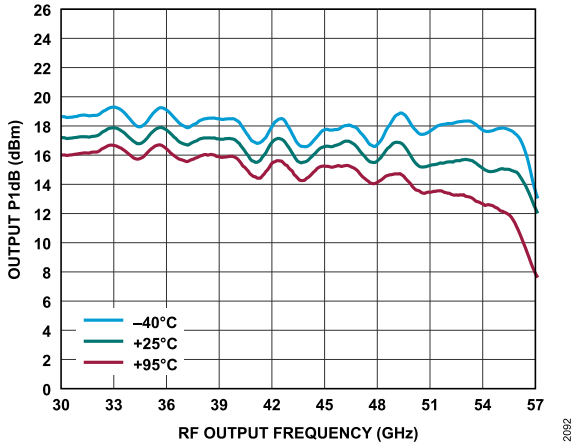


Figure 94. Output P1dB vs. RF Output Frequency at Various Temperatures

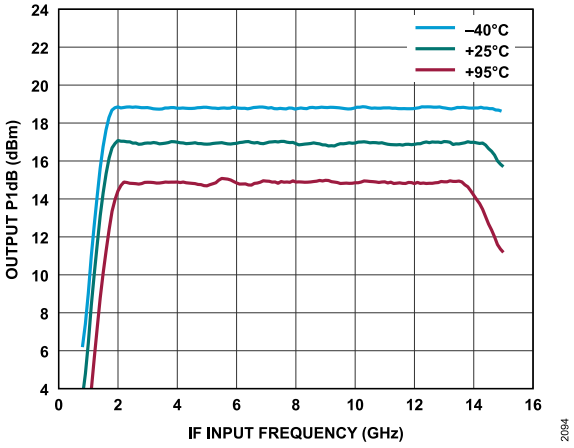


Figure 96. Output P1dB vs. IF Input Frequency at Various Temperatures, High Frequency Complex IF Mode

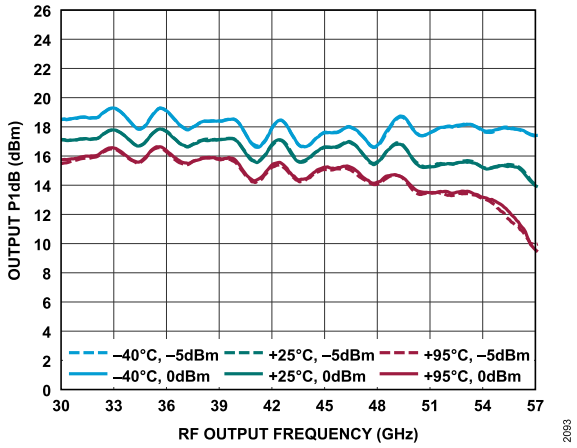


Figure 95. Output P1dB vs. RF Output Frequency at Various Temperatures and LO Powers

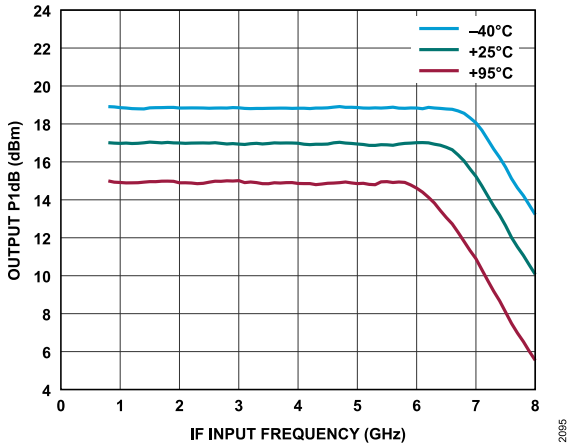


Figure 97. Output P1dB vs. IF Input Frequency at Various Temperatures, Low Frequency Complex IF Mode

TYPICAL PERFORMANCE CHARACTERISTICS

Sideband Rejection

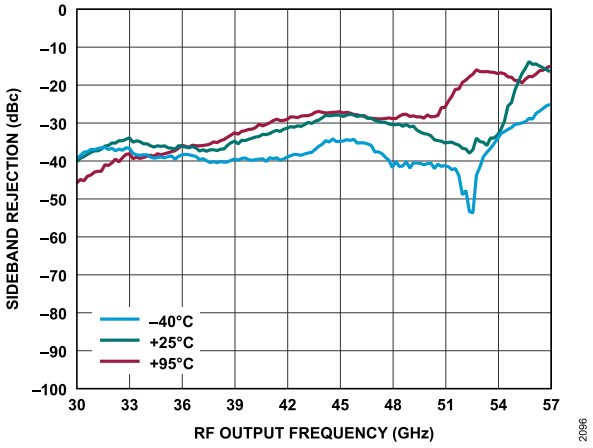


Figure 98. Sideband Rejection vs. RF Output Frequency at Various Temperatures with No Calibration and, No RF Filters Applied

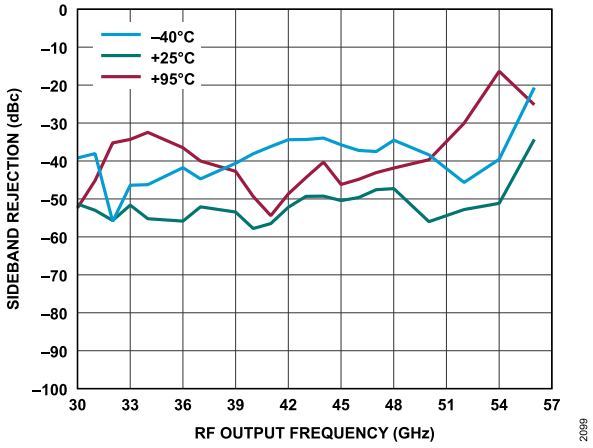


Figure 101. Sideband Rejection vs. RF Output Frequency at Various Temperatures with Optimization at 25°C and No RF Filters Applied

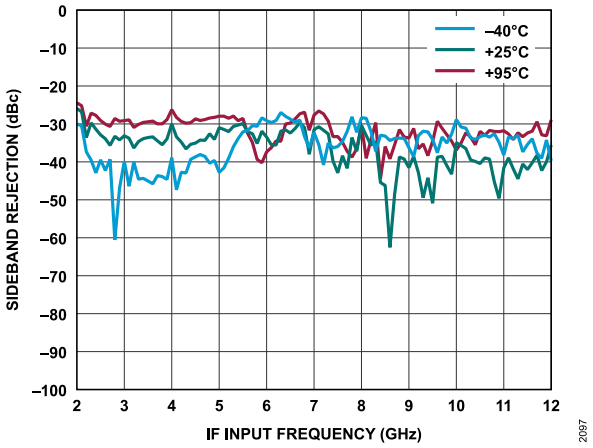


Figure 99. Sideband Rejection vs. IF Input Frequency at Various Temperatures with No Calibration, No RF Filters Applied, and High Frequency Complex IF Mode

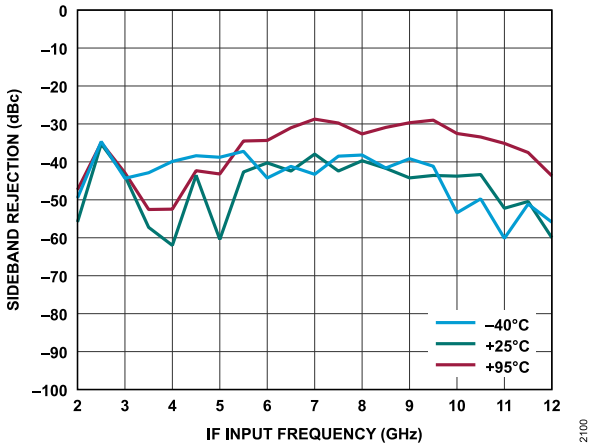


Figure 102. Sideband Rejection vs. IF Input Frequency at Various Temperatures with Optimization at 25°C, No RF Filters Applied, and High Frequency Complex IF Mode

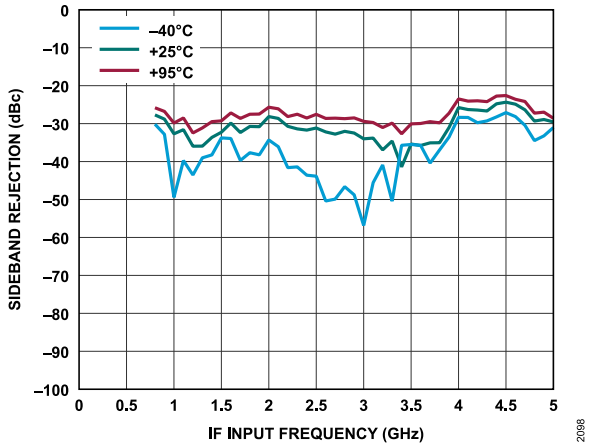


Figure 100. Sideband Rejection vs. IF Input Frequency at Various Temperatures with No Calibration, No RF Filters Applied, and Low Frequency Complex IF Mode

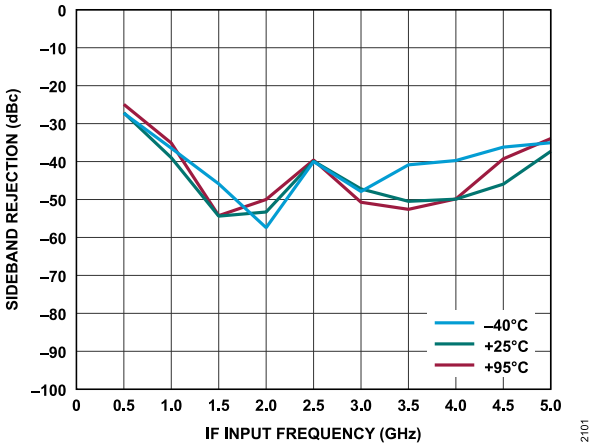


Figure 103. Sideband Rejection vs. IF Input Frequency at Various Temperatures with Optimization at 25°C, No RF Filters Applied, and Low Frequency Complex IF Mode

TYPICAL PERFORMANCE CHARACTERISTICS

Spurs

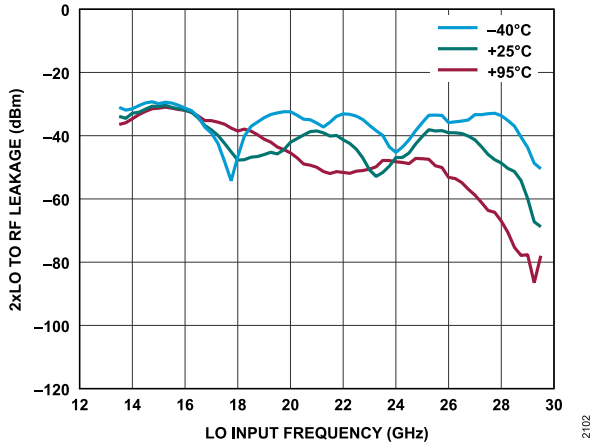


Figure 104. 2×LO to RF Leakage vs. LO Input Frequency at Various Temperatures with No Calibration and No RF Filters Applied

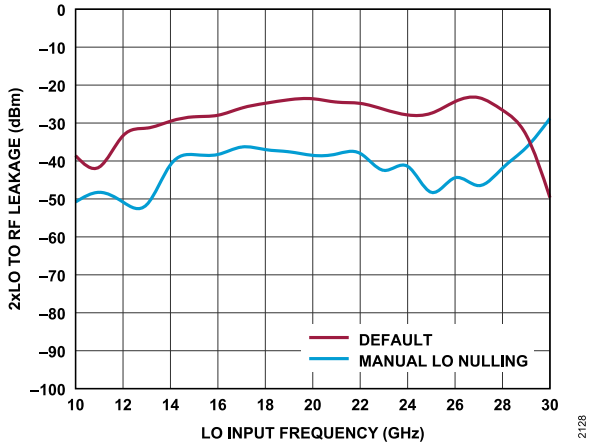


Figure 107. 2×LO to RF Leakage vs. LO Input Frequency at 25°C, With and Without Manual LO Nulling Calibration, and No RF Filters Applied

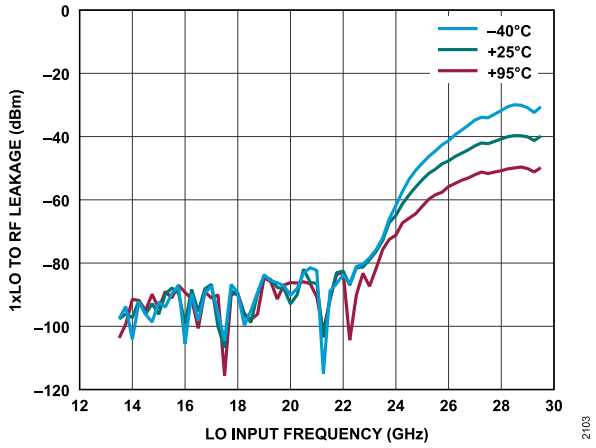


Figure 105. 1×LO to RF Leakage vs. LO Input Frequency at Various Temperatures with No Calibration and No RF Filters Applied

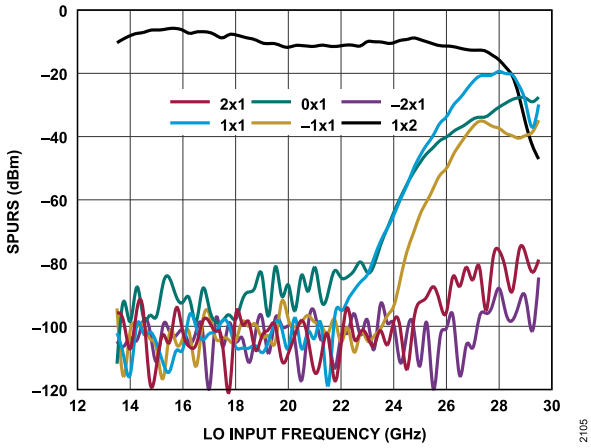


Figure 108. (IF × m) + 1× LO Spurs to RF Leakage vs. LO Input Frequency with No RF Filters Applied

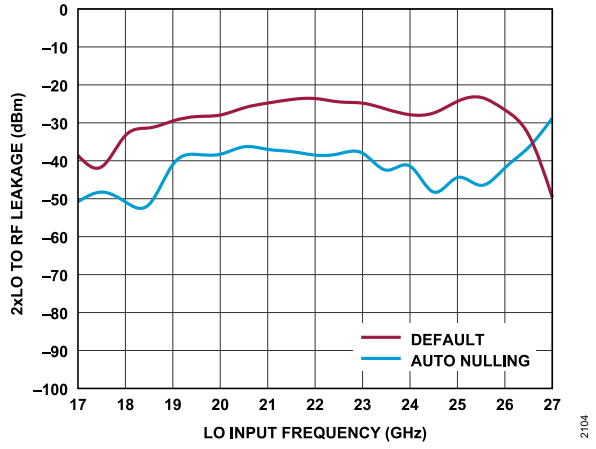


Figure 106. 2×LO to RF Leakage vs. LO Input Frequency at 25°C, With and Without Auto LO Nulling Calibration, and No RF Filters Applied

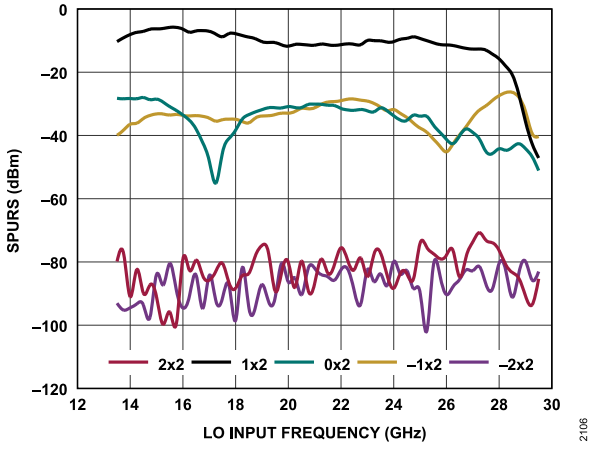


Figure 109. (IF × m) + 2× LO Spurs to RF Leakage vs. LO Input Frequency with No RF Filters Applied

TYPICAL PERFORMANCE CHARACTERISTICS

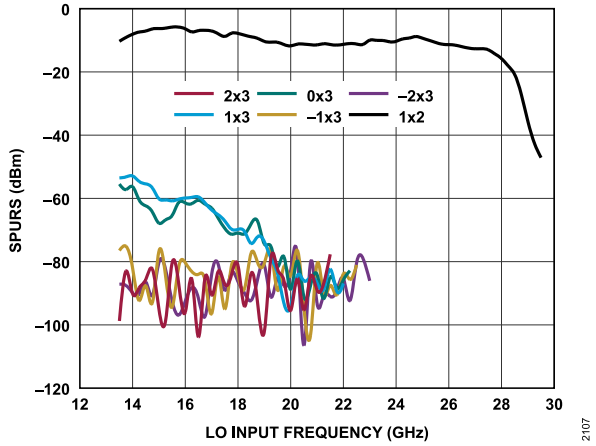


Figure 110. (IF × m) + 3× LO Spurs to RF Leakage vs. LO Input Frequency with No RF Filters Applied

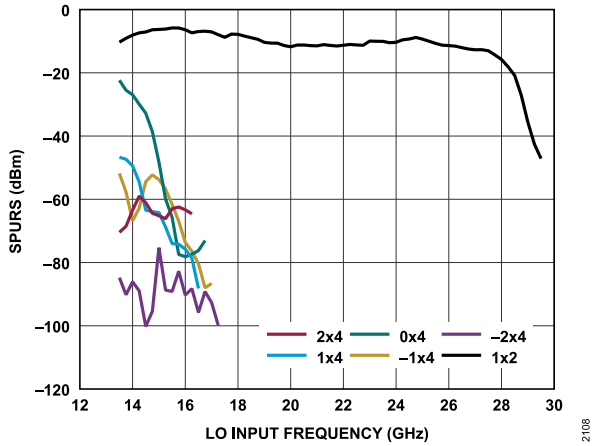


Figure 111. (IF × m) + 4× LO Spurs to RF Leakage vs. LO Input Frequency with No RF Filters Applied

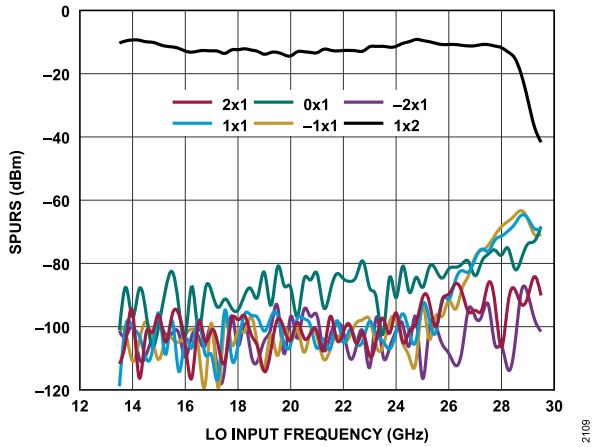


Figure 112. (IF × m) + 1× LO Spurs to RF Leakage vs. LO Input Frequency with LO and RF Filter Settings Adjusted with Sweeping Frequency

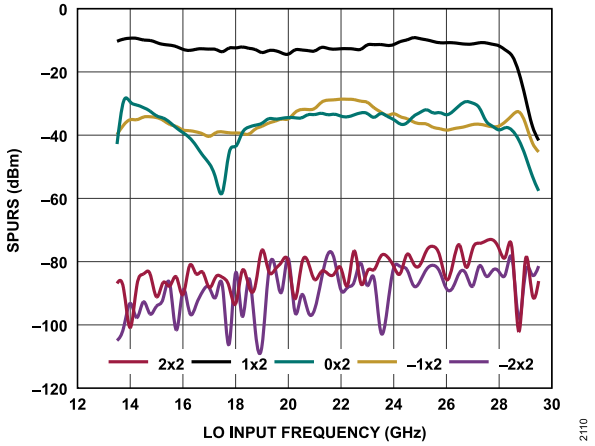


Figure 113. (IF × m) + 2× LO Spurs to RF Leakage vs. LO Input Frequency with LO and RF Filter Settings Adjusted with Sweeping Frequency

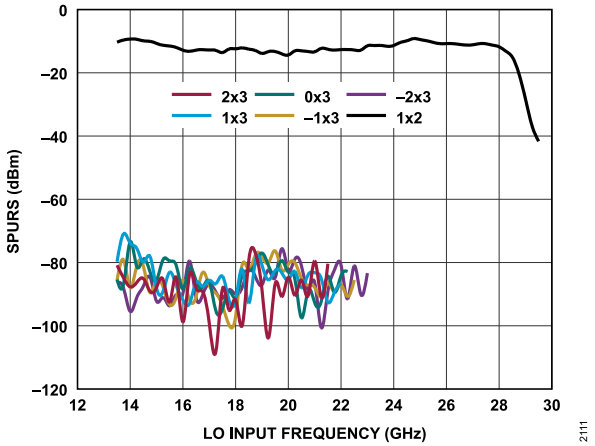


Figure 114. (IF × m) + 3× LO Spurs to RF Leakage vs. LO Input Frequency and LO and RF Filter Settings Adjusted with Sweeping Frequency

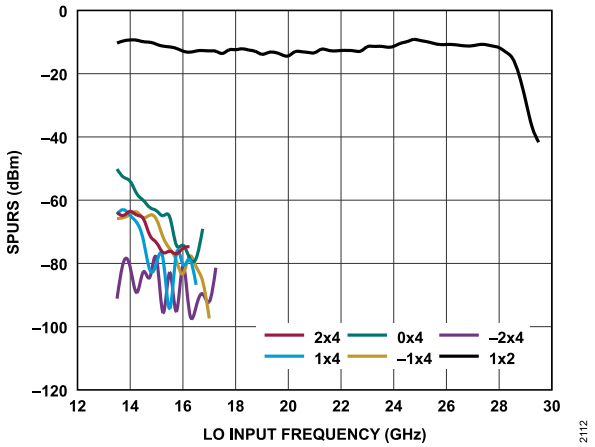


Figure 115. (IF × m) + 4× LO Spurs to RF Leakage vs. LO Input Frequency and LO and RF Filter Settings Adjusted with Sweeping Frequency

TYPICAL PERFORMANCE CHARACTERISTICS

COMPLEX IF MODE, IF_X, LOW BAND

All measurements use IF_I and IF_Q as inputs and RF_OUT as an output with the RF low-band settings. VDD_DRV = 3V, all other supply voltages = 1.8V, and T_C = 25°C, unless otherwise noted.

All measurements taken with P_{IF} = −21dBm, P_{LO} = −5dBm, f_{IF} = 1GHz, lower sideband, maximum gain, RF LPF setting = 0x00 (highest cutoff), and LO tunable filter wideband high settings, unless otherwise noted. Trace and connector losses are de-embeded to the RF pins (see the IF_I and IF_Q input pins and RF_OUT output pin in Figure 3).

Conversion Gain

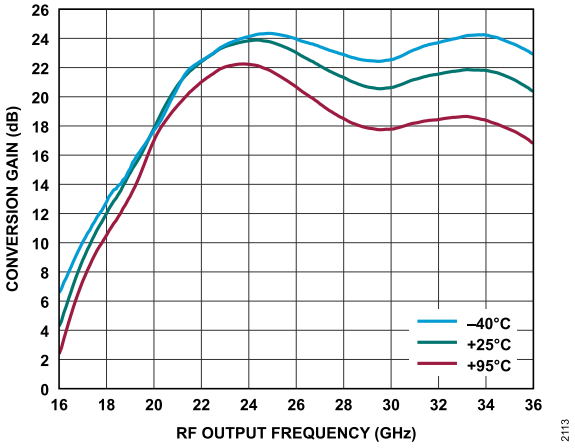


Figure 116. Conversion Gain vs. RF Output Frequency at Various Temperatures

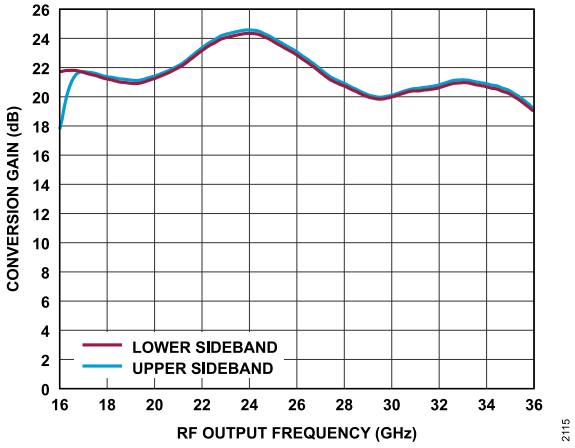


Figure 118. Conversion Gain vs. RF Output Frequency, Upper Sideband and Lower Sideband

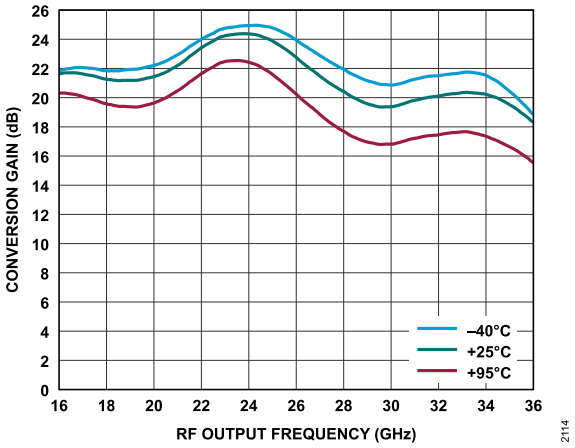


Figure 117. Conversion Gain vs. RF Output Frequency at Various Temperatures and Wideband Low LO Filter

TYPICAL PERFORMANCE CHARACTERISTICS

Output IP3

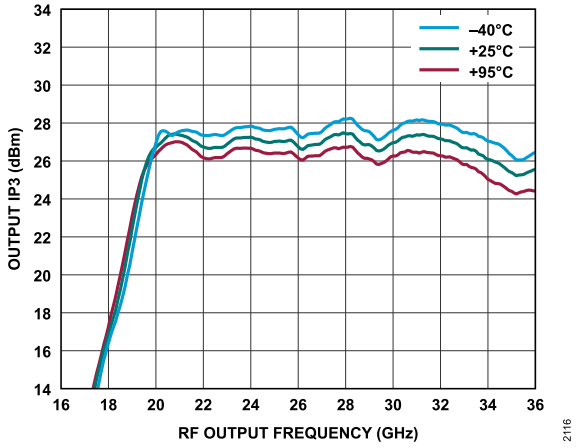


Figure 119. Output IP3 vs. RF Output Frequency at Various Temperatures

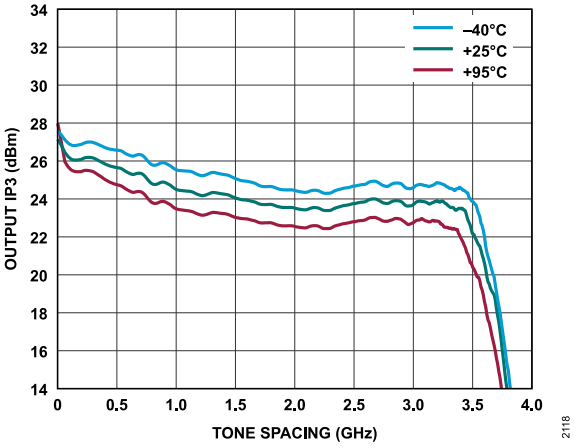


Figure 121. Output IP3 vs. Tone Spacing at Various Temperatures

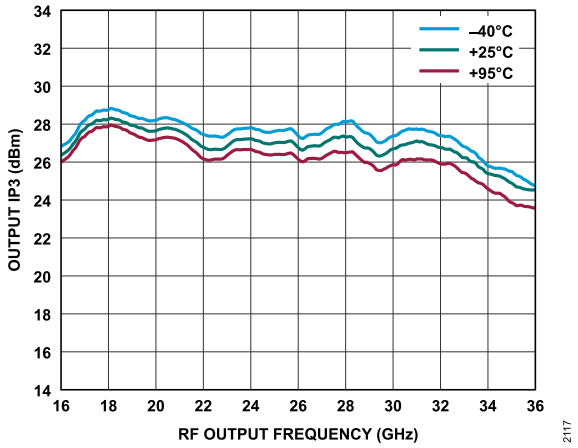


Figure 120. Output IP3 vs. RF Output Frequency at Various Temperatures and Wideband Low LO Filter

TYPICAL PERFORMANCE CHARACTERISTICS

Noise Figure

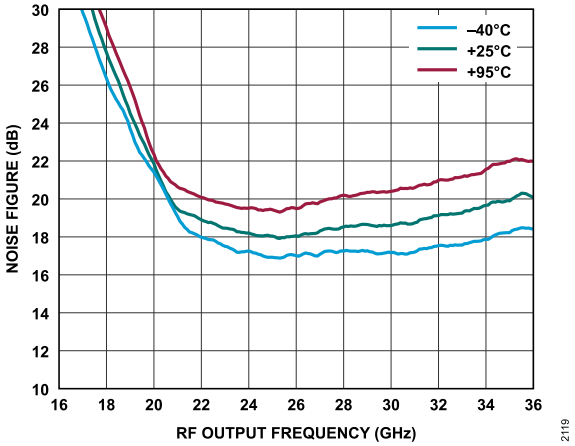


Figure 122. Noise Figure vs. RF Output Frequency at Various Temperatures

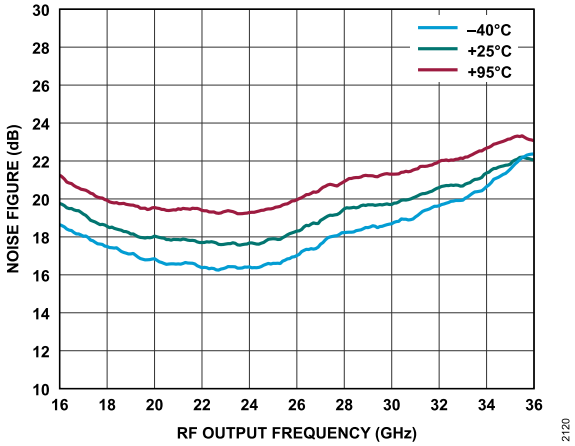


Figure 123. Noise Figure vs. RF Output Frequency at Various Temperatures and Wideband Low LO Filter

TYPICAL PERFORMANCE CHARACTERISTICS

Output P1dB

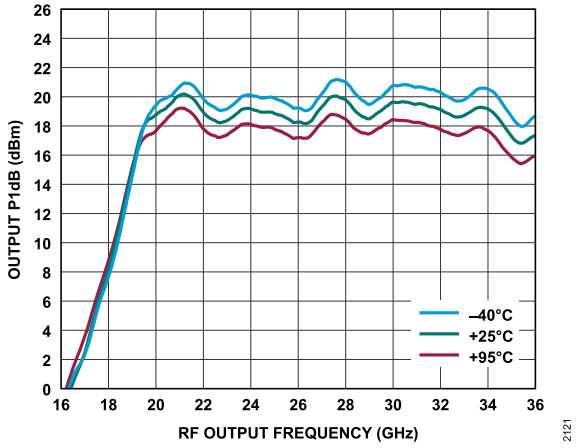


Figure 124. Output P1dB vs. RF Output Frequency at Various Temperatures

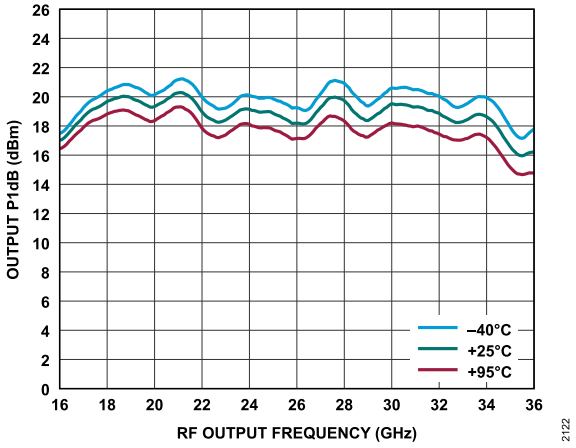


Figure 125. Output P1dB vs. RF Output Frequency at Various Temperatures and Wideband Low LO Filter

TYPICAL PERFORMANCE CHARACTERISTICS

Sideband Rejection

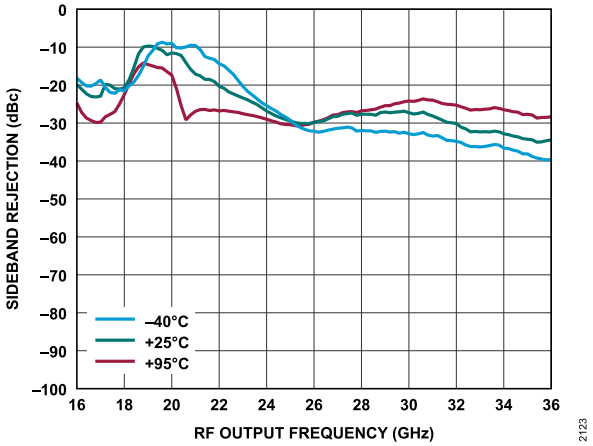


Figure 126. Sideband Rejection vs. RF Output Frequency at Various Temperatures with No Calibration and No RF Filters Applied, and Wideband High LO Filter

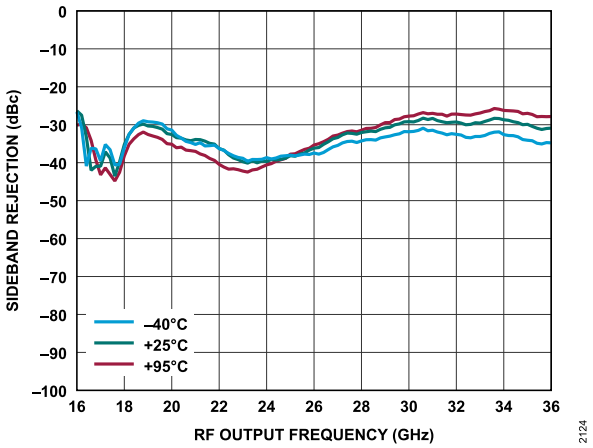


Figure 127. Sideband Rejection vs. RF Output Frequency at Various Temperatures with No Calibration and No RF Filters Applied, and Wideband Low LO Filter

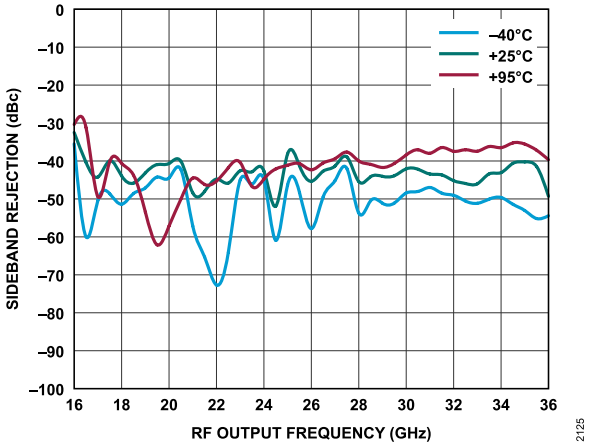


Figure 128. Sideband Rejection vs. RF Output Frequency at Various Temperatures with Optimization at 25°C, No RF Filters Applied, and LO Filter Settings Adjusted with Sweeping Frequency

TYPICAL PERFORMANCE CHARACTERISTICS

Spurs

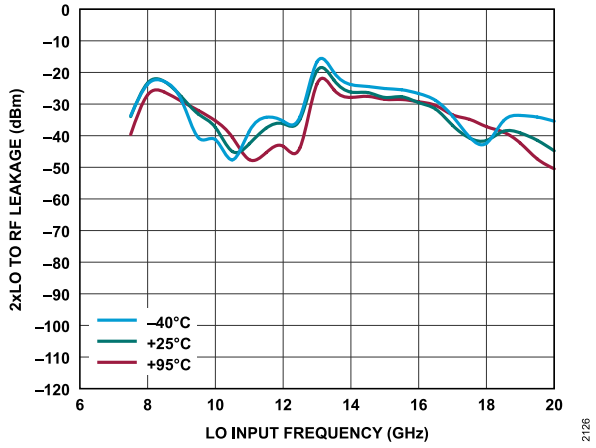


Figure 129. 2×LO to RF Leakage vs. LO Input Frequency at Various Temperatures with No Calibration and No RF Filters Applied

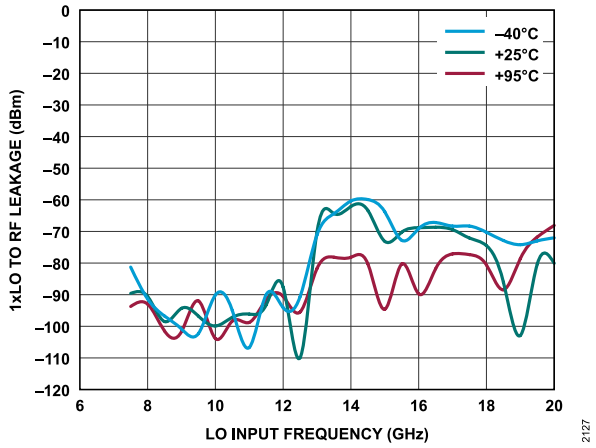


Figure 130. 1×LO to RF Leakage vs. LO Input Frequency at Various Temperatures with No Calibration and No RF Filters Applied

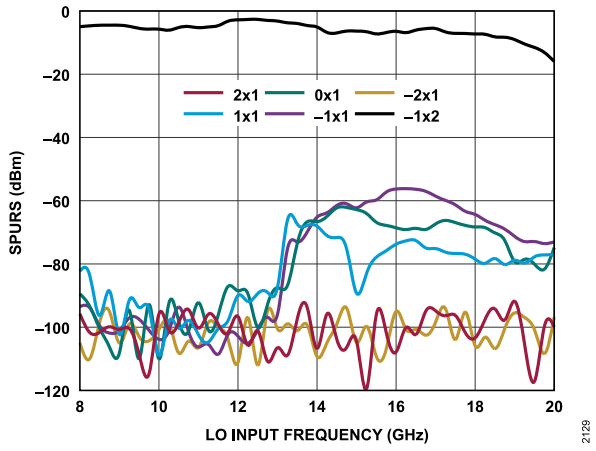


Figure 131. (IF × m) + 1× LO Spurs to RF Leakage vs. LO Input Frequency with No Wideband RF Filters Applied

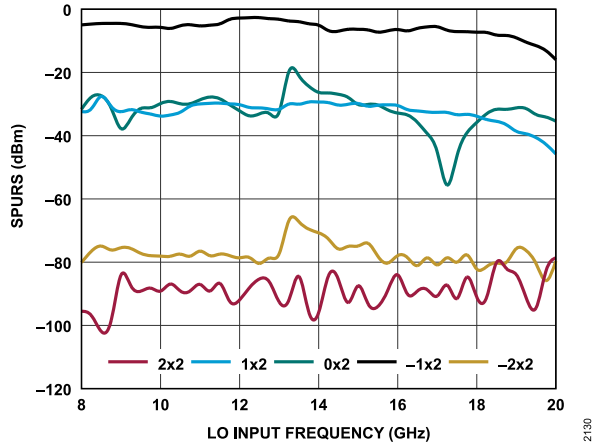


Figure 132. (IF × m) + 2× LO Spurs to RF Leakage vs. LO Input Frequency with No RF Filters Applied

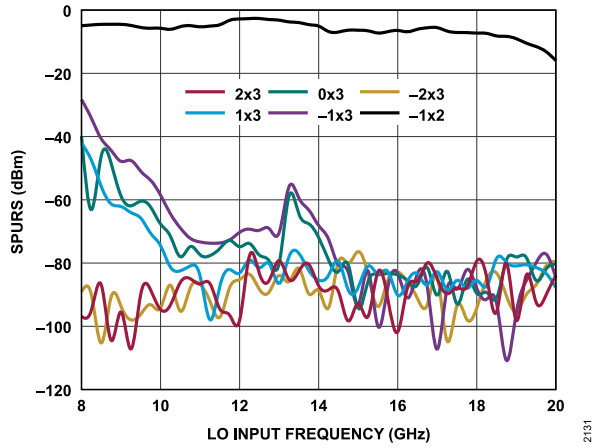


Figure 133. (IF × m) + 3× LO Spurs to RF Leakage vs. LO Input Frequency with No RF Filters Applied

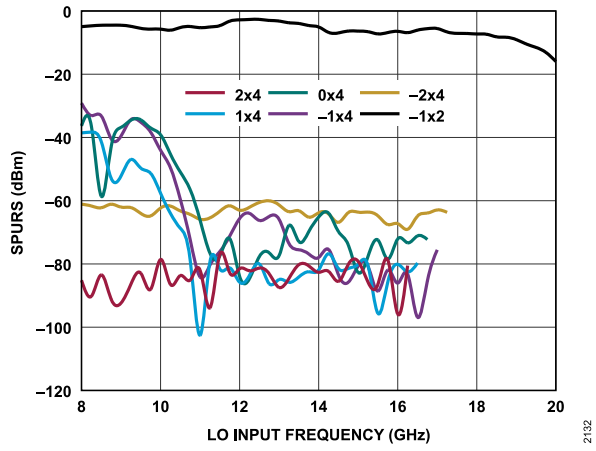


Figure 134. (IF × m) + 4× LO Spurs to RF Leakage vs. LO Input Frequency with No RF Filters Applied

TYPICAL PERFORMANCE CHARACTERISTICS

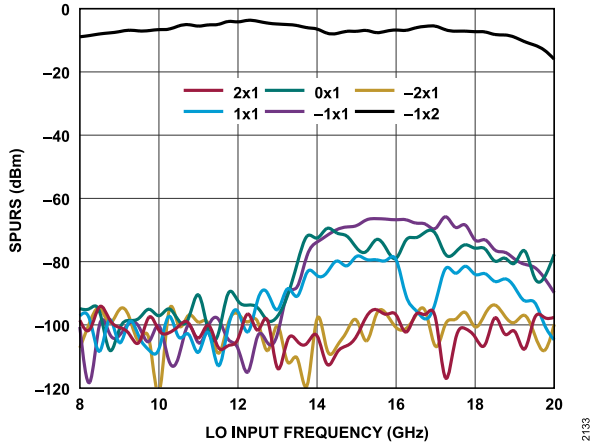


Figure 135. (IF × m) + 1× LO Spurs to RF Leakage vs. LO Input Frequency with LO and RF Filter Settings Adjusted with Sweeping Frequency

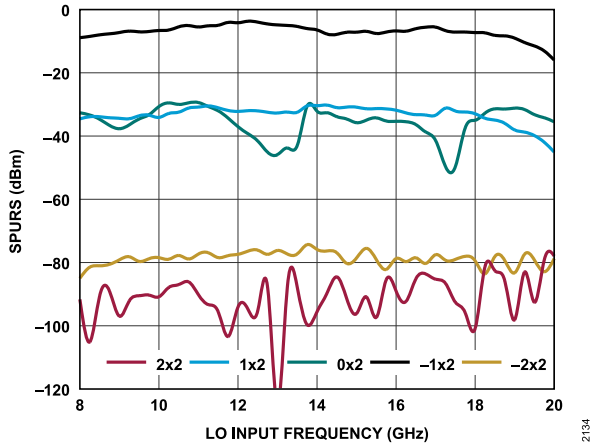


Figure 136. (IF × m) + 2× LO Spurs to RF Leakage vs. LO Input Frequency with LO and RF Filter Settings Adjusted with Sweeping Frequency

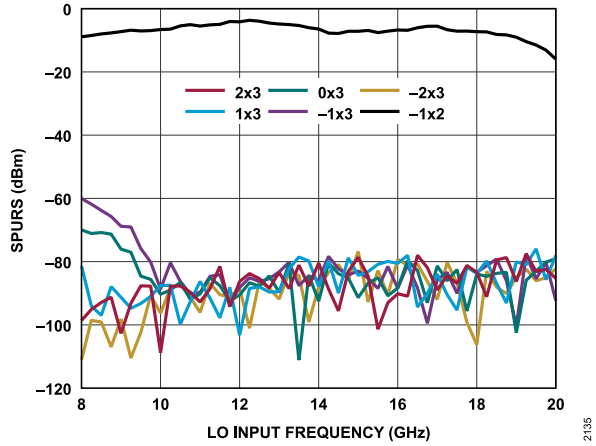


Figure 137. (IF × m) + 3× LO Spurs to RF Leakage vs. LO Input Frequency, LO and RF Filter Settings Adjusted with Sweeping Frequency

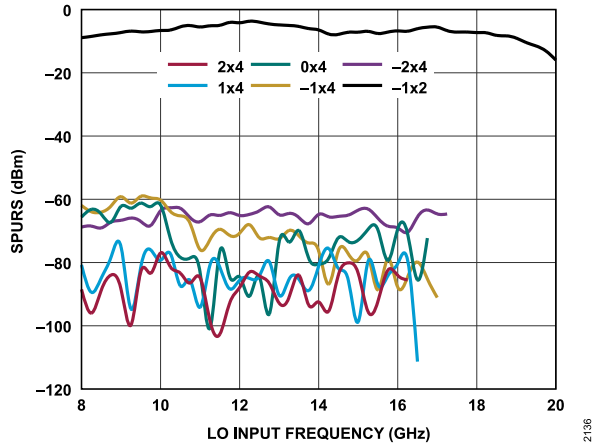


Figure 138. (IF × m) + 4× LO Spurs to RF Leakage vs. LO Input Frequency, LO and RF Filter Settings Adjusted with Sweeping Frequency

TYPICAL PERFORMANCE CHARACTERISTICS

I/Q BASEBAND MODE, BB_IX AND BB_QX, HIGH BAND

All measurements use BB_IP, BB_IN, BB_QP, and BB_QN as inputs and RF_OUT as an output with the RF high-band settings. VDD_DRV = 3V, all other supply voltages = 1.8V, and T_C = 25°C, unless otherwise noted.

Measurements performed with P_{BB} = −20dBm, P_{LO} = 0dBm, f_{BB} = 100MHz, f_{RF} = 49GHz, f_{LO} = 48.9GHz (upper sideband), maximum gain, RF LPF setting = 0x00 (highest cutoff), RF HPF setting = 0x3F (lowest cutoff), LO tunable filter wideband high settings, and V_{ICM} = 1V, unless otherwise noted.

Conversion Gain

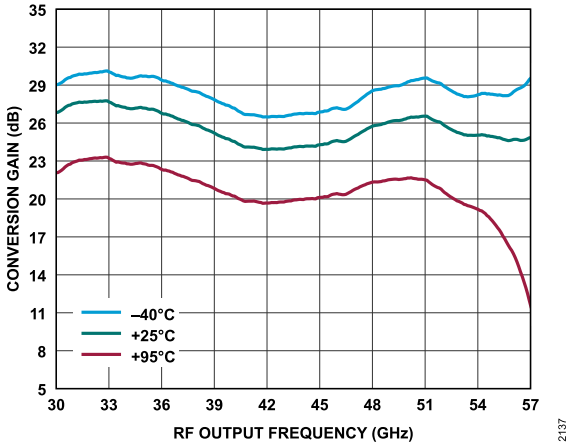


Figure 139. Conversion Gain vs. RF Output Frequency at Various Temperatures

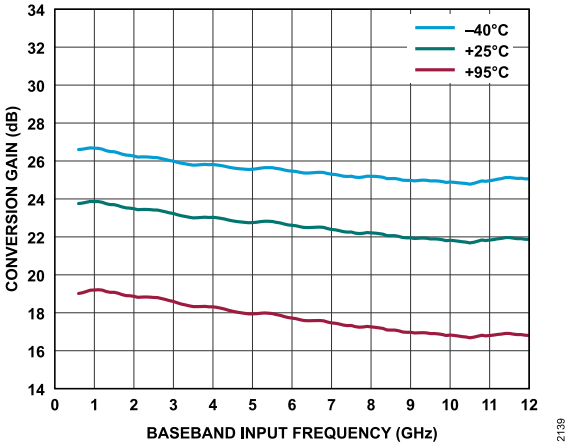


Figure 141. Conversion Gain vs. Baseband Input Frequency at Various Temperatures and High Frequency External Hybrid

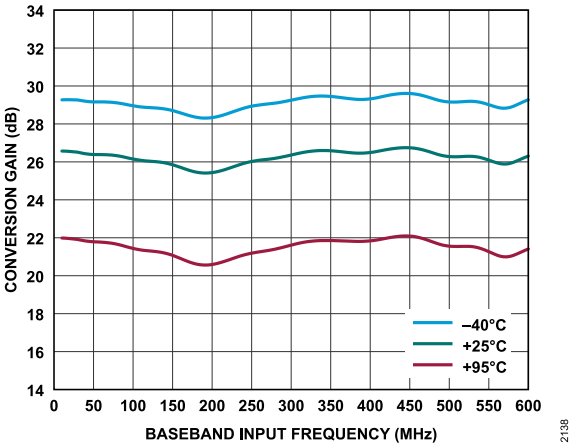


Figure 140. Conversion Gain vs. Baseband Input Frequency at Various Temperatures and Low Frequency External Hybrid

TYPICAL PERFORMANCE CHARACTERISTICS

Sideband Rejection

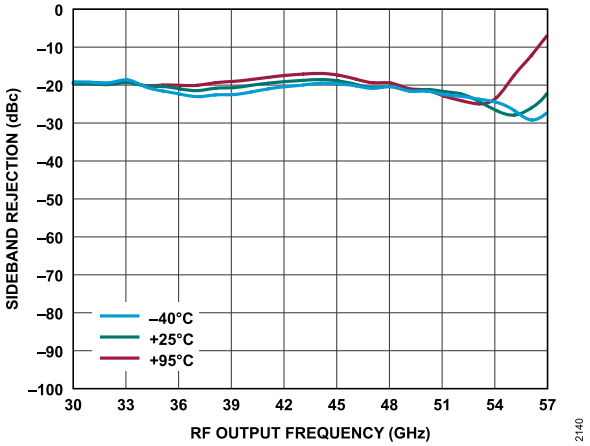


Figure 142. Sideband Rejection vs. RF Output Frequency at Various Temperatures with No Calibration and No RF Filters Applied

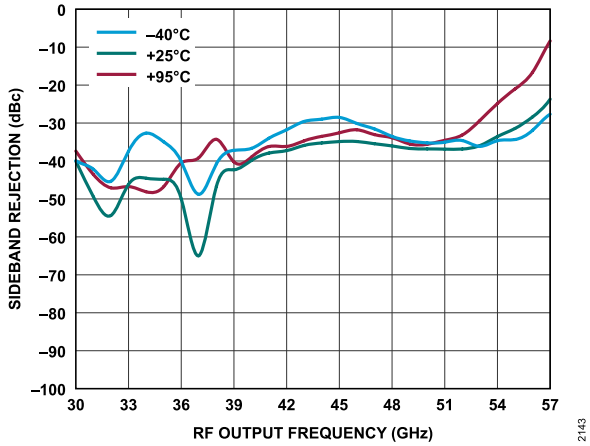


Figure 145. Sideband Rejection vs. RF Output Frequency at Various Temperatures with Optimization at 25°C and No RF Filters Applied

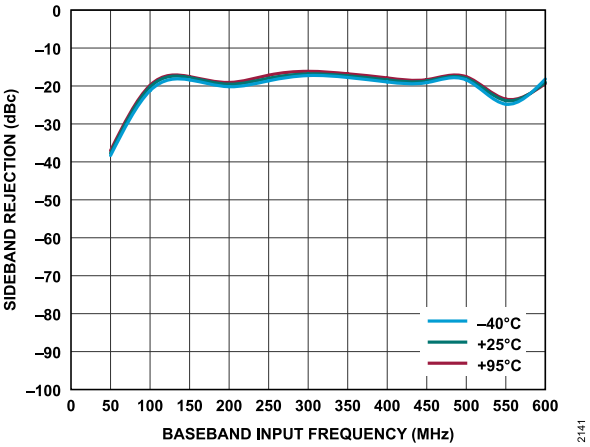


Figure 143. Sideband Rejection vs. Baseband Input Frequency at Various Temperatures with No Calibration, No RF Filters Applied, and Low Frequency External Hybrid

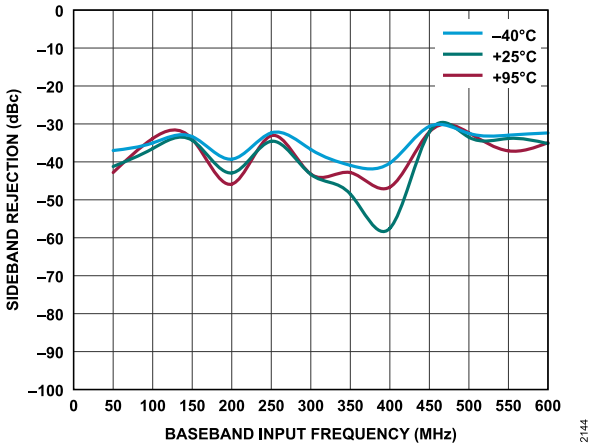


Figure 146. Sideband Rejection vs. Baseband Input Frequency at Various Temperatures with Optimization at 25°C, No RF Filters Applied, and Low Frequency External Hybrid

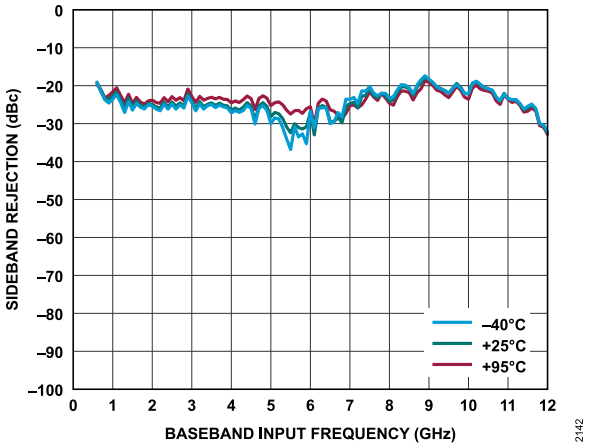


Figure 144. Sideband Rejection vs. Baseband Input Frequency at Various Temperatures with No Calibration, No RF Filters Applied, and High Frequency External Hybrid

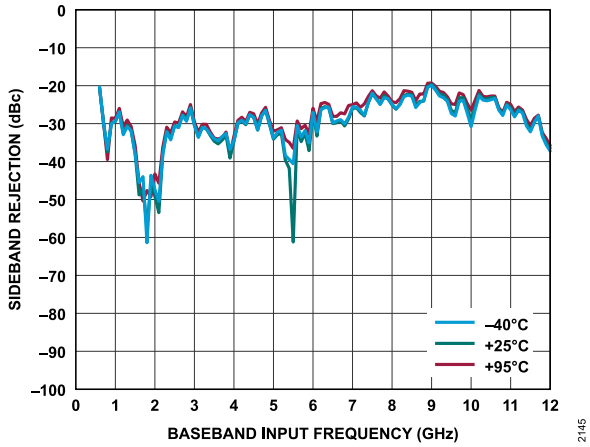


Figure 147. Sideband Rejection vs. Baseband Input Frequency at Various Temperatures with Optimization at 25°C, No RF Filters Applied, and High Frequency External Hybrid

TYPICAL PERFORMANCE CHARACTERISTICS

Output IP3

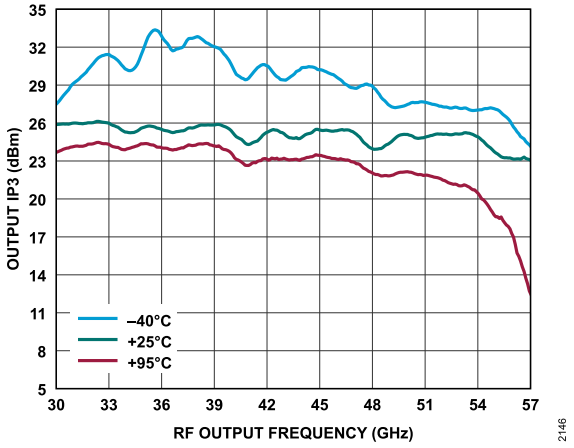


Figure 148. Output IP3 vs. RF Output Frequency at Various Temperatures

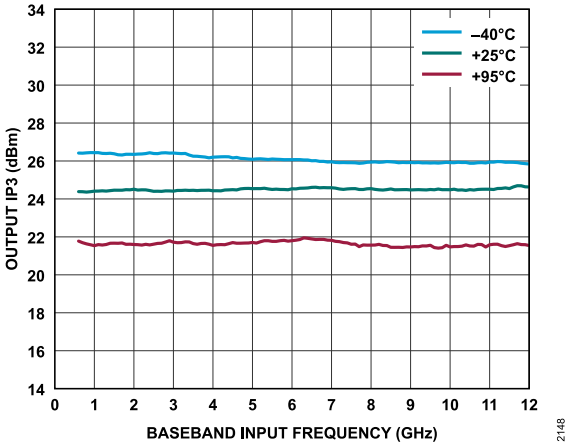


Figure 150. Output IP3 vs. Baseband Input Frequency at Various Temperatures, High Frequency Hybrid

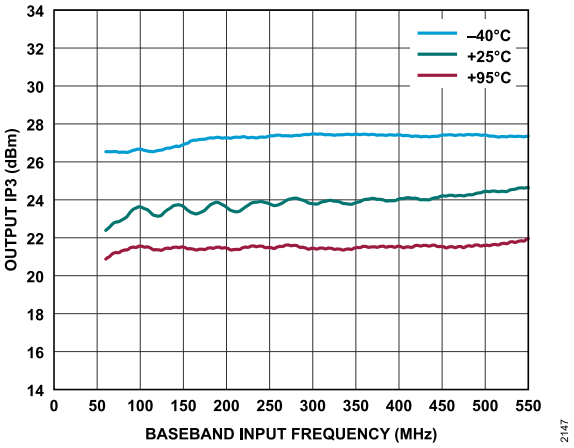


Figure 149. Output IP3 vs. Baseband Input Frequency at Various Temperatures, Low Frequency Hybrid

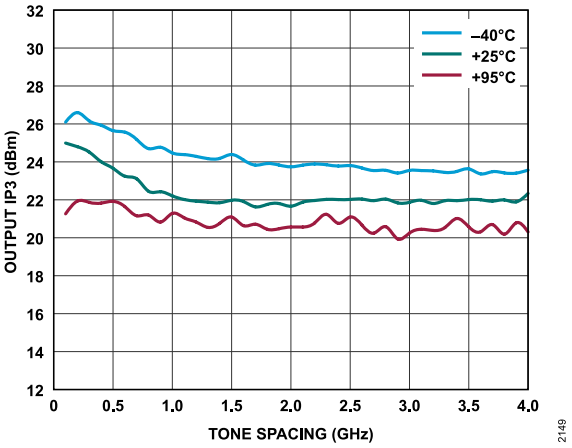


Figure 151. Output IP3 vs. Tone Spacing at Various Temperatures

TYPICAL PERFORMANCE CHARACTERISTICS

Noise Figure

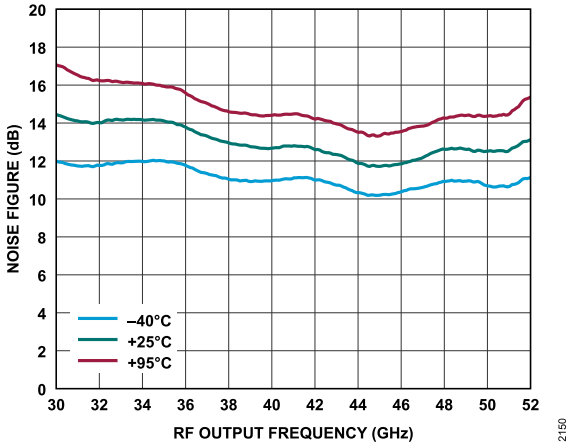


Figure 152. Noise Figure vs. RF Output Frequency at Various Temperatures

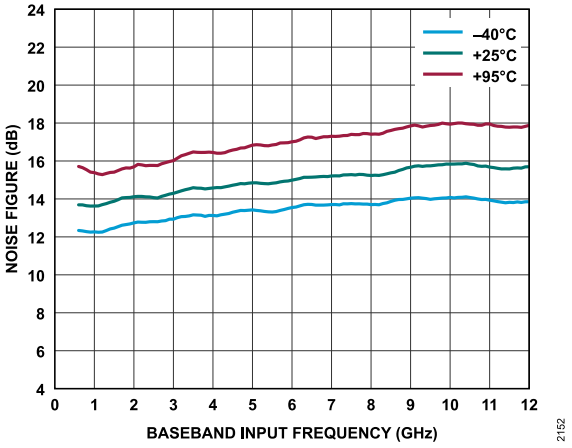


Figure 154. Noise Figure vs. Baseband Input Frequency at Various Temperatures and High Frequency External Hybrid

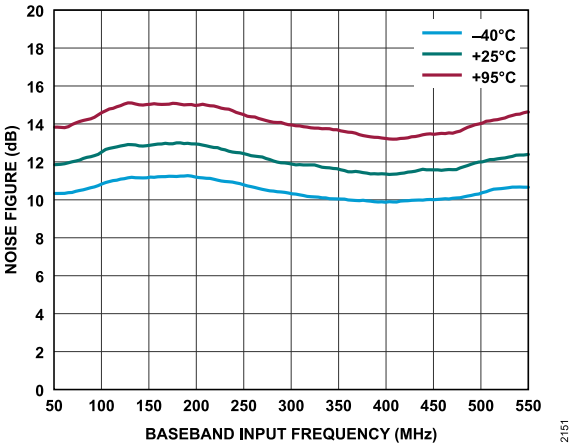


Figure 153. Noise Figure vs. Baseband Input Frequency at Various Temperatures and Low Frequency External Hybrid

TYPICAL PERFORMANCE CHARACTERISTICS

Output P1dB

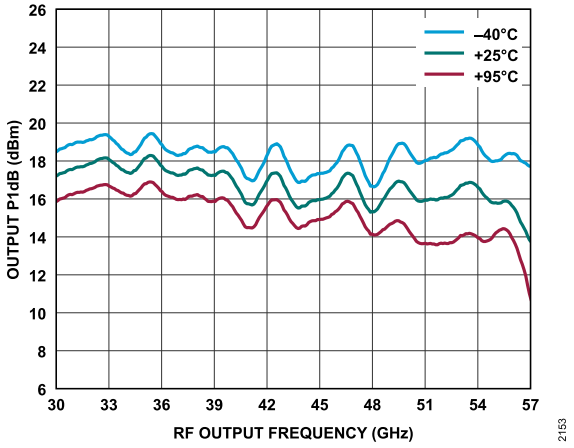


Figure 155. Output P1dB vs. RF Output Frequency at Various Temperatures

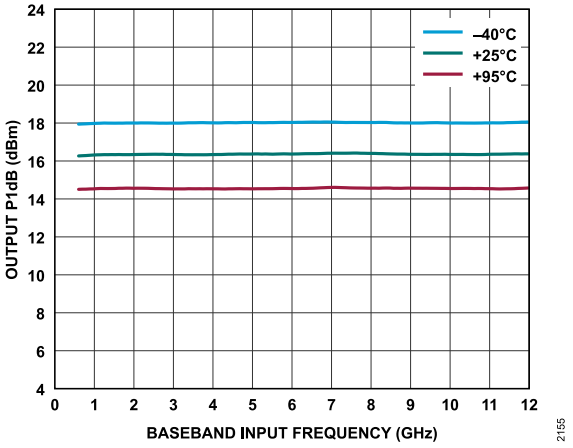


Figure 157. Output P1dB vs. Baseband Input Frequency at Various Temperatures and High Frequency External Hybrid

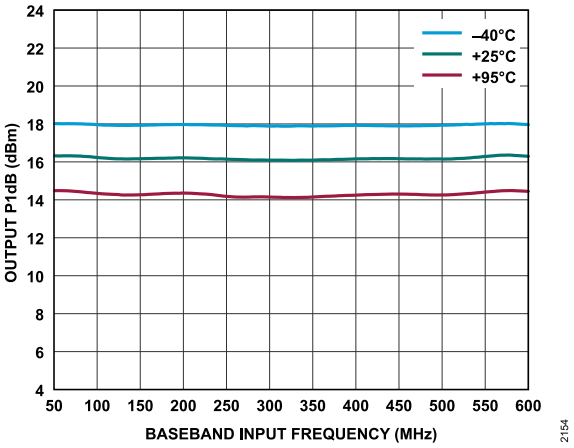


Figure 156. Output P1dB vs. Baseband Input Frequency at Various Temperatures and Low Frequency External Hybrid

TYPICAL PERFORMANCE CHARACTERISTICS

I/Q BASEBAND MODE, BB_IX AND BB_QX, LOW BAND

All measurements use BB_IP, BB_IN, BB_QP, and BB_QN as inputs and RF_OUT as an output with the RF high-band settings. VDD_DRV = 3V, all other supply voltages = 1.8V, and T_C = 25°C, unless otherwise noted.

Measurements performed with P_{BB} = −20dBm, P_{LO} = 0dBm, f_{BB} = 100MHz, f_{LO} = 48.9GHz (upper sideband), maximum gain, RF LPF setting = 0x00 (highest cutoff), and V_{ICM} = 1V, unless otherwise noted.
See Table 19 for the digital common-mode voltage settings.

Conversion Gain

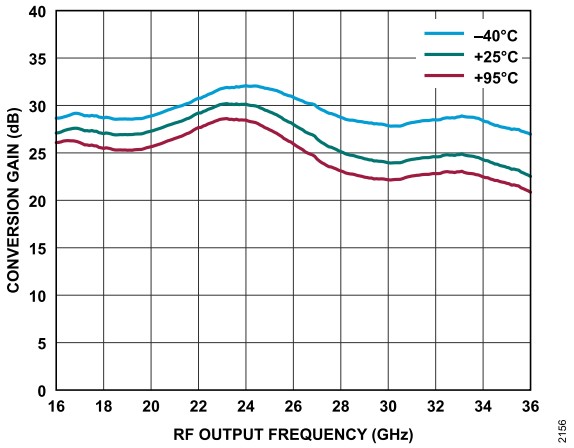


Figure 158. Conversion Gain vs. RF Output Frequency at Various Temperatures, WIdeband Low LO Filter

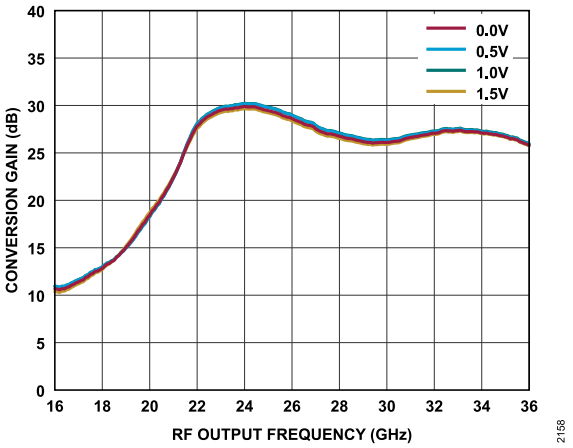


Figure 160. Conversion Gain vs. RF Output Frequency at Common-Mode Voltages, Wideband Low LO Filter

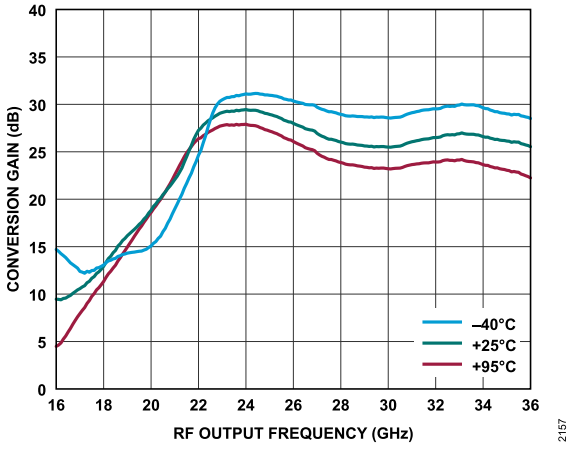


Figure 159. Conversion Gain vs. RF Output Frequency at Various Temperatures, Wideband High LO Filter

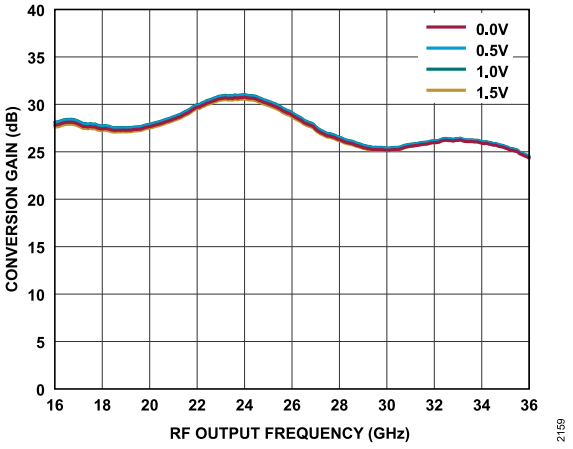


Figure 161. Conversion Gain vs. RF Output Frequency at Common-Mode Voltages, Wideband High LO Filter

TYPICAL PERFORMANCE CHARACTERISTICS

Sideband Rejection

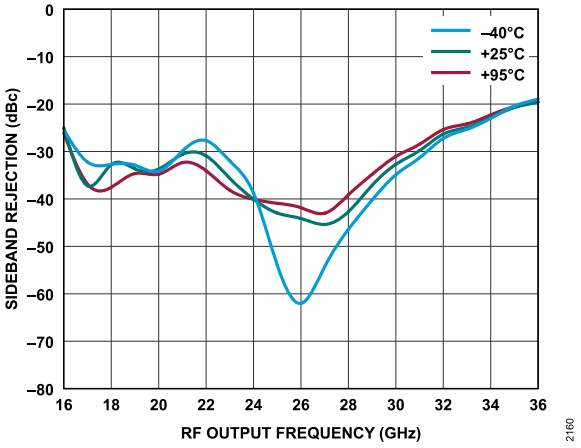


Figure 162. Sideband Rejection vs. RF Output Frequency at Various Temperatures with No Calibration, No RF Filters, and Wideband Low LO Filter

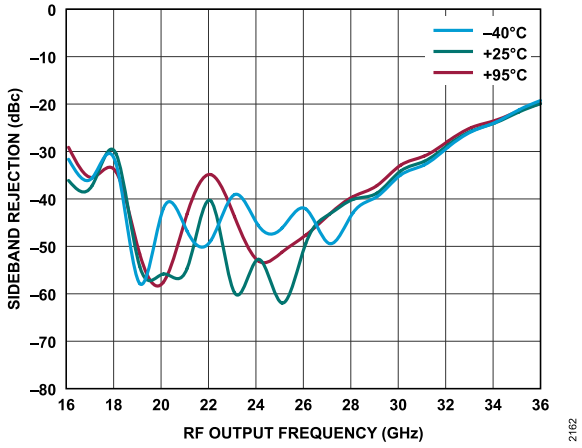


Figure 164. Sideband Rejection vs. RF Output Frequency at Various Temperatures with Optimization at 25°C, No RF Filters, and Wideband Low LO Filter

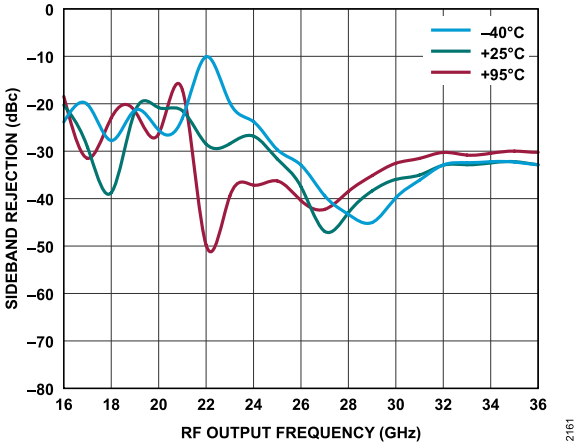


Figure 163. Sideband Rejection vs. RF Output Frequency at Various Temperatures with No Calibration, No RF Filters, and Wideband High LO Filter

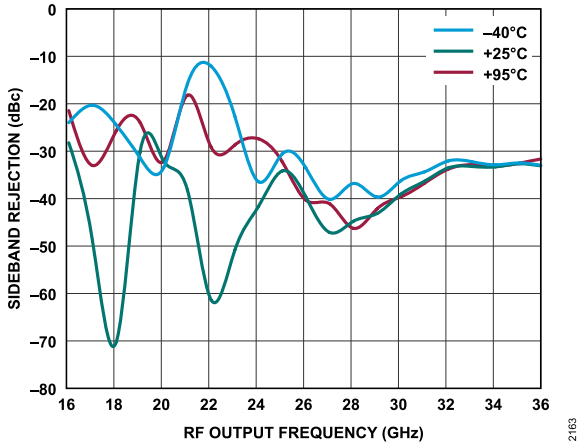


Figure 165. Sideband Rejection vs. RF Output Frequency at Various Temperatures with Optimization at 25°C, No RF Filters, and Wideband High LO Filter

TYPICAL PERFORMANCE CHARACTERISTICS

Output IP3

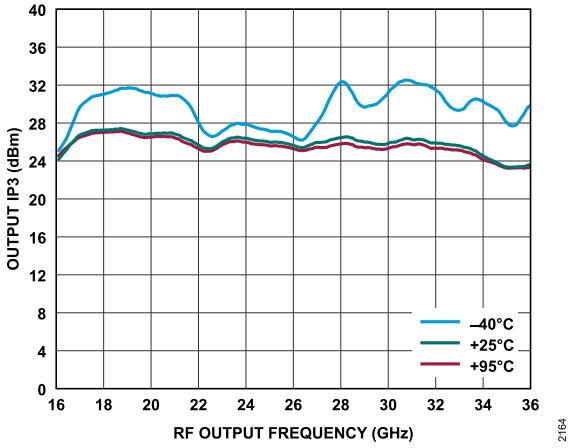


Figure 166. Output IP3 vs. RF Output Frequency at Various Temperatures, Wideband Low LO Filter

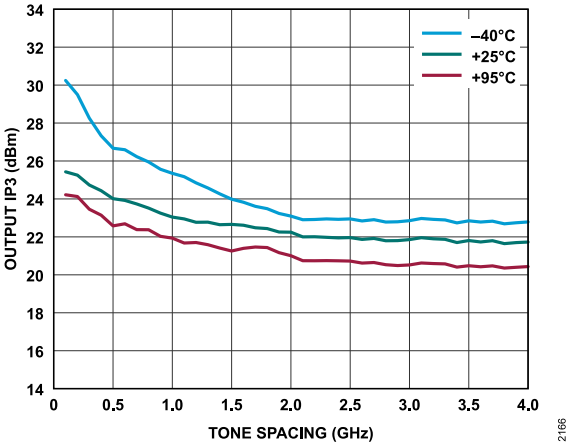


Figure 168. Output IP3 vs. Tone Spacing at Various Temperatures, Wideband Low LO Filter

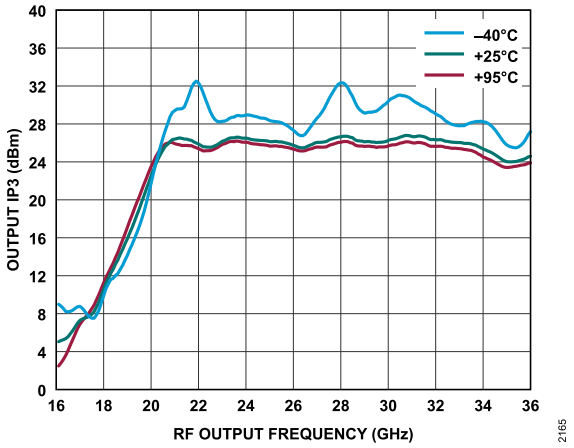


Figure 167. Output IP3 vs. RF Output Frequency at Various Temperatures, Wideband High LO Filter

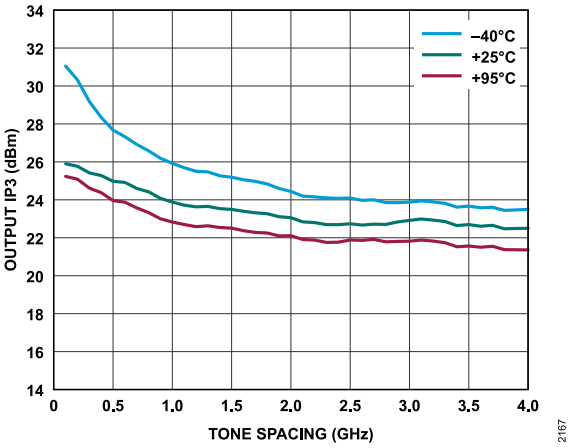


Figure 169. Output IP3 vs. Tone Spacing at Various Temperatures, Wideband High LO Filter

TYPICAL PERFORMANCE CHARACTERISTICS

Noise Figure

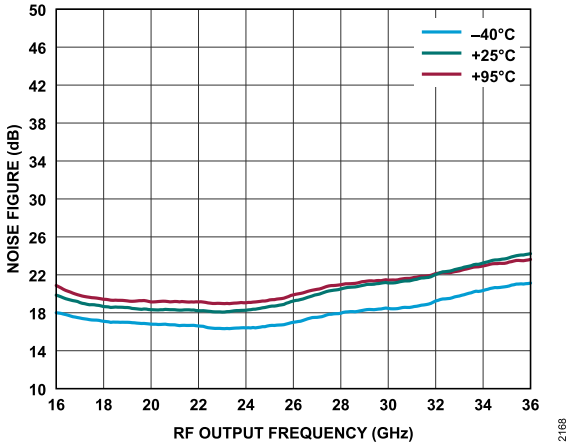


Figure 170. Noise Figure vs. RF Output Frequency at Various Temperatures, Wideband Low LO Filter

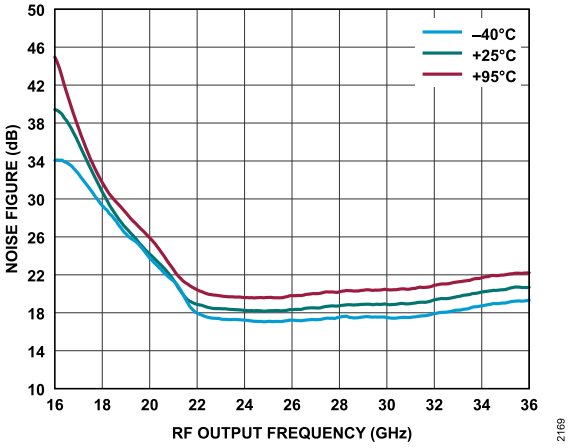


Figure 171. Noise Figure vs. RF Output Frequency at Various Temperatures, Wideband High LO Filter

TYPICAL PERFORMANCE CHARACTERISTICS

Output P1dB

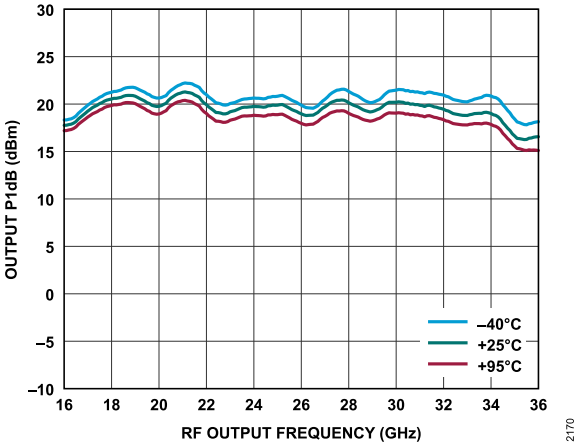


Figure 172. Output P1dB vs. RF Output Frequency at Various Temperatures, Wideband Low LO Filter

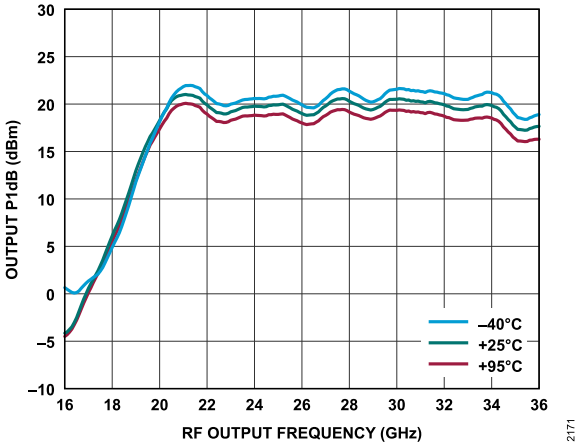


Figure 173. Output P1dB vs. RF Output Frequency at Various Temperatures, Wideband High LO Filter

TYPICAL PERFORMANCE CHARACTERISTICS

RETURN LOSS

The VDD_DRV = 3V, all other supply voltages = 1.8V, and T_C = 25°C, unless otherwise noted.

All measurements taken with input power set to small signal level, maximum gain, RF LPF setting = 0x00 (highest cutoff), and RF HPF setting = 0x3F (lowest cutoff).

Probe measurements, where applicable, were performed by probing the trace terminated out of the device.

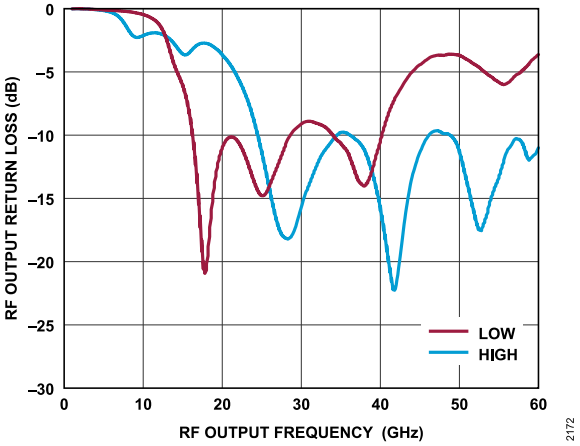


Figure 174. RF Output Return Loss vs. RF Output Frequency at Various RF Bands

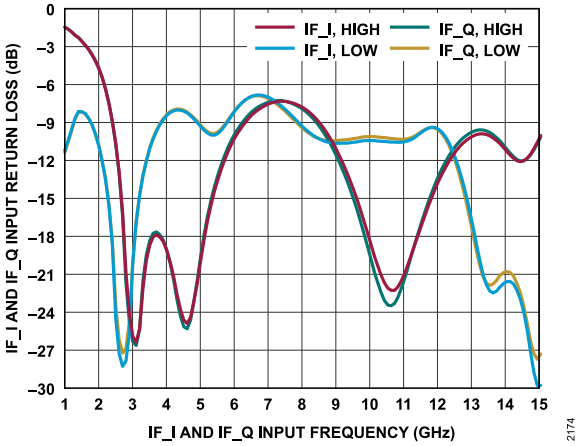


Figure 176. IF_I and IF_Q Input Return Loss vs. IF_I and IF_Q Input Frequency at Various Complex IF Frequency Modes

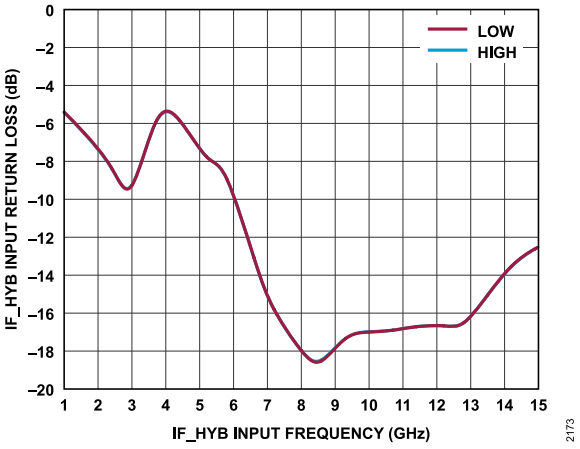


Figure 175. IF_HYB Input Return Loss vs. IF_HYB Input Frequency at Various RF Bands

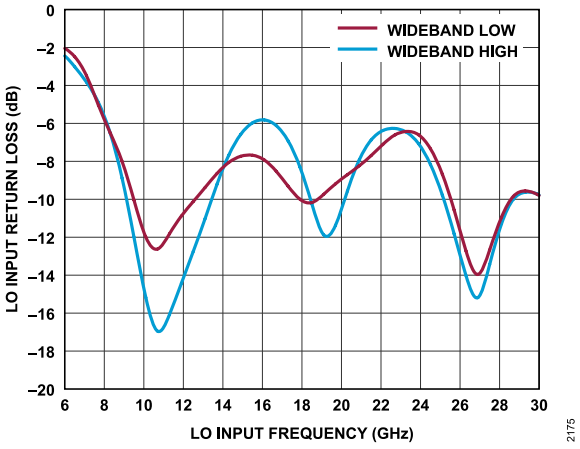


Figure 177. LO Input Return Loss vs. LO Input Frequency at Various Wideband LO Filters

TYPICAL PERFORMANCE CHARACTERISTICS

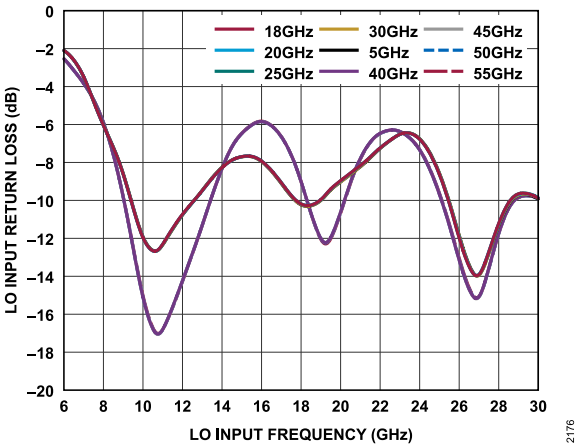


Figure 178. LO Input Return Loss vs. LO Input Frequency at Various Narrow-Band LO Filters

THEORY OF OPERATION

CHIP OVERVIEW

The ADMV1355 is a highly integrated microwave upconverter designed for wideband radio systems operating across a broad RF frequency range of 17.7GHz to 55GHz. The device supports single-ended IF and complex IF inputs up to 12GHz, enabling seamless integration with modern high-speed data converters and extending their effective frequency coverage into the millimeter-wave spectrum.

The chip incorporates a fully configurable architecture that includes an I/Q mixer, a LO signal chain, two RF signal chains, an IF signal chain, and baseband I/Q signal chain, all of which are configurable via a simple SPI. This level of integration minimizes the external component count while offering maximum design flexibility.

With its compact, 6mm × 6.5mm footprint, wideband capabilities, and configurable signal chains, the ADMV1355 is ideally suited for next generation, high data-rate systems requiring low size, weight, and power (SWaP) without compromising on system performance.

POWER-UP SEQUENCE

To power up and initialize the ADMV1355, take the following steps and refer to the Timing Diagrams Overview section and Figure 180 for more information:

1. Ensure that all digital logic inputs are logic level low.
2. Power on all supply voltages simultaneously, with a rise time of 1ms or longer.
3. Once the supplies are stable, set $\overline{\text{RST}}$ to logic level high.
4. Program the nonvolatile memory (NVM) load instructions.
5. Program the necessary registers for the intended chip operation.
6. Set CEN to logic level high.

POWER-DOWN SEQUENCE

There are three possible power-down options available for the ADMV1355. One power-down option removes all power from the chip, and the other two power-down options disable the chip, causing it to enter low power mode.

Full Power-Down

To fully power down the chip, take the following steps and refer to Figure 183 for more information:

1. Set CEN to logic level low.
2. Set all other logic inputs to logic level low.
3. Power off all supply voltages.

Chip Disable with CEN

To disable the chip and enter low power mode while the supply voltages are still powered on, bring CEN to logic level low. Bringing CEN to logic level low causes the chip to power off most of the RF circuits within the chip. Refer to Figure 182 for more information.

Chip Disable with SPI

Another option for disabling the chip and entering low power mode while the supply voltages are still powered on is to set Register 0x13E, Bit 0 to 1.

THEORY OF OPERATION

SPI

The ADMV1355 utilizes the SPI for communication to configure the chip settings. The SPI can be implemented in either 3-wire or 4-wire configurations, supports 1.8V logic levels, and SCLK frequencies up to 100MHz.

The SPI consists of digital inputs and outputs. CHIP_ADD0, CHIP_ADD1, SCLK, and $\overline{CS}$ are the digital inputs. SDIO is bidirectional and can be an input or output, depending upon the type of SPI operation being performed, and SDO is a digital output that remains in a high impedance state unless a read operation is being performed. $\overline{CS}$ is an active low digital input and must be asserted low during a SPI instruction. Be sure to deasserted $\overline{CS}$ at the end of a SPI instruction.

The chip address inputs, CHIP_ADD0 and CHIP_ADD1, can be used in multichip systems to assign an address to a particular chip. This feature allows up to four chips to share SCLK, SDIO, SDO, and $\overline{CS}$ connections. To set a chip address input to 0, ground the ball or add a 0Ω pull-down resistor. To set a chip address input to 1, leave it floating, and the internal 15kΩ resistor will set it to a logic level high. The assigned chip address modifies the SPI Communications Frame Bits[21:20].

For single SPI instructions, the communications frame is 24-bits wide and consists of a 16-bit header and 8 bits of data. The header contains a R/W bit, a broadcast (BR) bit, two chip address bits, and 12 register address bits. Both the header and data are organized MSB first and must be shifted in on SDIO with the chip sampling the logic level on the rising edge of SCLK. See Figure 179 for the SPI communications frame.

Set the R/W bit to 0 for a write operation and set the R/W to 1 for a read operation. Set the BR bit to 0 for single chip SPI instructions and set this bit to 1 to have all chips, regardless of their chip address, respond to a SPI instruction. For read operations, the BR bit must only be set to 0.

For a read operation when using a 3-wire SPI, the SDIO changes from an input to an output after the last header SCLK rising edge. The data is then shifted out on SDIO, with the logic level changing on the falling edge of SCLK, so that it can be sampled on the next rising edge of SCLK. When $\overline{CS}$ is deasserted, SDIO changes back to a digital input.

For a read operation when using a 4-wire SPI, the SDO transitions from a high impedance state to an active output, after the last header SCLK rising edge. The data is then shifted out on SDO, with the logic level changing on the falling edge of SCLK, so that it can be sampled on the next rising edge of SCLK. When $\overline{CS}$ is deasserted, SDO returns to a high impedance state.

The ADMV1355 supports SPI streaming that minimizes the SPI instruction time. During a SPI streaming instruction, $\overline{CS}$ is asserted low, a single 16-bit header instruction is given, followed by multiple bytes of data, and then $\overline{CS}$ is deasserted to end the instruction. Sequential register addresses are assumed in ascending or descending order based on how Register 0x000, Bit 5 and Bit 2 are set. Note that the default order is descending addresses.

If $\overline{CS}$ is deasserted during any header portion of a SPI instruction, the operation is ignored. If $\overline{CS}$ is deasserted during a data portion of a SPI instruction, then that data is ignored. For SPI streaming operations, any complete bytes (8 bits) of data are accepted by the chip, but a partial byte is ignored.

See the Timing Diagrams Overview section, the Power-Up and Apply the Digital Inputs section, the Initialization SPI Instructions section, the Chip Enable and Operation section, the Chip Disable and Reset section, and the Chip Disable and Power-Down section for additional timing information and refer to the ADI-SPI, Serial Control Interface Standard (Rev 1.0) for more information on SPI and communications protocol.

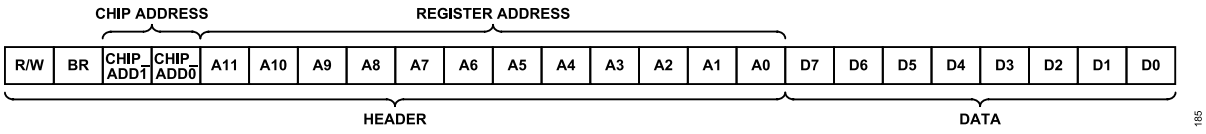


Figure 179. Single SPI Frame Timing Diagram

THEORY OF OPERATION

TIMING DIAGRAMS OVERVIEW

The timing diagrams shown in Figure 180, Figure 181, Figure 182, and Figure 183 help with visualizing the various programming and power sequences of operation for the ADMV1355. These timing diagrams utilize the timing specifications detailed in Table 8.

Contained within this guidance are limitations to prevent possible damage to the ADMV1355, such as keeping the digital inputs low during power up and removing the digital inputs before or at the same time as power down. Additionally, the timing diagrams contain best practices for operation, such as programming the necessary SPI instructions prior to enabling the RF portions of the chip using the CEN input.

See the Power-Up and Apply the Digital Inputs section, the Initialization SPI Instructions section, the Chip Enable and Operation section, the Chip Disable and Reset section, and the Chip Disable and Power-Down section for additional details regarding these timing diagrams.

Power-Up and Apply the Digital Inputs

The power-up and initialization timing diagram (see Figure 180) shows the power supplies rising by t_1, starting from the start time, t_{START}. After the power supply voltages have been brought to 90% of their nominal values, valid digital inputs can be applied after waiting a minimum time of t_2 at $t_{DIGITAL}$. To prevent possible damage to the chip, do not apply digital inputs before $t_{DIGITAL}$.

Generally, at $t_{DIGITAL}$, the $\overline{RST}$ and $\overline{CS}$ inputs go high together. If applicable, the CHIP_ADD0 and CHIP_ADD1 are also set at this time in preparation for the SPI instructions. Wait a minimum of t_3 to allow the chip to reset before beginning the SPI instructions at the initialization time, $t_{INITIALIZE}$.

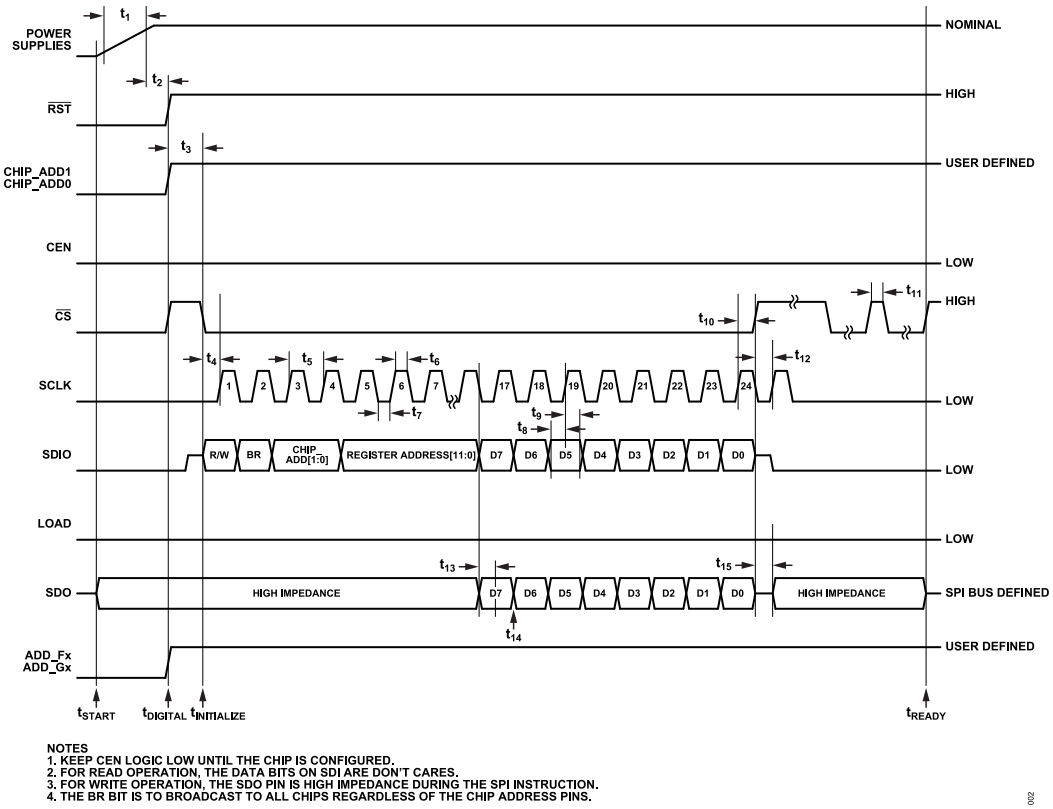


Figure 180. Power-Up and Initialization Timing Diagram

THEORY OF OPERATION

Initialization SPI Instructions

Starting at $t_{INITIALIZE}$ (see Figure 180), configure the chip by using the SPI instructions for its intended operation. Give all the necessary SPI instructions to configure the chip, looping from $t_{INITIALIZE}$ to the ready time, t_{READY} for each instruction. Keep the CEN input low during the initialization SPI instructions, and complete the initialization at t_{READY}.

Chip Enable and Operation

After all the initialization SPI instructions have been completed, wait a minimum of t_{16} to ensure that the digital logic has processed the instructions prior to setting the CEN input high at $t_{OPERATIONAL}$ to enable chip operation. At $t_{OPERATIONAL}$, the RF portions of the chip are enabled. See Figure 181 for more information.

During chip operation, any necessary SPI instructions can be given, along with the LOAD input toggles, and any changes to the ADD_Fx and ADD_Gx inputs. Continue operating, looping from $t_{OPERATIONAL}$ to $t_{CONTINUE}$ until it is desired to either disable the chip, reset the chip, or power down the chip.

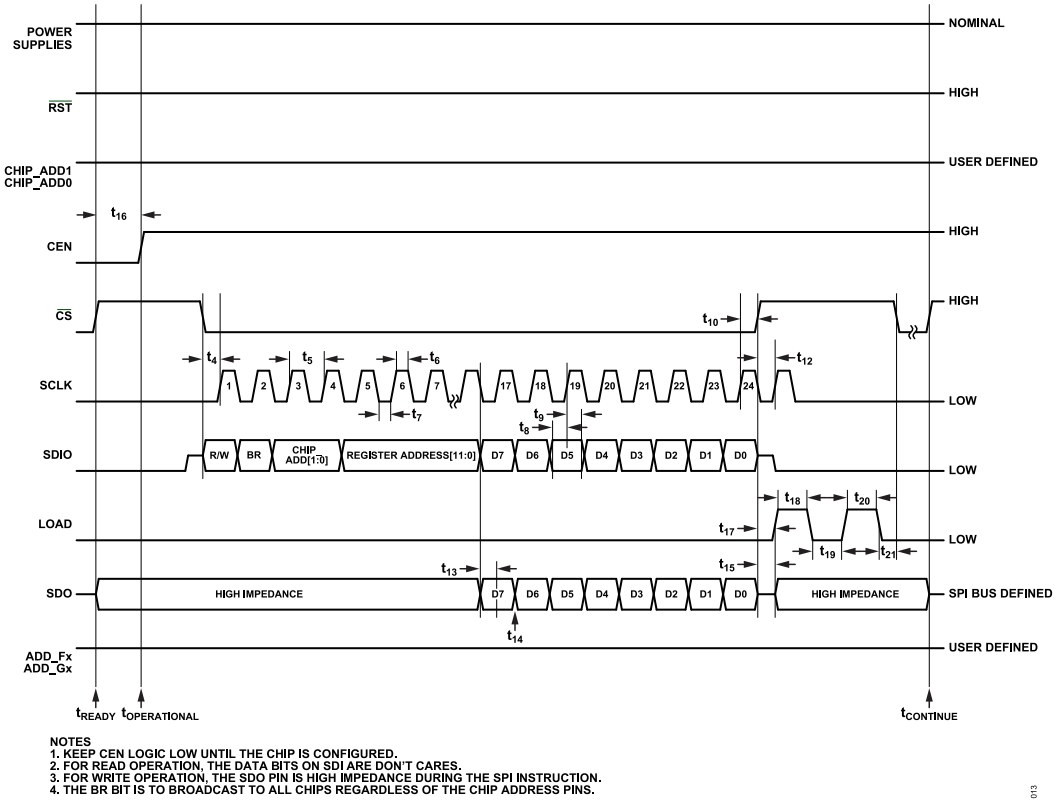


Figure 181. Operational Timing Diagram

THEORY OF OPERATION

Chip Disable and Reset

When it is desired to either disable the chip or reset the chip, follow Figure 182 starting at $t_{CONTINUE}$. Wait a minimum of t_{22} from the last SPI instruction before disabling the chip by setting the CEN input low at $t_{DISABLE}$.

After setting the CEN input low, wait a minimum of t_{23} to allow the RF portions of the chip to power down. The $\overline{RST}$ input can then be set low for a minimum of t_{24} before the $\overline{RST}$ input can be set high again. Wait a minimum of t_3 before looping back to $t_{INITIALIZE}$, which is shown in Figure 180.

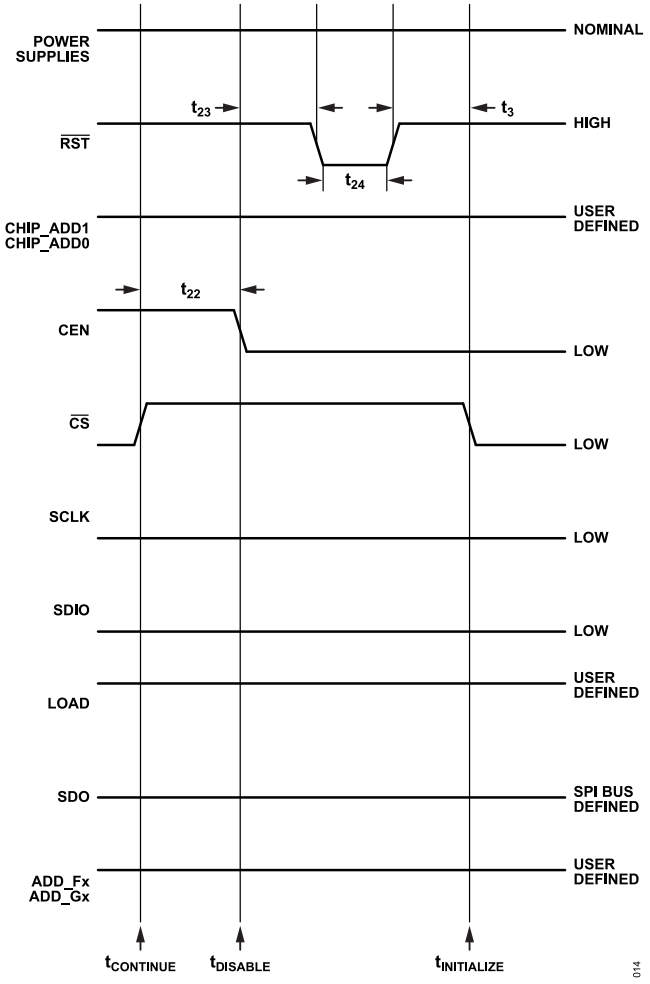


Figure 182. Chip Disable and Reset Timing Diagram

Chip Disable and Power-Down

When it is desired to disable and power down the chip, follow Figure 183 starting at $t_{CONTINUE}$. Wait a minimum of t_{22} from the last SPI instruction before disabling the chip by setting the CEN input low at $t_{DISABLE}$.

After setting the CEN input low, wait a minimum of t_{25} to allow the RF portions of the chip to power down before starting the chip power down at $t_{POWER-DOWN}$. At $t_{POWER-DOWN}$, all other logic inputs must be set low with a fall time of t_{26}, and the power supply voltages can be turned off with a fall time of t_{27}. Ideally, the logic inputs are removed prior to the power supply ramp down, but they can occur simultaneously provided that the logic inputs fall time does not exceed the t_{26} maximum time. Note that the time units for t_{26} are in microseconds, and the time units for t_{27} are milliseconds.

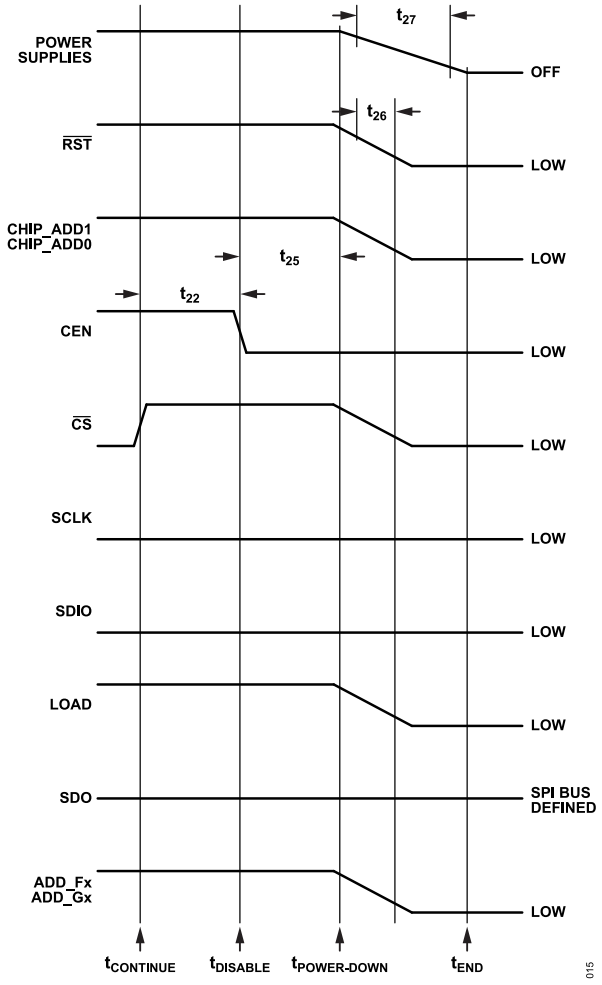


Figure 183. Chip Disable and Power-Down Timing Diagram

THEORY OF OPERATION

NVM

The ADMV1355 contains a simple NVM that is used to store factory calibration values to minimize part to part variation. The values in the NVM set the chip bias current, trim the internal analog-to-digital converter (ADC), and trim the internal temperature sensor. At chip power-up, it is recommended to ensure that the NVM has loaded its values into the correct shadow registers. The NVM is static and can not be modified by the user.

NVM Health Check

To confirm the NVM values have loaded, use the following NVM health check instructions:

1. Shadow Register 0x033 by doing the following:
   - Set Register 0x07B to 0x33 value.
   - Read Register 0x07B, it should return 0x33.
   - Read Register 0x07C, it should return a nonzero value.
2. Shadow Register 0x034, by doing the following:
   - Set Register 0x07B to 0x34 value.
   - Read Register 0x07B, it should return 0x34.
   - Read Register 0x07C, it should return a nonzero value.
3. Shadow Register 0x037 by doing the following:
   - Set Register 0x07B to 0x37 value.
   - Read Register 0x07B, it should return 0x37.
   - Read Register 0x07C, it should return a nonzero value.
4. Shadow Register 0x038 by doing the following:
   - Set Register 0x07B to 0x38 value.
   - Read Register 0x07B, it should return 0x38.
   - Read Register 0x07C, it should return a nonzero value.

If any of the return values are zero, follow the instructions detailed in the NVM Load Instructions section.

NVM Load Instructions

If any of the return values from Register 0x07C are zero, run the following NVM load instructions:

1. Set Register 0x078 to 0x08 value.
2. Pause 1ms.
3. Set Register 0x07E to 0x40 value.
4. Pause 1ms.
5. Set Register 0x07E to 0x54 value.
6. Pause 1ms.
7. Set Register 0x078 to 0x09 value.

DIGITAL OVERVIEW

The ADMV1355 contains advanced digital logic that allows for various methods of configuring each circuit block within the chip. These methods include simple register configurations, a synchronous LOAD feature, LUTs, logic state machines, parallel input logic pointers, and general-purpose logic outputs.

The digital logic can be partitioned into two subsections, one for frequency control (filters) and the other for gain control (attenuators). See Figure 184 and Figure 185 for representative diagrams for each subsection. When reviewing these diagrams, it may be helpful to follow from right to left, starting from the items being controlled, then deciding the input control method.

For the frequency control subsection, the most simple way to configure the filters and GPO_Fx logic outputs is by using Register 0x800 to Register 0x80C. Register 0x2A0 is a bypass register that allows setting the RF chain LPF value, and this register gives more resolution than the LPF value in Register 0x80B. Similarly, Register 0x2A1 is the bypass register for the RF chain HPF value, and this register gives more resolution than the HPF value in Register 0x80B.

For the gain control subsection, the most simple way to configure the attenuators and GPO_Gx logic outputs is by using Register 0x28B and Register 0x28C. Register 0x600 and Register 0x601 can also be used when using the LOAD feature is required.

THEORY OF OPERATION

Digital Diagrams

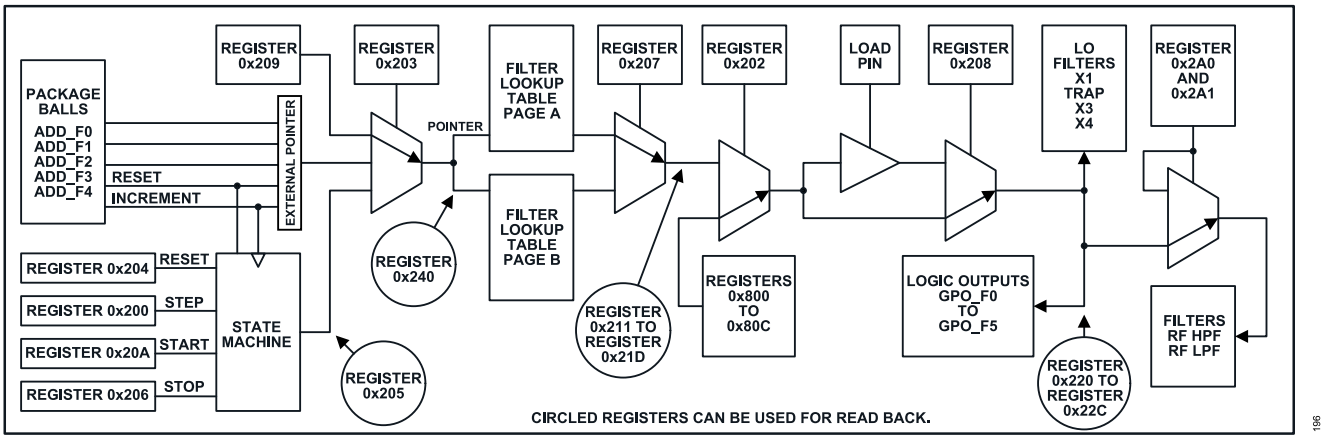


Figure 184. Filter Diagram

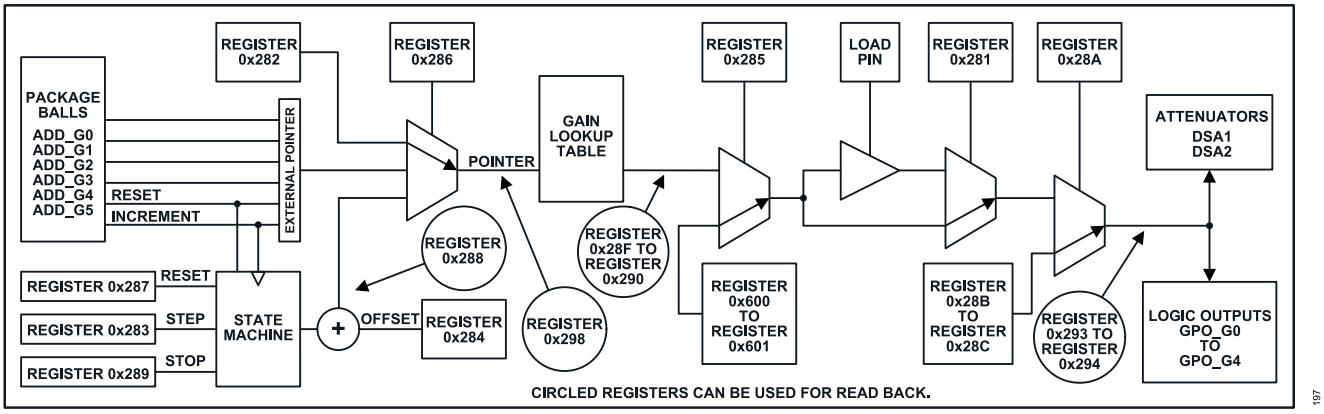


Figure 185. Gain Diagram

SYNCHRONOUS LOAD FEATURE

The ADMV1355 includes a synchronous load feature that allows the filter settings and gain settings to be applied at specific trigger rising edge events on the LOAD ball. See Figure 181 for the LOAD feature timing. To enable the load feature for the filter settings, set Register 0x208 to 1. To enable the load feature for the gain settings, set Register 0x281 to 1.

FILTER LUT

The digital logic contains a filter LUT that can be used to determine the state of the LO tunable filters, RF tunable filters, and GPO_F logic outputs. This LUT can be beneficial for fast frequency hopping applications, where it may be necessary to quickly change chip configuration states.

To use the LUT, set Register 0x202 to 1 and setup the LUT from Register 0x900 to Register 0xC3F.

The LUT contains two pages that have 32 indices each, or 64 total. To select Page A, set Register 0x207 to 0, and to select Page B, set Register 0x207 to 1.

There are three potential sources for the LUT index (pointer), as determined by Register 0x203. The pointer can be set by using the parallel logic input ADD_F balls, by using Register 0x209, or by using the internal state machine. Set Register 0x203 to value 0 to use ADD_F balls as the pointer, set Register 0x203 to value 1 to use Register 0x209 as the pointer, and set Register 0x203 to value 2 to use the internal state machine.

Regardless of the LUT pointer source, use Register 0x240 to read back the pointer value.

The LUT output values can be read from Register 0x211 to Register 0x21D. The values in these registers represent the filter values prior to the mux controlled by Register 0x202 and the LOAD feature.

THEORY OF OPERATION

Filter State Machine

The internal state machine can be used to sequence through many states, using the ADD_F4 input to advance, and the ADD_F3 to reset. It has several input parameters from the SPI, such as start value, stop value, step size, wrap setting, and reset.

At power up, the state machine output is zero, and it can be reset to zero using either the ADD_F3 ball or Register 0x204. Set ADD_F3 to logic high to hold the state machine in reset, and then bring ADD_F3 to logic low to re-enter normal operation. Alternatively, set Register 0x204 to 0 to hold the state machine in reset and then set this register back to 1 to re-enter normal operation.

To ensure that the state machine is well behaved, it is recommended to set the stop value greater than the start value. The step size is an 8-bit twos complement value, with a range of −128 to +127, where −128 is represented by 0x80, +127 is represented by 0x7F, and −1 is represented by 0xFF. A step size of zero is invalid.

Use Register 0x205 to read back the current value of the state machine.

When the wrap setting is disabled, incremental sequencing starts at zero, incrementing by the step size. If the state machine has reached the stop value, the next state is the start value. If the step size increments to more than the stop value, the start value is used.

When the wrap setting is disabled, decremental sequencing starts at zero, then decrementing by the step size. If the state machine has reached zero, the next state is the stop value. If the step size decrements to less than zero, the stop value is used. The start value is ignored during this sequence.

When the wrap setting is enabled, incremental sequencing starts at zero, incrementing by the step size. If the step size increments to more than the stop value, the sequence rolls over and continues the remaining count from zero. The start value is ignored during this sequence.

When the wrap setting is enabled, decremental sequencing starts at zero, decrementing by the step size. If the step size decrements to less than zero, the sequence rolls over and continues the remaining count from the stop value. The start value is ignored during this sequence.

Refer to Table 14 for the applicable registers and example state machine behavior. The sequences shown in Table 14 continue indefinitely for each rising edge on ADD_F4.

Table 14. Filter State Machine Example Behavior

Example	Step[1]	Start[2]	Stop[3]	Wrap[4]	State Machine Sequence
1	+1	3	6	0	0, 1, 2, 3, 4, 5, 6, 3, 4, 5, 6, 3, 4, 5, 6...
2	+2	3	6	0	0, 2, 4, 6, 3, 5, 3, 5, 3, 5, 3, 5, 3, 5, 3...
3	+3	3	6	0	0, 3, 6, 3, 6, 3, 6, 3, 6, 3, 6, 3, 6, 3, 6...
4	+4	3	6	0	0, 4, 3, 3, 3, 3, 3, 3, 3, 3, 3, 3, 3, 3, 3...
5	−1	3	6	0	0, 6, 5, 4, 3, 2, 1, 0, 6, 5, 4, 3, 2, 1, 0...
6	−2	3	6	0	0, 6, 4, 2, 0, 6, 4, 2, 0, 6, 4, 2, 0, 6, 4...
7	−3	3	6	0	0, 6, 3, 0, 6, 3, 0, 6, 3, 0, 6, 3, 0, 6, 3...
8	−4	3	6	0	0, 6, 2, 6, 2, 6, 2, 6, 2, 6, 2, 6, 2, 6, 2...
9	+1	3	6	1	0, 1, 2, 3, 4, 5, 6, 0, 1, 2, 3, 4, 5, 6, 0...
10	+2	3	6	1	0, 2, 4, 6, 1, 3, 5, 0, 2, 4, 6, 1, 3, 5, 0...
11	+3	3	6	1	0, 3, 6, 2, 5, 1, 4, 0, 3, 6, 2, 5, 1, 4, 0...
12	+4	3	6	1	0, 4, 1, 5, 2, 6, 3, 0, 4, 1, 5, 2, 6, 3, 0...
13	−1	3	6	1	0, 6, 5, 4, 3, 2, 1, 0, 6, 5, 4, 3, 2, 1, 0...
14	−2	3	6	1	0, 5, 3, 1, 6, 4, 2, 0, 5, 3, 1, 6, 4, 2, 0...
15	−3	3	6	1	0, 4, 1, 5, 2, 6, 3, 0, 4, 1, 5, 2, 6, 3, 0...
16	−4	3	6	1	0, 3, 6, 2, 5, 1, 4, 0, 3, 6, 2, 5, 1, 4, 0...

[1] The step size is determined by Register 0x200, Bits[7:0].

[2] The start is determined by Register 0x20A, Bits[4:0].

[3] The stop is determined by Register 0x206, Bits[4:0].

[4] The wrap setting is determined by Register 0x20A, Bit 5.

THEORY OF OPERATION

GAIN LUT

The digital logic contains a gain LUT with 67 indices that can be used to determine the state of the DSAs and the GPO_G logic outputs. This LUT can be beneficial for fast frequency hopping applications, where it may be necessary to quickly change the chip configuration states.

To use the LUT, set Register 0x285 to 1 and setup the LUT from Register 0xE00 to Register 0xE85.

There are three potential sources for the LUT index (pointer), as determined by Register 0x286. The pointer can be set by using the parallel logic input ADD_G balls, by using Register 0x282, or by using the internal state machine. Set Register 0x286 to value 0 to use ADD_G balls as the pointer, set Register 0x286 to value 1 to use Register 0x282 as the pointer, and set Register 0x286 to value 2 to use the internal state machine.

Regardless of LUT pointer source, use Register 0x298 to read back the pointer value.

The LUT output values can be read from Register 0x28F to Register 0x290. The values in these registers represent the DSA values prior to the mux controlled by Register 0x285 and the LOAD feature.

Gain State Machine

The internal state machine can be used to sequence through many states, using the ADD_G5 input to advance and the ADD_G4 input to reset. It has several input parameters from the SPI, such as offset value, stop value, step size, and reset.

At power up, the state machine output is zero, and it can be reset to zero using either the ADD_G4 ball or Register 0x287. Set ADD_G4 to logic high to hold the state machine in reset and then bring it to logic low to re-enter normal operation. Alternatively, set Register 0x287 to 0 to hold the state machine in reset and then set it back to 1 to re-enter normal operation.

The step size is a 8-bit twos complement value, with a range of −128 to +127, where −128 is represented by 0x80, +127 is represented by 0x7F, and −1 is represented by 0xFF. A step size of zero is invalid.

The state machine increments or decrements on each rising edge of ADD_G5 based upon the step size value programmed. The state machine is always bound by zero and the stop value. Once the machine has reached one of these bounds, it will remain there. When the state machine value is equal to the stop value, changing the step size from a positive number to a negative number allows the state machine to be decremented back to zero.

The offset value is a 8-bit twos complement value, with a range of −128 to +127, where −128 is represented by 0x80, +127 is represented by 0x7F, and −1 is represented by 0xFF.

The pointer value is equal to the state machine value plus the offset value. Use Register 0x288 to read back the current value of the pointer.

Both the state machine value and the pointer are bound by zero and the stop value. If the state machine is left at a particular value, and the stop value or offset value is changed, the pointer may update if it is within these bounds. The minimum pointer value is bound by the offset value or zero, whichever one is greater.

Refer to Table 15 for the applicable registers and example state machine behavior. The sequences shown in Table 15 do not continue indefinitely for each rising edge on ADD_G5. The state machine must be reset, the step size changed, or the stop value changed to allow additional sequencing after it has reached the end of a sequence.

Table 15. Gain State Machine Example Behavior

Example	Step[1]	Offset[2]	Stop[3]	State Machine Sequence
1	+1	0	6	0, 1, 2, 3, 4, 5, 6
2	+2	0	6	0, 2, 4, 6
3	+4	0	6	0, 4, 6
4	+6	0	6	0, 6
5	+1	1	6	1, 2, 3, 4, 5, 6
6	+2	1	6	1, 3, 5, 6
7	+3	1	6	1, 4, 6
8	−1	0	6	6, 5, 4, 3, 2, 1, 0

[1] The step size is determined by Register 0x283, Bits[7:0].

[2] The offset is determined by Register 0x284, Bits[7:0].

[3] The stop is determined by Register 0x289, Bits[6:0].

THEORY OF OPERATION

GENERAL-PURPOSE OUTPUTS

The ADMV1355 includes 11 general-purpose outputs that can be used to set logic levels of other components within a system, such as standalone tunable filters or standalone DSAs. These outputs support 1.8V logic levels and can be defined by either the SPI or by the LUTs.

Before using any of the general-purpose outputs, it is necessary to set the output enable bit to 1 for that output by using Register 0x780 and Register 0x781. The output state, logic high or logic low, is then determined by the values programmed into Register 0x601 and Register 0x803. Refer to Table 16 for more details.

Table 16. GPO Registers

	Output Enable		Output State	
Output	Register	Bit	Register	Bit
GPO_F0	0x780	0	0x803	0
GPO_F1	0x780	1	0x803	1
GPO_F2	0x780	2	0x803	2
GPO_F3	0x780	3	0x803	3
GPO_F4	0x780	4	0x803	4
GPO_F5	0x780	5	0x803	5
GPO_G0	0x780	6	0x601	0
GPO_G1	0x780	7	0x601	1
GPO_G2	0x781	0	0x601	2
GPO_G3	0x781	1	0x601	3
GPO_G4	0x781	2	0x601	4

RF CONNECTIONS

The RF connections of the ADMV1355 are considered DC-coupled. If a DC voltage is present on the connections from other components within the system, it is recommended to place DC blocking capacitors in series with these pins. The DC blocking capacitors must be selected based on the operating frequency of the filter. Generally, a value greater than 100pF is sufficient to minimize insertion loss at the lower frequencies of operation. At higher frequencies of operation, it may be necessary to consider the parasitic elements of the selected capacitor. Figure 186 shows a general model of a capacitor with the parasitic elements. The parasitic series inductance (L_{ESL}) is typically of most concern given that its impedance can become dominant at frequencies of more than 10GHz. The other parasitic elements, including the leakage resistance (R_L), dielectric absorption resistance (R_{DA}), dielectric absorption capacitance (C_{DA}), and electrical series resistance (R_{ESR}) are less critical elements for consideration but are shown here for completeness.

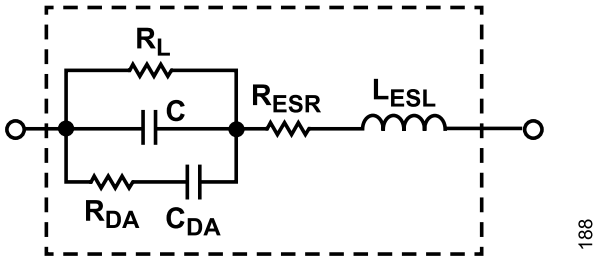


Figure 186. General Model of a Capacitor

LO SIGNAL CHAIN

The LO signal chain of the ADMV1355 accepts an input signal from the LO ball. The LO input signal is buffered with an amplifier, doubled using a ×2 multiplier, before being fed into tunable filters, a wideband 90° hybrid, and two adjustable phase shifters. See Figure 187 to see the LO signal chain. The LO signal chain is specified to operate with input frequencies from 8.85GHz to 27.5GHz.

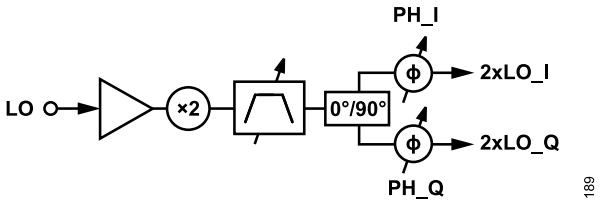


Figure 187. LO Chain Diagram

For input frequencies less than 25GHz, the specified power levels are from −7dBm to −3dBm. Functional, but degraded performance, is possible with input power levels from −10dBm to −7dBm and from −3dBm to 0dBm.

For input frequencies greater than or equal to 25GHz, the specified input levels are from −3dBm to 0dBm. Functional, but degraded, performance is possible with input power levels from −10dBm to −3dBm.

Minimize the harmonic content of the LO input signal to prevent unwanted spurious mixer products. It is recommended to keep all LO input harmonic signals −30dBc less than the fundamental LO signal.

To help reduce spurious mixer products, the LO tunable filters are used to optimize any LO harmonic content that may be present after the ×2 multiplier. Refer to the LO Tunable Filter section for additional recommendations on setting these tunable filters.

The wideband 90° hybrid and adjustable phase shifters generate the necessary mixer LO signals, 2×LO_I and 2×LO_Q. The mixer LO signals operate from 17.7GHz to 55GHz. The adjustable phase shifters allow trimming of the quadrature phase of the mixer LO signals to optimize the sideband rejection capabilities of the ADMV1355. Refer to the Sideband Rejection Optimization section for more information on how to perform this optimization. In addition, the LO chain includes an integrated LO-nulling loop that can operate in both automatic mode and manual mode. Refer to the

THEORY OF OPERATION

LO Nulling section for more information on how to perform this optimization.

LO TUNABLE FILTER

The LO tunable filter is set using Register 0x800, Register 0x801, Register 0x802, Register 0x804, Register 0x805, Register 0x806, and Register 0x80C. Refer to Table 17 for guidance on setting these filter based upon the LO input frequency.

For wideband applications, where the LO input frequency is continuously changing, it is beneficial to set the LO tunable filter for wideband operation. Setting the filter to wideband operation allows the mixer to be driven with a healthy input power level at the expense of spurious mixer products. See Table 18 for guidance on setting the filter based upon the wideband LO input frequencies.

Table 17. LO Tunable Filter Narrow-Band Recommended Settings

LO Frequency		4×LO	3×LO	1×LO	LO Trap		LO Band	LO Doubler
Minimum	Maximum	Register 0x800, Bits[3:0]	Register 0x801, Bits[4:0]	Register 0x802, Bits[4:0]	Register 0x804, Bits[7:0]	Register 0x805, Bits[1:0]	Register 0x806, Bit 7	Register 0x80C, Bits[7:0]
8.85	9.99	0x08	0x1C	0x1F	0x18	0x03	0x00	0x1F
10	11.99	0x00	0x1C	0x1F	0x18	0x03	0x00	0x1D
12	12.49	0x00	0x07	0x0A	0xAA	0x03	0x00	0x04
12.5	12.99	0x00	0x07	0x0A	0xAA	0x03	0x00	0x04
13	13.99	0x00	0x07	0x0A	0xAA	0x03	0x00	0x04
14	14.49	0x05	0x07	0x0A	0xAA	0x03	0x00	0x08
14.5	14.99	0x05	0x07	0x0A	0xA3	0x01	0x00	0x08
15	16.99	0x05	0x05	0x05	0xA3	0x01	0x00	0x08
17	17.99	0x05	0x04	0x01	0xA3	0x01	0x00	0x08
18	18.49	0x07	0x04	0x01	0xA3	0x01	0x01	0x80
18.5	18.99	0x07	0x04	0x01	0xA7	0x01	0x01	0x80
19	20.99	0x07	0x03	0x01	0xA7	0x01	0x01	0x80
21	23.99	0x07	0x02	0x00	0xE7	0x01	0x01	0x80
24	27.5	0x07	0x00	0x00	0xE7	0x01	0x01	0xC0

Table 18. LO Tunable Filter Wideband Recommended Settings

LO Frequency		4×LO	3×LO	1×LO	LO Trap		LO Band	LO Doubler
Minimum	Maximum	Register 0x800, Bits[3:0]	Register 0x801, Bits[4:0]	Register 0x802, Bits[4:0]	Register 0x804, Bits[7:0]	Register 0x805, Bits[1:0]	Register 0x806, Bit 5	Register 0x80C, Bits[7:0]
8.85	12.99	0x05	0x00	0x1F	0x18	0x03	0x00	0x08
13	27.5	0x05	0x00	0x1F	0xA7	0x01	0x01	0x80

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LO NULLING

In a RF system, the LO leakage at the output of a mixer can degrade the spectral purity and modulation accuracy of the transmitted signal. The ADMV1355 supports two methods of LO nulling to suppress the unwanted LO leakage that can appear at the RF output.

Automatic LO Nulling

The ADMV1355 includes an automatic LO nulling loop that uses an internal ADC, envelope detector, and calibration logic to measure and then minimize the LO leakage. The automatic LO nulling is supported in IF hybrid and complex IF modes and for LO frequencies from 12.5GHz to 27.5GHz. Because the LO leakage varies with frequency, temperature, supply voltage, and device tolerance, rerunning automatic LO nulling after configuration changes ensures optimal performance.

To run the automatic LO nulling, ensure that the LO signal is enabled at the required frequency and that the device is configured for the required input mode. Set the following registers sequentially to run the automatic LO nulling loop:

1. Set Register 0x302 to 0x02 to reset the internal ADC.
2. Set Register 0x300 to 0x09 to enable the internal ADC and ADC clock.
3. Set Register 0x306 to 0x02 to reset the LO nulling loop.
4. Set Register 0x305 to 0x20 to enable the LO nulling loop.
5. Set Register 0x13E to 0x00 to power up the ADC reference.
6. Set Register 0x2A7 to 0x00 to set the ADC multiplexer for LO nulling.
7. When using RF high band, set Register 0x306 to 0x12 and when using RF low band set Register 0x306 to 0x22. Register 0x306 is used to tap the envelop detector for the required RF frequency band.
8. Set Register 0x302 to 0x22 to set the LO nulling current using Register 0x304.
9. For LO nulling current optimum setting, set Register 0x304 to 0x1F. The register value can be tuned for the best LO nulling results at different frequencies.
10. Set Register 0x302 to 0x26 to enable the automatic LO nulling functionality.

Then, wait for 1ms and set the following registers sequentially to turn off the automatic LO nulling loop:

1. Set Register 0x302 to 0x22 to turn off the automatic LO nulling.
2. Set Register 0x306 to 0x02 to disable the envelope tapping.
3. Set Register 0x300 to 0x00 to disable the internal ADC and the ADC clock.

Manual LO Nulling

The ADMV1355 also supports manual LO nulling in IF hybrid and complex IF modes for applications requiring custom optimization or when automatic LO nulling cannot be executed during normal operation. To use manual LO nulling, disable the automatic LO nulling loop, by setting Register 0x305 to 0x03, and then use Register 0x808 and Register 0x809 to manually make adjustments to the internal LO nulling currents. Note that Register 0x808 and Register 0x809 use a twos complement format where 0x00 is zero correction, 0x7F is maximum positive current, and 0x80 is maximum negative current. These values are adjusted iteratively while monitoring LO leakage externally to achieve the desired LO nulling level.

To start manual LO nulling, ensure that the LO signal is enabled at the required frequency and that the device is configured for the required input mode. The following optimization sequence can be used to achieve effective LO nulling:

1. Initialize Register 0x808 and Register 0x809 by setting both to 0x00, which establishes a known starting point and ensures a stable LO leakage measurement setup prior to optimization.
2. Sweep Register 0x808 using four signed coarse values (for example: −64, −32, +32, +64) while holding Register 0x809 constant at its initialize value. For each programmed value, allow a sufficient settling time and record the corresponding LO leakage power in dBm.
3. Convert the measured LO leakage values from dBm to linear power. Using these linear values, perform a second-order polynomial curve fit of the form by using the following equation:
   $y = Ax^2 + Bx + C$
   where x represents the signed register value.
   y represents the measured linear power.
4. Determine the minimum of the fitted curve by taking the derivative and solving for the following equation:
   $x_0 = -(B/2A)$.
5. Round the computed value to the nearest valid signed integer and ensure that it is within the allowable range (−128 to +127).
6. Program Register 0x808 with the computed optimal value.
7. Sweep Register 0x809 using the same set of coarse signed values (−64, −32, +32, +64) while holding the optimized value of Register 0x808 fixed. Record the LO leakage at each step, convert to linear power, perform the same quadratic fitting procedure, and compute the optimal value by using the following equation:
   $-B/2A$.
8. Program Register 0x809 with the computed optimal value. At this stage, both registers contain coarse-optimized settings that significantly reduce the LO leakage.
9. To further improve LO leakage suppression, perform a fine optimization of Register 0x808. Sweep the four values centered around the coarse optimum x_0 using a small step size. For example: $x_0 - 6$, $x_0 - 2$, $x_0 + 2$, and $x_0 + 6$.

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10. Measure the LO leakage at each point, convert to linear power, perform a quadratic fitting, and compute the refined optimum by using the following equation:
$-B/2A$.
11. Program Register 0x808 with the refined value obtained from the fine sweep.
12. Perform fine optimization of Register 0x809 using the same method, sweeping values centered around its coarse optimum while holding the updated Register 0x808 fixed. Measure, fit, and compute the refined optimum, and then program Register 0x809 accordingly.
13. If, during either coarse or fine optimization, the calculated optimum lies outside the range of the sampled points, this indicates that the minimum has not been bracketed. In this case, shift the sweep window in the direction where LO leakage improves and repeat the measurement and fitting process until the minimum lies within the sampled range.
14. After completing the fine optimization for both registers, the final programmed values of 0x808 and 0x809 represent the optimized LO nulling settings. These values minimize LO leakage for the given operating conditions and LO frequency.

I/Q BASEBAND SIGNAL CHAIN

The I/Q baseband signal chain of the ADMV1355 supports frequencies from DC to 12GHz. Figure 188 shows the I/Q baseband signal chain. To enable the I/Q baseband signal chain, set Register 0x602 to 0x01. The I/Q baseband input ports, BB_IP, BB_IN, BB_QP, and BB_QN, are internally DC-coupled with a 100Ω differential input impedance. To disable the I/Q baseband signal chain, set Register 0x602, Bit 0, to 0.

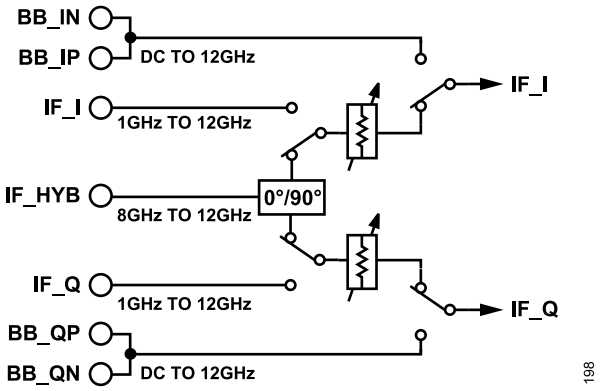


Figure 188. IF and I/Q Baseband Signal Chain

I/Q BASEBAND V_{ICM}

The V_{ICM} for the baseband input ports can range from 0V to 1.55V, and selecting an appropriate V_{ICM} ensures optimal mixer performance and linearity. When V_{ICM} is more than 0.5V, the mixer gate voltage automatically adjusts to maintain correct biasing of the mixer transistors. For V_{ICM} values equal to and less than 0.5V, the ADMV1355 requires manual configuration of the mixer gate bias.

To configure the chip when $V_{ICM} \leq 0.5V$, take the following steps:

1. Set Register 0x700, Bit 5, to 1 to enable manual mode.
2. Set Resister 0x702, Bit 5, to 1 to enable baseband switches to operate in manual mode.
3. Set Register 0x700, Bits[4:0], Register 0x702, Bits[4:0], and Register 0x703, Bits[4:0], as suggested in Table 19.

Table 19. Register 0x700, Register 0x702, and Register 0x703 Settings When $V_{ICM} \leq 0.5V$

Baseband V_{ICM} (V)	Register 0x700, Bits[4:0] (Hex)	Register 0x702, Bits[4:0] (Hex)	Register 0x703, Bits[4:0] (Hex)
0	0x02	0x0A	0x00
0.05	0x03	0x0B	0x00
0.1	0x04	0x0B	0x00
0.15	0x05	0x0C	0x00
0.2	0x06	0x0C	0x00
0.25	0x07	0x0D	0x00
0.3	0x08	0x0D	0x00
0.35	0x09	0x0E	0x00
0.4	0x0A	0x0E	0x00
0.45	0x0B	0x0F	0x00
0.5	0x0C	0X0F	0X00

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IF HYBRID SIGNAL CHAIN

The IF hybrid signal of the ADMV1355 supports frequencies from 8GHz to 12GHz and consists of a 90° hybrid. The IF_I and IF_Q outputs from the hybrid are fed to the mixer through fine adjust quadrature amplitude correction blocks. Refer to Figure 188 for representation of the IF signal chain. To enable the single-ended IF hybrid signal chain, set Register 0x602 to 0x08.

The IF_HYB input is internally DC-coupled with a 50Ω single-ended impedance. When the IF_HYB is not used, the IF_HYB ball can be left floating. To disable the single-ended IF hybrid signal chain, set Register 0x602, Bit 3, to 0.

COMPLEX IF SIGNAL CHAIN

The complex IF signal of the ADMV1355 supports frequencies from 1GHz to 12GHz, and each of IF_I and IF_Q paths consist of a low frequency signal chain ranging from 1GHz to 4GHz and a high frequency signal chain ranging from 3GHz to 12GHz. The ADMV1355 allows users to select the required path for their input frequency. The IF_I and IF_Q inputs are fed to the mixer through fine adjust quadrature amplitude correction blocks. Refer to Figure 188 for representation of the complex IF signal chain. To enable the complex IF low frequency signal chain, set Register 0x602 to 0x02. To enable the complex IF high frequency signal chain, set Register 0x602 to 0x04.

The IF_I and IF_Q inputs are internally DC-coupled with a 50Ω single-ended impedance. When the IF_I and IF_Q are not used, the IF_I and IF_Q balls can be left floating.

To disable the complex IF low frequency signal chain, set Register 0x602, Bit 1, to 0. To disable the complex IF high frequency signal chain, set Register 0x602, Bit 2, to 0.

MIXER OVERVIEW

The ADMV1355 contains a sideband rejecting, up converting I/Q mixer with excellent linearity and noise figure. The necessary LO signals, 2×LO_I and 2×LO_Q, to drive the mixer come from the LO signal chain. The quadrature inputs from the IF signal chain and I/Q baseband signal chain, IF_I and IF_Q, also feeds into the mixer. The output from the mixer, RF_C, is then used to drive the RF signal chains. The mixer supports RF output and 2×LO input frequencies up to 55GHz. Figure 189 shows the mixer.

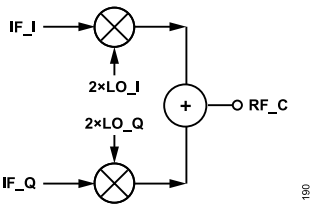


Figure 189. Mixer Diagram

MIXER SIDEBAND SELECTION

The ADMV1355 mixer sideband can be selected by swapping the mixer LO inputs, 2×LO_I and 2×LO_Q. To swap these inputs, use Register 0x806, Bit 5. When the RF frequency < the 2×LO frequency, set Bit 5 to 0 for the lower sideband, and when the RF frequency > the 2×LO frequency, set Bit 5 to 1 for upper sideband.

RF SIGNAL CHAINS

The RF_OUT ball of the ADMV1355 is connected directly to switch selectable, wideband, RF signal chains. The low band, RF signal chain operates from 17.7GHz to 34GHz, and the high band, RF signal chain operates from 30GHz to 55GHz. Each signal chain includes multiple DSAs and tunable filters. Figure 190 shows the RF signal chains.

To select the low band, RF signal chain, set Register 0x805, Bit 7, and Register 0x806, Bit 6, to 0.To select the high band, RF signal chain, set Register 0x805, Bit 7, and Register 0x806, Bit 6, to 1.

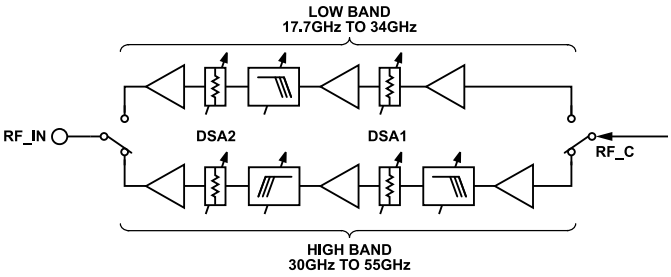


Figure 190. RF Signal Chain Diagram

DSA1

The DSA directly after the mixer signal chain in the RF signal chains is DSA1. This attenuator offers 16 states, 0dB to 15dB, with 1dB steps. The attenuation is proportional to the value programmed.

When using the bypass registers (Register 0x28A, Bit 0, set to 1), use Register 0x28B, Bits[3:0], to set the DSA1 state. When not using the bypass registers (Register 0x28A, Bit 0, set to 0), use Register 0x600, Bits[3:0], to set the DSA1 state.

DSA2

The DSA directly after DSA1 in the RF signal chains is DSA2. This attenuator offers 16 states, 0dB to 15dB, with 1dB steps. The attenuation is proportional to the value programmed.

When using the bypass registers (Register 0x28A, Bit 0, set to 1), use Register 0x28B, Bits[7:4], to set the DSA2 state. When not using the bypass registers (Register 0x28A, Bit 0, set to 0), use Register 0x600, Bits[7:4], to set the DSA2 state.

RF TUNABLE LPFS

Both the low-band and the high-band RF signal chains contain a tunable LPF to help with sideband rejection. Each tunable LPF contains 4 bits, or 16 states, that control the cutoff frequency.

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The cutoff frequency is inversely proportional to the LPF value programmed.

When using the bypass register (Register 0x2A0), set Bit 4 to 1, and then program the intended LPF value into Bits[3:0]. When not using the bypass register (Register 0x2A0), set Bit 4 to 0, and then use Register 0x80B, Bits[3:0], or the frequency LUT.

When using either Register 0x80B or the frequency LUT, the low-band tunable LPF has three control bits (0 to 7), and the value programmed is multiplied by 2 (shifted left by one position). For example, when Register 0x80B, Bits[3:0], are set to 7, the effective LPF value is 14.

When using either Register 0x80B or the frequency LUT, the high-band tunable LPF retains the full four control bits.

RF TUNABLE HPF

The high-band RF signal chain contains a tunable HPF to help with sideband rejection. The tunable HPF contains 6 bits, or 64 states, that control the cutoff frequency. The cutoff frequency is inversely proportional to the HPF value programmed.

When using the bypass register (Register 0x2A1), set Bit 7 to 1, and then program the intended HPF value into Bits[5:0]. When not using the bypass register (Register 0x2A1), set Bit 7 to 0, and then use Register 0x80B, Bits[7:4], or the frequency LUT.

When using either Register 0x80B or the frequency LUT, the tunable HPF has four control bits, and the value programmed is multiplied by 4 (shifted left by two positions). For example, when Register 0x80B, Bits[7:4], are set to 15, the effective HPF value is 60.

SIDEBAND REJECTION OPTIMIZATION

The sideband rejection capability of a mixer is defined as the ability to suppress the unwanted sideband (image sideband) that would otherwise appear at the output RF frequency. For example, if the intended IF input frequency is 8GHz, the 2×LO_I and 2×LO_Q mixer 2×LO frequencies are 28GHz, and if the desired RF output frequency is 36GHz, the unwanted image sideband appears at 20GHz.

Imperfections in the quadrature phase imbalance of the mixer LO signals (ideal 90°), amplitude imbalance between the mixer I/Q paths (ideal 0dB), as well as imbalance in the IF input hybrid network, may cause a residual unwanted sideband to appear at the mixer RF output. To overcome these imperfections and optimize the sideband rejection capability of the ADMV1355, the phase of the mixer LO signals and the amplitude of the mixer inputs can be finely adjusted.

The adjustable phase shifters, PH_I and PH_Q, in the LO signal chain allow correction of quadrature phase imbalance between the 2×LO_I and 2×LO_Q signals. Each phase shifter has a typical 0.6° step size and a 20° tuning range across 32 states. Use Register 0x806, Bits[4:0], to adjust the phase of 2×LO_I, and use Register 0x805, Bits[6:2], to adjust the phase of 2×LO_Q.

The IF_I and IF_Q input signals to the mixer feed through fine-adjust DSAs, DSAI and DSAQ. These attenuators allow for small 0.1dB steps and 1.5dB total amplitude control to optimize the sideband rejection capability of the ADMV1355. Use Register 0x80A to adjust these attenuators. Bits [3:0] set DSAI, and Bits[7:4] set DSAQ.

When applying an IF input frequency and observing the RF output power level, there are various options to perform sideband rejection optimization. See the Sensitivity Guided Optimization section and the Coarse and Fine Sweep Optimization section for two possible options.

Sensitivity Guided Optimization

The first option for performing sideband rejection optimization uses sensitivity analysis to assist in making decisions to narrow the scope of possible optimization values. To perform this optimization, apply an IF image frequency and take the following steps while measuring the RF output power at the image frequency:

1. Set both PH_I and PH_Q to 15.
2. Set both DSAI and DSAQ to 0.
3. Step through the DSAI values starting from 0. Stop sweeping when a local minima for the RF output power has been achieved and retain the DSAI value that provides the local minima.
4. Repeat Step 3 for DSAQ.
5. Set PH_I to 14 and then 16 to determine the optimum direction to step through. If PH_I = 14 provides a better result than PH_I = 16, then step through the values from 13 to 0; otherwise, step through values 17 to 31. Stop sweeping when a local minima for the RF output power has been achieved and retain the PH_I value that provides the local minima.
6. Repeat Step 5 for PH_Q.
7. With the values determined in Step 3 to Step 6 for DSAI, DSAQ, PH_I, and PH_Q, further optimization may be possible by adjusting each ±1 value.

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Coarse and Fine Sweep Optimization

The second option for performing sideband rejection optimization uses a coarse sweep followed by a fine sweep to determine the optimization values. To perform this optimization, apply an IF image frequency and take the following steps while measuring the RF output power:

1. Set both PH_I and PH_Q to 0.
2. Set DSAQ to 0. Step through the DSAI values starting from 0 to 15. Record the RF output power for each value.
3. Set DSAI to 0. Step through the DSAQ values starting from 0 to 15. Record the RF output power for each value.
4. Pick the combination of values from Step 2 and Step 3 that provide the lowest RF output power. Note, that one fine step DSA value will be zero.
5. Perform a nested coarse sweep of PH_I and PH_Q for values 0, 4, 8, 12, 16, 20, 24, and 28. There are 64 combinations of those values for both phase shifters that are tested. Record the combination of values that provides the lowest RF output power.
6. Use the combination of values determined in Step 5 to then determine the fine sweep range by adding and subtracting 4 from each value. Perform a nested fine sweep of PH_I and PH_Q for these values. For example, if Step 5 yielded PH_I = 16 and PH_Q = 12, then the fine sweep range for PH_I is 12 to 20, and the fine sweep range for PH_Q is 8 to 16. Excluding the coarse values from the fine sweep, there are an additional 80 combinations of fine sweep values. Pick the combination of values that provides the lowest RF output power.

TOTAL GAIN CONTROL

The typical total available gain (attenuation) control for each type of configuration that can be implemented with the ADMV1355 is 30dB.

RF GAIN POLICY

The RF gain (attenuation) policy for ideal mixer performance is to keep all DSAs at their maximum gain state.

To optimize output P1dB and output IP3 performance, set the attenuation by introducing attenuation in DSA1, followed by DSA2. Applying attenuation in this order ensures that the signal level presented to the downstream RF stages is appropriately managed while minimizing degradation of the linearity of the system. By prioritizing attenuation in DSA1 before DSA2, the cascade linearity of the signal chain is preserved, resulting in improved compression and intermodulation performance.

ADC CONFIGURATION

The ADMV1355 includes an on-chip, ADC that can capture the temperature sensor value. The value can then be read back using the SPI via Register 0x30D.

To set up the automatic ADC configuration, take the following steps:

1. Set Register 0x302 to 0x02 to enable the ADC_RESET.
2. Set Register 0x300 to 0x09 to enable the ADC configuration and to enable ADC_CLK_EN.
3. Set Register 0x306 to 0x02 to enable LON_RESET, which resets the internal registers in LO nulling block.
4. Set Register 0x13E to 0x00 to make sure ADC_REF_PD and TEMP_SENSOR_PD are set to normal operation.
5. Set Register 0x2A7 to 0x01 to set ADC_MUX_SELECT for the temperature sensor.
6. Set Register 0x302 to 0x06 to enable LON_AUTO_EN and start the ADC.
7. Read Register 0x30D (ADC_OUT) for the temperature sensor value.

TEMPERATURE SENSOR

The ADMV1355 contains an on-chip temperature sensor that allows monitoring of the chip temperature. The temperature sensor output can be sampled using the on-chip ADC, and the value can then be read back via the SPI.

Follow the instructions in the ADC Configuration section for information on setting up the ADC and reading back the temperature sensor value.

To estimate the T_C of the ADMV1355, use the following equation:

$$T_C = -\frac{5}{6} \times ADC_CODE + 173 \quad (3)$$

where *ADC_CODE* is what the chip reads back from the ADC_OUT bits (Register 0x30D, Bits[7:0]).

APPLICATIONS INFORMATION

BASEBAND MODE SIDEBAND REJECTION WITH THE APOLLO DACS

The baseband mode sideband rejection of the ADMV1355 can be improved by directly driving the I and Q ports with the Apollo DACs (2× or 4× DAC outputs). This configuration enables well-balanced, wide baseband frequency coverage with minimal external analog conditioning, and it also reflects practical system-level operation with high-speed DACs. Figure 194 shows a block diagram of the measurement setup using the EVAL-AD9084 evaluation board.

Figure 191 and Figure 192 show the measured I/Q amplitude imbalance and phase imbalance over temperature of the ADMV1355 when the baseband frequency is fixed at 100MHz and the LO frequency is swept across the high RF band. Figure 193 shows the sideband rejection that is achieved when using the Apollo coarse numerically controlled oscillators (CNCO) to correct for the I/Q imbalance of the ADMV1355 at different temperatures. The Apollo CNCOs have sufficient resolution to achieve < −60dBc sideband rejection. Refer toFigure 142 for the uncorrected sideband rejection performance. Figure 191 through Figure 193 can help determine the amount of temperature drift that is tolerable before requiring an updated I/Q correction.

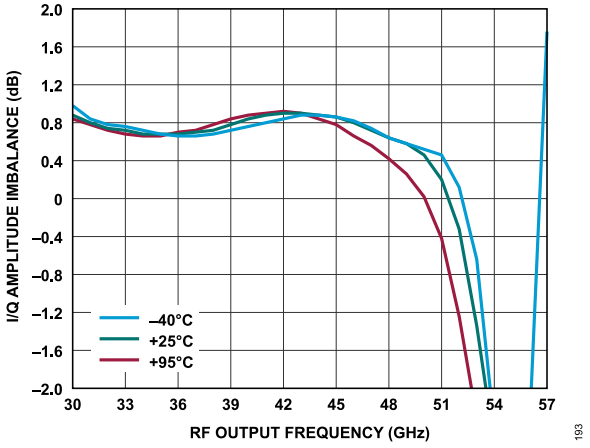


Figure 191. I/Q Amplitude Imbalance vs. RF Output Frequency at Various Temperatures Using the Apollo DACs

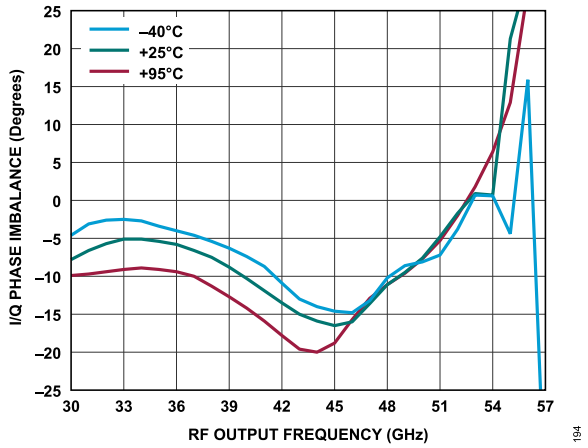


Figure 192. I/Q Phase Imbalance vs. RF Output Frequency at Various Temperatures Using the Apollo DACs

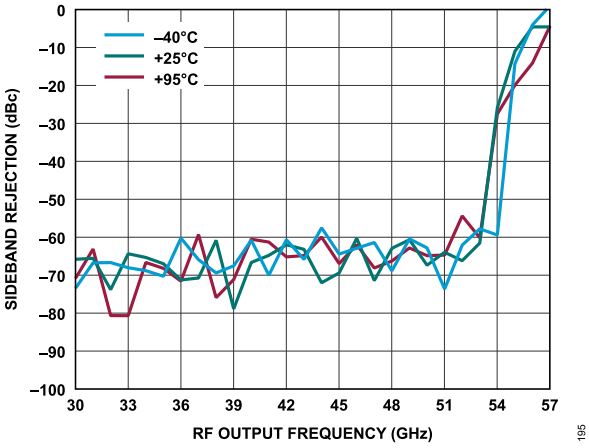
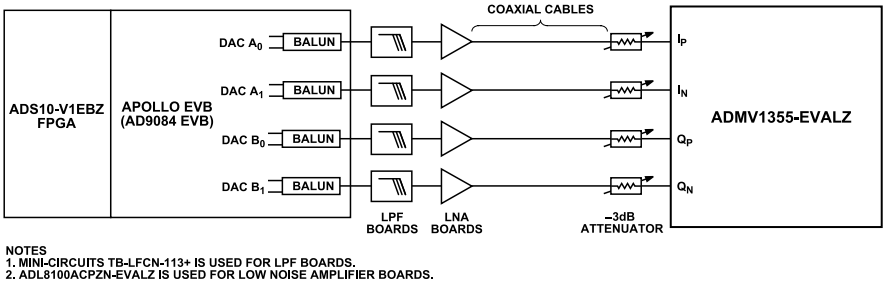


Figure 193. Sideband Rejection vs. RF Output Frequency at Various Temperatures Using the Apollo DACs



NOTES
1. MINI-CIRCUITS TB-LFCN-113+ IS USED FOR LPF BOARDS.
2. ADL8100ACPZN-EVALZ IS USED FOR LOW NOISE AMPLIFIER BOARDS.

Figure 194. Block Diagram of Measurement Setup Using the Apollo DACs

APPLICATIONS INFORMATION

RECOMMENDED SETTINGS

For wideband operation or to begin evaluating the ADMV1355, refer to Table 20 and Table 21 for the recommended settings. These recommended settings can be considered the minimum requirements for configuring the ADMV1355. Additional features can be configured, and all settings can be tailored for a particular end application. Refer to the Theory of Operation for more details.

Table 20. Recommended Settings for IF Hybrid Mode and I/Q Baseband Mode

	IF Hybrid Mode		I/Q Baseband Mode		
Register	RF Low Band	RF High Band	RF Low Band	RF High Band	Notes
0x000	0x18	0x18	0x18	0x18	Enables the SDO output.
0x13E	0x02	0x02	0x02	0x02	Configures the power downs.
0x202	0x00	0x00	0x00	0x00	Disables the LUT of the filter.
0x208	0x00	0x00	0x00	0x00	Disables the load enable bit for the filter.
0x2A0	0x10	0x10	0x10	0x10	Sets the RF chain LPF to the highest cutoff frequency.
0x2A1	Don't care	0xBF	Don't care	0xBF	Sets the RF chain HPF to the lowest cutoff frequency.
0x600	0x00	0x00	0x00	0x00	Configures the maximum gain.
0x602	0x08	0x08	0x01	0x01	Sets the single-ended IF hybrid or baseband signal chain.
0x800	0x05	0x05	0x05	0x05	Configures the filters.
0x801	0x00	0x00	0x00	0x00	Configures the filters.
0x802	0x1F	0x1F	0x1F	0x1F	Configures the filters.
0x804	0xA7	0xA7	0xA7	0xA7	Configures the filters.
0x805	0x41	0xC1	0x41	0xC1	Configures the bands, LO phase, and filters.
0x806	0x90	0xF0	0x90	0xF0	Configures the LO phase and LO band.
0x80A	0x00	0x00	0x00	0x00	Configures the IF gain adjust for the sideband rejection.
0x80C	0x80	0x80	0x80	0x80	Configures the filters.

Table 21. Recommended Settings for Complex IF Low Frequency Mode and Complex IF High Frequency Mode

	Complex IF Low Frequency Mode		Complex IF High Frequency Mode		
Register	RF Low Band	RF High Band	RF Low Band	RF High Band	Notes
0x000	0x18	0x18	0x18	0x18	Enables the SDO output.
0x13E	0x02	0x02	0x02	0x02	Configures the power downs.
0x202	0x00	0x00	0x00	0x00	Disables the LUT of the filter.
0x208	0x00	0x00	0x00	0x00	Disables the load enable bit for the filter.
0x2A0	0x10	0x10	0x10	0x10	Sets the RF chain LPF to the highest cutoff frequency.
0x2A1	Don't care	0xBF	Don't care	0xBF	Sets the RF chain HPF to the lowest cutoff frequency.
0x600	0x00	0x00	0x00	0x00	Configures the maximum gain.
0x602	0x02	0x02	0x04	0x04	Enables the complex IF low frequency or high frequency signal chain.
0x800	0x05	0x05	0x05	0x05	Configures the filters.
0x801	0x00	0x00	0x00	0x00	Configures the filters.
0x802	0x1F	0x1F	0x1F	0x1F	Configures the filters.
0x804	0xA7	0xA7	0xA7	0xA7	Configures the filters.
0x805	0x41	0xC1	0x41	0xC1	Configures the bands, LO phase, and filters.
0x806	0x90	0xF0	0x90	0xF0	Configures the LO phase and LO band.
0x80A	0x00	0x00	0x00	0x00	Configures the IF gain adjust for the sideband rejection.
0x80C	0x80	0x80	0x80	0x80	Configures the filters.

APPLICATIONS INFORMATION

RECOMMENDED PCB LAYOUT

The ADMV1355 package type is a ball grid array that allows for a high pin count in a small footprint. The exposed balls on the underside of the package are intended to be soldered to a low thermal and electrical impedance ground plane. Typically, the PCB contains a solder mask defined land pattern for each ball to ensure proper solder containment and attachment.

Care must be taken with the RF trace routing escape plan for a particular implementation. In order of precedence, it is recommended to prioritize the RF traces, followed by the power supply pins, and then the digital logic connections.

The RF connections into and out of the ADMV1355 are near the edge of the package to ease the escape plan. Inner layer trace stripline routing is encouraged, particularly for applications where RF isolation performance metrics are important. Regardless of the type of RF traces employed in a PCB design, it is generally recommended to have via stitching run parallel to either side of the RF traces. The via stitching can be either through-board type vias or blind layer-to-layer vias.

Ideally, the ground connection balls are connected to the through-board type vias to maximum the heat transfer from the package to the PCB thermal plane. Refer to the Thermal Resistance section for more information on the thermal performance metrics of the ADMV1355.

The ADMV1355 evaluation board utilizes the recommendations listed within this section, and this section is a good starting point for many applications. Refer to the ADMV1355-EVALZ user guide for more information regarding the evaluation board.

EVALUATION BOARD INFORMATION

See the ADMV1355-EVALZ evaluation board web page for additional information on the evaluation board for the ADMV1355.

REGISTER SUMMARY

Note: The Filter LUT A Index 1 to filter LUT B Index 31 bit fields functionality (Register 0x90D to Register 0xC3F) is identical to filter LUT A Index 0 bit fields functionality (Register 0x900 and Register 0x90C). The Gain LUT Index 1 to gain LUT Index 66 bit fields functionality (Register 0xE02 to Register 0xE85) is identical to gain LUT_0 bit fields functionality (Register 0xE00 and Register 0xE01).

Table 22. ADMV1355 Register Summary

Reg	Name	Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset	Access
0x000	REG0000	[7:0]	SOFT_RESET_R	LSB_FIRST_R	ADDR_ASCN_R	SDO_ACTIVE_R	SDO_ACTIVE	ADDR_ASCN	LSB_FIRST	SOFT_RESET	0x00	R/W
0x004	REG0004	[7:0]	PRODUCT_ID[7:0]								0x00	R
0x005	REG0005	[7:0]	PRODUCT_ID[15:8]								0x00	R
0x00A	REG000A	[7:0]	SCRATCH_PAD								0x00	R/W
0x078	REG0078	[7:0]	RESERVED			NVM_OSC_CONFIG					0x09	R/W
0x07B	REG007B	[7:0]	NVM_READ_ADDRESS								0x00	R/W
0x07C	REG007C	[7:0]	NVM_READ_DATA[7:0]								0x00	R
0x07D	REG007D	[7:0]	NVM_READ_DATA[15:8]								0x00	R
0x07E	REG007E	[7:0]	NVM_REFRESH								0x68	R/W
0x13E	REG013E	[7:0]	TEMP_SENSOR_PD	RESERVED		LON_PD	ADC_REF_PD	RE-SERVED	RF_HS_PD	CHIP_PD	0x00	R/W
0x200	REG0200	[7:0]	FILTER_SM_STEP								0x01	R/W
0x202	REG0202	[7:0]	RESERVED							FILTER_LUT_EN	0x00	R/W
0x203	REG0203	[7:0]	RESERVED						FILTER_LUT_MODE		0x00	R/W
0x204	REG0204	[7:0]	RESERVED							FILTER_SM_RESET	0x01	R/W
0x205	REG0205	[7:0]	FILTER_SM_POINTER								0x00	R
0x206	REG0206	[7:0]	RESERVED			FILTER_SM_STOP					0x1F	R/W
0x207	REG0207	[7:0]	RESERVED							FILTER_LUT_SELECT	0x00	R/W
0x208	REG0208	[7:0]	RESERVED							FILTER_LOAD_EN	0x00	R/W
0x209	REG0209	[7:0]	RESERVED			FILTER_SPI_POINTER					0x00	W
0x20A	REG020A	[7:0]	RESERVED		FILTER_SM_WRAP	FILTER_SM_START					0x00	R/W
0x210	REG0210	[7:0]	RESERVED			FILTER_ADD_F_READBACK					0x00	R
0x211	REG0211	[7:0]	FILTER_LUT_OUTPUT[7:0]								0x00	R
0x212	REG0212	[7:0]	FILTER_LUT_OUTPUT[15:8]								0x00	R
0x213	REG0213	[7:0]	FILTER_LUT_OUTPUT[23:16]								0x00	R
0x214	REG0214	[7:0]	FILTER_LUT_OUTPUT[31:24]								0x00	R
0x215	REG0215	[7:0]	FILTER_LUT_OUTPUT[39:32]								0x00	R
0x216	REG0216	[7:0]	FILTER_LUT_OUTPUT[47:40]								0x00	R
0x217	REG0217	[7:0]	FILTER_LUT_OUTPUT[55:48]								0x00	R
0x218	REG0218	[7:0]	FILTER_LUT_OUTPUT[63:56]								0x00	R
0x219	REG0219	[7:0]	FILTER_LUT_OUTPUT[71:64]								0x00	R
0x21A	REG021A	[7:0]	FILTER_LUT_OUTPUT[79:72]								0x00	R
0x21B	REG021B	[7:0]	FILTER_LUT_OUTPUT[87:80]								0x00	R
0x21C	REG021C	[7:0]	FILTER_LUT_OUTPUT[95:88]								0x00	R
0x21D	REG021D	[7:0]	FILTER_LUT_OUTPUT[103:96]								0x00	R
0x220	REG0220	[7:0]	FILTER_READBACK[7:0]								0x00	R
0x221	REG0221	[7:0]	FILTER_READBACK[15:8]								0x00	R

REGISTER SUMMARY

Table 22. ADMV1355 Register Summary (Continued)

Reg	Name	Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset	Access
0x222	REG0222	[7:0]	FILTER_READBACK[23:16]								0x00	R
0x223	REG0223	[7:0]	FILTER_READBACK[31:24]								0x00	R
0x224	REG0224	[7:0]	FILTER_READBACK[39:32]								0x00	R
0x225	REG0225	[7:0]	FILTER_READBACK[47:40]								0x00	R
0x226	REG0226	[7:0]	FILTER_READBACK[55:48]								0x00	R
0x227	REG0227	[7:0]	FILTER_READBACK[63:56]								0x00	R
0x228	REG0228	[7:0]	FILTER_READBACK[71:64]								0x00	R
0x229	REG0229	[7:0]	FILTER_READBACK[79:72]								0x00	R
0x22A	REG022A	[7:0]	FILTER_READBACK[87:80]								0x00	R
0x22B	REG022B	[7:0]	FILTER_READBACK[95:88]								0x00	R
0x22C	REG022C	[7:0]	FILTER_READBACK[103:96]								0x00	R
0x240	REG0240	[7:0]	FILTER_LUT_POINTER								0x00	R
0x281	REG0281	[7:0]	RESERVED							GAIN_LOAD_EN	0x00	R/W
0x282	REG0282	[7:0]	RE-SERVED	GAIN_SPI_POINTER							0x00	R/W
0x283	REG0283	[7:0]	GAIN_SM_STEP								0x01	R/W
0x284	REG0284	[7:0]	GAIN_SM_OFFSET								0x00	R/W
0x285	REG0285	[7:0]	RESERVED							GAIN_LUT_EN	0x01	R/W
0x286	REG0286	[7:0]	RESERVED						GAIN_LUT_MODE		0x00	R/W
0x287	REG0287	[7:0]	RESERVED							GAIN_SM_RESET	0x01	R/W
0x288	REG0288	[7:0]	GAIN_SM_POINTER_PLUS_OFFSET								0x00	R
0x289	REG0289	[7:0]	RE-SERVED	GAIN_SM_STOP							0x42	R/W
0x28A	REG028A	[7:0]	RESERVED							GAIN_LUT_BYPASS_EN	0x00	R/W
0x28B	REG028B	[7:0]	DSA2_BYPASS_VALUE				DSA1_BYPASS_VALUE				0x00	R/W
0x28C	REG028C	[7:0]	RESERVED			GPO_G_BYPASS					0x00	R/W
0x28F	REG028F	[7:0]	GAIN_LUT_OUTPUT[7:0]								0x00	R
0x290	REG0290	[7:0]	RESERVED			GAIN_LUT_OUTPUT[12:8]					0x00	R
0x293	REG0293	[7:0]	GAIN_READBACK[7:0]								0x00	R
0x294	REG0294	[7:0]	RESERVED			GAIN_READBACK[12:8]					0x00	R
0x298	REG0298	[7:0]	GAIN_LUT_POINTER								0x00	R
0x29B	REG029B	[7:0]	GAIN_SM_POINTER_PRE_OFFSET								0x00	R
0x2A0	REG02A0	[7:0]	RESERVED			LPF_SELECT	LPF_BYPASS_VALUE				0x00	R/W
0x2A1	REG02A1	[7:0]	HPF_SELECT	RE-SERVED	HPF_BYPASS_VALUE						0x3F	R/W
0x2A3	REG02A3	[7:0]	RESERVED				LPF_READBACK				0x00	R
0x2A4	REG02A4	[7:0]	RESERVED		HPF_READBACK						0x00	R
0x2A7	REG02A7	[7:0]	RESERVED			ADC_MUX_SELECT					0x00	R/W
0x2B0	REG02B0	[7:0]	RESERVED		GAIN_ADD_G_READBACK						0x00	R
0x300	REG0300	[7:0]	RESERVED				ADC_EN	RESERVED		ADC_CLK_EN	0x00	R/W
0x302	REG0302	[7:0]	RESERVED		LON_CURRENT	RESERVED		LON_AUTO_EN	ADC_RESET	RE-SERVED	0x00	R/W

REGISTER SUMMARY

Table 22. ADMV1355 Register Summary (Continued)

Reg	Name	Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset	Access
					_SELECT							
0x304	REG0304	[7:0]	RESERVED			LON_CURRENT					0x14	R/W
0x305	REG0305	[7:0]	RESERVED		LON_EN	RESERVED			LON_Q_SELECT	LON_I_SELECT	0x00	R/W
0x306	REG0306	[7:0]	RESERVED		RF_LB_ENV_TAP	RF_HB_ENV_TAP	RESERVED		LON_RESET	RE-SERVED	0x00	R/W
0x30D	REG030D	[7:0]	ADC_OUT								0x00	R
0x402	REG0402	[7:0]	RESERVED		BGR_TEMP_SENSOR_PD	BGR_CHIP_PD	BGR_ADC_PD	RESERVED			0x04	R/W
0x600	REG0600	[7:0]	RF_DSA2_GAIN				RF_DSA1_GAIN				0x00	R/W
0x601	REG0601	[7:0]	RESERVED			GPO_G					0x00	R/W
0x602	REG0602	[7:0]	RESERVED				IF_HYBRID_EN	IF_HIGH_FREQ_EN	IF_LOW_FREQ_EN	BB_EN	0x08	R/W
0x700	REG0700	[7:0]	RESERVED		MIXER_GATE_SELECT	MIXER_GATE					0x10	R/W
0x702	REG0702	[7:0]	RESERVED		BB_SW_SELECT	BB_SW_NMOS					0x00	R/W
0x703	REG0703	[7:0]	RESERVED			BB_SW_PMOS					0x00	R/W
0x780	REG0780	[7:0]	GPO_G_OE[1:0]		GPO_F_OE						0x00	R/W
0x781	REG0781	[7:0]	RESERVED					GPO_G_OE[4:2]			0x00	R/W
0x800	REG0800	[7:0]	RESERVED				LO_X4_FILTER				0x00	R/W
0x801	REG0801	[7:0]	RESERVED			LO_X3_FILTER					0x00	R/W
0x802	REG0802	[7:0]	RESERVED			LO_X1_FILTER					0x00	R/W
0x803	REG0803	[7:0]	RESERVED		GPO_F						0x00	R/W
0x804	REG0804	[7:0]	LO_TRAP_FILTER[7:0]								0x00	R/W
0x805	REG0805	[7:0]	RF_BAND_SELECT	LO_PHASE_Q					LO_TRAP_FILTER[9:8]		0x40	R/W
0x806	REG0806	[7:0]	LO_BAND	MIXER_BAND	LO_SIDEBAND	LO_PHASE_I					0x30	R/W
0x808	REG0808	[7:0]	LON_OFFSET_I								0x00	R/W
0x809	REG0809	[7:0]	LON_OFFSET_Q								0x00	R/W
0x80A	REG080A	[7:0]	DSAQ				DSAI				0x00	R/W
0x80B	REG080B	[7:0]	HPF_VALUE				LPF_VALUE				0x00	R/W
0x80C	REG080C	[7:0]	LO_DOUBLER_BAND								0x00	R/W
0x900	REG0900	[7:0]	RESERVED				LO_X4_FILTER_LUT_A_0				0x00	R/W
0x901	REG0901	[7:0]	RESERVED			LO_X3_FILTER_LUT_A_0					0x00	R/W
0x902	REG0902	[7:0]	RESERVED			LO_X1_FILTER_LUT_A_0					0x00	R/W
0x903	REG0903	[7:0]	RESERVED		GPO_F_LUT_A_0						0x00	R/W
0x904	REG0904	[7:0]	LO_TRAP_FILTER_LUT_A_0[7:0]								0x00	R/W
0x905	REG0905	[7:0]	RF_BAND_SELECT_LUT_A_0	LO_PHASE_Q_LUT_A_0					LO_TRAP_FILTER_LUT_A_0[9:8]		0x00	R/W
0x906	REG0906	[7:0]	LO_BAND_LUT_A_0	MIXER_BAND_LUT_A_0	LO_SIDE-BAND_LUT_A_0	LO_PHASE_I_LUT_A_0					0x00	R/W

REGISTER SUMMARY

Table 22. ADMV1355 Register Summary (Continued)

Reg	Name	Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset	Access
0x908	REG0908	[7:0]	LON_OFFSET_I_LUT_A_0								0x00	R/W
0x909	REG0909	[7:0]	LON_OFFSET_Q_LUT_A_0								0x00	R/W
0x90A	REG090A	[7:0]	DSAQ_LUT_A_0				DSAI_LUT_A_0				0x00	R/W
0x90B	REG090B	[7:0]	HPF_VALUE_LUT_A_0				LPF_VALUE_LUT_A_0				0x00	R/W
0x90C	REG090C	[7:0]	LO_DOUBLER_BAND_LUT_A_0								0x00	R/W
…	…	…	…								…	…
0xA93	REG0A93	[7:0]	RESERVED				LO_X4_FILTER_LUT_A_31				0x00	R/W
0xA94	REG0A94	[7:0]	RESERVED			LO_X3_FILTER_LUT_A_31					0x00	R/W
0xA95	REG0A95	[7:0]	RESERVED			LO_X1_FILTER_LUT_A_31					0x00	R/W
0xA96	REG0A96	[7:0]	RESERVED		GPO_F_LUT_A_31						0x00	R/W
0xA97	REG0A97	[7:0]	LO_TRAP_FILTER_LUT_A_31[7:0]								0x00	R/W
0xA98	REG0A98	[7:0]	RF_BAND_SELECT_LUT_A_31	LO_PHASE_Q_LUT_A_31					LO_TRAP_FILTER_LUT_A_31[9:8]		0x00	R/W
0xA99	REG0A99	[7:0]	LO_BAND_LUT_A_31	MIXER_BAND_LUT_A_31	LO_SIDE-BAND_LUT_A_31	LO_PHASE_I_LUT_A_31					0x00	R/W
0xA9B	REG0A9B	[7:0]	LON_OFFSET_I_LUT_A_31								0x00	R/W
0xA9C	REG0A9C	[7:0]	LON_OFFSET_Q_LUT_A_31								0x00	R/W
0xA9D	REG0A9D	[7:0]	DSAQ_LUT_A_31				DSAI_LUT_A_31				0x00	R/W
0xA9E	REG0A9E	[7:0]	HPF_VALUE_LUT_A_31				LPF_VALUE_LUT_A_31				0x00	R/W
0xA9F	REG0A9F	[7:0]	LO_DOUBLER_BAND_LUT_A_31								0x00	R/W
0xAA0	REG0AA0	[7:0]	RESERVED				LO_X4_FILTER_LUT_B_0				0x00	R/W
0xAA1	REG0AA1	[7:0]	RESERVED			LO_X3_FILTER_LUT_B_0					0x00	R/W
0xAA2	REG0AA2	[7:0]	RESERVED			LO_X1_FILTER_LUT_B_0					0x00	R/W
0xAA3	REG0AA3	[7:0]	RESERVED		GPO_F_LUT_B_0						0x00	R/W
0xAA4	REG0AA4	[7:0]	LO_TRAP_FILTER_LUT_B_0[7:0]								0x00	R/W
0xAA5	REG0AA5	[7:0]	RF_BAND_SELECT_LUT_B_0	LO_PHASE_Q_LUT_B_0					LO_TRAP_FILTER_LUT_B_0[9:8]		0x00	R/W
0xAA6	REG0AA6	[7:0]	LO_BAND_LUT_B_0	MIXER_BAND_LUT_B_0	LO_SIDE-BAND_LUT_B_0	LO_PHASE_I_LUT_B_0					0x00	R/W
0xAA8	REG0AA8	[7:0]	LON_OFFSET_I_LUT_B_0								0x00	R/W
0xAA9	REG0AA9	[7:0]	LON_OFFSET_Q_LUT_B_0								0x00	R/W
0xAAA	REG0AAA	[7:0]	DSAQ_LUT_B_0				DSAI_LUT_B_0				0x00	R/W
0xAAB	REG0AAB	[7:0]	HPF_VALUE_LUT_B_0				LPF_VALUE_LUT_B_0				0x00	R/W
0xAAC	REG0AAC	[7:0]	LO_DOUBLER_BAND_LUT_B_0								0x00	R/W
…	…	…	…								…	…
0xC33	REG0C33	[7:0]	RESERVED				LO_X4_FILTER_LUT_B_31				0x00	R/W
0xC34	REG0C34	[7:0]	RESERVED			LO_X3_FILTER_LUT_B_31					0x00	R/W
0xC35	REG0C35	[7:0]	RESERVED			LO_X1_FILTER_LUT_B_31					0x00	R/W
0xC36	REG0C36	[7:0]	RESERVED		GPO_F_LUT_B_31						0x00	R/W
0xC37	REG0C37	[7:0]	LO_TRAP_FILTER_LUT_B_31[7:0]								0x00	R/W
0xC38	REG0C38	[7:0]	RF_BAND_SELECT_LUT_B_31	LO_PHASE_Q_LUT_B_31					LO_TRAP_FILTER_LUT_B_31[9:8]		0x00	R/W
0xC39	REG0C39	[7:0]	LO_BAND_LUT_B_31	MIXER_BAND_LUT_B_31	LO_SIDE-BAND_LUT_B_31	LO_PHASE_I_LUT_B_31					0x00	R/W

REGISTER SUMMARY

Table 22. ADMV1355 Register Summary (Continued)

Reg	Name	Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset	Access
0xC3B	REG0C3B	[7:0]	LON_OFFSET_I_LUT_B_31								0x00	R/W
0xC3C	REG0C3C	[7:0]	LON_OFFSET_Q_LUT_B_31								0x00	R/W
0xC3D	REG0C3D	[7:0]	DSAQ_LUT_B_31				DSAI_LUT_B_31				0x00	R/W
0xC3E	REG0C3E	[7:0]	HPF_VALUE_LUT_B_31				LPF_VALUE_LUT_B_31				0x00	R/W
0xC3F	REG0C3F	[7:0]	LO_DOUBLER_BAND_LUT_B_31								0x00	R/W
0xE00	REG0E00	[7:0]	RF_DSA2_GAIN_LUT_0				RF_DSA1_GAIN_LUT_0				0x00	R/W
0xE01	REG0E01	[7:0]	RESERVED			GPO_G_LUT_0					0x00	R/W
…	…	…	…								…	…
0xE84	REG0E84	[7:0]	RF_DSA2_GAIN_LUT_66				RF_DSA1_GAIN_LUT_66				0x00	R/W
0xE85	REG0E85	[7:0]	RESERVED			GPO_G_LUT_66					0x00	R/W

REGISTER DETAILS

REGISTER 0X000 TO REGISTER 0X13E

Address: 0x000, Reset: 0x00, Name: REG0000

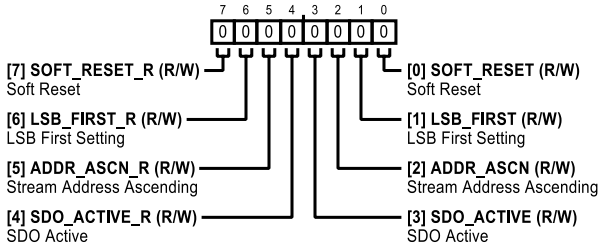


Figure 195.

Table 23. Bit Descriptions for REG0000

Bits	Bit Name	Description	Reset	Access
7	SOFT_RESET_R	Soft Reset. This bit field will self reset to zero; no need to set to zero after initiating a reset. 0: Reset Not Asserted. 1: Reset Asserted.	0x0	R/W
6	LSB_FIRST_R	LSB First Setting. 0: MSB First. 1: LSB First.	0x0	R/W
5	ADDR_ASCN_R	Stream Address Ascending. 0: Disable. 1: Enable.	0x0	R/W
4	SDO_ACTIVE_R	SDO Active. 0: Enable 3-wire SPI. 1: Enable 4-wire SPI.	0x0	R/W
3	SDO_ACTIVE	SDO Active. 0: Enable 3-wire SPI. 1: Enable 4-wire SPI.	0x0	R/W
2	ADDR_ASCN	Stream Address Ascending. 0: Disable. 1: Enable.	0x0	R/W
1	LSB_FIRST	LSB First Setting. 0: MSB First. 1: LSB First.	0x0	R/W
0	SOFT_RESET	Soft Reset. This bit field will self reset to zero; no need to set to zero after initiating a reset. 0: Reset Not Asserted. 1: Reset Asserted.	0x0	R/W

Address: 0x004, Reset: 0x00, Name: REG0004

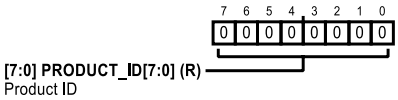


Figure 196.

Table 24. Bit Descriptions for REG0004

Bits	Bit Name	Description	Reset	Access
[7:0]	PRODUCT_ID[7:0]	Product ID.	0x0	R

REGISTER DETAILS

Address: 0x005, Reset: 0x00, Name: REG0005

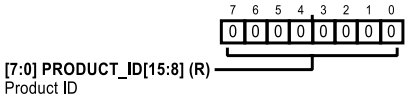


Figure 197.

Table 25. Bit Descriptions for REG0005

Bits	Bit Name	Description	Reset	Access
[7:0]	PRODUCT_ID[15:8]	Product ID.	0x0	R

Address: 0x00A, Reset: 0x00, Name: REG000A

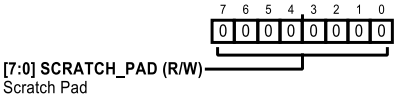


Figure 198.

Table 26. Bit Descriptions for REG000A

Bits	Bit Name	Description	Reset	Access
[7:0]	SCRATCH_PAD	Scratch Pad.	0x0	R/W

Address: 0x078, Reset: 0x09, Name: REG0078

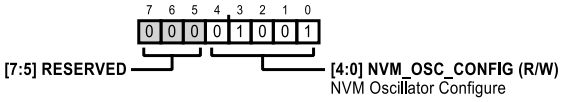


Figure 199.

Table 27. Bit Descriptions for REG0078

Bits	Bit Name	Description	Reset	Access
[7:5]	RESERVED	Reserved.	0x0	R
[4:0]	NVM_OSC_CONFIG	NVM Oscillator Configure.	0x9	R/W

Address: 0x07B, Reset: 0x00, Name: REG007B

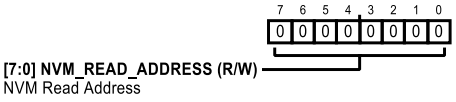


Figure 200.

Table 28. Bit Descriptions for REG007B

Bits	Bit Name	Description	Reset	Access
[7:0]	NVM_READ_ADDRESS	NVM Read Address. This bit field defines a pointer to the NVM register address that is read back when performing a read operation of NVM_READ_DATA. Applicable NVM register addresses to read back from are 0x33 to 0x38.	0x0	R/W

Address: 0x07C, Reset: 0x00, Name: REG007C

REGISTER DETAILS

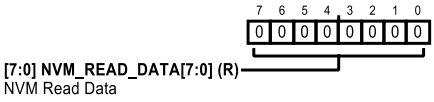


Figure 201.

Table 29. Bit Descriptions for REG007C

Bits	Bit Name	Description	Reset	Access
[7:0]	NVM_READ_DATA[7:0]	NVM Read Data. Set NVM_READ_ADDRESS to the NVM address to be read back, then perform a read operation of NVM_READ_DATA to retrieve the value.	0x0	R

Address: 0x07D, Reset: 0x00, Name: REG007D

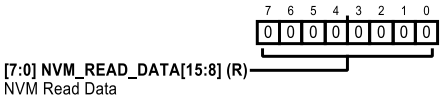


Figure 202.

Table 30. Bit Descriptions for REG007D

Bits	Bit Name	Description	Reset	Access
[7:0]	NVM_READ_DATA[15:8]	NVM Read Data. Set NVM_READ_ADDRESS to the NVM address to be read back, then perform a read operation of NVM_READ_DATA to retrieve the value.	0x0	R

Address: 0x07E, Reset: 0x68, Name: REG007E

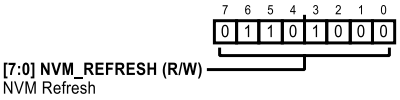


Figure 203.

Table 31. Bit Descriptions for REG007E

Bits	Bit Name	Description	Reset	Access
[7:0]	NVM_REFRESH	NVM Refresh.	0x68	R/W

Address: 0x13E, Reset: 0x00, Name: REG013E

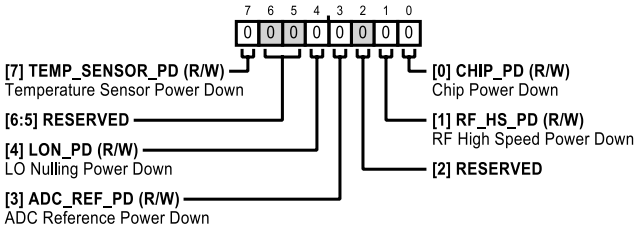


Figure 204.

Table 32. Bit Descriptions for REG013E

Bits	Bit Name	Description	Reset	Access
7	TEMP_SENSOR_PD	Temperature Sensor Power Down. 0: Normal Operation. 1: Power Down.	0x0	R/W
[6:5]	RESERVED	Reserved.	0x0	R/W
4	LON_PD	LO Nulling Power Down.	0x0	R/W

REGISTER DETAILS

Table 32. Bit Descriptions for REG013E (Continued)

Bits	Bit Name	Description	Reset	Access
		0: Normal Operation. 1: Power Down.		
3	ADC_REF_PD	ADC Reference Power Down. Power down this bit, when powering down the LO nulling circuit by using LON_PD. 0: Normal Operation. 1: Power Down.	0x0	R/W
2	RESERVED	Reserved.	0x0	R
1	RF_HS_PD	RF High Speed Power Down. When this bit is set, the unused band will automatically power down. 0: Normal Operation. 1: Power Down.	0x0	R/W
0	CHIP_PD	Chip Power Down. 0: Normal Operation. 1: Power Down.	0x0	R/W

REGISTER 0X200 TO REGISTER 0X2B0

Address: 0x200, Reset: 0x01, Name: REG0200

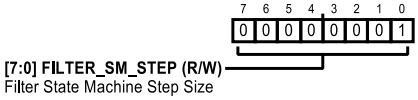


Figure 205.

Table 33. Bit Descriptions for REG0200

Bits	Bit Name	Description	Reset	Access
[7:0]	FILTER_SM_STEP	Filter State Machine Step Size. This twos complement value determines how much the filter state machine is incremented or decremented. A step size of zero is invalid.	0x1	R/W

Address: 0x202, Reset: 0x00, Name: REG0202

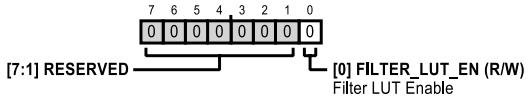


Figure 206.

Table 34. Bit Descriptions for REG0202

Bits	Bit Name	Description	Reset	Access
[7:1]	RESERVED	Reserved.	0x0	R
0	FILTER_LUT_EN	Filter LUT Enable. When disabled, filter settings defined using Register 0x800 to Register 0x80C. When enabled, filter settings are dependent upon the LUT, that is, set using Register 0x900 to Register 0xC3F. 0: Disable. 1: Enable.	0x0	R/W

Address: 0x203, Reset: 0x00, Name: REG0203

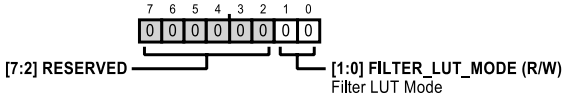


Figure 207.

REGISTER DETAILS

Table 35. Bit Descriptions for REG0203

Bits	Bit Name	Description	Reset	Access
[7:2]	RESERVED	Reserved.	0x0	R
[1:0]	FILTER_LUT_MODE	Filter LUT Mode. 00: LUT pointer selected by using the ADD_F balls. 01: LUT pointer selected by using Register 0x209 (FILTER_SPI_POINTER). 10: LUT pointer is incremented or decremented on rising edge of ADD_F4.	0x0	R/W

Address: 0x204, Reset: 0x01, Name: REG0204

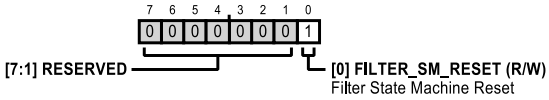


Figure 208.

Table 36. Bit Descriptions for REG0204

Bits	Bit Name	Description	Reset	Access
[7:1]	RESERVED	Reserved.	0x0	R
0	FILTER_SM_RESET	Filter State Machine Reset. Active low reset. Set this bit field to 0 and then to 1 to reset the state machine to 0. When this bit field is kept at 0, the state machine remains at 0. 0: Reset Address Pointer to Zero. 1: Normal Operation.	0x1	R/W

Address: 0x205, Reset: 0x00, Name: REG0205

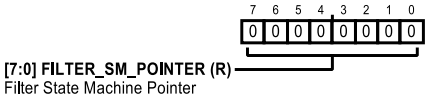


Figure 209.

Table 37. Bit Descriptions for REG0205

Bits	Bit Name	Description	Reset	Access
[7:0]	FILTER_SM_POINTER	Filter State Machine Pointer.	0x0	R

Address: 0x206, Reset: 0x1F, Name: REG0206

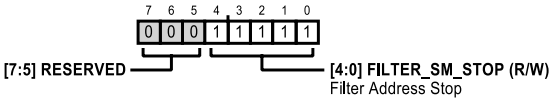


Figure 210.

Table 38. Bit Descriptions for REG0206

Bits	Bit Name	Description	Reset	Access
[7:5]	RESERVED	Reserved.	0x0	R
[4:0]	FILTER_SM_STOP	Filter State Machine Stop.	0x1F	R/W

Address: 0x207, Reset: 0x00, Name: REG0207

REGISTER DETAILS

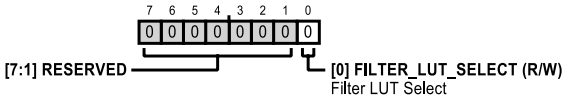


Figure 211.

Table 39. Bit Descriptions for REG0207

Bits	Bit Name	Description	Reset	Access
[7:1]	RESERVED	Reserved.	0x0	R
0	FILTER_LUT_SELECT	Filter LUT Select. 0: Table A. 1: Table B.	0x0	R/W

Address: 0x208, Reset: 0x00, Name: REG0208

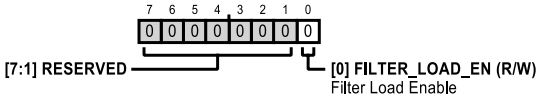


Figure 212.

Table 40. Bit Descriptions for REG0208

Bits	Bit Name	Description	Reset	Access
[7:1]	RESERVED	Reserved.	0x0	R
0	FILTER_LOAD_EN	Filter Load Enable. When disabled, the filter values are applied immediately. When enabled, the filter values are applied upon the rising edge of the LOAD ball. 0: Disable. 1: Enable.	0x0	R/W

Address: 0x209, Reset: 0x00, Name: REG0209

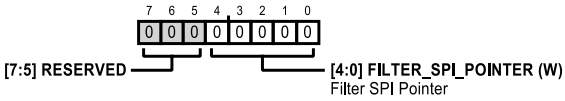


Figure 213.

Table 41. Bit Descriptions for REG0209

Bits	Bit Name	Description	Reset	Access
[7:5]	RESERVED	Reserved.	0x0	R
[4:0]	FILTER_SPI_POINTER	Filter SPI Pointer.	0x0	W

Address: 0x20A, Reset: 0x00, Name: REG020A

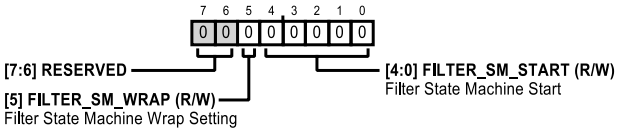


Figure 214.

Table 42. Bit Descriptions for REG020A

Bits	Bit Name	Description	Reset	Access
[7:6]	RESERVED	Reserved.	0x0	R

REGISTER DETAILS

Table 42. Bit Descriptions for REG020A (Continued)

Bits	Bit Name	Description	Reset	Access
5	FILTER_SM_WRAP	Filter State Machine Wrap Setting.	0x0	R/W
[4:0]	FILTER_SM_START	Filter State Machine Start.	0x0	R/W

Address: 0x210, Reset: 0x00, Name: REG0210

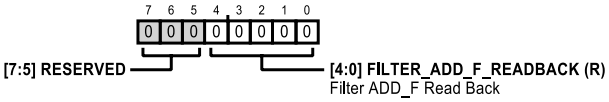


Figure 215.

Table 43. Bit Descriptions for REG0210

Bits	Bit Name	Description	Reset	Access
[7:5]	RESERVED	Reserved.	0x0	R
[4:0]	FILTER_ADD_F_READBACK	Filter ADD_F Read Back.	0x0	R

Address: 0x211, Reset: 0x00, Name: REG0211

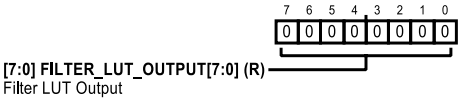


Figure 216.

Table 44. Bit Descriptions for REG0211

Bits	Bit Name	Description	Reset	Access
[7:0]	FILTER_LUT_OUTPUT[7:0]	Filter LUT Output. This bit field represents the filter values as determined by the LUT prior to the mux controlled by Register 0x202 and the LOAD feature.	0x0	R

Address: 0x212, Reset: 0x00, Name: REG0212

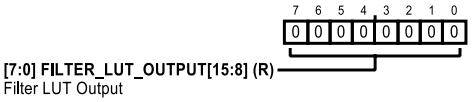


Figure 217.

Table 45. Bit Descriptions for REG0212

Bits	Bit Name	Description	Reset	Access
[7:0]	FILTER_LUT_OUTPUT[15:8]	Filter LUT Output. This bit field represents the filter values as determined by the LUT prior to the mux controlled by Register 0x202 and the LOAD feature.	0x0	R

Address: 0x213, Reset: 0x00, Name: REG0213

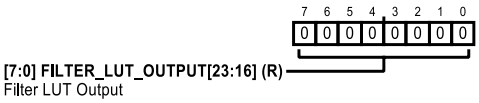


Figure 218.

REGISTER DETAILS

Table 46. Bit Descriptions for REG0213

Bits	Bit Name	Description	Reset	Access
[7:0]	FILTER_LUT_OUTPUT[23:16]	Filter LUT Output. This bit field represents the filter values as determined by the LUT prior to the mux controlled by Register 0x202 and the LOAD feature.	0x0	R

Address: 0x214, Reset: 0x00, Name: REG0214

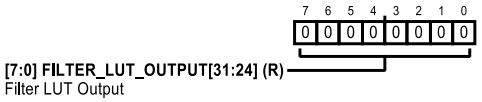


Figure 219.

Table 47. Bit Descriptions for REG0214

Bits	Bit Name	Description	Reset	Access
[7:0]	FILTER_LUT_OUTPUT[31:24]	Filter LUT Output. This bit field represents the filter values as determined by the LUT prior to the mux controlled by Register 0x202 and the LOAD feature.	0x0	R

Address: 0x215, Reset: 0x00, Name: REG0215

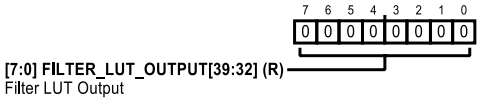


Figure 220.

Table 48. Bit Descriptions for REG0215

Bits	Bit Name	Description	Reset	Access
[7:0]	FILTER_LUT_OUTPUT[39:32]	Filter LUT Output. This bit field represents the filter values as determined by the LUT prior to the mux controlled by Register 0x202 and the LOAD feature.	0x0	R

Address: 0x216, Reset: 0x00, Name: REG0216

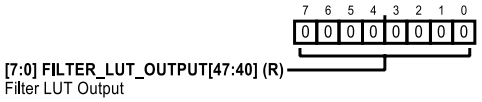


Figure 221.

Table 49. Bit Descriptions for REG0216

Bits	Bit Name	Description	Reset	Access
[7:0]	FILTER_LUT_OUTPUT[47:40]	Filter LUT Output. This bit field represents the filter values as determined by the LUT prior to the mux controlled by Register 0x202 and the LOAD feature.	0x0	R

Address: 0x217, Reset: 0x00, Name: REG0217

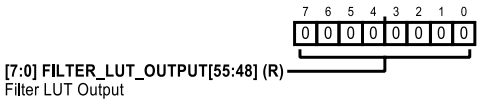


Figure 222.

REGISTER DETAILS

Table 50. Bit Descriptions for REG0217

Bits	Bit Name	Description	Reset	Access
[7:0]	FILTER_LUT_OUTPUT[55:48]	Filter LUT Output. This bit field represents the filter values as determined by the LUT prior to the mux controlled by Register 0x202 and the LOAD feature.	0x0	R

Address: 0x218, Reset: 0x00, Name: REG0218

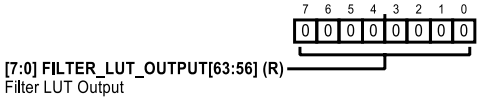


Table 51. Bit Descriptions for REG0218

Bits	Bit Name	Description	Reset	Access
[7:0]	FILTER_LUT_OUTPUT[63:56]	Filter LUT Output. This bit field represents the filter values as determined by the LUT prior to the mux controlled by Register 0x202 and the LOAD feature.	0x0	R

Address: 0x219, Reset: 0x00, Name: REG0219

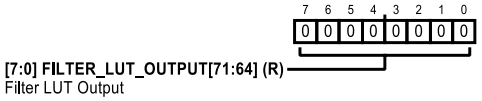


Figure 223.

Table 52. Bit Descriptions for REG0219

Bits	Bit Name	Description	Reset	Access
[7:0]	FILTER_LUT_OUTPUT[71:64]	Filter LUT Output. This bit field represents the filter values as determined by the LUT prior to the mux controlled by Register 0x202 and the LOAD feature.	0x0	R

Address: 0x21A, Reset: 0x00, Name: REG021A

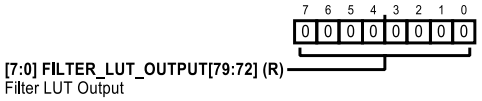


Figure 224.

Table 53. Bit Descriptions for REG021A

Bits	Bit Name	Description	Reset	Access
[7:0]	FILTER_LUT_OUTPUT[79:72]	Filter LUT Output. This bit field represents the filter values as determined by the LUT prior to the mux controlled by Register 0x202 and the LOAD feature.	0x0	R

Address: 0x21B, Reset: 0x00, Name: REG021B

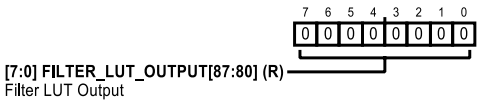


Figure 225.

Table 54. Bit Descriptions for REG021B

Bits	Bit Name	Description	Reset	Access
[7:0]	FILTER_LUT_OUTPUT[87:80]	Filter LUT Output. This bit field represents the filter values as determined by the LUT prior to the mux controlled by Register 0x202 and the LOAD feature.	0x0	R

REGISTER DETAILS

Address: 0x21C, Reset: 0x00, Name: REG021C

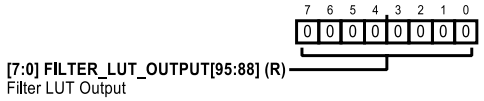


Figure 226.

Table 55. Bit Descriptions for REG021C

Bits	Bit Name	Description	Reset	Access
[7:0]	FILTER_LUT_OUTPUT[95:88]	Filter LUT Output. This bit field represents the filter values as determined by the LUT prior to the mux controlled by Register 0x202 and the LOAD feature.	0x0	R

Address: 0x21D, Reset: 0x00, Name: REG021D

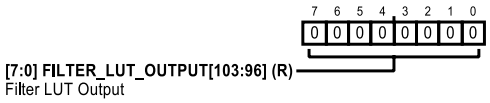


Figure 227.

Table 56. Bit Descriptions for REG021D

Bits	Bit Name	Description	Reset	Access
[7:0]	FILTER_LUT_OUTPUT[103:96]	Filter LUT Output. This bit field represents the filter values as determined by the LUT prior to the mux controlled by Register 0x202 and the LOAD feature.	0x0	R

Address: 0x220, Reset: 0x00, Name: REG0220

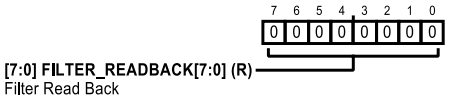


Figure 228.

Table 57. Bit Descriptions for REG0220

Bits	Bit Name	Description	Reset	Access
[7:0]	FILTER_READBACK[7:0]	Filter Read Back. This bit field represents the final value applied to the filters.	0x0	R

Address: 0x221, Reset: 0x00, Name: REG0221

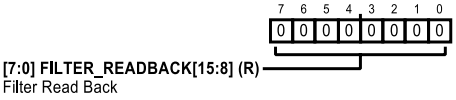


Figure 229.

Table 58. Bit Descriptions for REG0221

Bits	Bit Name	Description	Reset	Access
[7:0]	FILTER_READBACK[15:8]	Filter Read Back. This bit field represents the final value applied to the filters.	0x0	R

Address: 0x222, Reset: 0x00, Name: REG0222

REGISTER DETAILS

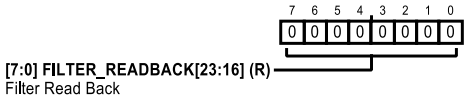


Figure 230.

Table 59. Bit Descriptions for REG0222

Bits	Bit Name	Description	Reset	Access
[7:0]	FILTER_READBACK[23:16]	Filter Read Back. This bit field represents the final value applied to the filters.	0x0	R

Address: 0x223, Reset: 0x00, Name: REG0223

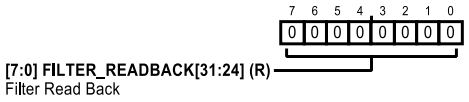


Figure 231.

Table 60. Bit Descriptions for REG0223

Bits	Bit Name	Description	Reset	Access
[7:0]	FILTER_READBACK[31:24]	Filter Read Back. This bit field represents the final value applied to the filters.	0x0	R

Address: 0x224, Reset: 0x00, Name: REG0224

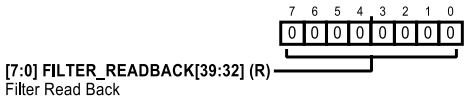


Figure 232.

Table 61. Bit Descriptions for REG0224

Bits	Bit Name	Description	Reset	Access
[7:0]	FILTER_READBACK[39:32]	Filter Read Back. This bit field represents the final value applied to the filters.	0x0	R

Address: 0x225, Reset: 0x00, Name: REG0225

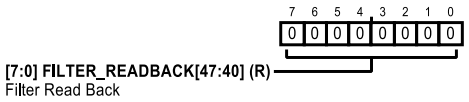


Figure 233.

Table 62. Bit Descriptions for REG0225

Bits	Bit Name	Description	Reset	Access
[7:0]	FILTER_READBACK[47:40]	Filter Read Back. This bit field represents the final value applied to the filters.	0x0	R

Address: 0x226, Reset: 0x00, Name: REG0226

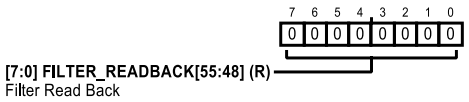


Figure 234.

REGISTER DETAILS

Table 63. Bit Descriptions for REG0226

Bits	Bit Name	Description	Reset	Access
[7:0]	FILTER_READBACK[55:48]	Filter Read Back. This bit field represents the final value applied to the filters.	0x0	R

Address: 0x227, Reset: 0x00, Name: REG0227

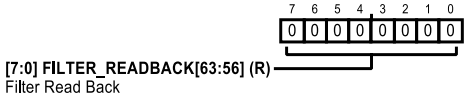


Figure 235.

Table 64. Bit Descriptions for REG0227

Bits	Bit Name	Description	Reset	Access
[7:0]	FILTER_READBACK[63:56]	Filter Read Back. This bit field represents the final value applied to the filters.	0x0	R

Address: 0x228, Reset: 0x00, Name: REG0228

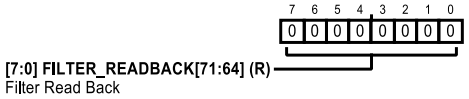


Figure 236.

Table 65. Bit Descriptions for REG0228

Bits	Bit Name	Description	Reset	Access
[7:0]	FILTER_READBACK[71:64]	Filter Read Back. This bit field represents the final value applied to the filters.	0x0	R

Address: 0x229, Reset: 0x00, Name: REG0229

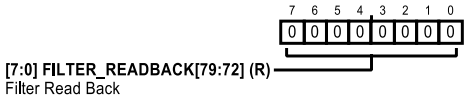


Table 66. Bit Descriptions for REG0229

Bits	Bit Name	Description	Reset	Access
[7:0]	FILTER_READBACK[79:72]	Filter Read Back. This bit field represents the final value applied to the filters.	0x0	R

Address: 0x22A, Reset: 0x00, Name: REG022A

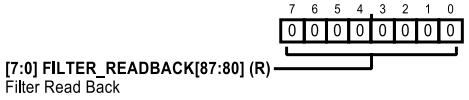


Figure 237.

Table 67. Bit Descriptions for REG022A

Bits	Bit Name	Description	Reset	Access
[7:0]	FILTER_READBACK[87:80]	Filter Read Back. This bit field represents the final value applied to the filters.	0x0	R

Address: 0x22B, Reset: 0x00, Name: REG022B

REGISTER DETAILS

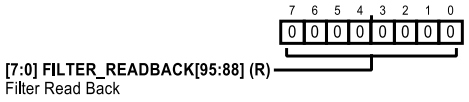


Figure 238.

Table 68. Bit Descriptions for REG022B

Bits	Bit Name	Description	Reset	Access
[7:0]	FILTER_READBACK[95:88]	Filter Read Back. This bit field represents the final value applied to the filters.	0x0	R

Address: 0x22C, Reset: 0x00, Name: REG022C

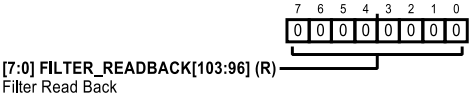


Figure 239.

Table 69. Bit Descriptions for REG022C

Bits	Bit Name	Description	Reset	Access
[7:0]	FILTER_READBACK[103:96]	Filter Read Back. This bit field represents the final value applied to the filters.	0x0	R

Address: 0x240, Reset: 0x00, Name: REG0240

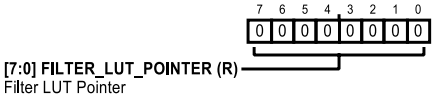


Figure 240.

Table 70. Bit Descriptions for REG0240

Bits	Bit Name	Description	Reset	Access
[7:0]	FILTER_LUT_POINTER	Filter LUT Pointer. This bit field represents the index pointer for the filter LUT after the mux that is controlled by Register 0x203.	0x0	R

Address: 0x281, Reset: 0x00, Name: REG0281

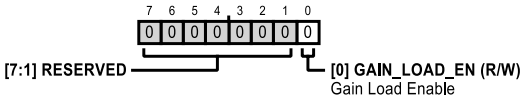


Figure 241.

Table 71. Bit Descriptions for REG0281

Bits	Bit Name	Description	Reset	Access
[7:1]	RESERVED	Reserved.	0x0	R
0	GAIN_LOAD_EN	Gain Load Enable. When disabled, the gain values are applied immediately. When enabled, the gain values are applied upon the rising edge of the LOAD ball. 0: Disable. 1: Enable.	0x0	R/W

Address: 0x282, Reset: 0x00, Name: REG0282

REGISTER DETAILS

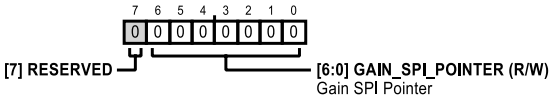


Figure 242.

Table 72. Bit Descriptions for REG0282

Bits	Bit Name	Description	Reset	Access
7	RESERVED	Reserved.	0x0	R
[6:0]	GAIN_SPI_POINTER	Gain SPI Pointer.	0x0	R/W

Address: 0x283, Reset: 0x01, Name: REG0283

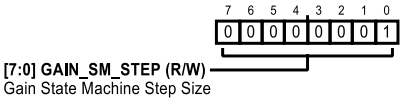


Figure 243.

Table 73. Bit Descriptions for REG0283

Bits	Bit Name	Description	Reset	Access
[7:0]	GAIN_SM_STEP	Gain State Machine Step Size. This twos complement value determines how much the gain state machine is incremented or decremented. A step size of zero is invalid.	0x1	R/W

Address: 0x284, Reset: 0x00, Name: REG0284

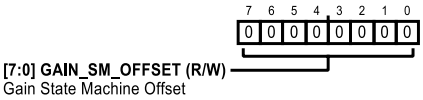


Figure 244.

Table 74. Bit Descriptions for REG0284

Bits	Bit Name	Description	Reset	Access
[7:0]	GAIN_SM_OFFSET	Gain State Machine Offset. This twos complement value determines how much the state machine output will be offset.	0x0	R/W

Address: 0x285, Reset: 0x01, Name: REG0285

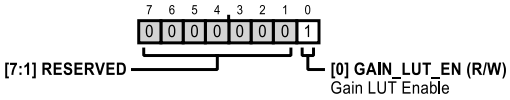


Figure 245.

Table 75. Bit Descriptions for REG0285

Bits	Bit Name	Description	Reset	Access
[7:1]	RESERVED	Reserved.	0x0	R
0	GAIN_LUT_EN	Gain LUT Enable. When disabled, filter settings defined using Register 0x600 to Register 0x602. When enabled, gain settings are dependent upon the LUT, that is set using Registers 0xE00 to Register 0xE85. 0: Disable. 1: Enable.	0x1	R/W

Address: 0x286, Reset: 0x00, Name: REG0286

REGISTER DETAILS

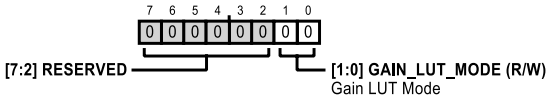


Figure 246.

Table 76. Bit Descriptions for REG0286

Bits	Bit Name	Description	Reset	Access
[7:2]	RESERVED	Reserved.	0x0	R
[1:0]	GAIN_LUT_MODE	Gain LUT Mode. 00: LUT pointer selected by using the ADD_G balls. 01: LUT pointer selected by using Register 0x282 (GAIN_SPI_POINTER). 10: LUT pointer is incremented or decremented on rising edge of ADD_G5.	0x0	R/W

Address: 0x287, Reset: 0x01, Name: REG0287

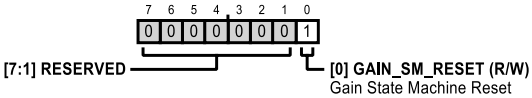


Figure 247.

Table 77. Bit Descriptions for REG0287

Bits	Bit Name	Description	Reset	Access
[7:1]	RESERVED	Reserved.	0x0	R
0	GAIN_SM_RESET	Gain State Machine Reset. Active low reset. Set this bit field to 0 and then to 1 to reset the state machine to 0. When this bit field is kept at 0, the state machine remains at 0. 0: Reset Address Pointer to Zero. 1: Normal Operation.	0x1	R/W

Address: 0x288, Reset: 0x00, Name: REG0288



Figure 248.

Table 78. Bit Descriptions for REG0288

Bits	Bit Name	Description	Reset	Access
[7:0]	GAIN_SM_POINTER_PLUS_OFFSET	Gain State Machine Pointer Plus Offset.	0x0	R

Address: 0x289, Reset: 0x42, Name: REG0289

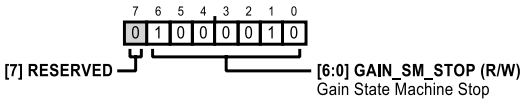


Figure 249.

Table 79. Bit Descriptions for REG0289

Bits	Bit Name	Description	Reset	Access
7	RESERVED	Reserved.	0x0	R
[6:0]	GAIN_SM_STOP	Gain State Machine Stop.	0x42	R/W

REGISTER DETAILS

Address: 0x28A, Reset: 0x00, Name: REG028A

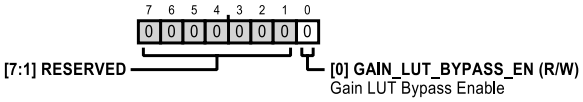


Figure 250.

Table 80. Bit Descriptions for REG028A

Bits	Bit Name	Description	Reset	Access
[7:1]	RESERVED	Reserved.	0x0	R
0	GAIN_LUT_BYPASS_EN	Gain LUT Bypass Enable. When enabled, gain and GPO_G values are set using Register 0x28B and Register 0x28C. 0: Disable. 1: Enable.	0x0	R/W

Address: 0x28B, Reset: 0x00, Name: REG028B

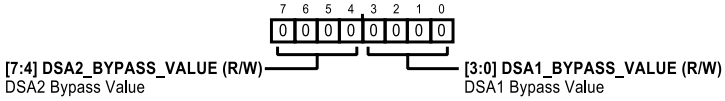


Figure 251.

Table 81. Bit Descriptions for REG028B

Bits	Bit Name	Description	Reset	Access
[7:4]	DSA2_BYPASS_VALUE	DSA2 Bypass Value. Where 0x0 is maximum gain, and 0xF is minimum gain.	0x0	R/W
[3:0]	DSA1_BYPASS_VALUE	DSA1 Bypass Value. Where 0x0 is maximum gain, and 0xF is minimum gain.	0x0	R/W

Address: 0x28C, Reset: 0x00, Name: REG028C

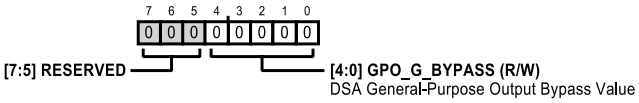


Figure 252.

Table 82. Bit Descriptions for REG028C

Bits	Bit Name	Description	Reset	Access
[7:5]	RESERVED	Reserved.	0x0	R
[4:0]	GPO_G_BYPASS	DSA General-Purpose Output Bypass Value.	0x0	R/W

Address: 0x28F, Reset: 0x00, Name: REG028F

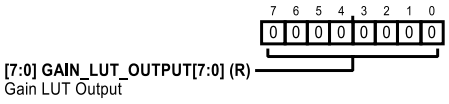


Figure 253.

Table 83. Bit Descriptions for REG028F

Bits	Bit Name	Description	Reset	Access
[7:0]	GAIN_LUT_OUTPUT[7:0]	Gain LUT Output. This bit field represents the gain values as determined by the LUT prior to the mux controlled by Register 0x285 and the LOAD feature.	0x0	R

REGISTER DETAILS

Address: 0x290, Reset: 0x00, Name: REG0290

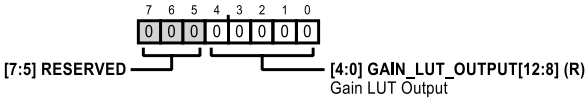


Figure 254.

Table 84. Bit Descriptions for REG0290

Bits	Bit Name	Description	Reset	Access
[7:5]	RESERVED	Reserved.	0x0	R
[4:0]	GAIN_LUT_OUTPUT[12:8]	Gain LUT Output. This bit field represents the gain values as determined by the LUT prior to the mux controlled by Register 0x285 and the LOAD feature.	0x0	R

Address: 0x293, Reset: 0x00, Name: REG0293

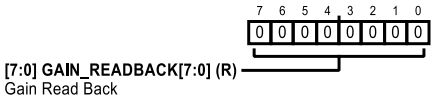


Figure 255.

Table 85. Bit Descriptions for REG0293

Bits	Bit Name	Description	Reset	Access
[7:0]	GAIN_READBACK[7:0]	Gain Read Back. This bit field represents the final value applied to the DSAs.	0x0	R

Address: 0x294, Reset: 0x00, Name: REG0294

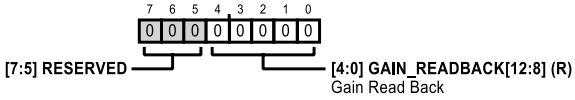


Figure 256.

Table 86. Bit Descriptions for REG0294

Bits	Bit Name	Description	Reset	Access
[7:5]	RESERVED	Reserved.	0x0	R
[4:0]	GAIN_READBACK[12:8]	Gain Read Back. This bit field represents the final value applied to the DSAs.	0x0	R

Address: 0x298, Reset: 0x00, Name: REG0298

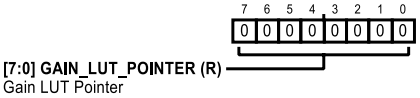


Figure 257.

Table 87. Bit Descriptions for REG0298

Bits	Bit Name	Description	Reset	Access
[7:0]	GAIN_LUT_POINTER	Gain LUT Pointer. This bit field represents the index pointer for the gain LUT after the mux that is controlled by Register 0x286.	0x0	R

Address: 0x29B, Reset: 0x00, Name: REG029B

REGISTER DETAILS



Figure 258.

Table 88. Bit Descriptions for REG029B

Bits	Bit Name	Description	Reset	Access
[7:0]	GAIN_SM_POINTER_PRE_OFFSET	Gain State Machine Pointer Pre Offset.	0x0	R

Address: 0x2A0, Reset: 0x00, Name: REG02A0

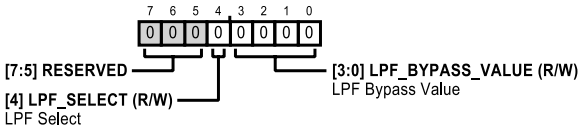


Figure 259.

Table 89. Bit Descriptions for REG02A0

Bits	Bit Name	Description	Reset	Access
[7:5]	RESERVED	Reserved.	0x0	R
4	LPF_SELECT	LPF Select. 0: Filter state determined from LUT or Register 0x800 to Register 0x80C. 1: Filter state determined from SPI (LPF_BYPASS_VALUE).	0x0	R/W
[3:0]	LPF_BYPASS_VALUE	LPF Bypass Value. Cutoff frequency is inversely proportional to this bit field value.	0x0	R/W

Address: 0x2A1, Reset: 0x3F, Name: REG02A1

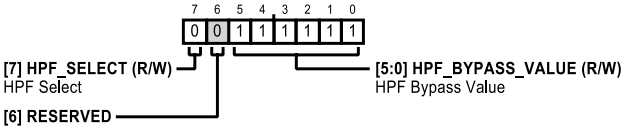


Figure 260.

Table 90. Bit Descriptions for REG02A1

Bits	Bit Name	Description	Reset	Access
7	HPF_SELECT	HPF Select. 0: Filter state determined from LUT or Register 0x800 to Register 0x80C. 1: Filter state determined from SPI (HPF_BYPASS_VALUE).	0x0	R/W
6	RESERVED	Reserved.	0x0	R/W
[5:0]	HPF_BYPASS_VALUE	HPF Bypass Value. Cutoff frequency is inversely proportional to this bit field value.	0x3F	R/W

Address: 0x2A3, Reset: 0x00, Name: REG02A3

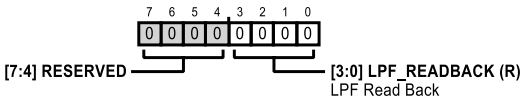


Figure 261.

REGISTER DETAILS

Table 91. Bit Descriptions for REG02A3

Bits	Bit Name	Description	Reset	Access
[7:4]	RESERVED	Reserved.	0x0	R
[3:0]	LPF_READBACK	LPF Read Back.	0x0	R

Address: 0x2A4, Reset: 0x00, Name: REG02A4

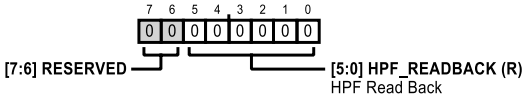


Figure 262.

Table 92. Bit Descriptions for REG02A4

Bits	Bit Name	Description	Reset	Access
[7:6]	RESERVED	Reserved.	0x0	R
[5:0]	HPF_READBACK	HPF Read Back.	0x0	R

Address: 0x2A7, Reset: 0x00, Name: REG02A7

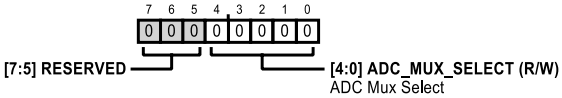


Figure 263.

Table 93. Bit Descriptions for REG02A7

Bits	Bit Name	Description	Reset	Access
[7:5]	RESERVED	Reserved.	0x0	R
[4:0]	ADC_MUX_SELECT	ADC Mux Select. 0: LO Nulling. 1: Temperature Sensor.	0x0	R/W

Address: 0x2B0, Reset: 0x00, Name: REG02B0

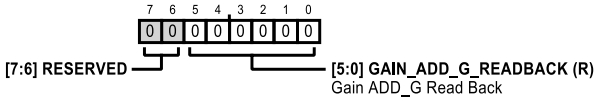


Figure 264.

Table 94. Bit Descriptions for REG02B0

Bits	Bit Name	Description	Reset	Access
[7:6]	RESERVED	Reserved.	0x0	R
[5:0]	GAIN_ADD_G_READBACK	Gain ADD_G Read Back.	0x0	R

REGISTER 0X300 TO REGISTER 0X402

Address: 0x300, Reset: 0x00, Name: REG0300

REGISTER DETAILS

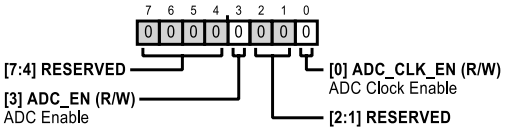


Figure 265.

Table 95. Bit Descriptions for REG0300

Bits	Bit Name	Description	Reset	Access
[7:4]	RESERVED	Reserved.	0x0	R
3	ADC_EN	ADC Enable. 0: Disable. 1: Enable.	0x0	R/W
[2:1]	RESERVED	Reserved.	0x0	R/W
0	ADC_CLK_EN	ADC Clock Enable. 0: Disable. 1: Enable.	0x0	R/W

Address: 0x302, Reset: 0x00, Name: REG0302

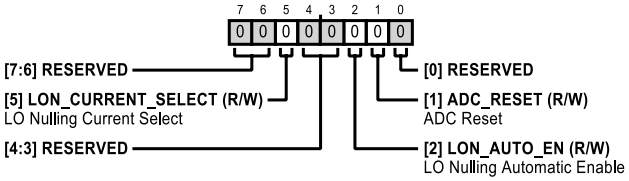


Figure 266.

Table 96. Bit Descriptions for REG0302

Bits	Bit Name	Description	Reset	Access
[7:6]	RESERVED	Reserved.	0x0	R
5	LON_CURRENT_SELECT	LO Nulling Current Select. 0: LO Nulling current determined automatically. 1: LO Nulling current set using Register 0x304 (LON_CURRENT).	0x0	R/W
[4:3]	RESERVED	Reserved.	0x0	R/W
2	LON_AUTO_EN	LO Nulling Automatic Enable. 0: Disable. 1: Enable.	0x0	R/W
1	ADC_RESET	ADC Reset. 0: Normal Operation. 1: Reset.	0x0	R/W
0	RESERVED	Reserved.	0x0	R

Address: 0x304, Reset: 0x14, Name: REG0304

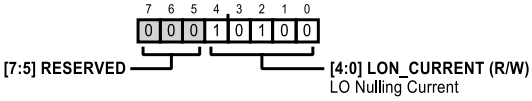


Figure 267.

REGISTER DETAILS

Table 97. Bit Descriptions for REG0304

Bits	Bit Name	Description	Reset	Access
[7:5]	RESERVED	Reserved.	0x0	R
[4:0]	LON_CURRENT	LO Nulling Current. The current is proportional to this bit field value. The recommended value for automatic LO nulling is 0x1F. This value can be tuned for best LO nulling results at different frequencies.	0x14	R/W

Address: 0x305, Reset: 0x00, Name: REG0305

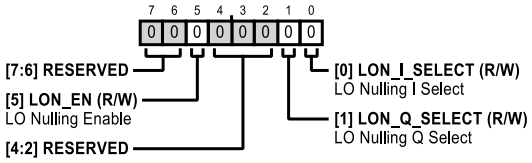


Figure 268.

Table 98. Bit Descriptions for REG0305

Bits	Bit Name	Description	Reset	Access
[7:6]	RESERVED	Reserved.	0x0	R
5	LON_EN	LO Nulling Enable. 0: Disable. 1: Enable.	0x0	R/W
[4:2]	RESERVED	Reserved.	0x0	R/W
1	LON_Q_SELECT	LO Nulling Q Select. 0: LO Nulling Q offset current determined automatically. 1: LO Nulling Q offset current set using Register 0x809 (LON_OFFSET_Q).	0x0	R/W
0	LON_I_SELECT	LO Nulling I Select. 0: LO Nulling I offset current determined automatically. 1: LO Nulling I offset current set using Register 0x808 (LON_OFFSET_I).	0x0	R/W

Address: 0x306, Reset: 0x00, Name: REG0306

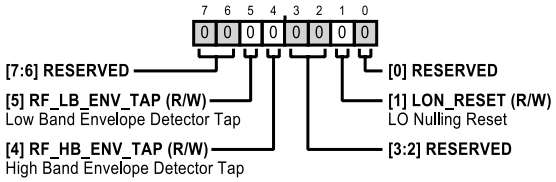


Figure 269.

Table 99. Bit Descriptions for REG0306

Bits	Bit Name	Description	Reset	Access
[7:6]	RESERVED	Reserved.	0x0	R
5	RF_LB_ENV_TAP	Low Band Envelope Detector Tap. 0: Disconnected. 1: Connected.	0x0	R/W
4	RF_HB_ENV_TAP	High Band Envelope Detector Tap. 0: Disconnected. 1: Connected.	0x0	R/W
[3:2]	RESERVED	Reserved.	0x0	R/W
1	LON_RESET	LO Nulling Reset. This bit field resets all the internal registers in the LO Nulling block.	0x0	R/W
0	RESERVED	Reserved.	0x0	R/W

REGISTER DETAILS

Address: 0x30D, Reset: 0x00, Name: REG030D

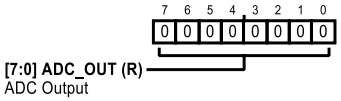


Figure 270.

Table 100. Bit Descriptions for REG030D

Bits	Bit Name	Description	Reset	Access
[7:0]	ADC_OUT	ADC Output.	0x0	R

Address: 0x402, Reset: 0x04, Name: REG0402

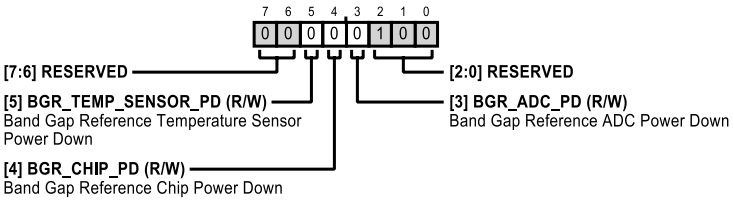


Figure 271.

Table 101. Bit Descriptions for REG0402

Bits	Bit Name	Description	Reset	Access
[7:6]	RESERVED	Reserved.	0x0	R
5	BGR_TEMP_SENSOR_PD	Band Gap Reference Temperature Sensor Power Down. 0: Normal Operation. 1: Power Down.	0x0	R/W
4	BGR_CHIP_PD	Band Gap Reference Chip Power Down. 0: Normal Operation. 1: Power Down.	0x0	R/W
3	BGR_ADC_PD	Band Gap Reference ADC Power Down. 0: Normal Operation. 1: Power Down.	0x0	R/W
[2:0]	RESERVED	Reserved.	0x0	R/W

REGISTER 0X600 TO REGISTER 0X80C

Address: 0x600, Reset: 0x00, Name: REG0600

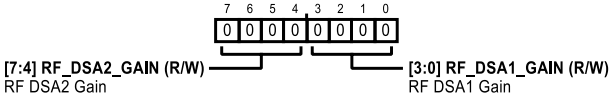


Figure 272.

Table 102. Bit Descriptions for REG0600

Bits	Bit Name	Description	Reset	Access
[7:4]	RF_DSA2_GAIN	RF DSA2 Gain. Provides gain range of 15dB with gain step of 1dB. 0000: 0dB. 0001: −1dB. 0010: −2dB. 0011: −3dB.	0x0	R/W

REGISTER DETAILS

Table 102. Bit Descriptions for REG0600 (Continued)

Bits	Bit Name	Description	Reset	Access
		0100: −4dB. 0101: −5dB. 0110: −6dB. 0111: −7dB. 1000: −8dB. 1001: −9dB. 1010: −10dB. 1011: −11dB. 1100: −12dB. 1101: −13dB. 1110: −14dB. 1111: −15dB.		
[3:0]	RF_DSA1_GAIN	RF DSA1 Gain. Provides gain range of 15dB with gain step of 1dB. 0000: 0dB. 0001: −1dB. 0010: −2dB. 0011: −3dB. 0100: −4dB. 0101: −5dB. 0110: −6dB. 0111: −7dB. 1000: −8dB. 1001: −9dB. 1010: −10dB. 1011: −11dB. 1100: −12dB. 1101: −13dB. 1110: −14dB. 1111: −15dB.	0x0	R/W

Address: 0x601, Reset: 0x00, Name: REG0601

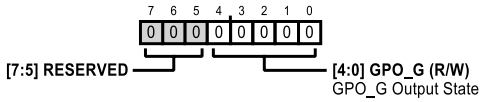


Figure 273.

Table 103. Bit Descriptions for REG0601

Bits	Bit Name	Description	Reset	Access
[7:5]	RESERVED	Reserved.	0x0	R
[4:0]	GPO_G	GPO_G Output State. Use this bit field to set the logic state of the GPO_G outputs	0x0	R/W

Address: 0x602, Reset: 0x08, Name: REG0602

REGISTER DETAILS

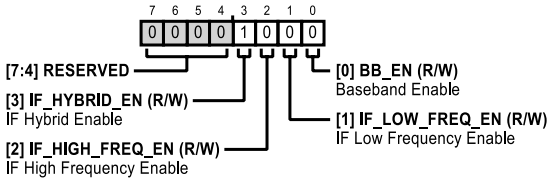


Figure 274.

Table 104. Bit Descriptions for REG0602

Bits	Bit Name	Description	Reset	Access
[7:4]	RESERVED	Reserved.	0x0	R
3	IF_HYBRID_EN	IF Hybrid Enable. Enable this bit field when using single-ended IF input. 0: Disable. 1: Enable.	0x1	R/W
2	IF_HIGH_FREQ_EN	IF High Frequency Enable. Enable this bit field when using high frequency 3GHz to 12GHz complex IF inputs. 0: Disable. 1: Enable.	0x0	R/W
1	IF_LOW_FREQ_EN	IF Low Frequency Enable. Enable this bit field when using low frequency 1GHz to 4GHz complex IF inputs. 0: Disable. 1: Enable.	0x0	R/W
0	BB_EN	Baseband Enable. Enable this bit field when using the baseband inputs. 0: Disable. 1: Enable.	0x0	R/W

Address: 0x700, Reset: 0x10, Name: REG0700

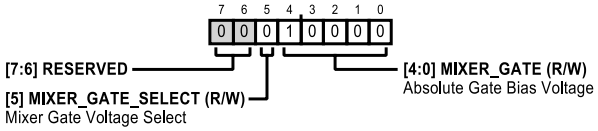


Figure 275.

Table 105. Bit Descriptions for REG0700

Bits	Bit Name	Description	Reset	Access
[7:6]	RESERVED	Reserved.	0x0	R
5	MIXER_GATE_SELECT	Mixer Gate Voltage Select. Automatic adjustment sets mixer gate voltage automatically if input common-mode voltage is below 0.5V. Manual adjustment is used to set mixer gate voltage if input common-mode voltage is above 0.5V. 0: Automatic Adjustment. 1: Manual Adjustment.	0x0	R/W
[4:0]	MIXER_GATE	Absolute Gate Bias Voltage. Sets the mixer gate voltage when MIXER_GATE_SELECT = 1. The gate voltage is computed as: VGATE = MIXER_GATE × 50mV.	0x10	R/W

Address: 0x702, Reset: 0x00, Name: REG0702

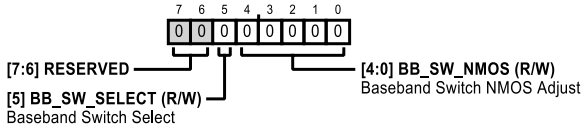


Figure 276.

REGISTER DETAILS

Table 106. Bit Descriptions for REG0702

Bits	Bit Name	Description	Reset	Access
[7:6]	RESERVED	Reserved.	0x0	R
5	BB_SW_SELECT	Baseband Switch Select. 0: Automatic Adjustment. 1: Manual Adjustment.	0x0	R/W
[4:0]	BB_SW_NMOS	Baseband Switch NMOS Adjust. Adjusts the NMOS devices in baseband switches for manual mixer gate adjustment mode when BB_SW_SELECT = 1.	0x0	R/W

Address: 0x703, Reset: 0x00, Name: REG0703

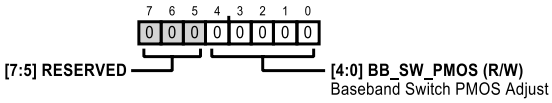


Figure 277.

Table 107. Bit Descriptions for REG0703

Bits	Bit Name	Description	Reset	Access
[7:5]	RESERVED	Reserved.	0x0	R
[4:0]	BB_SW_PMOS	Baseband Switch PMOS Adjust. Adjusts the PMOS devices in baseband switches for manual mixer gate adjustment mode when BB_SW_SELECT = 1.	0x0	R/W

Address: 0x780, Reset: 0x00, Name: REG0780

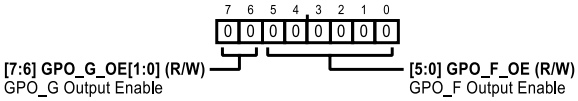


Figure 278.

Table 108. Bit Descriptions for REG0780

Bits	Bit Name	Description	Reset	Access
[7:6]	GPO_G_OE[1:0]	GPO_G Output Enable. This bit field enables the general-purpose output buffers. 0: Disable. 1: Enable.	0x0	R/W
[5:0]	GPO_F_OE	GPO_F Output Enable. 0: Disable. 1: Enable.	0x0	R/W

Address: 0x781, Reset: 0x00, Name: REG0781

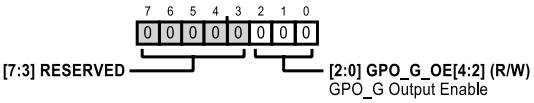


Figure 279.

Table 109. Bit Descriptions for REG0781

Bits	Bit Name	Description	Reset	Access
[7:3]	RESERVED	Reserved.	0x0	R
[2:0]	GPO_G_OE[4:2]	GPO_G Output Enable. This bit field enables the general-purpose output buffers. 0: Disable.	0x0	R/W

REGISTER DETAILS

Table 109. Bit Descriptions for REG0781 (Continued)

Bits	Bit Name	Description	Reset	Access
		1: Enable.		

Address: 0x800, Reset: 0x00, Name: REG0800

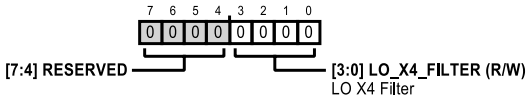


Figure 280.

Table 110. Bit Descriptions for REG0800

Bits	Bit Name	Description	Reset	Access
[7:4]	RESERVED	Reserved.	0x0	R/W
[3:0]	LO_X4_FILTER	LO ×4 Filter. 0000: 10GHz ≤ LO Frequency < 14GHz. 0101: 14GHz ≤ LO Frequency < 18GHz. 0111: LO Frequency ≥ 18GHz. 1000: LO Frequency < 10GHz.	0x0	R/W

Address: 0x801, Reset: 0x00, Name: REG0801

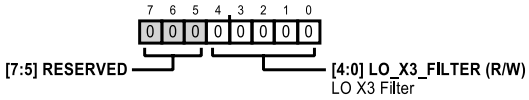


Figure 281.

Table 111. Bit Descriptions for REG0801

Bits	Bit Name	Description	Reset	Access
[7:5]	RESERVED	Reserved.	0x0	R
[4:0]	LO_X3_FILTER	LO ×3 Filter. 00000: LO Frequency ≥ 24GHz. 00010: 21GHz ≤ LO Frequency < 24GHz. 00011: 19GHz ≤ LO Frequency < 21GHz. 00100: 17GHz ≤ LO Frequency < 19GHz. 00101: 15GHz ≤ LO Frequency < 17GHz. 00111: 12GHz ≤ LO Frequency < 15GHz. 11100: LO Frequency < 12GHz.	0x0	R/W

Address: 0x802, Reset: 0x00, Name: REG0802

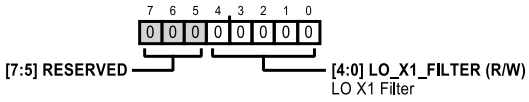


Figure 282.

Table 112. Bit Descriptions for REG0802

Bits	Bit Name	Description	Reset	Access
[7:5]	RESERVED	Reserved.	0x0	R
[4:0]	LO_X1_FILTER	LO ×1 Filter. 00000: LO Frequency ≥ 21GHz.	0x0	R/W

REGISTER DETAILS

Table 112. Bit Descriptions for REG0802 (Continued)

Bits	Bit Name	Description	Reset	Access
		00001: 17GHz ≤ LO Frequency < 21GHz. 00101: 15GHz ≤ LO Frequency < 17GHz. 01010: 12GHz ≤ LO Frequency < 15GHz. 11111: LO Frequency < 12GHz.		

Address: 0x803, Reset: 0x00, Name: REG0803

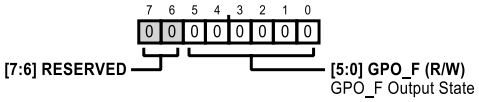


Figure 283.

Table 113. Bit Descriptions for REG0803

Bits	Bit Name	Description	Reset	Access
[7:6]	RESERVED	Reserved.	0x0	R
[5:0]	GPO_F	GPO_F Output State. Use this bit field to set the logic state of the GPO_F outputs.	0x0	R/W

Address: 0x804, Reset: 0x00, Name: REG0804



Figure 284.

Table 114. Bit Descriptions for REG0804

Bits	Bit Name	Description	Reset	Access
[7:0]	LO_TRAP_FILTER[7:0]	LO Trap Filter. 0x1E7: LO Frequency ≥ 21GHz. 0x1A7: 18.5GHz ≤ LO Frequency < 21.0GHz. 0x1A3: 14.5GHz ≤ LO Frequency < 18.5GHz. 0x3AA: 12.0GHz ≤ LO Frequency < 14.5GHz. 0x318: LO Frequency < 12GHz.	0x0	R/W

Address: 0x805, Reset: 0x40, Name: REG0805

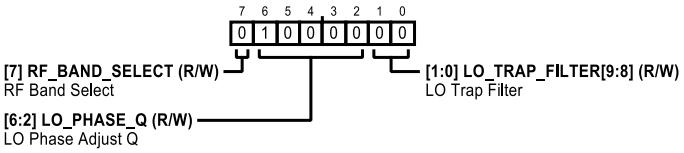


Figure 285.

Table 115. Bit Descriptions for REG0805

Bits	Bit Name	Description	Reset	Access
7	RF_BAND_SELECT	RF Band Select. 0: Low Band. 1: High Band.	0x0	R/W
[6:2]	LO_PHASE_Q	LO Phase Adjust Q. This bit field adjusts the phase of the Q path within the LO block. It can be used to calibrate the sideband rejection.	0x10	R/W

REGISTER DETAILS

Table 115. Bit Descriptions for REG0805 (Continued)

Bits	Bit Name	Description	Reset	Access
[1:0]	LO_TRAP_FILTER[9:8]	LO Trap Filter. 0x1E7: LO Frequency ≥ 21GHz. 0x1A7: 18.5GHz ≤ LO Frequency < 21.0GHz. 0x1A3: 14.5GHz ≤ LO Frequency < 18.5GHz. 0x3AA: 12.0GHz ≤ LO Frequency < 14.5GHz. 0x318: LO Frequency < 12GHz.	0x0	R/W

Address: 0x806, Reset: 0x30, Name: REG0806

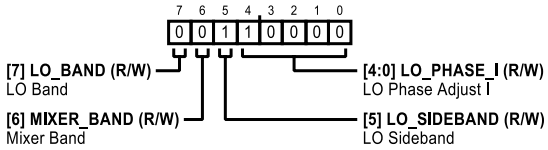


Figure 286.

Table 116. Bit Descriptions for REG0806

Bits	Bit Name	Description	Reset	Access
7	LO_BAND	LO Band. 0: Low Band. 1: High Band.	0x0	R/W
6	MIXER_BAND	Mixer Band. 0: Low Band. 1: High Band.	0x0	R/W
5	LO_SIDEBAND	LO Sideband. 0: LSB. 1: USB.	0x1	R/W
[4:0]	LO_PHASE_I	LO Phase Adjust I. This bit field adjusts the phase of the I path within the LO block. It can be used to calibrate the sideband rejection.	0x10	R/W

Address: 0x808, Reset: 0x00, Name: REG0808

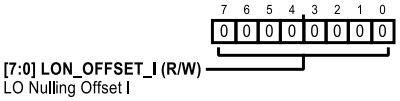


Figure 287.

Table 117. Bit Descriptions for REG0808

Bits	Bit Name	Description	Reset	Access
[7:0]	LON_OFFSET_I	LO Nulling Offset I. LO Nulling Offset I. This is a twos complement value, that determines the offset current. A value of 0x80 is the minimum negative current, a value of 0x00 is the zero current, and a value of 0x7F is the maximum positive current. Effective when LON_I_SELECT = 1.	0x0	R/W

Address: 0x809, Reset: 0x00, Name: REG0809

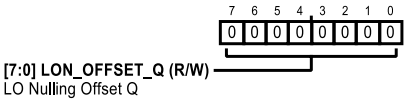


Figure 288.

REGISTER DETAILS

Table 118. Bit Descriptions for REG0809

Bits	Bit Name	Description	Reset	Access
[7:0]	LON_OFFSET_Q	LO Nulling Offset Q. LO Nulling Offset Q. This is a twos complement value, that determines the offset current. A value of 0x80 is the minimum negative current, a value of 0x00 is the zero current, and a value of 0x7F is the maximum positive current. Effective when LON_Q_SELECT = 1.	0x0	R/W

Address: 0x80A, Reset: 0x00, Name: REG080A

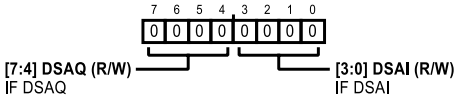


Figure 289.

Table 119. Bit Descriptions for REG080A

Bits	Bit Name	Description	Reset	Access
[7:4]	DSAQ	IF DSAQ. 1.5dB Range with 0.1dB Step, Used for Sideband Rejection Calibration.	0x0	R/W
[3:0]	DSAI	IF DSAI. 1.5dB Range with 0.1dB Step, Used for Sideband Rejection Calibration.	0x0	R/W

Address: 0x80B, Reset: 0x00, Name: REG080B

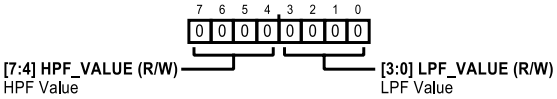


Figure 290.

Table 120. Bit Descriptions for REG080B

Bits	Bit Name	Description	Reset	Access
[7:4]	HPF_VALUE	HPF Value. Cutoff frequency is inversely proportional to this bit field value.	0x0	R/W
[3:0]	LPF_VALUE	LPF Value. Cutoff frequency is inversely proportional to this bit field value.	0x0	R/W

Address: 0x80C, Reset: 0x00, Name: REG080C

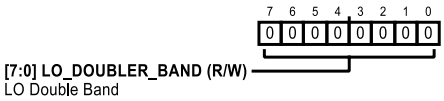


Figure 291.

Table 121. Bit Descriptions for REG080C

Bits	Bit Name	Description	Reset	Access
[7:0]	LO_DOUBLER_BAND	LO Double Band. 0xC0: LO Frequency ≥ 24GHz. 0x80: 18GHz ≤ LO Frequency < 24GHz. 0x08: 14GHz ≤ LO Frequency < 18GHz. 0x04: 12GHz ≤ LO Frequency < 14GHz. 0x1D: 10GHz ≤ LO Frequency < 12GHz. 0x1F: LO Frequency < 10GHz.	0x0	R/W

REGISTER 0X900 TO REGISTER 0XE01

Address: 0x900, Reset: 0x00, Name: REG0900

REGISTER DETAILS

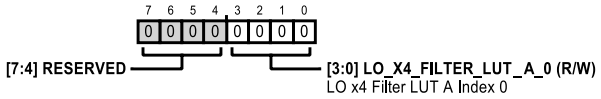


Figure 292.

Table 122. Bit Descriptions for REG0900

Bits	Bit Name	Description	Reset	Access
[7:4]	RESERVED	Reserved.	0x0	R/W
[3:0]	LO_X4_FILTER_LUT_A_0	LO ×4 Filter LUT A Index 0. 0000: 10GHz ≤ LO Frequency < 14GHz. 0101: 14GHz ≤ LO Frequency < 18GHz. 0111: LO Frequency ≥ 18GHz. 1000: LO Frequency < 10GHz.	0x0	R/W

Address: 0x901, Reset: 0x00, Name: REG0901

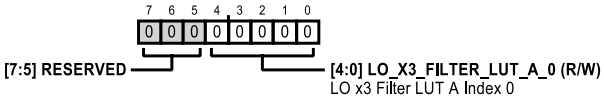


Figure 293.

Table 123. Bit Descriptions for REG0901

Bits	Bit Name	Description	Reset	Access
[7:5]	RESERVED	Reserved.	0x0	R
[4:0]	LO_X3_FILTER_LUT_A_0	LO ×3 Filter LUT A Index 0. 00000: LO Frequency ≥ 24GHz. 00010: 21GHz ≤ LO Frequency < 24GHz. 00011: 19GHz ≤ LO Frequency < 21GHz. 00100: 17GHz ≤ LO Frequency < 19GHz. 00101: 15GHz ≤ LO Frequency < 17GHz. 00111: 12GHz ≤ LO Frequency < 15GHz. 11100: LO Frequency < 12GHz.	0x0	R/W

Address: 0x902, Reset: 0x00, Name: REG0902

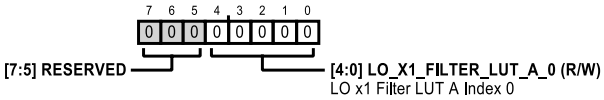


Figure 294.

Table 124. Bit Descriptions for REG0902

Bits	Bit Name	Description	Reset	Access
[7:5]	RESERVED	Reserved.	0x0	R
[4:0]	LO_X1_FILTER_LUT_A_0	LO ×1 Filter LUT A Index 0. 00000: LO Frequency ≥ 21GHz. 00001: 17GHz ≤ LO Frequency < 21GHz. 00101: 15GHz ≤ LO Frequency < 17GHz. 01010: 12GHz ≤ LO Frequency < 15GHz. 11111: LO Frequency < 12GHz.	0x0	R/W

REGISTER DETAILS

Address: 0x903, Reset: 0x00, Name: REG0903

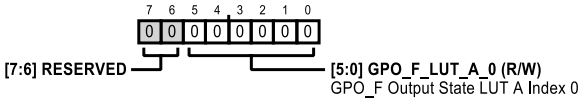


Figure 295.

Table 125. Bit Descriptions for REG0903

Bits	Bit Name	Description	Reset	Access
[7:6]	RESERVED	Reserved.	0x0	R
[5:0]	GPO_F_LUT_A_0	GPO_F Output State LUT A Index 0.	0x0	R/W

Address: 0x904, Reset: 0x00, Name: REG0904

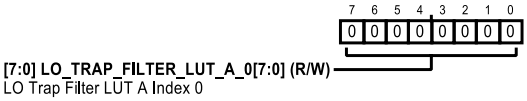


Figure 296.

Table 126. Bit Descriptions for REG0904

Bits	Bit Name	Description	Reset	Access
[7:0]	LO_TRAP_FILTER_LUT_A_0[7:0]	LO Trap Filter LUT A Index 0. 0x1E7: LO Frequency ≥ 21GHz. 0x1A7: 18.5GHz ≤ LO Frequency < 21.0GHz. 0x1A3: 14.5GHz ≤ LO Frequency < 18.5GHz. 0x3AA: 12.0GHz ≤ LO Frequency < 14.5GHz. 0x318: LO Frequency < 12GHz.	0x0	R/W

Address: 0x905, Reset: 0x00, Name: REG0905

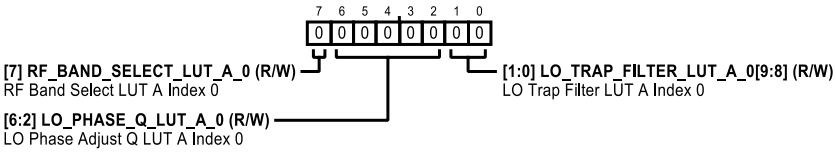


Figure 297.

Table 127. Bit Descriptions for REG0905

Bits	Bit Name	Description	Reset	Access
7	RF_BAND_SELECT_LUT_A_0	RF Band Select LUT A Index 0. 0: Low Band. 1: High Band.	0x0	R/W
[6:2]	LO_PHASE_Q_LUT_A_0	LO Phase Adjust Q LUT A Index 0. This bit field adjusts the phase of the Q path within the LO block. It can be used to calibrate the sideband rejection.	0x0	R/W
[1:0]	LO_TRAP_FILTER_LUT_A_0[9:8]	LO Trap Filter LUT A Index 0. 0x1E7: LO Frequency ≥ 21GHz. 0x1A7: 18.5GHz ≤ LO Frequency < 21.0GHz. 0x1A3: 14.5GHz ≤ LO Frequency < 18.5GHz. 0x3AA: 12.0GHz ≤ LO Frequency < 14.5GHz. 0x318: LO Frequency < 12GHz.	0x0	R/W

REGISTER DETAILS

Address: 0x906, Reset: 0x00, Name: REG0906

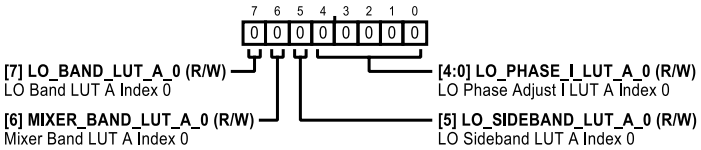


Figure 298.

Table 128. Bit Descriptions for REG0906

Bits	Bit Name	Description	Reset	Access
7	LO_BAND_LUT_A_0	LO Band LUT A Index 0. 0: Low Band. 1: High Band.	0x0	R/W
6	MIXER_BAND_LUT_A_0	Mixer Band LUT A Index 0. 0: Low Band. 1: High Band.	0x0	R/W
5	LO_SIDEBAND_LUT_A_0	LO Sideband LUT A Index 0. 0: LSB. 1: USB.	0x0	R/W
[4:0]	LO_PHASE_I_LUT_A_0	LO Phase Adjust I LUT A Index 0. This bit field adjusts the phase of the I path within the LO block. It can be used to calibrate the sideband rejection.	0x0	R/W

Address: 0x908, Reset: 0x00, Name: REG0908

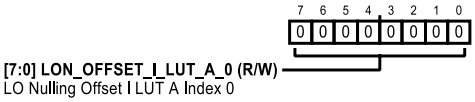


Figure 299.

Table 129. Bit Descriptions for REG0908

Bits	Bit Name	Description	Reset	Access
[7:0]	LON_OFFSET_I_LUT_A_0	LO Nulling Offset I LUT A Index 0.	0x0	R/W

Address: 0x909, Reset: 0x00, Name: REG0909

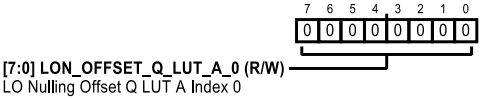


Figure 300.

Table 130. Bit Descriptions for REG0909

Bits	Bit Name	Description	Reset	Access
[7:0]	LON_OFFSET_Q_LUT_A_0	LO Nulling Offset Q LUT A Index 0.	0x0	R/W

Address: 0x90A, Reset: 0x00, Name: REG090A

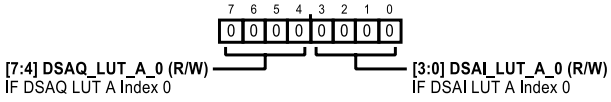


Figure 301.

REGISTER DETAILS

Table 131. Bit Descriptions for REG090A

Bits	Bit Name	Description	Reset	Access
[7:4]	DSAQ_LUT_A_0	IF DSAQ LUT A Index 0. 1.5dB Range with 0.1dB Step, Used for Sideband Rejection Calibration.	0x0	R/W
[3:0]	DSAI_LUT_A_0	IF DSAI LUT A Index 0. 1.5dB Range with 0.1dB Step, Used for Sideband Rejection Calibration.	0x0	R/W

Address: 0x90B, Reset: 0x00, Name: REG090B

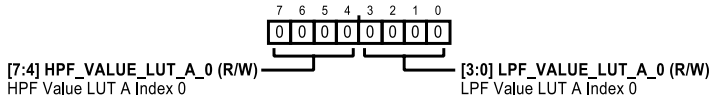


Figure 302.

Table 132. Bit Descriptions for REG090B

Bits	Bit Name	Description	Reset	Access
[7:4]	HPF_VALUE_LUT_A_0	HPF Value LUT A Index 0.	0x0	R/W
[3:0]	LPF_VALUE_LUT_A_0	LPF Value LUT A Index 0.	0x0	R/W

Address: 0x90C, Reset: 0x00, Name: REG090C

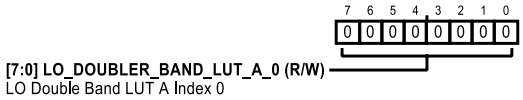


Figure 303.

Table 133. Bit Descriptions for REG090C

Bits	Bit Name	Description	Reset	Access
[7:0]	LO_DOUBLER_BAND_LUT_A_0	LO Double Band LUT A Index 0. 0xC0: LO Frequency ≥ 24GHz. 0x80: 18GHz ≤ LO Frequency < 24GHz. 0x08: 14GHz ≤ LO Frequency < 18GHz. 0x04: 12GHz ≤ LO Frequency < 14GHz. 0x1D: 10GHz ≤ LO Frequency < 12GHz. 0x1F: LO Frequency < 10GHz.	0x0	R/W

Note: The Filter LUT A Index 1 to Filter LUT B Index 31 bit fields functionality (Register 0x90D to Register 0xC3F) is identical to filter LUT A Index 0 bit fields functionality (Register 0x900 and Register 0x90C). See Table 22 for the register address information.

Address: 0xE00, Reset: 0x00, Name: REG0E00

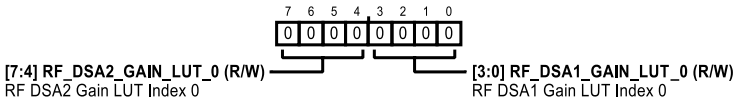


Figure 304.

Table 134. Bit Descriptions for REG0E00

Bits	Bit Name	Description	Reset	Access
[7:4]	RF_DSA2_GAIN_LUT_0	RF DSA2 Gain LUT Index 0. 0000: 0dB. 0001: −1dB. 0010: −2dB.	0x0	R/W

REGISTER DETAILS

Table 134. Bit Descriptions for REG0E00 (Continued)

Bits	Bit Name	Description	Reset	Access
		0011: −3dB. 0100: −4dB. 0101: −5dB. 0110: −6dB. 0111: −7dB. 1000: −8dB. 1001: −9dB. 1010: −10dB. 1011: −11dB. 1100: −12dB. 1101: −13dB. 1110: −14dB. 1111: −15dB.		
[3:0]	RF_DSA1_GAIN_LUT_0	RF DSA1 Gain LUT Index 0. 0000: 0dB. 0001: −1dB. 0010: −2dB. 0011: −3dB. 0100: −4dB. 0101: −5dB. 0110: −6dB. 0111: −7dB. 1000: −8dB. 1001: −9dB. 1010: −10dB. 1011: −11dB. 1100: −12dB. 1101: −13dB. 1110: −14dB. 1111: −15dB.	0x0	R/W

Address: 0xE01, Reset: 0x00, Name: REG0E01

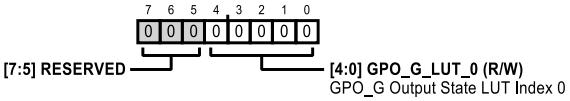


Figure 305.

Table 135. Bit Descriptions for REG0E01

Bits	Bit Name	Description	Reset	Access
[7:5]	RESERVED	Reserved.	0x0	R
[4:0]	GPO_G_LUT_0	GPO_G Output State LUT Index 0.	0x0	R/W

Note: The Gain LUT Index 1 to Gain LUT Index 66 bit fields functionality (Register 0xE02 to Register 0xE85) is identical to gain LUT_0 bit fields functionality (Register 0xE00 and Register 0xE01). See Table 22 for the register address information.

OUTLINE DIMENSIONS

Package Drawing Option	Package Type	Package Description
BC-120-4	CSP_BGA	120-Ball Chip Scale Package Ball Grid Array

For the latest package outline information and land patterns (footprints), go to Package Index.

ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Packing Quantity	Package Option
ADMV1355BBCZ	−40°C to +95°C	120-Ball Chip Scale Package Ball Grid Array	Pocket Tape, 500	BC-120-4
ADMV1355BBCZ-R7	−40°C to +95°C	120-Ball Chip Scale Package Ball Grid Array	Reel, 500	BC-120-4

[1] Z = RoHS Compliant Part.

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