ADMT4000

True Power-On Multiturn Sensor

FEATURES

- True power-on multiturn counter
- 46-turn magnetic sensor
- >16k° digital output
- ±0.25° accuracy
- Measurement update rate 100 kSPS
- 16 mT to 31 mT operating range
- Internal temperature sensor
- IC supply, 3.3 V
- SPI interface, 1.7 V to 5 V
- Junction temperature range: −40°C to +150°C
- 24-pin TSSOP
- Industrial applications

APPLICATION

- Rotation count detection and storage without power
- Contactless absolute position measurement
- Brushless DC motor control and positioning
- Actuator control and positioning

GENERAL DESCRIPTION

The ADMT4000 is a magnetic turn count sensor capable of recording the number of rotations of a magnetic system even while the device is powered down. On power-up, the device can be interrogated to report the absolute position of the system. The absolute position is reported through a serial-peripheral interface (SPI). The ADMT4000 counts up to 46-turns of an external magnetic field, which increments the absolute position in the clockwise (CW) direction.

The device includes three magnetic sensors, a giant magneto resistance (GMR) turn count sensor, which is used to count the number of rotations on the system, a GMR quadrant detecting sensor, and an anisotropic magnetoresistance (AMR) angle sensor. The AMR angle sensor is used in combination with a GMR quadrant detecting sensor to determine the absolute position of the system within 360°. Combining the GMR turn count sensor output with the AMR angle sensor output enables the device to report the position of the system with a high degree of angular accuracy.

PRODUCT HIGHLIGHTS

- True power-on multiturn counter
- Angle sensor with ±0.25° accuracy
- SPI interface
- Under and over voltage detection

FUNCTIONAL BLOCK DIAGRAM

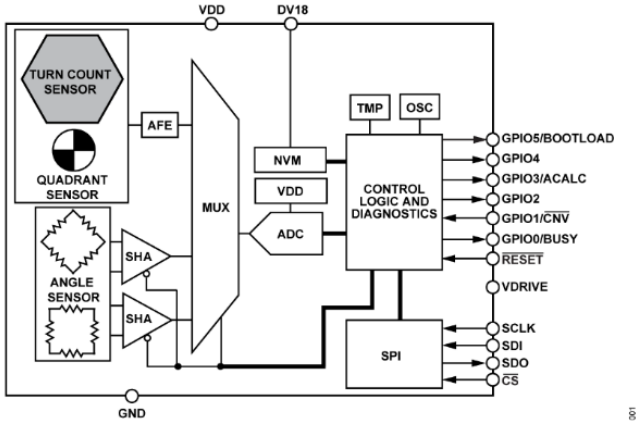


Figure 1. Functional Block Diagram

© 2026 Analog Devices, Inc. All rights reserved.

TABLE OF CONTENTS

Features ... 1
Application ... 1
General Description ... 1
Product Highlights ... 1
Functional Block Diagram ... 1
Table of Contents ... 2
Revision History ... 2
Specifications ... 3
  Electrical Characteristics ... 3
  Diagnostics Fault Conditions ... 5
  SPI Timing Specifications ... 6
  SPI Timing Diagrams ... 7
Absolute Maximum Ratings ... 8
  Thermal Resistance ... 8
  ESD Ratings for ADMT4000 ... 8
  ESD Caution ... 9
Pin Configuration and Function Descriptions ... 10
Typical Performance Characteristics ... 12
Theory of Operation ... 13
  Overview ... 13
  Sampling Modes ... 15
  Turn Count Behavior ... 16
  Angle Measurement Filter ... 17
  GMR Turn Count Sensor Reset ... 18
  Diagnostics and Fault Detection ... 19
  Serial-Peripheral Interface (SPI) ... 20
  Device Identification ... 22
  Calibration ... 23
  Register Details ... 25
  Page Agnostic Registers ... 26
  Page 0x0 Registers ... 28
  Page 0x2 Registers ... 30
Applications ... 37
  Rotational Speed Considerations ... 37
  Magnet Considerations ... 37
  Typical System Configuration ... 38
Outline Dimensions ... 40
Ordering Guide ... 40
Notes ... 41

REVISION HISTORY

Revision 0 | 10/2024
Initial Version

Revision A | 11/2024
Update to the ANGLE register definition

Revision B | 1/2026
Update to the legend on Figure 8

Revision C | 7/2026
Update to Table 30

SPECIFICATIONS

Electrical Characteristics

V_{DD} = 3.3 V ± 10%, V_{SS} = 0 V, T_J = −40°C to +150°C, where T_J is the junction temperature.

Table 1. Electrical Characteristics

PARAMETER	CONDITIONS/ COMMENTS	MIN	TYP	MAX	UNIT
MAGNETIC CHARACTERISTICS					
Turn-Count Detection Range		0		46	Turns
Angle Measurement Accuracy	Accuracy in a perfect magnetic system Measured at 25 mT	−0.90	±0.25	+0.90	Degrees
Angle Measurement Noise[1]					
IIR-Filter Disabled	Measured at 25°C, 25 mT			0.25	Degrees RMS
IIR-Filter Enabled	Measured at 25°C, 25 mT			0.03	Degrees RMS
Magnetic Window					
Magnetic-Field Operating Window[2]	Measured at 25°C, for more details, see the Magnet Considerations section	16		31	mT
T_C (B_{MAX})			−0.050		$\%K^{-1}$
T_C (B_{MIN})			−0.065		$\%K^{-1}$
INTERNAL TEMPERATURE SENSOR					
Accuracy			±5		°C
Resolution			±0.07		°C
MEASUREMENT RATE			100		kSPS
SAMPLE TIMING					
$\overline{CNV}$ to Angle Sample	When configured to use an external convert start signal, the time between a falling edge on the $\overline{CNV}$ pin and sampling instant of the SIN and COS inputs			1	µs
$\overline{CNV}$ Pulse Width[1]	The minimum time that $\overline{CNV}$ must be at V_{IH} or above before initiating a conversion with a falling edge	100			ns
Convert Start Synchronization (CNVSYNC)	Minimum time between triggering new samples in CNVSYNC mode	10			µs
Start-Up Time	Time from V_{DD} above the minimum specified-voltage level to the time when bootload has completed			10	ms

PARAMETER	CONDITIONS/ COMMENTS	MIN	TYP	MAX	UNIT
LOGIC SUPPLY					
V_{DRIVE}		1.7		5.5	V
DIGITAL OUTPUTS					
Output Voltage					
High, V_{OH}	200 µA load	V_{DRIVE} × 0.9			V
Low, V_{OL}	200 µA load			0.4	V
Floating State-Leakage Current[1]				10	µA
Floating State-Output Capacitance[1], C_{OUT}			5		pF
DIGITAL INPUTS					
Input Voltage[1]					
High, V_{IH}		V_{DRIVE} × 0.7			V
Low, V_{IL}				V_{DRIVE} × 0.3	V
Input Leakage Current, I_{IN}				±10	µA
Input Capacitance, C_{IN}			5		pF
POWER SUPPLY					
Supply Voltage, V_{DD}		3.0	3.3	3.6	V
Supply Current					
Zero Power Mode, I_{SY}	V_{DD} = 0 V, V_{DRIVE} = 0 V, and digital inputs = 0 V			0	nA
Active Mode, I_{SY}	Typical at V_{DD} = 3.3 V, T_J = 25°C		18	22	mA
Active Mode, I_{SY}	Typical at V_{DD} = 3.3 V, T_J = 25°C, and continuous conversion mode		23	30	mA

[1] Not production tested. Guaranteed by design and/or characterization.
[2] The minimum magnetic field strength is defined as the magnetic field required to ensure an error rate of less than 1 ppm.

Diagnostics Fault Conditions

V_{DD} = 3.3 V ± 10%, V_{SS} = 0 V, T_J = −40°C to +150°C, where T_J is the junction temperature.

Table 2. Diagnostics Fault Conditions

PARAMETER	CONDITIONS/ COMMENTS	MIN	TYP	MAX	UNIT
DIAGNOSTICS FAULT CONDITIONS					
Angle Sensor Radius		4352		23296	Code (decimal)
Power Supply					
V_{DD} Undervoltage			3.0		V
V_{DD} Overvoltage			5.4		V
V_{DRIVE} Undervoltage			1.5		V
V_{DRIVE} Overvoltage			5.7		V

SPI Timing Specifications

V_{DD} = 3.3 V ± 10%, V_{SS} = 0 V, T_J = −40°C to +150°C, where T_J is the junction temperature. Parameters are not production tested, guaranteed by design and/or characterization.

Table 3. SPI Timing Specifications

PARAMETER	CONDITIONS/ COMMENTS	MIN	TYP	MAX	UNIT
f_{SCLK}	SCLK frequency			10	MHz
t_{CSS}	$\overline{CS}$ setup time[1]	0			ns
t_{CSH}	$\overline{CS}$ hold time[1]	0			ns
t_{CSD}	$\overline{CS}$ disable time[1]	0			µs
t_{SU}	Data-setup time[1]	20			ns
t_{HD}	Data-hold time[1]	20			ns
t_R	SCLK rise time	0		5	ns
t_F	SCLK fall time	0		5	ns
t_{HIGH}	SCLK high time[1]	40			ns
t_{LOW}	SCLK low time[1]	40			ns
t_{CLD}	SCLK delay time[1]	10			ns
t_{CLE}	SCLK enable time[1]	10			ns
t_V	Output delay from SCLK low			40	ns
t_{HO}	Output hold time[1]	10			ns
t_{DIS}	Output disable time[1]			5	ns

[1] Timing is between the 50% V_{DRIVE} levels.

SPI Timing Diagrams

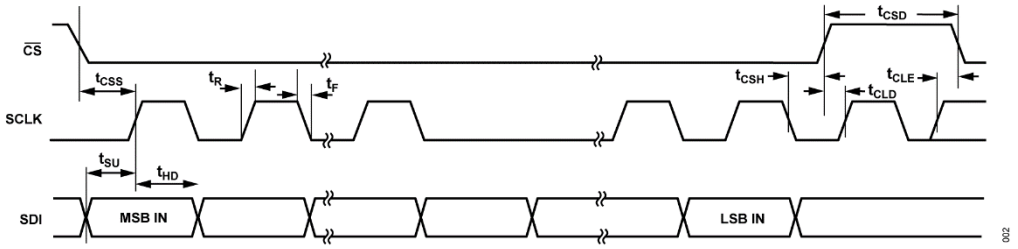


Figure 2. SPI Controller Request Timing Diagram

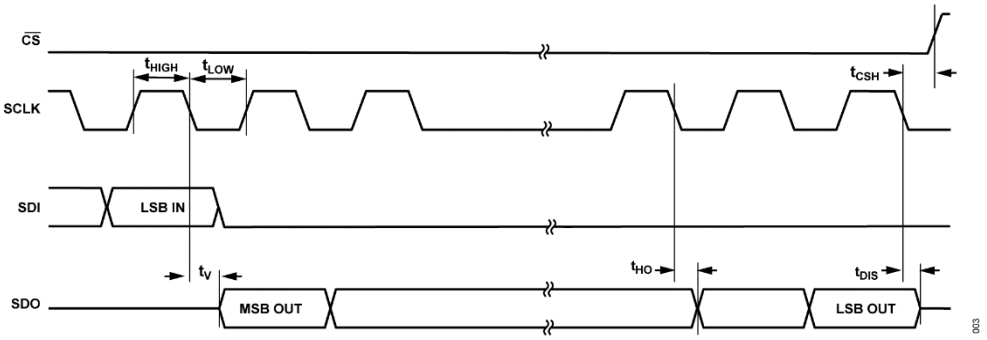


Figure 3. SPI Timing Diagram for Subordinate Response

ABSOLUTE MAXIMUM RATINGS

Table 4. Absolute Maximum Ratings

PARAMETER	RATING
Magnetic Field Strength	200 mT
V_{DD} to V_{SS}	−0.3 V to +6.0 V
Digital Input Voltage	−0.3 V to V_{DRIVE} + 0.3 V
Digital Output Voltage	−0.3 V to V_{DRIVE} + 0.3 V
V_{DRIVE}	−0.3 V to +6.0 V
TEST	−0.3 V to +0.3 V
DV18	−0.3 V to +2.5 V
Temperature	
Operating Junction, T_J	−40°C to +150°C
Storage	−55°C to +150°C

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

Thermal Resistance

Thermal performance is directly linked to printed circuit board (PCB) design and operating environment. Careful attention to PCB thermal design is required.

θ_{JA} is the natural convection junction-to-ambient thermal resistance measured in a one cubic foot sealed enclosure.

θ_{JC} is the junction-to-case thermal resistance.

Thermal performance is defined by the JEDEC JESD-51 test specifications.

Table 5. Thermal Resistance

Package Type	θ_{JA}	θ_{JC}	Unit
RU-24	73.25	17.56	°C/W

ESD Ratings for ADMT4000

The following ESD information is provided for handling of ESD-sensitive devices in an ESD protected area only.

Human body model (HBM) per ANSI/ESDA/JEDEC JS-001.

Charged device model (CDM) per ANSI/ESDA/JEDEC JS-002.

Table 6. ESD Ratings for ADMT4000

ESD Model	Withstand Threshold (V)	Class
HBM	±2000	2
CDM (on corner pins)	±750	C3
CDM (on non-corner pins)	±500	C3

ESD Caution



ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

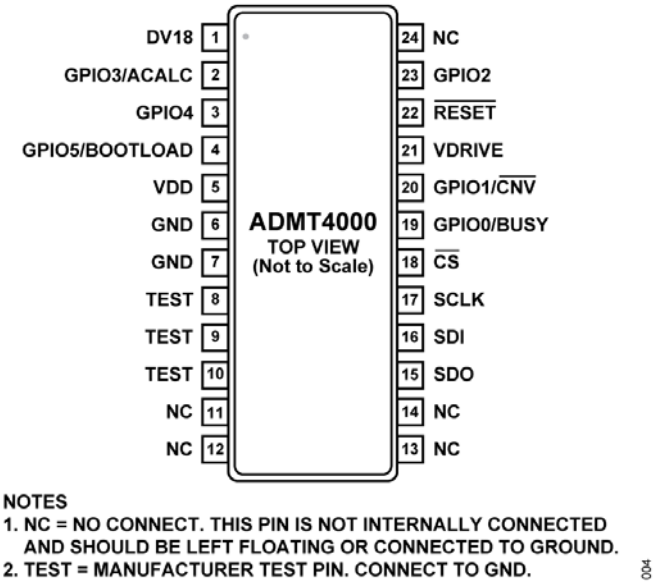


Figure 4. ADMT4000 PIN CONFIGURATION

Table 7. Pin Function Descriptions

PIN NO.	NAME	DESCRIPTION
1	DV18	1.8 V Regulator Decoupling. A 100 nF X8R capacitor to GND must be placed as close as possible to Pin 1.
2	GPIO3/ACALC	Digital Input and Output or Angle Calculation Status Output. Pin 2 is a dual-function pin. GPIO3 is a user-configurable digital input and output. ACALC is an output signal, which indicates when the angle is being calculated so the user can synchronize SPI angle read commands. By default, Pin 2 is configured as a digital input. If not used, this pin must be connected to GND through a 100 kΩ resistor.
3	GPIO4	Digital Input and Output. Pin 3 is a user-configurable digital input and output. By default this pin is configured as a digital input. If not used, Pin 3 must be configured as an input and connected to GND through a 100 kΩ resistor.
4	GPIO5/BOOTLOAD	Digital Input and Output or Bootloader Status Output. Pin 4 is a dual-function pin. GPIO5 is a user-configurable digital input and output. The BOOTLOAD output function is configured by default and set high at power on. Once the bootload sequence has successfully completed, Pin 4 is set low. The user must connect Pin 4 to VDRIVE through a 100 kΩ resistor.
5	VDD	Positive Power-Supply Voltage. A 100 nF X8R and a 1 µF X8R capacitor must be placed in parallel to GND as close as possible to Pin 5.
6	GND	Negative Power-Supply Voltage.
7	GND	Negative Power-Supply Voltage.
8	TEST	Connect Pin 8 to GND.
9	TEST	Connect Pin 9 to GND.
10	TEST	Connect Pin 10 to GND.

PIN NO.	NAME	DESCRIPTION
11	NC	No Connect. This pin is not internally connected and should be left floating or connected to ground.
12	NC	No Connect. This pin is not internally connected and should be left floating or connected to ground.
13	NC	No Connect. This pin is not internally connected and should be left floating or connected to ground.
14	NC	No Connect. This pin is not internally connected and should be left floating or connected to ground.
15	SDO	Serial Data Output. A 100 kΩ resistor must be connected between the SDO pin and GND.
16	SDI	Serial Data Input.
17	SCLK	Serial Clock.
18	$\overline{CS}$	Chip-Select Signal (Active Low) to Frame the SDI.
19	GPIO0/BUSY	Digital Input and Output or Busy. Pin 19 is a dual-function pin. GPIO0 is a user-configurable digital input and output. BUSY is set high when the part is performing a measurement. By default, Pin 19 is configured as a digital input. If not used, Pin 19 must be connected to GND through a 100 kΩ resistor.
20	GPIO1/$\overline{CNV}$	Digital Input and Output or Convert Start. Pin 20 is a dual-function pin. GPIO1 is a user-configurable digital input and output. A falling edge on Pin 20 initiates a conversion when configured as the convert start pin CNV, and bits 15:14 of the Convert Start and Register Page Select register are set to 0b00. By default, Pin 20 is configured as a digital input. If not used, Pin 20 must be connected to GND through a 100 kΩ resistor.
21	VDRIVE	Logic Power-Supply Input. A 100 nF X8R capacitor to GND must be placed as close as possible to Pin 5.
22	$\overline{RESET}$	Reset. Taking Pin 22 low performs a reset of the digital and analog circuitry and does not reset the GMR turn count sensor element. If not used, Pin 22 must be connected to VDRIVE through a 100 kΩ resistor.
23	GPIO2	Digital Input and Output. GPIO2 is a user-configurable digital input and output. By default, this pin is configured as a digital input. If not used, Pin 23 must be configured as an input and connected to GND through a 100 kΩ resistor.
24	NC	No Connect. This pin is not internally connected and should be left floating or connected to ground.

TYPICAL PERFORMANCE CHARACTERISTICS

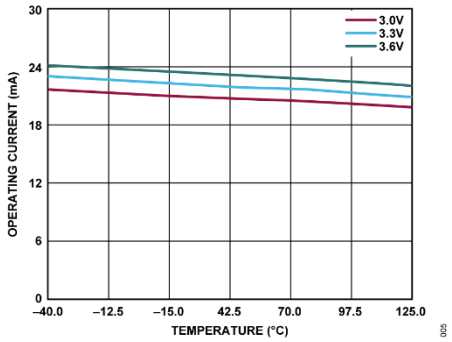


Figure 5. Supply Current in Continuous Conversion Mode vs. Ambient Temperature

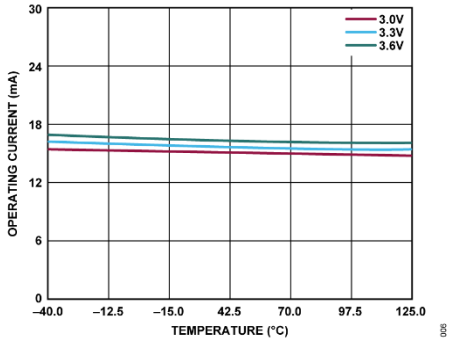


Figure 6. Supply Current in One-Shot Mode when not Sampling vs. Ambient Temperature

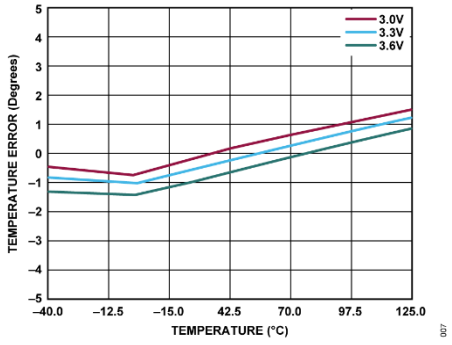


Figure 7. Temperature Sensor Error vs. Ambient Temperature

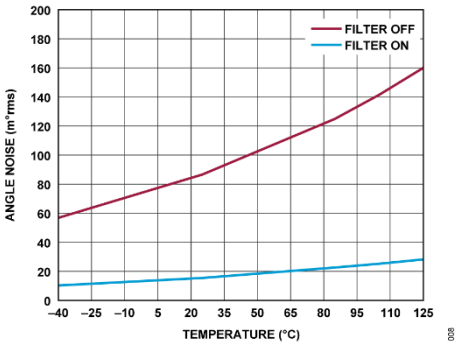


Figure 8. Angular Measurement Noise at 3.3 V, 25 mT vs. Ambient Temperature

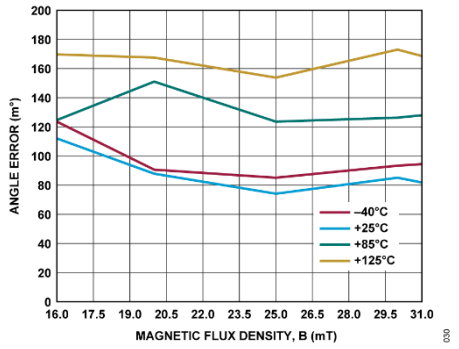


Figure 9. Angle Measurement Accuracy vs. Operating Magnetic Flux Density at 3.3 V

THEORY OF OPERATION

Overview

The ADMT4000 is a sensor that records the absolute position of an incident magnetic field over a maximum of 46 rotations, incrementing in the clockwise direction. When powered down, the sensor continues to track the rotational state of the magnetic field. When power is restored, the state of the sensors can be interrogated through the SPI interface.

The block diagram for the ADMT4000 is shown in Figure 10.

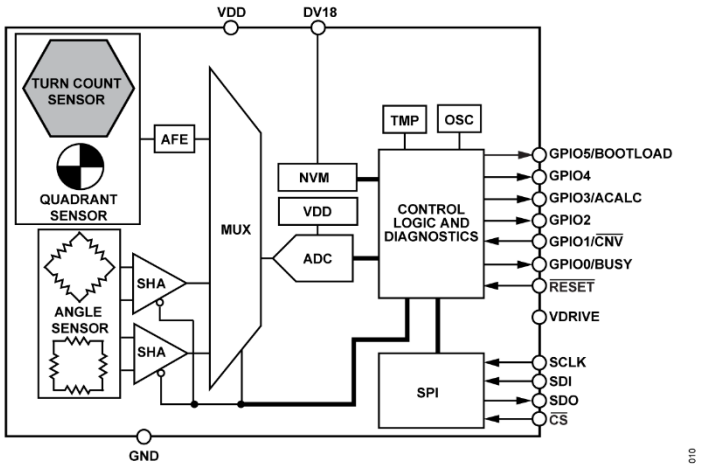


Figure 10. Functional Block Diagram

GMR Turn Count Sensor

The magnetic multiturn technology is based on a spiral made of a ferromagnetic nanowire. A rotating magnetic field can cause a local change in magnetization enabled by magnetic domain walls propagating along the spiral. Since the nanowire is fabricated using a GMR stack, a propagating domain wall causes a resistance change. Small portions of the spiral resistances are measured to locate the domain walls. The number of turns a magnetic field has rotated can be determined by decoding the measured resistance pattern of the spiral.

AMR Angle Sensor

The AMR angle sensor is formed by two sets of AMR elements. The resistance of each element varies with the direction of the external magnetic field. The AMR elements of each set are configured as a Wheatstone bridge offset by an angle of 45° so that the outputs are proportional to the sine and cosine of the direction of the external magnetic field. The sine output and the cosine output measure one full cycle for every 180° rotation of the external magnetic field.

GMR Quadrant Sensor

The GMR quadrant sensor provides the information required to enable the 0° to 180° AMR angle sensor data to be extended to 360°.

Temperature Sensor

To compensate for the temperature drift of the AMR angle sensor, an internal temperature sensor, TMP, is integrated into the part. Factory set calibration coefficients are applied. The temperature measurements are available through the TMP register using the SPI interface.

Signal Conditioning

The outputs from the GMR turn count, GMR quadrant, and AMR angle sensors require conditioning to match the input requirements of the analog-to-digital converter (ADC). The turn count and quadrant sensors outputs are conditioned in the turn count channel analog front end (AFE) block. The AMR angle sensor outputs are conditioned with two sample-and-hold amplifiers (SHA). The SHAs are also used to enable simultaneous sampling of the two AMR angle sensor outputs to ensure phase alignment when measurements are taken in a rotating magnetic field.

Analog-to-Digital Converter (ADC)

A single 12-bit successive approximation register (SAR) ADC using VDD as the reference is used to sample the GMR turn count sensor, AMR angle sensors, GMR quadrant detector, and some of the diagnostic features. Using VDD as the voltage reference for the ADC enables ratiometric measurements to be made, which optimizes performance across the voltage-supply ranges.

System Oscillators

The oscillator, OSC, is used to provide the clock for the on-board logic and AFE.

Control and Diagnostics

The core functionality of the device is determined by the control logic and diagnostics block. Key functions of the control logic include:

- Loading the factory set nonvolatile memory (NVM) into a series of volatile registers, which are used during the operation of the device. Factory set data includes calibration, device configuration, and identification data.
- Decoding the GMR turn count sensor elements to determine the turn count. A redundant turn count decoding block is included as a cross-check to the primary turn count decoder.
- Combining the outputs of the GMR turn count sensor, GMR quadrant detector, and AMR angle sensor to provide the absolute position of the system across a 0° to 16560° range, without further need for synchronization or data processing by the host system.
- On-chip harmonic calibration of the measured angle to provide the correction of system mechanical and magnet imperfections without the need for external processing. This calibration function enables system tolerances to be taken into account by compensating for first, second, and third harmonics when operating with the SPI interface. In addition, the use of the sensor in low field conditions can be optimized by updating the factory set eighth harmonic calibration to the specific operating environment.
- A state machine to control the measurement sequence of the GMR turn count sensor elements, GMR quadrant detector, AMR angle sensor, and diagnostics.
- Control of the sample acquisition mode, continuous or one-shot sampling.
- Enabling the angle measurement filter.

Interface Logic

The SPI interface pins are powered by the VDRIVE supply, enabling the part to be paired with a wide variety of microprocessors. The SPI is a bidirectional interface, which gives access to the configuration and results registers of the device.

Sampling Modes

It is possible to operate the device in either a continuous conversion mode or a one-shot conversion mode. In both modes, the sampling sequence is initiated by either writing to the CNVPAGE register or by using an external signal on the $\overline{\text{CNV}}$ pin. An additional triggering mode, synchronized angle, can be used in a continuous sampling mode to synchronize the angle measurement with an external source.

Continuous Conversion Mode

Following a device reset, Bit 0 (CNVMDE) of the General Register is set to zero to configure the device in the continuous conversion mode, and a conversion sequence is initiated. Conversion sequences repeat until the host system interrupts the sequence with a rising edge on $\overline{\text{CNV}}$ (Pin 20) or an SPI write to Bits 15:14 of the Convert Start and Register Page Select register to 0b11. To reinitialize the conversion sequence, a convert-start signal must be generated. This is achieved with either a falling edge on the $\overline{\text{CNV}}$ (Pin 20) or an SPI write to Bits 15:14 of the Convert Start and Register Page Select register to 0b00. By default, Pin 20 is configured as digital input, to make use of Pin 20 for convert-start control, the user must configure DIGIO register. If Pin 20 is configured as the $\overline{\text{CNV}}$ input, Bits 15:14 of the Convert Start and Register Page Select register are disabled.

As shown in Figure 11, if configured, the BUSY (Pin 19) remains high until the continuous conversion mode is aborted or paused. The turn count becomes valid at the end of the first conversion sequence. The turn count Absolute Angle Register is updated once an angle measurement has been completed within the conversion sequence.

The ACALC (Pin 2) is set high when the part is calculating the current angle and is set low once the angle has been calculated and the angle register updated, as shown in Figure 11.

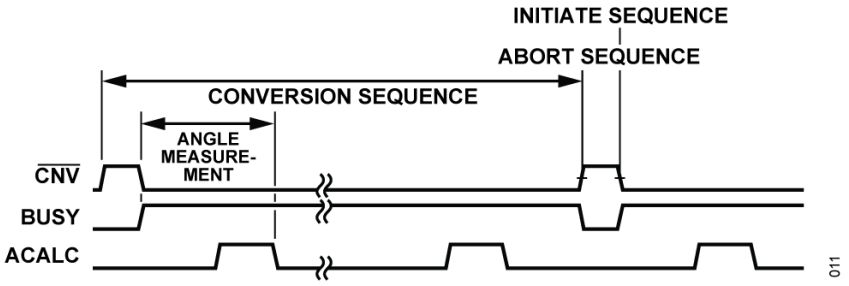


Figure 11. Continuous Conversion Sampling Mode Showing an Abort Sequence and Reinitialization of the Measurement

One-Shot Conversion Mode

By default, and following a reset, the device is in a continuous conversion mode. The user must set Bit 0 (CNVMDE) high in the General Register to configure the device to operate in the one-shot mode. The conversion sequence is initiated either by a falling edge of a signal applied to the $\overline{\text{CNV}}$ (Pin 20) or by setting Bits 15:14 ($\overline{\text{CNV}}$) of the Convert Start and Register Page Select register to 0b00. To make use of an external convert start signal, the $\overline{\text{CNV}}$ pin must be configured in the Digital Input/Output Enable Register (Bit 1). The Convert Start and Register Page Select register cannot be used to generate the convert-start signal once Pin 20 has been configured in this way.

As shown in Figure 12, the BUSY (Pin 19) remains high until the conversion sequence is complete and the angle registers have been updated. The turn count and angle are available once the conversion sequence has completed as indicated by the falling edge of the BUSY signal.

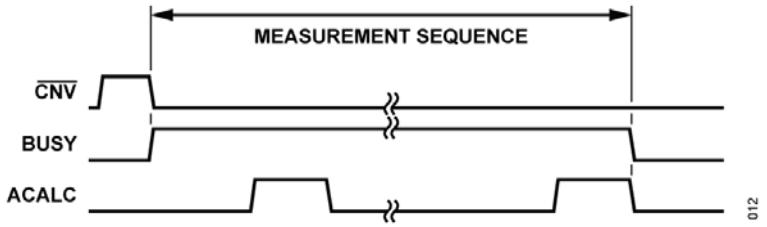


Figure 12. *One-Shot Conversion Sequence*

Synchronized Angle

An optional sampling mode, CNVSYNC, is available to enable the angle measurements to be synchronized within a conversion sequence with an external $\overline{\text{CNV}}$ signal.

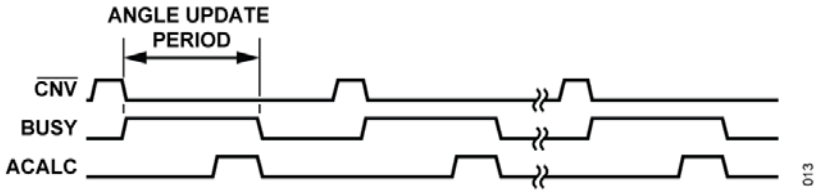


Figure 13. Angle Measurements are Initiated in Synchronized Angle Mode by a Falling Edge on the $\overline{\text{CNV}}$ Signal

Changing Sequence Mode

When changing the sampling mode, the current conversion operation must be aborted. The current conversion sequence is aborted by setting Bits 15:14 of the Convert Start and Register Page Select register to 0b11 or with a rising edge on the $\overline{\text{CNV}}$ (Pin 20), if configured as a CNV input in the Digital Input/Output Enable Register. Once the conversion sequence mode has been updated, conversions are restarted by setting Bits 15:14 of the Convert Start and Register Page Select register to 0b00.

Turn Count Behavior

There are three sensors in the ADMT4000, a GMR turn count sensor, a GMR quadrant detector, and an AMR angle sensor. The initial position is determined by the GMR turn count sensor with subsequent turn count positions derived from the AMR angle sensor combined with GMR quadrant detector. The GMR turn count sensor in the ADMT4000 provides true power-on turn count capability. When powered down, the ADMT4000 tracks the number of rotations of the external magnetic field between the 0 to 46 turn range shown by the red curve in Figure 14. On power-up, or at the start of a conversion sequence, the initial absolute position of the system is derived from the GMR turn count sensor combined with the AMR angle sensor (combined with the GMR quadrant detector) and is reported in the Absolute Angle Register. The GMR turn count sensor is used as the turn count reference for each measurement sequence in the one-shot mode but only for the initial sequence in the continuous conversion mode. The AMR angle sensor derived turn count has a range of −9 to 54 turns (blue curve in Figure 14). However, true power-on capability is only available in the 0 to 46 turn range of the GMR turn count sensor. If the external magnetic field is rotated beyond this range in the power-off state, the reported angle can be incorrect with no FAULT flag set after the next power-on. The extended range of the AMR angle sensor derived turn count is to facilitate system calibration only and should not be used in the normal operation of the part.

The GMR turn count sensor is decoded once during each measurement sequence and is used to verify the AMR angle sensor derived turn count. Figure 14 shows the behavior of the GMR turn count sensor derived turn count (red) and the AMR angle sensor derived turn count (blue):

- If the turn count has exceeded the maximum or minimum range, the reported position cycles within a range of one turn.
- The turn count cross check flag, Bit D13 in the FAULT register, is set high if the difference between the GMR turn count sensor derived position and the AMR angle sensor derived position exceeds 0.5 turns. For example, if the turn count is out of range of the GMR turn count sensor shown by the red curve in Figure 14. The FAULT flag, Bit D13, is not set if this happens while the part is powered down or if the part is in the one-shot mode.

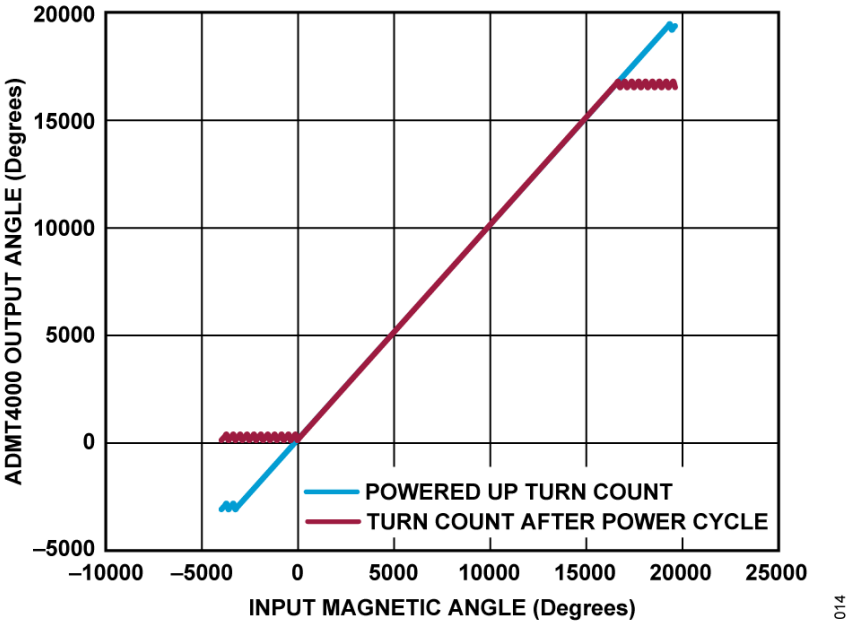


Figure 14. Turn Count Behavior vs. Input Magnetic Field Angle

Angle Measurement Filter

The ADMT4000 has an optional infinite impulse response (IIR) filter to reduce angle noise. The-IIR filter is enabled by setting the ANGLFILT Bit D12 of the General Register high:

- If the turn count is above 53.5 turns, the filter is bypassed. The filter is reenabled when the input drops below 53 turns again. Angle data is correct but is unfiltered in both cases.
- If the turn count is below −8.5 turns, the filter is bypassed and is only reenabled when the turn count is above −8 turns to prevent incorrect turn count data due to the wrapping at the end stop.

In the one-shot mode, the number of angle measurements reported depends on the turn count, since the angle measurement is only valid once the state of the GMR turn count sensor has been determined. Since the number of valid angle measurements available to be filtered varies depending on the absolute position of the system, it is recommended that the angle filter is not used in this conversion mode.

The transfer function for the IIR-filter is (see Figure 15):

$$Out[n] = Out[n-1] + (In[n] - Out[n-1])/16$$

where:

In[n] is the current angle measurement.

Out[n−1] is the previous filtered angle measurement.

Out[n] is the current filtered angle measurement.

Filtering occurs over the current angle measurement and the previous 15 angle measurements, this leads to a latency of 15 × 9 µs, assuming an angle measurement timing interval of 9 µs.

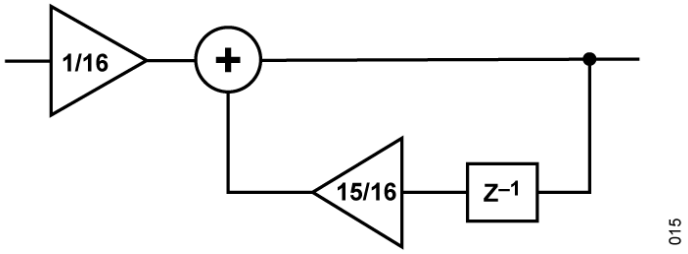


Figure 15. IIR Transfer Function Used for the Angle Filter

GMR Turn Count Sensor Reset

Note that the user must reset the GMR turn count sensor once the GMR turn count sensor is assembled into the magnetic system of the final application.

The turn counter must also be reset if any of the following conditions are true:

- The GMR turn count sensor is exposed to a magnetic field greater than BMAX.
- Bit D9 or Bit D13 of the FAULT register are set.

Once the reset has been executed, the conversion sequence must be aborted and restarted before the ADMT4000 shows a turn count of 45 plus the actual reset angle used.

The FAULT register, Table 14, has two bits that are used to indicate when a magnetic reset is required, Bit D9 and Bit D13. Bit D9 indicates that a false state of the GMR turn count sensor has been detected, and Bit D13 indicates that the turn count derived from the AMR angle sensor does not match the turn count derived from the GMR turn count sensor. The GMR turn count sensor can be reset by either rotating the external magnetic field 46 turns clockwise or by applying an external magnetic field at the required angle.

Reset Using A Magnetic Field

The GMR turn count sensor can be reset by applying an external magnetic field with a field strength greater than 60 mT at the 315° orientation, as shown in Figure 16. This is irrespective of the current turn count value. Both sets of arrows in Figure 16 point from a magnetic north to a magnetic south. The solid arrows indicate the 0° direction and the dashed lines indicate the direction of the magnetic reset field, 315°. The user can generate the magnetic field in any way as long as the combined field strength of the application magnet (if installed) and the magnetic reset field is greater than 60 mT for a duration of no less than 10 µs. Typical methods of creating the magnetic reset field are:

- Using an electromagnet. This can be a wire coil close to the sensor embedded in the application circuit board or housing.
- Mechanically bring the application magnet closer to the sensor such that the field incident on the sensor is greater than 60 mT at 315°.

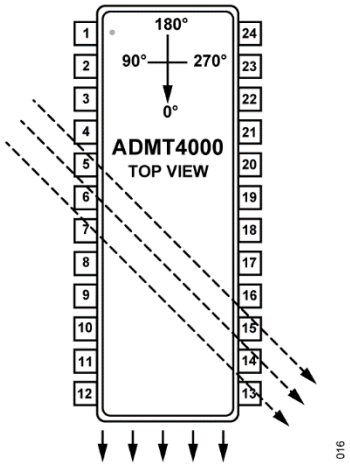


Figure 16. Resetting the GMR Turn Count Sensor by Applying an External Magnetic Field

Reset by Overturning the System Magnet

The GMR turn counter can be reset by turning the system magnet by 46 or more turns in the clockwise direction.

Diagnostics and Fault Detection

The ADMT4000 has some built-in fault detection and diagnostic features to detect incorrect position information. The fault detection and diagnostic features result in a bit being set in the Fault Register. In addition, the SPI output frame includes the cyclic redundancy checks (CRCs) to validate a data transfer. For more details on the CRC coverage and implementation, see the relevant interface sections of this data sheet.

FAULT Register Reported Errors

ANGLE SENSOR RADIUS

The AMR angle sensor is configured as two AMR bridges offset by 45°, as shown in Figure 17, with the SINE and COSINE calculated, as shown in Table 8. The AMR angle sensor radius, SQRT(SINE^2 + COSINE^2), is compared against a factory preset limit. If it exceeds that limit, Bit D14 is set in the Fault Register.

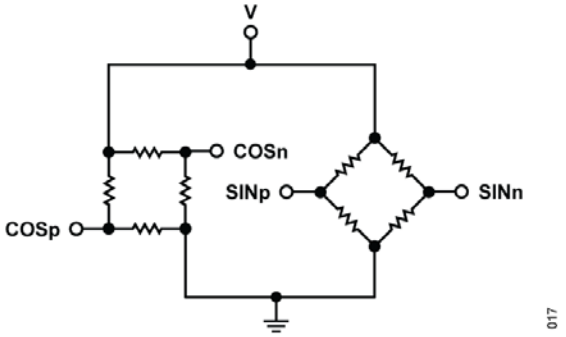


Figure 17. Sine and Cosine Signals from AMR Bridges of the Angle Sensor

Table 8. SINE and COSINE Calculation from the AMR Bridge Measurements

Function	Calculation
SINE	$SIN_p - SIN_n$
COSINE	$COS_p - COS_n$

TURN COUNT DIAGNOSTICS

To validate the GMR turn count sensor, the user must monitor the Fault Register. Some examples of errors that may transpire are as follows:

- Bit D9 of the Fault Register indicates an error relating to a false state of the GMR turn count sensor. An illegal state can happen if the following occurs:
  - The sensor is exposed to a stray magnetic field larger than BMAX, which causes one or more elements of the sensor to change state out of sequence.
  - A fault has developed in the sensor, which has caused an element not to change state when expected.
  - The turn counter has been turned below typically 2 turns.
  - Illegal value in the factory set the NVM for the GMR configuration.
- Bit D13 of the Fault Register indicates that the turn count derived from the GMR turn count sensor is different from the turn count derived from the AMR angle sensor. This can happen if the following occurs:
  - The difference between the GMR based turn count sensor and the AMR based turn count exceeds 0.5 turns.
  - The turn count is above 46.5 turns or below 0 turns.
  - The redundant GMR turn count sensor decoder does not match the primary GMR turn count sensor decoder.
  - An error occurs in the GMR turn count and AMR angle sensor combination logic.
  - GMR quadrant sensor cross check error occurs.

MEMORY

The ADMT4000 contains NVM, which is used to store factory set calibration, configuration, and device traceability data. Following a device reset, the contents of the NVM memory are loaded into the volatile memory. The NVM controller uses error correction codes (ECC), which can detect and correct single-bit errors and detect two-bit errors.

Following the NVM data being loaded into the volatile memory, if the ECC algorithm detects a 2-bit error, the device does not enter into normal operation. The detection of a fault is indicated to the user by BOOTLOAD output (Pin 4) remaining high and Bit D7 of the Fault Register set high. In this state, the SPI interface remains operational to interrogate the device registers. During operation, the contents of the data volatile memory loaded from NVM is continually checked using a CRC. If a fault is detected, then Bit D5 of the Fault Register is set. An ECC algorithm also protects the user-configuration registers. When the user updates the contents of these registers, the ECC Generation register must be updated in the ECCEDC register, Bit D7 of the Fault Register set high if a two-bit error is detected in the user-configuration register.

POWER SUPPLIES

There are two power supplies for the ADMT4000 listed as follows:

- VDD provides the main power supply for the internal analog and digital functions.
- VDRIVE supplies the power supply for the GPIO and SPI ports.
- Undervoltage (UV) and overvoltage (OV) faults are detected and reported for VDD and VDRIVE. The user can check the status by monitoring Bit D0 to Bit D3 of the Fault Register, where a logic-high means that a fault state has been triggered.

Serial-Peripheral Interface (SPI)

The ADMT4000 SPI is Mode 0 SPI compatible, that is, the clock polarity (CPOL) is 0, and the clock phase (CPHA) is 0. The interface consists of four signals: CS, SDI, SCLK, and SDO, as shown in Figure 29. The SDI line transfers data into the on-chip registers, and the SDO line transfers data from the on-chip registers. SCLK is the serial-clock input for

the device and all data transfers take place with respect to SCLK. Data clocks into the ADMT4000 on the SCLK rising edge, and data clocks out of the ADMT4000 on the SCLK falling edge. The CS input frames the 32-bit serial data being transferred to or from the device to access the 16-bit device registers.

ECC Generation

The ECCEDC register contains two ECC codes, ECC_CONFIG0 and ECC_CONFIG1. When calculating the ECC, it is important to order the configuration registers in the order shown in Table 30. For example, for ECC_CONFIG0, the GENERAL register is at the lower end of the data set and the lower byte of the H3MAG register (H3MAG[7:0]) is at the upper end of the data set. Code to demonstrate how to implement the ECC calculation is available in the no-OS drivers for the ADMT4000.

CRC Implementation

The CRC engine implements a 5-bit, $x^5 + x^2 + 1$, CRC polynomial using the serial linear feedback shift register (LFSR) approach and a seed value of 0x1F. The CRC is calculated on the following bits:

- SPI read: Rb/W bit and Address[5:0] on SDI, Data[15:0], the bit permanently set high, and conversion count[1:0] on SDO.
- SPI write: Rb/W bit, Address[5:0], Data[15:0] and the 3 following bits on SDI.

In both the SPI write and read modes, the CRC provides coverage on 26-bits, achieving a hamming distance of 3.

To calculate the CRC value from 26 bits of data, use the following pseudo code:

```
shft[5] = {1,1,1,1,1};
for (i=30; i>=5; i--)
   {
    xor_0 = data_in[i] ^ shft[4] ;
    shft[4] = shft[3];
    shft[3] = shft[2];
    shft[2] = shft[1] ^ xor_0;
    shft[1] = shft[0];
    shft[0] = xor_0;
   }
Crc5calc = shft;
```

Register Read Operations

REGISTER READ

The register read operation is shown in Figure 18. Note the following:

- The first data bit sent by the microcontroller to the ADMT4000 is ignored.
- The second bit is set low to select the read register configuration.
- The 6-bit register address A5 to A0 is then clocked into the ADMT4000.
- On the next falling edge, the most significant bit (MSB) of the addressed register is clocked out of the ADMT4000, and the remaining 15 bits are clocked out on the following 15 falling edges of the clock.
- The first bit following the register data is always set high.
- A two-bit conversion counter (C1 and C0) increments, indicating that the measurement sequence has been completed. The conversion counter is increment after each successful conversion sequence and loops from 0b00 to 0b11.

- Following the life counter, a 5-bit CRC is included to enable the user to determine the integrity of the received data (for more details, see the CRC Implementation section).

When not transmitting data, the SDO line of the ADMT4000 is set to high impedance so that the part does not interfere with other devices on the SPI bus.

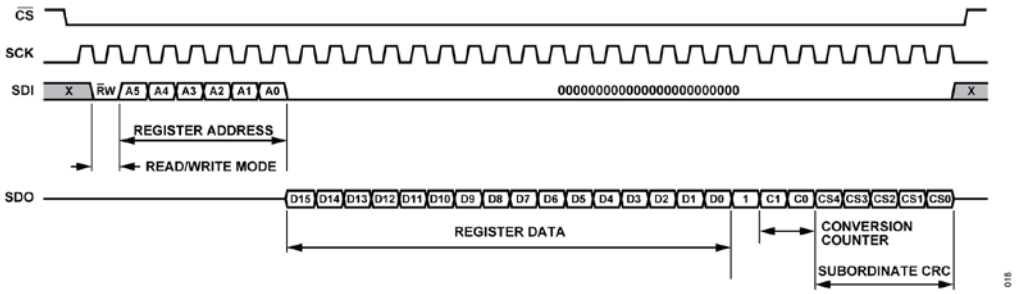


Figure 18. SPI Register Read Operation

ANGLE AND ABSANGLE READ

Reading the contents of the Angle Register and Absolute Angle Register is a special case. To ensure that the contents of the Angle Register and Absolute Angle Register are taken from the same sampling point, the user is required to read the contents of both the Angle Register and Absolute Angle Register as a single SPI transaction. The registers are updated when CS is high and keeping CS low prevents the second register from being updated before it can be read. The recommended method of reading the Angle Register and Absolute Angle Register registers is to use a single 64-bit write and read operation where the SPI frame is constructed from the 32-bit read frames used for the Angle Register and Absolute Angle Register.

Register Write Operations

The register write operation is shown in Figure 19. Note the following:

- The first data bit sent from the microcontroller to the ADMT4000 is ignored.
- The second bit is set high to select the write register configuration.
- The 6-bit register address A5 to A0 is then clocked into the ADMT4000.
- On the next rising edge, the first bit of the address register is clocked into the ADMT4000, and the remaining 15 bits are clocked in on the following 15 rising edges of the clock.
- The following 3 bits are not specified.
- The remaining 5 bits contain the frame CRC. For more details, see the CRC Implementation section.



Figure 19. 32-Bit Write Operation for 16-Bit Register

Device Identification

A set of unique identification registers are factory set for the ADMT4000:

- UNIQID0, UNIQID1, and UNIQID2 contain the codes that identify each individual part to allow full traceability.
- UNIQID3 contains the part type identification:

- Product type
- Voltage supply
- Silicon revision

The codes are accessed by a SPI register read.

Calibration

Basic Principle

Magnetic angle sensors are used for position sensing in many different applications. For applications where the end of a rotating shaft can be accessed, a low cost and highly accurate angle sensor can be implemented using just a simple dipole magnet and the ADMT4000, as shown in Figure 20.

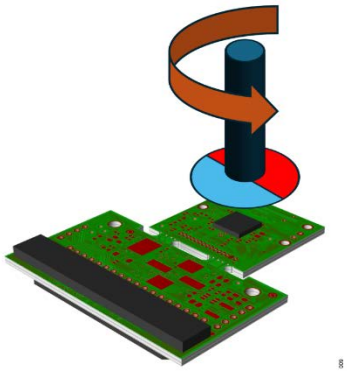


Figure 20. EV-ADMT4000SDV Evaluation Board in an End-of-Shaft Configuration

System Error Sources

For an end-of-shaft configuration, the highest system-level accuracy is achieved if the angle sensor is perfectly centered with the magnet.

Due to mechanical tolerances, nonidealities are seen on the angle measurements.

The four most significant types of mechanical and magnetic error sources are:

- Sensor alignment error. This is caused by a misalignment between the center of the magnetic field and the center of the angle sensor. See Figure 21.
- Magnet axis displacement error. This is caused by an incorrect centering of the magnet and the axis of the rotating shaft. See Figure 22.
- Magnet magnetization error. This is caused by tolerances in the magnet manufacturing process. See Figure 23.
- Magnet tilt error. This is caused by an inclination between the rotating shaft and the sensor, creating an irregular air gap. See Figure 24.

The above-mentioned mechanical and magnetic error sources manifest as harmonics in the data measured by the sensor. The error produced by misalignment can be analyzed by taking the Fourier transform of the measured data over multiple revolutions of the system.

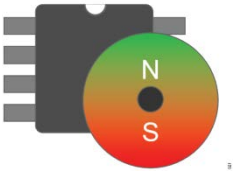


Figure 21. Sensor Alignment Error

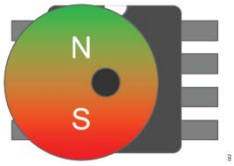


Figure 22. Magnet Axis Displacement Error



Figure 23. Magnetization Error

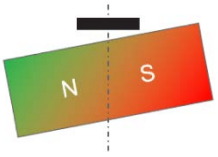


Figure 24. Magnet Tilt Error

Calibration Procedure

The ADMT4000 contains a total of eight registers to enable the user to compensate for harmonic errors. 1st, 2nd, 3rd, and 8th harmonics can be corrected by writing to the appropriate harmonic magnitude (HxMAG) and phase (HxPH) registers. The calibration engine allows a wide range of mechanical errors to be corrected on chip, see the register descriptions for the various harmonic calibration coefficient ranges. The user must ensure that the harmonic calibration registers are set to zero before the calibration process is initiated.

The harmonic magnitude and phase values are typically extracted from the Fourier transform of a set of angle measurements taken with a magnetic field rotating with a constant angular velocity. Do the following steps to perform a calibration;

1. Perform a magnetic reset on the GMR turn count sensor.
2. Before the calibration process is initiated, the user must ensure that the harmonic calibration registers are set to zero. By default, the 1st, 2nd, 3rd harmonics coefficients are set to zero, but the 8th harmonic have a factory set value. If the user intends to update the 8th harmonic coefficient, Bit 10 of the General Register must be set.
3. If the angle filter is enabled during calibration, the turn count range must be kept between 0 and 46 turns.
4. To avoid aliasing in the FFT algorithm:
    1. The number of measurements taken must be of the form 2N, where N is an integer, typically 512 samples is sufficient.
    2. The number of rotations of the external magnetic field must be a prime number, 11 is typical.
5. It is recommended that calibration is performed with the CNVSYNC bit (13) set in the General Register.
6. The CNVSYNC function ensures that the SINE and COSINE measurements are synchronized with an external CNV signal to reduce phase error. In the case where it is not possible to provide a CNV signal, the part must be configured to operate with continuous conversions, this limits the effectiveness of the harmonic calibration but should still reduce errors due to imperfections in the magnetic system.
7. Once the AMR angle sensor has been calibrated, a magnetic reset of the GMR turn count sensor is highly recommended to ensure the part is in a known good state.

Register Details

The register map for the ADMT4000 is split into pages. To access registers on a specific page, the appropriate page address must be written into the CNVPAGE register. The default (power-on-reset) value for each register is 0x0000, unless otherwise stated in Table 9. The CNVPAGE, ABSANGLE, DIGIO, ANGLE, and FAULT registers are page agnostic, which means that they can be accessed without setting the CNVPAGE register before they are addressed.

Table 9. Register Map Summary

Register	Function	Page	Address	Default Value	Access
CNVPAGE	Convert Start and Page Select	Agnostic	0x01	0x0000	R/W
ABSANGLE	Absolute Angle	Agnostic	0x03	0xDB00	R
DIGIO	Digital Input Output	Agnostic	0x04	0x0000	R/W
ANGLE	Angle Register	Agnostic	0x05	0x8000	R
FAULT	Fault Register	Agnostic	0x06	0xFFFF	R/W
SINE	Sine Measurement	0x00	0x10	0x0000	R
COSINE	Cosine Measurement	0x00	0x11	0x0000	R
RADIUS	Angle Measurement Radius	0x00	0x18	0x0000	R
TMP	Temperature Sensor	0x00	0x20	0x0000	R
GENERAL	General Device Configuration	0x02	0x10	0x1230	R/W
DIGIOEN	Enable Digital Input/Outputs	0x02	0x12	0x201F	R/W
CNVCNT	Conversion Count	0x02	0x14	0x0000	R
H1MAG	1st harmonic Error Magnitude	0x02	0x15	0x0000	R/W
H1PH	1st Harmonic Error Phase	0x02	0x16	0x0000	R/W
H2MAG	2nd Harmonic Error Magnitude	0x02	0x17	0x0000	R/W
H2PH	2nd Harmonic Error Phase	0x02	0x18	0x0000	R/W
H3MAG	3rd Harmonic Error Magnitude	0x02	0x19	0x0000	R/W
H3PH	3rd Harmonic Error Phase	0x02	0x1A	0x0000	R/W
H8MAG	8th Harmonic Error Magnitude	0x02	0x1B	0x0000	R/W
H8PH	8th Harmonic Error Phase	0x02	0x1C	0x0000	R/W
ECCEDC	Error Correction and Detection Codes	0x02	0x1D	0xXXXX	R/W
UNIQID0	Unique ID Register 0	0x02	0x1E	0xXXXX	R
UNIQID1	Unique ID Register 1	0x02	0x1F	0xXXXX	R
UNIQID2	Unique ID Register 2	0x02	0x20	0xXXXX	R
UNIQID3	Product, Voltage Supply, and ASIC Revision	0x02	0x21	0x0002	R
ECCDIS	Error Correction Code Disable	0x02	0x23	0x0000	R/W

Page Agnostic Registers

CONVERT START AND REGISTER PAGE SELECT

Address: 0x01, Reset: 0x0000, Name: CNVPAGE

The CNVPAGE register has two functions:

1. Select the page of the register that the user wants to access. If accessing multiple registers on the same page, set the CVNPAGE resister only before the first register access.
2. Trigger or abort a conversion sequence, setting bits 15:14 of the CNVPAGE register to 0b00 starts a conversion sequence, setting 0b11 aborts a conversion sequence, as shown in Table 10.

Table 10. Bit Description for the CNVPAGE Register

Bit	Bit Name	Description	Access
[15:14]	$\overline{\text{CNV}}$	00 mimics the falling edge of convert start pin to trigger conversions. 11 mimics the rising edge of convert start pin to abort a conversion.	R/W
[13:5]	RESERVED	Reserved.	R
[4:0]	PAGE	Register Page Address.	R/W

ABSOLUTE ANGLE REGISTER

Address: 0x03, Reset: 0xDB00, Name: ABSANGLE

The ABSANGLE register stores the combined turn count and angle information with a range of 16560°.

ABSANGLE[15:8] contains the turn count in quarter turns.

ABSANGLE[15:10] contains the number of whole turns, including a code for an invalid turn count:

- 0b0000 00 to 0b1101 01: straight binary turn count.
- 0b1101 10: invalid turn count.
- 0b1101 11 to 0b1111 11: two's compliment turn count value.

The lower ten bits contain the angle information in straight binary with a resolution of 0.351°.

Table 11. Bit Description for the ABSANGLE Register

Bit	Bit Name	Description	Access
[15:0]	ABSANGLE	Absolute Angle.	R

DIGITAL INPUT OUTPUT REGISTER

Address: 0x04, Reset: 0x0000, Name: DIGIO

Depending on how the GPIO ports are configured with the DIGIOEN register, the DIGIO register is used to either set or read the state of GPIO ports. The GPIO pins are mapped directly to the bit position in the register, GPIO5 to GPIO0 are controlled by DIGIO[5:0], respectively.

Table 12. Bits Description for the DIGIO Register

Bit	Bit Name	Description	Access
[15:6]	RESERVED	Reserved.	R
[5:0]	DIGIO	GPIO Logic State.	R/W

ANGLE REGISTER

Address: 0x05, Reset: 0x8000, Name: ANGLE

The ANGLE register stores the angle information with the offset, gain, phase, and harmonic corrections applied and provides an accurate 0° to 360° position. For more details on when the angle register is updated, see the Sampling Modes section.

Angle Resolution = 360°/4096.

Table 13. Bit Description for the ANGLE Register

Bit	Bit Name	Description	Access
[15:4]	ANGLE	Magnetic Field Angle with 360° Range.	R
[3:0]	RESERVED	Reserved.	R

FAULT REGISTER

Address: 0x06, Reset: 0xFFFF, Name: FAULT

The FAULT register stores various fault flags. Following a power-on reset, the FAULT register is set to 0xFFFF. The user must verify that all bits can be set to 0xFFFF by reading this register at power up. After verifying the register functionality, the user must clear the register by writing 0x0000 to the register. A bit in the FAULT register stays set to high until the user writes 0x0000 to the FAULT register, the set fault bit does not clear if the potential fault condition persists.

Table 14. Bit Description for the FAULT Register

Bit	Function	Description	Status	Access
D15	RESERVED	Reserved.	Not Active	R/W
D14	AMR Angle Sensor Radius Check	AMR Angle Sensor Radius Check.	Active	R/W
D13	Turn Counters Cross-Check Error	D13 bit flags if any of the following are detected: • The difference between turn count reported in the ABSANGLE register and the GMR turn count sensor exceeds 0.5 turns. • The turn count is above 46.5 turns or below 0 turns while the part is powered up. • The primary and redundant turn count decoders do not match. • There is a GMR turn count sensor and AMR angle sensor combination logic error.	Active	R/W

Bit	Function	Description	Status	Access
		• A GMR quadrant sensor decode error occurs.		
D12	RESERVED	Reserved.	Not Active	R/W
D11	RESERVED	Reserved.	Not Active	R/W
D10	RESERVED	Reserved.	Not Active	R/W
D9	GMR Turn Count Sensor False State or Reference Resistor Flip	D9 flags if any of the following are detected: • An unrecognized state of the GMR turn count sensor, • A reference resistor in the wrong state, • An illegal value (either 0x01 or 0b10) is set in the, CW/CCW NVM setting, • The turn count is between 0 turns to typically 2 turns.	Active	R/W
D8	RESERVED	Reserved.	Not Active	R/W
D7	ECC Double Bit Error	Two-bit fault detected in NVM or user-configuration registers.	Active	R/W
D6	RESERVED	Reserved.	Not Active	R/W
D5	NVM CRC Fault	Nonvolatile memory CRC fault.	Active	R/W
D4	RESERVED	Reserved.	Not Active	R/W
D3	VDRIVE Overvoltage Detected	VDRIVE above the expected range, see Table 2.	Active	R/W
D2	VDRIVE Undervoltage Detected	VDRIVE below the expected range, see Table 2.	Active	R/W
D1	VDD Overvoltage Detected	VDD above the expected range, see Table 2.	Active	R/W
D0	VDD Undervoltage Detected	VDD below the expected range, see Table 2.	Active	R/W

Page 0x0 Registers

SINE REGISTER

Page: 0x00, Address: 0x10, Reset: 0x0000, Name: SINE

The SINE register contains the value of the sine portion of the AMR angle sensor without the sensor gain, offset, and harmonic calibration applied.

At the start of a measurement sequence, the register is set to 0x2000 and is updated once a valid measurement is available. The reset value of the register is 0x0000 and is stored in 2's complement data format.

Table 15. Bit Description for the SINE Register

Bit	Bit Name	Description	Access
[15:2]	SINE	Uncorrected Sine Output.	R
[1]	RESERVED	Reserved.	R
[0]	STATUS	During continuous conversions, this flag is set high when new data is available. This flag is set low when the user reads the register contents. In One-Shot mode, this bit is always set low.	R

COSINE REGISTER

Page: 0x00, Address: 0x11, Reset: 0x0000, Name: COSINE

The COSINE register contains the value of the cosine portion of the AMR angle sensor without the sensor gain, offset, and harmonic calibration applied. At the start of a measurement sequence, the register is set to 0x2000 and is updated once a valid measurement is available. The reset value of the register is 0x0000 and is stored in 2's complement data format.

Table 16. Bit Description for the COSINE Register

Bit	Bit Name	Description	Access
[15:2]	COSINE	Uncorrected Cosine Output.	R
[1]	RESERVED	Reserved.	R
[0]	STATUS	During continuous conversions, this flag is set high when new data is available. This flag is set low when the user reads the register contents. In One-Shot mode, this bit is always set low.	R

RADIUS

Page: 0x00, Address: 0x18, Reset: 0x0000, Name: RADIUS

The RADIUS register stores the magnitude of the vector from the SINE and COSINE angle measurements in bits 15 to 1, the RADIUS.

Resolution = 0.000924 mV/V.

Table 17. Bit Description for the RADIUS Register

Bit	Bit Name	Description	Access
[15:1]	RADIUS	Angle Vector Magnitude, or Radius.	R
[0]	STATUS	During continuous conversions, this flag is set high when new data is available. This flag is set low when the user reads the register contents. In One-Shot mode, this bit is always set low.	R

TEMPERATURE SENSOR

Page: 0x00, Address: 0x20, Reset: 0x0000, Name: TMP

The Temperature Sensor register stores the temperature used for the AMR angle sensor and the GMR turn count sensor calibration. This register is set to 0xFFF0 at the start of every conversion sequence.

$$TMP_{DEGC} = (TMP_{CODE} - 1168)/15.66$$

where, TMP_{CODE} is the 12-bit register value and TMP_{DEGC} is the internal temperature in degrees Celsius.

Table 18. Bit Description for the TMP Register

Bit	Bit Name	Description	Access
[15:4]	TMP	Internal Temperature Sensor.	R
[3:0]	RESERVED	Reserved.	R

Page 0x2 Registers

GENERAL REGISTER

Page: 0x02, Address: 0x10, Reset: 0x1230, Name: GENERAL

The GENERAL register enables control of the various functions of the ADMT4000.
The GENERAL register is set to 0x1230 by default, which configures the device as follows:

- Convert start synchronization mode off.
- Angle filter enabled.
- Factory set 8th harmonic calibration coefficients.
- Continuous conversion mode.
- STORAGE[7:0] set to 0x00.

Table 19. Bit Description for the GENERAL Register

Bit	Bit Name	Description	Access
[15]	STORAGE[7]	Available for user data storage and part of ECC calculation.	R/W
[14:13]	CNVSYNC	Convert Start Synchronization Mode. 00: Sequencer controls the start of the sampling of the SINE and COSINE channels. 01: Not valid. 10: Not valid. 11: Synchronize sampling instants of SINE and COSINE channels to convert start edge.	R/W
[12]	ANGLFILT	Filter on Calculated Angle. 0: Filter disabled. 1: Filter enabled.	R/W
[11]	STORAGE[6]	Available for user data storage and part of ECC calculation.	R/W
[10]	H8CNTRL	8th Harmonic Correction Source. 0: ADI factory-set values.	R/W

Bit	Bit Name	Description	Access
		1: User-supplied values.	
[9]	RESERVED	This bit must be set 1.	R/W
[8:6]	STORAGE[5:3]	Available for user data storage and part of ECC calculation.	R/W
[5:4]	RESERVED	This bit must be set to 0b11.	R/W
[3:1]	STORAGE[2:0]	Available for user data storage and part of ECC calculation.	R/W
[0]	CNVMDE	Conversion Mode. 0: Continuous conversions. 1: One-shot conversion, sequencer stops at the end of the conversion sequence.	R/W

DIGITAL INPUT/OUTPUT ENABLE REGISTER

Page: 0x02, Address: 0x12, Reset: 0x201F, Name: DIGIOEN

All digital Input/Outputs can be used either in functional mode or GPIO mode. The relevant digital Input/Output pin can be configured as GPIO by setting the corresponding bit in the lower byte of this register high.

To enable the output drivers of the digital Input/Output pins, the bit for the corresponding pin must be set high. When the driver enable bit is set low and the function is set to GPIO the pin is configured as an input.

By default, DIGIOEN is configured to enable the BOOTLOAD output at power on.

Table 20. Bit Description for the DIGIOEN Register

Bit	Bit Name	Description	Access
[15:14]	RESERVED	Reserved.	R
[13]	DIGIO5EN	1: GPIO5 output enable. 0: GPIO5 output disable.	R/W
[12]	DIGIO4EN	1: GPIO4 output enable. 0: GPIO4 output disable.	R/W
[11]	DIGIO3EN	1: GPIO3 output enable. 0: GPIO3 output disable.	R/W
[10]	DIGIO2EN	1: GPIO2 output enable. 0: GPIO2 output disable.	R/W
[9]	DIGIO1EN	1: GPIO1 output enable. 0: GPIO1 output disable.	R/W
[8]	DIGIO0EN	1: GPIO0 output enable. 0: GPIO0 output disable.	R/W
[7:6]	RESERVED	Reserved.	R
[5]	DIGIO5FNC	1: GPIO5. 0: BOOTLOAD (output only).	R/W
[4]	DIGIO4FNC	1: GPIO4. 0: Reserved.	R/W
[3]	DIGIO3FNC	1: GPIO3.	R/W

Bit	Bit Name	Description	Access
		0: ACALC (output only).	
[2]	DIGIO2FNC	1: GPIO2. 0: Reserved.	R/W
[1]	DIGIO1FNC	1: GPIO1. 0: $\overline{\text{CNV}}$ (input only).	R/W
[0]	DIGIO0FNC	1: GPIO0. 0: BUSY (output only).	R/W

CONVERSION COUNT REGISTER

Page: 0x02, Address: 0x14, Reset: 0x0000, Name: CNVCNT

The CNVCT register stores the conversion count information and is updated every time a conversion sequence is completed. The conversion counter does not increment if the conversion sequence is aborted early by initiating a new conversion sequence whilst the current conversion sequence is executing. On reaching the full scale value of 0xFF, the counter wraps around to 0x00.

Table 21. Bit Description for the CNVCNT Register

Bit	Bit Name	Description	Access
[15:8]	RESERVED	Reserved.	R
[7:0]	CNVCNT	Conversion Count.	R

1ST HARMONIC ERROR CALIBRATION MAGNITUDE

Page: 0x02, Address: 0x15, Reset: 0x0000, Name: H1MAG

The H1MAG register stores the amplitude of the 1st harmonic error. The user must multiply the calculated harmonic coefficient by the CORDIC scaler of 0.6072 and write the resulting unsigned integer to the register. The LSB is $11.2455°/2^{11} = 0.005493°$.

Table 22. Bit Description for the H1MAG Register

Bit	Bit Name	Description	Access
[15:11]	RESERVED	Reserved.	R
[10:0]	H1MAG	1st Harmonic Error Amplitude.	R/W

1ST HARMONIC ERROR CALIBRATION PHASE

Page: 0x02, Address: 0x16, Reset: 0x0000, Name: H1PH

The H1PH register stores the phase of the 1st harmonic error as an unsigned integer with an LSB of $360°/2^{12} = 0.087891°$.

Table 23. Bit Description for the H1PH Register

Bit	Bit Name	Description	Access
[15:12]	RESERVED	Reserved.	R

Bit	Bit Name	Description	Access
[11:0]	H1PH	1st Harmonic Error Phase.	R/W

2ND HARMONIC ERROR CALIBRATION MAGNITUDE

Page: 0x02, Address: 0x17, Reset: 0x0000, Name: H2MAG

The H2MAG register stores the amplitude of the 2nd harmonic error. The user must multiply the calculated harmonic coefficient by the CORDIC scaler of 0.6072 and write the resulting unsigned integer to the register. The LSB is $11.2455°/2^{11} = 0.005493°$.

Table 24. Bit Description for the H2MAG Register

Bit	Bit Name	Description	Access
[15:11]	RESERVED	Reserved.	R
[10:0]	H2MAG	2nd Harmonic Error Amplitude.	R/W

2ND HARMONIC ERROR CALIBRATION PHASE

Page: 0x02, Address: 0x18, Reset: 0x0000, Name: H2PH

The H2PH register stores the phase of the 2nd harmonic error as an unsigned integer with an LSB of $360°/2^{12} = 0.087891°$.

Table 25. Bit Description for the H2PH Register

Bit	Bit Name	Description	Access
[15:12]	RESERVED	Reserved.	R
[11:0]	H2PH	2nd Harmonic Error Phase.	R/W

3RD HARMONIC ERROR CALIBRATION MAGNITUDE

Page: 0x02, Address: 0x19, Reset: 0x0000, Name: H3MAG

The H3MAG register stores the amplitude of the 3rd harmonic error. The user must multiply the calculated harmonic coefficient by the CORDIC scaler of 0.6072 and write the resulting unsigned integer to the register. The LSB is $1.40076°/2^{8} = 0.005493°$.

Table 26. Bit Description for the H3MAG Register

Bit	Bit Name	Description	Access
[15:8]	RESERVED	Reserved.	R
[7:0]	H3MAG	3rd Harmonic Error Amplitude.	R/W

3RD HARMONIC ERROR CALIBRATION PHASE

Page: 0x02, Address: 0x1A, Reset: 0x0000, Name: H3PH

The H3PH register stores the phase of the 3rd harmonic error as an unsigned integer with an LSB of $360°/2^{12} = 0.087891°$.

Table 27. Bit Description for the H3PH Register

Bit	Bit Name	Description	Access
[15:12]	RESERVED	Reserved.	R
[11:0]	H3PH	3rd Harmonic Error Phase.	R/W

8TH HARMONIC ERROR CALIBRATION MAGNITUDE

Page: 0x02, Address: 0x1B, Reset: 0x0000, Name: H8MAG

The H8MAG register stores the amplitude of the 8th harmonic error. The user must multiply the calculated harmonic coefficient by the CORDIC scaler of 0.6072 and write the resulting unsigned integer to the register. The LSB is $1.40076°/2^8 = 0.005493°$.

Table 28. Bit Description for the H8MAG Register

Bit	Bit Name	Description	Access
[15:8]	RESERVED	Reserved.	R
[7:0]	H8MAG	8th Harmonic Error Amplitude.	R/W

8TH HARMONIC ERROR CALIBRATION PHASE

Page: 0x02, Address: 0x1C, Reset: 0x0000, Name: H8PH

The H8PH register stores the phase of the 8th harmonic error as an unsigned integer with an LSB of $360°/2^{12} = 0.087891°$.

Table 29. Bit Description for the H8PH Register

Bit	Bit Name	Description	Access
[15:12]	RESERVED	Reserved.	R
[11:0]	H8PH	8th Harmonic Error Phase.	R/W

ECCEDC

Page: 0x02, Address: 0x1D, Reset: 0x0000, Name: ECCEDC

The ECCEDC register stores the error correction and detection codes (ECC) required when the user-configuration registers are updated. The ECC provides single bit error correction and double bit error detection capability. The hex value of 0x000F should be included in the ECC calculation, as shown in Table 30.

Table 30. Bit Description for the ECCEDC Register

Bits	Bit Name	Description	Access
[15:8]	ECC_CONFIG1	ECC for: H3MAG[15:8] H3PH H8MAG H8PH	R/W
[7:0]	ECC_CONFIG0	ECC for: GENERAL DIGIOEN 0x000F H1MAG H1PH H2MAG H2PH H3MAG[7:0]	R/W

UNIQUE ID REGISTER 0

Page: 0x02, Address: 0x1E, Reset: 0xXXXX, Name: UNIQID0

Unique identification register 0.

Table 31. Bit Description for the UNIQID0 Register

Bit	Bit Name	Description	Access
[15:0]	UNIQID0	Unique Device Identification 0.	R

UNIQUE ID REGISTER 1

Page: 0x02, Address: 0x1F, Reset: 0xXXXX, Name: UNIQID1

Unique identification register 1.

Table 32. Bit Description for the UNIQID1 Register

Bit	Bit Name	Description	Access
[15:0]	UNIQID1	Unique Device Identification 1.	R

UNIQUE ID REGISTER 2

Page: 0x02, Address: 0x20, Reset: 0xXXXX, Name: UNIQID2

Unique identification register 2.

Table 33. Bit Description for the UNIQID2 Register

Bit	Bit Name	Description	Access
[15:0]	UNIQID2	Unique Device Identification 2.	R

UNIQUE ID REGISTER 3

Page: 0x02, Address: 0x21, Reset: 0x0002 Name: UNIQID3

Unique identification register 3.

Table 34. Bit Description for the UNIQID3 Register

Bit	Bit Name	Description	Access
[15:11]	RSDV	Reserved.	R
[10:8]	ID_PROD	Product Identifier.	R
[7:6]	ID_SUPY	Voltage Supply Identifier.	R
[5:3]	RSDV	Reserved.	R
[2:0]	ID_REVN	ASIC Silicon Revision.	R

ECC DISABLE

Page: 0x02, Address: 0x23, Reset: 0xXXXX, Name: ECCDIS

The ECCDIS register is used to disable single bit error correction of the user-configuration registers. The user must disable ECC before updating the configuration registers (see the ECCEDC register description) by setting the contents of the ECCDIS register to 0x4D54. Once the configuration registers have been updated, and the new ECC code added to the ECCEDC register, ECC must be reenabled by writing a value other than 0x4D54 to the ECCDIS register, it is recommended that a value of 0x0000 is used.

Table 35. Bit Description for the ECCDIS Register

Bit	Bit Name	Description	Access
[15:0]	ECCDIS	Set to 0x4D54 to disable ECC on the configuration registers. Set to 0x0000 to enable ECC on the configuration registers.	R/W

APPLICATIONS

Rotational Speed Considerations

With the filter enabled, there is a latency between the current angle of the system and the angle reported. The worst-case error due to the latency is dependent on the maximum speed of the system. The worst-case error in degrees is $864 \times 10^{-6} \times$ rotation speed (rpm), in addition to latency due to the SPI interface.

Magnet Considerations

The maximum and minimum field strength that can be used with the ADMT4000 is bounded, defined by the red and blue curves (B_{MAX} and B_{MIN}) in Figure 25 for NdFeB and Figure 26 for SmCo. As shown in the plot, this usable field strength range is temperature dependent. The operating magnetic field range is measured in the x, y plane of the sensor at the center of the GMR (turn count) sensor, as shown in Figure 30. The z component of the external magnetic field does not influence the behavior of the GMR turn count or AMR angle sensor.

To extend the operating temperature range of the system, the user must consider the selection of the system magnet. The temperature coefficient of the magnetic field strength of a magnet is a characteristic of the magnetic material. Typical examples of a NdFeB and a SmCo magnet are shown in Figure 25 and Figure 26 alongside the typical maximum operating range of the ADMT4000. The green shaded areas in Figure 25 and Figure 26 show the expected performance of a typical NdFeB and SmCo magnet, including temperature variation and manufacturing tolerances. The design of the green shaded region must ensure that the magnetic flux density never goes beyond the B_{MAX} and B_{MIN} limits, under worst-case conditions of mechanical tolerances, stray magnetic field influence, temperature, and lifetime.

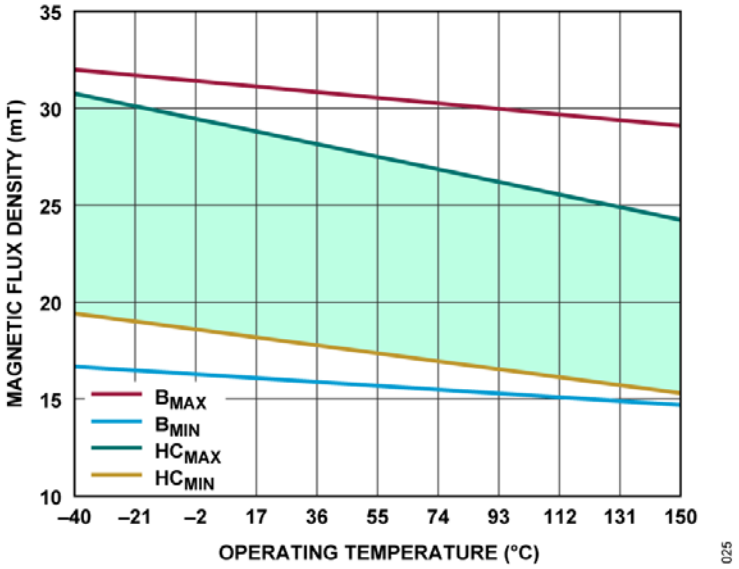


Figure 25. Typical NdFeB Magnet Performance vs. Magnetic Operating Window of the GMR Turn Count Sensor

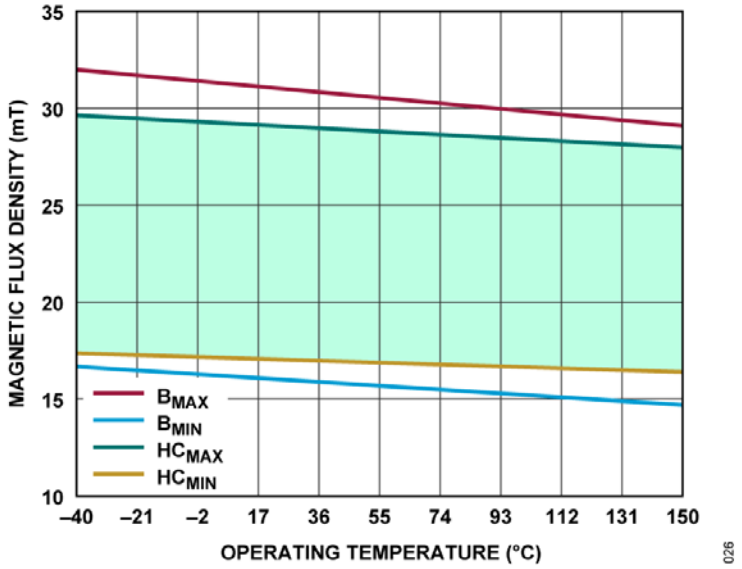


Figure 26. Typical SmCo Magnet Performance vs. Magnetic Operating Window of the GMR Turn Count Sensor

The turn count error rate is determined by the constant magnetic flux density that the GMR turn count sensor is exposed to. Figure 27 shows the error rate for 1 million parts vs. the magnetic flux density for the various number of expected cycles in the target application. For example, a constant magnetic flux density of 16 mT is required to ensure less than 1 failure per 1 million parts after 10 million cycles per part.

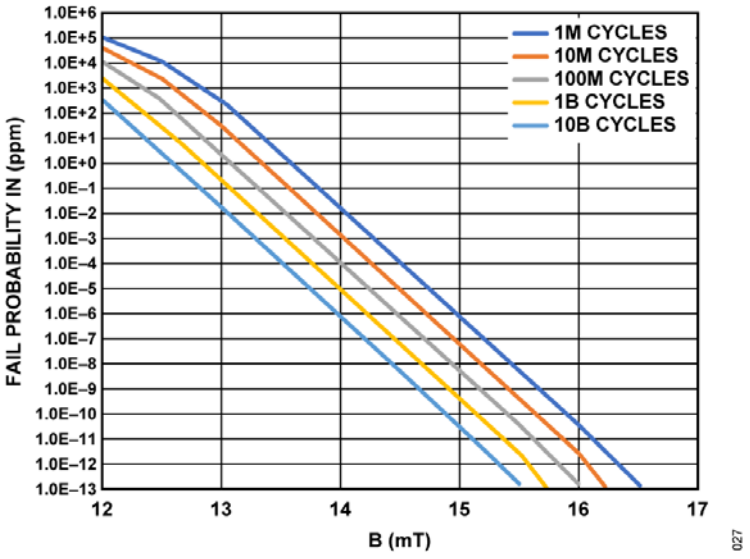


Figure 27. Minimum Magnetic Feld Strength on the GMR Turn Count Sensor vs. Error Rate

Typical System Configuration

Figure 28 and Figure 29 show how the ADMT4000 can be configured to operate in the case where GPIO functions are used and when they are not required,

In the case where the GPIO functions are not required, Figure 28, the GPIO ports must be configured as digital inputs and connected to GND through a 100 kΩ resistor. Pin 4, Bootload, must be connected to VDRIVE by 100 kΩ resistor, since at power up, the BOOTLOAD function is set by default. Figure 29 shows the case where the GPIO

functions are required, in this case, the GPIOs are set to outputs except for Pin 20, $\overline{\text{CNV}}$, which has been configured as the convert start input.

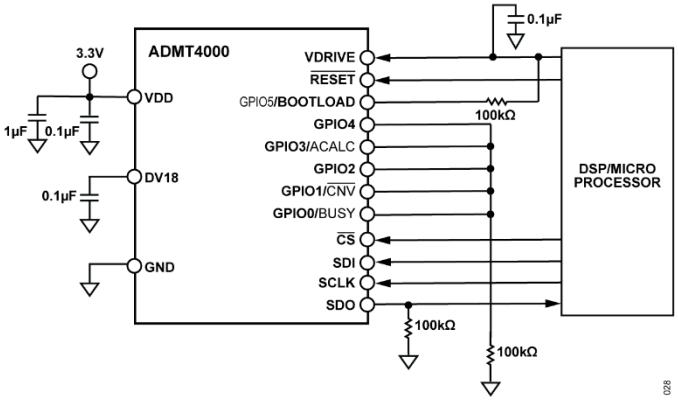


Figure 28. Typical System Configuration for the Case where no GPIO Functions are Required

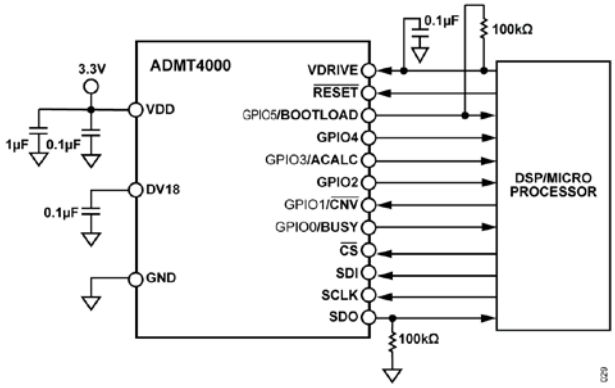


Figure 29. Typical System Configuration for the Case where GPIO Functions are Required

OUTLINE DIMENSIONS

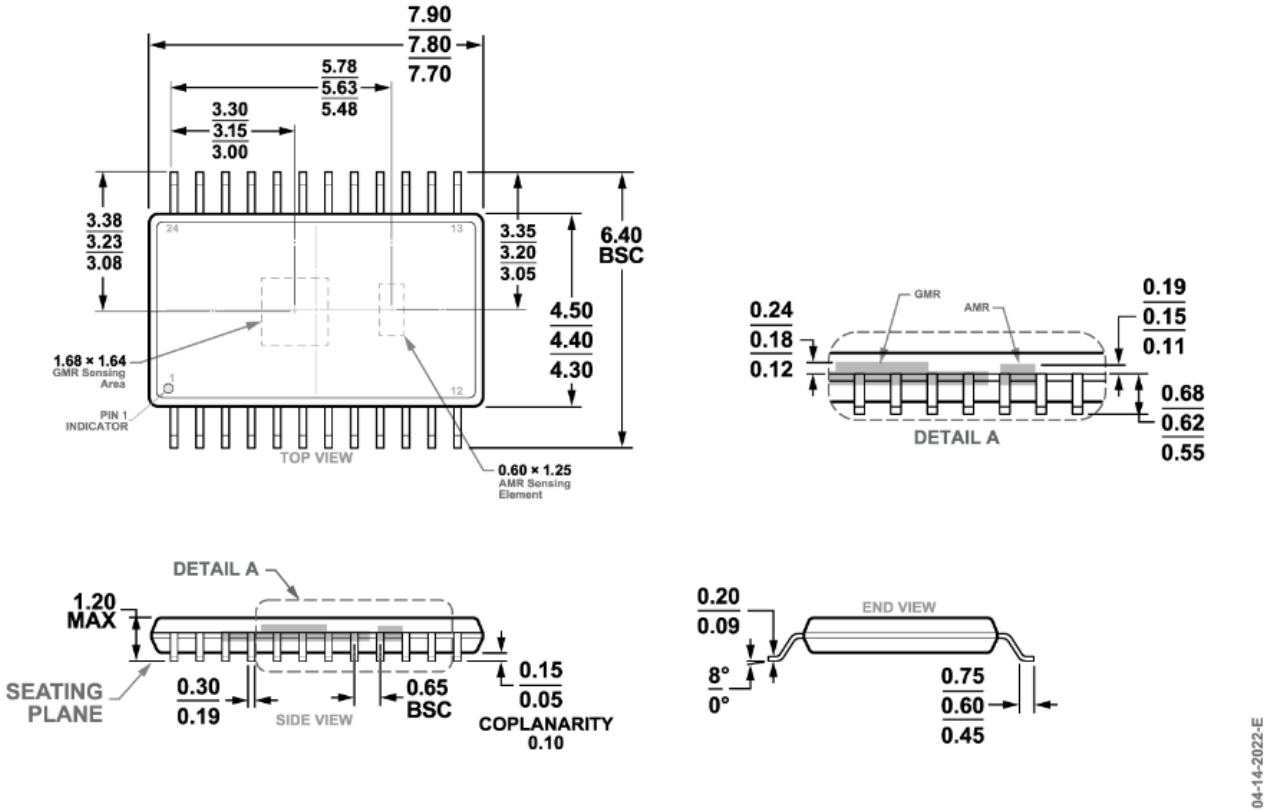


Figure 30. 24-Lead Thin Shrink Small-Outline Package [TSSOP]
(RU-24)
Dimensions Shown in millimeters

ORDERING GUIDE

Table 36. Ordering Guide

Model	Temperature Range	Package Description	Package Option
ADMT4000BRUZAB	−40°C to +125°C Ambient	24-Lead TSSOP, 3.3 V	RU-24

NOTES

ALL INFORMATION CONTAINED HERE IN IS PROVIDED “AS IS” WITHOUT REPRESENTATION OR WARRANTY. NO RESPONSIBILITY IS ASSUMED BY ANALOG DEVICES FOR ITS USE, NOR FOR ANY INFRINGEMENTS OF PATENTS OR OTHER RIGHTS OF THIRD PARTIES THAT MAY RESULT FROM ITS USE. SPECIFICATIONS ARE SUBJECT TO CHANGE WITHOUT NOTICE. NO LICENCE, EITHER EXPRESSED OR IMPLIED, IS GRANTED UNDER ANY ADI PATENT RIGHT, COPYRIGHT, MASK WORK RIGHT, OR ANY OTHER ADI INTELLECTUAL PROPERTY RIGHT RELATING TO ANY COMBINATION, MACHINE, OR PROCESS WHICH ADI PRODUCTS OR SERVICES ARE USED. TRADEMARKS AND REGISTERED TRADEMARKS ARE THE PROPERTY OF THEIR RESPECTIVE OWNERS.