Data Sheet

ADM6840

Adjustable Hex/Octal Sequencer-Supervisor with Reverse Power-Down and Daisy-Chain Capability

FEATURES

- 2.7V to 15V Wide Operating Voltage Range
- Monitor Up to Eight Voltages
- Sequence Up to Eight Voltages
- Power-Off in Reverse Order or Simultaneously
- Unlimited Daisy-Chain
- Capacitor-Adjustable Sequence Delay
- Factory-Trimmable Options Power-Good Timeout
- Resistor-Programmable Power-Supply ON Threshold (V_{SEQON_TH})
- Factory-Trimmable Options Power-Supply OFF Thresholds (V_{SEQOFF_TH})
- 0.8% Accuracy Voltage Monitoring Threshold (V_{MON_TH})
- Open-Drain Output
- POK Output for System Microcontroller Reset
- DONE Output for Sequencing Done Signal
- Bidirectional $\overline{FAULT}$ Input/Output
- 25-Bump WLP, 24L and 28L TQFN Package
- -40°C to +125°C Operating Temperature Range

APPLICATIONS

- Telecom Equipment
- Test Equipment
- Servers and Network Cards
- Healthcare Imaging
- Industrial Sensors and Motor Controls
- FPGA/ASIC Power Supply Sequencing
- Microprocessor and Microcontroller Sequencing
- Multi-Supply Sequencing

GENERAL DESCRIPTION

The ADM6840 is a sequencer and a supervisor that can sequence and monitor up to six or eight voltages. This device provides an adjustable delay when each supply is turned on and monitors the voltage of each power supply.

The ADM6840 operates from a supply range of 2.7V to 15V and has an internal regulator output (ABP) that supplies power to internal circuits.

The sequencing is enabled by two inputs, ON and $\overline{OFF}$. A rising edge on the ON input initiates power-on sequencing of the channels, whereas a falling edge on the $\overline{OFF}$ Input initiates power-off sequencing. During the power-on sequencing, when all the voltages reach their final values, the DONE output asserts high, followed by the Power-OK (POK) output after the reset timeout period (t_{RP}) has expired, allowing the microcontroller to operate. If any voltage falls below its monitor threshold (V_{MON_TH}), the POK asserts low, and all outputs disable simultaneously, turning off all sequenced power supplies. When the sequencer initiates power-off sequencing, the ADM6840 can reverse-sequence the outputs.

The ADM6840 is an open-drain reset output and can be daisy-chained indefinitely to control any number of voltages in a system.

The ADM6840 features a bidirectional active-low $\overline{FAULT}$ input/output, which asserts low during any fault condition. It is a one-shot pulse output during any fault conditions. An external signal pulling $\overline{FAULT}$ low disables all outputs immediately. The ADM6840 is available in a 2.46mm x 2.46mm, 25-bump Wafer-Level Package (WLP) (0.5 mm pitch), a 4mm x 4mm (24L), and a 5mm x 5mm (28L) TQFN package. The device is fully specified over the -40°C to +125°C operating temperature range.

One Analog Way, Wilmington, MA 01887-2356, U.S.A. | Tel: 781.329.4700

SIMPLIFIED APPLICATION DIAGRAM

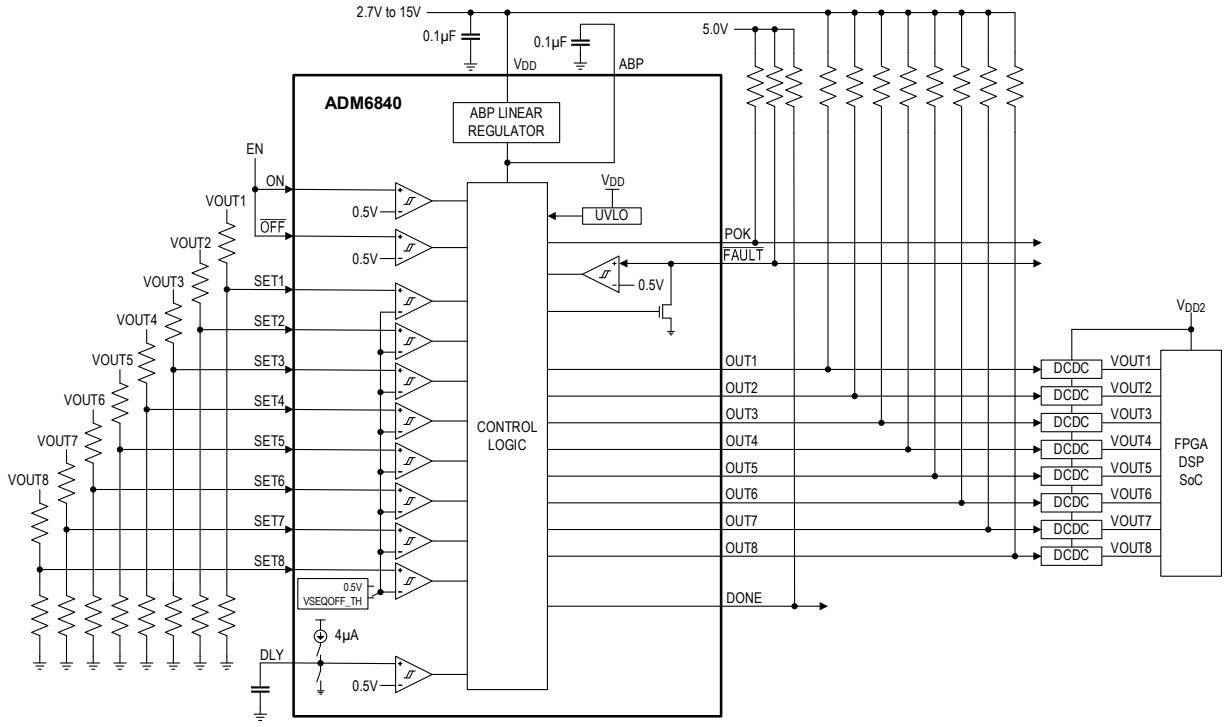


Figure 1. ADM6840E Simplified Application Diagram

REVISION HISTORY

3/2026 – Rev. 0: Initial Release

5/2026 – Rev. A: Updated Table 3 on page 7

SPECIFICATIONS

Table 1. Electrical Characteristics

(V_{DD} = 2.7V to 15V, V_{ON} = V_{OFF} = V_{ABP}, T_A = -40°C to +125°C, unless otherwise noted. Typical values are at T_A = +25°C.[1])

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Operating Voltage Range	V_{DD}		2.7		15	V
Undervoltage Lockout	V_{UVLO}	Minimum supply voltage (V_{DD}) V_{DD} falling	2.3	2.4	2.5	V
Undervoltage Lockout Hysteresis	V_{UVLO_HYS}	V_{DD} rising		100		mV
Regulated Supply Voltage	V_{ABP}	ABP to GND = 0.1µF		1.8		V
Supply Current	I_{DD}	V_{DD} = 5V, all OUT_ = HIGH, no load		240	370	µA
ON, $\overline{OFF}$ INPUTS						
ON Input Threshold	V_{ON_TH}	ON rising (0.8% accuracy)	0.496	0.5	0.504	V
$\overline{OFF}$ Input Threshold	V_{OFF_TH}	$\overline{OFF}$ falling (0.8% accuracy)	0.496	0.5	0.504	V
ON Input Threshold Hysteresis	$V_{ON\_TH\_HYS}$			1		$\%V_{ON\_TH}$
$\overline{OFF}$ Input Threshold Hysteresis	$V_{OFF\_TH\_HYS}$			1		$\%V_{OFF\_TH}$
ON, $\overline{OFF}$ Threshold Tempco	V_{TH_TC}			30		ppm/°C
ON, $\overline{OFF}$ Input Current	I_{ON}, I_{OFF}	V_{ON} = V_{OFF} = 0V and 5V	-100		+100	nA
MONITORED ANALOG INPUTS (SET_)						
SET Monitor Threshold	V_{MON_TH}		0.496	0.5	0.504	V
SET_ Monitor Threshold Accuracy	$V_{MON\_TH\_ACC}$	SET_ falling	-0.8		+0.8	%
SET_ Monitor Threshold Hysteresis	$V_{MON\_TH\_HYS}$	SET_ rising		1		$\%V_{TH}$
SET_ Sequence $\overline{OFF}$ Threshold	V_{SEQOFF_TH}	67%V_{MON_TH} (ADM6840_ _ _B_ _)	0.315	0.333	0.351	V
		33%V_{MON_TH} (ADM6840_ _ _C_ _)	0.149	0.167	0.185	V
		10%V_{MON_TH} (ADM6840_ _ _D_ _)	0.032	0.050	0.068	V
SET_ Threshold Tempco				30		ppm/°C
SET_ Input Current	I_{SET}	$V_{SET\_}$ = 0V and 5V	-100		+100	nA
DELAY TIMER (DLY)						
Source Current	I_{DLY}	-40°C to +125°C	3.8	4.0	4.2	µA
Voltage Threshold	V_{DLY_TH}			0.5		V

(V_{DD} = 2.7V to 15V, V_{ON} = V_{OFF} = V_{ABP}, T_A = -40°C to +125°C, unless otherwise noted. Typical values are at T_A = +25°C.[1])

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
SEQUENCER OUTPUTS (OUT_)						
OUT_ Output Voltage Low	V_{OUTL}	I_{SINK} = 3.2mA			0.3	V
OUT_ Leakage Current	I_{OUT_LKG}				1	µA
$\overline{\text{FAULT}}$ INPUT/OUTPUT						
$\overline{\text{FAULT}}$ Output Voltage Low	V_{FAULTL}	I_{SINK} = 3.2mA			0.3	V
$\overline{\text{FAULT}}$ Leakage Current	I_{FAULT_LKG}	$\overline{\text{FAULT}}$ = HIGH, V_{FAULT} = 5V			1	µA
$\overline{\text{FAULT}}$ Input Threshold	V_{FAULT_TH}	$\overline{\text{FAULT}}$ falling		0.5		V
POWER-OK OUTPUT (POK)						
POK Output Voltage Low	V_{POKL}	I_{SINK} = 3.2mA			0.3	V
POK Leakage Current	I_{POK_LKG}	POK = HIGH, V_{POK} = 5V			1	µA
DONE OUTPUT (DONE)						
DONE Output Voltage Low	V_{DONEL}	I_{SINK} = 3.2mA			0.3	V
DONE Leakage Current	I_{DONE_LKG}	POK = HIGH, V_{DONE} = 5V			1	µA
TIMING						
POK Reset Timeout Accuracy	t_{RP_ACC}		-15		+15	%
Power Good Timer Accuracy	t_{PGT_ACC}		-15		+15	%
ON Input Pulse Width	t_{ON_PW}	ON rising	6			µs
$\overline{\text{OFF}}$ Input Pulse Width	t_{OFF_PW}	$\overline{\text{OFF}}$ falling	6			µs
External $\overline{\text{FAULT}}$ Input Pulse Width	t_{FAULT_PW}	$\overline{\text{FAULT}}$ falling	6			µs
ON Input, $\overline{\text{OFF}}$ Input, External $\overline{\text{FAULT}}$ Input Transient Immunity					1	µs
$\overline{\text{FAULT}}$ Output Hold Timeout	t_{FAULT_HOLD}		68	80	92	µs
SET_ to $\overline{\text{FAULT}}$, OUT_ Low Delay Time	t_{SET_FAULT}	SET_ falling below V_{TH}		1		µs
External $\overline{\text{FAULT}}$ to OUT_ Low Delay Time	t_{FAULT_OUT}	$\overline{\text{FAULT}}$ falling below V_{TH}		9		µs
ON to $\overline{\text{FAULT}}$, OUT_ Low Delay Time	t_{ON_FAULT}	ON rising above V_{TH}		9		µs
$\overline{\text{OFF}}$ to $\overline{\text{FAULT}}$, OUT_ Low Delay Time	t_{OFF_FAULT}	$\overline{\text{OFF}}$ falling below V_{TH}		9		µs

[1] Devices are tested at T_A = +25°C and are guaranteed by design for T_A = -40°C to +125°C—single-pass flow.

Timing Diagrams

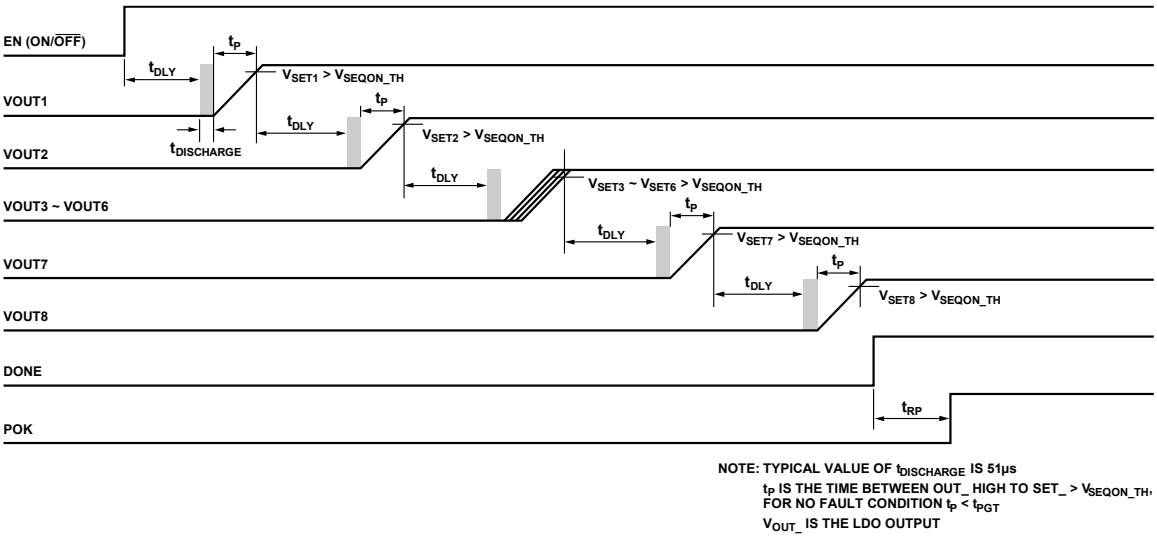


Figure 2. Power-On Sequence and Monitoring Timing Diagram (see the Application Circuit in Figure 35)

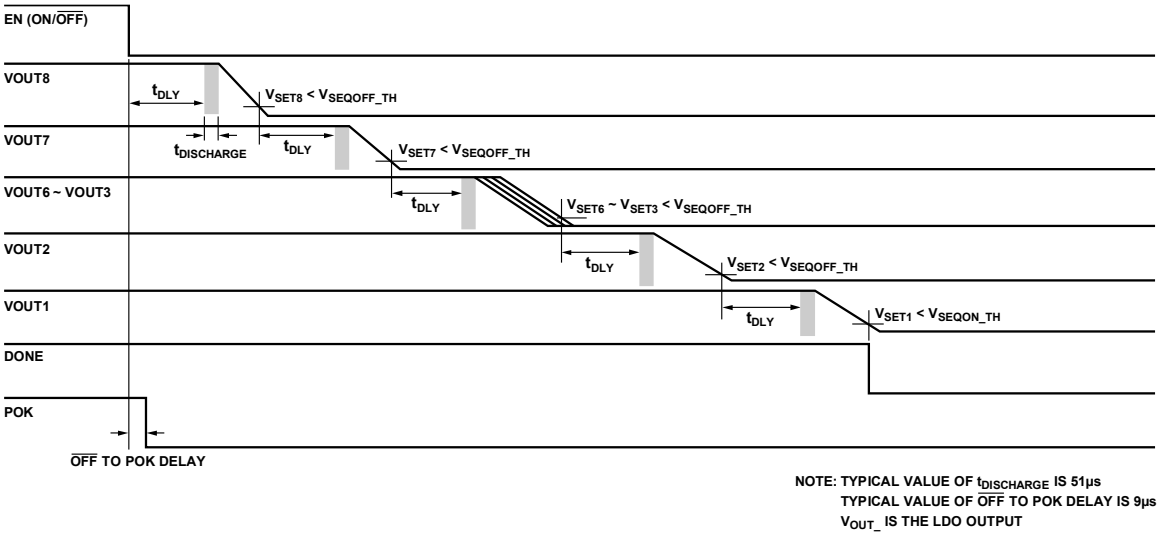


Figure 3. Power-Off Sequence and Monitoring Timing Diagram (see the Application Circuit in Figure 35)

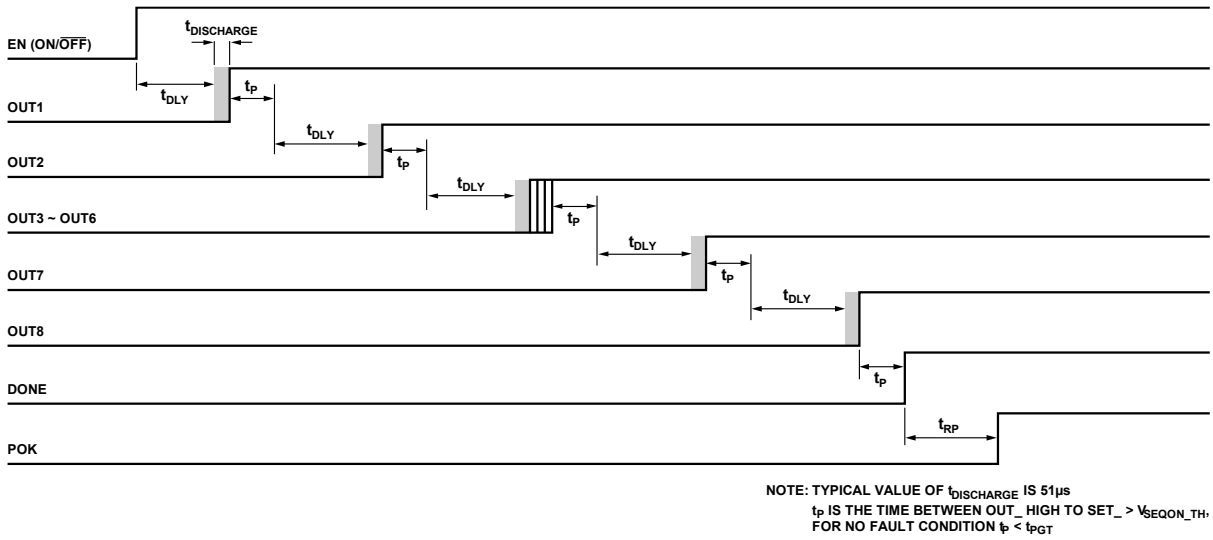


Figure 4. Power-On Sequencing Timing Diagram (see the Application Circuit in Figure 36)

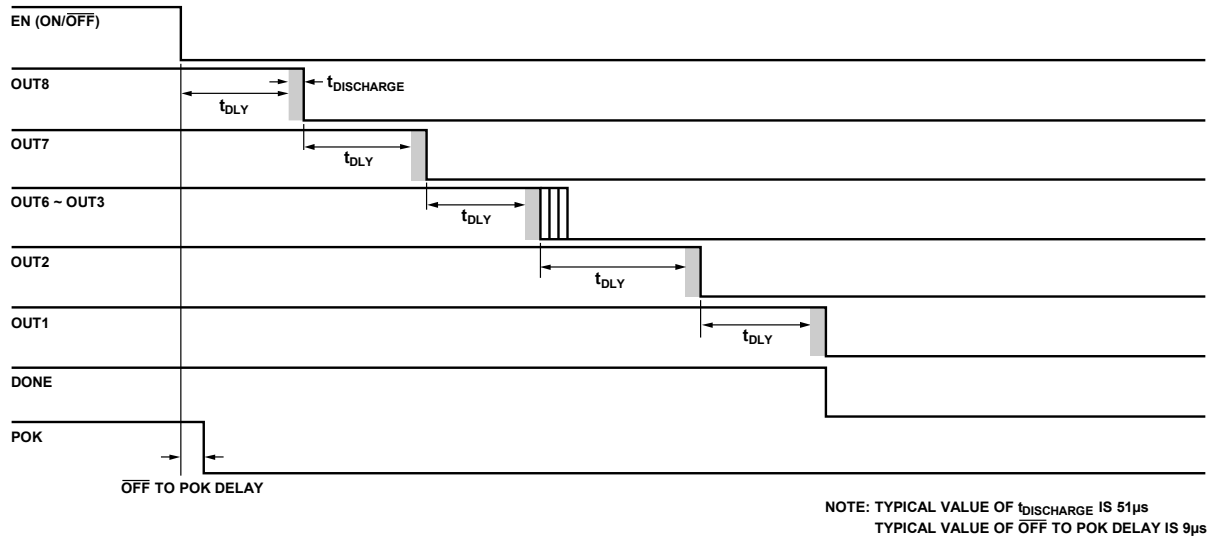


Figure 5. Power-Off Sequencing Timing Diagram (see the Application Circuit in Figure 36)

ABSOLUTE MAXIMUM RATINGS

T_A = +25°C unless otherwise specified.

Table 2. Absolute Maximum Ratings

PARAMETER	RATING
V_{DD}, OUT_ to GND	-0.3V to +22V
ABP, DLY to GND	-0.3V to +2.2V
DONE, POK, $\overline{FAULT}$, ON, $\overline{OFF}$, SET_ to GND	-0.3V to +6V
Input/Output Current	36mA
Continuous Power Dissipation, WLP, Multilayer board (T_A = +70°C, derate 22.73mW/°C above +70°C)	1819mW
Continuous Power Dissipation, 28L TQFN, Multilayer board (T_A = +70°C, derate 34.50mW/°C above +70°C)	2759mW
Continuous Power Dissipation, 24L TQFN, Multilayer board (T_A = +70°C, derate 27.80mW/°C above +70°C)	2222mW
Operating Temperature Range	-40°C to +125°C
Junction Temperature	+150°C
Storage Temperature Range	-55°C to +150°C
Soldering Temperature (reflow)	+260°C

Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

Electrostatic Discharge (ESD)

The following ESD information is provided for handling of ESD-sensitive devices in an ESD protected area only. Human body model (HBM) per ANSI/ESDA/JEDEC JS-001. Field induced charged device model (FICDM) per ANSI/ESDA/JEDEC JS-002.

ESD Ratings for ADM6840

Table 3. ADM6840, 25-Bump WLP

ESD MODEL	WITHSTAND THRESHOLD (V)	CLASS
HBM	±3000	2
FICDM	±500	C2a

ESD Caution

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PACKAGE INFORMATION

Table 4. Package Information

WLP	
Package Code	W252Y2+1
Outline Number	*21-100778*
Land Pattern Number	Refer to *Application Note 1891*
Thermal Resistance, Multi-Layer Board:	
Junction-to-Ambient (θ_{JA})	43.98°C/W

28L TQFN	
Package Code	T2855+6C
Outline Number	*21-0140*
Land Pattern Number	*90-0026*
Thermal Resistance, Multi-Layer Board:	
Junction-to-Ambient (θ_{JA})	29°C/W

24L TQFN	
Package Code	T2444+4C
Outline Number	*21-0139*
Land Pattern Number	*90-0022*
Thermal Resistance, Multi-Layer Board:	
Junction-to-Ambient (θ_{JA})	36°C/W

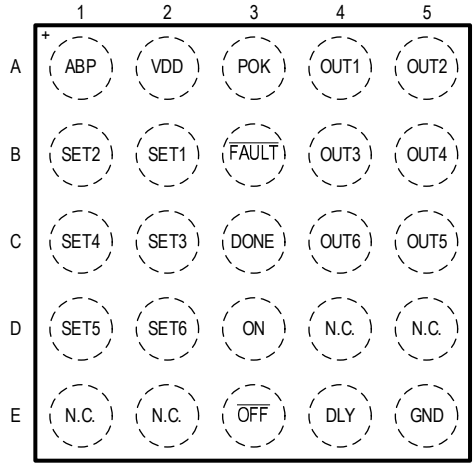
For the latest package outline information and land patterns (footprints), go to *Package Index*. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to *Thermal Characterization of IC Packages*.

PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS

ADM6840S 25-Bump WLP

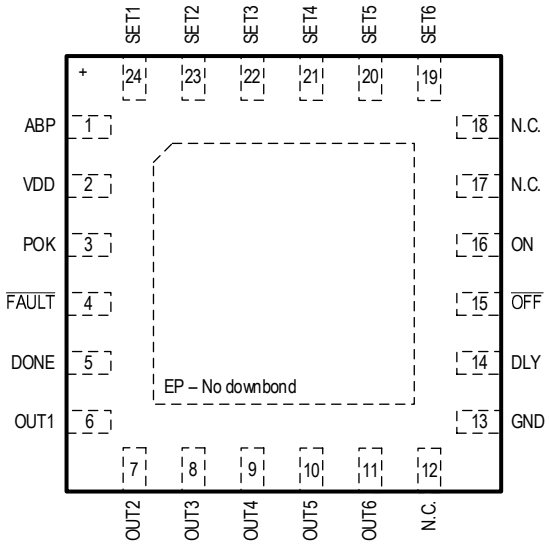
TOP VIEW
(BUMP SIDE DOWN)



WLP (2.46mm x 2.46mm)

ADM6840S 24L TQFN

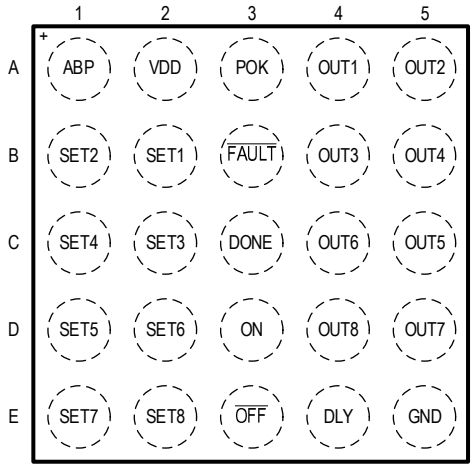
TOP VIEW



THIN QFN (4mm x 4mm)

ADM6840E 25-Bump WLP

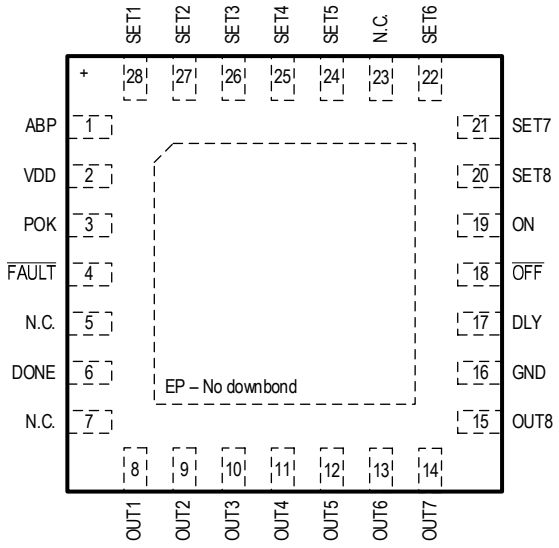
TOP VIEW
(BUMP SIDE DOWN)



WLP (2.46mm x 2.46mm)

ADM6840E 28L TQFN

TOP VIEW



THIN QFN (5mm x 5mm)

Pin Descriptions

Table 5. Pin Descriptions

PIN				NAME	DESCRIPTION	TYPE
ADM6840S WLP	ADM6840S 24L TQFN	ADM6840E WLP	ADM6840E 28L TQFN			
A1	1	A1	1	ABP	Internal Supply Bypass Input. Connect a 0.1µF capacitor from ABP to GND. ABP is an internally generated voltage that powers internal circuits. Do not connect to external circuitry; leave unconnected or short to GND.	Power
A2	2	A2	2	V_{DD}	Device Power-Supply Input. Connect to 2.7V to 15V. Bypass V_{DD} to GND with a 0.1µF capacitor.	Power
A3	3	A3	3	POK	Open-Drain Power-OK Output. During power-on sequencing, when SET6 (ADM6840S)/SET8 (ADM6840E) voltage rises above 0.5V, the output changes from low-impedance to high-impedance after the reset timeout period. This output is driven low if the voltage on any SET input drops below 0.5V or when $\overline{FAULT}$ is pulled low by an external signal. POK requires an external pull-up resistor.	Digital Output
A4	6	A4	8	OUT1	Open-Drain Output 1. Upon power-on sequencing (ON input rises from low to above 0.5V), OUT1 changes from low to high-impedance after the sequence delay t_{DLY}. During power-off sequencing, when the voltage at the SET2 pin falls below 0.5V, OUT1 switches from high-impedance to low-impedance after a sequence delay t_{DLY}. OUT1 requires an external pull-up resistor.	Digital Output
A5	7	A5	9	OUT2	Open-Drain Output 2. During power-on sequencing, when the voltage at SET1 rises	Digital Output

PIN				NAME	DESCRIPTION	TYPE
ADM6840S WLP	ADM6840S 24L TQFN	ADM6840E WLP	ADM6840E 28L TQFN			
					above threshold voltage (rising), OUT2 changes from low-impedance to high-impedance after sequence delay t_{DLY} During power-off sequencing, when the voltage at the SET3 pin falls below 0.5V, OUT2 switches from high-impedance to low-impedance after the sequence delay t_{DLY}. OUT2 requires an external pull-up resistor.	
B1	23	B1	27	SET2	Set Monitored Threshold 2 Input. Monitor a voltage by setting the threshold with an external resistive divider. The SET2 threshold is 0.5V. To disable Channel 2, connect SET2 to ABP. Do not leave SET2 unconnected or short to GND.	Analog Input
B2	24	B2	28	SET1	Set Monitored Threshold 1 Input. Monitor a voltage by setting the threshold with an external resistive divider. The SET1 threshold is 0.5V. To disable Channel 1, connect SET1 to ABP. Do not leave SET1 unconnected or short to GND.	Analog Input
B3	4	B3	4	$\overline{\text{FAULT}}$	Bidirectional Input and Active-Low Open-Drain Output. When an internal fault is detected, this pin is asserted low. An external signal pulling this pin low disables all outputs and sets the ADM6840 to the initialization state.	Digital Input/Output
B4	8	B4	10	OUT3	Open-Drain Output 3. During power-on sequencing, when the voltage at SET2 rises above the threshold voltage (rising), OUT3 changes from low-impedance to high-impedance after sequence delay t_{DLY}.	Digital Output

PIN				NAME	DESCRIPTION	TYPE
ADM6840S WLP	ADM6840S 24L TQFN	ADM6840E WLP	ADM6840E 28L TQFN			
					During power-off sequencing, when the voltage at the SET4 pin falls below 0.5V, OUT3 switches from high-impedance to low-impedance after a sequence delay t_{DLY}. OUT3 requires an external pull-up resistor.	
B5	9	B5	11	OUT4	Open-Drain Output 4. During power-on sequencing, when the voltage at SET3 rises above the threshold voltage (rising), OUT4 changes from low to high-impedance after a sequence delay t_{DLY}. During power-off sequencing, when the voltage at the SET5 pin falls below 0.5V, OUT4 switches from high-impedance to low-impedance after a sequence delay t_{DLY}. OUT4 requires an external pull-up resistor.	Digital Output
C1	21	C1	25	SET4	Set Monitored Threshold 4 Input. Monitor a voltage by setting the threshold with an external resistive divider. The SET4 threshold is 0.5V. To disable Channel 4, connect SET4 to ABP. Do not leave SET4 unconnected or short to GND.	Analog Input
C2	22	C2	26	SET3	Set Monitored Threshold 3 Input. Monitor a voltage by setting the threshold with an external resistive divider. The SET3 threshold is 0.5V. To disable Channel 3, connect SET3 to ABP. Do not leave SET3 unconnected or short to GND.	Analog Input
C3	5	C3	6	DONE	Open-Drain Sequencing Done Output. When power-on sequencing is complete, DONE changes from low-impedance to high-impedance. During power-off	Digital Output

PIN				NAME	DESCRIPTION	TYPE
ADM6840S WLP	ADM6840S 24L TQFN	ADM6840E WLP	ADM6840E 28L TQFN			
					sequencing, the pin remains high-impedance until the SET1 voltage falls below its threshold. When a fault occurs, this pin is asserted low.	
C4	11	C4	13	OUT6	Open-Drain Output 6. During power-on sequencing, when the voltage at SET5 rises above the threshold (rising), OUT6 changes from low-impedance to high-impedance after the sequence delay t_{DLY}. During power-off sequencing, when the voltage at $\overline{OFF}$ (ADM6840S)/SET7 (ADM6840E) falls below 0.5V, OUT6 switches from high-impedance to low after sequence delay t_{DLY}. OUT6 requires an external pull-up resistor.	Digital Output
C5	10	C5	12	OUT5	Open-Drain Output 5. During power-on sequencing, when the voltage at SET4 rises above the threshold voltage (rising), OUT5 changes from low-impedance to high-impedance after a sequence delay t_{DLY}. During power-off sequencing, when the voltage at the SET6 pin falls below 0.5V, OUT5 switches from high-impedance to low-impedance after a sequence delay t_{DLY}. OUT5 requires an external pull-up resistor.	Digital Output
D1	20	D1	24	SET5	Set Monitored Threshold 5 Input. Monitor a voltage by setting the threshold with an external resistive divider. The SET5 threshold is 0.5V. To disable Channel 5, connect SET5 to ABP. Do not leave SET5 unconnected or short to GND.	Analog Input
D2	19	D2	22	SET6	Set Monitored Threshold 6 Input.	Analog Input

PIN				NAME	DESCRIPTION	TYPE
ADM6840S WLP	ADM6840S 24L TQFN	ADM6840E WLP	ADM6840E 28L TQFN			
					Monitor a voltage by setting the threshold with an external resistive divider. The SET6 threshold is 0.5V. To disable Channel 6, connect SET6 to ABP. Do not leave SET6 unconnected or short to GND.	
D3	16	D3	19	ON	Non-inverting Comparator Input. A rising voltage above 0.5V on this pin initiates power-on sequencing.	Digital Input
—	—	D4	15	OUT8	Open-Drain Output 8. During power-on sequencing, when the voltage at SET7 rises above the threshold voltage (rising), OUT8 changes from low-impedance to high-impedance after a sequence delay t_{DLY}. During power-off sequencing, when the voltage at $\overline{OFF}$ falls below 0.5V, OUT8 switches from high-impedance to low-impedance after a sequence delay t_{DLY}. OUT8 requires an external pull-up resistor.	Digital Output
—	—	D5	14	OUT7	Open-Drain Output 7. During power-on sequencing, when the voltage at SET6 rises above the threshold voltage (rising), OUT7 changes from low-impedance to high-impedance after a sequence delay t_{DLY}. During power-off sequencing, when the voltage at the SET8 pin falls below 0.5V, OUT7 switches from high-impedance to low-impedance after a sequence delay t_{DLY}. OUT7 requires an external pull-up resistor.	Digital Output
—	—	E1	21	SET7	Set Monitored Threshold 7 Input. Monitor a voltage by setting the threshold with an external resistive divider. The SET7	Analog Input

PIN				NAME	DESCRIPTION	TYPE
ADM6840S WLP	ADM6840S 24L TQFN	ADM6840E WLP	ADM6840E 28L TQFN			
					threshold is 0.5V. To disable Channel 7, connect SET7 to ABP. Do not leave SET7 unconnected or short to GND.	
—	—	E2	20	SET8	Set Monitored Threshold 8 Input. Monitor a voltage by setting the threshold with an external resistive divider. The SET8 threshold is 0.5V. To disable Channel 8, connect SET8 to ABP. Do not leave SET8 unconnected or short to GND.	Analog Input
E3	15	E3	18	$\overline{\text{OFF}}$	Noninverting Comparator Input. A falling voltage below 0.5V on this pin initiates power-off sequencing. Do not leave the pin unconnected or open.	Digital Input
E4	14	E4	17	DLY	Adjustable Sequence Delay Timing Input. Connect a capacitor from DLY to GND to set the sequence delay between each OUT. Leave DLY unconnected for a 58µs (typ) delay.	Analog Input
E5	13	E5	16	GND	Ground	Ground
D4, D5, E1, E2	12, 17, 18	—	5, 7, 23	N.C.	No Connect. Leave the N.C. pins unconnected or open. Do not connect to any potential (ground or power supply).	—
—	—	—	—	EP	Exposed Pad. Connect to the GND plane for improved heat dissipation. Do not use EP as the only ground connection.	—

TYPICAL PERFORMANCE CHARACTERISTICS

V_{DD} = 5V, V_{ON} = V_{OFF} = V_{ABP}, all OUT_ = HIGH, T_A = 25°C, unless otherwise noted.

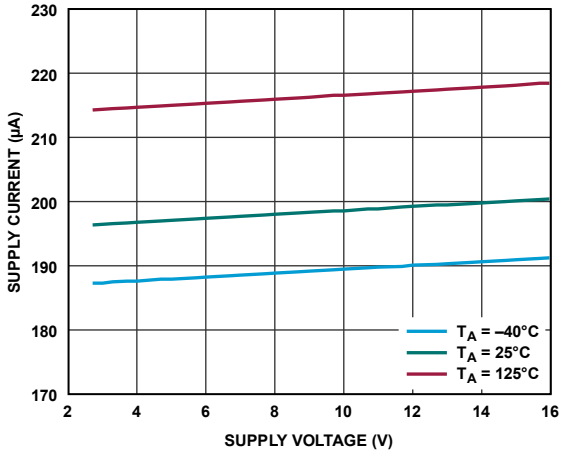


Figure 6. Supply Current vs. Supply Voltage

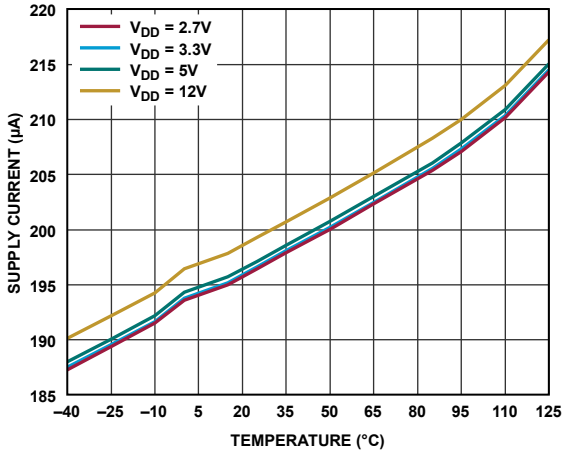


Figure 7. V_{DD} Supply Current vs. Temperature

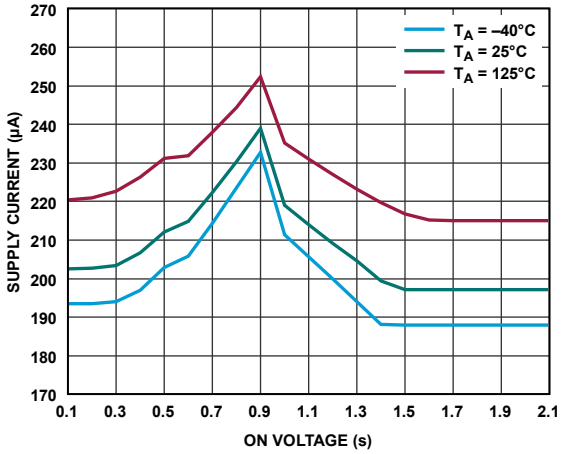


Figure 8. Supply Current vs. ON Voltage

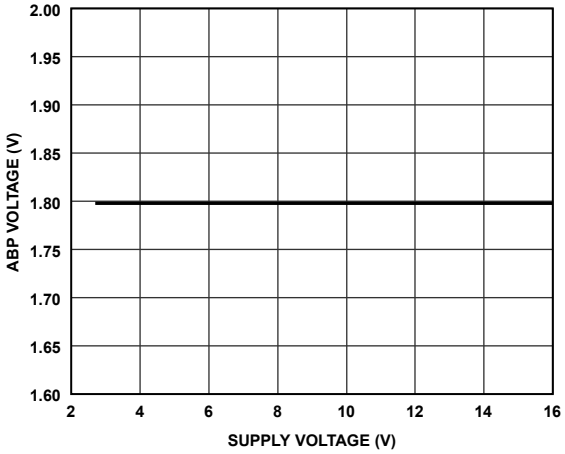


Figure 9. ABP Voltage vs. V_{DD} Supply Voltage

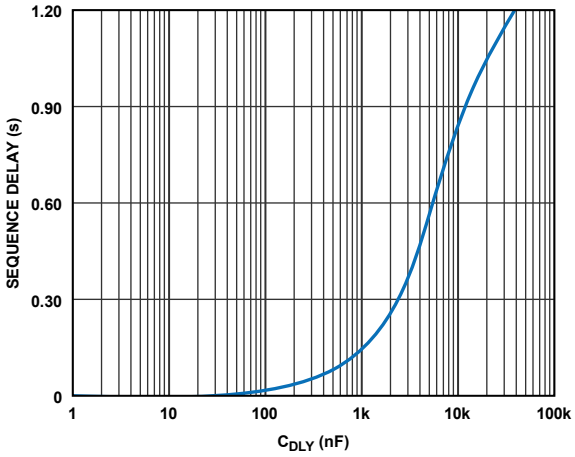


Figure 10. Sequence Delay vs. C_{DLY}

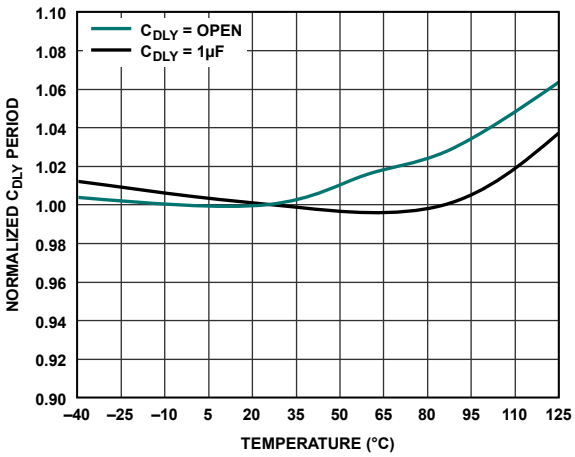


Figure 11. Normalized C_{DLY} Period vs. Temperature

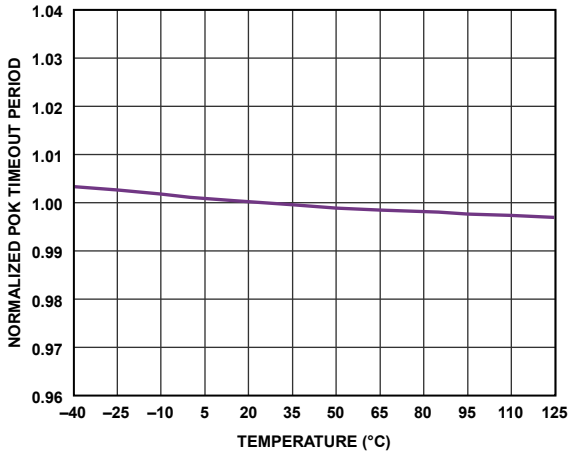


Figure 12. Normalized POK Timeout Period vs. Temperature

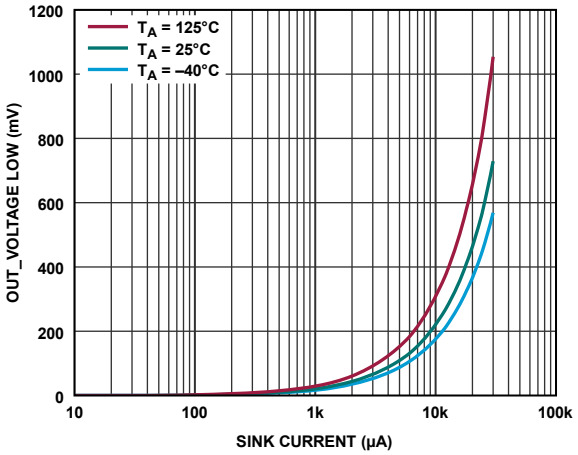


Figure 13. OUT_ Voltage Low vs. Sink Current

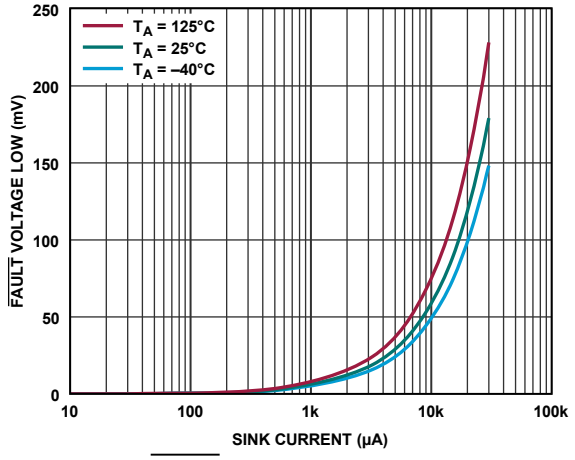


Figure 14. FAULT Voltage Low vs. Sink Current

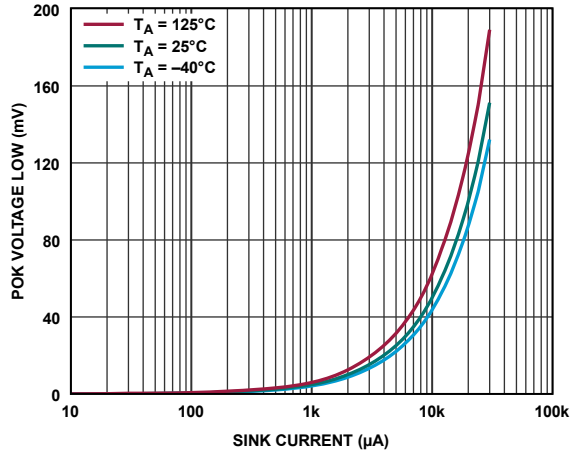


Figure 15. POK Voltage Low vs. Sink Current

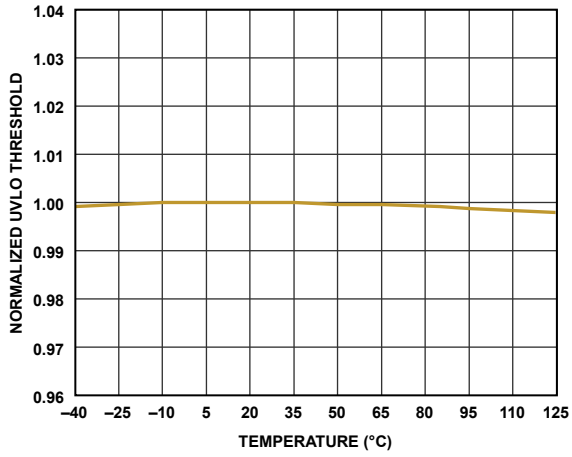


Figure 16. Normalized UVLO Threshold vs. Temperature

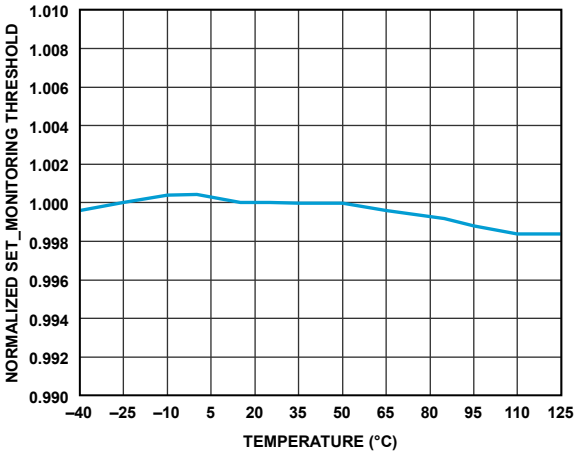


Figure 17. Normalized SET_ Monitoring vs. Temperature

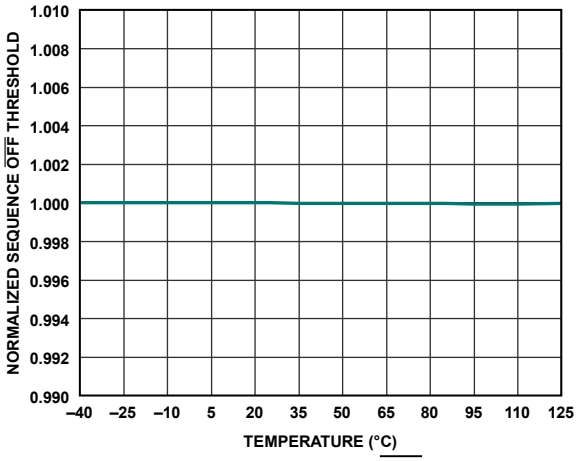


Figure 18. Normalized SET_ Sequence OFF vs. Temperature

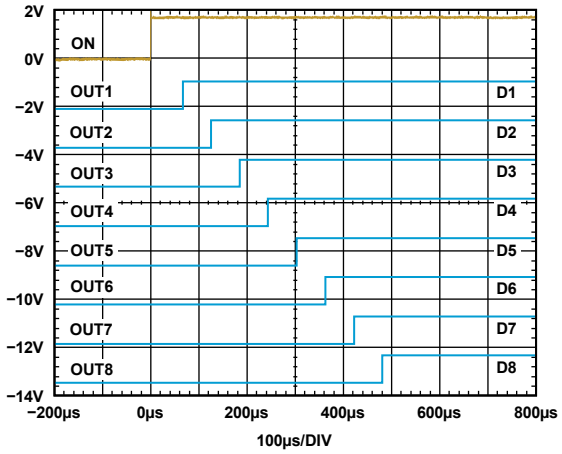


Figure 19. Power ON Sequence (C_{DLY} = OPEN)

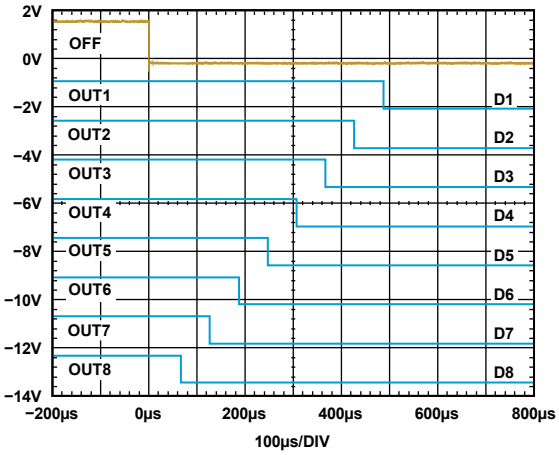


Figure 20. Power OFF Sequence (C_{DLY} = OPEN)

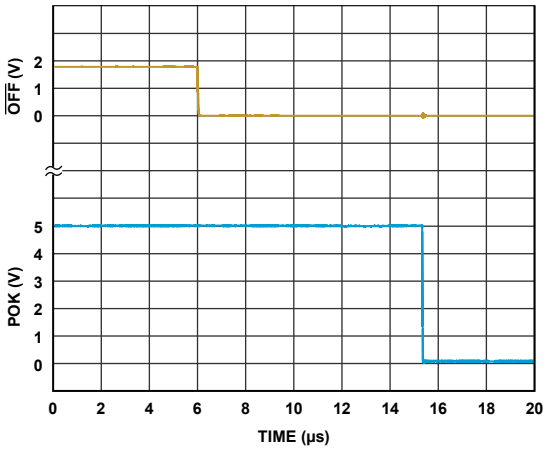


Figure 21. OFF to POK Delay

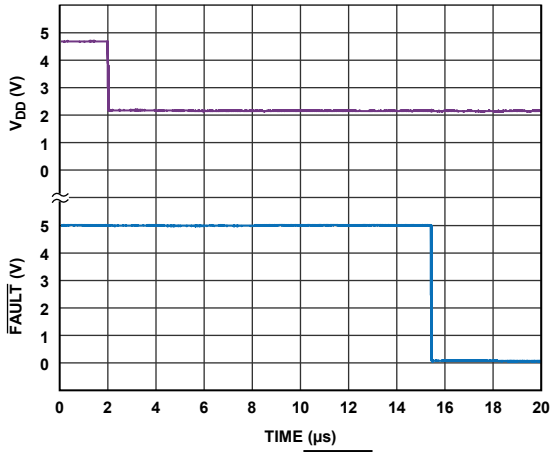


Figure 22. UVLO to FAULT Delay

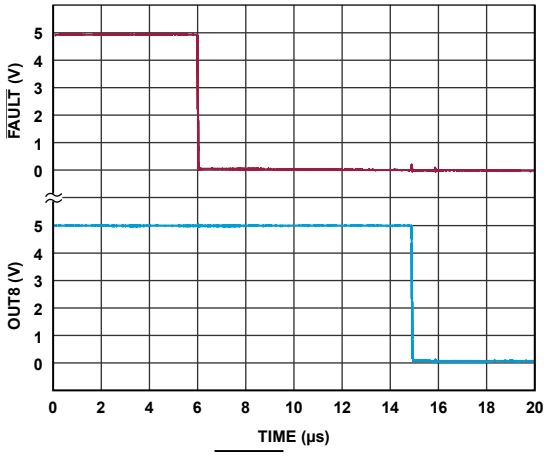


Figure 23. FAULT to OUT8 Delay

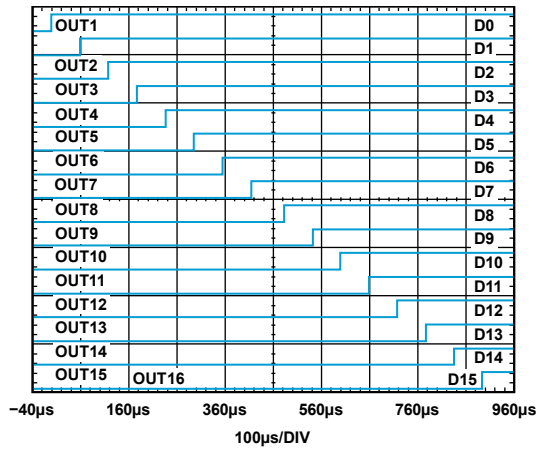


Figure 24. Daisy-Chaining Two Devices with ON Rising (C_{DLY} = OPEN)

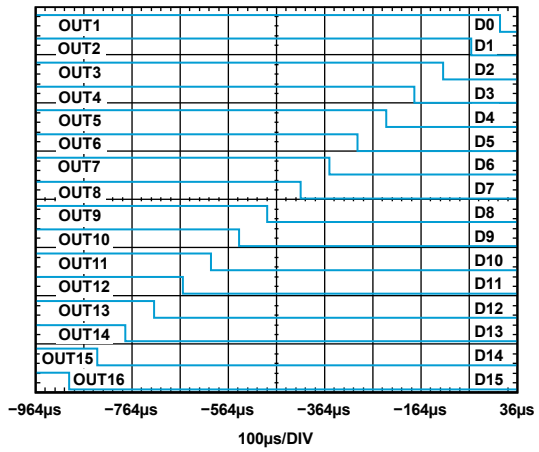


Figure 25. Daisy-Chaining Two Devices with $\overline{OFF}$ Falling (C_{DLY} = OPEN)

THEORY OF OPERATION

The ADM6840 enables six or eight power supplies when the sequencer turns on (rising edge in the ON pin) and disables the power supplies in reverse order when the sequencer turns off (Falling edge in $\overline{OFF}$ pin). The ADM6840 monitors each power supply once it is turned on.

When the sequencer initiates a power-on sequencing, the ADM6840 provides a capacitor-adjustable delay time (t_{DLY}) before the first output (OUT1) is enabled. After OUT1 is enabled, the ADM6840 monitors the enabled power supply voltage by feeding it back into the voltage-sensing input (SET1). If the voltage at SET1 reaches its power-on threshold voltage (V_{SEQON_TH} = V_{MON_TH} + $V_{MON\_TH\_HYS}$) within the factory-trimmable power-good timeout period (t_{PGT}), the sequencer waits for the delay time (t_{DLY}), and then enables the second output (OUT2). The power-on sequencing repeats until the last output channel is enabled and the last sensing input channel reaches its threshold. At this time, all SET_ thresholds are switched to the SET_ monitor threshold (V_{MON_TH}) with 0.8% accuracy, and power-on sequencing is complete. During power-on sequencing, the DONE output asserts high, and the power-OK (POK) outputs assert high after the reset timeout period (t_{RP}), allowing a system microcontroller (µC) to reset and begin operation.

The ADM6840 monitors each sequenced voltage feedback on SET_ after the respective channel is enabled. If any voltage falls below its V_{MON_TH}, the POK output asserts low, and all outputs are disabled simultaneously to turn off all sequenced power supplies. The device enters the fault condition and returns to the state machine's initialization phase, waiting for another power-on sequencing command.

When the sequencer initiates a power-off sequence, POK asserts low after a 10µs delay, and the ADM6840 waits the delay time (t_{DLY}) before disabling the last output channel. When the last sensing input channel voltage drops below its $\overline{OFF}$ threshold (V_{SEQOFF_TH}), the ADM6840 waits for the delay time (t_{DLY}), and then disables the next output. The power-off sequencing repeats until the first output channel is disabled. After SET1 reaches the V_{SEQOFF_TH}, the DONE output asserts low.

The ADM6840 can be cascaded to control a higher number of power supplies in a system. See the *Daisy-Chaining Capability* in the *Applications Information* section.

$\overline{FAULT}$ Input/Output

$\overline{FAULT}$ is bidirectional. It is an active-low input and active-low open-drain output. When an internal fault is detected, this pin is asserted low. An external signal pulling this pin low disables all outputs and sets the ADM6840 to a fault condition. See the *State Diagram* for all the conditions that assert a $\overline{FAULT}$. During any fault condition, except $\overline{UVLO}$ undervoltage detection, a one-shot pulse of pulse width 80µs (typ) is asserted. For multichip solutions, all the $\overline{FAULT}$ input/output can be connected. In case of a fault condition, all outputs on every device are turned off simultaneously.

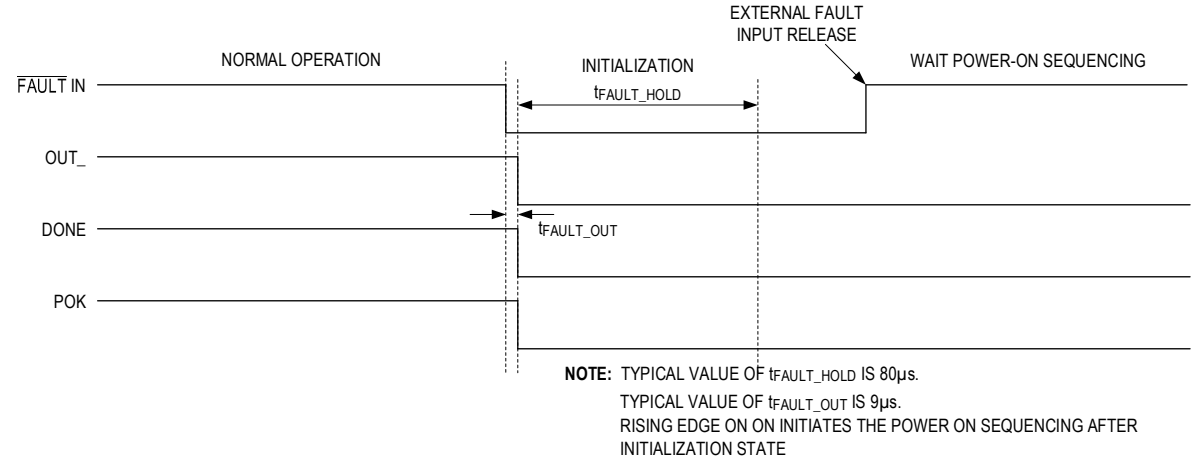


Figure 26. External Fault Response

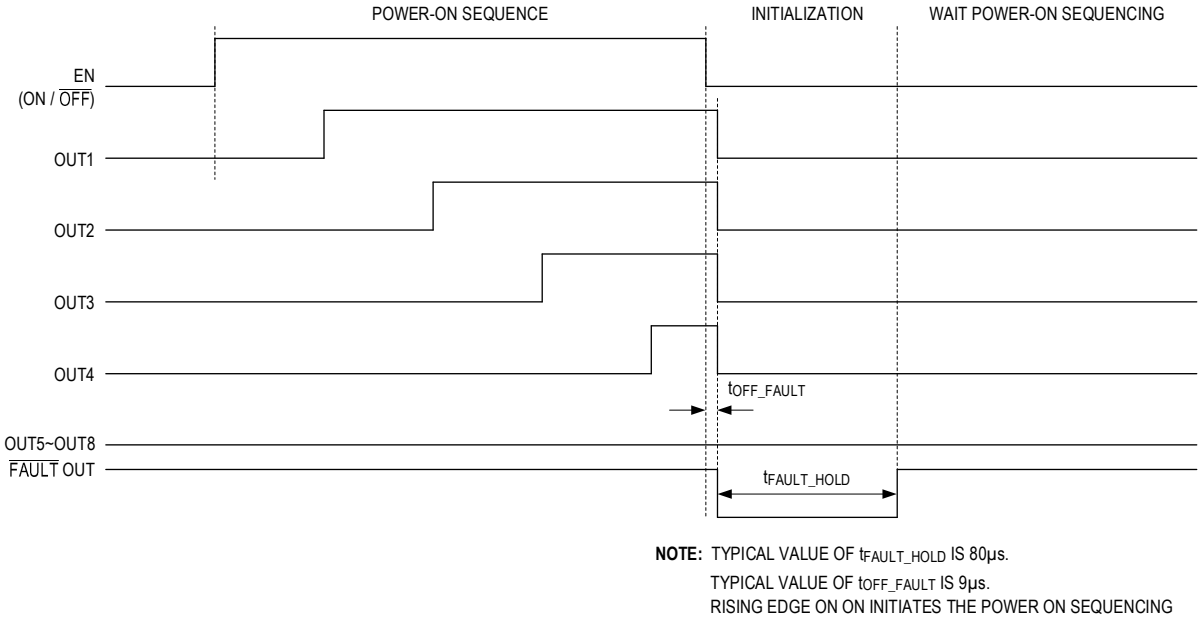


Figure 27. Internal Fault Response During Power-On Sequence ($\overline{OFF}$ goes from High to Low)

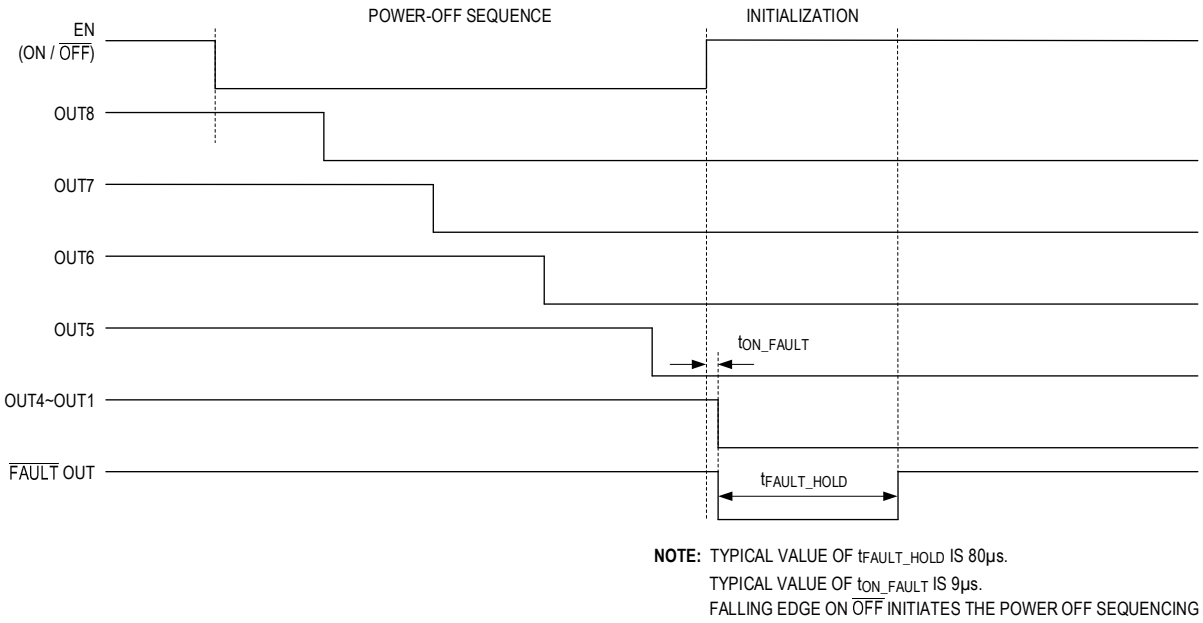


Figure 28. Internal Fault Response During Power-Off Sequence (ON goes from Low to High)

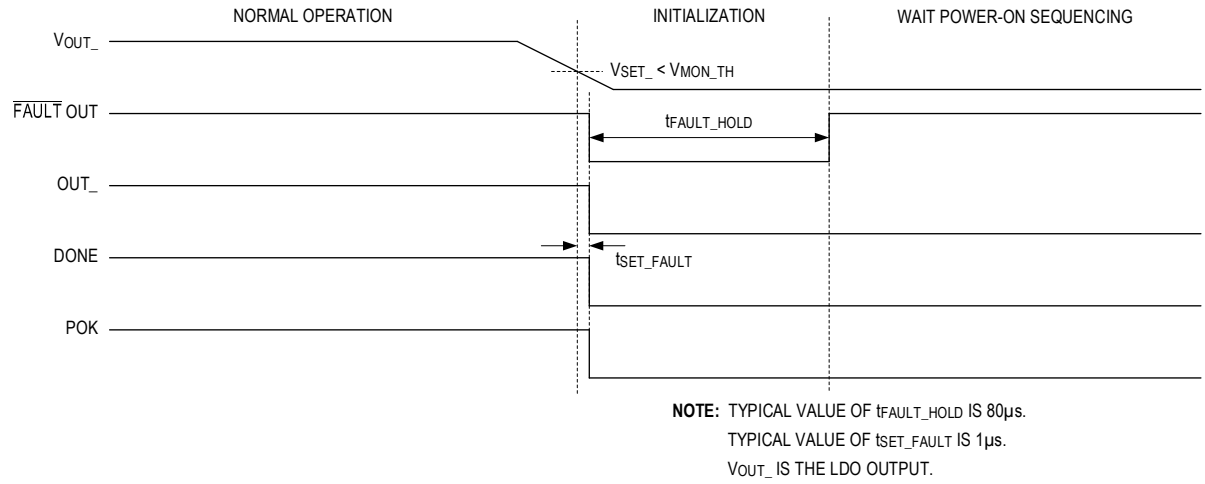


Figure 29. SET Fault Response

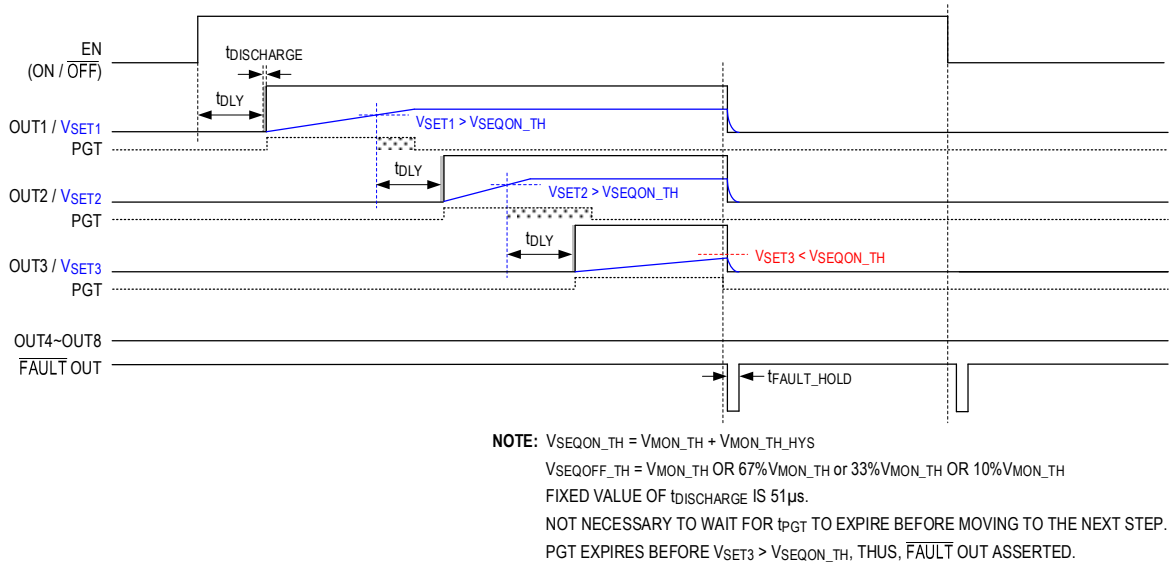


Figure 30. OUT and Fault Response during the Power-Good Timeout Period

Skip or Disable Channels

If fewer than eight channels are required, skip a channel by connecting the SET_ pin to the ABP pin. The sequencing is similar to eight-channel sequencing, just treat the ADM6840 like fewer channels. For example, if SET8 is connected to ABP, all logic for channel 8 is removed from the state machine, so there is no delay, no timer, no undervoltage detection, and no fault triggered from this channel. If all channels are skipped, the device asserts DONE and POK immediately after initialization.

Channel skipping decision is decided during the initialization phase after every fault condition. The ADM6840 checks for the respective SET_ voltage during the initialization phase. If the voltage at SET_ is above 0.5V, the corresponding channel gets skipped. Therefore, it is important to ensure the voltage at SET_ is below 0.5V after each fault condition. If the power supplies are not properly loaded, it can take a long time to discharge the channel SET_ voltage. This situation is more crucial when the threshold voltage levels are low, or the load current of the power supply is less.

ON and $\overline{\text{OFF}}$ Inputs

The ON and $\overline{\text{OFF}}$ inputs are edge-triggered inputs with a threshold of 0.5V, which are used to initiate power sequencing. If no fault condition persists, a rising edge on the ON input initiates power-on sequencing, while a falling edge on the $\overline{\text{OFF}}$ input initiates a power-off sequencing in the reverse order.

During the power-on sequence, when a falling edge is detected in the $\overline{\text{OFF}}$ pin, a $\overline{\text{FAULT}}$ is asserted, resulting in stopping the sequence and simultaneously turning off all the outputs, see *Figure 27.* To prevent a fault condition, no rising edge must be detected in the ON pin after the power-on sequence is completed or during normal operation.

During the power-off sequence, when a rising edge is detected in the ON pin, a $\overline{\text{FAULT}}$ is asserted, resulting in stopping the sequence and simultaneously turning off all the outputs, see *Figure 28*.

Normally, ON and $\overline{\text{OFF}}$ inputs are tied together or used separately in special cases such as daisy-chaining. See the *Daisy-Chaining Capability* in the *Applications Information* section.

DONE Output

During the power-on sequence, the DONE output asserts high after the last channel of the sequence is asserted. Skipped or disabled channel is being disregarded in this sequence. For example, when OUT8 is skipped, the DONE output asserts high after OUT7 is asserted.

During the power-off sequence, the DONE output asserts low after the first channel goes below the threshold voltage (V_{SEQOFF_TH}).

Power-OK (POK) Output

The POK reset timeout period (t_{RP}) has the following options: 20µs, 1ms, 5ms, 10ms, 20ms, 30ms, 50ms, 100ms, 200ms, 300ms, 500ms, 1000ms, or 2000ms.

The POK asserts high after all channels reach the power-on threshold voltage (V_{SEQON_TH}). When a channel goes below the monitoring threshold (V_{MON_TH}), POK asserts low and triggers the $\overline{FAULT}$.

The POK asserts low when there is a falling edge in the $\overline{OFF}$ input with a delay of around 10µs.

Power Good Timer (PGT)

The PGT is used to check a power supply's capability to reach its power-on threshold voltage (V_{SEQON_TH}) on SET_ within the factory-trimmed power-good timeout period (t_{PGT}).

The internal state machine should stop the PGT if SET_ voltage reaches 0.5V before the PGT expires. The ADM6840 does not have to wait for t_{PGT} to expire before moving to the next step. The $\overline{FAULT}$ output is asserted when any enabled voltage cannot reach its threshold on the SET_ pin within the t_{PGT}. The PGT is only for power-on sequencing and is not used during power-off sequencing, see *Figure 30*.

The PGT (t_{PGT}) has the following options: 20µs, 10ms, 50ms, 100ms, 500ms, or no PGT.

For no PGT, during the power-on sequence, there is no time limit on any power supply output to reach its threshold. The device waits until the SET_ pin goes above its threshold before asserting the corresponding OUT_. The POK reset timeout reuses the PGT timer.

State Diagram

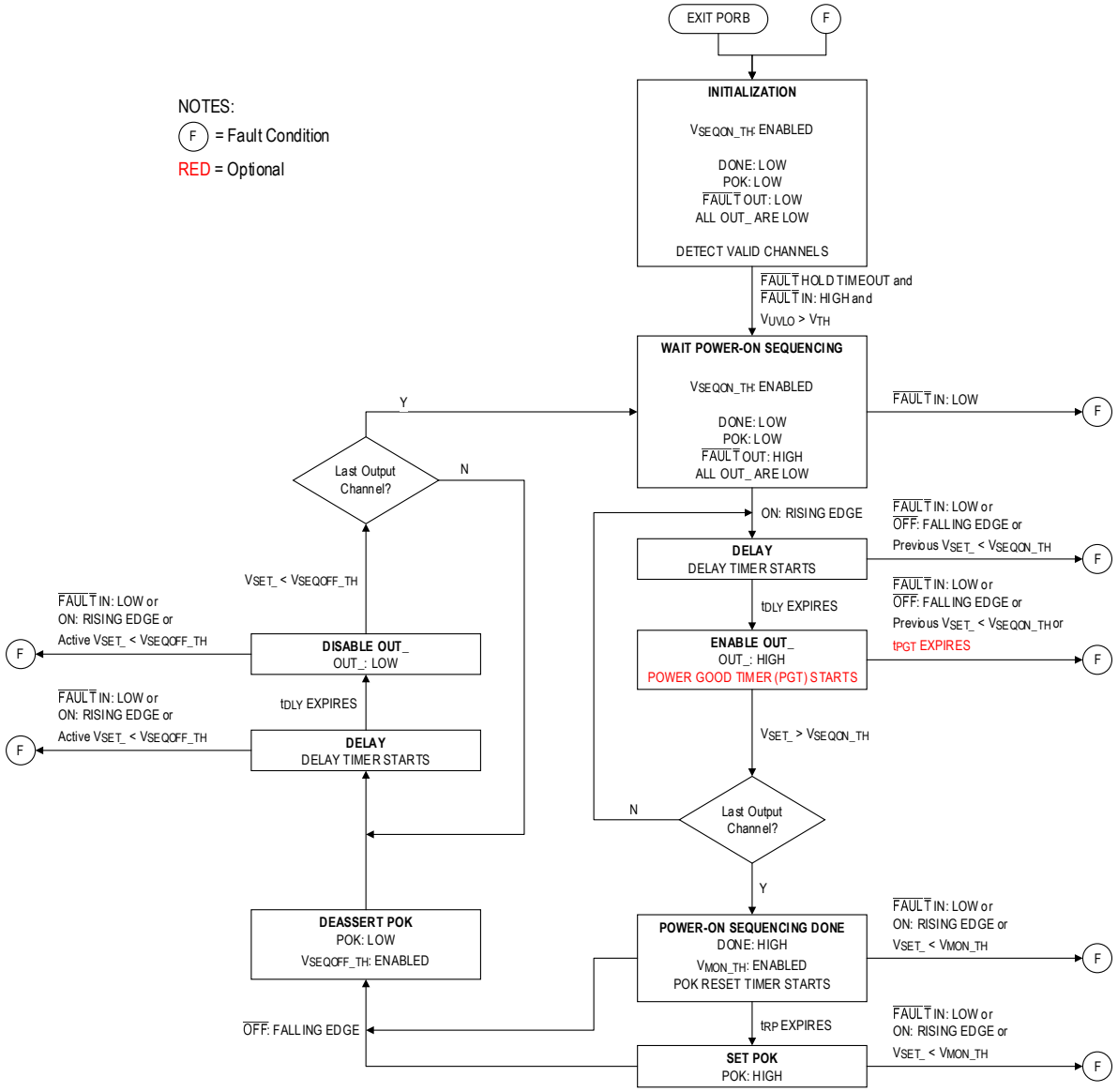


Figure 31. State Diagram

APPLICATIONS INFORMATION

Selecting SET_ Feedback Resistors

The ADM6840 features eight SET_ inputs, and the monitoring threshold voltage (V_{MON_TH}) at each SET_ input is 0.5V (typ). To monitor voltage V1, connect a resistive divider network to the circuit as shown in *Figure 32*. Use the following equation to calculate the monitored threshold voltage.

$$V1 = V_{MON\_TH} \times \left(1 + \frac{R1}{R2}\right)$$

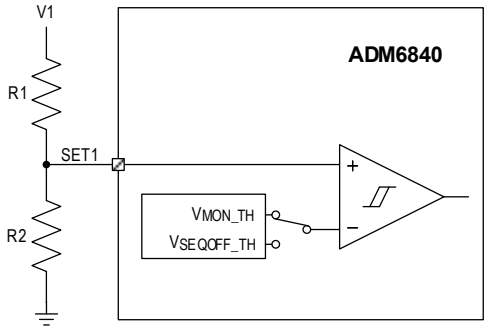


Figure 32. SET_ Pin Feedback Resistors

Balance accuracy and power dissipation when choosing the external resistors. The voltage monitor has a high-impedance input with a ±100nA leakage current. This leakage current contributes to the overall error in the threshold voltage, and the error is proportional to the resistor values used to set the threshold. Small, high-value resistors reduce error but increase power consumption. Use the following equation to estimate the value of the resistors based on the amount of acceptable error:

$$R1 = \frac{eA \times V1}{I_{SET}}$$

where eA is the fraction of the maximum acceptable absolute resistive divider error attributable to the input leakage current (use 0.01 for ±1%), V1 is the power-good threshold for the power supply being monitored, and I_{SET} is the worst-case SET_ input leakage current (see *Table 1*). Calculate R2 as follows:

$$R2 = \frac{V_{MON\_TH} \times R1}{V1 - V_{MON\_TH}}$$

The eA error adds to any errors caused by the resistive voltage divider.

For the power-off threshold implementation, after POK asserts low, reverse power sequencing starts, and the comparator reference voltage changes to V_{SEQOFF_TH}.

V_{SEQOFF_TH} has the following options: V_{MON_TH}, 67%V_{MON_TH}, 33%V_{MON_TH}, 10%V_{MON_TH}

Sequence Delay Time

When the power-on sequence starts, the sequence delay time input (DLY) has an internal switch in series with an internal current source of 4µA, connected to the C_{DLY} present at the DLY pin. The current charges the C_{DLY} linearly until the voltage reaches the threshold of 0.5V, and signals to continue enabling the subsequent channel. Connect a capacitor (C_{DLY}) between DLY and GND to adjust the sequencing delay period (t_{DLY}) that occurs between sequenced channels. Use the following formula to estimate the delay:

$$t_{DLY} = 125k\Omega \times C_{DLY}$$

where t_{DLY} is in seconds, and C_{DLY} is in Farads. Leave DLY unconnected for the minimum 58µs (typ) delay. After each t_{DLY}, the DLY capacitor discharges (internal 4Ω) with a typical 51µs ($t_{DISCHARGE}$), as shown in *Figure 33*. The accuracy of the t_{DLY} is affected by the C_{DLY} capacitor leakage and tolerance. A low-leakage ceramic capacitor is recommended.

For a discharge time of 51µs, accurate estimation of sequence delays up to 500ms using the provided formula requires limiting the external capacitor to at most 4µF. Exceeding this capacitance may result in timing deviations from the calculated delay, as shown in *Figure 10.* Therefore, other $t_{DISCHARGE}$ options may be considered. Note that this recommendation applies only to the *Sequence Eight Power Supplies without Monitoring* use case.

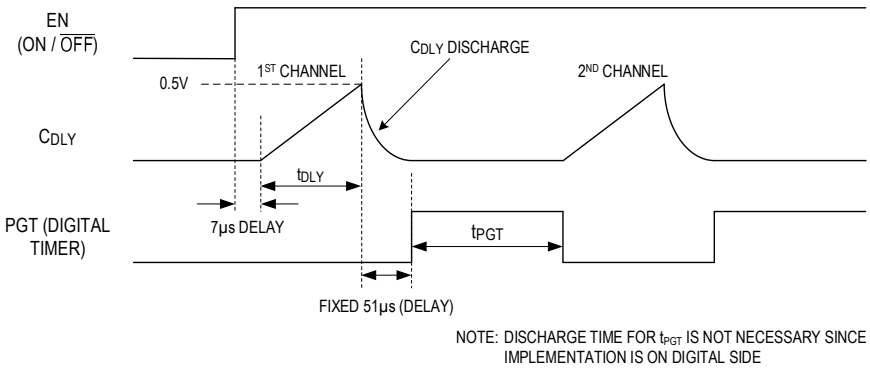


Figure 33. Sequence Delay Timing and Discharge Time

Pullup Resistor Values

The exact value of the pullup resistors for the open-drain outputs is not critical, but some consideration should be made to ensure the proper logic levels when the device is sinking current. For example, if V_{DD} = 3.3V and the pullup voltage is 5V, keep the sink current less than 3.2mA, as shown in *Table 1*. As a result, the pullup resistor should be greater than 1.6kΩ. For a 12V pullup, the resistor should be larger than 3.74kΩ.

Daisy-Chaining the ADM6840

Multiple ADM6840 devices can be daisy-chained to sequence and monitor a large number of voltages. When a fault occurs on any of the monitored inputs, $\overline{FAULT}$ goes low which signals a fast power-down. Connect all $\overline{FAULT}$ pins of the ADM6840 together to ensure that all power supplies are turned off during a fault. *Figure 39* shows an example of two daisy-chained devices.

Layout and Bypassing

For better noise immunity, bypass V_{DD} to GND with a 0.1µF capacitor installed as close to the device as possible. Bypass ABP to GND with a 0.1µF capacitor installed as close to the device as possible. Minimize stray capacitance on the SET_ inputs. The layout of the divider resistors should be as close to the ADM6840 as possible. Connect the exposed pad (EP) to the ground plane for improved heat dissipation. Do not use EP as the only ground connection.

ORDERING GUIDE

MODEL	TEMPERATURE RANGE	PACKAGE DESCRIPTION	PACKAGE OPTION
ADM6840EAWABFH+T	-40°C to +125°C	25-BUMP WLP (2.46mm x 2.46mm)	W252Y2+1

+Denotes a lead(Pb)-free/RoHS-compliant package

T = Tape and reel

SELECTOR GUIDE

The ADM6840 includes different variants or device options; however, not all options are released for sale. Released variants are called standard models and are listed in the *Ordering Guide*. For the most up-to-date list of standard models, refer to the product page's *Sample and Buy* section. Contact an Analog Devices representative for information on nonstandard models, and be aware that samples and production units may have long lead times.

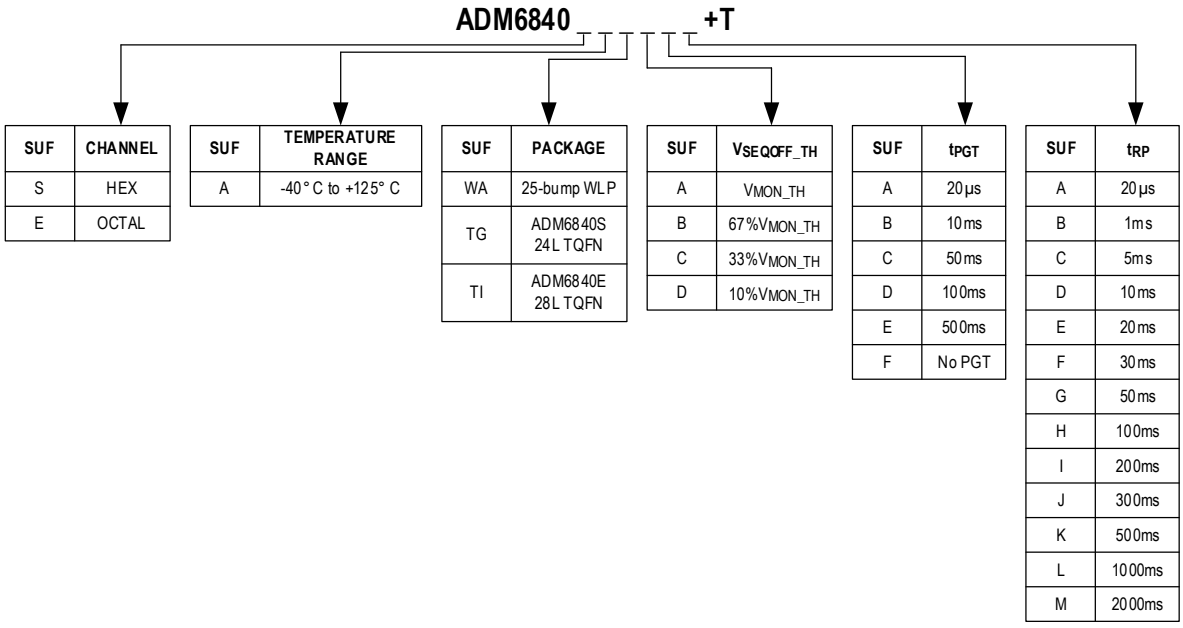


Figure 34. Selector Guide

USE CASES

Sequence and Monitor Eight Power Supplies

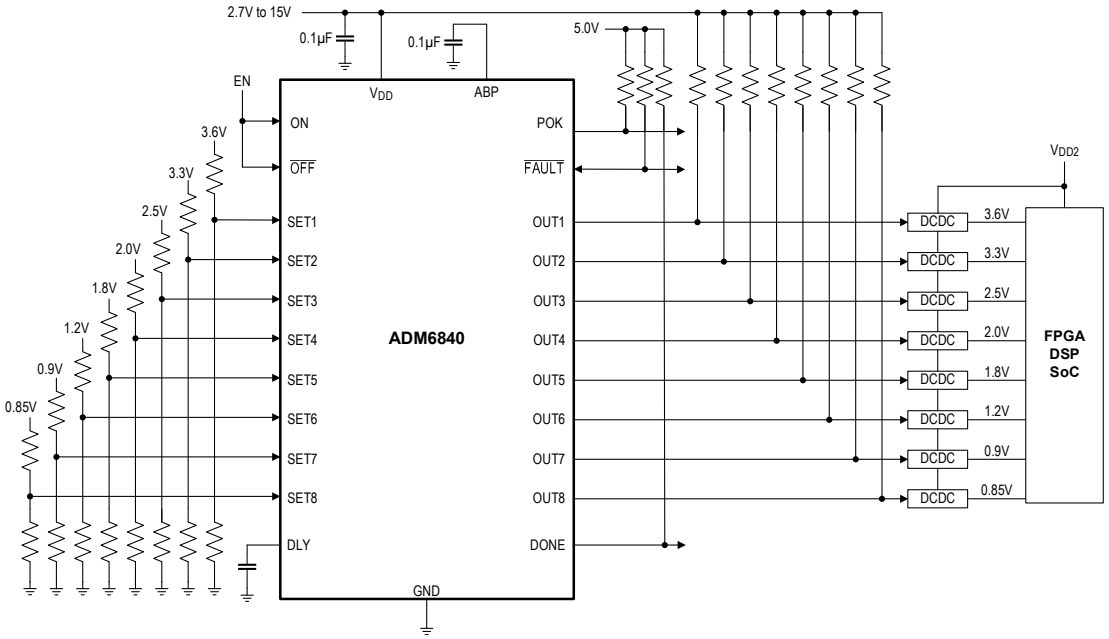


Figure 35. Sequence and Monitor Eight Power Supplies Circuit

Sequence Eight Power Supplies without Monitoring

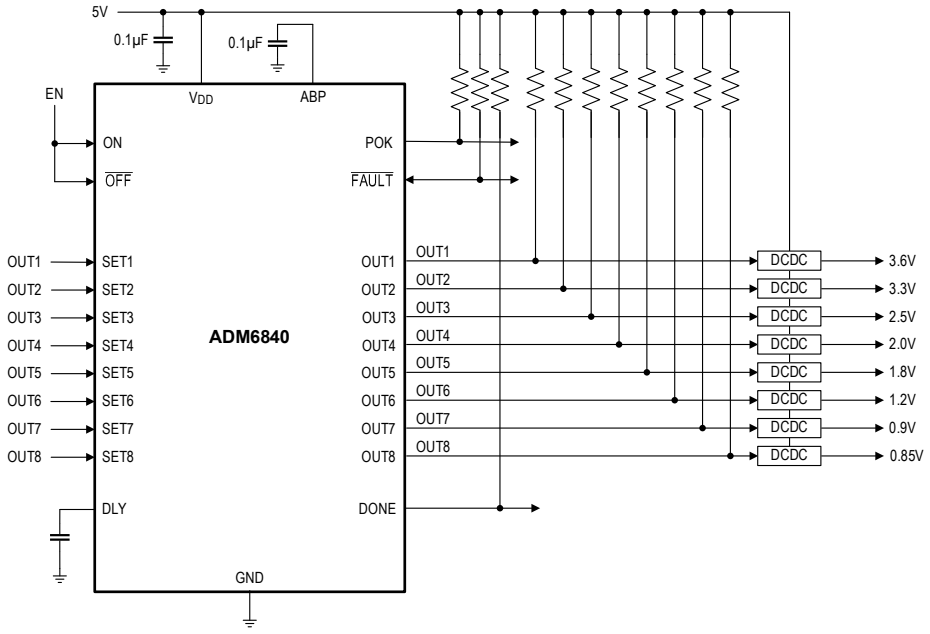


Figure 36. Sequence Eight Power Supplies without Monitoring Circuit

Sequence Eight Power Supplies and Monitor Power-Good/Power-OK Outputs

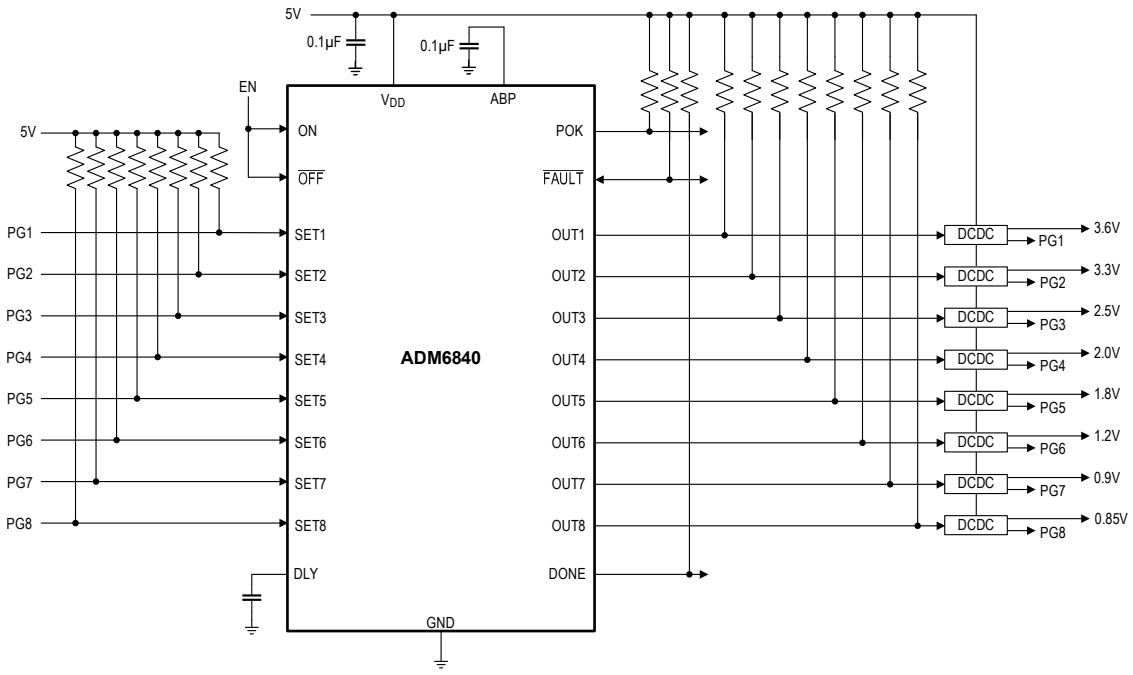


Figure 37. Sequence Eight Power Supplies and Monitor Power-Good Outputs Circuit

Sequence and Monitor Power Supplies with Disabled/Skipped Channel

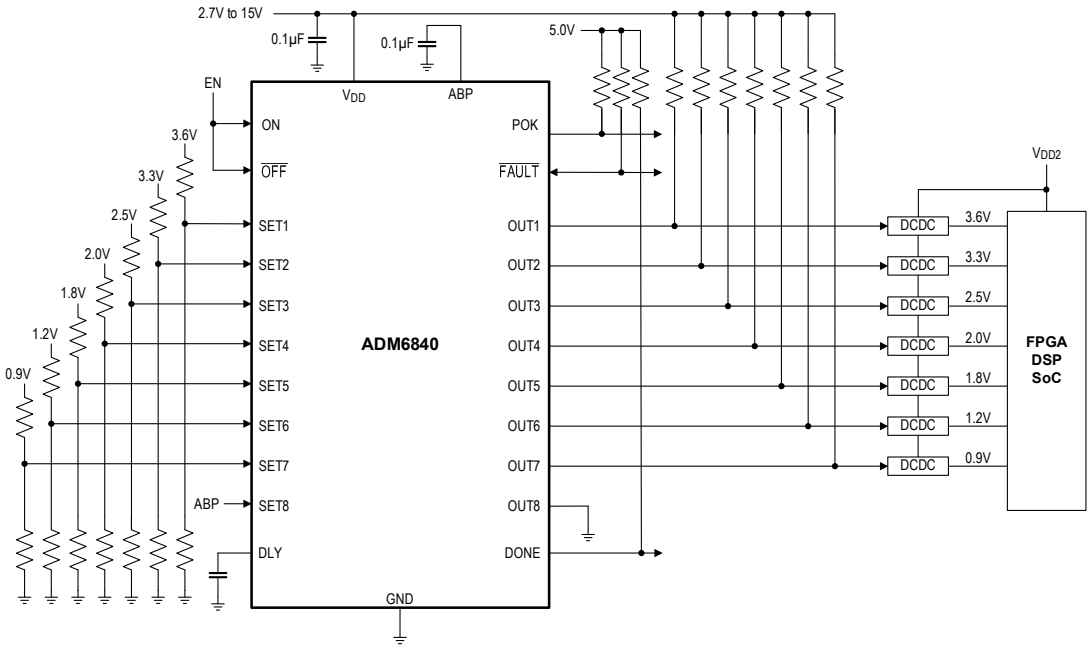


Figure 38. Sequence and Monitor Power Supplies with Disabled/Skipped Channel Circuit

Daisy-Chaining Capability

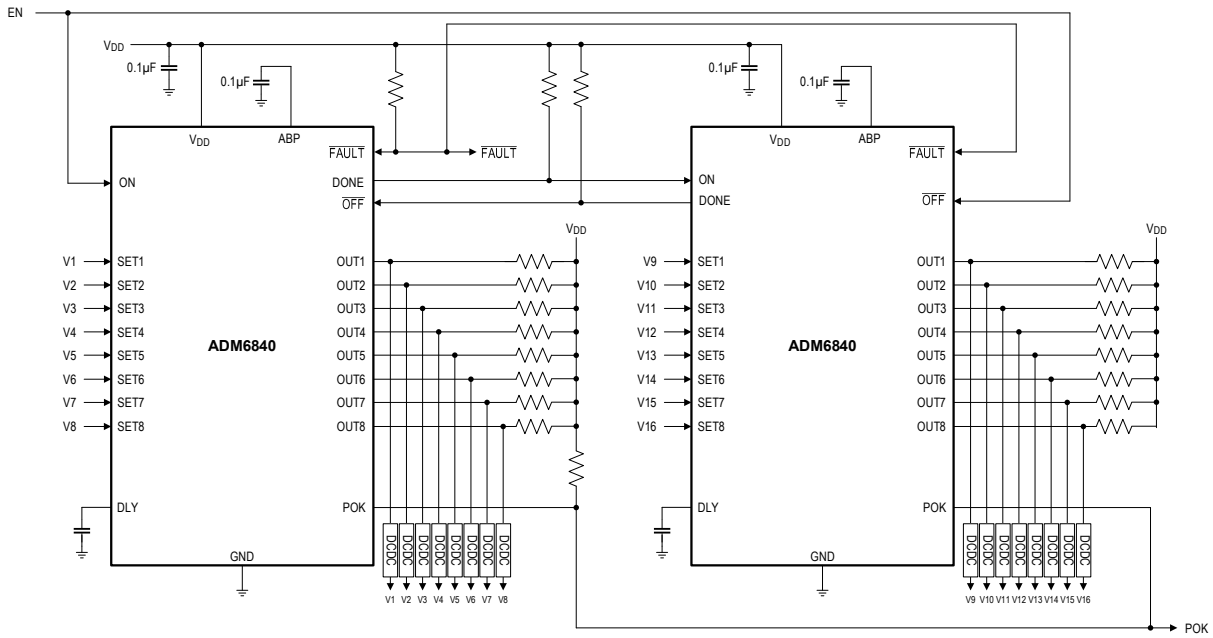


Figure 39. Daisy-Chaining using Multiple ADM6840 Circuits